THE UNIVERSITY OF TEXAS AT DALLAS

Erik Jonsson School of Engineering
and Computer Science

Amplifier Sizing Analysis

by

James R. Hellums, Ph.D.

Design Procedure for 2 Stage Amp

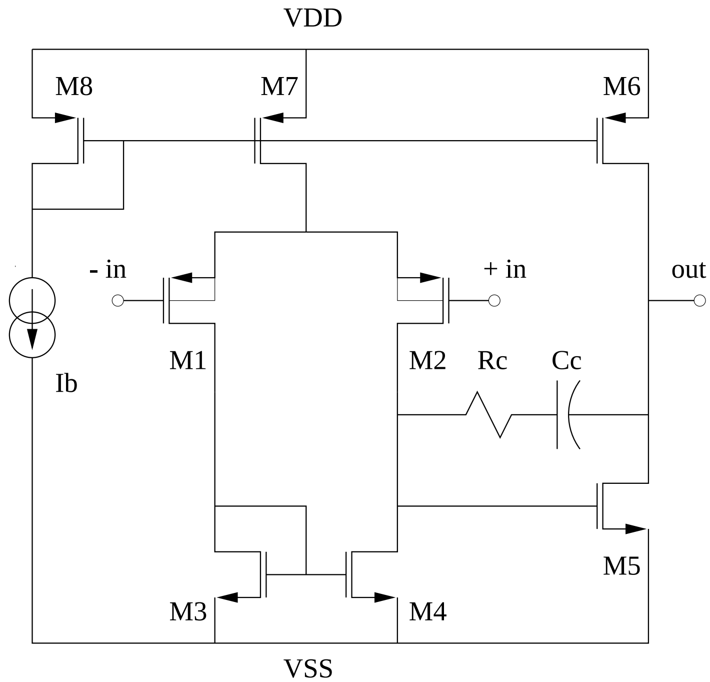


Figure 1: Two stage CMOS transconductance amplifier with PMOS inputs

1 Design Specs for a Two-Stage TC Amp

The following design equations and specs must be met simultaneously driving a load capacitor, $C_L = 10\text{pF}$. The total current for the amplifier must be less than $200\mu\text{A}$ counting the bias, $I_b = 10\mu\text{A}$, flowing through M_8.

$$|A_v| = \left(\frac{g_{m_2}}{g_{ds_2} + g_{ds_4}}\right)\left(\frac{g_{m_5}}{g_{ds_5} + g_{ds_6}}\right) \geq 90\text{dB} \tag{1}$$

$$\omega_u = \left(\frac{g_{m_2}}{C_c}\right) \geq 2\pi \cdot 6\text{MHz} \tag{2}$$

$$SR_{input} = \frac{dV_o}{dt} = \frac{I_7}{C_c} = \frac{2I_2}{C_c} = \frac{2I_2\,\omega_u}{g_{m_2}} \geq 6\text{V}/\mu\text{s} \tag{3}$$

$$SR_{output} = \frac{dV_o}{dt} = \frac{I_6}{C_L + C_c} > SR_{input} \tag{4}$$

For the 4V$_{pp}$ output voltage swing spec, the output devices must meet the following conditions:

$$V_{dsat_6} \simeq V_{gst_6} = \sqrt{\frac{2I_6}{\mu_p C_o S_6}} < 0.5\text{V} \tag{5}$$

$$V_{dsat_5} \simeq V_{gst_5} = \sqrt{\frac{2I_5}{\mu_n C_o S_5}} < 0.5\text{V} \tag{6}$$

The compensation network will be used to put the right half plane (RHP) zero at ∞ with $R_c = 1/g_{m_5}$. Therefore, our engineering approximation says only 4 poles remain in the LHP. Magnitudes of these poles are:

$$|p_1| \cong \frac{g_{m_2}}{A_v C_c} \tag{7}$$

$$|p_2| \cong \frac{g_{m_5} C_c}{C_1 C_c + C_1 C_L + C_c C_L} \simeq \frac{g_{m_5}}{C_L} \tag{8}$$

$$|p_3| \cong \frac{1}{R_c C_1} \simeq \frac{g_{m_5}}{C_{g_5}} \simeq \omega_{T_5} \tag{9}$$

$$|p_4| \cong \frac{g_{m_3}}{C_{g_3} + C_{g_4}} \simeq \frac{g_{m_3}}{2C_{gs_3}} \simeq \frac{\omega_{T_3}}{2} \tag{10}$$

where p_4 is the mirror pole, $C_1 \cong C_{g_5} + C_{db_2} + C_{db_4}$, and C_g is all MOS capacitance from the gate to AC ground. Note: we do not know apriori whether p_3 or p_4 is actual the lower frequency pole. However since $\omega_T = 2\pi f_T$ is the transition frequency, it is possible that the mirror pole is at a lower frequency.

With the 4-pole approximation, the phase margin (PM) equation can be written as:

$$PM = 180^\circ - \tan^{-1}\frac{\omega_u}{|p_1|} - \tan^{-1}\frac{\omega_u}{|p_2|} - \tan^{-1}\frac{\omega_u}{|p_3|} - \tan^{-1}\frac{\omega_u}{|p_4|} \tag{11}$$

Note that $\omega_u/|p_1| \simeq A_v$ which is a very large number. The arctan of a very large number is aproximately 90°. Also we want to design the amp so that it has a 2-pole-like settling which will require that the magnitude of the third pole be $|p_3| \geq 10\omega_u$ and fourth pole be $|p_4| \geq 20\omega_u$. Substituting arctan(0.1)=5.71° and arctan(0.2)=2.86°, so the total phase shift from these 2 non-dominate poles is 8.57°. Now the phase margin in equation (11) becomes

$$PM = 81.43^\circ - \tan^{-1}\frac{\omega_u}{|p_2|} \tag{12}$$

For a phase margin of 60° equation (12) can be solved to give the magnitude of the second pole.

$$|p_2| = \frac{\omega_u}{\tan 21.43^\circ} = 2.548\,\omega_u \tag{13}$$

Now equating (8) and (13) we can get an equation for g_{m_5}.

$$g_{m_5} \geq 2.548\,\omega_u C_L = 2.548 \cdot 2\pi \cdot 6 \cdot 10^6 \cdot 10 \cdot 10^{-12} = 960.0\mu\mho \tag{14}$$

If we have the 4 poles with the magnitudes described above, then the gain margin (GM) can be approximated by the following mathematics. The GM is the difference in the magnitude of the voltage gain from 0dB to the gain at the frequency when the phase shift is −180°. The dominant pole accounts for −90° of phase so that the remaining −90° is:

$$\phi_{shift} = \tan^{-1}\frac{\omega}{|p_2|} + \tan^{-1}\frac{\omega}{|p_3|} + \tan^{-1}\frac{\omega}{|p_4|} \tag{15}$$

After substitution into (15) for the values of the phase shift and pole magnitudes yields:

$$\frac{\pi}{2} = \tan^{-1}\frac{\omega}{2.548\,\omega_u} + \tan^{-1}\frac{\omega}{10\,\omega_u} + \tan^{-1}\frac{\omega}{20\,\omega_u} \tag{16}$$

Solving for ω requires series expansion approximations of the arctan function. Also, some apriori knowledge is needed about the value of ω. Doing quick graphical or numerical work shows the frequency ω is between the non-dominant poles p_2 and p_3, thus, two different series expansions are needed for the arctan functions. Dropping all higher order terms leads to the next equation:

$$\frac{\pi}{2} = \frac{\pi}{2} - \frac{2.548\,\omega_u}{\omega} + \frac{\omega}{10\,\omega_u} + \frac{\omega}{20\,\omega_u} \tag{17}$$

Solving for the frequency gives $\omega = 4.121\,\omega_u$. Now the GM can be calculated by:

$$GM = 0\text{dB} - 20\log_{10}\left[\frac{A_v}{\sqrt{1+\frac{\omega_\pi^2}{|p_1|^2}}\sqrt{1+\frac{\omega_\pi^2}{|p_2|^2}}\sqrt{1+\frac{\omega_\pi^2}{|p_3|^2}}\sqrt{1+\frac{\omega_\pi^2}{|p_4|^2}}}\right] \tag{18}$$

Remember that $|p_1| = \omega_u/A_v$, $|p_2| = 2.548\,\omega_u$, $|p_3| = 10\,\omega_u$ and $|p_4| = 20\,\omega_u$ so the frequency that we get -180° phase shift at is $\omega_\pi = 4.121\,\omega_u$. After substitution:

$$GM = 0\text{dB} - 20\log_{10}\left[\frac{A_v}{\sqrt{1+\frac{16.99\omega_u^2 A_v^2}{\omega_u^2}}\sqrt{1+\frac{16.99\omega_u^2}{6.492\omega_u^2}}\sqrt{1+\frac{16.99\omega_u^2}{100\omega_u^2}}\sqrt{1+\frac{16.99\omega_u^2}{400\omega_u^2}}}\right]$$

$$GM \simeq 0\text{dB} - 20\log_{10}\left[\frac{1}{\sqrt{16.99}\sqrt{3.617}\sqrt{1.1699}\sqrt{1.0425}}\right]$$

$$GM \simeq 0\text{dB} - 20\log_{10}\left[\frac{1}{9.561}\right]$$

$$GM \simeq 0\text{dB} - (-19.61\text{dB})$$

So GM = 19.61 dB which means that, if we meet the PM of 60°, we then meet the GM of 15 dB as well.

Now that we have gone through all the design equations and specs we have to start combining different conditions to determine the device sizes. Since the maximum total current is given, all we can do is decide how to partition it between branches. To get an idea about this, we should look at the input slew rate to output slew rate equations and the unity gain frequency to second pole equations:

$$\frac{I_6}{C_L + C_c} > \frac{I_7}{C_c} \Rightarrow \frac{I_6}{I_7} > 1 + \frac{C_L}{C_c} \tag{19}$$

From equation (13):

$$|p_2| \geq 2.548\,\omega_u \Rightarrow \frac{g_{m_5}}{C_L} \geq \frac{g_{m_2}}{C_c} \Rightarrow \frac{g_{m_5}}{g_{m_2}} \geq 2.548\frac{C_L}{C_c} \tag{20}$$

Both of these equations suggest that, if C_c is smaller than C_L, then the current in the second gain stage must be larger than the first (otherwise, the specs cannot be met!) Also, as an aside, the only free parameter left in this design is the choice of the value of C_c. No single specification sets the compensation capacitor size and, in fact, if it is set arbitrarily then it may be impossible to meet all the specs given for a particular ampifier. You must be free to adjust C_c to simultaneously meet the specifications. No noise spec was given for this design example, but the compensation capacitor can play a major role in meeting noise specs.

Now we will choose a value for the compensation capacitor, $C_c = 4$pF and with C_L given as 10pF we can start determining design values. From equation (19), the ratio I_6/I_7 must be greater than 3.5 and from equation (20), the ratio g_{m_5}/g_{m_2} must be greater than 6.37. Since the maximum current is $\sim 200\mu$A, with 10μA used in the bias, that leaves 190μA to split between I_6 and I_7. Remember, for low systematic offsets, we need to match the current mirrors in the amp (*i.e.* $M_6 - M_7 - M_8$). This means an integer ratio of currents. Choose $I_6 = 5I_7$ so that $I_7 = 30\mu$A and $I_6 = 150\mu$A. Now that we set C_c

and I_7, have we met the input slew rate spec? Substituting into equation (3) ideally the input slew rate will be 7.5V/μs. That is good enough.

We can go in any order to determine transistor sizes. There is no required or special way, just whatever you like. I will work on the input devices first. The transconductance appears in the first 3 equations, and we must find the case that gives the largest value and use it. The way I usually proceed is to combine equations (2) and (3) to get the next equation:

$$S_2 = \frac{C_c\,\omega_u^2}{\mu_p C_o\,SR_{in}} = 49.87 \tag{21}$$

which after substitution of the spec values into equation (21) and assuming $\mu_p C_o = 19\mu\text{A/V}^2$ we find a value for S_2, we will use $S_2 = 50$. We will use the gain equation to help determine the length of M_2 and M_4. You can split the total voltage gain up equally between the two stages but, from past experience, it is easier to get a little more gain in the second stage. So I will give it $\sim$ 47dB, leaving the remainder for the input. Modifying equation (1) for the first stage gain yields:

$$|A_{v_1}| = \left(\frac{\sqrt{2\mu_p C_o S_2}}{(\lambda_p + \lambda_n)\sqrt{I_2}}\right) \simeq 43\text{dB} \tag{22}$$

The only variables we don't know are the λ's, so we solve for them and get $(\lambda_p + \lambda_n)$=0.0797. From the BSIM3 SPICE model I found that 4μm P-channel devices had a λ_p=0.0209 and that 3μm N-channel devices had a λ_n=0.0564. The sum is 0.0773. Now we have the length of the input devices and the NMOS loads. The input pair initial size is set to $W_1/L_1 = W_2/L_2 =$ 200μm/4μm.

Next we will consider the tail current source length. The usual condition used to calculate L_7 is the $CMRR \simeq 2g_{m_2}r_{ds_7}$. Since g_{m_2} has been determined, we just need a spec for $CMRR$. The default spec is 60dB which gives a value for $g_{ds_7} = 0.338\mu\mho$. The λ_p can be found by dividing by I_7, which is 0.0113. From SPICE with the BSIM3 model, a 6μm P-channel has a $\lambda_p = 0.0128$, which is fairly close. So $L_6 = L_7 = L_8 = 6\mu$m. The W's are set by the output swing from equation (5). Since we want some margin in the design, we will set $V_{gst_6} = 0.4$V. Then $S_6 = 98.68$ and $W_6 = 592.1$. I will make $W_6 = 600\mu$m because I need integer ratios for W_7 and W_8. The current ratios set $W_7 = 120\mu$m and $W_8 = 40\mu$m.

The W's of the loads will be determined by the ratio with M_5 to meet low systematic offset (i.e. $S_4 = (I_4/I_5)S_5$). For the best design the length of M_5 should be made equal to M_3 and M_4. This will give the best matching and therefore systematic offset, but this is not a requirement. I will choose to make $L_5 = 3\mu$m. I am looking ahead at the third pole location, equation (9). We wanted it to be greater than $10\,\omega_u$, and we need $C_{g_5} \propto GateArea$ to not get very large. Therefore we want to use the shortest length we can and still meet the gain. W_5 will be set by the following condition that yields the largest value: the output swing equation (6), the second pole which gave a value for g_{m_5} spec from equation (14) or the voltage gain of the second stage. If we set the swing equation equal to 0.4V then $W_5 = 114.8$. From equation (14), $W_5 = 188.1$. Rearranging the gain equation gives:

$$|A_{v_2}| = \left(\frac{\sqrt{2\mu_n C_o S_5}}{(\lambda_n + \lambda_p)\sqrt{I_6}} \right) \simeq 47\text{dB} = 223.87 \qquad (23)$$

Solving for W_5 yields:

$$W_5 = \frac{(223.87)^2(\lambda_n + \lambda_p)^2 I_6 L_5}{2\mu_n C_o} \qquad (24)$$

The $(\lambda_{n_5} + \lambda_{p_6}) = 0.0475 + 0.0103 = 0.0578$ is found from SPICE. Assuming $\mu_n C_o = 49\mu\text{A/V}^2$ then, $W_5 = 768.8$, so I will use $W_5 = 750\mu$m for matching reasons. This makes $W_3 = W_4 = 75\mu$m from the current ratio between the input stage and output stage (i.e. $I_5/I_4 = 10$). With the second stage driver device size set the compensation resistor R_c can be calculated. We have designed the amp assuming that the zero will be at ∞ so $R_c = 1/g_{m_5} \simeq 522\Omega$. I will use 600Ω to ensure the zero is not in the RHP.

The initial design is complete, the component values for the amplifier are:

$$M_1 = M_2 = \frac{200\ \mu\text{m}}{4\ \mu\text{m}}$$
$$M_3 = M_4 = \frac{75\ \mu\text{m}}{3\ \mu\text{m}}$$
$$M_5 = \frac{750\ \mu\text{m}}{3\ \mu\text{m}}$$
$$M_6 = \frac{600\ \mu\text{m}}{6\ \mu\text{m}}$$
$$M_7 = \frac{120\ \mu\text{m}}{6\ \mu\text{m}}$$
$$M_8 = \frac{40\ \mu\text{m}}{6\ \mu\text{m}}$$
$$R_c = 600\ \Omega$$
$$C_c = 4\ \text{pF}$$

We now run SPICE. The results from the AC simulation are:

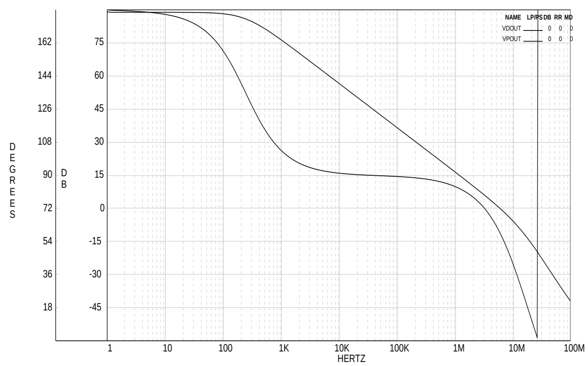
$$A_v = 89.10\ \text{dB}$$
$$f_u = 5.934\ \text{MHz}$$
$$PM = 60.52^\circ$$
$$GM = 20.64\ \text{dB}$$

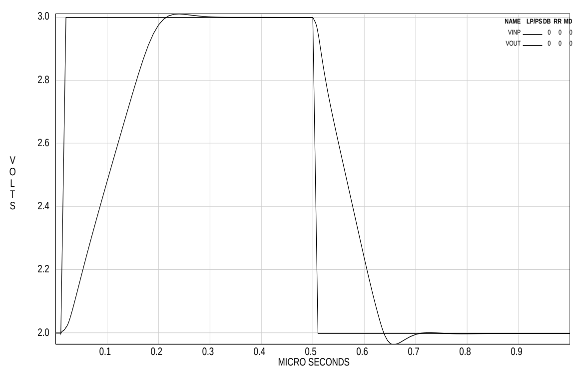
and you can see we are low on gain and bandwidth. It turns out that the third lowest value pole was actually the mirror pole p_4 which is at 59.85 MHz (9.975 ω_u). The largest value (farthest out) pole is p_3 which is at 96.06 MHz (16 ω_u). Our quess of poles at 10 ω_u and 20 ω_u was close even though we got the order wrong. The transient step simulation gives the input slew rate:

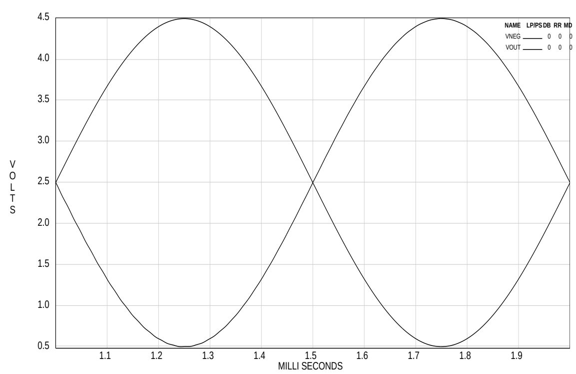
$$SR^{+} = +6.29 \text{ V}/\mu\text{s}$$

$$SR^{-} = -7.26 \text{ V}/\mu\text{s}$$

without the well diode connected from the tail node to V_{SS}. These meet the spec. Also the output swing with a sine wave met the 4 V_{pp} spec. The total current is 197.6 μA which is under the 200 μA spec. Next I show plots of the SPICE AC, Transient, and steady-state sine wave simulations.







When I add the well diode the input slew rate becomes:

$$SR^+ = +5.46 \text{ V}/\mu\text{s}$$
$$SR^- = -7.47 \text{ V}/\mu\text{s}$$

and then the positive slew rate is out of spec! This happen because when the amplifier slew's positive, all the tail current flows through M1 and has to charge the well capacitance and the mirror (M3 & M4) capacitance plus the compensation capacitor.

In industry this might meet spec depending on schedule or if there was some design margin in the spec to start with but, for an academic class, you would tweak a little more. Also in the real world noise specs will require you to work harder on sizing the input device W's and L's as well as the L's of the loads and the compensation capacitor C_c.

We need to tweak the design. Since gain, bandwidth, and slew rate are short. Increasing the current would probably solve everything, I am at the constraint limit and these usually are hard (not soft) limits in practice. Therefore I will solve this problem another way. First since the bandwidth and slew rate need to be increased, it is obvious that decreasing the compensation capacitor will help both parameters and the expense of the phase and gain margins. I tried making $C_c = 3.5$ pF. This got the slew rate and lots of bandwidth but the phase margin was now too low and the gain was not effected. To increase the gain I increased the lengths of all the transistors except the input devices. I decreased to width of the input transistors because I had extra bandwidth to help on the phase margin. I also decreased to width of the input stage load devices decrease the parasitic capacitance in the positive slew direction. This required the same ratio decrease in the width of the second stage input M5. The PMOS current sources used to bias the amplifier had to get wider to maintain the output swing because I increased there length to get more gain. The last thing I did was to use the compensation resistor to help tweak the phase margin, making it bigger than the inverse of the transconductance of M5, which would be 600 Ω. I made it 1.1 kΩ which add a little extra phase to cancel out some excess phase due to parasitic poles.

The result of the modifications lead to a design that meet all specs, with the well diode in the circuit. The new sizes are given below:

$$M_1 = M_2 = \frac{170\ \mu\text{m}}{4\ \mu\text{m}}$$
$$M_3 = M_4 = \frac{60\ \mu\text{m}}{3.25\ \mu\text{m}}$$
$$M_5 = \frac{600\ \mu\text{m}}{3.25\ \mu\text{m}}$$
$$M_6 = \frac{750\ \mu\text{m}}{10\ \mu\text{m}}$$
$$M_7 = \frac{150\ \mu\text{m}}{10\ \mu\text{m}}$$
$$M_8 = \frac{50\ \mu\text{m}}{10\ \mu\text{m}}$$
$$R_c = 1.1\ k\Omega$$
$$C_c = 3.5\ \text{pF}$$

The new AC simulation results shown below meet all specs:

$$A_v = 90.04\ \text{dB}$$
$$f_u = 6.21\ \text{MHz}$$
$$PM = 60.24^\circ$$
$$GM = 27.33\ \text{dB}$$

The final transient step simulation showed the input slew rate met both the positive and negative spec with the well diode in the circuit and the sine wave output swing is still good.

$$SR^{+} = +6.21 \text{ V}/\mu\text{s}$$
$$SR^{-} = -8.49 \text{ V}/\mu\text{s}$$

The final total current was 195.3 μA which still meets the spec.

An alternate solution was found for the strategy of letting some systematic offset into the design and using different length devices between M3 & M4 and M5. This leads to the following transistor sizes.

$$M_1 = M_2 = \frac{180\ \mu\text{m}}{3.75\ \mu\text{m}}$$
$$M_3 = M_4 = \frac{80\ \mu\text{m}}{4\ \mu\text{m}}$$
$$M_5 = \frac{550\ \mu\text{m}}{2.75\ \mu\text{m}}$$
$$M_6 = \frac{600\ \mu\text{m}}{8\ \mu\text{m}}$$
$$M_7 = \frac{120\ \mu\text{m}}{8\ \mu\text{m}}$$
$$M_8 = \frac{40\ \mu\text{m}}{8\ \mu\text{m}}$$
$$R_c = 1.1\ k\Omega$$
$$C_c = 3.5 \text{ pF}$$

The AC simulation results shown below meet all specs for the alternate design:

$$A_v = 90.15 \text{ dB}$$
$$f_u = 6.59 \text{ MHz}$$
$$PM = 60.68^\circ$$
$$GM = 29.91 \text{ dB}$$

The alternate design's transient step simulation showed the input slew rate met both the positive and negative spec with the well diode in the circuit and the sine wave output swing also was is still good.

$$SR^{+} = +6.71 \text{ V}/\mu\text{s}$$
$$SR^{-} = -8.90 \text{ V}/\mu\text{s}$$

The final total current for the alternate design was 196.7 μA which still meets the spec.

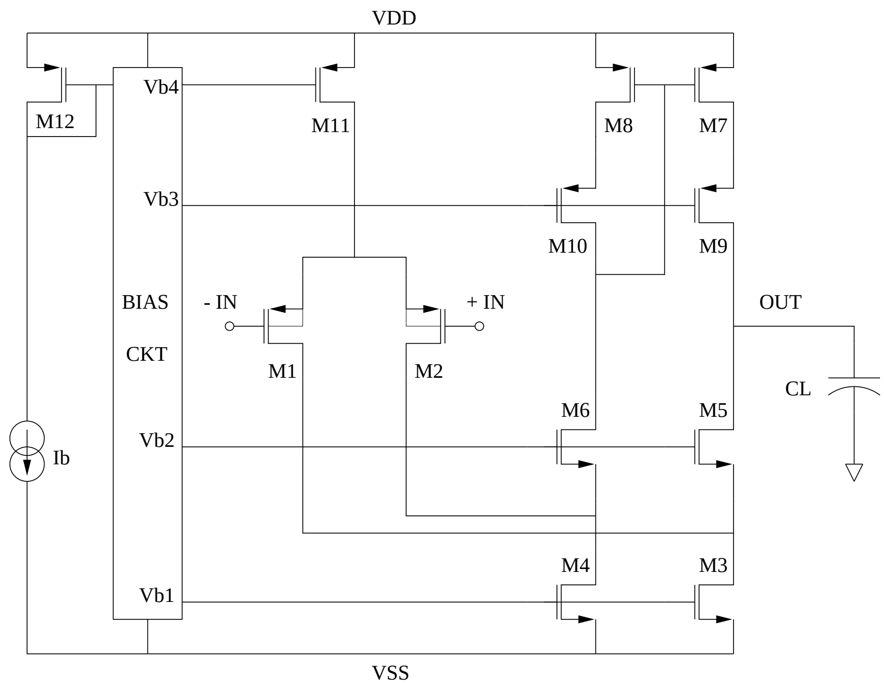


Figure 2: CMOS folded-cascode transconductance amplifier with PMOS inputs

2 Design Specs for a Folded-Cascode TC Amp

The following design equations and specs must be met simultaneously driving a load capacitor, $C_L = 5\text{pF}$. The total current for the amplifier must be less than $160\mu\text{A}$ counting the bias, $I_b = 10\mu\text{A}$, flowing through M12 with a power supply voltage $V_{DD} - V_{SS} = 5\text{V}$.

$$|A_{v_o}| = \frac{G_{m_{in}}}{G_{out}} = \frac{g_{m_1}}{\frac{(g_{ds_1}+g_{ds_3})g_{ds_5}}{G_{m_5}} + \frac{g_{ds_7}g_{ds_9}}{G_{m_9}}} \geq 80\text{dB} \tag{25}$$

where $G_{m_{5,9}} = g_m + g_{mb}$.

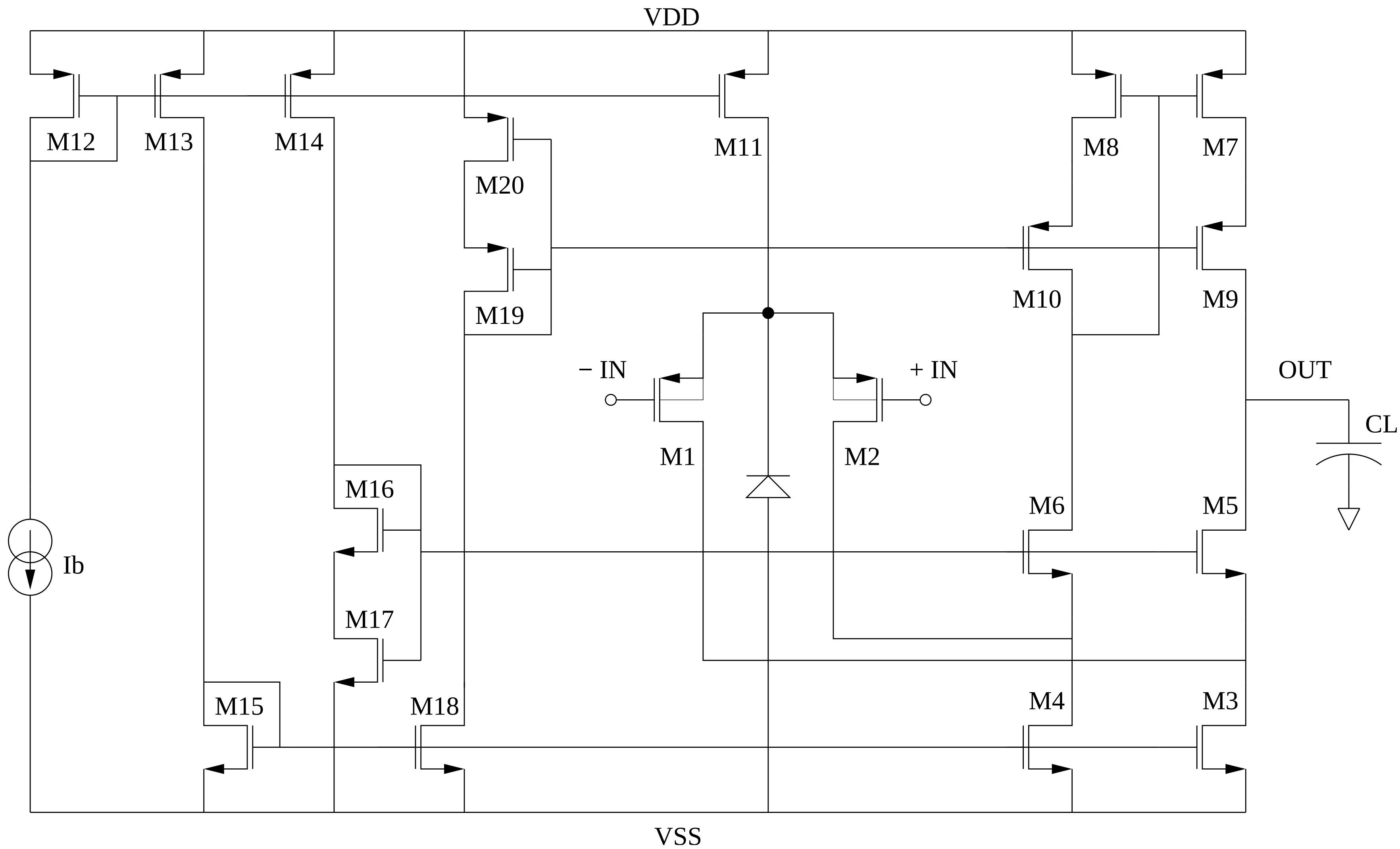
$$\omega_u = \left(\frac{g_{m_1}}{C_L}\right) \geq 2\pi \cdot 9\text{MHz} \tag{26}$$

$$SR = \frac{dV_o}{dt} = \frac{I_{11}}{C_L} = \frac{2I_1}{C_L} = \frac{2I_1\,\omega_u}{g_{m_1}} = V_{gst_1}\omega_u \geq 8\text{V}/\mu\text{s} \tag{27}$$

$$\text{OutputSwing } V_o \geq 3.5\text{V}_{pp} \text{ with } THD \leq 0.1\% \text{ at } f_{in} = 1\text{kHz} \tag{28}$$

$$\text{Total Settling Time, } T_s \leq 236\text{ns for 1V step}$$
$$\text{Linear Settling Time, } T_{s_{small}} \leq 122\text{ns for 100mV step} \tag{29}$$

The first problem to work on is the quiescent bias point. A bias network must be synthesized that will ensure all devices in the amplifier M1−M11 are maintained in saturation under all DC conditions. Depending on the type of circuit technique used to bias the cascode transistors, possibly some of the transistors in the bias itself may work in triode. To meet the 3.5 V_{pp} output voltage swing spec, the output devices, M3 & M5 on the low side and M7 & M9 on the high side, must remain in in saturation when the output voltage is less than 750 mV from the power supply rail. Because we have a cascoded output stage, we must proportion the voltage drops across two devices with the total being less than a threshold voltage. This means we must use what's called a 2 V_{dsat} current mirror or high swing current mirror circuit. A very good bias network, with close to the minimum number of devices, that accomplishes this is shown in the Figure below.


VDD
M12
M13
M14
M20
M11
M8
M7
M10
M9
M19
− IN
+ IN
OUT
CL
M1
M2
M16
M6
M5
Ib
M17
M15
M18
M4
M3
VSS

The NMOS mirror consisting of the diode connected transistor M15, which is the bias for M3, M4 current source loads, sets the V_{gst} and therefore the V_{dsat} of M3 & M4. This group of transistors must be matched. Next the NMOS cascode devices M5, M6 must be designed to have a small V_{dsat}. This is set by the V_{gst} of M16. So M5, M6 & M16 are a matched set. What is meant by saying they are matched, is the physics of each device must be the same. It is the channel length of the transistor that sets the physics (i.e. the threshold voltage, the body effect, the channel length modulation, the $1/f$ noise, and second order matching). So the L's of M3, M4 and M15 must be the same. Also the L's of M5, M6 and M16 must be the same. Now we must decide how much voltage to allow across the current source versus the cascode device. I will choose $V_{DS_3} \simeq 500$ mV and $V_{dsat_5} \simeq 150$ mV. This will allow the output to swing to within 650 mV of the V_{SS} supply. To ensure that M3 is always in saturation I will make its $V_{dsat_3} \simeq 330$ mV, which gives us 170 mV of headroom for the current source. The method to get a DC bias of 500 mV V_{DS} across M3, uses a bias loop consisting of M17, M16, M5 and M3. We match M17 (use the same L) to M15, M4, M3; but since M17 will be in triode, we size the W just to get an IR drop of 500 mV. This is a nonlinear problem and requires several SPICE runs to find the right value for W_{17}. Once it is found then by making the V_{gst}'s of M5, M6 & M16 exactly the same which will force 500 mV at the drains of M3 & M4. Now for the PMOS mirror load we must follow the same procedure. We match M9, M10 & M19 by making their L's the same and bias them with equal V_{gst}'s approximately equal to 150 mV. Then make M7, M8 & M20 have the same L. Iteratively size the width of M20 to get its $V_{DS} \simeq 500$ mV. Then design the V_{dsat} for M7 & M8 to be about 330 mV. The bias loop of M9, M10, M19 & M20 forces 500 mV across the drains of M7 & M8 which guarantees that they will operate in saturation. So the equations that we must solve for the bias to meet the above conditions are:

$$V_{dsat_3} \simeq V_{gst_3} = \sqrt{\frac{2I_3}{\mu_n C_o S_3}} \leq 0.33\text{V} \tag{30}$$

$$V_{dsat_5} \simeq V_{gst_5} = \sqrt{\frac{2I_5}{\mu_n C_o S_5}} \leq 0.15\text{V} \tag{31}$$

$$V_{dsat_7} \simeq V_{gst_7} = \sqrt{\frac{2I_7}{\mu_p C_o S_7}} \leq 0.33\text{V} \tag{32}$$

$$V_{dsat_9} \simeq V_{gst_9} = \sqrt{\frac{2I_9}{\mu_p C_o S_9}} \leq 0.15\text{V} \tag{33}$$

The compensation for a folded-cascode amplifier is considered relatively easy because it is thought of as a single pole system. This is not quite accurate. The small equivalent model for the folded-cascode gives 4 poles and 2 zeros in the LHP. The magnitudes of these poles are:

$$|p_1| \cong \frac{G_{out}}{C_L} = \frac{\frac{(g_{ds_1}+g_{ds_3})g_{ds_5}}{G_{m_5}} + \frac{g_{ds_7}g_{ds_9}}{G_{m_9}}}{C_L} = \frac{g_{m_1}}{A_v C_L} = \frac{\omega_u}{A_v} \tag{34}$$

$$|p_2| \cong \frac{g_{m_8}}{2C_{gs_8}} \simeq \frac{\omega_{T_8}}{2} \tag{35}$$

$$|p_3| \cong \frac{G_{m_9}}{C_{gs_9}} \simeq \omega_{T_9} \tag{36}$$

$$|p_4| \cong \frac{G_{m_5}}{C_{gs_5}} \simeq \omega_{T_5} \tag{37}$$

where p_2 is the mirror pole, and $\omega_T = 2\pi f_T$ is the intrinsic bandwidth of the MOSFET. The 2 zeros are usually off axis and approximately cancel two of the poles. This leaves a 2 pole system to deal with. For the PMOS input folded-cascode, the non-dominate pole is usually the mirror pole, p_2. However, for an NMOS input amplifier the non-dominate pole can become the pole associated with the folding transistor which will be a PMOS device. So with a 2-pole approximation, the phase margin (PM) equation can be written as:

$$PM = 180^\circ - \tan^{-1}\frac{\omega_u}{|p_1|} - \tan^{-1}\frac{\omega_u}{|p_2|} \tag{38}$$

Note that $\omega_u/|p_1| \simeq A_v$ which is a very large number. The arctan of a very large number is aproximately 90°, so the phase margin for this 2 pole system is:

$$PM = 90^\circ - \tan^{-1}\frac{\omega_u}{|p_2|}\,. \tag{39}$$

For a phase margin of 70° equation (12) can be solved to give the magnitude of the second, non-dominate, pole location for p_2.

$$|p_2| = \frac{\omega_u}{\tan 20^\circ} = 2.7475\,\omega_u \tag{40}$$

So we want the mirror pole to be greater than 24.73 MHz.

Now that we have gone through all the design equations and specs we have to start combining different conditions to determine the device sizes. Since the maximum total current is given, all we can do is decide how to partition it between branches. To get an idea about this, we should look at the input slew rate equation (3) where we know C_L

$$I_{11} = C_L\,SR \geq 40\mu\text{A} \tag{41}$$

But this does not include the N-well diode capacitance at the tail node or the mirror capacitance that must also be charged on positive steps. So we will need more current bias for M11. But we don't know how much more current will be needed because we have not sized any transistors yet. Since the maximum current is $\sim 160\mu$A, with 10μA used in the input bias M12, that leaves 150μA to split between the three bias branches and the amplifier. If we pick 10μA for each bias branch, that leaves 120μA for the amp. The normal bias condition for folded-cascode amplifiers is to have an equal amount of current flowing in the input device and the PMOS load transistor. This bias point gives the amp the optimal point between voltage gain and slew rate. So we will choose to have the tail current $I_{11} = 60\mu$A and the NMOS current sources $I_3 = I_4 = 60\mu$A. Substituting into equation (27) **ideally** the slew rate will be 12V/μs. This should meet the spec even with the parasitic capacitances in the circuit.

We can go in any order to determine transistor sizes. There is no required or special way, just whatever you like. I will work on the input devices first. We can start with equation (2) and solve for the ratio of width to length, S:

$$S_1 = \frac{(C_L\,\omega_u)^2}{2\,\mu_p\,C_o\,I_1} = 70.126\ , \tag{42}$$

which after substitution of the spec values into equation (42) and assuming $\mu_p C_o = 19\mu\text{A/V}^2$ we find a value for S_1, we will use $S_1 = 72$ to make it divisible by 4 for layout matching. We will use the gain equation to help determine the length of M1, M3 and M7. For the cascode transistors M5 and M9, we want to maximize their self-gain and minimize their self-capacitance, therefore I will use a channel length of 2 μm. The process that we are using to design this amp has a minimum channel length of 1 μm and my rule-of-thumb is to use 2 times this minimum for devices that don't have critical matching or noise requirements. Modifying equation (25) for the gain with bandwidth equation (26) yields an equation for the output resistance:

$$G_{out} = \frac{(g_{ds_1} + \, g_{ds_3})g_{ds_5}}{G_{m_5}} + \frac{g_{ds_7}g_{ds_9}}{G_{m_9}} \leq \frac{\omega_u \, C_L}{10^4} \; . \tag{43}$$

I will now substitute the simple first order models for the conductances in the output resistance term to get:

$$G_{out} = \frac{(\lambda_1 I_1 + \, \lambda_3 I_3)\lambda_5 I_5}{g_{m_5}(1+\delta_n)} + \frac{\lambda_7 I_7 \, \lambda_9 I_9}{g_{m_9}(1+\delta_p)} \; , \tag{44}$$

where $\delta \equiv g_{mb}/g_m$. Substituting for $g_m = 2I/V_{gst}$ and noting that we chose $I_3 = 2I_1$. Also, $I_1 = I_5 = I_7 = I_9$ therefore after some algebra:

$$G_{out} = \frac{(\lambda_1 + \, 2\lambda_3)\lambda_5 I_5 V_{gst_5}}{2(1+\delta_n)} + \frac{\lambda_7 \, \lambda_9 I_9 V_{gst_9}}{2(1+\delta_p)} \; , \tag{45}$$

with $\delta_n \approx 1/3$ and $\delta_p \approx 1/4$. From the BSIM3 SPICE model a 2μm P-channel device has a λ=0.081 and that 2μm N-channel device has a λ=0.084. From equation (31) and equation (33) we know what the V_{gst}'s need to be and we know the current. So we can substitute the knows to get the following:

$$1.417 \, (\lambda_1 + \, 2\lambda_3) + 1.458 \, \lambda_7 \leq 0.28274 \; . \tag{46}$$

Because of the factor of 2 in front of λ_3, means M3 is usually longer than the PMOS transistors. Also noise and matching, which has not be considered, tends to make M3 longer. If each term is given equal contribution to the output resistance then; $\lambda_7 < 0.06464$, $\lambda_1 < 0.0665$ and $\lambda_3 < 0.0332$. A 4μm P-channel device has a λ=0.062, so make $L_7 = 4\mu$m and $L_1 = 3\mu$m. The NMOS current source M3 must be longer than the PMOS because of the smaller λ, but a noise calculation would force it to be longer too. A 6μm N-channel device has a λ=0.0324, I will make $L_3 = 6\mu$m. Now the input width can be determined from the earlier calculation for the ratio, S_1. So $W_1 = S_1 \, L_1 = 216\mu$m.

The widths of transistors M3 $-$ M10 can now be found from equations (30), (31), (32) and (33) using the L's just computed. Starting with M3 &

M4, we can re-arrange equation (30) to get:

$$W_3 \geq \frac{2\, I_3\, L_3}{\mu_n\, C_o\, (0.33)^2} = 125.6\ , \tag{47}$$

with $\mu_n\, C_o = 49.9\mu$A. I will use $W_3 = W_4 = 126\mu$m. Now the NMOS cascode devices, M5 & M6 from equation (31):

$$W_5 \geq \frac{2\, I_5\, L_5}{\mu_n\, C_o\, (0.15)^2} = 90.3\ . \tag{48}$$

I will use $W_5 = W_6 = 90\mu$m. The PMOS load transistors are next. Using equation (32);

$$W_7 \geq \frac{2\, I_7\, L_7}{\mu_p\, C_o\, (0.33)^2} = 115.4\ , \tag{49}$$

I will make $W_5 = W_6 = 120\mu$m. Finally the PMOS cascode devices are calculated with equation (33);

$$W_9 \geq \frac{2\, I_9\, L_9}{\mu_p\, C_o\, (0.33)^2} = 138.9\ , \tag{50}$$

So I will make $W_9 = W_{10} = 138\mu$m.

Next we will consider the tail current source length. The usual condition used to calculate L_{11} is the $CMRR \simeq 2g_{m_1} r_{ds_{11}}$. Since g_{m_1} has been determined, we just need a spec for $CMRR$. The default spec is 60dB which gives a value for $g_{ds_{11}} \leq 0.565\mu\mho$. The λ_p can be found by dividing by I_{11}, which is 0.009425. From SPICE with the BSIM3 model, a 9μm P-channel has a $\lambda_p = 0.00883$, which is fairly close. So $L_{11} = L_{12} = L_{13} = L_{14} = 9\mu$m. If common-mode input range is not important, then the W's for this PMOS mirror are set by good current matching, so we want V_{gst}'s to be between 0.4V and 0.5V. Then $S_{12} = S_{13} = S_{14} = 4.21$ for $V_{gst} = 0.5$V with 10μA bias. Therefore $W_{12} = 37.89$, but I will round up to make $W_{12} = W_{13} = W_{14} = 40\mu$m. This means the width of M11 is just $W_{11} = 6 \times W_{12}$.

The initial design is complete, the component values for the amplifier are:

$$M_1 = M_2 = 4\left(\frac{54\ \mu\text{m}}{3\ \mu\text{m}}\right)$$

$$M_3 = M_4 = 6\left(\frac{21\ \mu\text{m}}{6\ \mu\text{m}}\right)$$

$$M_5 = M_6 = 3\left(\frac{30\ \mu\text{m}}{2\ \mu\text{m}}\right)$$

$$M_7 = M_8 = 2\left(\frac{60\ \mu\text{m}}{4\ \mu\text{m}}\right)$$

$$M_9 = M_{10} = 3\left(\frac{46\ \mu\text{m}}{2\ \mu\text{m}}\right)$$

$$M_{11} = 6\left(\frac{40\ \mu\text{m}}{9\ \mu\text{m}}\right)$$

$$M_{12} = M_{13} = M_{14} = \frac{40\ \mu\text{m}}{9\ \mu\text{m}}$$

$$M_{15} = M_{18} = \frac{21\ \mu\text{m}}{6\ \mu\text{m}}$$

$$M_{16} = \frac{30\ \mu\text{m}}{2\ \mu\text{m}}$$

$$M_{17} = \frac{4\ \mu\text{m}}{6\ \mu\text{m}}$$

$$M_{19} = \frac{46\ \mu\text{m}}{2\ \mu\text{m}}$$

$$M_{20} = \frac{8\ \mu\text{m}}{4\ \mu\text{m}}$$

We now run SPICE. The results from the AC simulation are:

$$A_v = 81.24\ \text{dB}$$

$$f_u = 8.749\ \text{MHz}$$

$$PM = 71.76^\circ$$

and you can see we are low on bandwidth. The total current is 161.4 μA which is close enough to the 160 μA spec. So I will make a little tweek to the sizes based on the SPICE output information.

The result of the modifications lead to a design that meet all specs. The new sizes are given below:

$$M_1 = M_2 = 4\left(\frac{60\ \mu\text{m}}{3\ \mu\text{m}}\right)$$
$$M_3 = M_4 = 6\left(\frac{20\ \mu\text{m}}{6\ \mu\text{m}}\right)$$
$$M_5 = M_6 = 3\left(\frac{20\ \mu\text{m}}{2\ \mu\text{m}}\right)$$
$$M_7 = M_8 = 2\left(\frac{60\ \mu\text{m}}{4\ \mu\text{m}}\right)$$
$$M_9 = M_{10} = 3\left(\frac{40\ \mu\text{m}}{2\ \mu\text{m}}\right)$$
$$M_{11} = 6\left(\frac{40\ \mu\text{m}}{9\ \mu\text{m}}\right)$$
$$M_{12} = M_{13} = M_{14} = \frac{40\ \mu\text{m}}{9\ \mu\text{m}}$$
$$M_{15} = M_{18} = \frac{20\ \mu\text{m}}{6\ \mu\text{m}}$$
$$M_{16} = \frac{20\ \mu\text{m}}{2\ \mu\text{m}}$$
$$M_{17} = \frac{4\ \mu\text{m}}{6\ \mu\text{m}}$$
$$M_{19} = \frac{40\ \mu\text{m}}{2\ \mu\text{m}}$$
$$M_{20} = \frac{8\ \mu\text{m}}{4\ \mu\text{m}}$$

The new AC simulation results shown below meet all specs:

$$A_v = 80.73\ \text{dB}$$
$$f_u = 9.254\ \text{MHz}$$
$$PM = 70.91^\circ$$

The final transient step simulation showed the input slew rate met both the positive and negative spec with the well diode in the circuit and the sine wave output swing is good.

$$SR^{+} = +8.294\ \mathrm{V}/\mu\mathrm{s}$$
$$SR^{-} = -11.3\ \mathrm{V}/\mu\mathrm{s}$$

The settling time for the large step input is the sum of the slewing time and the small-signal settling time. The spec is for an ideal one pole system. However, this amplifier is actually closer to a two pole system with a small over/under shoot. The total settling times are:

$$T_s^{+} = 155.5\ \mathrm{ns} \qquad \text{for} \quad \leq 0.1\% \ \text{error}$$
$$T_s^{-} = 165.7\ \mathrm{ns} \qquad \text{for} \quad \leq 0.1\% \ \text{error}$$

The negative step has a 108.6 mV undershoot. The small-signal or linear step response was:

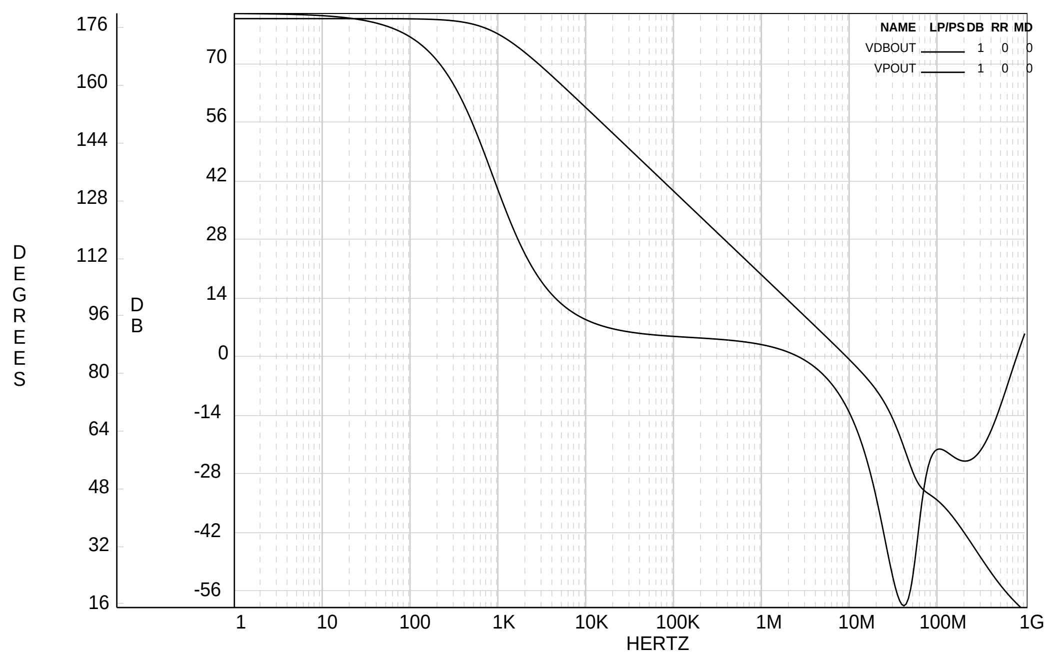
$$T_{s_{small}}^{+} = 96.0\ \mathrm{ns} \qquad \text{for} \quad \leq 0.1\% \ \text{error}$$
$$T_{s_{small}}^{-} = 94.2\ \mathrm{ns} \qquad \text{for} \quad \leq 0.1\% \ \text{error}$$

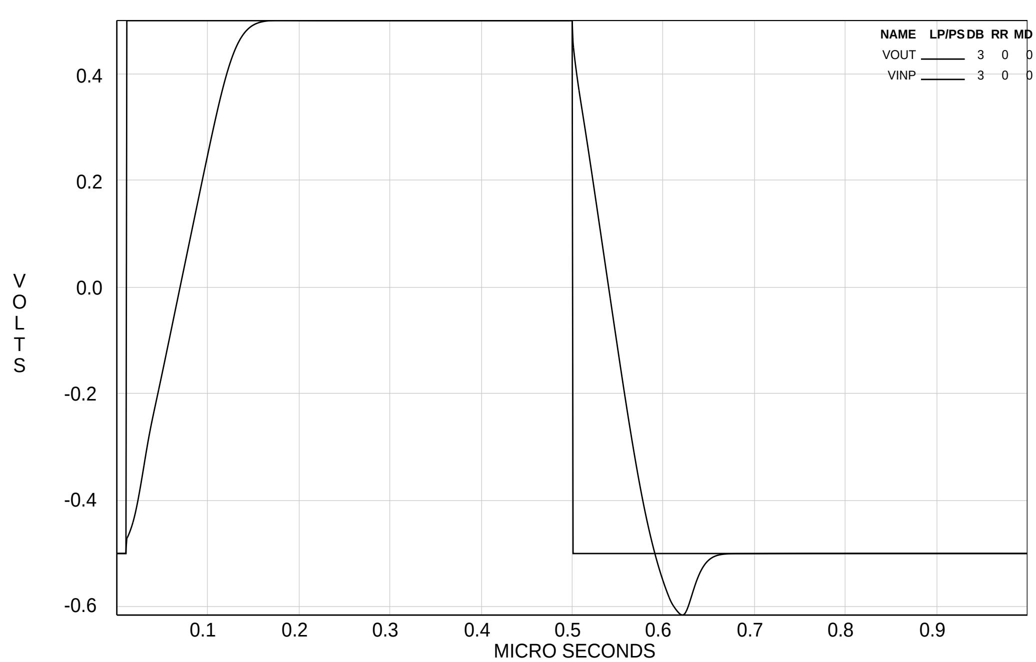
The small positive step had 240 μV overshoot and the small negative step had 645 μV undershoot.

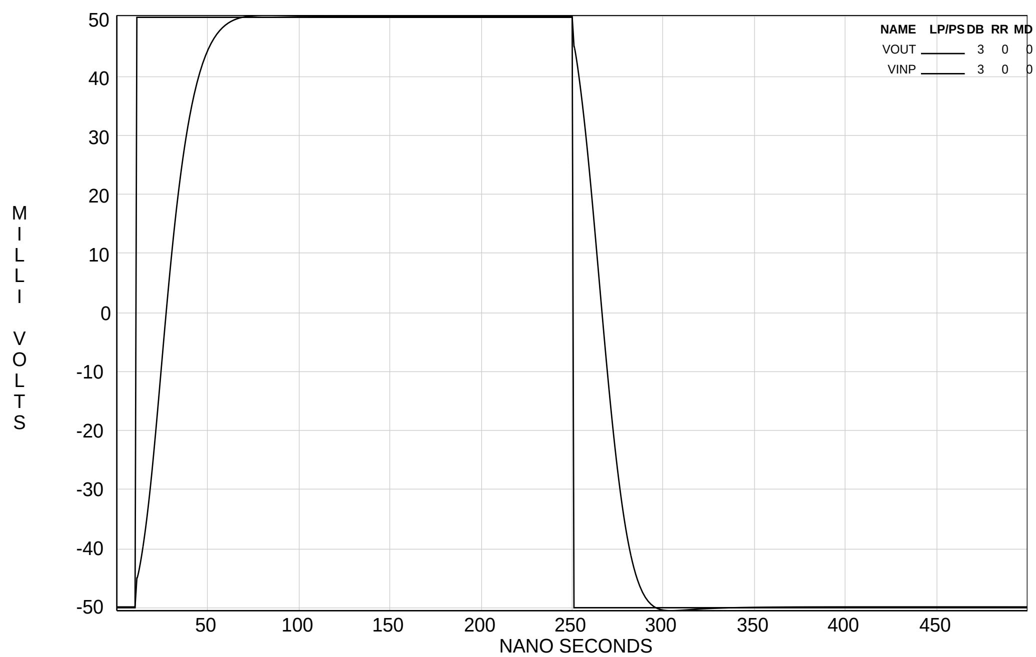
The THD for a 3.5 V_{pp} sinewave was 0.04045 % or -67.86 dB.

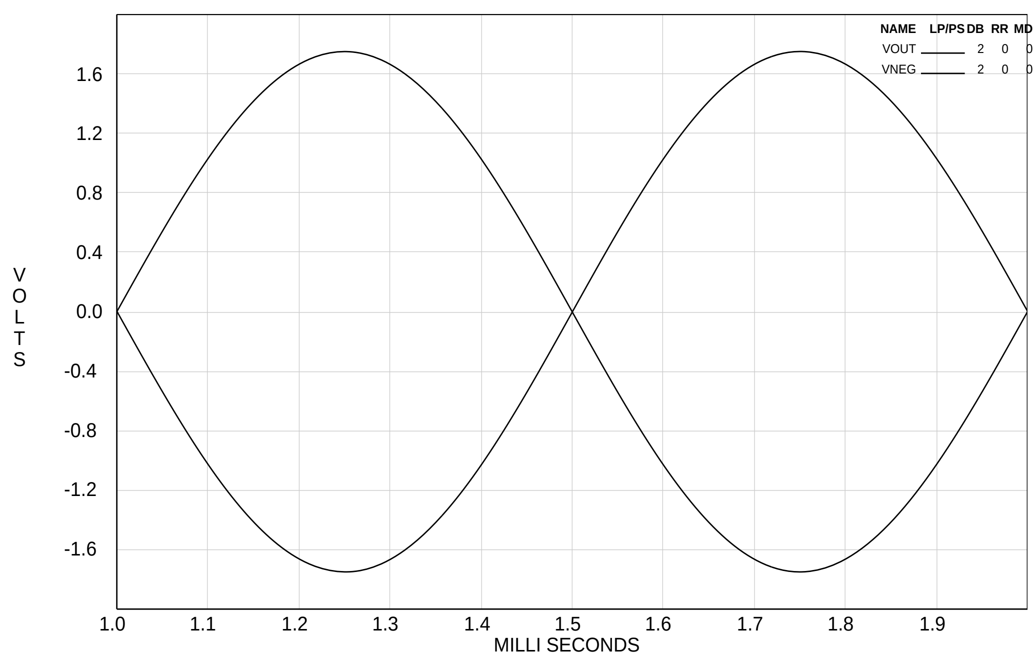
The AC bode analysis, large transient step, linear response step and harmonic distortion time domain simulation with a 3.5 V_{pp} sinewave are plotted and shown on the next pages.

The plots of the simulation outputs follow.






50
40
30
20
10
0
-10
-20
-30
-40
-50
MILLI VOLTS
50
100
150
200
250
300
350
400
450
NANO SECONDS
NAME LP/PS DB RR MD
VOUT 3 0 0
VINP 3 0 0


1.6
1.2
0.8
0.4
0.0
-0.4
-0.8
-1.2
-1.6
VOLTS
1.0
1.1
1.2
1.3
1.4
1.5
1.6
1.7
1.8
1.9
MILLI SECONDS
NAME LP/PS DB RR MD
VOUT 2 0 0
VNEG 2 0 0