CMOS Differential Amplifier

1. Current Equations of Differential Amplifier

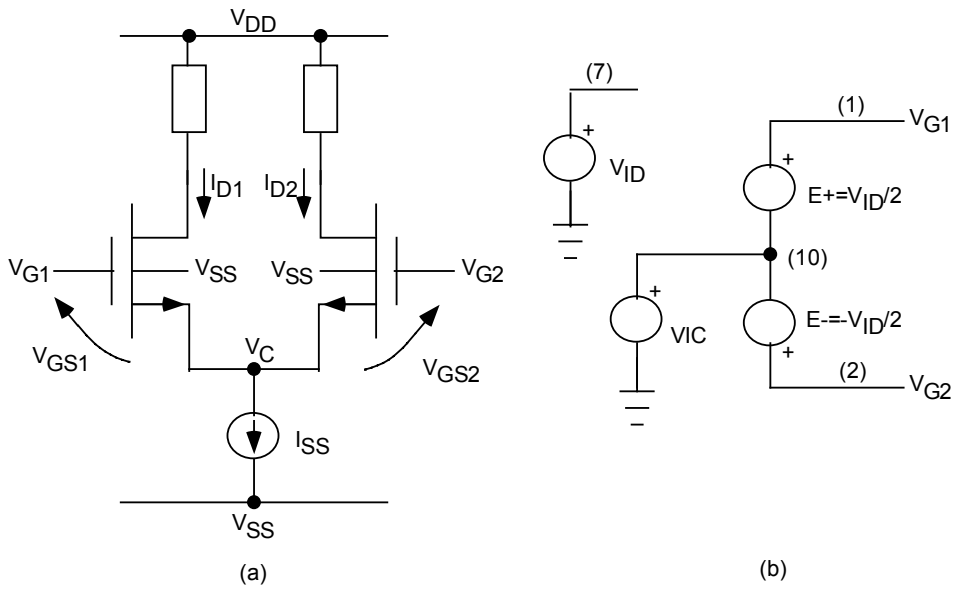


Figure 1. General MOS Differential Amplifier: (a) Schematic Diagram, (b) Input Gate Voltages Implementation.

Figure 1(a) shows the schematic diagram of a typical differential amplifier. The differential input is given by:

$$V_{ID} = V_{G1} - V_{G2} = (V_{GS1} + V_C) - (V_{GS2} + V_C) \quad \text{--(1)}$$

$$V_{ID} = V_{GS1} - V_{GS2} = (V_{GS1} - V_{TN}) - (V_{GS2} - V_{TN}) = \sqrt{\frac{2I_{D1}}{\beta_1}} - \sqrt{\frac{2I_{D2}}{\beta_2}} \quad \text{--(2)}$$

The common-mode input signal is given by:

$$V_{IC} = \frac{V_{G1} + V_{G2}}{2} \quad \text{--(3)}$$

The input voltages in term of V_{ID} and V_{IC} are given by

$$V_{G1} = V_{IC} + V_{ID}/2 \quad \text{--(4)}$$

$$V_{G2} = V_{IC} - V_{ID}/2 \quad \text{--(5)}$$

Figure 1(b) shows the implementation of the 2 gate voltages in terms of the differential and common mode voltages. Its PSpice implementation using voltage controlled voltage source is given below:

```
VID 7 0 DC 0V
E+ 1 10 7 0  0.5
E- 2 10 7 0 -0.5
VIC 10 0 DC 0V
```

Two special cases of input gate signals are of interests : pure differential and pure common mode input signals. Pure differential input signals mean V_{IC}=0, from equation (4) and (5);

$$V_{G1} = V_{ID}/2$$
$$V_{G2} = -V_{ID}/2$$

This case is of interest when studying the differential gain of differential amplifier, see Figure 2(a). Pure common-mode input signals mean V_{ID}=0, from equation (4) and (5);

$$V_{G1} = V_{IC}$$
$$V_{G2} = V_{IC}$$

This case is of interest when studying the common-mode gain of differential amplifier, see Figure 5(a).

Assume both transistor drivers are matched, that is:

$$\beta_1 = \beta_2 = \beta$$

$$V_{ID} = \sqrt{\frac{2I_{D1}}{\beta}} - \sqrt{\frac{2I_{D2}}{\beta}} \quad \text{--(6)}$$

$$\sqrt{\beta/2}V_{ID} = \sqrt{I_{D1}} - \sqrt{I_{D2}} \quad \text{--(7)}$$

The transistor currents satisfy the following equations:

$$I_{SS} = I_{D1} + I_{D2} \quad \text{--(8)}$$

$$I_{OD} = I_{D1} - I_{D2} \quad \text{--(9)}$$

$$I_{D1} = (I_{SS} + I_{OD})/2 \quad \text{--(10)}$$

$$I_{D2} = (I_{SS} - I_{OD})/2 \quad \text{--(11)}$$

Substituting Eq(10) and Eq(11) to Eq(7)

$$\sqrt{\beta/2}V_{ID} = \sqrt{(I_{SS} + I_{OD})/2} - \sqrt{(I_{SS} - I_{OD})/2} \quad \text{--(12)}$$

Normalizing by I_{SS}

$$\sqrt{\frac{\beta}{I_{SS}}}V_{ID} = (\sqrt{1+\frac{I_{OD}}{I_{SS}}} - \sqrt{1-\frac{I_{OD}}{I_{SS}}}) \quad \text{--(13)}$$

To simplify the equation, let

$$x = \sqrt{\frac{\beta}{I_{SS}}}V_{ID}\text{ , and }\ y = \frac{I_{OD}}{I_{SS}} \quad \text{--(14)}$$

The equation reduces to:

$$x = \sqrt{1+y} - \sqrt{1-y}$$

Solve for y,

$$x^2 = (1+y) - 2\sqrt{(1+y)(1-y)} + (1-y) = 2 - 2\sqrt{1-y^2}$$

$$\sqrt{1-y^2} = 1 - \frac{x^2}{2}$$

$$1 - y^2 = 1 - x^2 + \frac{x^4}{4}$$

$$y^2 = x^2(1 - \frac{x^2}{4})$$

The result is:

$$y = x\sqrt{1-\frac{x^2}{4}}\text{ , provided } |\frac{x}{2}| \le 1 \quad \text{--(15)}$$

Substituting for x and y, one obtains

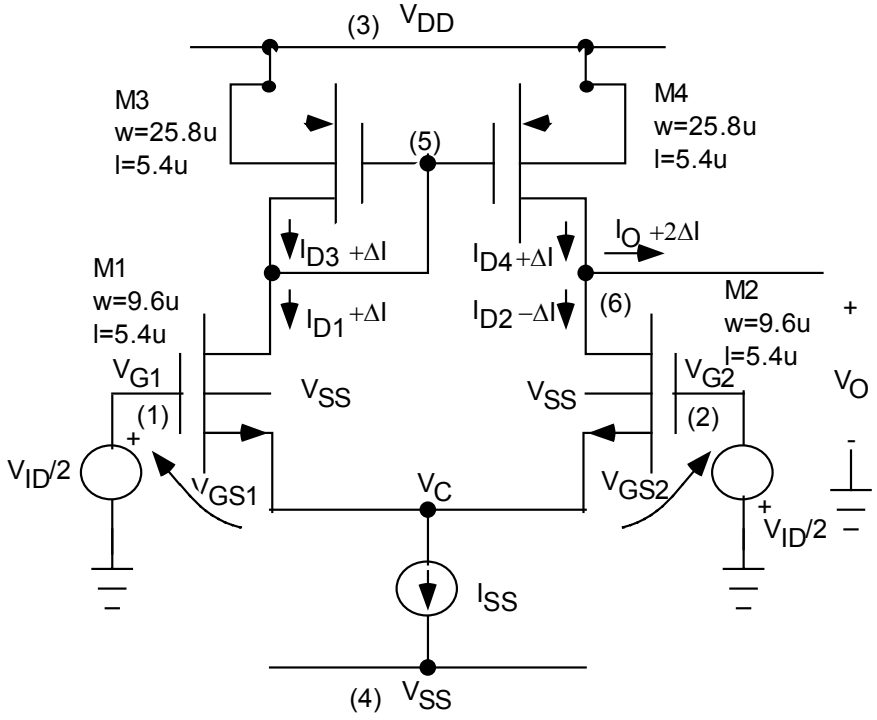
$$\frac{I_{OD}}{I_{SS}} = \sqrt{\frac{\beta}{I_{SS}}}V_{ID}\sqrt{1-\frac{\beta {V_{ID}}^2}{I_{SS}4}} \quad \text{--(16)}$$

$$I_{OD} = I_{SS}\sqrt{\frac{\beta {V_{ID}}^2}{I_{SS}} - \frac{\beta {V_{ID}}^4}{4{I_{SS}}^2}} \quad \text{--(17)}$$

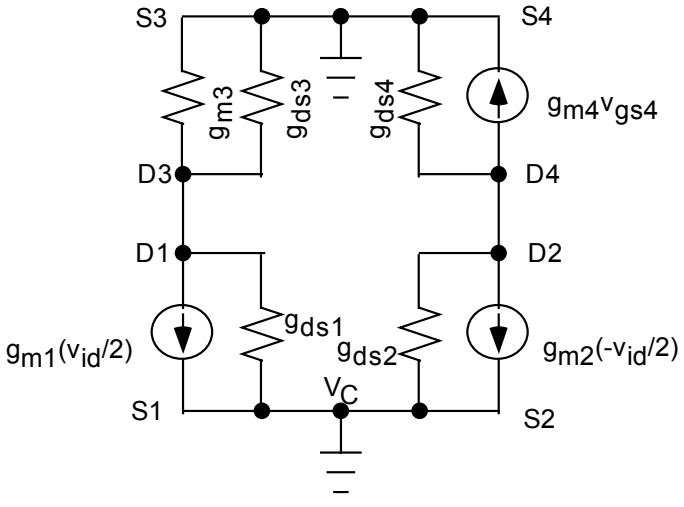
$$I_{D1} = \frac{1}{2}I_{SS} + \frac{1}{2}I_{SS}\sqrt{\frac{\beta {V_{ID}}^2}{I_{SS}} - \frac{\beta {V_{ID}}^4}{4{I_{SS}}^2}} \quad \text{--(18)}$$

$$I_{D2} = \frac{1}{2} I_{SS} - \frac{1}{2} I_{SS} \sqrt{\frac{\beta V_{ID}^{\ 2}}{I_{SS}} - \frac{\beta V_{ID}^{\ 4}}{4 I_{SS}^{\ 2}}} \text{, provided } | V_{ID} | \leq \sqrt{\frac{2 I_{SS}}{\beta}} \qquad \text{--(19)}$$

2. Low Frequency Small Signal Equivalent Circuit With Pure Differential Input Signal



(a)



(b)

Figure 2. Differential Amplifier Implementation: (a) Differential Amplifier with PMOS current mirror load, (b) Small Signal Equivalent Circuit for Purely Differential Input Signal.

An active load acts as a current source. Thus it must be biased such that their currents add up exactly to I_{SS}. In practice this is quite difficult. Thus a feedback circuit is required to ensure this equality. This is achieved by using a current mirror circuit as load, as in Figure 2. The current mirror consists of transistor M3 and M4. One transistor (M3) is always connected as diode and drives the other transistor (M4). Since $V_{GS3}=V_{GS4}$, if both transistors have the same β, then the current I_{D3} is mirrored to I_{D4}, i.e., $I_{D3}=I_{D4}$.

The advantage of this configuration is that the differential output signal is converted to a single ended output signal with no extra components required. In this circuit, the output voltage or current is taken from the drains of M2 and M4. The operation of this circuit is as follows. If a differential voltage, $V_{ID}=V_{G1}-V_{G2}$, is applied between the gates, then half is applied to the gate-source of M1 and half to the gate-source of M2. The result is to increase I_{D1} and decrease I_{D2} by equal increment, ΔI. The ΔI increase I_{D1} is mirrored through M3-M4 as an increase in I_{D4} of ΔI. As a consequence of the ΔI increase in I_{D4} and the ΔI decrease in I_{D2} , the output must sink a current of $2\Delta I$. The sum of the changes in I_{D1} and I_{D2} at the common node V_C is zero. That is, the node V_C is at an ac ground, see Figure 2(b). From Eq(4) and Eq(5) for pure differential input signal means the common-mode signal V_{IC} is zero. That is, the input signals are $V_{G1}=V_{ID}/2$ and $V_{G2}=-V_{ID}/2$. This is shown in Figure 2(a). The transconductance of the differential amplifier is given by:

$$g_{mD} = \frac{\Delta I_O}{\Delta V_{ID}} = \frac{2\Delta I}{\Delta V_{ID}} = \frac{\Delta I}{\Delta V_{ID}/2} = \frac{\Delta I}{V_{gs1}} = g_{m1}$$

That is, the differential amplifier has the same transconductance as a single stage common source amplifier.

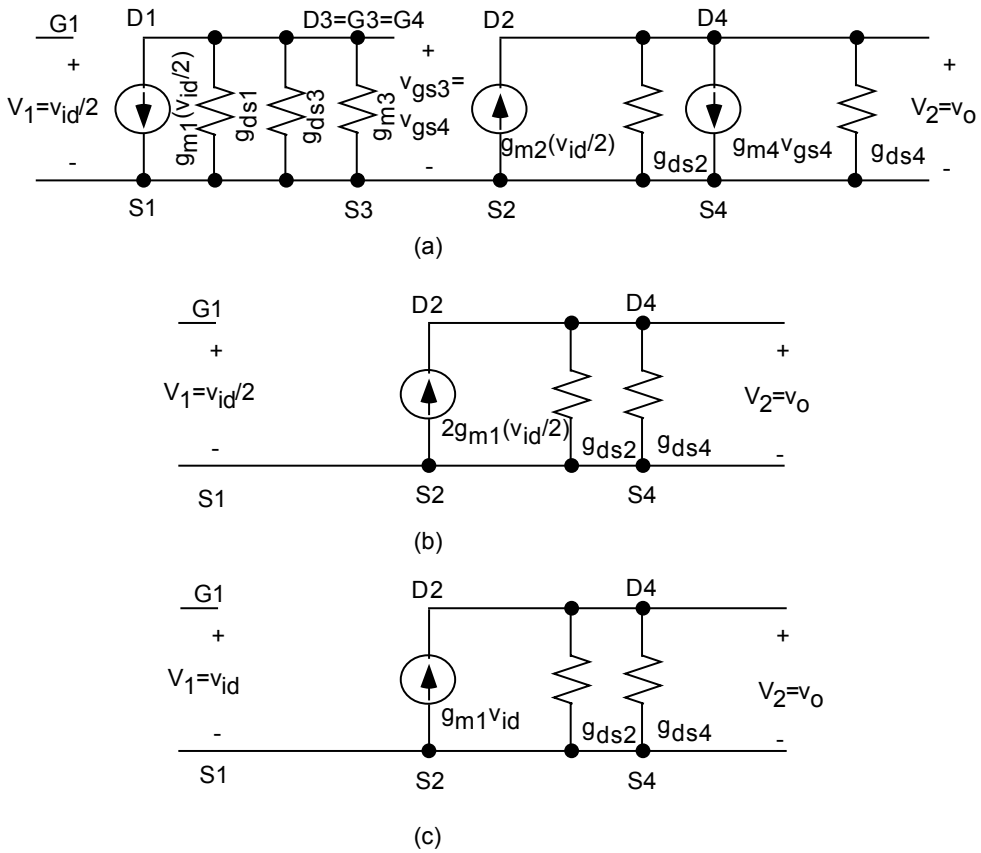


Figure 3. Differential Amplifier Operating in Purely Differential Input Signal: (a) Original Equivalent Circuit, (b) Reduction to Two-port Network, and (c) Changing Input Port Variable to $V_1=V_{id}$.

The derivation of the small signal equivalent circuit is shown in Figure 2. The simplification is based on the symmetry of the circuit. In Figure 2(b), each transistor equivalent circuit is drawn. Figure 3(a) redraws the equivalent circuit in Figure 2(b) in a form suitable for two-port analysis. The further reduction is obtained after the two-port parameters are obtained.

From Figure 3(a), the following two-port variables and load are obtained.

$$Y_L = 0$$
$$V_1 = V_{ID}/2$$
and
$$V_2 = V_O$$

The port current equations are derived to obtain the Y parameters:

$$I_1 = 0 \qquad \text{--(20)}$$

$$I_2 = -g_{m2}V_1 + g_{m4}V_{gs4} + (g_{ds2} + g_{ds4})V_2 \qquad \text{--(21)}$$

$$V_{gs4} = -\frac{g_{m1}}{g_{ds1} + g_{ds3} + g_{m3}} V_1 \qquad \text{--(22)}$$

Substitute eq(22) to eq(21)

$$\begin{aligned} I_2 &= -g_{m2}V_1 - \frac{g_{m1}g_{m4}}{g_{ds1} + g_{ds3} + g_{m3}} V_1 + (g_{ds2} + g_{ds4})V_2 \\ &= -(g_{m2} + \frac{g_{m1}g_{m4}}{g_{ds1} + g_{ds3} + g_{m3}})V_1 + (g_{ds2} + g_{ds4})V_2 \\ &= -2g_{m1}V_1 + (g_{ds2} + g_{ds4})V_2 \end{aligned} \qquad \text{--(23)}$$

assuming $g_{m1} = g_{m2}$ $g_{m3} = g_{m4}$ $g_{m3} >> g_{ds1} + g_{ds3}$

The resulting Y-parameter matrix is:

$$Y = \begin{bmatrix} 0 & 0 \\ -2g_{m1} & g_{ds2} + g_{ds4} \end{bmatrix}$$

The dc voltage gain is,

$$A_{VD02} = \frac{V_2}{V_1} = \frac{V_O}{V_{id}/2} = -\frac{y_{21}}{y_{22} + Y_L} = \frac{2g_{m1}}{g_{ds2} + g_{ds4}}$$

Instead of half differential input, dc gain with respect to full differential input is desired. That is,

$$A_{VDO} = \frac{V_2}{V_1} = \frac{V_O}{V_{id}} = \frac{g_{m1}}{g_{ds2} + g_{ds4}} = \frac{g_{m2}}{g_{ds2} + g_{ds4}} \qquad \text{--(24)}$$

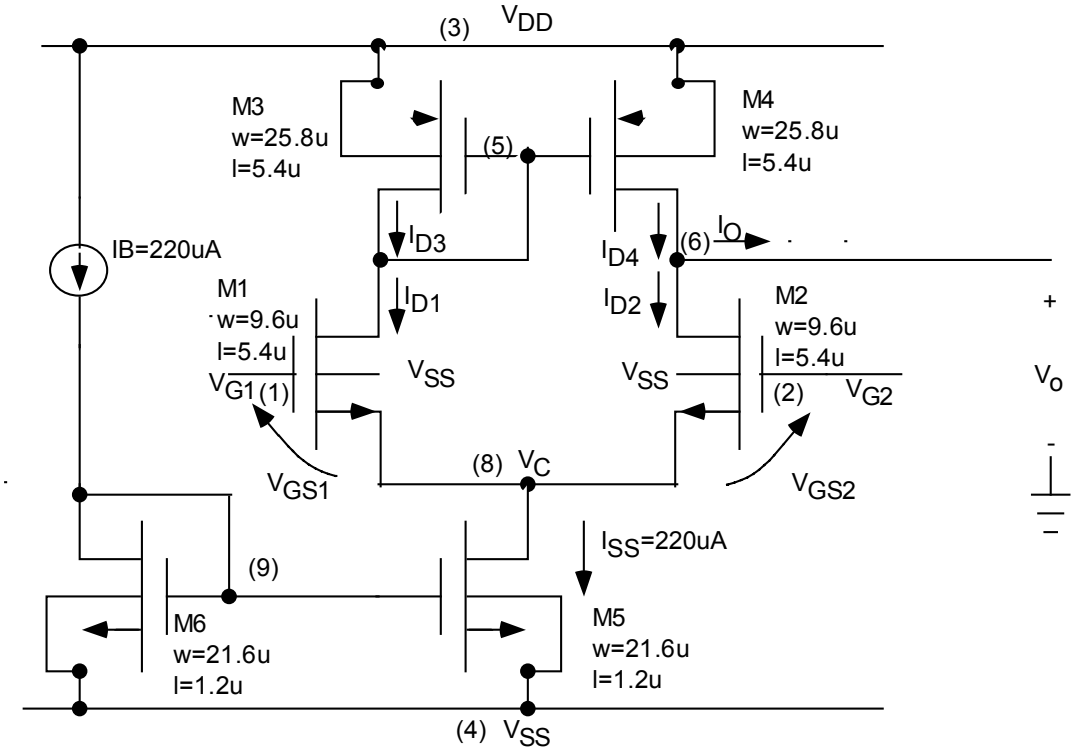
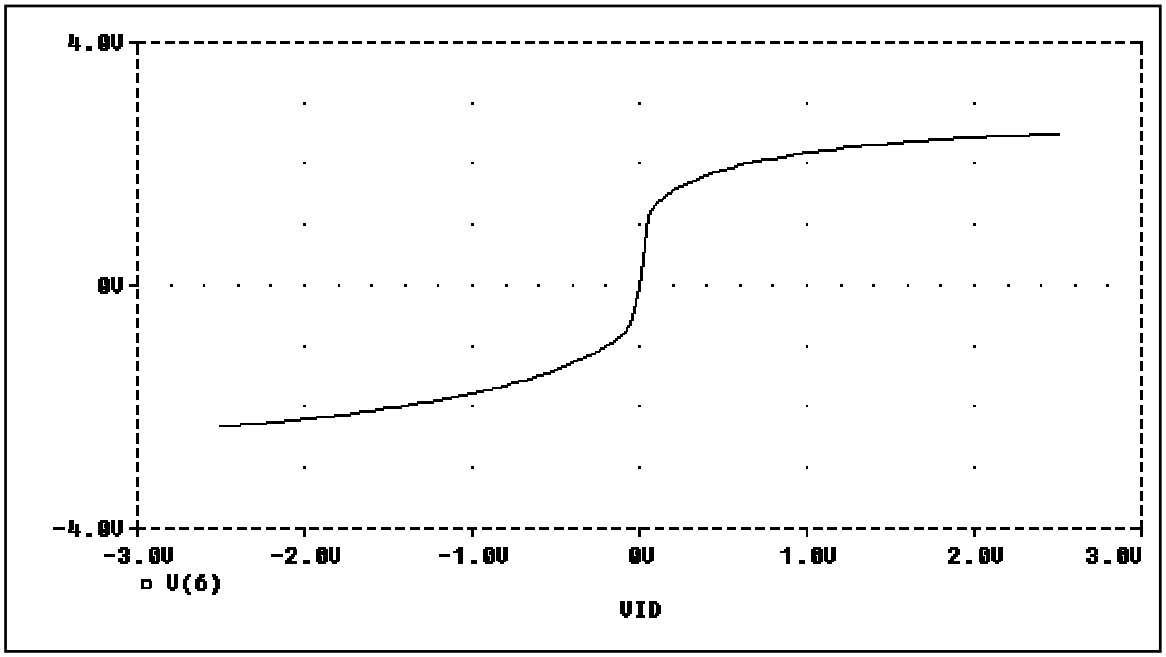


Figure 4. The Complete Differential Amplifier Schematic Diagram

Figure 3(c) is the resulting two-port equivalent circuit. Except for the polarity this gain equation is identical to that of the single NMOS inverter with PMOS current load. Figure 4 shows the complete differential amplifier implemented using a pair of inverter amplifier with PMOS current load, and 200uA current souce. The PSpice netlist is given below:

```
* Filename="diffvid.cir"
* MOS Diff Amp with Current Mirror Load
*DC Transfer Characteristics vs VID
VID 7 0 DC 0V  AC 1V
E+ 1 10 7 0  0.5
E- 2 10 7 0 -0.5
VIC 10 0 DC 0.65V
VDD 3 0 DC 2.5VOLT
VSS 4 0 DC -2.5VOLT
M1 5 1 8 8  NMOS1  W=9.6U       L=5.4U
M2 6 2 8 8  NMOS1  W=9.6U       L=5.4U
M3 5 5 3 3  PMOS1  W=25.8U      L=5.4U
M4 6 5 3 3  PMOS1  W=25.8U      L=5.4U
M5 8 9 4 4  NMOS1  W=21.6U      L=1.2U
M6 9 9 4 4  NMOS1  W=21.6U      L=1.2U
IB 3 9 220UA
.MODEL NMOS1 NMOS VTO=1 KP=40U
+ GAMMA=1.0 LAMBDA=0.02 PHI=0.6
+ TOX=0.05U LD=0.5U CJ=5E-4 CJSW=10E-10
+ U0=550 MJ=0.5 MJSW=0.5 CGSO=0.4E-9 CGDO=0.4E-9
.MODEL PMOS1 PMOS VTO=-1 KP=15U
+ GAMMA=0.6 LAMBDA=0.02 PHI=0.6
```

```
+ TOX=0.05U LD=0.5U CJ=5E-4 CJSW=10E-10
+ U0=200 MJ=0.5 MJSW=0.5 CGSO=0.4E-9 CGDO=0.4E-9
.DC VID -2.5 2.5 0.05V
.TF V(6) VID
.PROBE
.END
```



The operating point current is determined by the source current I_{SS}, which is split between the two PMOS current loaded inverters. $I_{DSQ1}=I_{DSQ2}=I_{SS}/2$, and similarly $I_{DSQ3}=I_{DSQ4}=I_{SS}/2$. For the given differential amplifier I_{SS}=220uA. The voltage gain is computed as follows:

$$\beta_{N1} = \beta_{N2} = K_{N1}(W_{N1}/L_{N1}) = (40E-6)(9.6u/(5.4u-2*0.5u)) = 87.3uA/V^2$$
$$\beta_{P3} = \beta_{P4} = K_{P3}(W_{P3}/L_{P3}) = (15E-6)(25.8u/(5.4u-2*0.5u)) = 87.95uA/V^2$$

$$g_{m1} = g_{m2} = \sqrt{2\beta_{N1}I_{DSQ1}} = \sqrt{2(87.3E-6)(110E-6)} = 138.59\,\text{umho}$$
$$g_{m3} = g_{m4} = \sqrt{2\beta_{P3}I_{DSQ3}} = \sqrt{2(87.95E-6)(110E-6)} = 139.1\,\text{umho}$$

$$g_{ds2} = \lambda_{DS2}I_{DSQ2} = \lambda_N I_{DSQ1} = .02(110E-6) = 2.2\,\text{umho}$$
$$g_{ds4} = \lambda_{DS4}I_{DSQ4} = \lambda_P I_{DSQ1} = .02(110E-6) = 2.2\,\text{umho}$$
$$g_{ds5} = \lambda_{DS5}I_{DSQ} = \lambda_P I_{DSQ5} = .02(220E-6) = 4.4\,\text{umho}$$

$$A_{VD} \approx \frac{g_{m1}}{g_{ds2}+g_{ds4}} = \frac{138.59E-6}{2.2E-6+2.2E-6} = 31.5$$

The low frequency input resistance Rin = ∞. The output resistance Rout = $1/(g_{ds2}+g_{ds4})$= 1/(2.2E-6+2.2E-6) =.2272M, see Figure 3(d), and the computation above. These calculations agree well with Pspice simulation results of:

**** SMALL-SIGNAL CHARACTERISTICS

V(6)/VID = 3.347E+01

INPUT RESISTANCE AT VID = 1.000E+20

OUTPUT RESISTANCE AT V(6) = 2.423E+05

3. Determination of the input common-mode range

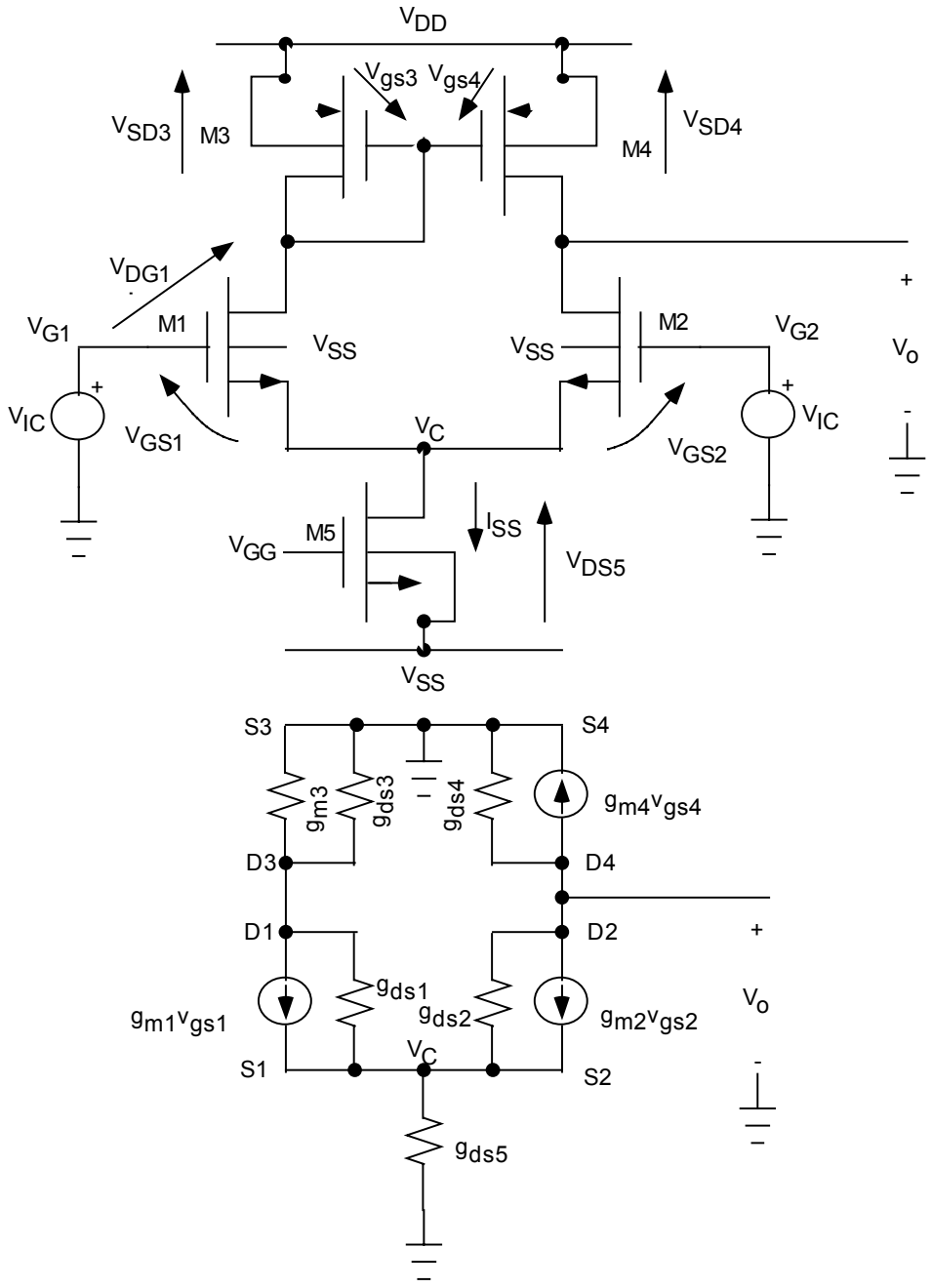


Figure 5. Differential Amplifier with Purely Common-mode Input Signal: (a) Schematic Diagram, and (b) Small Signal Equivalent Circuit.

The input common-mode range is the range of common-mode voltage Vic=V_{G1}=V_{G2} in which all the transistors are operating in saturation region. To determine this a purely common-mode input is applied at both inputs, see Figure 5.

3.1 Maximum V_{G1} or V_{G2} Determination

As VG1 approaches VDD transistor M1 and M2 go into the triode region. V_{G1}(max) is the value of the input when it occurs. This can be determined from Figure 5 by writing the KVL equation from V_{DD} toward V_{G1}.

$$V_{G1} = V_{DD} - V_{SD3} - V_{DG1}$$
$$= V_{DD} - V_{SG3} - V_{DG1}, \quad \text{since } D = G$$

$$V_{SG3} = (|V_{GS3}| - |V_{TP3}|) + |V_{TP3}| = \sqrt{\frac{2|I_{DS3}|}{\beta_{P3}}} + |V_{TP3}|$$

$$V_{G1} = V_{DD} - \sqrt{\frac{2|I_{DS3}|}{\beta_{P3}}} - |V_{TP3}| - V_{DG1}$$

From Figure 5(a), V_{DG1} can be determined in term of the commonly known transistor voltages of M1.

$$V_{DG1} = V_{DS1} - V_{GS1}$$
or
$$V_{DS1} = V_{GS1} + V_{DG1}$$

Transistor M1 is on saturation when the following condition holds.

$$V_{GS1} - V_{TN1} \le V_{DS1} = V_{GS1} + V_{DG1}$$

That is,

$$-V_{TN1} \le V_{DG1}$$

The minimum value of V_{DG1} is achieved when transistor M1 is on the threshold of saturation. That is,

$$-V_{TN1} = V_{DG1}$$

The maximum input voltage is obtained when $-V_{TN1} = V_{DG1}$. That is,

$$V_{G1}(\max) = V_{DD} - \sqrt{\frac{2|I_{DS3}|}{\beta_{P3}}} - |V_{TP3}| + V_{TN1}$$
$$= V_{DD} - \sqrt{\frac{2|I_{DS3}|}{\beta_{P3}}} = V_{DD} - \sqrt{\frac{I_{SS}}{\beta_{P3}}} \qquad \text{--(25)}$$

Assuming $|V_{TP3}| \approx V_{TN1}$.

3.2 Minimum V_{G1} or V_{G2} Determination

As V_{G1} approaches V_{SS}, M1 becomes cutoff. The minimum input voltage V_{G1} is determined when M5 is no longer in saturation. This is obtained by writing the KVL equation from V_{SS} to V_{G1}.

$$V_{G1} = V_{SS} + V_{DS5} + V_{GS1}$$

Transistor M5 is on saturation when,

$$V_{GS5} - V_{TN5} \le V_{DS5}$$

M5 is at verge of saturation when, $V_{GS5} - V_{TN5} = V_{DS5} = V_{DS5(SAT)}$

That is, the minimum input voltage occurs when, $V_{GS5} - V_{TN5} = V_{DS5(SAT)}$.

$$V_{G1}(\min) = V_{SS} + V_{DS5(SAT)} + V_{GS1} \qquad \text{--(26)}$$

$$V_{G1}(\min) = V_{SS} + (V_{GS5} - V_{TN5}) + V_{GS1}$$

$$V_{G1}(\min) = V_{SS} + (V_{GG} - V_{SS} - V_{TN5}) + (V_{GS1} - V_{TN1}) + V_{TN1}$$

$$= V_{GG} - V_{TN5} + \sqrt{\frac{2I_{DS1}}{\beta_{N1}}} + V_{TN1} \qquad \text{--(27)}$$

$$= V_{GG} + \sqrt{\frac{2I_{DS1}}{\beta_{N1}}} = V_{GG} + \sqrt{\frac{I_{SS}}{\beta_{N1}}}$$

Ignoring the bulk bias effect.

Using the SPICE parameters for the differential amplifier implemented in Figure 4.
From Eq(25),

$$V_{G1}(\max) = V_{DD} - \sqrt{\frac{I_{SS}}{\beta_{P3}}}$$

$$\beta_{P3} = K_P(W_3 / L_3) = (15E-6)(25.8u/(5.4u - 2*0.5u)) = 87.95\ \text{uA/V}^2$$

$$V_{G1}(\max) = 2.5 - \sqrt{\frac{220E-6}{87.95E-6}} = 2.5 - 1.58 = 0.92\ \text{V}$$

and from Eq(27),

$$V_{G1}(\min) = \sqrt{\frac{I_{SS}}{\beta_{N1}}} + V_{GG} = \sqrt{\frac{220E-6}{87.3}} - 1.2 = 1.58 - 1.2 = 0.38\ \text{V}$$

To guarantee that the differential amplifier stays on the linear region of operation, set common-mode signal at half way the common-mode range. That is, $V_{IC}=[V_{G1}(\max)+V_{G1}(\min)]/2=[0.92+.38]/2=0.65$.

4. Low Frequency Small Signal Equivalent Circuit With Pure Common-Mode Input Signal

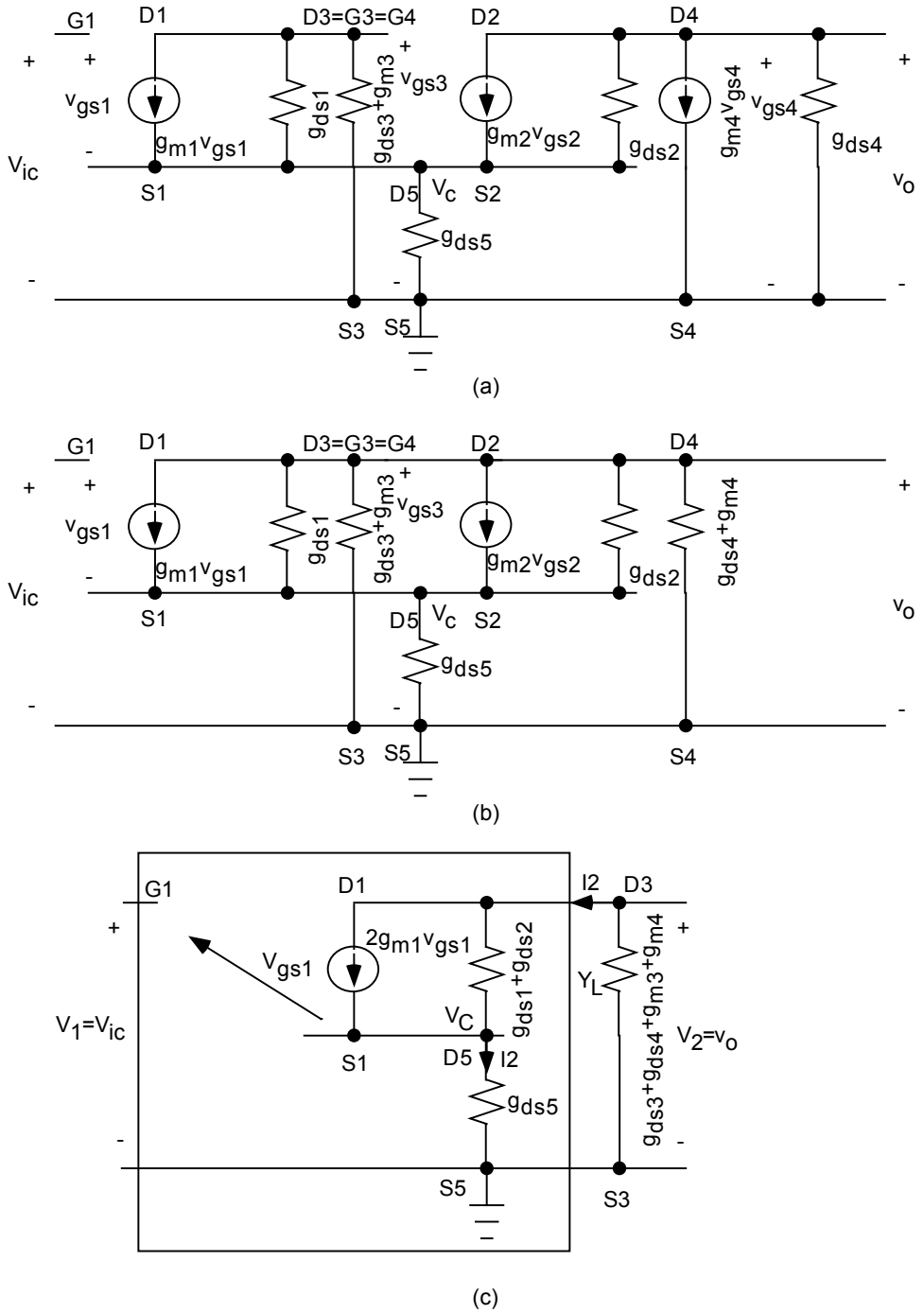


Figure 6. Small Signal Equivalent Circuit: (a) Original Small Signal Equivalent Circuit, (b) Accounting for Source Values and Polarities, and (c) Two-port Conversions.

Figure 5(a) shows the schematic when a purely common-mode input is applied at both inputs that is, $V_{G1}=V_{G2}=V_{IC}$. If V_{IC} increases both I_{D1} and I_{D2} increases. Their sum at the common node V_C also increases. Figure 5(b) shows that V_C is not at ac ground, unlike the pure differential input signal case shown in Figure 2(b). Due to signal symmetry when both inputs are the same, $V_{DS3}=V_{DS4}$. Since both G and S of M3 and M4 are connected to each other, means $V_{GS3}=V_{GS4}$. M3 is diode connected with G and D connected, means $V_{GS3}=V_{DS3}$. From these expressions, $V_{DS4}=V_{GS4}$ can be deduced. That is the voltage

across D and S of M4 can be labelled as V_{GS4}, see Figure 6(a). The current source of M4 is therefore reduced to conductance g_{m4}, see Figure 6(b). Since V_{DS3}=V_{DS4}, the D3 and D4 can be connected together. Figure 6(c) shows the final equivalent circuit after combining all components that are in parallel.

From Figure 6(c), the following two-port variables and load are obtained.

$$Y_L = g_{ds3} + g_{ds4} + g_{m3} + g_{m4} = 2g_{ds3} + 2g_{m3}$$

assuming $g_{ds3} = g_{ds4}$ $g_{m3} = g_{m4}$

$$V_1 = V_{IC}$$

and

$$V_2 = V_O$$

The two-port current equations are derived to obtain the Y parameters.

$$I_1 = 0$$

$$I_2 = (g_{ds1} + g_{ds2})(V_2 - V_C) + 2g_{m1}(V_1 - V_C)$$

$$= 2g_{m1}V_1 + (g_{ds1} + g_{ds2})V_2 - (g_{ds1} + g_{ds2} + 2g_{m1})V_C$$

$$V_C = \frac{1}{g_{ds5}} I_2$$

$$I_2 = 2g_{m1}V_1 + (g_{ds1} + g_{ds2})V_2 - (g_{ds1} + g_{ds2} + 2g_{m1})\frac{1}{g_{ds5}} I_2$$

$$I_2 = \frac{2g_{m1}g_{ds5}}{g_{ds1} + g_{ds2} + g_{ds5} + 2g_{m1}} V_1 + \frac{(g_{ds1} + g_{ds2})g_{ds5}}{g_{ds1} + g_{ds2} + g_{ds5} + 2g_{m1}} V_2$$

The Y-parameter matrix is:

$$Y = \begin{bmatrix} 0 & 0 \\ \frac{2g_{m1}g_{ds5}}{g_{ds1} + g_{ds2} + g_{ds5} + 2g_{m1}} & \frac{(g_{ds1} + g_{ds2})g_{ds5}}{g_{ds1} + g_{ds2} + g_{ds5} + 2g_{m1}} \end{bmatrix}$$

$$= \begin{bmatrix} 0 & 0 \\ \frac{2g_{m1}g_{ds5}}{2g_{ds1} + g_{ds5} + 2g_{m1}} & \frac{2g_{ds1}g_{ds5}}{2g_{ds1} + g_{ds5} + 2g_{m1}} \end{bmatrix}$$

assuming $g_{ds1} = g_{ds2}$ $g_{m3} = g_{m4}$

The dc common-mode voltage gain is,

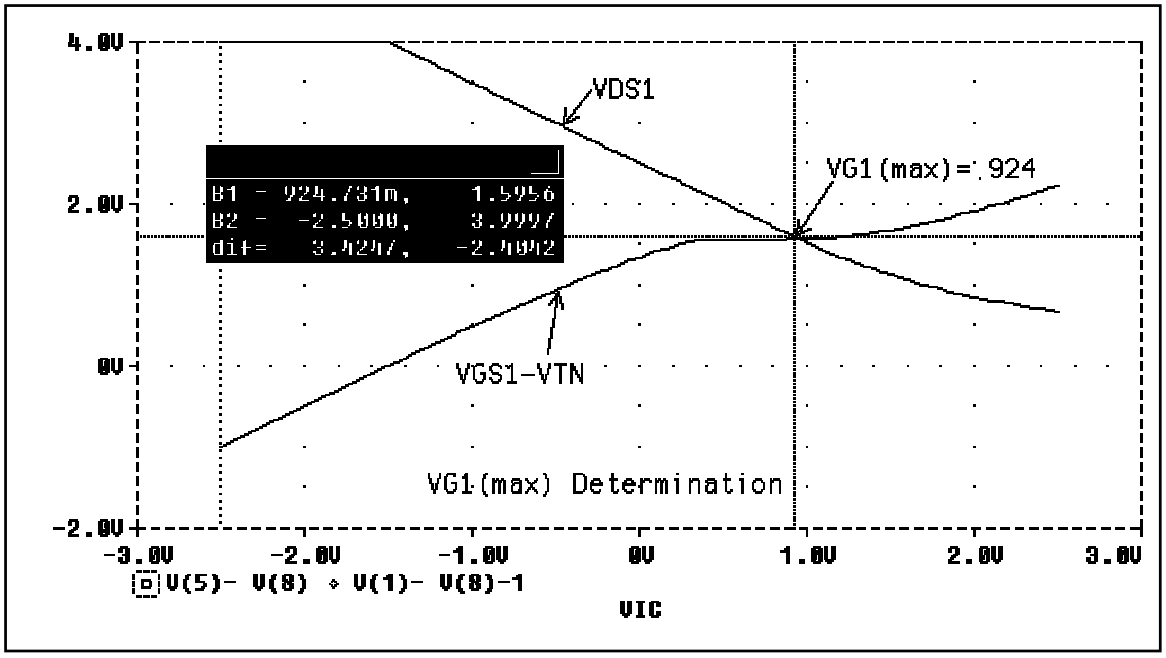
$$A_{VC0} = \frac{-y_{21}}{y_{22} + Y_L} = \frac{-\dfrac{2g_{m1}g_{ds5}}{2g_{ds1} + g_{ds5} + 2g_{m1}}}{\dfrac{2g_{ds1}g_{ds5}}{2g_{ds1} + g_{ds5} + 2g_{m1}} + 2(g_{ds3} + g_{m3})}$$

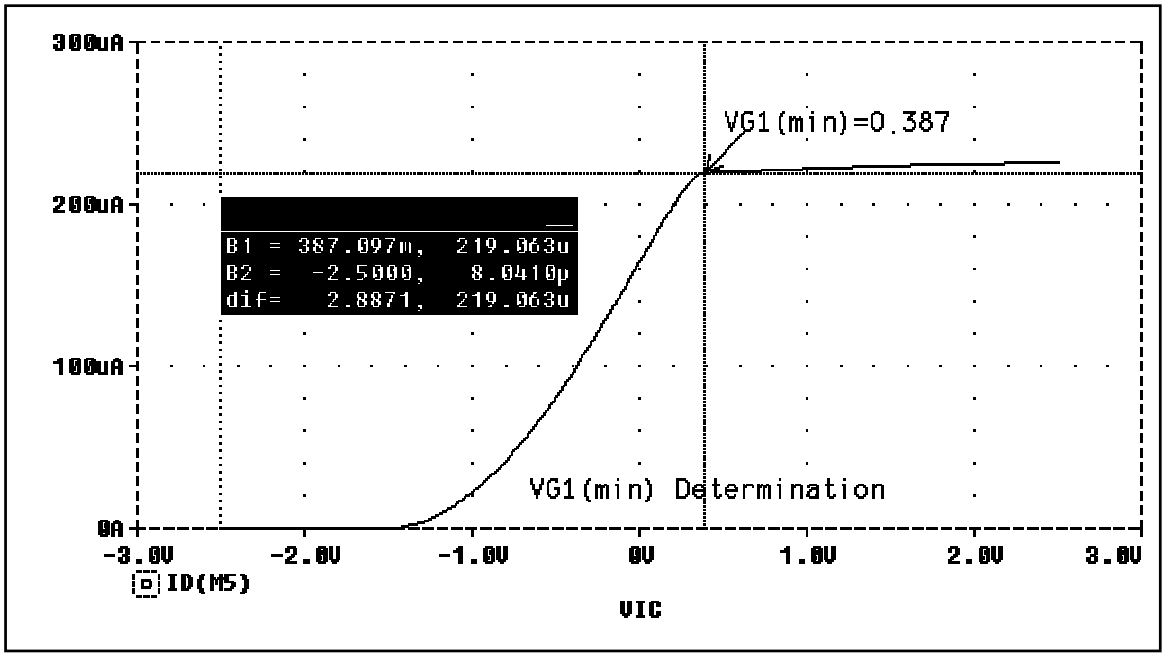
$$= \frac{-2g_{m1}g_{ds5}}{2g_{ds1}g_{ds5} + 2(g_{ds3} + g_{m3})(2g_{ds1} + g_{ds5} + 2g_{m1})}$$

$$= \frac{-\dfrac{g_{m1}}{g_{m3}}}{\dfrac{g_{ds1}}{g_{m3}} + 1 + \dfrac{2g_{ds1} + 2g_{m1}}{g_{ds5}}} \approx \frac{-\dfrac{g_{m1}}{g_{m3}}}{1 + 2g_{m1}r_{ds5}} \approx \frac{-\dfrac{g_{m1}}{g_{m3}}}{2g_{m1}r_{ds5}} \approx \frac{-1}{2g_{m3}r_{ds5}}$$

assuming $g_{m3} >> g_{ds3}$.

```
* Filename="diffvic.cir"
* MOS Diff Amp with Current Mirror Load
*DC Transfer Characteristics vs VIC
VID 7 0 DC 0V
E+ 1 10 7 0  0.5
E- 2 10 7 0 -0.5
VIC 10 0 DC 0V
VDD 3 0 DC 2.5VOLT
VSS 4 0 DC -2.5VOLT
M1 5 1 8 8  NMOS1  W=9.6U L=5.4U
M2 6 2 8 8  NMOS1  W=9.6U L=5.4U
M3 5 5 3 3  PMOS1  W=25.8U   L=5.4U
M4 6 5 3 3  PMOS1  W=25.8U   L=5.4U
M5 8 9 4 4  NMOS1  W=21.6U  L=1.2U
M6 9 9 4 4  NMOS1  W=100.8U  L=3.6U
M7 9 9 3 3  PMOS1  W=3.6U   L=3.6U
.MODEL NMOS1 NMOS VTO=1 KP=40U
+ GAMMA=1.0 LAMBDA=0.02 PHI=0.6
+ TOX=0.05U LD=0.5U CJ=5E-4 CJSW=10E-10
+ U0=550 MJ=0.5 MJSW=0.5 CGSO=0.4E-9 CGDO=0.4E-9
.MODEL PMOS1 PMOS VTO=-1 KP=15U
+ GAMMA=0.6 LAMBDA=0.02 PHI=0.6
+ TOX=0.05U LD=0.5U CJ=5E-4 CJSW=10E-10
+ U0=200 MJ=0.5 MJSW=0.5 CGSO=0.4E-9 CGDO=0.4E-9
.OP
.DC VIC -2.5 2.5 0.05V
.TF V(6) VIC
.PROBE
.END
```





$$A_{VCO} = -\frac{1}{2g_{m3}r_{ds5}} = -\frac{1}{2(139.1E-6)(.2272E6)} = -0.01582$$

This is very closed to the PSpice simulation result.

**** SMALL-SIGNAL CHARACTERISTICS

V(6)/VIC = -1.459E-02

INPUT RESISTANCE AT VIC = 1.000E+20

OUTPUT RESISTANCE AT V(6) = 2.386E+05

The goal of differential amplifier is to amplify the difference signal and to reject common-mode signal. A figure of merit called common-mode rejection ration (CMRR) is defined as:

$$\text{CMRR} = \left|\frac{A_{VD}}{A_{VC}}\right| = \left|\frac{31.5}{-0.01582}\right| = 1991.15$$

5. Differential Gain Frequency Response

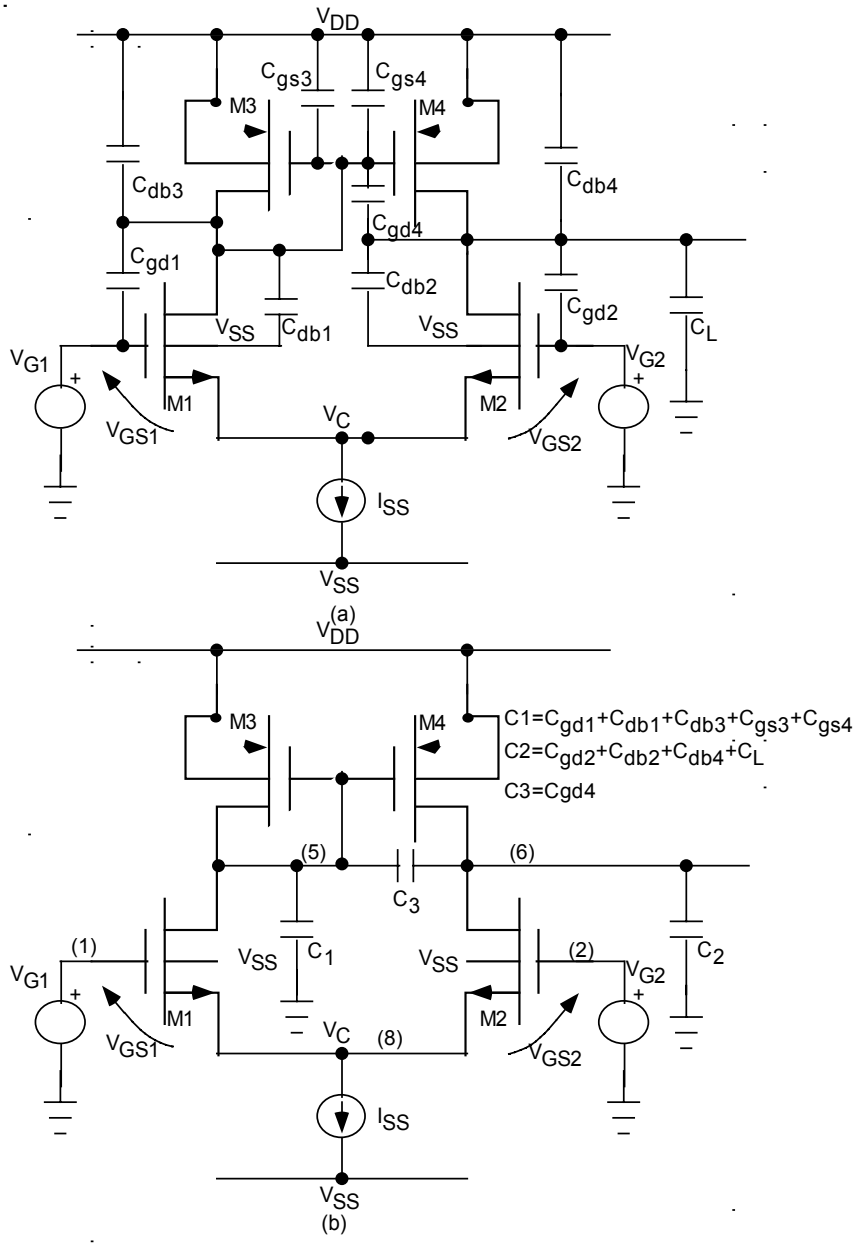


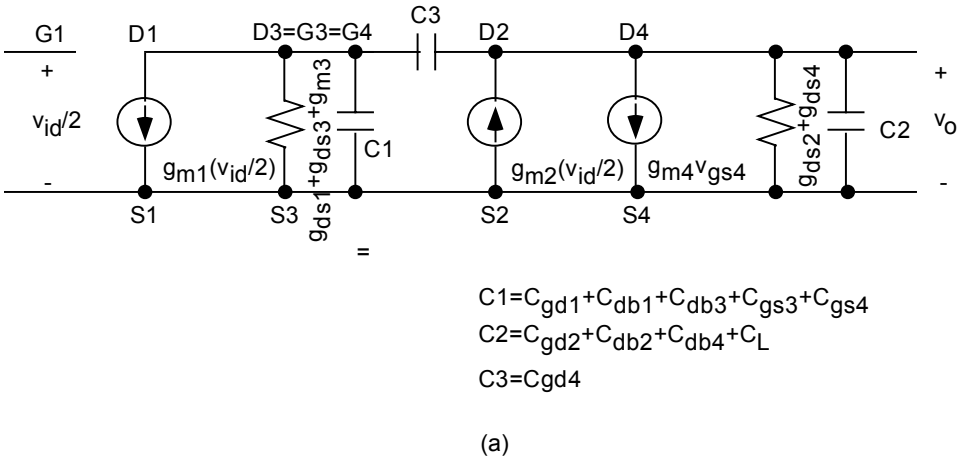
Figure 7. Parasitic Capacitances of Differential Amplifier Operating in Purely Differential Input Signal: (a) Parasitic Capacitances of each Transistor, (b) Lumped Parasitic Capacitances.

Figure 7(a) shows all the parasitic capacitances of the differential amplifier with purely differential input signals. Since both inputs are voltage sources, they are at ac ground when considering the effects of gate capacitances. Figure 7(b) shows that there are basically three capacitances. These are:

$$C_1 = C_{gd1} + C_{db1} + C_{db3} + C_{gs3} + C_{gs4}$$

$$C_2 = C_{gd2} + C_{db2} + C_{db4} + C_L$$

$$C_3 = C_{gd4}$$



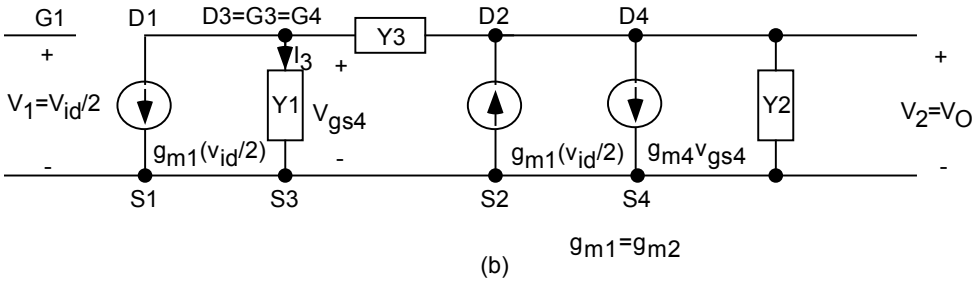


Figure 8. High Frequency Small Signal Equivalent Circuit: (a) Small Signal Equivalent Circuit Showing Lumped Capacitances, (b) Small Signal Equivalent Circuit Combining Capacitance and Resistance to Admittance.

NOTE C_3 is not a miller capacitance, it is connected between the outputs of the two inverter amplifiers, and not between an output and an input terminals of an amplifier. C_3 in this case is normally small and can be ignored. Figure 8(b) shows that the three admittances are given by:

$$Y_1 = g_{ds1} + g_{ds3} + g_{m3} + sC_1$$
$$Y_2 = g_{ds2} + g_{ds4} + sC_2$$
$$Y_3 = sC_3 = sC_{gd4}$$

The two-port Y parameters are to be determined. Figure 8(b) shows that the two-port variables are:

$$Y_L = 0$$
$$V_1 = V_{id}/2$$
and
$$V_2 = V_O$$

$$I_1 = 0$$

$$I_2 = Y_3(V_2 - V_{gs4}) - g_{m1}V_1 + g_{m4}V_{gs4} + Y_2V_2$$

$$= -g_{m1}V_1 + (Y_2 + Y_3)V_2 + (-Y_3 + g_{m4})V_{gs4}$$

At node D3

$$I_3 + g_{m1}V_1 - Y_3(V_2 - V_{gs4}) = 0$$

$$I_3 = Y_1V_{gs4}$$

$$Y_1V_{gs4} + g_{m1}V_1 - Y_3(V_2 - V_{gs4}) = 0$$

Solve for V_{gs4}

$$V_{gs4} = \frac{-g_{m1}}{Y_1 + Y_3}V_1 + \frac{Y_3}{Y_1 + Y_3}V_2$$

$$I_2 = -g_{m1}V_1 + (Y_2 + Y_3)V_2 + (-Y_3 + g_{m4})\left(\frac{-g_{m1}}{Y_1 + Y_3}V_1 + \frac{Y_3}{Y_1 + Y_3}V_2\right)$$

$$= \frac{-g_{m1}Y_1 - g_{m1}g_{m4}}{Y_1 + Y_3}V_1 + \frac{Y_1Y_2 + Y_1Y_3 + Y_2Y_3 + g_{m1}Y_3}{Y_1 + Y_3}V_2$$

The Y-parameter matrix is:

$$Y = \begin{bmatrix} 0 & 0 \\ \frac{-g_{m1}Y_1 - g_{m1}g_{m4}}{Y_1 + Y_3} & \frac{Y_1Y_2 + Y_1Y_3 + Y_2Y_3 + g_{m1}Y_3}{Y_1 + Y_3} \end{bmatrix}$$

For differential amplifier the assumption that Y3 or C3 is approximately 0 is valid. That is,

$$Y = \begin{bmatrix} 0 & 0 \\ -g_{m1} - \frac{g_{m1}g_{m4}}{Y_1} & Y_2 \end{bmatrix}$$

The differential gain is given by:

$$A_{VD2} = \frac{V_2}{V_1} = \frac{-y_{21}}{y_{22} + Y_L} = \frac{g_{m1} + \frac{g_{m1}g_{m4}}{Y_1}}{Y_2} = \frac{g_{m1}(1 + \frac{g_{m4}}{Y_1})}{Y_2}$$

$$= \frac{g_{m1}(1 + \frac{g_{m4}}{g_{ds1} + g_{ds3} + g_{m3} + sC_1})}{(g_{ds2} + g_{ds4} + sC_2)} = \frac{g_{m1}(g_{ds1} + g_{ds3} + g_{m3} + g_{m4} + sC_1)}{(g_{ds1} + g_{ds3} + g_{m3} + sC_1)(g_{ds2} + g_{ds4} + sC_2)}$$

$$= \left(\frac{g_{m1}}{g_{ds2} + g_{ds4}}\right) \frac{(g_{ds1} + g_{ds3} + g_{m3} + g_{m4})\left(1 + s\frac{C_1}{g_{ds1} + g_{ds3} + g_{m3} + g_{m4}}\right)}{(g_{ds1} + g_{ds3} + g_{m3})\left(1 + s\frac{C_1}{g_{ds1} + g_{ds3} + g_{m3}}\right)\left(1 + s\frac{C_2}{g_{ds2} + g_{ds4}}\right)}$$

$$= 2\left(\frac{g_{m1}}{g_{ds2} + g_{ds4}}\right) \frac{\left(1 + s\frac{C_1}{g_{ds1} + g_{ds3} + g_{m3} + g_{m4}}\right)}{\left(1 + s\frac{C_1}{g_{ds1} + g_{ds3} + g_{m3}}\right)\left(1 + s\frac{C_2}{g_{ds2} + g_{ds4}}\right)}$$

The differential gain when the input voltage V_1 is changed to V_{ID} is:

$$A_{VD} = \frac{V_O}{V_{id}} = \left(\frac{g_{m1}}{g_{ds2} + g_{ds4}}\right) \frac{\left(1 + s\frac{C_1}{g_{ds1} + g_{ds3} + g_{m3} + g_{m4}}\right)}{\left(1 + s\frac{C_1}{g_{ds1} + g_{ds3} + g_{m3}}\right)\left(1 + s\frac{C_2}{g_{ds2} + g_{ds4}}\right)}$$

$$= A_{VDO} \frac{(1 - \frac{s}{z})}{(1 - \frac{s}{p_2})(1 - \frac{s}{p_1})}$$

where :

$$p_1 = -\frac{g_{ds2} + g_{ds4}}{C_2}$$

$$p_2 = -\frac{g_{ds1} + g_{ds3} + g_{m3}}{C_1} \approx -\frac{g_{m3}}{C_1}$$

$$z = -\frac{g_{ds1} + g_{ds3} + g_{m3} + g_{m4}}{C_1} \approx -\frac{2g_{m3}}{C_1}$$

$p_1 << p_2 << z$

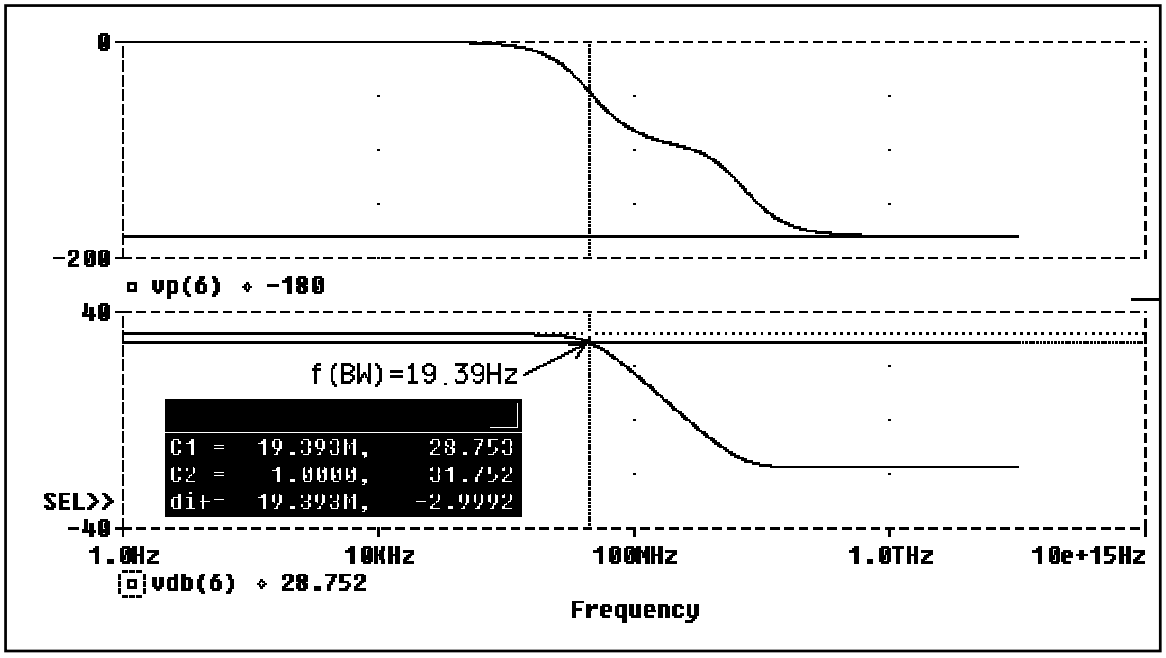
NOTE the differential voltage gain has pole-zero doublets. That is, the zero z is double that of the non-dominant pole p_2. The dominant (lowest frequency) pole p_1 occurs at the output node. The above transfer function can also be obtained by noting that each pole correspond to a node in the differential amplifier.

Each node is at a finite impedance with respect to ground. That is, each node there is a resistance R_n (or conductance) and capacitance C_n to ground. To determine which poles are dominant (or more significant), the impedance levels must be monitored. The parasitic capacitances C_n are of approximately the same magnitude, but R_n usually vary considerably. When the resistance (conductance) is high (low), a dominant pole is generated. The impedance levels are summarized in the follwing table:

Node(From Netlist)	Resistance	Capacitance	Pole
1	0 (ac ground)		X
2	0 (ac ground)		X
5	$R_5=1/(g_{ds1}+g_{ds3}+g_{m3)}$	C_1	$p_2=1/(R_5C_1)$*
6	$R_6=1/(g_{ds2}+g_{ds4)}$	C_2	$p_1=1/(R_6C_2)$
8	0 (ac ground)		X

The derivation shows that the pole p_2 create a zero doublet.

```
* Filename="diffreq.cir"
* MOS Diff Amp with Current Mirror Load
*DC Transfer Characteristics vs VID
VID 7 0 DC 0V  AC 1V
E+ 1 10 7 0  0.5
E- 2 10 7 0 -0.5
VIC 10 0 DC 0.65V
VDD 3 0 DC 2.5VOLT
VSS 4 0 DC -2.5VOLT
M1 5 1 8 8  NMOS1  W=9.6U       L=5.4U
M2 6 2 8 8  NMOS1  W=9.6U       L=5.4U
M3 5 5 3 3  PMOS1  W=25.8U      L=5.4U
M4 6 5 3 3  PMOS1  W=25.8U      L=5.4U
M5 8 9 4 4  NMOS1  W=21.6U      L=1.2U
M6 9 9 4 4  NMOS1  W=100.8U     L=3.6U
M7 9 9 3 3  PMOS1  W=3.6U       L=3.6U
.MODEL NMOS1 NMOS VTO=1 KP=40U
+ GAMMA=1.0 LAMBDA=0.02 PHI=0.6
+ TOX=0.05U LD=0.5U CJ=5E-4 CJSW=10E-10
+ U0=550 MJ=0.5 MJSW=0.5 CGSO=0.4E-9 CGDO=0.4E-9
.MODEL PMOS1 PMOS VTO=-1 KP=15U
+ GAMMA=0.6 LAMBDA=0.02 PHI=0.6
+ TOX=0.05U LD=0.5U CJ=5E-4 CJSW=10E-10
+ U0=200 MJ=0.5 MJSW=0.5 CGSO=0.4E-9 CGDO=0.4E-9
.AC DEC 100 1HZ 100000GHZ
.PROBE
.END
```



6. Common-Mode Frequency Response

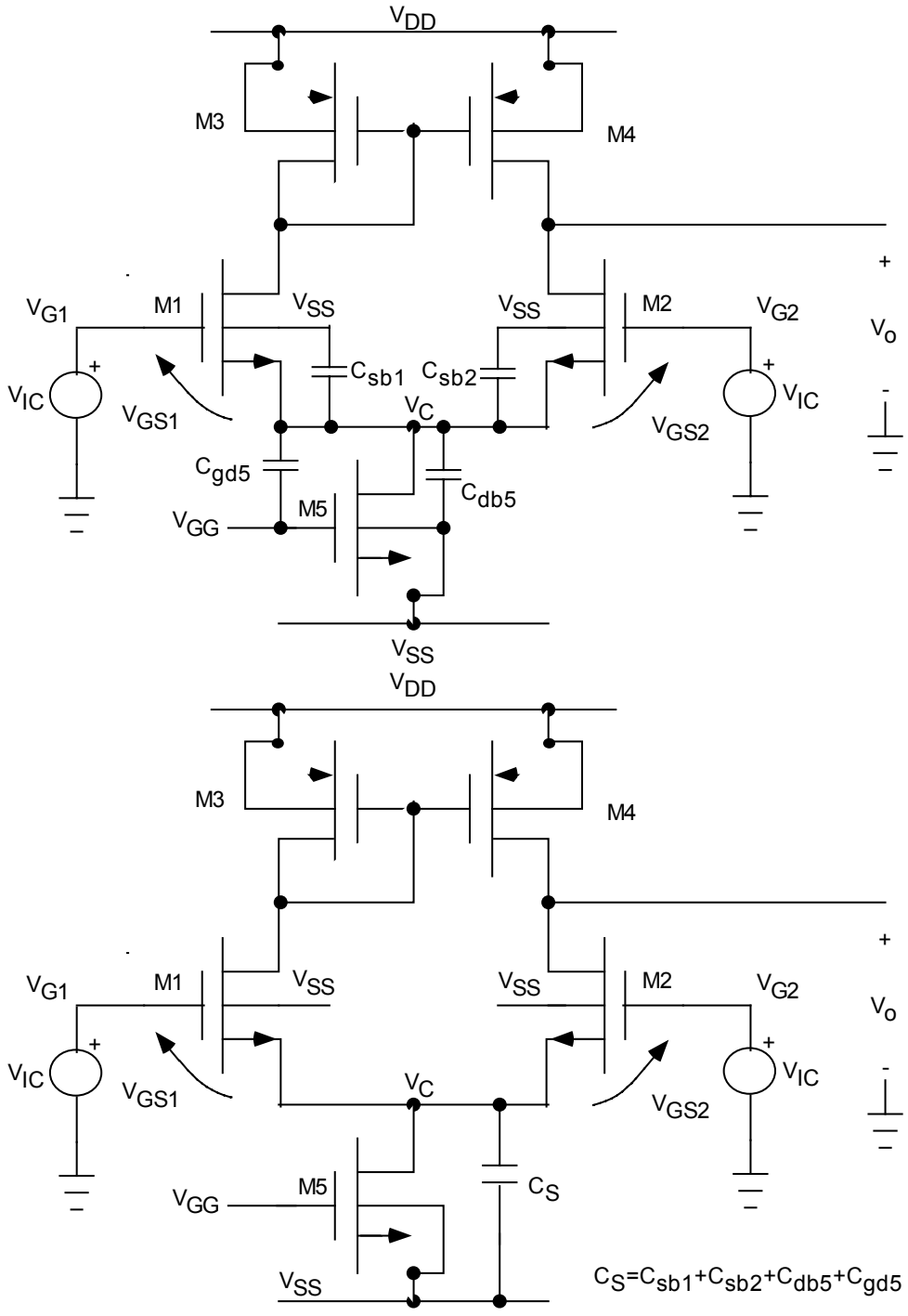


Figure 9. Differential Amplifier Operating in Pure Common-Mode Input Signal: (a) All Parasitic Capacitances at Common Node Vc, (b) Total Capacitances Across the Drain and Source of M5.

From the expression of the dc common-mode gain, it is primarily a function of g_{m3} and r_{ds5}. The first order frequency response analysis can be simplified by ignoring all parasitic capacitances except the capacitance C_S across r_{ds5}, see Figure 9. That is r_{ds5} is replaced by z_{ds5} in the the common-mode gain expression to account for frequency dependency.

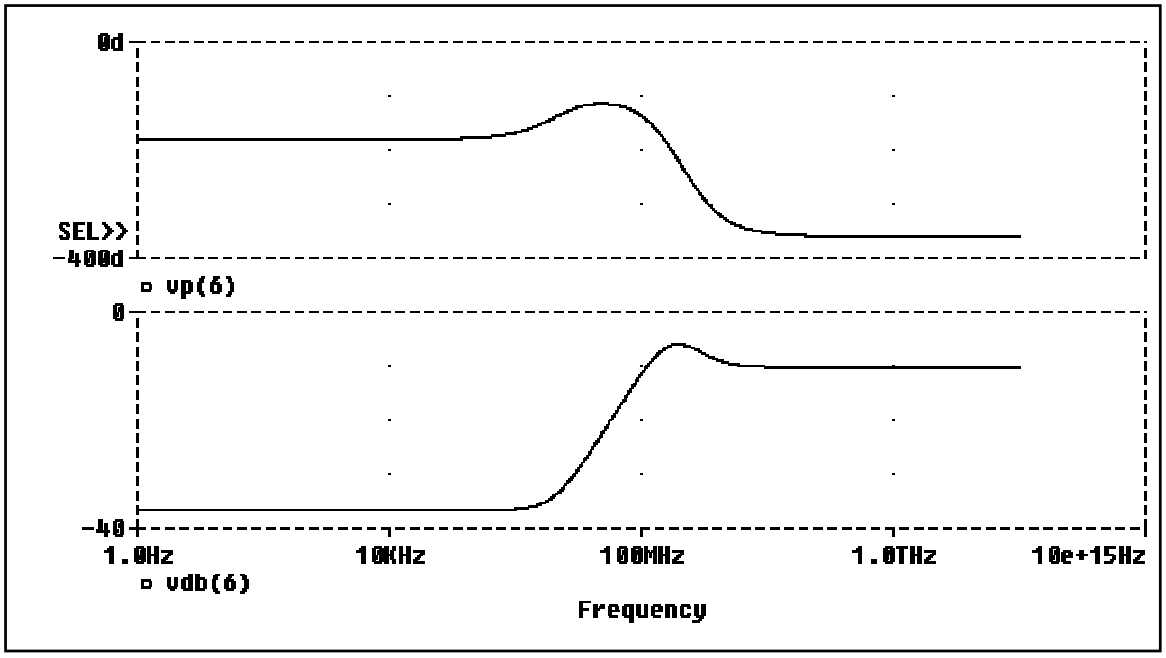
$$z_{ds5} = (r_{ds5} // C_S) = \frac{r_{ds5}}{1 + s r_{ds5} C_S}$$

$$A_{VC} = \frac{-1}{2 g_{m3} z_{ds5}} = \frac{-1}{2 g_{m3} \dfrac{r_{ds5}}{1 + s r_{ds5} C_S}} = \frac{-(1 + s r_{ds5} C_S)}{2 g_{m3} r_{ds5}}$$

where :

$$C_S = C_{sb1} + C_{sb2} + C_{db5} + C_{gd5}$$

```
* Filename="diffreqc.cir"
* MOS Diff Amp with Current Mirror Load
*DC Transfer Characteristics vs VIC
VID 7 0 DC 0V
E+ 1 10 7 0  0.5
E- 2 10 7 0 -0.5
VIC 10 0 DC 0.65V AC 1V
VDD 3 0 DC 2.5VOLT
VSS 4 0 DC -2.5VOLT
M1 5 1 8 8  NMOS1  W=9.6U       L=5.4U
M2 6 2 8 8  NMOS1  W=9.6U       L=5.4U
M3 5 5 3 3  PMOS1  W=25.8U      L=5.4U
M4 6 5 3 3  PMOS1  W=25.8U      L=5.4U
M5 8 9 4 4  NMOS1  W=21.6U      L=1.2U
M6 9 9 4 4  NMOS1  W=100.8U     L=3.6U
M7 9 9 3 3  PMOS1  W=3.6U       L=3.6U
.MODEL NMOS1 NMOS VTO=1 KP=40U
+ GAMMA=1.0 LAMBDA=0.02 PHI=0.6
+ TOX=0.05U LD=0.5U CJ=5E-4 CJSW=10E-10
+ U0=550 MJ=0.5 MJSW=0.5 CGSO=0.4E-9 CGDO=0.4E-9
.MODEL PMOS1 PMOS VTO=-1 KP=15U
+ GAMMA=0.6 LAMBDA=0.02 PHI=0.6
+ TOX=0.05U LD=0.5U CJ=5E-4 CJSW=10E-10
+ U0=200 MJ=0.5 MJSW=0.5 CGSO=0.4E-9 CGDO=0.4E-9
.AC DEC 100 1HZ 100000GHZ
.PROBE
.END
```



The differential-mode voltage gain decreases with increasing frequency but common-mode voltage increases. Therefore, CMRR decreases with increasing frequency.

7. Designing Differential Amplifier With Specified CMR

Given a common-mode range of –0.75 <= V_{IC} <=0.75 , V_{GG}=-1, I_{SS}=I_{DS5}=100uA, L_{min}=5.4u, $\Delta V = V_{GS} - V_{TN} = 0.5$. Determine the size of each transistor in the differential amplifier circuit, see Figure 4.

1. Determine the $(W/L)_5$ to sink 100uA.

$$I_{DS5} = \frac{\beta_{N5}}{2}(V_{GS5} - V_{TN5})^2 = \frac{K_N}{2}\left(\frac{W}{L}\right)_5 (V_{GS5} - V_{TN5})^2$$

$$\left(\frac{W}{L}\right)_5 = \frac{2I_{DS5}}{K_N(V_{GS5} - V_{TN5})^2} = \frac{2I_{DS5}}{K_N(V_{GG} - V_{SS} - V_{TN5})^2}$$

$$= \frac{2(100E-6)}{(40E-6)[-1-(-2.5)-1]^2} = 20 = \left(\frac{108u}{5.4u}\right)$$

2. Determine $(W/L)_1$ =$(W/L)_2$ from $V_{IC}(min)$=$V_{G1}(min)$ specification

From Eq(26),

$$V_{IC} = V_{G1}(\min) = V_{SS} + V_{DS5(SAT)} + V_{GS1} \geq -0.75$$

$$V_{GS1} \geq -0.75 - V_{SS} - V_{DS5(SAT)} = -0.75 - (-2.5) - 0.5 = 1.25$$

$$\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2 = \frac{2I_{DS1}}{K_N(V_{GS1} - V_{TN})^2} = \frac{2(50E-6)}{(40E-6)(1.25-1)^2} = 40 = \left(\frac{216u}{5.4u}\right)$$

3. Determine (W/L)3=(W/L)4 from $V_{IC}(max)=V_{G1}(max)$ specification

From Eq(25),

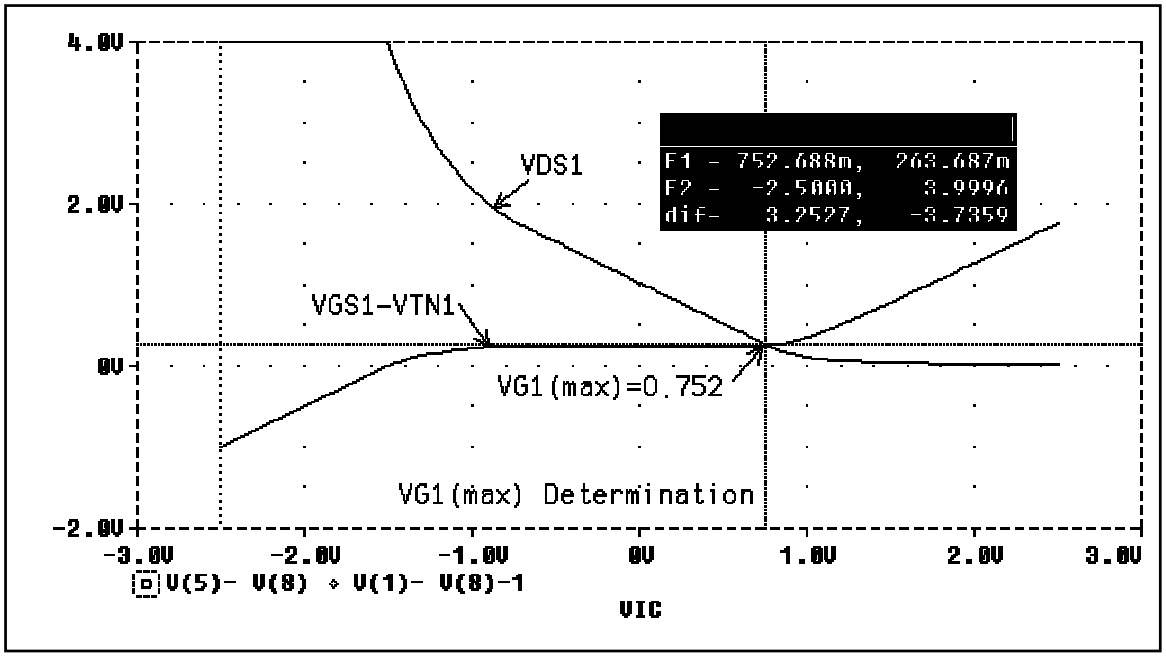
$$V_{IC}(max) = V_{G1}(max) = V_{DD} - \sqrt{\frac{2|I_{DS3}|}{\beta_{P3}}}$$

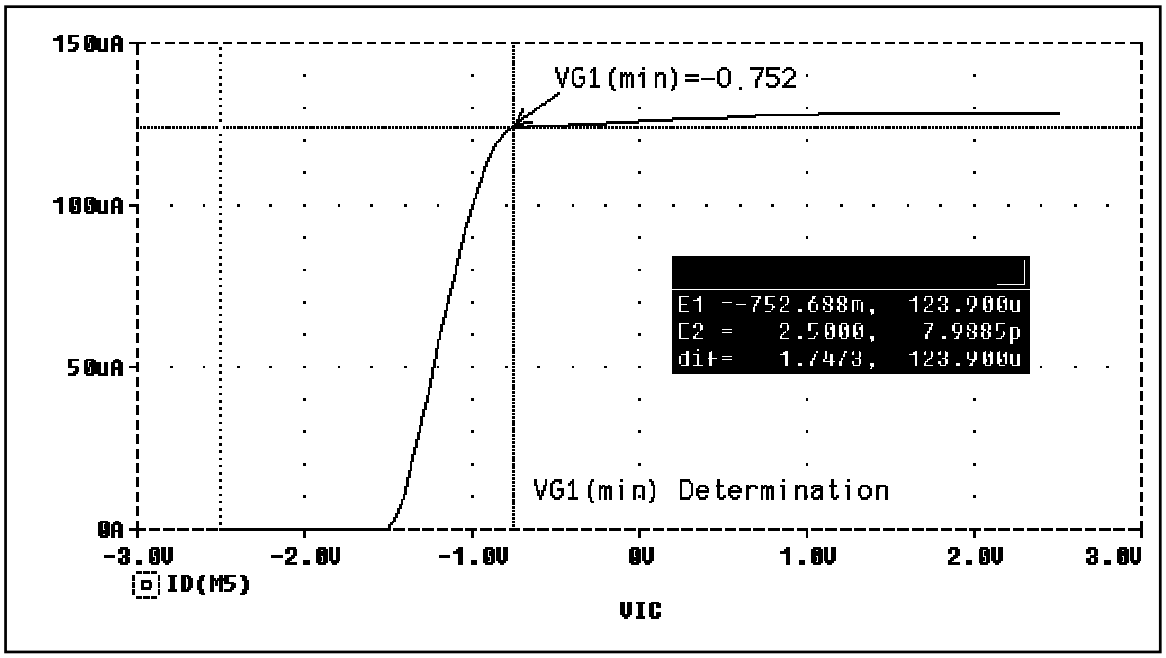
$$|I_{DS3}| = \frac{\beta_{P3}}{2}(V_{DD} - V_{G1}(max))^2 = \frac{K_P}{2}\left(\frac{W}{L}\right)_3 (V_{DD} - V_{G1}(max))^2$$

$$\left(\frac{W}{L}\right)_3 = \frac{2|I_{DS3}|}{K_P(V_{DD} - V_{G1}(max))^2} = \frac{2(50E-6)}{(15E-6)(2.5-0.75)^2} = 2.177 = \left(\frac{11.75u}{5.4u}\right)$$

The above is simulated using PSpice. The results agree well with the calculations.

```
* Filename="diffcmr.cir"
* MOS Diff Amp with Current Mirror Load
*DC Transfer Characteristics vs VIC
VID 7 0 DC 0V
E+ 1 10 7 0  0.5
E- 2 10 7 0 -0.5
VIC 10 0 DC 0V
VDD 3 0 DC 2.5VOLT
VSS 4 0 DC -2.5VOLT
M1 5 1 8 8  NMOS1  W=216U       L=5.4U
M2 6 2 8 8  NMOS1  W=216U       L=5.4U
M3 5 5 3 3  PMOS1  W=11.75U     L=5.4U
M4 6 5 3 3  PMOS1  W=11.75U     L=5.4U
M5 8 9 4 4  NMOS1  W=108U       L=5.4U
VGG 9 0 DC -1V
.MODEL NMOS1 NMOS VTO=1 KP=40U
+ GAMMA=1.0 LAMBDA=0.02 PHI=0.6
+ TOX=0.05U LD=0.5U CJ=5E-4 CJSW=10E-10
+ U0=550 MJ=0.5 MJSW=0.5 CGSO=0.4E-9 CGDO=0.4E-9
.MODEL PMOS1 PMOS VTO=-1 KP=15U
+ GAMMA=0.6 LAMBDA=0.02 PHI=0.6
+ TOX=0.05U LD=0.5U CJ=5E-4 CJSW=10E-10
+ U0=200 MJ=0.5 MJSW=0.5 CGSO=0.4E-9 CGDO=0.4E-9
.DC VIC -2.5 2.5 0.05V
.TF V(6) VIC
.PROBE
.END
```


4.0V
2.0V
0V
-2.0V
-3.0V
-2.0V
-1.0V
0V
1.0V
2.0V
3.0V
VDS1
VGS1-VTN1
VG1(max)=0.752
VG1(max) Determination
F1 = 752.688m, 268.687m
F2 = -2.5000, 3.9996
dif= 3.2527, -3.7359
V(5)- V(8) * V(1)- V(8)-1
VIC


150uA
100uA
50uA
0A
-3.0V
-2.0V
-1.0V
0V
1.0V
2.0V
3.0V
VG1(min)=-0.752
VG1(min) Determination
E1 =-752.688m, 123.900u
E2 = 2.5000, 7.9885p
dif= 1.7473, 123.900u
ID(M5)
VIC