Diplomarbeit:

Design of an integrated full differential operational amplifier in a 0.35um CMOS-AMS technology.

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Abstract :

This paper explains the choice made for a full differential operational amplifier. This op amp has been designed for the first stage of a pipelined A/D Converter (ADC). This means that it has the highest specification of every op amp of all stages, as it concerns the LSB of the ADC. It shows also the solution founded to reach high gain and short settling time, without degrading too much the output swing.

First the operational amplifier specification are explained; the different structures tested are then presented and the motivation of the final topology choice are shown. It presents then the op amp schematic implementation, the simulation results and the layout with the 0.35um CMOS-AMS design kit.

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1. Introduction

1.1 Introduction

1.1.1 General considerations

For a long time, Analog to Digital Converters (ADCs) have been used widely in digital equipment. Recently, the applications for ADCs have expanded widely as many electronic systems that used to be entirely analog have been implemented using digital electronics. Examples of such applications include digital telephone transmission, cordless phones, transportation, and medical imaging. Furthermore, ADCs have found their way into systems taht would normally be considered as being entirely digital as these digital systems are pushed to higher levels of performance. Data storage is one example of such a system. As storage density in disk drive systems is increased, the signals handled by the read circuitry have become increasingly analog character. Presently, 6-bit ADCs are commonly used in read circuits of disk drives.

Frequently, ADCs are integrated with other functions on a single monolithic device. Because the ADC must share the power budget with other functions on the integrated circuit, power dissipation is often an important consideration. Furthermore, many new applications, such as cordless phones and cellular phones, require portability and battery operation.

Operational amplifier (op amps) are an integral part of many analog and mixed signal systems. The design of op amps continues to pose a challenge as the supply voltage and transistor channel lengths scale down with each generation of CMOS technologies. This op amp, as usual, is used to implement a closed loop system, which is a sample/hold for the first stage of a pipelined ADC. The first requirement is the accuracy of this first pipeline stage, which means that this op amp should have a high open loop gain.

1.1.2 ADC Definition and characterization

An analog to digital converter (ADC) is a device that converts real world (analog) signals into digital codes. ADC are characterized in a number of different ways to indicate the performance capability, cost and ease to use. The resolution describes the fineness of the quantization performed in the ADC. As the resolution increase, the input-output charasteristic of the ADC better approximates a straight line. The transfer function for an ideal version of such an ADC progresses from low to high in a series of uniform steps.

1.2 The use of operational amplifier in ADC topology

The desired resolution of a pipeline A/D converter determines the MDAC (multiplying D/A converter) operational amplifier signal swing and open loop DC gain, while the gain-bandwidth product is also affected by the sampling speed specifications. Slew rate is totally dedicated to the speed requirements. A large signal swing is desired because of the sensitivity to kT/C noise, amplifier thermal noise and substrate coupling are minimized if the internal dynamic ranges of the ADC are high.

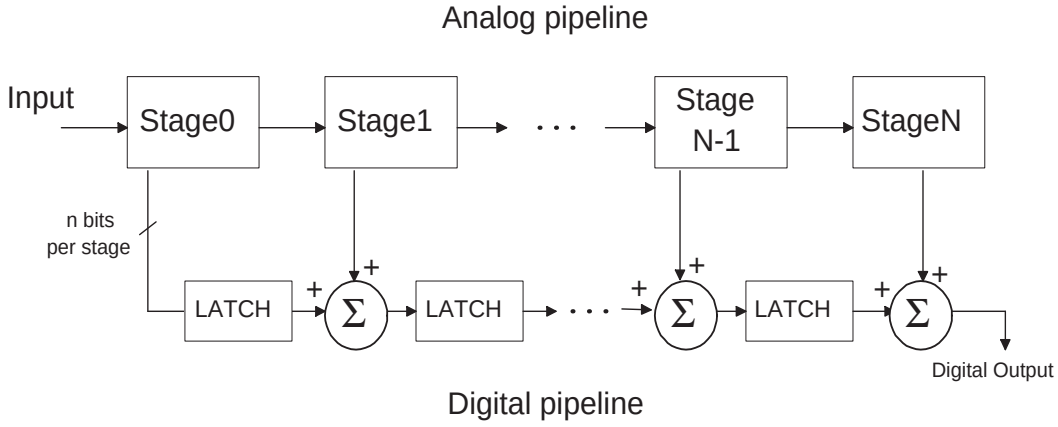

Fig. 1.1 Overall topology of the ADC.

1.3 The need of high specifications

Every stage of the ADC cares for a certain number of bits (fig. 1.2).

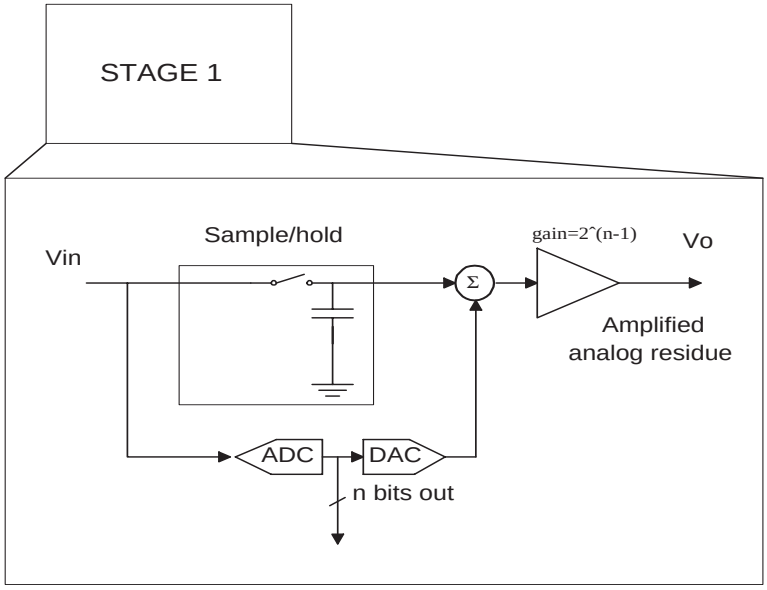

Fig. 1.2 Pipelined ADC stage 1 example.

Each pipeline stage consists of two parts, an analog arithmetic unit called multiplying D/A converter (MDAC), and a n-bit sub-ADC.

The aim of the work is to design the gain amplifier to generate the analog voltage residue. As this is the first stage, the error generated by this amplification must be the less important compared to any other stage. This mean that the error generated must be under 1 LSB.

2. Specifications

2.1 Signal to Noise Ratio (SNR) definition

The signal to noise ratio (SNR) is the ratio of signal power to noise power in the output of the operational amplifier. One way to plot the SNR is to plot the spectrum of the output of the operational amplifier. The SNR is calculated by measuring the difference between the signal peak and the noise floor and including a factor to adjust for the number of samples used to generate the spectrum as shown below :

$$SNR(dB) = signalpeak(dB) - noisefloor(dB) - 10LogN$$

The last term in the above equation may be understood as follows. To generate an N point fast Fourier transform (FFT) of a signal, N samples of the signal are taken. Sampling the signal N times increases the signal energy by a factor of N^2, and the noise by a factor of N. Thus the ratio of signal power to noise power in increased by a factor of N and the signal to noise ratio of the FFT is higher than the signal to noise ratio in one sample of the signal. The signal to noise ratio improvement in dB is 10Log(N). Thus, the noise floor in the FFT becomes lower relative to the signal as more samples are taken. The idea is illustrated in the following fig. 2.1.

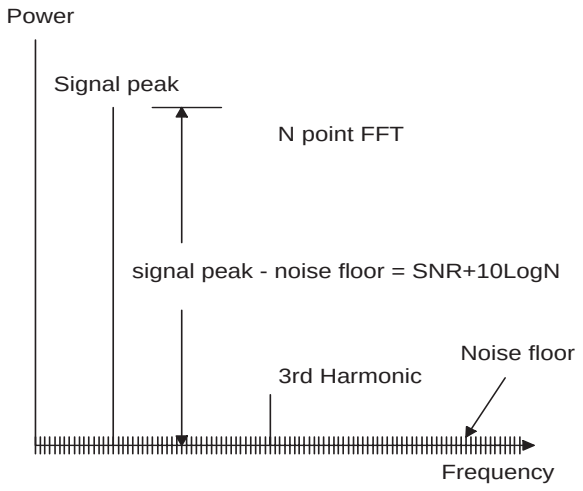

Fig. 2.1 Procedure for computing SNR from an N point FFT.

2.2 Signal Distortion to Noise Ratio (SNDR) definition

The signal to noise plus distortion ratio (SNDR) is often used to measure the performance of an ADC. It measures the degradation due to the combined effect of noise, quantization errors, and harmonic distortion. The SNDR of a system is usually measured for a sinusoidal input and is a function of the frequency and amplitude of the input signal. When a sinusoide signal of a single frequency is applied to a system, the output of the system generally contains a signal component at the input frequency. Due to distortion, the output also contains signal components at harmonics of the input frequency. An ADC usually samples an input signal at some finite rate. As a result, some of the harmonic distortion products are aliased down to lower frequencies. Furthermore, the ADC adds noise to the output, and this noise generally present to some degree at all frequencies. The SNDR of the ADC is defined as the ratio of the signal power in the fundamental to the sum of the power in all of the harmonic, all of the aliased harmonics, and all of the noise.

2.3 Power Supply Rejection Ratio (PSRR) definition

Noise on the power supply lines can couple into the output signal of an operational amplifier and so of an ADC. The power supply rejection ratio (PSRR) measures how well an op amp resists this distortion. It is the ratio of supply noise power to output noise due to the power supply noise

2.4 Common Mode Rejection Ratio (CMRR) definition

The CMRR reflects the amount of common-mode input voltage that is amplified or, in other words, the asymetry in the input devices and load resistors. Typical values are 60 dB for CMOS transistor stages (up to 80dB for fully differential topologies). It is calculated as illustrated in fig. 2.2.

This calculation is made in the lowest value when the input common mode is set in the input common mode scale.

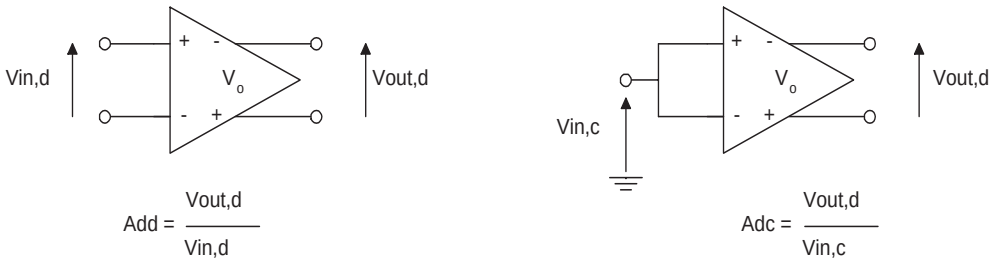

Fig. 2.2 CMRR calculation.

2.5 Power dissipation

Power dissipation is becoming an important ADC and op amp specification because many device are being implemented in portable systems powered by a battery with limited energy. Reducing power dissipation can reduce system weight or improve battery life. Reducing power dissipation can also make it easier to keep the temperature of the chip at a reasonable level.

2.6 Slew rate

The slew rate measures the maximum output slope of a signal. For a simple op-amp connected in inverter configuration, this output limitation is shown in fig. 2.3.

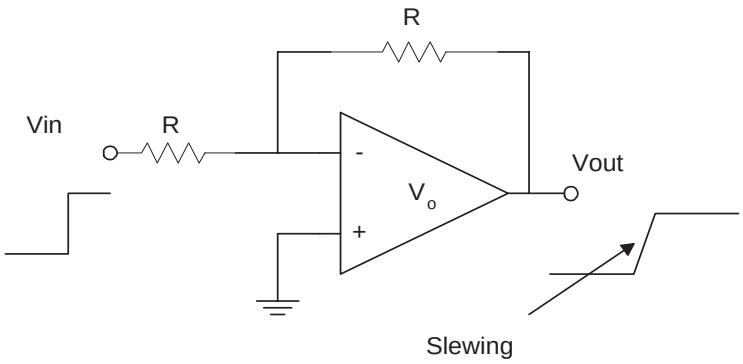

Fig. 2.3 Slew rate issue.

It is calculated as following :

$$Sr = Max\left(\frac{d}{dt}Vout\right)$$

The slew rate is important when the settling time is a concerning issue.

2.7 Settling time

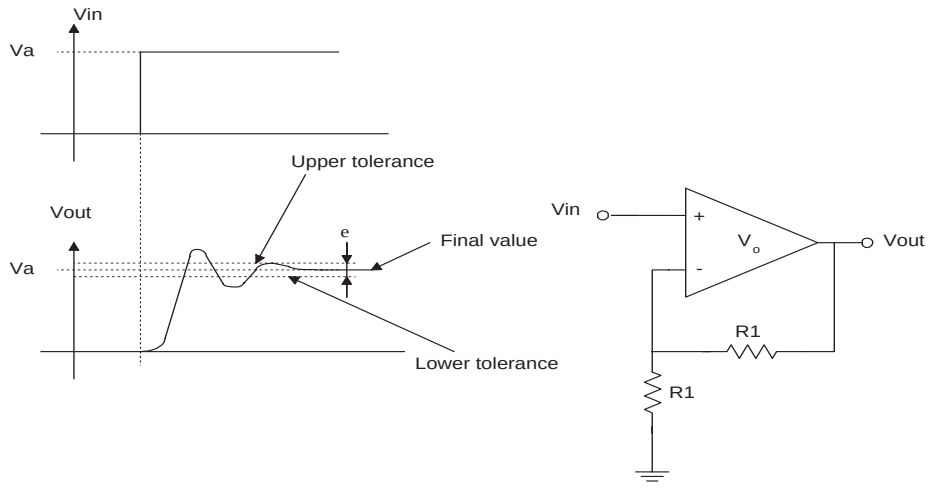

Fig. 2.4 Settling time calculation.

For a single pole small signal model, the first part of the curve is limited by the slew rate of the op amp, and the second part corresponds to an exponential settling. The calculatiton method is explained in fig. 2.4.

In a switched capacitor topology, the settling time should be less than the sampling period with an accuracy less than 1 LSB/2

2.8 Noise

In low noise applications, the input -referred noise of op amps becomes critical. With many transistor in an op amp, it may seem difficult to intuitively identify the dominant source of noise.

2.8.1 Thermal noise

Noise in a resistor is primarily the result of random motion of electrons due to the thermal effect. This type of noise is then called thermal noise, or Johnson noise

Thermal noise is characterized by adding a parallel current generator to the resistor. The root mean square value of the current generator, or voltage generator is given by :

$$\sqrt{\overline{i^2}} = \sqrt{\frac{4kT}{R}}\sqrt{B} \qquad \sqrt{\overline{v^2}} = \sqrt{4kTR}$$

The value of this noise generator can include or not the bandwidth over which the noise calculation is made.

2.8.2 1/f (flicker) noise

The interface between the gate oxide and the silicon substrate in a MOSFET entails an interesting phenomenon. Since the gate oxide cristal reaches an end at this interface, many “dangling” bonds appear, giving rise to extra energy states. As charge carriers move to the interface, some are randomly trapped and later released by such eneergy states, introducing “flicker” noise in the drain current of the transistor. In addition to trapping, several other mechanisms are believed to generate flicker noise

The 1/f noise can be modeled by an RMS noise source given by :

$$\sqrt{\overline{v^2}} = \sqrt{\frac{K}{f \times Cox \times W \times L}}$$

2.8.3 kT/C noise

A resistor charging a capacitor gives rise to a total rms noise of $\sqrt{\frac{kT}{C}}$
The similar effect occurs in sampling circuits. The on resistance of a the switch introduces a thermal noise at the output, and when the switch turns off, this noise is stored on the capacitor

along the instantaneous value of the input voltage. It can be proved that the rms voltage of the sampled noise in this case is approximativeley equal to $\sqrt{\frac{kT}{C}}$

As the operational amplifier will be integrated in a switched capacitor topology, in order to achieve a low noise, the sampling capacitor must be sufficiently large. A 17pF capacitor has been choosen, reducing the rms noise down to 4uV.

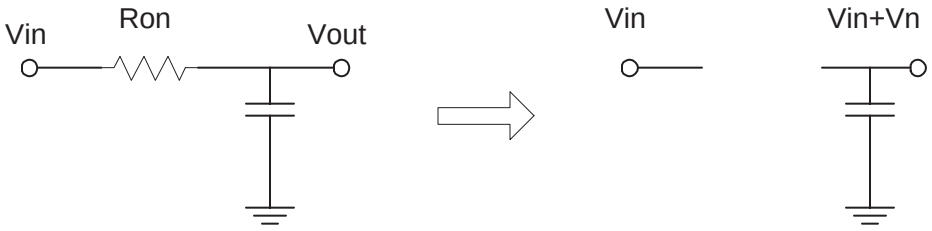

Fig. 2.5 Noise concern in switched capacitor topology.

2.9 Spurious free dynamic range

The spurious free dynamic range is the ratio of the input signal level for a maximum SNDR to the input signal level for 0dB SNDR. This measure of dynamic range is useful because it indicates the amount of dynamic range that can be obtained before distortion becomes dominant over noise. The next page (fig. 2.6) shows how to determine serious free dynamic range form a plot of SNDR versus input level.

2.10 Open loop DC gain

The open loop DC gain requirement of the amplifier can be determined from the tolerable gain error at the output of each pipelined ADC stage.

Assuming that the error due to the finite open loop DC gain of the operational amplifier (A0), in each stage of a n bit/stage pipeline A/D converter is e, the total error of the converter reduced to the input is also approximatively equal to when the number of the stage is large. To assure a total error less than LSB/2, in the input of an N-bit converter, the open loop DC gain must be at least

$$Ao > 2^{N+1}$$

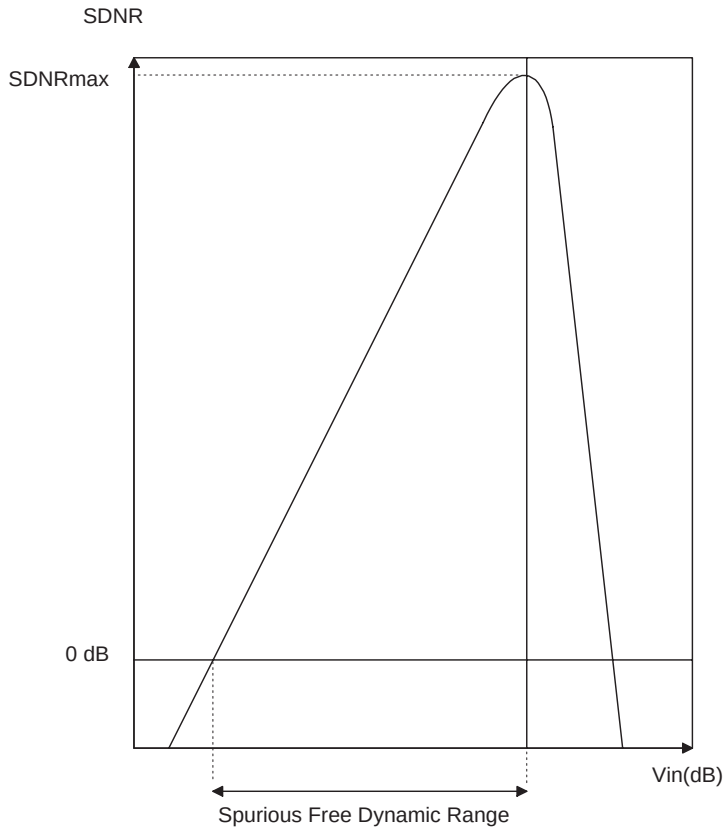

Fig. 2.6 Signal to Noise + Distortion ratio versus input signal level

3. Theoretical approach of operational amplifier

3.1 Simple single ended operational amplifier

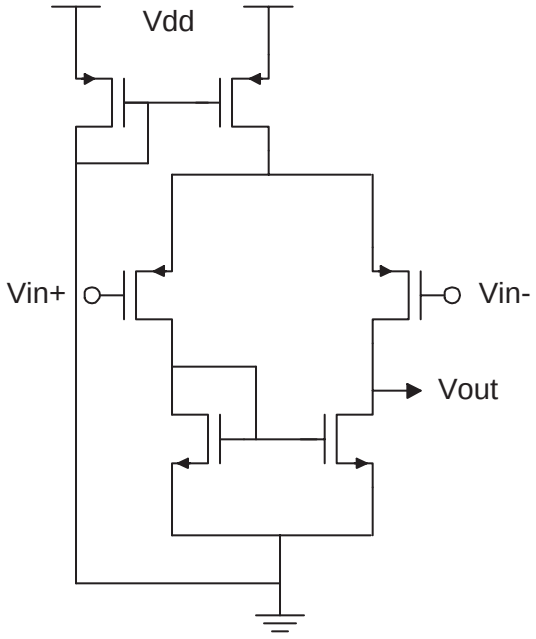

Fig. 3.1 Simple single ended operational amplifier with pmos input transistor.

The first operational amplifier, the simplest, is the simple pmos input transistor with nmos load transistor shown in fig. 3.1. It has the advantage to present a great output dynamic range, as shown in the following fig. 3.2. In fact one can expect to reach an output swing of :
Swing = Vdd-2*Vds,sat-Vth

This structure can't provide the gain required, because the output resistance seen from the drain of the input transistor can only reach maximum values around 100KOhms. This means that multiplied by a maximum gm of the input transistor of 5mS, the maximum gain provided by this structure is around 40 dB. Nevertheless, this structure will be useful for the future structure.

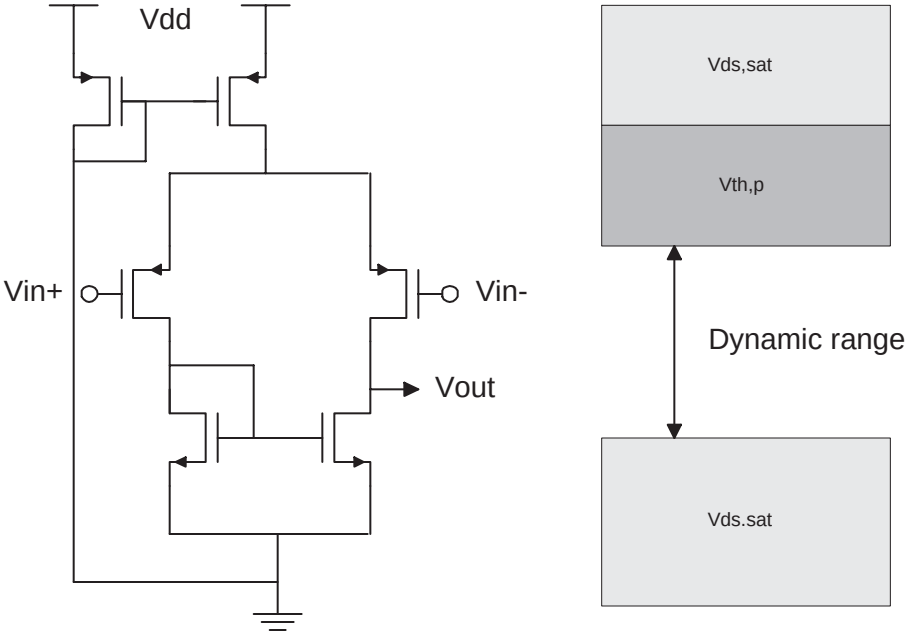

Fig. 3.2 Output swing of a simple single ended topology.

Mirrored poles structures reduces high frequency performance with single ended structure. The gain curve of this type of simple structure is given below in Fig. 3.3

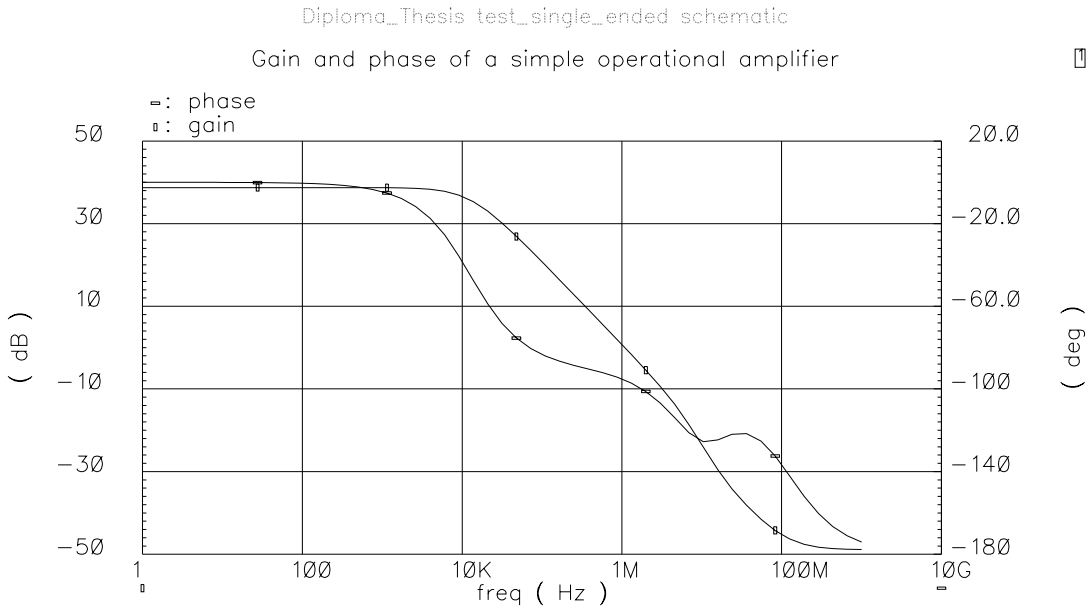

Fig. 3.3 Gain and Phase curve of a simple single ended topology.

Nevertheless, this structure will be useful for other application, mainly for the gain boosting.

3.2 Full differential operational amplifier

Using full differential implementations suppresses even-order harmonics and allow sufficient open-loopgain such that the closed feedback system achieves adequate linearity It is interesting to note that in many feedback circuits, the linearity requirement, rather than the gain error requirement, governs the choice of open loop gain.

Fully differential amplifier also have the advantage that the signal swing at the output is two times larger than the output signal swing of their single ended counterpart. This point can be understood by considering the case when Vdd=3V, Vss=0 and Vcm=1.5 V. For a single ended output op-amp, the maximum output voltage is 1.5 V. However, for the full-differential amplifier, the total output voltage, which is the difference between the two output signal, is 3V. The result is an increase in the dynamic range of circuits employing full differential signal paths.

3.2.1 General topology

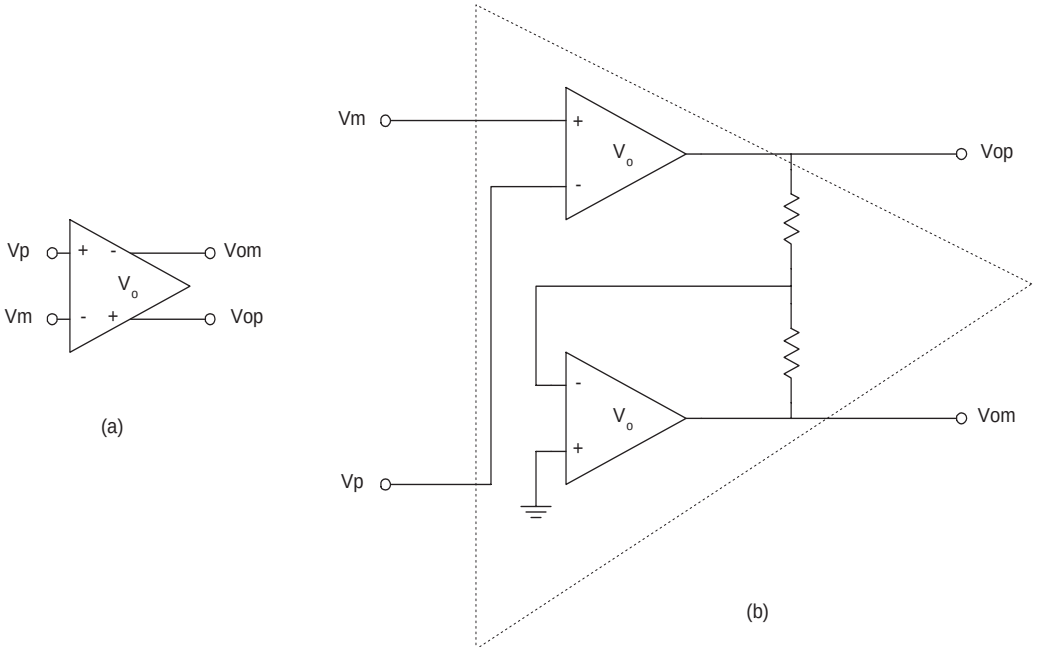

Fig. 3.4 Formation of a differential output op-amp using two single ended op-amp.

The differential output op-amp is shown in Fig. 3.4 (a). The open-loop gain of the op-amp is given in terms of the inputs and outputs by :

$$Adiff = \frac{Vop - Vom}{Vp - Vm} \qquad A\text{sin}gle = \frac{Vo}{Vp - Vm}$$

Where Adiff is the gain in differential configuration and Asingle is the gain in a single ended topology. One can use two single ended op-amps to form a differential output op-amp (fig. 3.4 (b)). This implementation works well at low frequency, but for higher frequency, other configuration have to be used.

3.2.2 Common mode feedback (CMFB) topology

3.2.2.1 Understanding the need of CMFB

The CMFB is necessary when designing a fully differential operational amplifier. If we look at a single ended operational amplifier, the DC level is set by the current mirror. For a full differential operational amplifier, the common mode is largely depending on the bias voltage of the current source. This mean that for a process variation, the gain is largely depending on the accuracy of these bias voltage. The following fig. 3.5 shows the DC gain without a common mode feedback

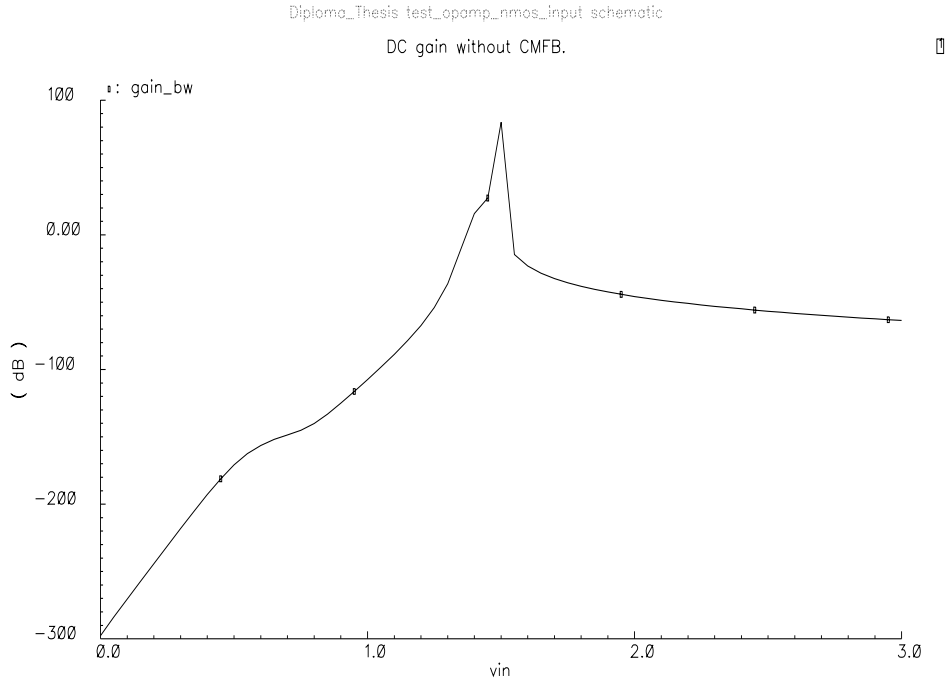

Fig. 3.5 DC gain towards input common mode without CMFB.

One can see on the Figure, that the operational point founded is not stable in the sense that a small deviation of the input common mode changes the DC gain in a really large extend.
An additional circuit that set the common voltage to a desire value can largely decrease the dependence of the gain towards the different bias voltage. Below, the fig. 3.6 shows the DC gain dependance on the input common mode with a common mode feedback. Clearly, one has to fix the common mode level in order to make the gain not so dependant on the input common mode.

In fact, a Monte Carlo analyse of the DC gain with and without CMFB shows that the DC point obtained is “unstable”; this type of simulation is more detailled later; let’s say that the simulator makes varying several paramaters to simulate process variations. The result of Monte Carlo simulation without CMFB is given in fig. 3.7.

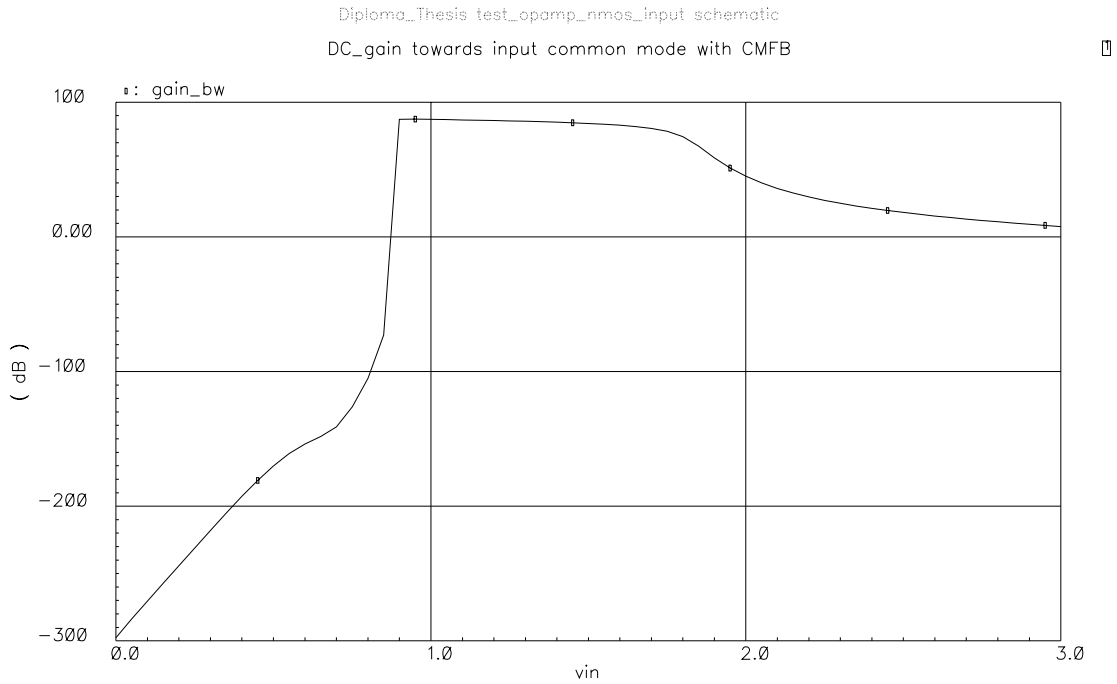

Fig. 3.6 DC gain with CMFB.

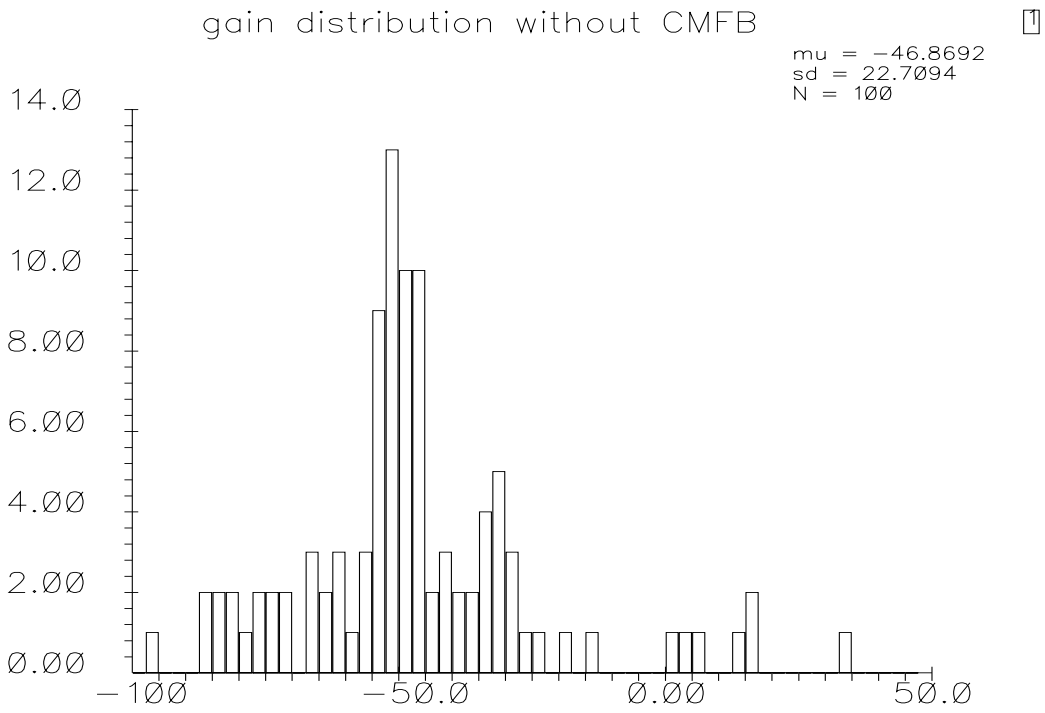

Fig. 3.7 DC gain distribution without CMFB. Monte Carlo analyse.

There are two approach to design CMFB circuits : a continuous time approach and a switch capacitor approach.

3.2.2.2 Continuous time CMFB

This method is described in fig. 3.8. It is composed of 2 parts : the Common mode level sensing bloc and the comparator.

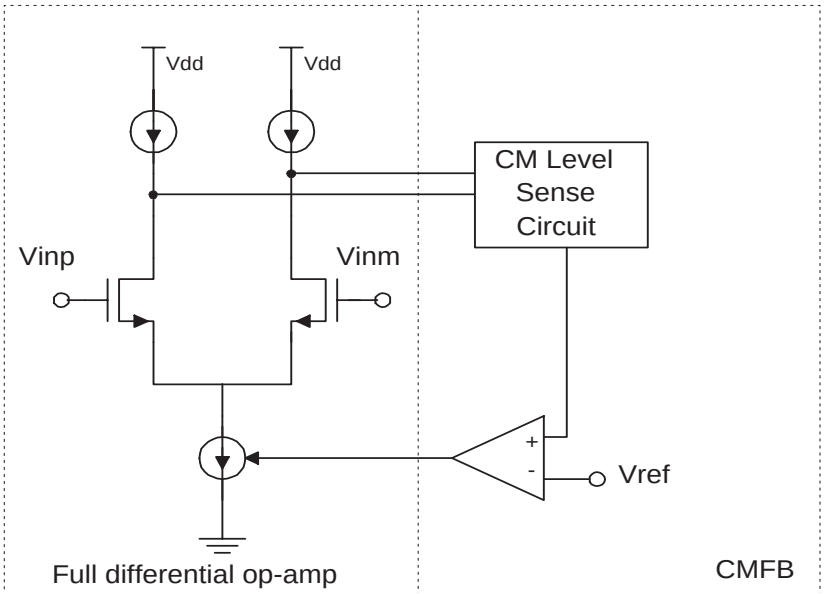

Fig. 3.8 Conceptual approach of CMFB.

The first part is sensing the level of the common mode and the second is comparing this level to a voltage reference. This means that it sense the difference between the output common mode level and the reference voltage.

The output of the comparator can then correct the current in the input stage. When the common mode level in increasing, the current in the input branch is increased to increase the current flowing in the PMOS load transistor. On the opposite case, the current is decreased when the common mode level is decreasing.

3.2.2.3 Sensing structure

First, one have to sense the common mode; in order not to disturb the output signal, large resistance can be used, such as 10 Mohm.

The most simple structure to sense the common mode level is evaluate the average of the two output. At first order, the following topology can be right to generate such a value.

The following fig. 3.9

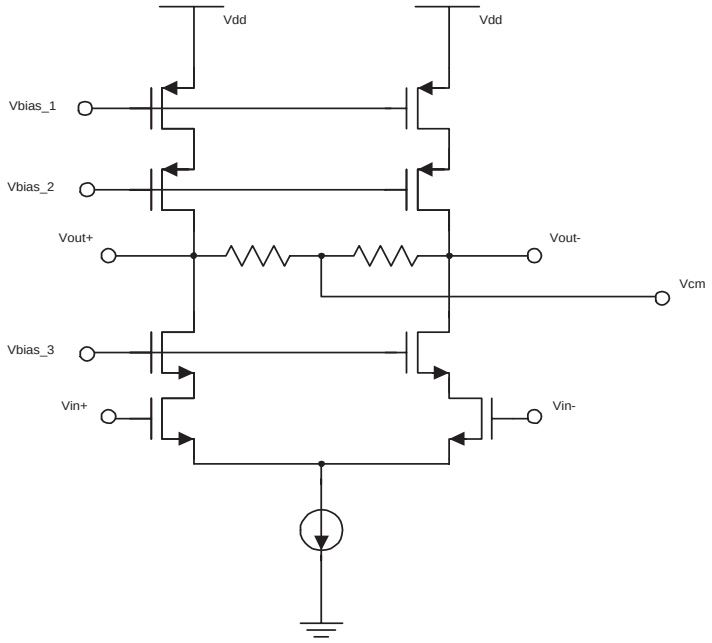

Fig. 3.9 CMFB structure with simple resistance level sensing.

In order not to decrease the gain of the operational amplifier, big resistance need to be used. The trouble is that such big resistance (1Mohm) can not be integrated. So a buffer can be inserted between the output and the resistance Fig. 3.10, so that the sensing resistance can be decreased to 100 Ohms.

The problem is that with this circuit, the Common mode level is decreased of a Vgs from its initial value, and after then the comparator needs to be designed with such DC input level. The other problem is the need of a compensation circuit in order to compensate the CMFB circuit. In large signal, this feedback circuit can generates oscillations such as in fig. 3.11. This is due to the phase

rotation of the first stage, the buffer and the comparator.

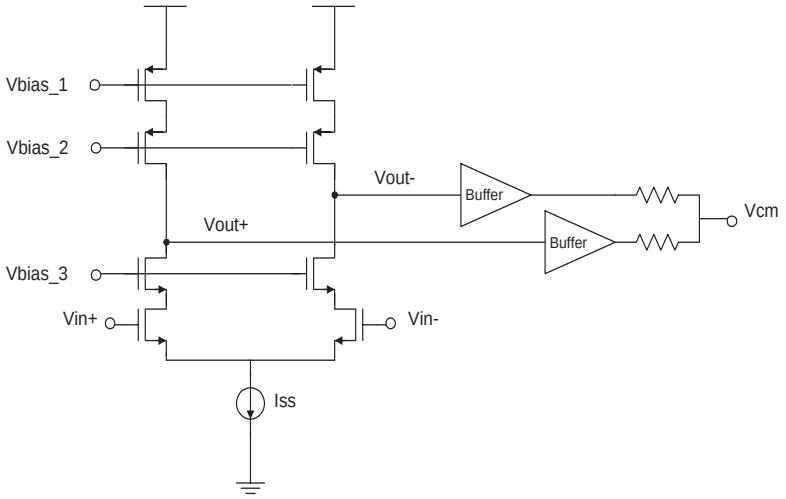

Fig. 3.10 Buffer sensing method.

3.2.2.4 Comparator design

The comparator is used in the amplification zone; this is named comparator, because at the input, the output common mode is compared to a fixed voltage reference. The comparator is used to sense the average of the common mode. The following fig. 3.12 shows the structure of such a comparator.

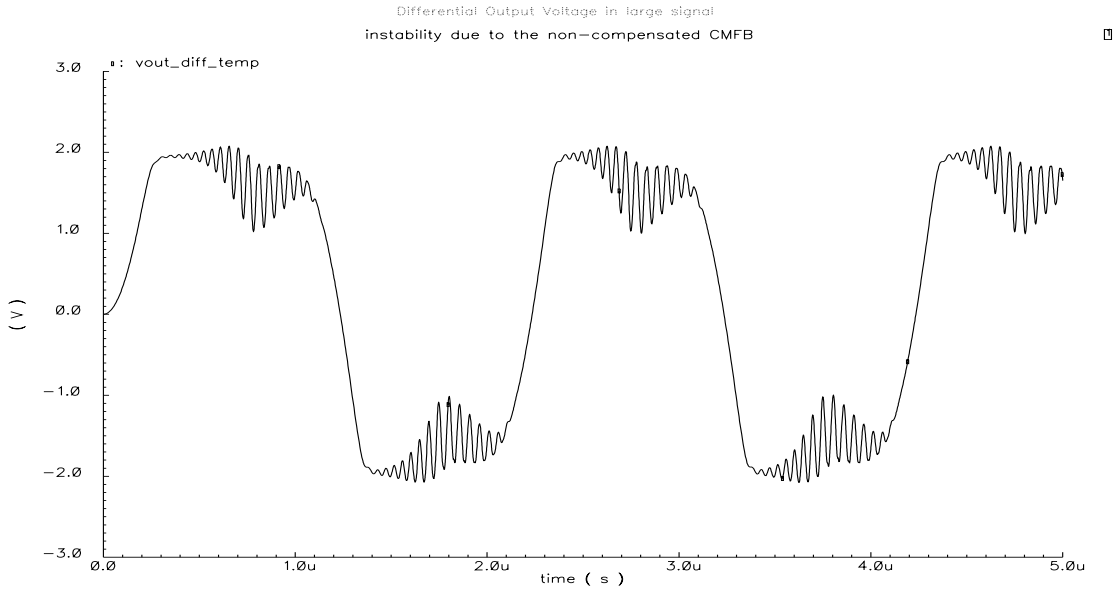

Fig. 3.11 Output oscillations. No CMFB compensation circuit.

3.2.2.5 Switched capacitor CMFB

As the ADC has a switched capacitor topology, it can be useful to use the command signal to adjust the Common mode level of the operational amplifier. In addition, switched capacitor common mode feedback allow larger output swing as continuous-time topologies, because it can sample any level between Vdd and Gnd. This is done by using transmission gate for the switches that are connected to the output.This structure of the switched capacitor CMFB is shown in fig. 3.13.

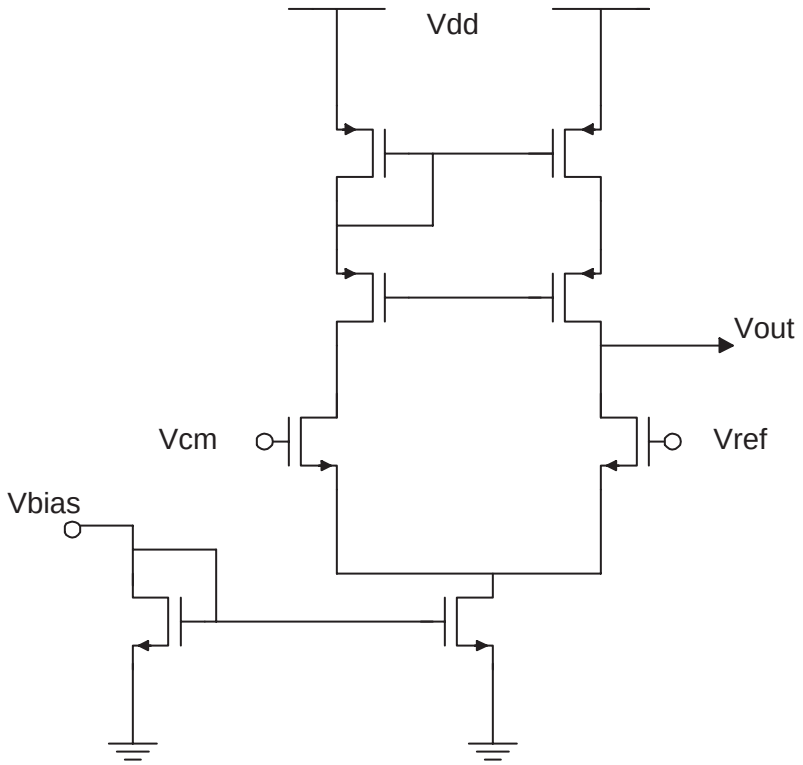

Fig. 3.12 Comparator used for CMFB.

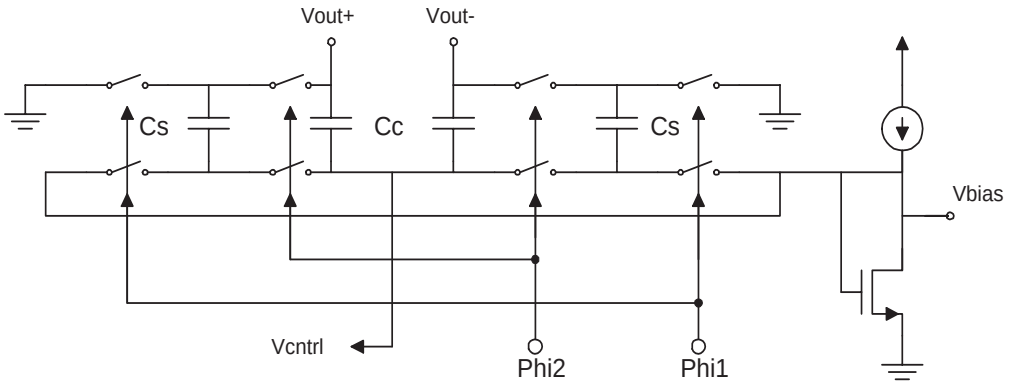

Fig. 3.13 : A switched-capacitor CMFB circuit.

In this approach, the Cc capacitance generate the average of the output signals.

The DC voltage across Cc is determined by Cs which are switched between bias voltage and between being connected in parallel with Cc. The output curve with Phi1 signal is shown in Fig. 3.14.

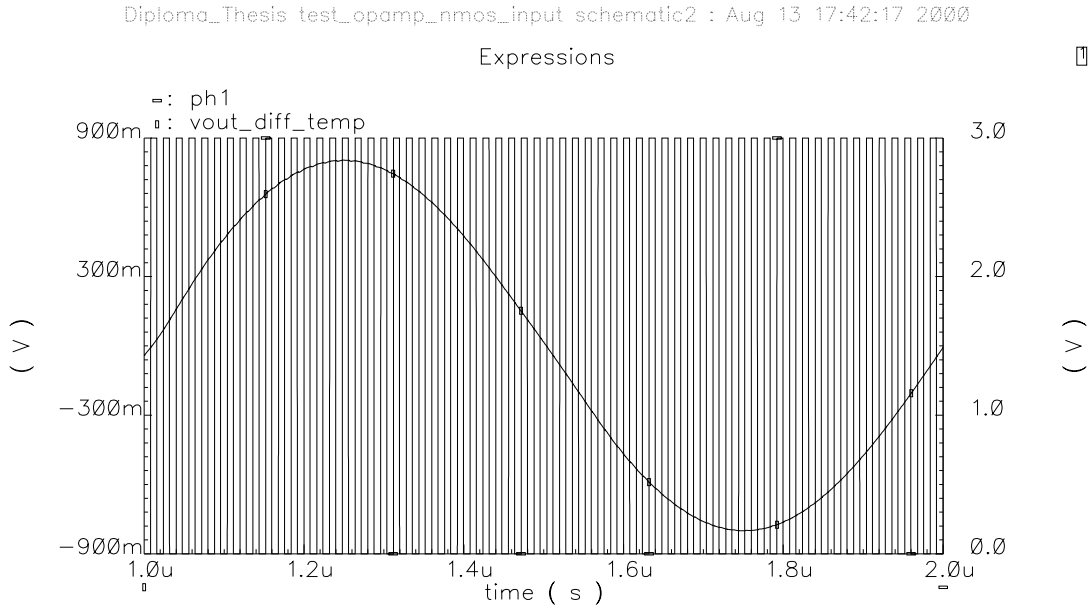

Fig. 3.14 Output signal with switched capacitor CMFB.

The problem is the non linearity introduced by the use of switch connected directly to the output. The next purpose was to decrease this non linearity with the use of different switch topology.

3.2.2.6 Switch care

Non linearity introduced by switched capacitor CMFB at the output can be explained by effect of charge injection. One has to seek for a injection charge cancelling method.

3.2.2.6.1 Dummy switch

To arrive at the first technique, one can assume that the charge injected by M1 can be removed by means of a second transistor M2 (fig. 3.15).

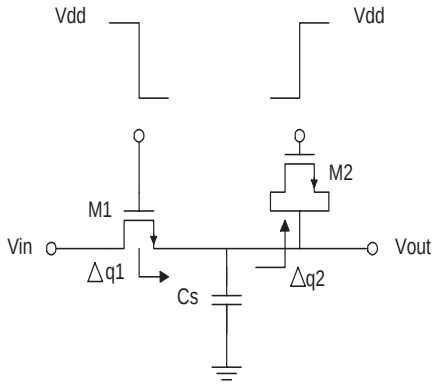

Fig. 3.15 Dummy switch use.

One can suppose that half of the chanel charge of M1 is injected onto Cs, so :

$$\Delta q1 = \frac{W1 \times L1 \times Cox}{2}(Vdd - Vin - Vth1)$$

$$\Delta q2 = W2 \times L2 \times Cox(Vdd - Vin - Vth2)$$

Choosing W2=W1 / 2 and L2 = L1 will cancel in first order the charge injected.
Unfortunately, the assumption of equal splitting of charge between source and drain is generally invalid, making this approach less attractive. Another approach is to use both NMOS and PMOS in a complementary structure.

3.2.2.6.2 Complementary switch

Using a NMOS and a PMOS in parallel allows electrons and holes injection at the output; one has

to design properly the size of this two devices (fig. 3.16).

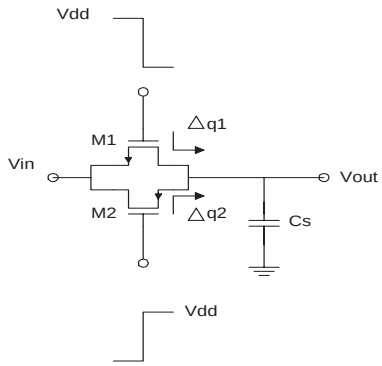

Fig. 3.16 Complementary transistor to reduce charge injection.

The charge injection is cancelled if the following equation is fullfilled :

$$W1 \times L1 \times (Vdd - Vin - Vthn) \;=\; W2 \times L2 \times (Vin - |Vthp|)$$

Thus the cancellation occurs for only one input level. Charge injection is a concerning issue.

3.2.3 Slew rate

The slew rate is depending on the compensation capacitance and on the gm of the input stage. As the whole phase margin is not that high, one can avoid decreasing this capacitance. The solution should be to increase the current flowing in this capacitance.

When a large signal is applied on the input transistor, one of the two input transistor turns off. This explains that the slope of each branch is Iss/(2 x Cc) and so the difference exhibits a slew rate equal to Iss/Cc. This is shown in the following fig. 3.17.

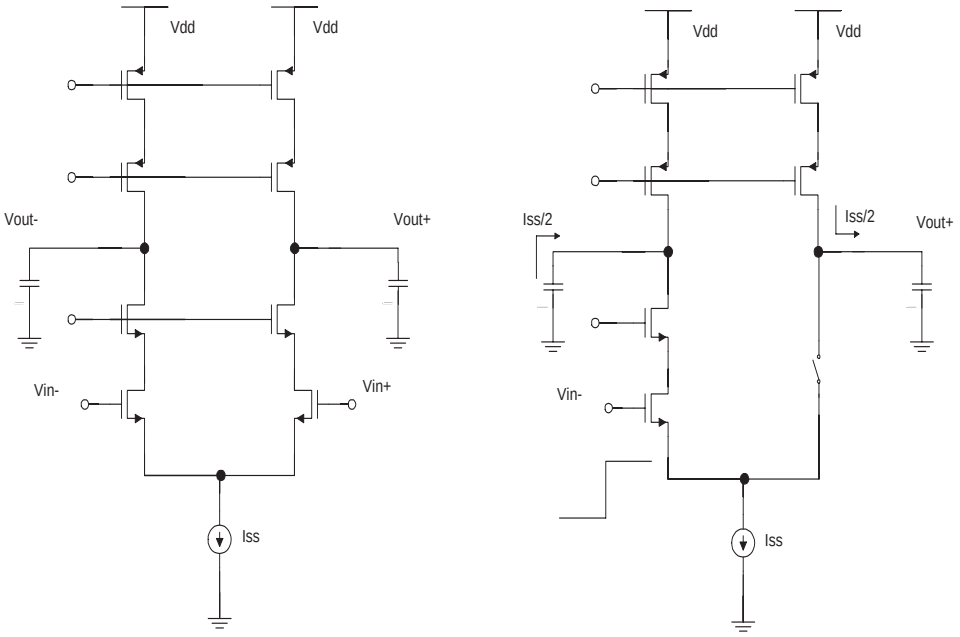

Fig. 3.17 Current flowing when step function at the input.

3.3 Folded cascode structure

3.3.1 Topology description

In order to alleviate the drawback of telescopic cascode op amps, namely, limited output swing, a “folded cascode” op amp can be used (fig. 3.18). The primary advantage of the folded structure lies in the choice of the voltage levels because it does not “stack” the cascode transistor on top of the input device. The lower swing of the output is given by Vds,sat3+Vds,sat5, and the upper end by Vdd-(Vds,sat7+Vds,sat9)

. Thus the peak to peak swing on each side is around Vdd-4*Vds,sat.

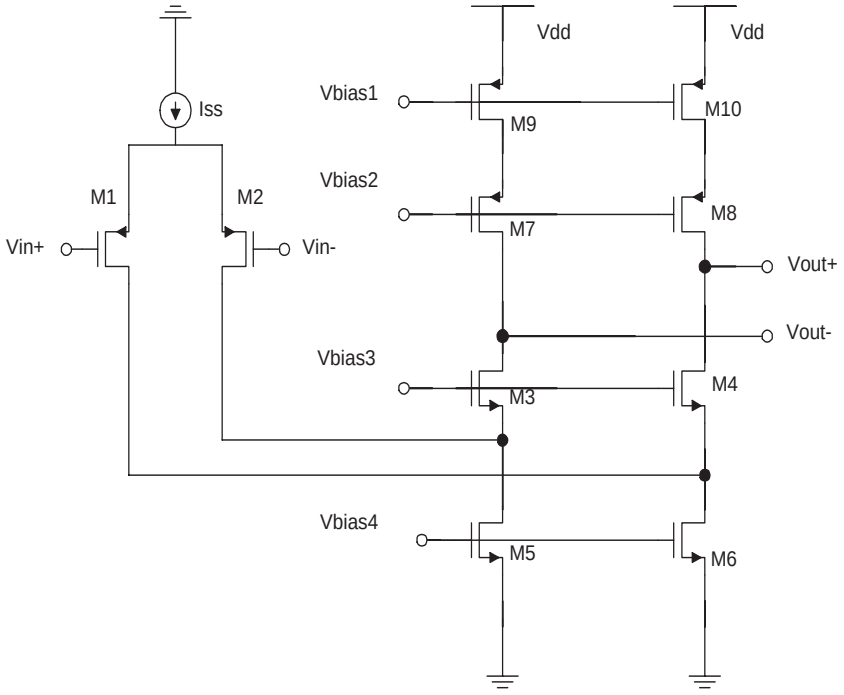

Fig. 3.18 Folded cascode structure.

3.3.2 Gain calculation

One can examine the small signal voltage gain of this topology.

Using the half circuit depicted in fig. 3.19 (a), and writing that |Av|=Gm*Rout, we must calculate the equivalent Gm and Rout.As shown in Fig. 3.19 (b), the output of the circuit current is approximatively equal to the drain current of M1, as the impedance seen looking into the source of M3 is much lower than Ron1||Ron5.

$$(gm3 + gmb3)^{-1} \left|\right| Ron3 \ll Ron1 \left|\right| Ron5$$

Thus Gm =gm1. To calculate Rout, we use the equivalent circuit of fig. 3.19. where Rop=(gm7+gmb7)Ron7*Ron9 to write that :

$$Rout \approx Rop \left|\right| [(gm3 + gmb3) Ron3 (Ron1 \left|\right| Ron5)]$$

How to compare with the gain of a telescopic cascode structure ? For comparable device

dimensions and bias current, the PMOS input differential pair exhibits a lower transconductance than does an NMOS pair. Furthermore, Ron1 and Ron5 appear in parallel reducing the output impedance, especially because M5 carries the current of both the input device and the cascode branch. As a consequence, the gain is usually two or three times lower than of a comparable telescopic cascode.

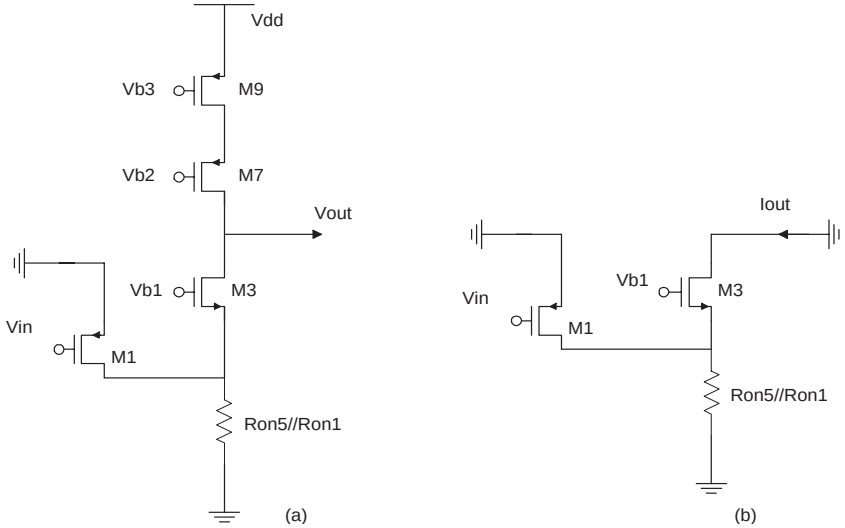

Fig. 3.19 Half circuit of folded cascode op amp.

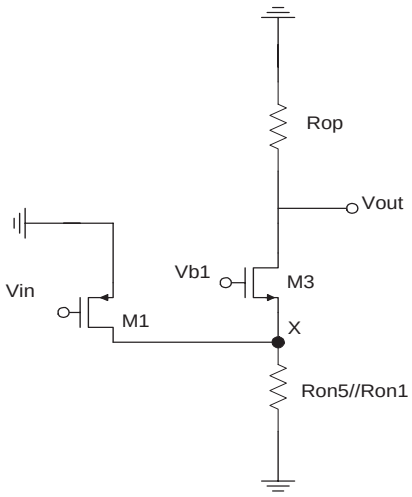

Fig. 3.20 Equivalent circuit for Rout calculation.

3.4 Telescopic structure

In order to achieve high gain, the differential telescopic topologies can be used (fig. 3.21).

This topology (fig. 3.21) is useful to reach higher gain. The output equivalent resistance seen at the output is multiplied by the gain of additional transistor.

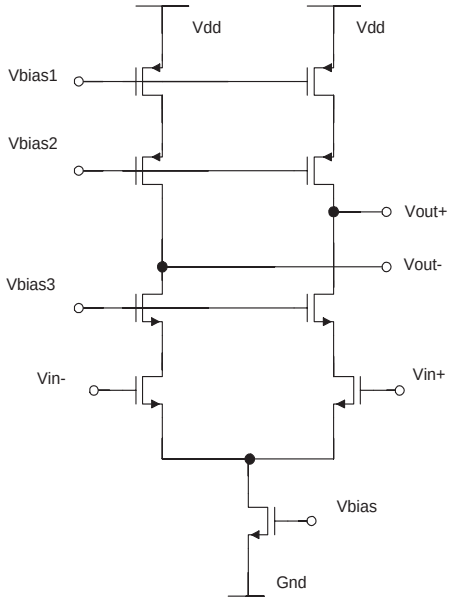

Fig. 3.21 Telescopic cascode topology.

The drawbacks of these structure is the outpout equivalent resistance seen by the load capacitance. The need of a second stage comes from the equivalent RC at the output that engender a pole at quite low frequency. For exemple an output resistance of 1MOhms multiplied by a 17pF load capacitance generates a pole at about 10KHz. For a first order response, the product gain by bandwidth is constant, so 10KHz multiplied by 90dB means that the maximum unity gain frequency would be 1MHz.
Actually, this means that a second stage is needed to make this pole appear at higher frequencies.

The telescopic cascode structure is remarquable for its large DC gain. The fig. 3.22 shows one branch with is used for calculation. Such circuits display a gain on the order of :

$$G = gm \times (gm \times Ron^2)^2$$

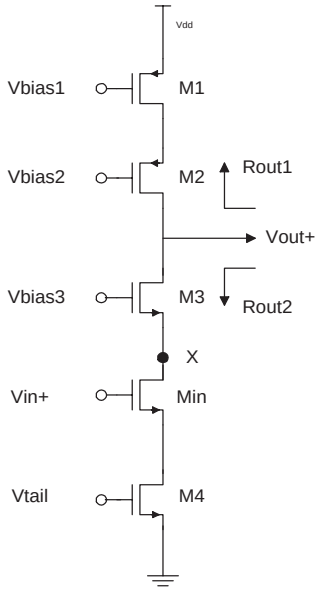

Fig. 3.22 One branch telescopic structure for hand calculation.

This gain magnitude order is explained by the following expressions

$$Av0 = gm1(Rout1 \backslash\backslash \text{Rout2})$$

where Rout1 and Rout2 are given by the following equations :

$$Rout1 = Ron1 + Ron2(1 + gm2 \times Ron3)$$
$$Rout2 = Ronin + Ron3(1 + gm3 \times Ronin)$$

Assuming that gmRon >> 1, one can simplify these expressions as following :

$$Rout1 = gm2 \times Ron2 \times Ron1$$
$$Rout2 = gm3 \times Ron3 \times Ronin$$
$$Av0 = gmin \times ((gm2 \times Ron2 \times Ron1) \backslash\backslash (\text{gm3} \times Ron3 \times Ronin))$$

3.4.1 Noise consideration

As the trend is to decrease the supply voltage to limit the power consumption, one has to be concerned with noise.

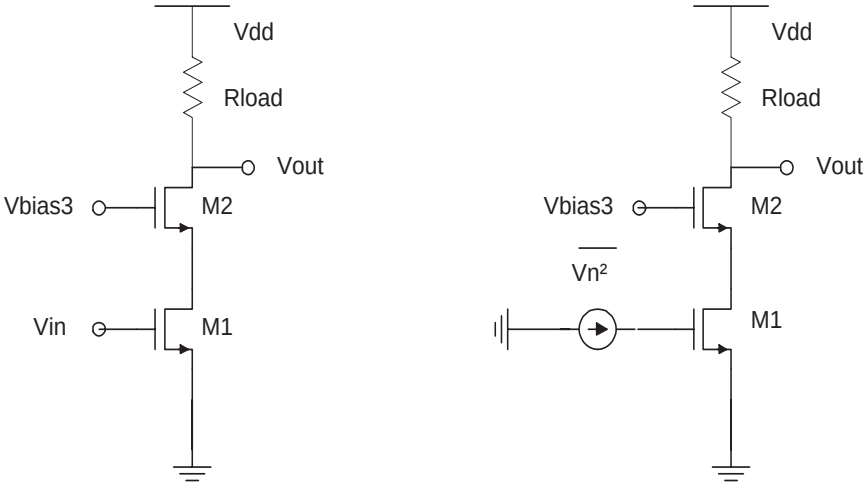

Fig. 3.23 Cascode stage and voltage source noise modeling.

Since low frequencies the noise currents of M1 (fig. 3.23) and Rload flow through Rload, the noise contributed by these two devices is quantified as in a common-source stage where the 1/f noise of M1 has been neglected.

$$\overline{Vn^2} = 4kT\left(\frac{2}{3gm1} + \frac{1}{gm1^2 \times Rload}\right)$$

At relatively low frequency, the cascode devices contribute negligible noise, leaving M1-M2 and M7-M8 as primary noise sources. When using the expression of Rload, the total input refered noise in given by :

$$\overline{Vn^2} = 4kT\left(2 \times \frac{2}{3gm1} + 2 \times \frac{2gm7}{3gm1^2}\right) + 2\frac{2Kn}{(W1 \times L1)Cox \times f} \times 2\frac{Kp}{(W7 \times L7)Cox \times f} \times \frac{gm7^2}{gm1^2}$$

3.4.2 Gain boosting

The need of a high gain due to the high final resolution leads to find solution to increase the DC gain of the operational amplifier, and specially for the first stage. The idea of a gain boosting can give additional gain. The general idea behind gain boosting is to increase the output impedance. As seen before, in a simple CMOS topology, to stack more transistor is limited, as it reduce the signal swing and after 2 transistors stacked, the maximum output impedance is reached.

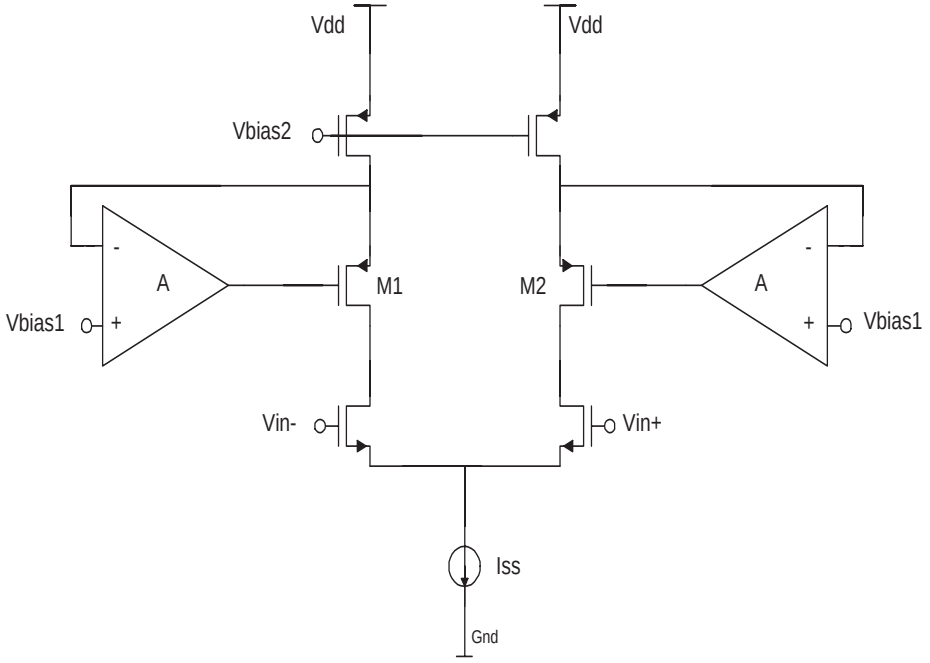

Fig. 3.24 Gain boosting principle schematic

The solution is to use an additional single ended operational amplifier as shown in fig. 3.24. The idea is to regulate the gate voltage of M1 and M2 around Vbias1.
The small signal equivalent schema is represented on fig. 3.25.

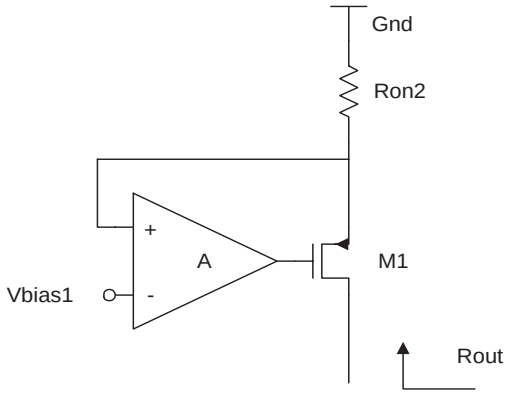

Fig. 3.25 Equivalent output impedance.

The small signal equivalent circuit is the following (fig. 3.26):

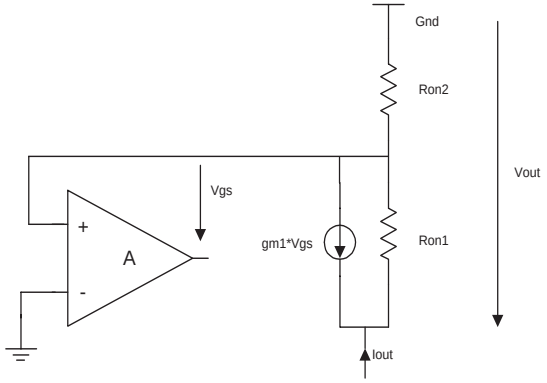

Fig. 3.26 Small signal equivalent circuit.

$$Vout = R02 \times iout + R01 \times (iout - gm1 \times V)$$

$$V = -A \times R02 \times iout \qquad Vout = R02 \times iout + R01 \times (iout + gm1 \times A \times R02 \times iou$$

$$Rout = R01 + R02 + A \times R02 \times R01 \times gm2 \qquad (R01 + R02) \ll A \times R01 \times R02 \times gm2$$

$$Rout \approx A \times R01 \times R02 \times gm2$$

This means that the output impedance is multiplied by the gain of the additional amplifier. The gain enhancement is illustrated on fig. 3.27.

The output resistance seen on the drain of M2 is the following

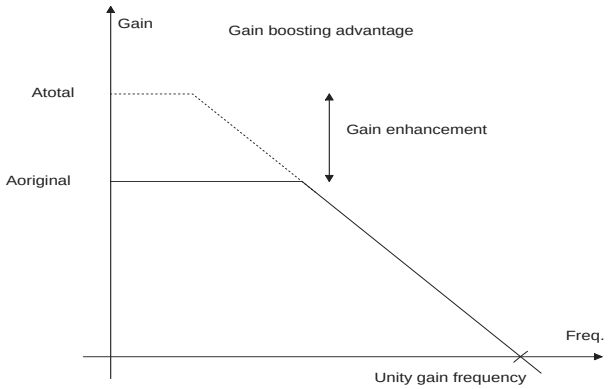

Fig. 3.27 Gain enhancement with gain boosting.

3.5 Two stage topology

In contrast to single stage operational amplifier, two stage configuration isolates the gain and the swing requirements (fig. 3.28).

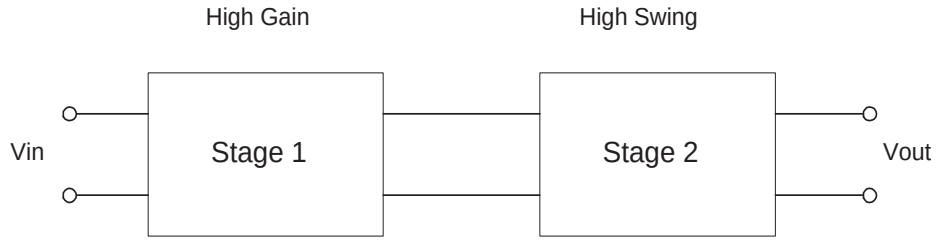

Fig. 3.28 Two stage operational amplifier.

3.5.1 Miller compensation

Full differenctial topology has the property to avoid mirrored poles, thereby exhibiting stable behavior for a greater bandwidth. In fact, we can identify one dominant pole at each output node and only one nondominant pole arising from node X on fig. 3.29.

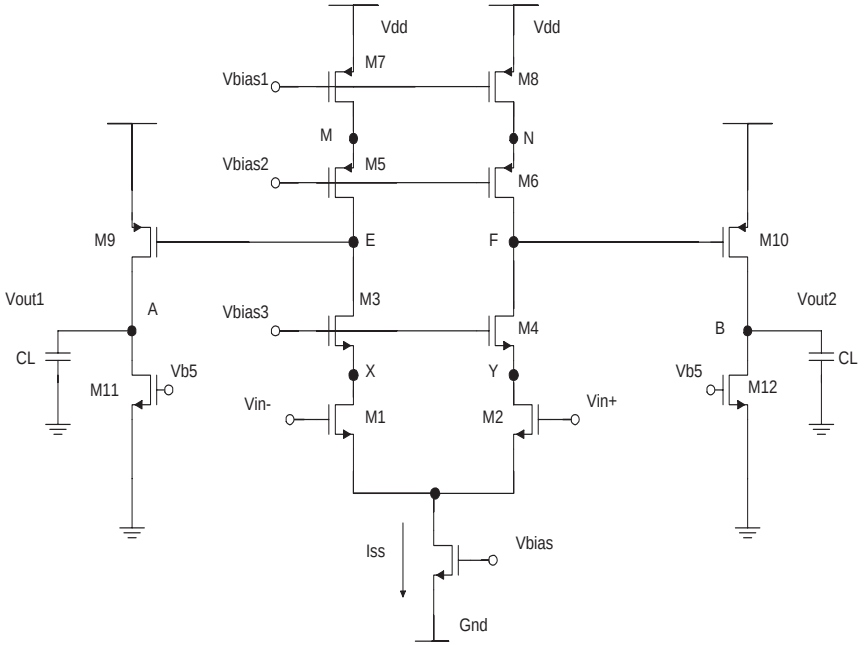

Fig. 3.29 Two stage topology.

Concerning the pole in node N, one can assume that the capacitance seen at this node is :
Cn = Cgs5 + Csb5 + Cgd7 + Cdb7, and that this capacitance shunts the output resistance of M7 at high frequency, thereby dropping the output impedance of the cascode.

To quantify this effect, we first determine Zout (fig. 3.30) :

$$Zout = (1 + gm5 \times Ron5)Zn + Ron5$$

The impedance Zn seen at node N is :

$$Zn = Ron7 \backslash\backslash (Cn \times s)^{-1}$$

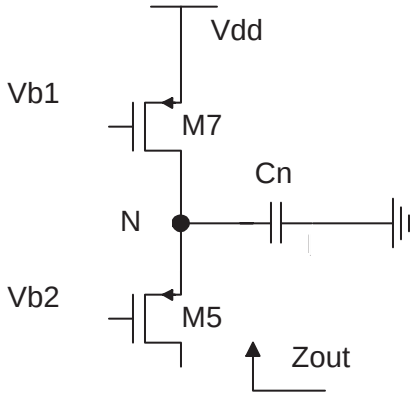

Fig. 3.30 Effect of device capacitance at internal node of a cascode current source.

Neglecting Ron5, the Zout expression is :

$$Zout \approx (1 + gm5 \times Ron5) \times \frac{Ron7}{Ron7Cn \times s + 1}$$

As illustrated in the following fig. 3.31, we take the output capacitance of the first stage into account.

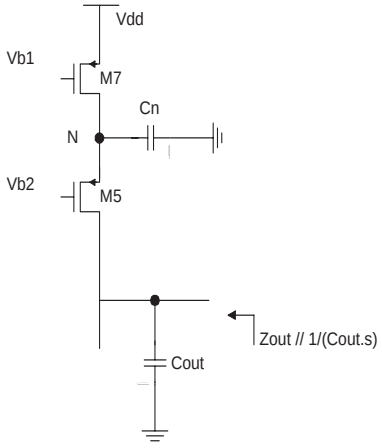

Fig. 3.31 First stage output impedance

The impedance seen at the output of the first stage is:

$$(Zout\backslash\backslash(\mathrm{Cl.s})^{-1}) = \frac{(1+gm5Ron5)\times\frac{Ron7}{Ron7Cn\times s+1}\times\frac{1}{(Cl\cdot s)}}{(1+gm5Ron5)\times\frac{Ron7}{Ron7Cn\times s+1}+\frac{1}{Cl\cdot s}}$$

$$(Zout\backslash\backslash(\mathrm{Cl.s})^{-1}) = \frac{(1+gm5Ron5)\times Ron7}{((1+gm5Ron5)\times Ron7\times Cl+Ron7Cn)s+1}$$

Thus the parallel combination of Zout and the load capacitance still contains a single pole corresponding to a time constant (1+gm5Ron5)Ron7Cl+Ron7Cn. This pole can be separated in two parts, the (1+gm5Ron5)Ron7Cl and the Ron7Cn one. The first is due to the low-frequency output resistance of the cascode. This mean that the overall time constant equals the “output” time constant plus Ron7Cn. The key point is that the pole generated by the cascode structure is merged with the output pole, thus creating no additional pole. This is a remarkable advantage of fully differential cascode operational amplifier.

3.5.2 Zero pole compensation

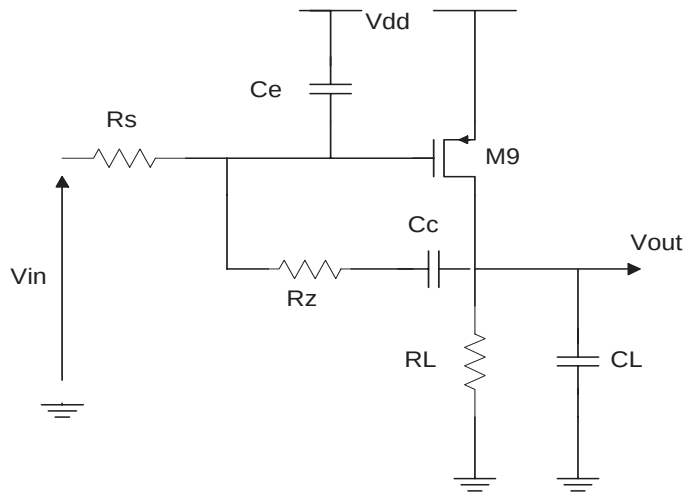

Fig. 3.32 Addition of Rz to move the zero.

in order to compensate the two stage operational amplifier, one can use the effect of zero in the tranfert function. In cascode topology, zero are quite far from the origin. The effect of Miller compensation makes zero appears at lower frequency. Normally, the zero with Miller compensation appears at gm/(Cc+Cgd9)

The equivalent circuit on fig. 3.32 shows the output resistance and capacitance of the input stage and the output stage.

Using a resistance in series with the compensation capacitance modify the the zero frequency. The zero frequency now appears at

$$Wz = \frac{1}{Cc(gm9 - Rz)}$$

3.5.3 Noise consideration

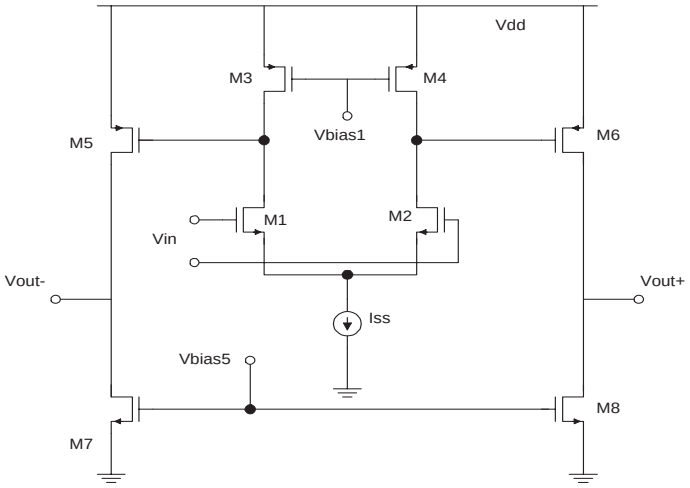

Fig. 3.33 Noise consideration in a two stage topology.

In order to simplify calculations, a simple input stage has been choosen. Considering the output stage, one can note that the noise current of M5 and M7 (fig. 3.33) flows through ron5 || ron7. Divinding the result voltage by the total gain, gm1(ron1||ron3)*gm5(ron5||ron7), and doubling the power, the input-referred contribution of M5-M8 is

$$\overline{Vn^2} = 2 \times kT \times \frac{2}{3}(gm5 + gm7)(ron5||ron7)^2 \times \frac{1}{gm1^2(Ron1||Ron3)^2 gm5^2(Ron5||Ron7)}$$

$$\overline{Vn^2} = \frac{16kT}{3} \times \frac{gm5 + gm7}{gm1^2 \times gm5^2(Ron1||Ron3)^2}$$

The noise due to M1-M4 is :

$$\overline{Vn^2} = 2 \times 4kT \times \frac{2}{3} \times \frac{gm1 + gm3}{gm1^2}$$

The output noise is now the result of the sum of the two previous terms :

$$\overline{Vn^2} = \frac{16kT}{3} \times \frac{1}{gm1^2} \times \left[gm1 + gm3 + \frac{gm5 + gm7}{gm5^2 (Ron1 || Ron3)^2} \right]$$

This means that the noise resulting from the output stage is negligible bacause it is devided by the gain of the first stage when referred to the main input.

3.6 Conclusion and choice

Once the different topologies studied and simulated, one can make the choice of the topolgogy that will best fullfill the specification.

3.6.1 Overall topology choice: 2 stage op amp

As explained before, one needs a 17pF load capacitance. In fact, the settling time performance requires a high bandwidth that cannot be reached by a single stage operational amplifier. For example, to reach the gain of 85dB, on can think at first order, that an equivalent load resistance of 5 MΩ multiplied by a gm of 4ms can be the solution (fig. 3.34), as the gain formula is the following

$$G_{dB} = 20 * \log(gm * Rc) = 86dB$$

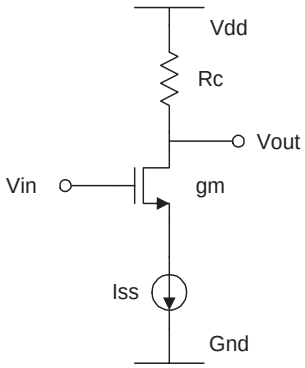

Fig. 3.34 Equivalent circuit. First order approach.

Assuming the topology to a single dominant pole, which is coming from the output, the bandwidth would be around :

$$Bw = \frac{1}{2\pi * Rc * C_{load}} = 1{,}872 KHz$$

This mean that the unity gain frequency Fu is :

$$Fu = Bw * G_{dB} = 161 KHz$$

The settling time goal is 16ns, so the unity gain frequency should be at least 300MHz. Consequently, this topology is not the proper one, and this although mean that the high gain and short settling time can be reconciled only if the output pole is rejected to higher frequency; In fact one can use a 2 stage topology; the first stage for amplification, and the second stage to reject the output pole and to enlarge the output swing.

Furthermore, one can choose the topology that can reach the highest gain for the first stage, the telescopic cascode structure, and then a simple source follower (inverter) to maximise the output swing.

3.6.2 Compensation method

The compensation method choosen is the miller compensation and zero compensation. The other

possibility would have been the cascode compensation; the problem is that cascode compensation is current consumming.

3.6.3 Common Mode Feedback choice

Switched capacitor topology has shown great advantages; it can samples the Common mode level in a large swing, and this could be simple to implement when the whole ADC is in a Switched capacitor topology.
Nevertheless, the introduction of digital signals in the topology would have engender a great layout care, such as additional substrat noise and charge injection at the output. The other trouble is the time simulation which is longer than for a continuous time CMFB.

4.Implementation

4.1. Schematic and simulations

4.1.1. Input stage

4.1.1.1 NMOS input transistor

As explained before, the input stage provides the gain of the operational amplifier.
First, one has to know why NMOS transistor had been choosen. For a comparable device dimensions and bias currents, the PMOS input differential pair exhibits a lower transconductance than does a NMOS pair. This is due to the greater mobility of NMOS device. The first stage should provide the largest gain, so NMOS transistor had been choosen.

4.1.1.2 Implementation

4.1.1.2.1 Voltage biasing

One has to care for the biaising of the stacked transistor (fig. 4.1).

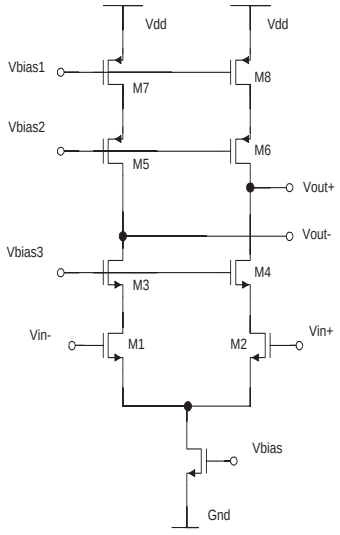

Fig. 4.1 telescopic topology.

The following table (fig. 4.2) sums up the bias voltage chosen :

Bias voltage	Theoritical value	implementation
Vbias1	Vdd-Vthp	1.9V
Vbias2	Vdd-Vthp-Vds,sat	1.8V
Vbias3	Vthn+ 2*Vds,sat	2V
Vbias	Vthn	1.4V

Fig. 4.2 Table of theoritical and implementation values.

The result of the first stage implementation is shown below (fig. 4.3).

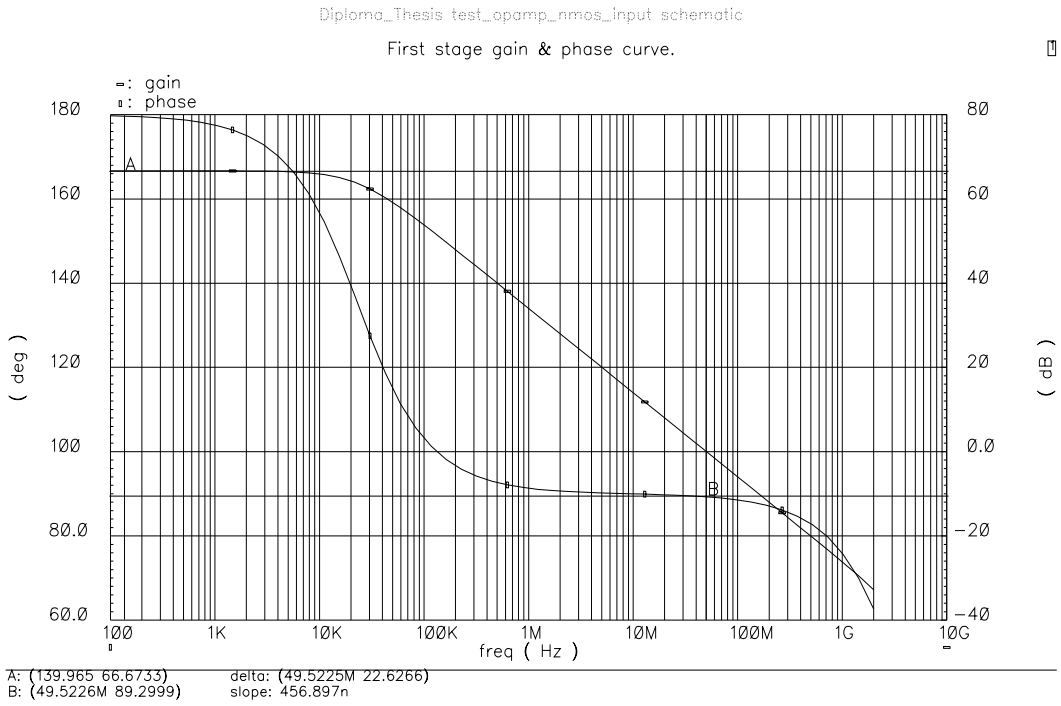

Fig. 4.3 Gain and phase curve of the input stage.

4.1.2. Gain boosting

The gain boosting can increase the gain at low frequencies. This means that the bandwidth has to be greater than the first stage bandwidth.

The main issue is to design the gain booster is to be in the amplification zone of the amplifier when the DC level of the cascode stage is applied at the input of the amplifer. This is illustrated in fig. 4.4.

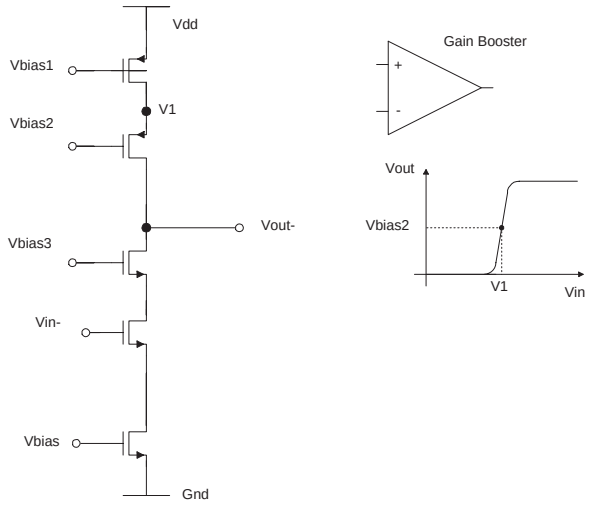

Fig.4.4 Gain booster implementation.

The gain obtained in this amplification zone (fig. 4.5) is around 30dB. This provide a great enhancement for the first stage amplification.

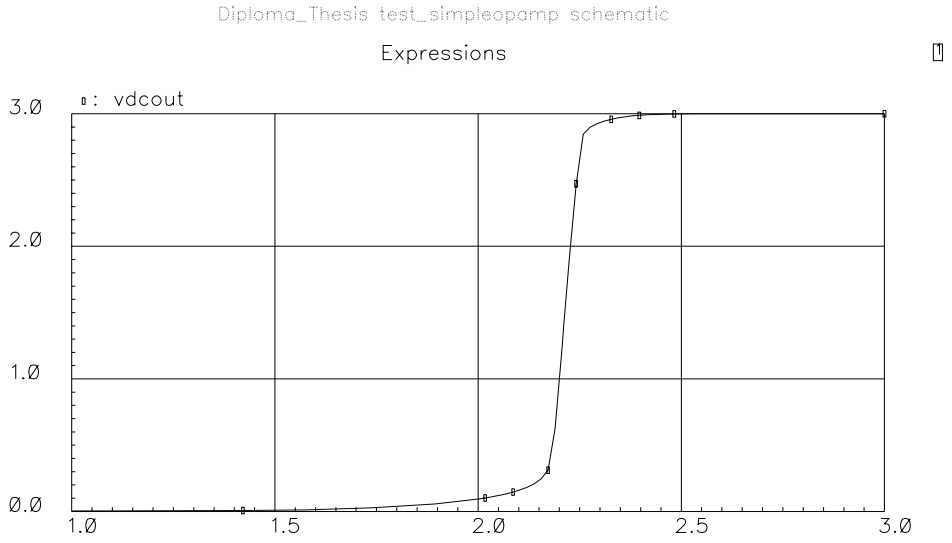

Fig. 4.5 Gain booster gain curve.

4.1.3. Output stage

As said previously, the output stage in used to reject the output pole to high frequency in order to reach a high unity gain frequency. Pmos input transistor have been choosen, as the input transistor were nmos. The equivalent schematic of this stage is shown in the following fig. 4.6. The more one will increase the output current, the faster the output capacitance will be load;

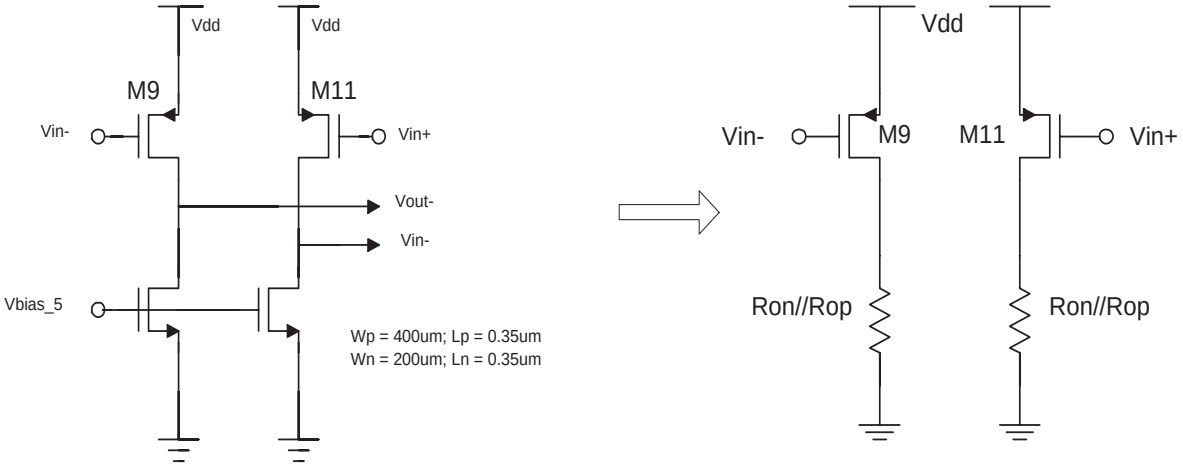

Fig. 4.6 Output equivalent schematic.

The on-resistance of the 2 transistors are verifying the equations :

$$Ron = \frac{1}{\lambda \times Id} \qquad Id = \frac{Kp}{2}\frac{W}{L} \times (Vgs - Vth)^2$$

$$Pole = \frac{1}{2 \times \Pi \times RonIIRop \times Cload}$$

The main goal was so to decrease Ron//Ronp. The solution found was to increase the current Id. This have been done by an increase of the gate-source voltage of both nmos and pmos transistor.

The gain and phase of the output stage is given on the following fig. 4.7. The following values can be measured :

$$Gdb = 10.06dB$$
$$PhaseMargin = 71.5°$$

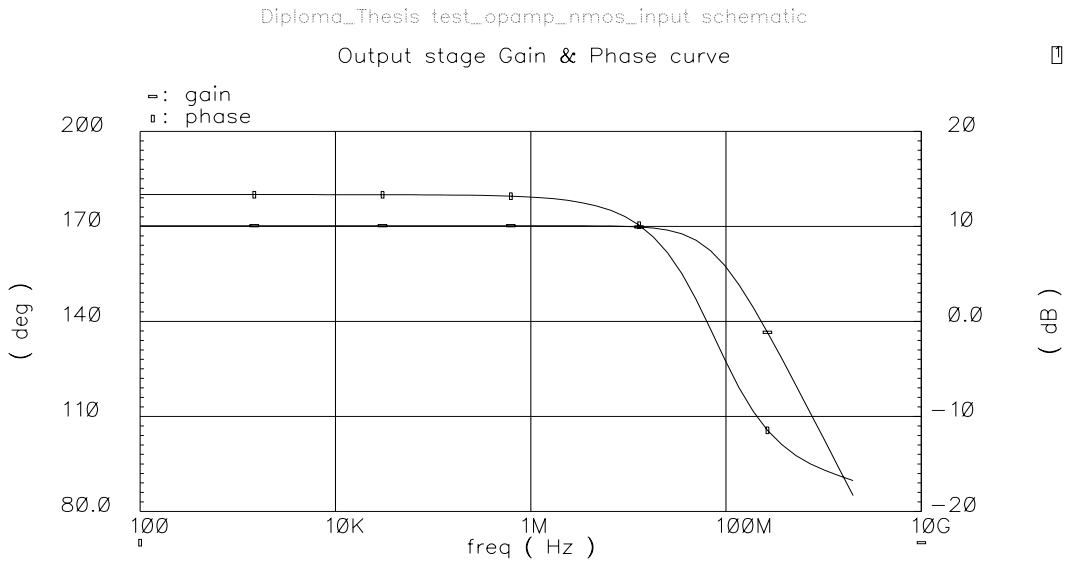

Fig. 4.7 Output stage gain and phase curve.

4.1.4. Common mode feedback (CMFB) circuit

The continuous time structure has been chosen. In fact, several reasons lead to this choice. First, the use of switch engender non linearity at the output more than with a continuous time structure. Then the use of digital signals in the first stage can generate additional noise and parasistic in general. The non use of digital signal in this stage avoid several coupling problems and layout

care that would have to be taken in account.

4.1.4.1 CMFB compensation network

The compensation method used is the miller compensation. It presents a good compromise concerning the phase margin, compared to the area used. The testing circuit is shown as following in fig. 4.8.

The loop has been opened at the output of the CMFB comparator. The output sees an infinite impedance on the grid of the bias transistor of the first stage.

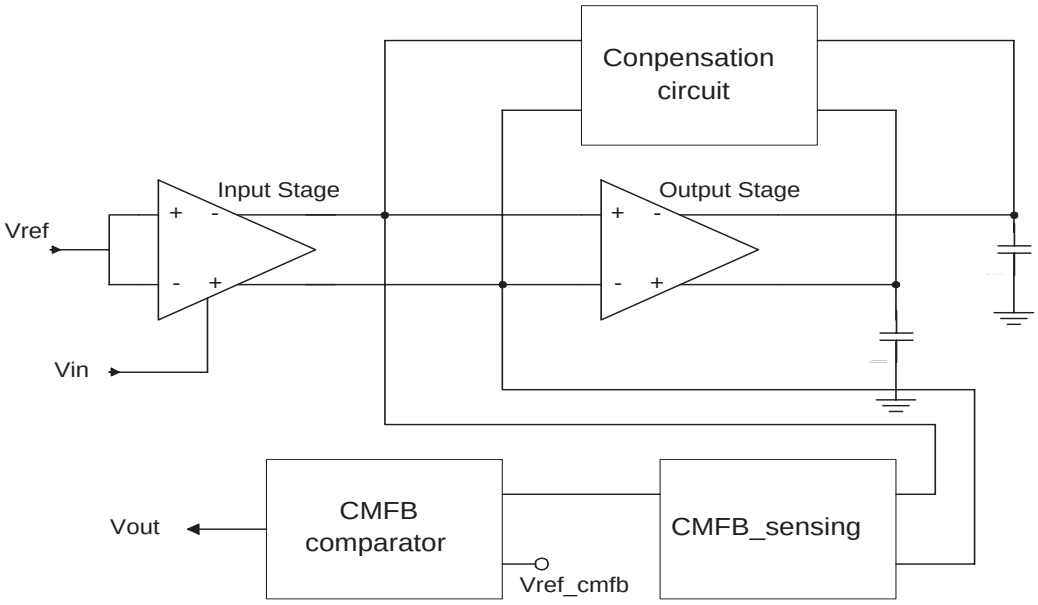

Fig. 4.8 CMFB Testing circuit

The gain and phase of the CMFB circuit is shown below (fig. 4.9):

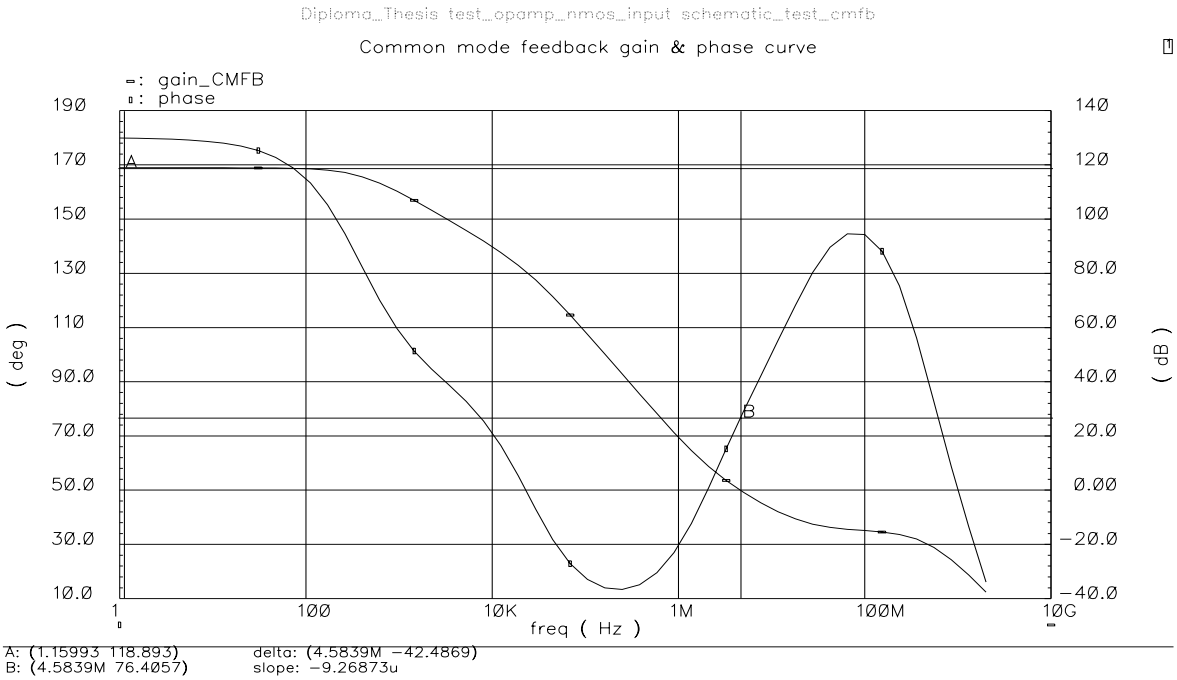

Fig. 4.9 Gain and phase curve of CMFB circuit.

4.1.5. Compensation

The compensation network is composed of Miller compensation and zero compensation.

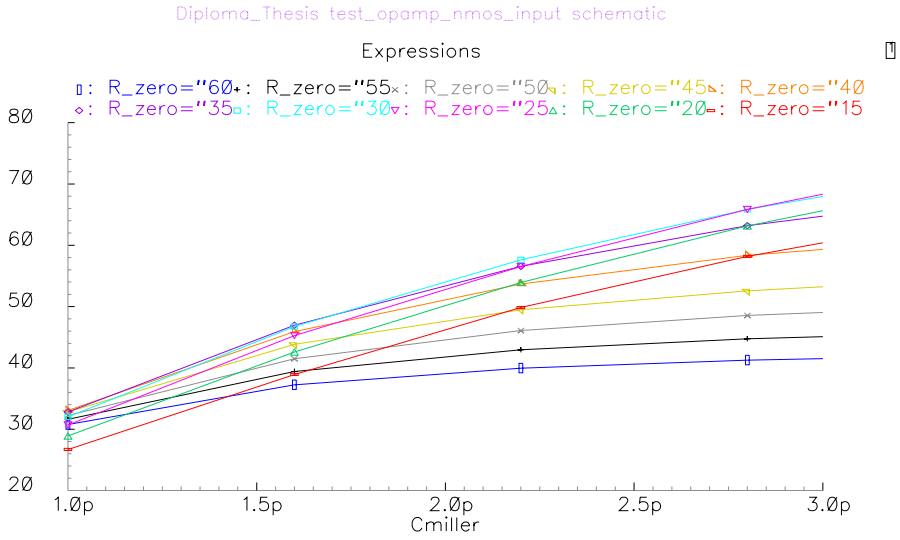

Fig. 4.10 Phase Margin towards capacitance and resistance compensation.

The trade off with the compensation network was between an acceptable stability, which means a

phase margin the closest to 60 Deg (fig 4.10)., and a high settling time (fig. 4.11). The following curve shows the settling time value towards the same parameters as before.

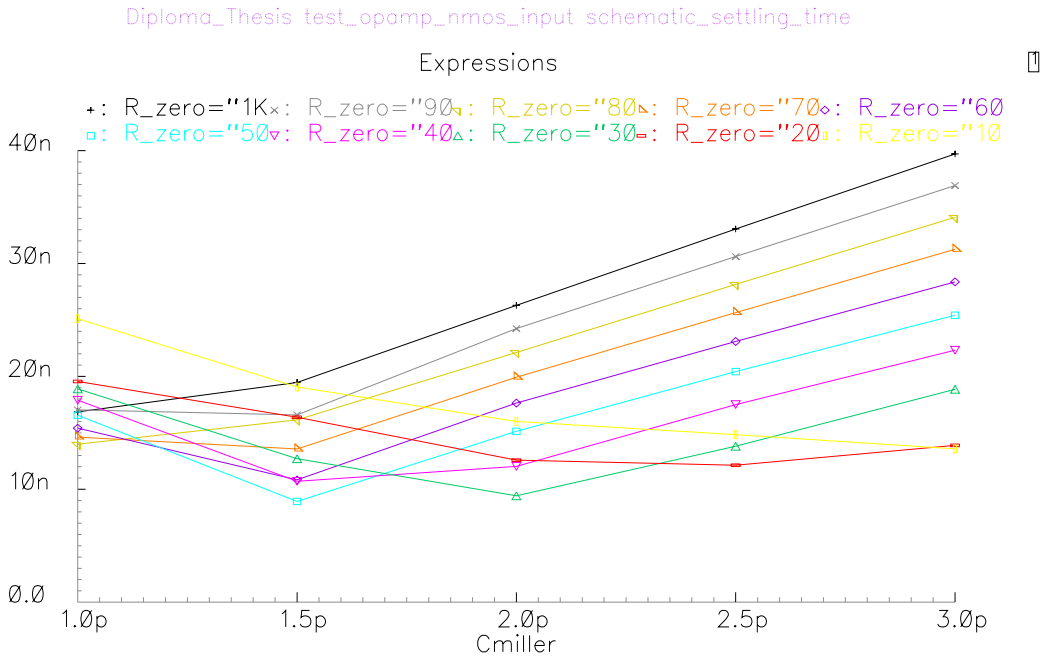

Fig. 4.11 Settling time towards capacitance and resistance compensation.

Finally, the choice of a resistance of 350 Ohm and a 2p capacitance has been made.

4.1.6. Overall topology and simulations

The topology of the overall structure is presented on the next page (fig. 4.12).

To reach the overall accuracy of the ADC, one has to focus on the DC gain. The gain error should be under 1 LSB. The gain has to verify the following equations ::

$$1LSB = \frac{1}{2^{14}}$$

$$Error = \frac{1}{DCgain} \qquad Error < 1LSB \qquad DCgain > 20\log(2^{14}) = 84.3dB$$

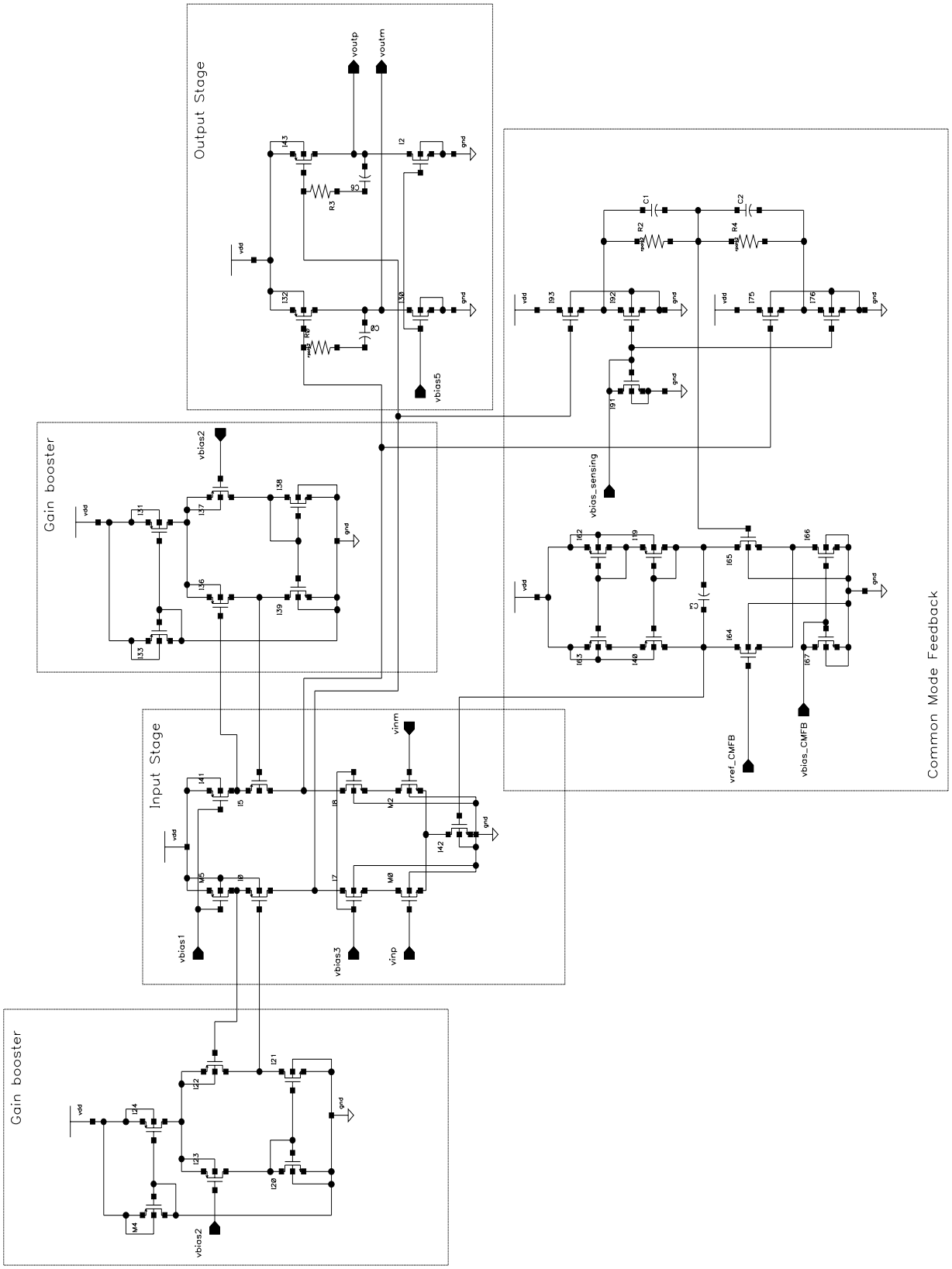

Fig. 4.12 Overall topology of the operational amplifier

The gain and phase curve obtained is given on fig. 4.13

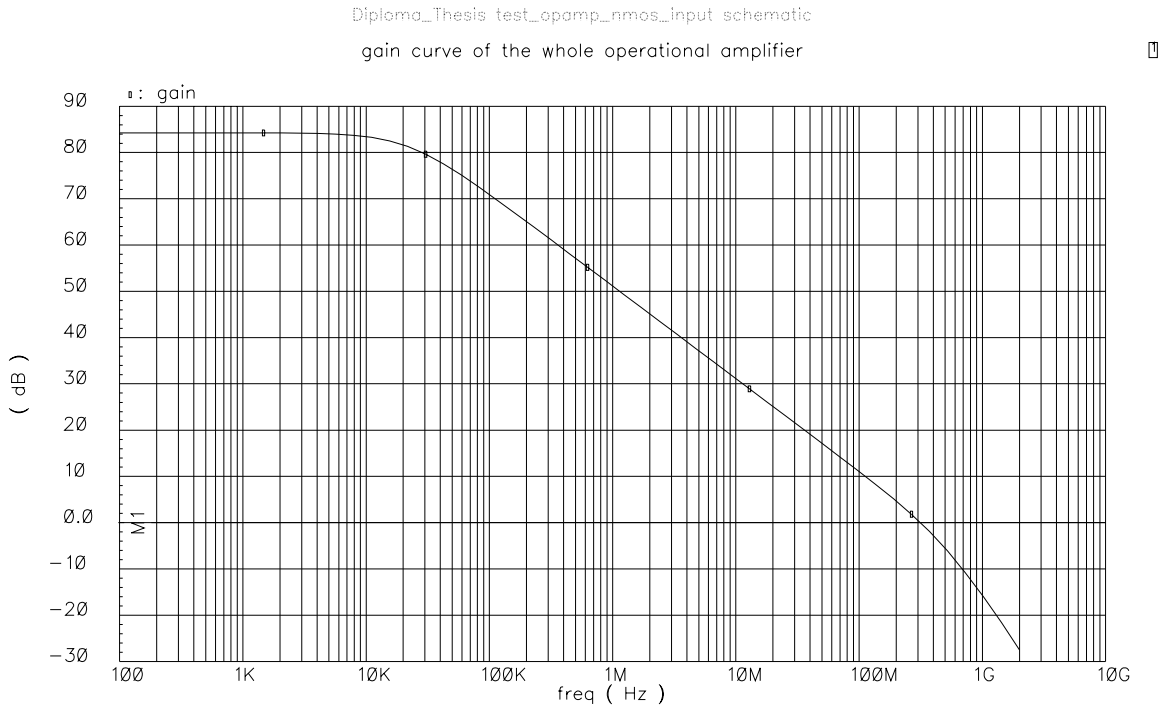

Fig. 4.13 Gain and Phase curve of the overall op-amp.

The important values mesured on this curve are the following ;

$$Gdb = 84.26dB$$
$$PhaseMargin = 54.4°$$

4.1.7 Spectral analyze

4.1.7.1 Spurious Free Dynamic Range

Simulation result is given on the following curve (fig. 4.14).

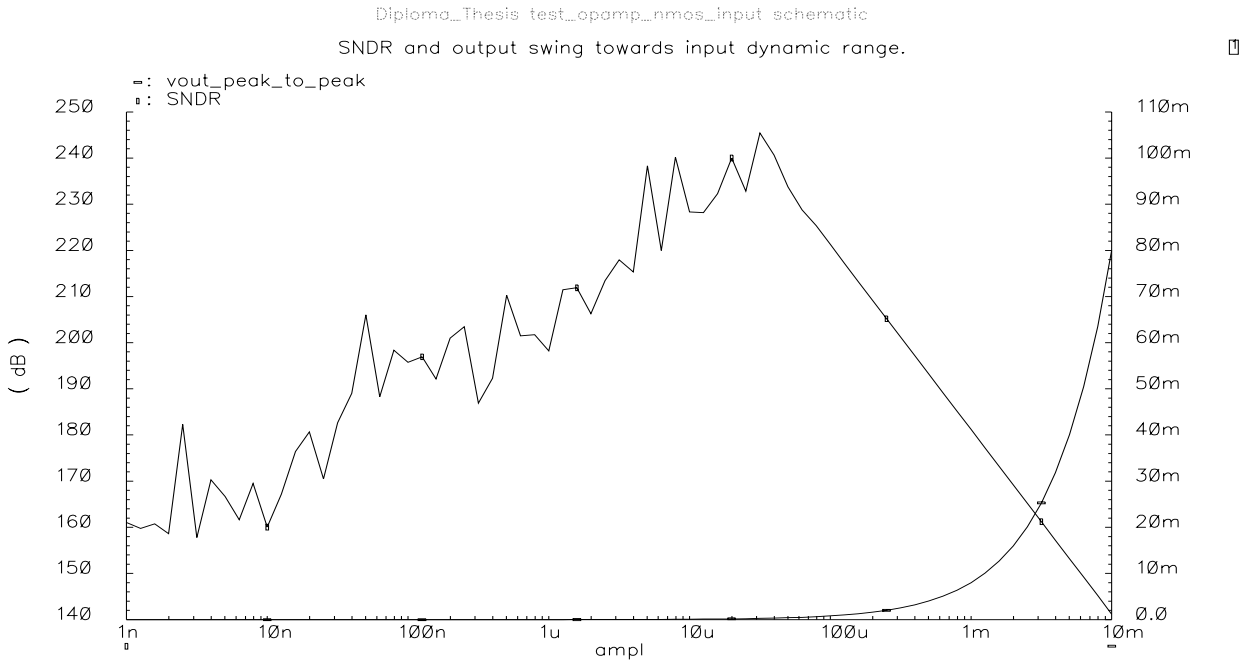

Fig. 4.14 Spurious free dynamic range.

4.1.7.2 Third harmonic rejection and output dynamic range

As explained is the first part, non linearity is a concerning issue for ADC. As even order harmonic are suppressed by the full differential topology, one can measure the third harmonic rejection when the input swing is increased and also mesaure the output swing (fig. 4.15).

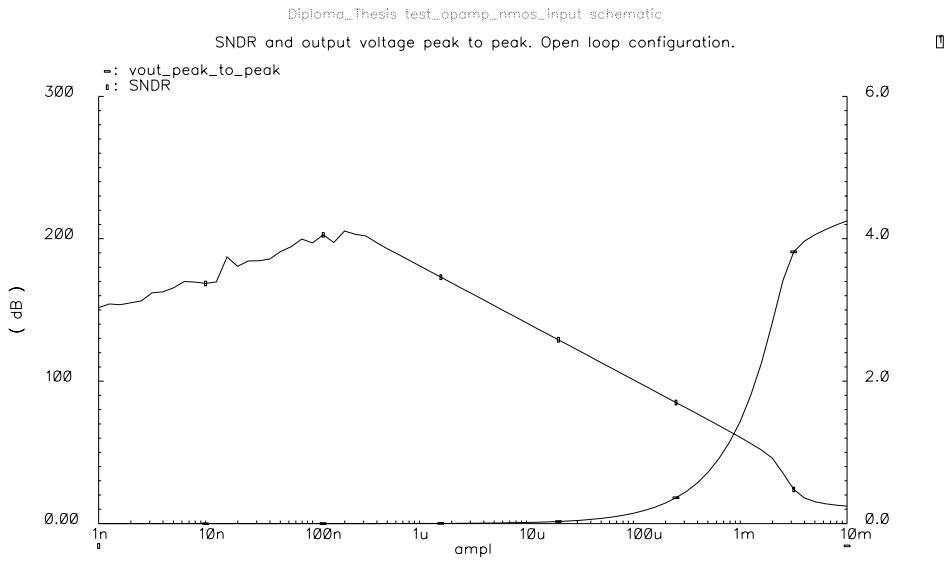

Fig. 4.15 Third harmonic rejection and output swing.

4.1.8 Slew rate

The slew rate in depending on the compensation capacitance and on the current to load this compensation capacitance.

The measure of the slew rate has been made in large signal. The curve of slew rate calculation is given on the following fig. 4.16.

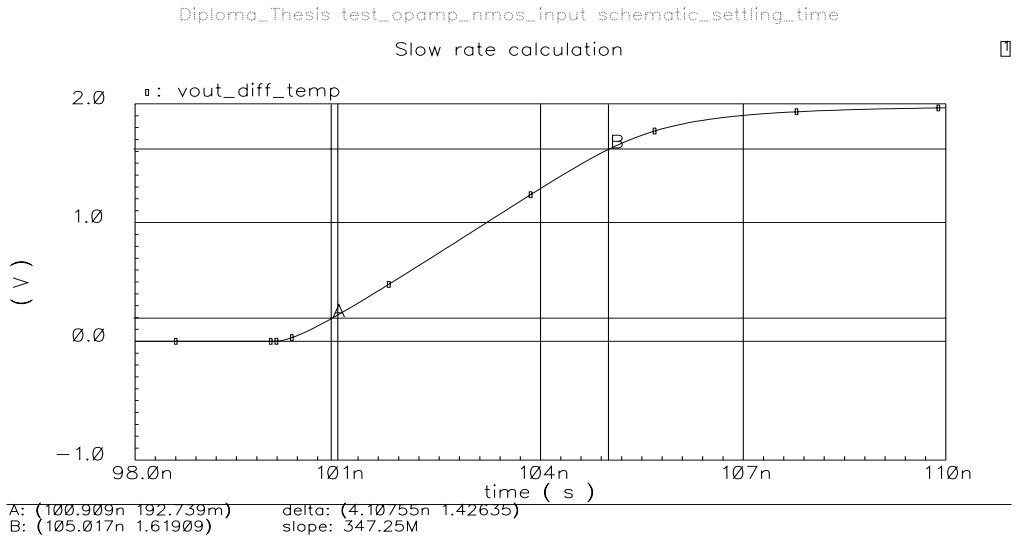

Fig. 4.16 Slew rate curve for calculation.

One can easily measure the slope of this curve :

Slew rate = 347 V/us

4.1.9 Power Supply Rejection Ratio (PSRR).

The Power supply rejection ratio measure the dependance of the output voltage toward the supply voltage variation. This have sense when the full design is made, with the voltage generator. In the opposite case, supply voltage will vary but bias voltage will stay constant has defined wit ideal voltage sources.

4.1.10 Noise analyse results

As previously said, full differential topology has the advantage to disable “environemental” noise. For example, line coupling is largely rejected in a differential mode, as the digital line for example as the same effet on the same analog lines, one can assume that the difference of these two signals will reveal no couling effect. This can although be understood for power noise rejection The rms noise is given on the following fig. 4.17.

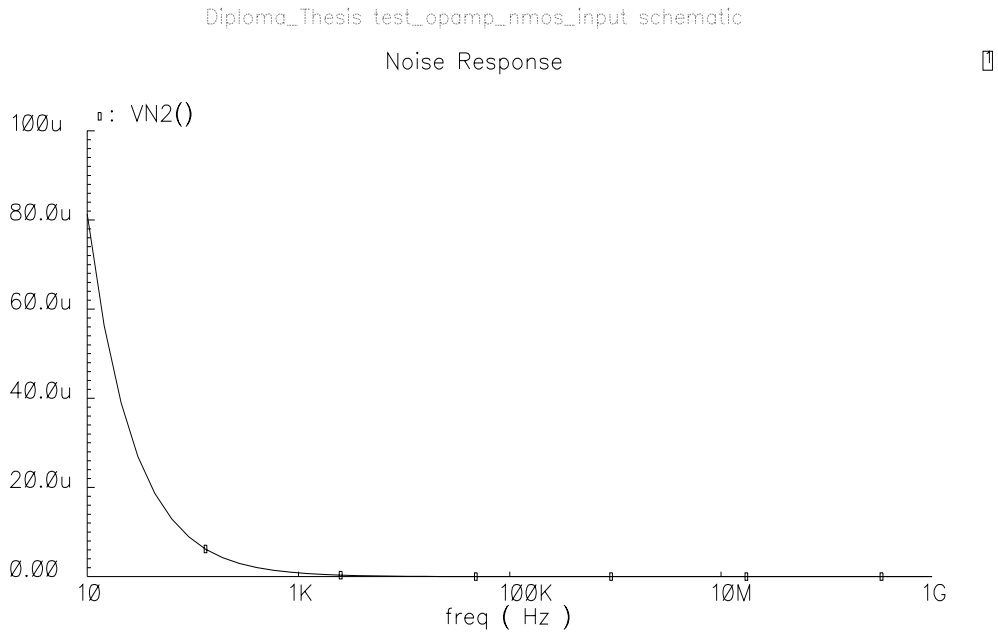

Fig. 4.17 Output noise.

The input referred voltage noise can be simulated in a gain of 1 configuration. The curve is given below (fig. 4.18).

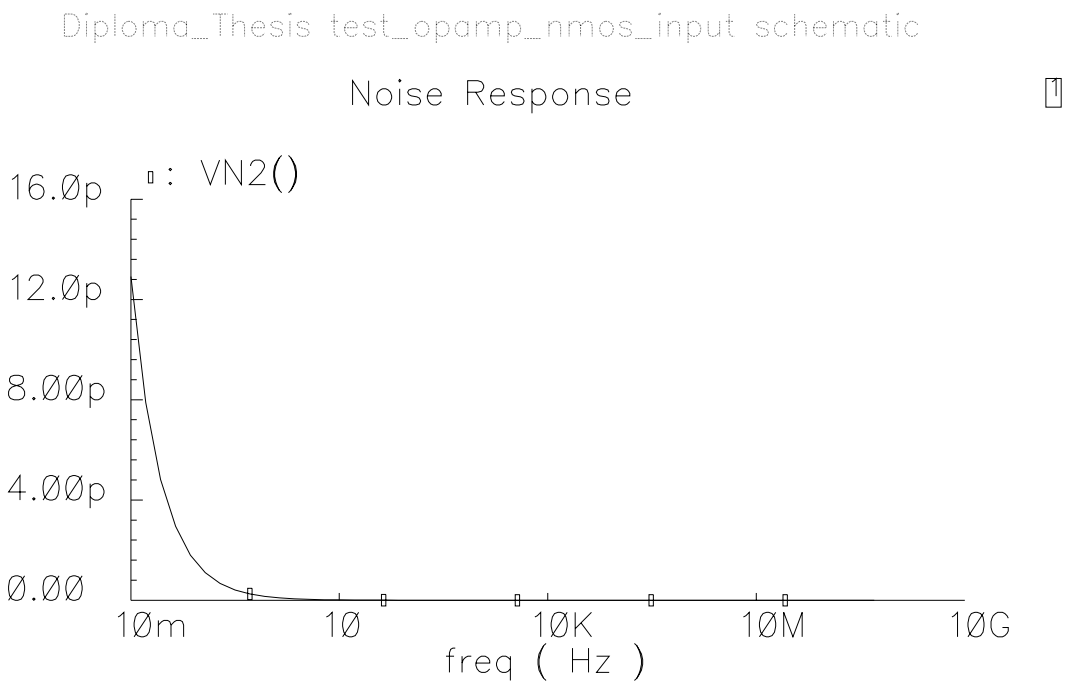

Fig.4.18 Input rms refered noise.

When the curve is integrated between the 0 Frequency and the unity gain frequency, the input refered rms noise is 28uV

One can sum up the result of the operational amplifier performance in the following fig. 4.19 :

Parameters	Value
DC_gain (open loop configuration)	84.3dB
Phase_Margin	54.4 Deg
Settling Time (closed loop configuration)	8.9ns
Power Consumption	141mW
Output swing (differential ended)	1V
3rd harmonic rejection	60 dB

Parameters	Value
Slew rate	347V/us
Vdd	3V
Vss	0V
unity gain frequency	314Mhz
BandWidth	18.1Khz
Input common mode swing	0.9-1.7V
Input refered noise	28uV
Area	$< 0.05mm^2$

Fig. 4.19 Performance result of the operational amplifier.

4.2. Layout

The layout of an integrated circuit defines the geometries that appear on the masks used in fabrication.

Full custom layout requires special care, especially for a fully differential topology.

The terminology full custom concerns the design where each transistor can be designed by hand, using directly the different layers of the kit.

Mismatches between the two branch of the operational amplifier is a real problem; the basic rule for layout design is to avoid rotate, mirror or flip the device which have to match. Then, one has to place these 2 device the nearest the better, so that process parameter will have less effect on the performance of the operational amplifier. Appendix B shows the recommendations form AMS to make device match.

4.2.1. Layout considerations

4.2.1.1. Common centroide structure

4.2.1.1.1 One dimension approach

When large transistor are used (for example the input transistor pair), gradients along the 2 dimensions axes can engender appreciable mismatches. To reduce this mismatches, the structure in fig. 4.19 can be used. For clarity, only gate connections are shown. To analyse the effect of a gradient on this structure, we can assume that the gate capacitance varies from dCox.

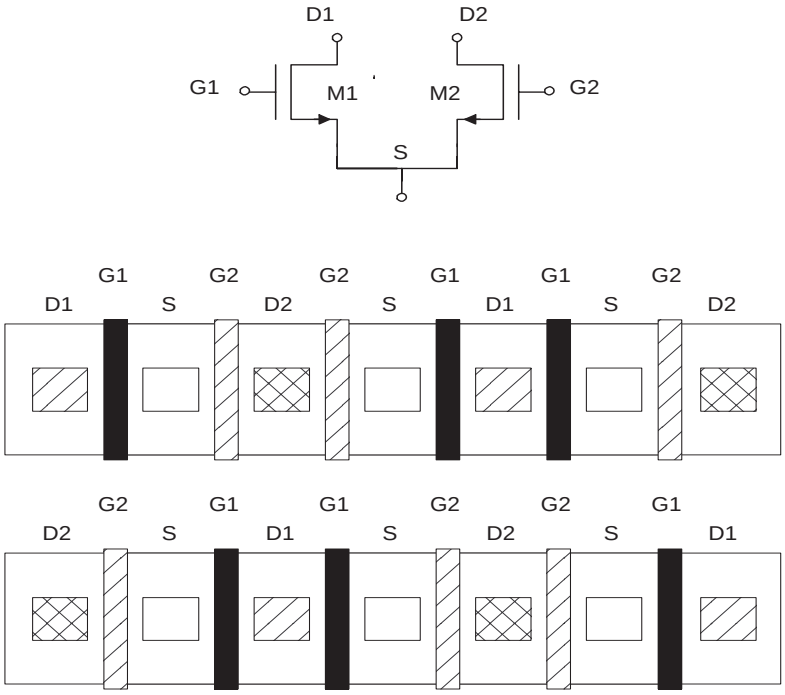

Fig. 4.20 Input transistor configuration.

If we compare the Drain current that flows in the 2 branches, the result is :

$$Id1 = \frac{1}{2}\mu n(Cox + Cox + 3\Delta Cox)\frac{W}{L}(Vgs - Vth)^2$$

$$Id2 = \frac{1}{2}\mu n(Cox + \Delta Cox + Cox + 2\Delta Cox)\frac{W}{L}(Vgs - Vth)^2$$

This type of cross coupling cancels the effect of the gradient. The effect of gradient on the other direction is cancelled naturally as the gradient involve the same number of transistor.

4.2.1.1.2 Two dimensional common centroide structure

As the input transistor, with have to match, have to be physically the nearest the better, a two dimensional topology has been used.

Of course, a gradient can happen in any direction; this gradient can then be divided in an X-gradient and a Y-gradient. So one has to use a proper two dimensional structure to avoid the process mismatch (fig. 4.21)

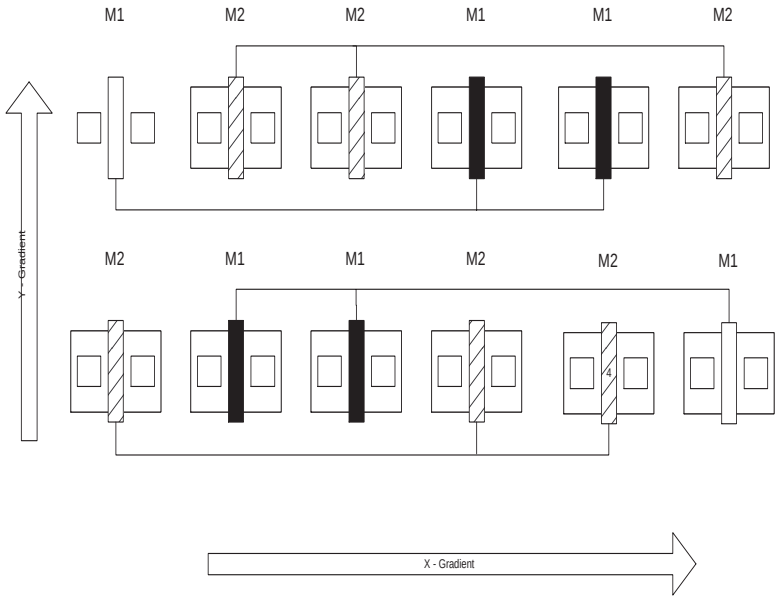

Fig. 4.21 : Common centroide structure.

4.2.1.2. Gate shadowing limitation

4.2.1.2.1 Source of the gate shadowing problem

The following figure shows the source of the trouble. During the drain and source implantation, the polysilicon gate shadows the drain or the source of the transistor because the implant is tilted by about 7 degres. As a result, the source and drain don’t receive the same implantation.The process step is represented in fig. 4.22.

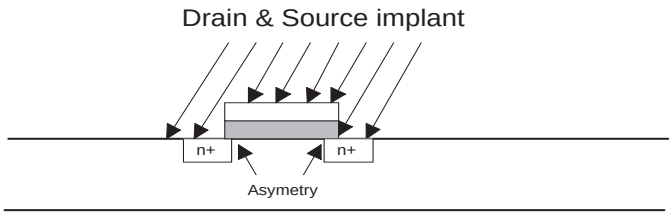

Fig. 4.22 Gate shadowing effect.

The topology used which is the topology (Fig. 4.23 (a)) suppress the effect of the gate shadowing. In fig. 4.23 (b), the transistor are not identical because the drain of M1 sees something dirrefent as the M2 drain. This is not the case in the topology (a).

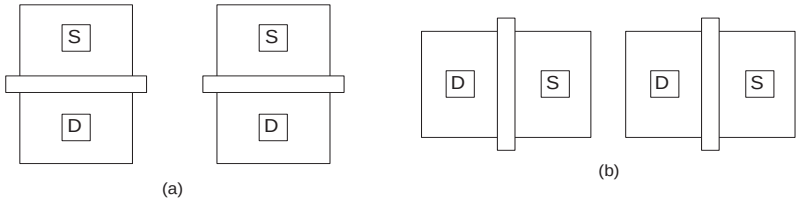

Fig. 4.23 Topology to limit the gate shadowing.

4.2.1.3. Dummy structure

The addition of elements to create the same environment for matching component can also decrease mismatch. The Fig. 4.24 shows the topology choosen to make the compensation capacitance match. This is a two dimensional structure.

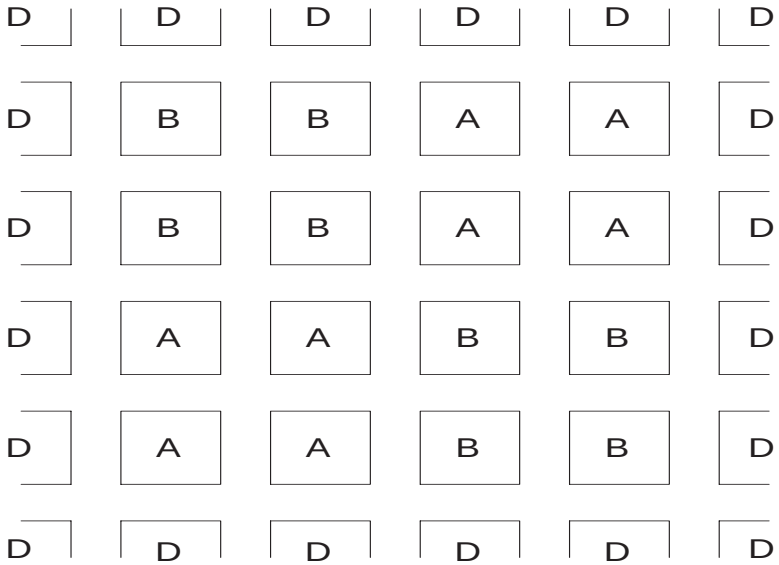

Fig. 4.24 Structure used for matching compensation capacitance

Special care must be taken with these dummy elements, specially during the extraction of the parameters. When one is adding these element, these have to match with the schematic to pass the LVS (Layout Versus Schematic). These elements have to be present in the schematic. The problem is that there is a minimum value for poly-poly capacitance in the schematic but not in the extracted view.

One has to know that the LVS of the AMS design kit, only match the perimeter and the area of capacitance. This mean that the first step is to create the layout with the dummy elements and then see the value of the extracted dummies. The second step is to add these elements in the schematic. The following menu in fig. 4.25 shows how to do so.

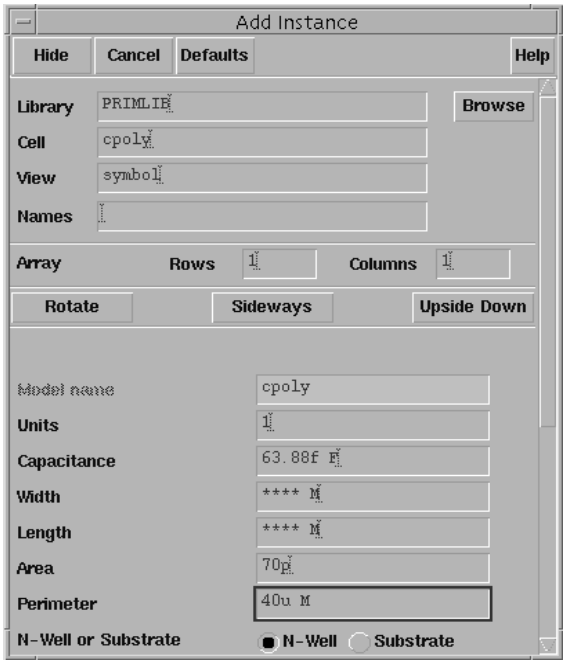

Fig. 4.25 Menu for dummy capacitance in schematic.

One has to provide the perimeter and the area value; doing this, some *** will remplace the width and length value of the capacitance.

4.2.1.4. Rooting care

4.2.1.4.1 Dummy lines

Once the designing structure chosen, in order to minimise the mismatch between the two differential branch of the operational amplifier, one has to care on the rooting. In the previous paragraph, we have discussed about the optimum topology in layout design. One must not forget the possible generation of mismatch when rooting the different elements. Dummy lines have been added in order to create same perturbation form rooting for the 2 branch. The example of a metal dummy line is set in fig. 4.26.

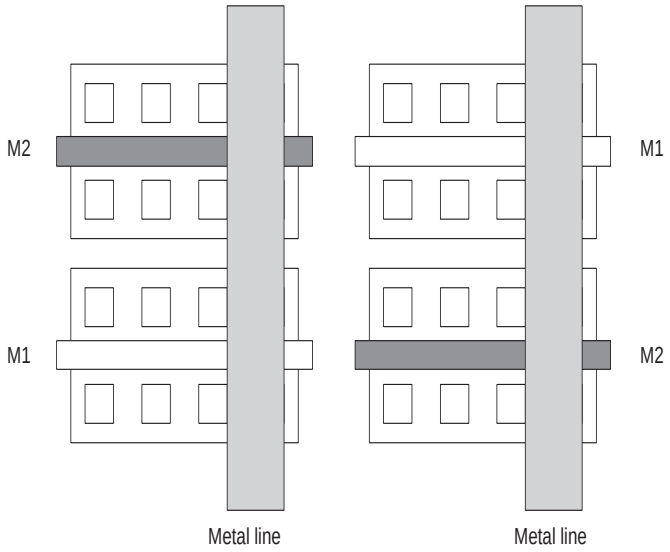

Fig. 4.26 Dummy metal line

4.2.1.4.2 Contact size and layers width

The maximum allowed DC-current densities are derived from reliability experience of the AMS process. The values specified in fig. 4.27 are also applicable as effective AC-current densities. In addition, the peak AC-current densities must not exceed 10 times the specified DC-value.

Layer type :	Maximum current density value :
METAL 1	1 mA/µm
METAL2	1 mA/µm
METAL 3	1.5 mA/µm
CONTACT 0.4µm/0.4µm	0.9mA/cnt
VIA (MET1 / MET2) 0.5µm/0.5µm	0.6mA/via
VIA (MET2/MET3) 0.5µm/0.5µm	0.9mA/via

Fig. 4.27 Maximum current densities towards layer type (extracted from AMS process)

4.2.1.5. Minimum gate finger number

As a rule of thumb, the width of each finger is chosen such that the resistance of the finger is less than the inverse transconductance associated with the finger. In low noise application, the gate resistance must be one-fifth to one-tenth of the 1/gm. For the AMS 0.35µm CMOS process, the poly1 gate resistance is 9 Ω/Square. The input transistor transconductance is 2ms, this means that

the total input gate resistance Rinput should verify :

$$50 \leq Rinput \leq 100$$

4.2.2. Actual layout

4.2.2.1 Input stage

The input transistor have to be designed with special care, because mismatch will be amplified by the output stage. The transistors are divided into several parts to make then better match in case of process variations as explained before.

The topology chosen is shown in fig. 4.28

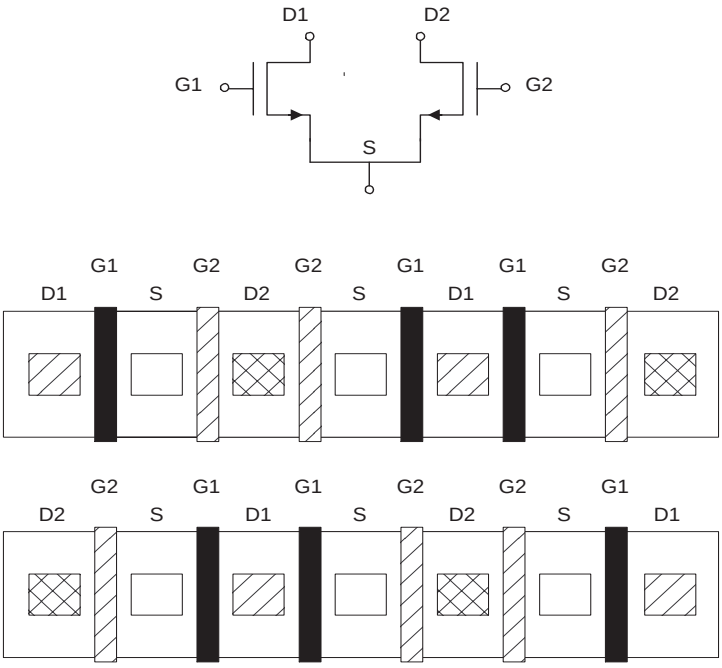

Fig. 4.28 Input transistor topology.

The layout design of this stage is given next page, on fig. 4.29

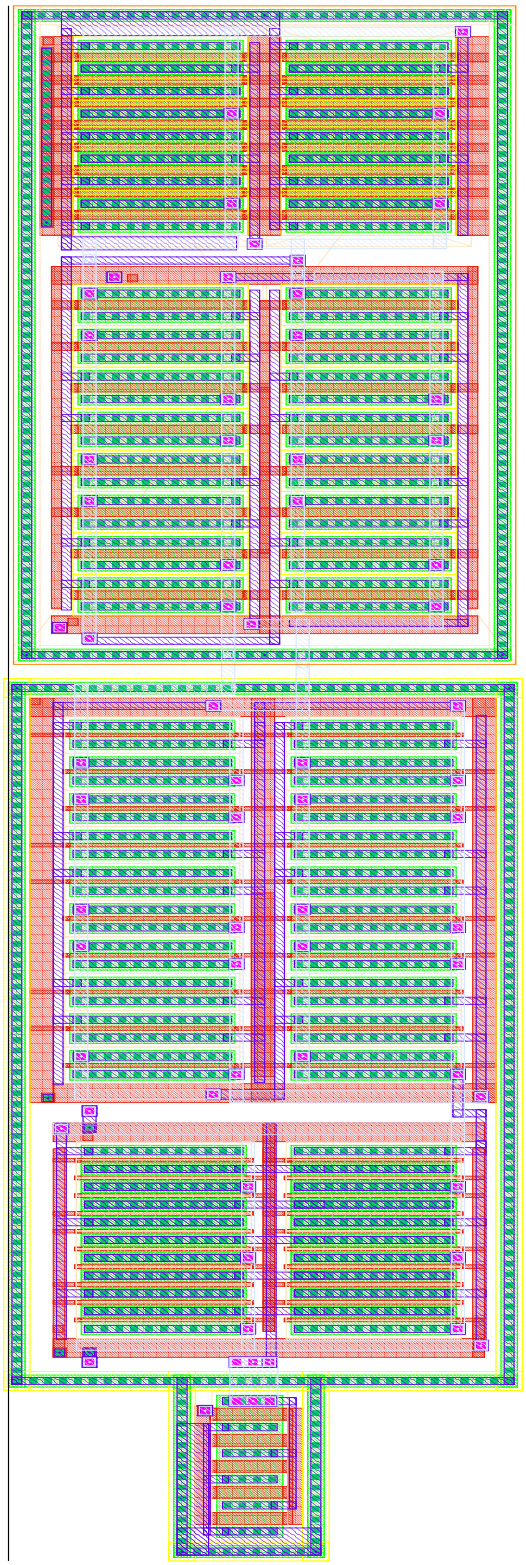

Fig. 4.29 Input stage Layout.

4.2.2.2 Output stage

The topology of the output stage uses the same kind of topology as the input transistor. The layout of these transistor are given on the following fig. 4.30

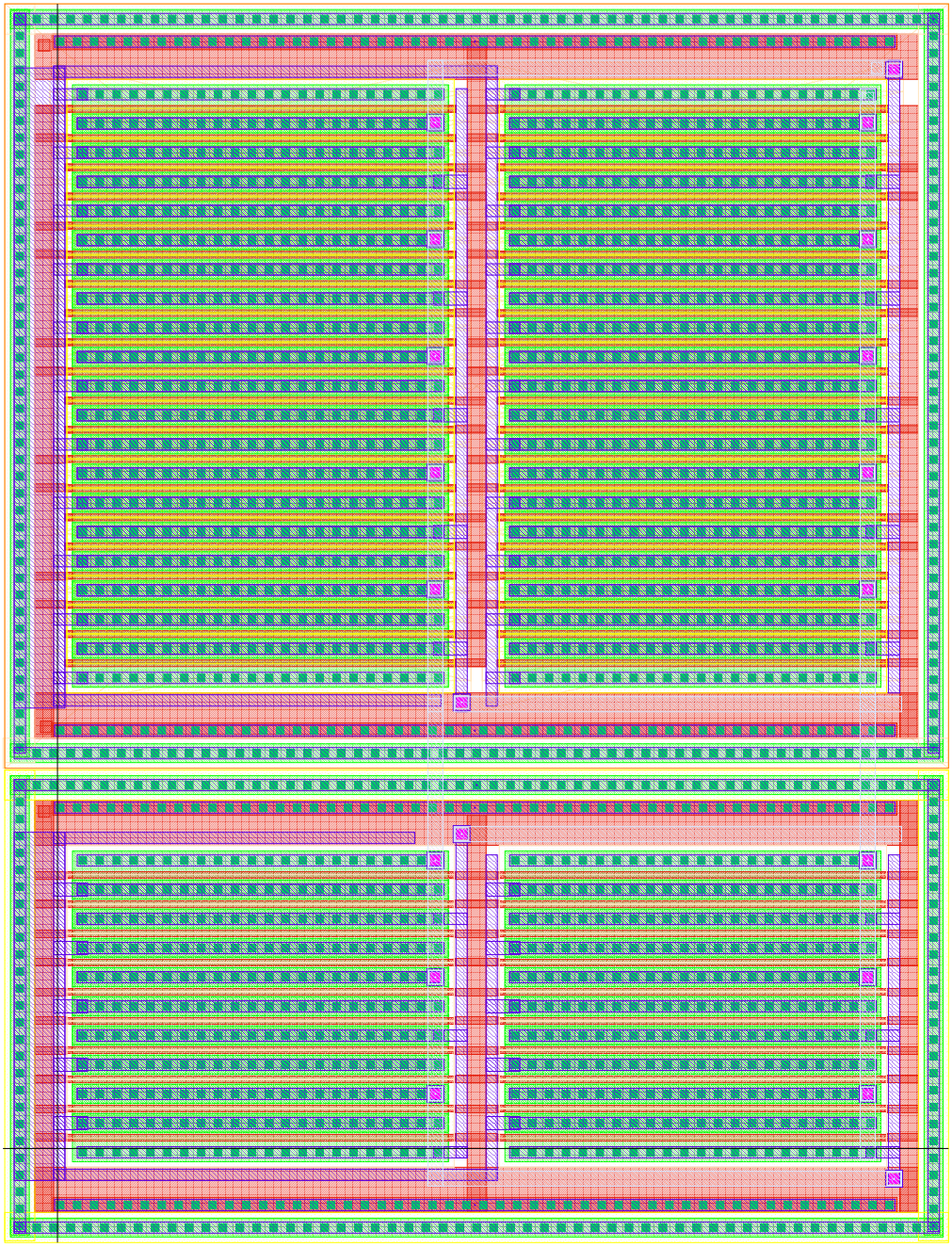

Fig. 4.30 Output transistor Layout.

4.2.2.3. Overall layout of the operational amplifier

The overall layout of the operational amplifier is given in fig. 4.31.

4.3 Layout Versus Schematic (LVS)

After one has designed the layout, the component from the layers have to be extracted. This step made, the comparaison has to be made between the extracted components and the components present in the schematic. This is the LVS (Layout Versus Schematic) step.

The result of the comparation between the schematic netlist and the extraction netlist produce a file to show the result of the matching operation. The file is given below; one can see that the two netlist match, this means that no rooting mistakes have been made during the generation of the layout.

```
@(#)$CDS: LVS version 4.4.3 10/27/1999 14:44 (cds230) $

Like matching is enabled.
Creating /home/fallu/LVS/xref.out file.

    Net-list summary for /home/fallu/LVS/layout/netlist
       count
40nets
12terminals
103nmos4
74cpoly
148pmos4
8rpoly2
```

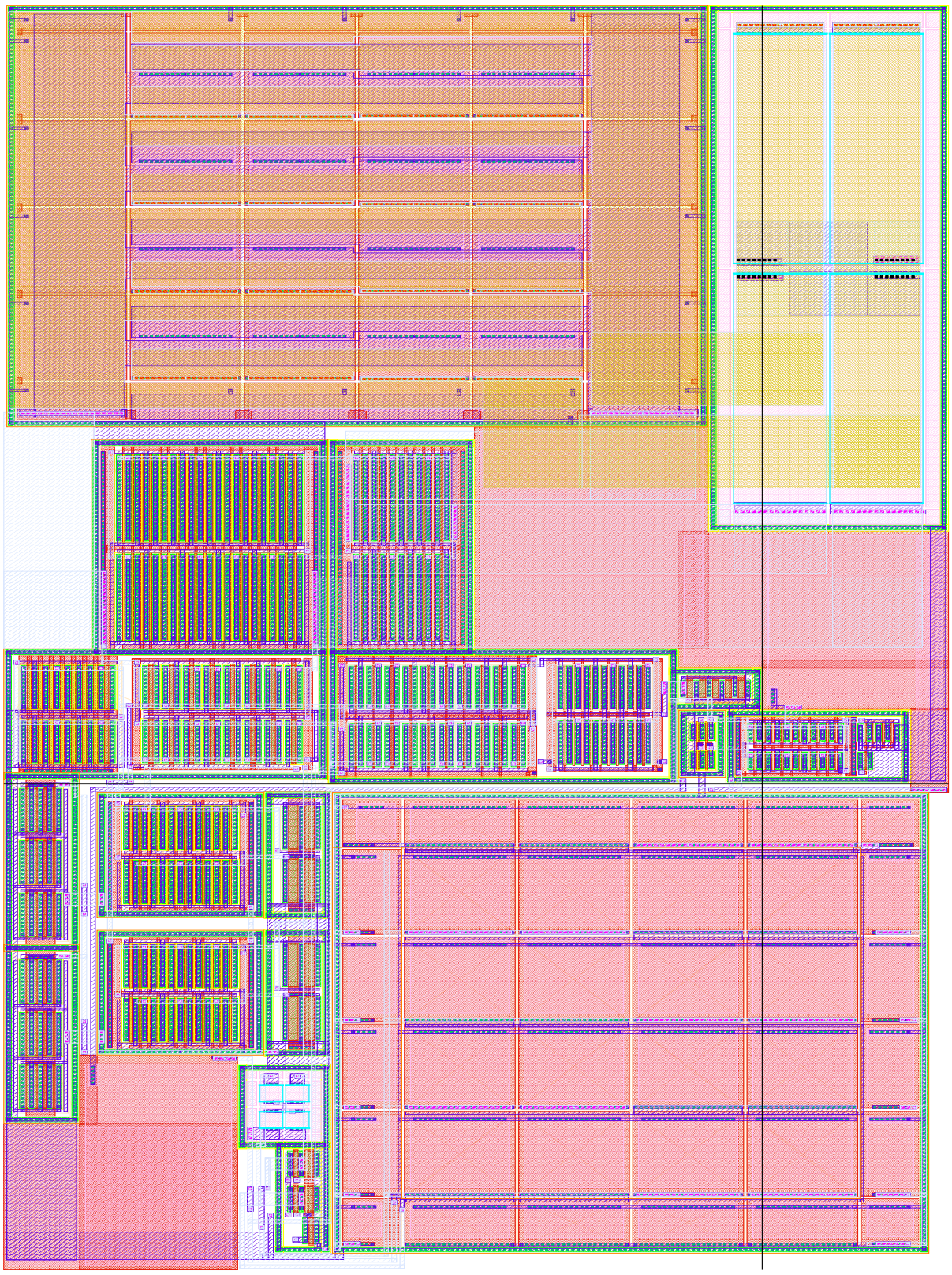

Fig. 4.31 Overall layout.

```
    Net-list summary for /home/fallu/LVS/schematic/netlist
       count
40nets
12terminals
20nmos4
74cpoly
18pmos4
8rpoly2

The net-lists match.

     layout  schematic
instances
un-matched00
rewired00
size errors00
pruned00
active333120
total333120

  nets
un-matched00
merged00
pruned00
active4040
total4040

terminals
un-matched00
matched but
```

```
different type00
total1212

Probe files from /home/fallu/LVS/schematic


devbad.out:
netbad.out:
mergenet.out:
termbad.out:
prunenet.out:
prunedev.out:
audit.out:

Probe files from /home/fallu/LVS/layout

devbad.out:
netbad.out:
mergenet.out:
termbad.out:
prunenet.out:
prunedev.out:
audit.out:
```

4.4 Post layout simulation

The extraction of the parameters can be made with parasistic elements. These are only capacitance between the different layers. As the width of the layers are not that big, the parasistic capacitance extracted are consequently not big. This means that post-layout simulations doen’t change the results in a large extend (fig. 4.32).

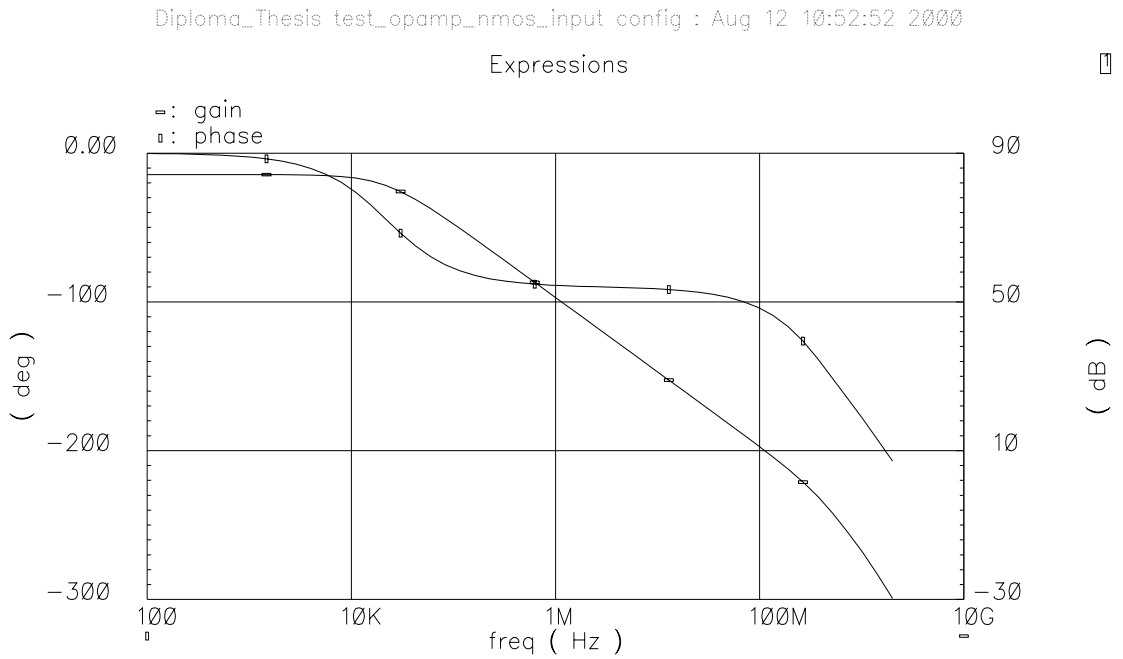

Fig. 4.32 Post layout simulation. Additional parasistic capacitance.

The “Hierarchy Editor” can help one to solve the problem due to the parasistic extraction. One can simulate the circuit using combined schematic and extrated netlist. This can help fixing the source of lower performance.The example of such menu is shown on fig. 4.33.

Making simulations does have a sens when model use justification is given. This mean that a designer should be aware of process and mismatch variations; For a chip production, several parameters can help to know how many chips will fullfill the specifications.

4.4.1 Worst case simulation

Process corners represent a selection of technological worst cases for each device type.
Process characterisation allows AMS to give process control parameters. In worst case model, the parameters are set to +3 Sigma and -3 Sigma. This mean that the value of the 4 parameters are set to the lower and upper limit of the gauss function corresponding to 99.7% of the case.
The next figure (fig. 4.34) shows the parameter values (threshold voltage and oxide thickness) towards the model name.

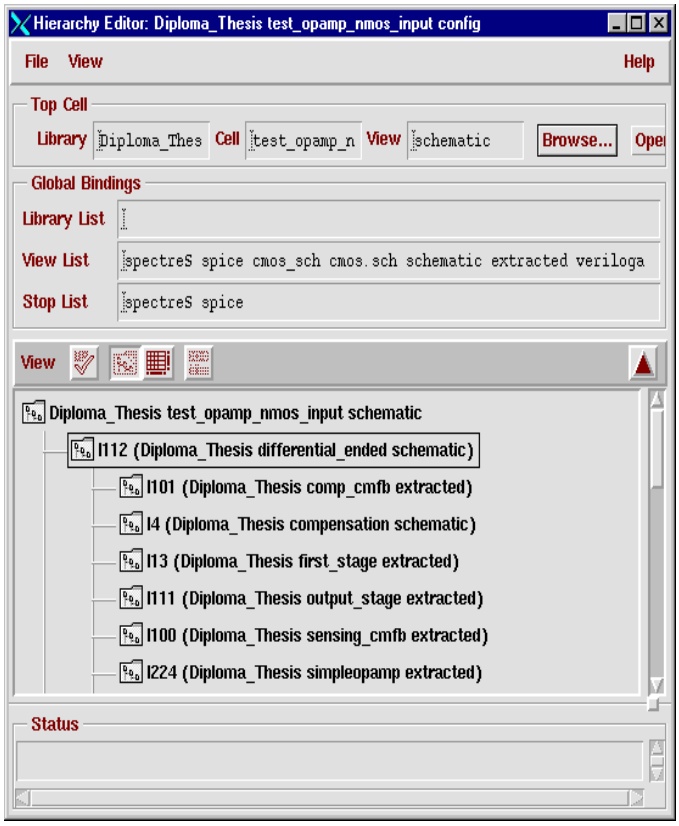

Fig. 4.33 Config menu example.

Model name	Threshold voltage	Oxide thickness
Typical mean (tm)	465.5 mV	7.7 nm
Worst case speed (ws)	575.5mV	7.9 nm
Worst case power (wp)	375.5mV	7.1 nm
Worst case zero (wz)	575.5 mV	7.5 nm
Worst case one (wo)	375.5 mV	7.5 nm

Fig. 4.34 Paramters value towards model name

4.4.1.1 Worst Power simulation

Worst power model corresponds to the -3Sigma Monte Carlo Model. The simulation result is shown below (fig. 4.35).

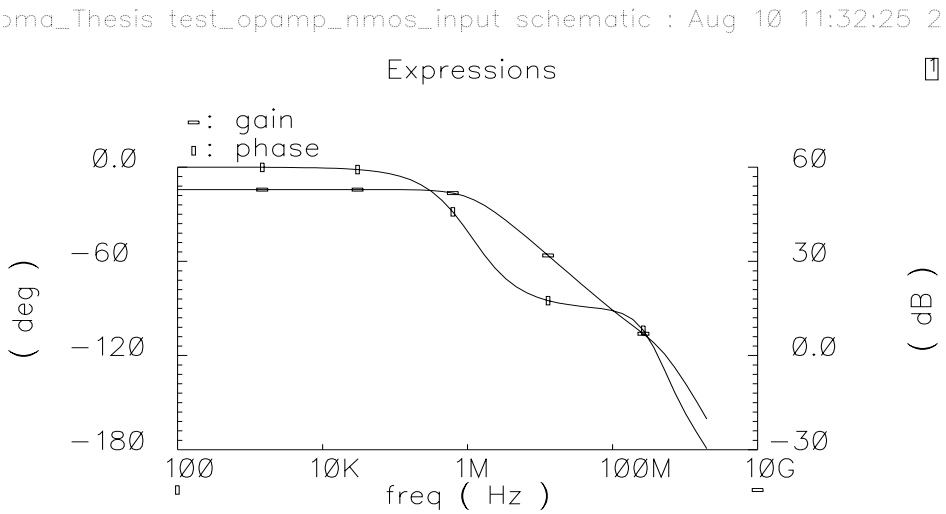

Fig. 4.35 Worst power gain and phase curve.

4.4.1.2 Worst Speed simulation.

Worst speed model corresponds to +3Sigma values of Monte Carlo model. The curve result is shown below (fig. 4.36).

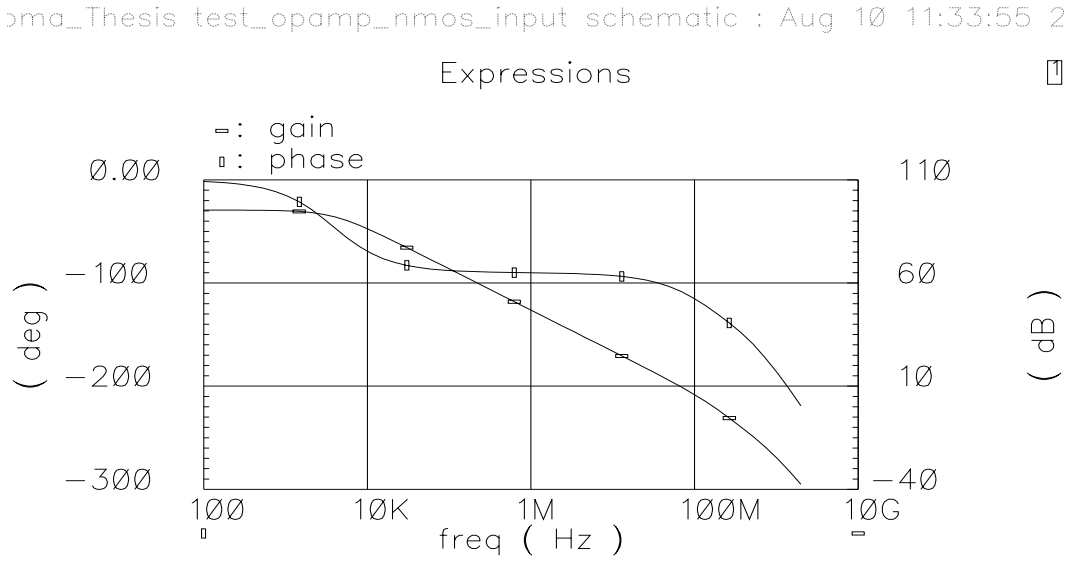

Fig. 4.36 Worst Speed gain and phase simulation.

4.4.1.3 Worst Zero simulation.

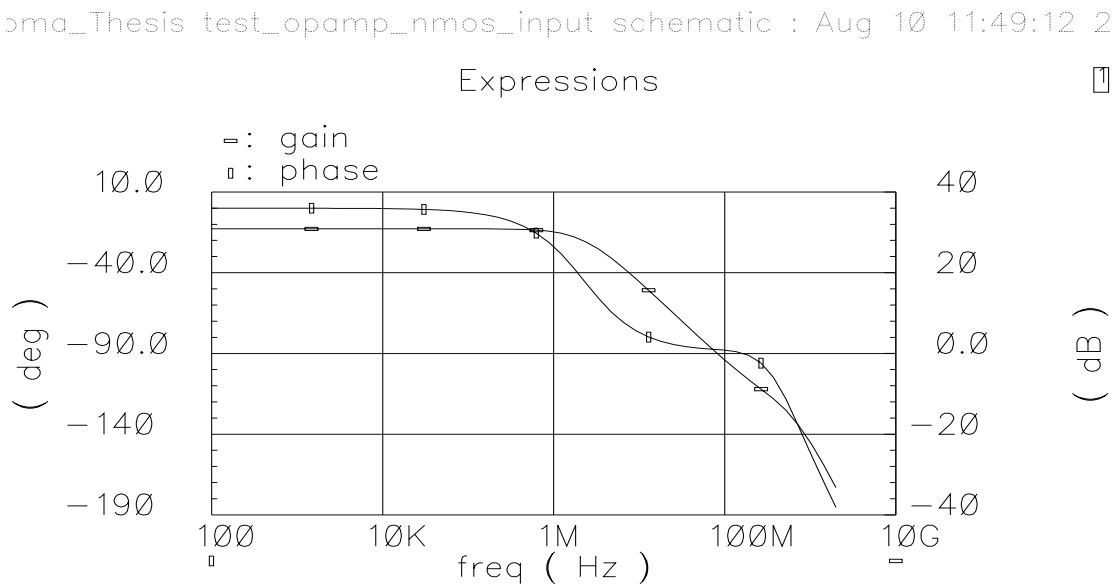

Fig. 4.37 Worst Zero gain and phase simulation.

The Worst Zero model corresponds to a +3Sigma value for the threshold voltage and a different value than the typical mean value for the oxide thiness. Fig. 4.37 shows the result when the mode lis used.

4.4.2 Other model

The following curve on next page (fig. 4.38) shows simulation made with the model untitled “AMS_Model”.

4.4.3 Monte Carlo simulations

Monte Carlo analysis provides information on circuit performance towards process variation and mismatches. For this purpose, SPICE-parameters are assumed to have statistical distrribution.

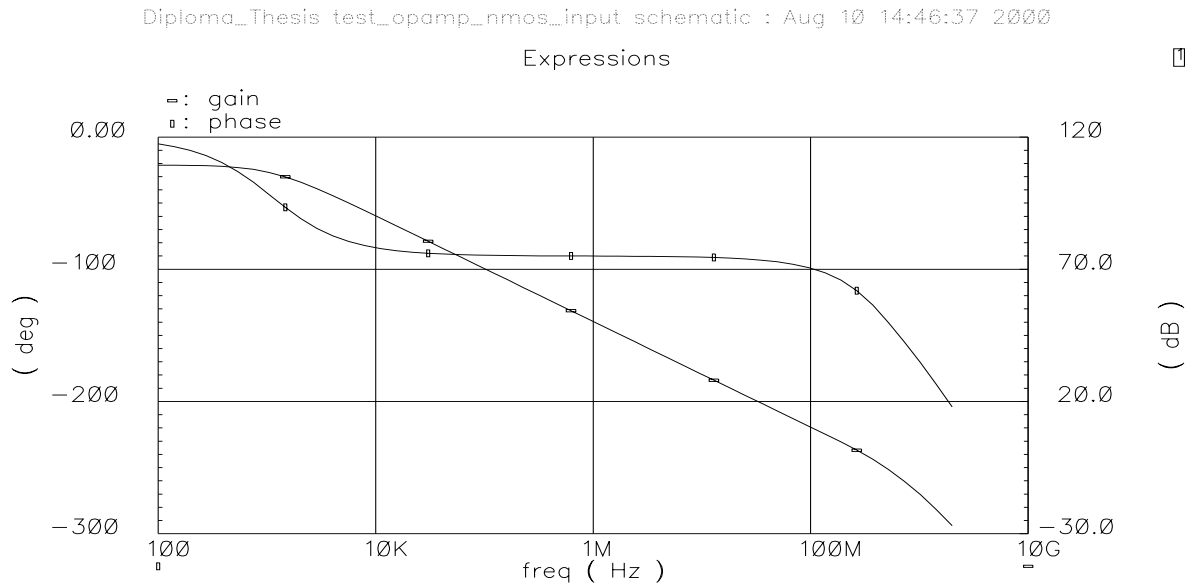

Fig. 4.38 “Cmos15 model” gain and phase simulation.

Some of the MOS transistor parameter do not vary independently: NMOS and PMOS transistors of the same wafer should have the same tox, WD, etc. Even for one type of transistor, most parameters are correlated. In principle, only 4 parameters, Tox, Xl, Xw, and Vth0 are linearly independent and their tolerances are related to process variation. As they vary independantly, one can understand that their values corresponds to a gaussien distribution. The exemple of the threshold voltage distribution is set in the following fig. 4.39.

This mean that Monte Carlo simulation gives a realistic distribution of the operational amplifier performance, when the chips are coming from a same wafer.

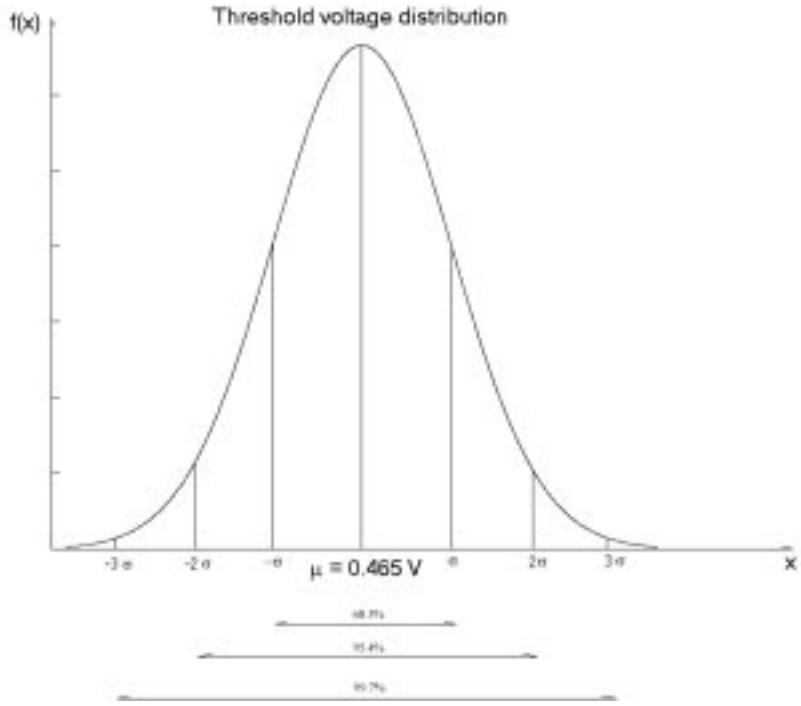

Fig. 4.39 Threshold voltage distribution.

4.4.3.1 Process variations

The DC gain distribution is given below on fig. 4.40 when only process variation is set. This shows a standard variation which is 1.6 dB around 83.5 dB. One can observe the results whe nthe temperature is set to 120C and -40C (fig. 4.41 and fig.4.42). The settling time variation is also considered.in fig. 4.43.

4.4.3.2 Mismatch variations

The following simulation result (fig. 4.44) shows the DC gain distribution result when mismatch is considered. One has to quote that the simulator doen't take into account the design. This means that this simulation is realistic only if no layout care is taken. In other words, 2 transistor in a common centroide structure have more chance to match, comparing to 2 transistor placed far away from each other.

One can use this simulation to show how layout care is a concerning problem.

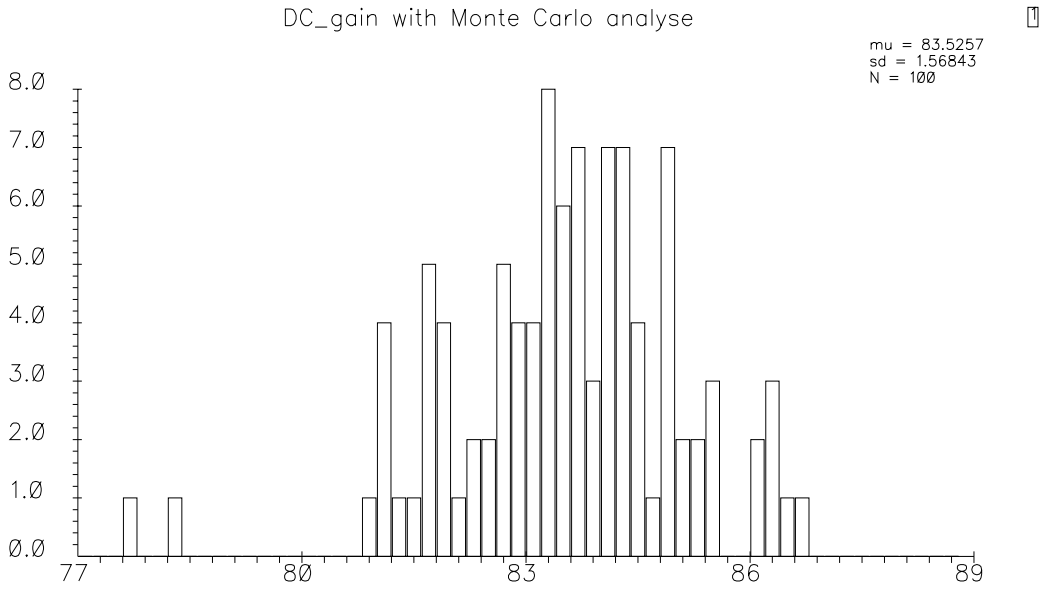

Fig. 4.40 DC gain variation with Monte Carlo process variation. T=27C.

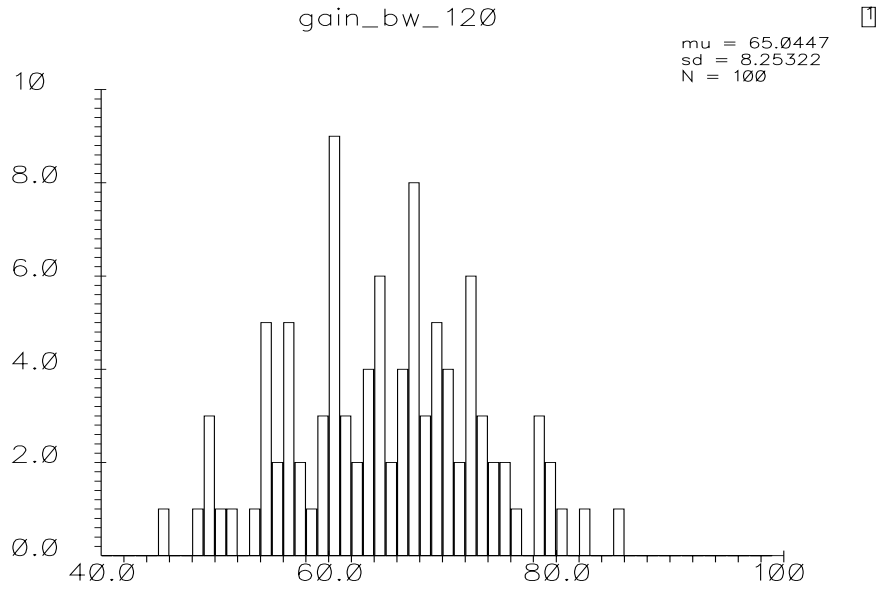

Fig. 4.41 DC gain variation with Monte Carlo process variation. T=120C

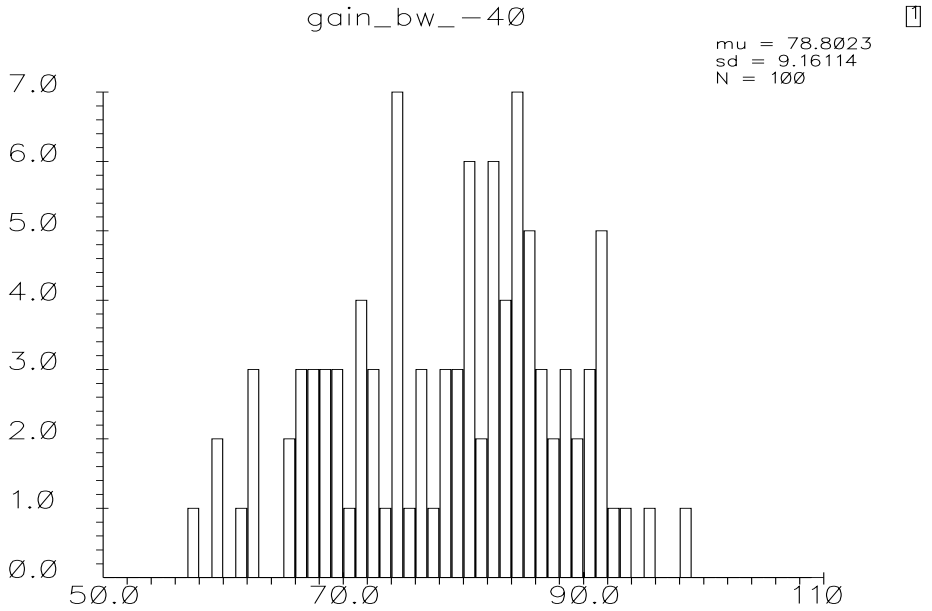

Fig. 4.42 DC gain variation with process variation. T=-40C

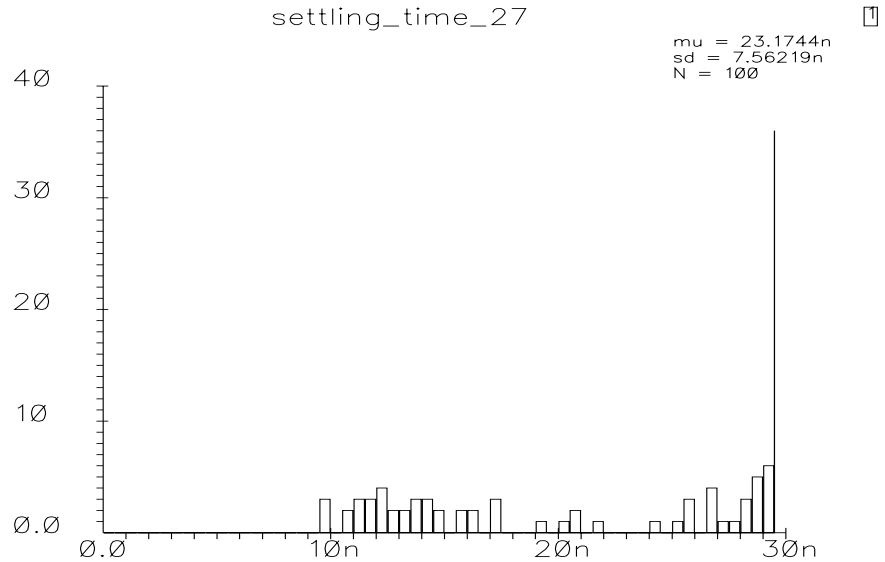

Fig. 4.43 Settling time variation with Monte Carlo process variation. T=27C

4.4.3.3 Process and mismatch variations

Monte Carlo simulation can also make vary the parameters for every transistor of the wafer at the same time (process variation), it can make vary the parameters for each transistor of the wafer (mismatch variation); it can also make vary a combinaison of process variations and mismatch variations. This means that this is the worst simulation one can ever expect to have (fig. 4.44).

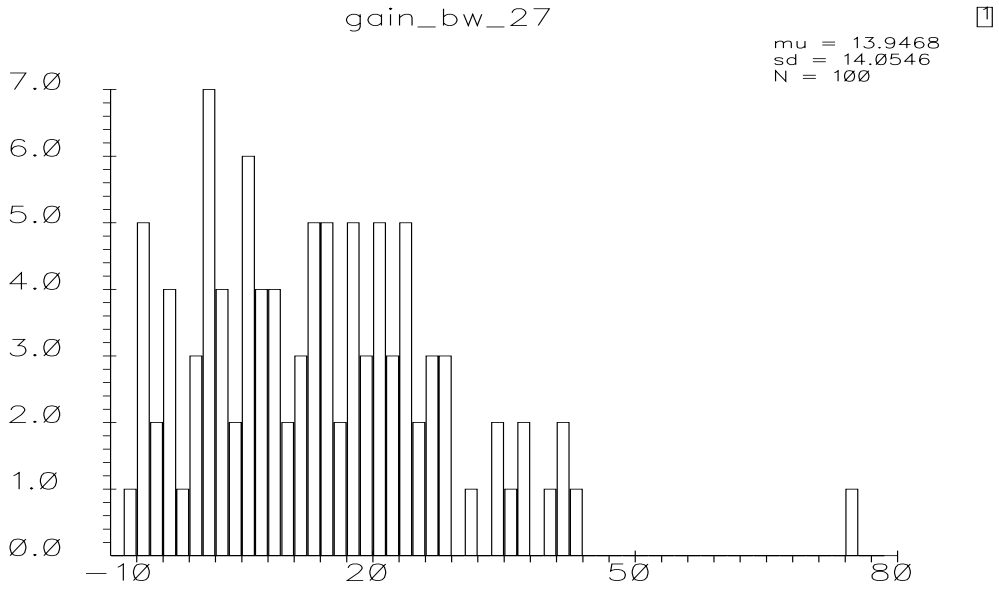

Fig. 4.44 DC gain distribution with Monte Carlo mismatch variation.

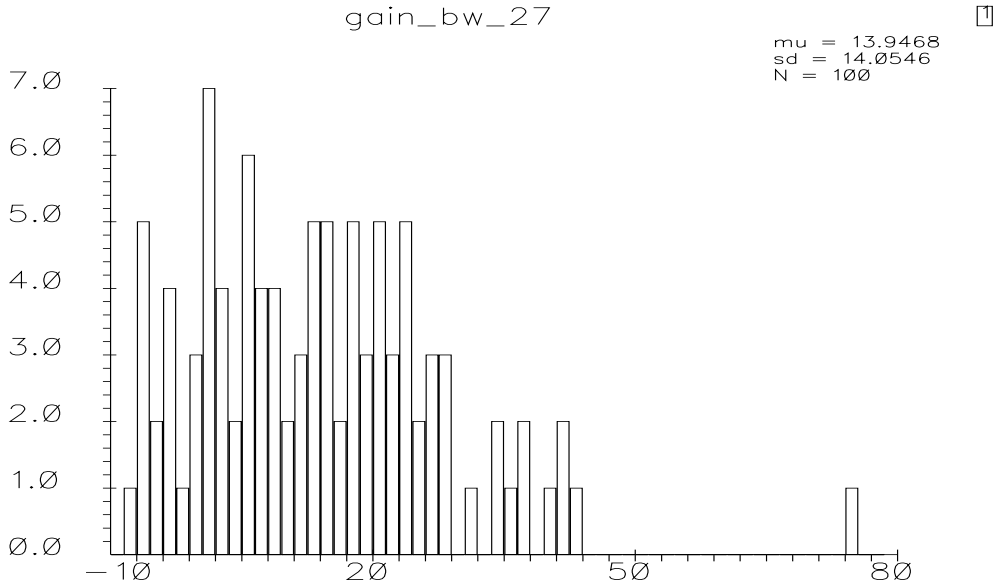

Fig. 4.45 DC gain distribution with process and mismatch variation.

4.4.4 Temperature variations.

Temperature is a concerning problem; simulation curve are given below for 2 extrem temperature (-40C and 120C) for 2 model (ws and wp). The result are shown in fig. 4.46 to fig. 4.49.

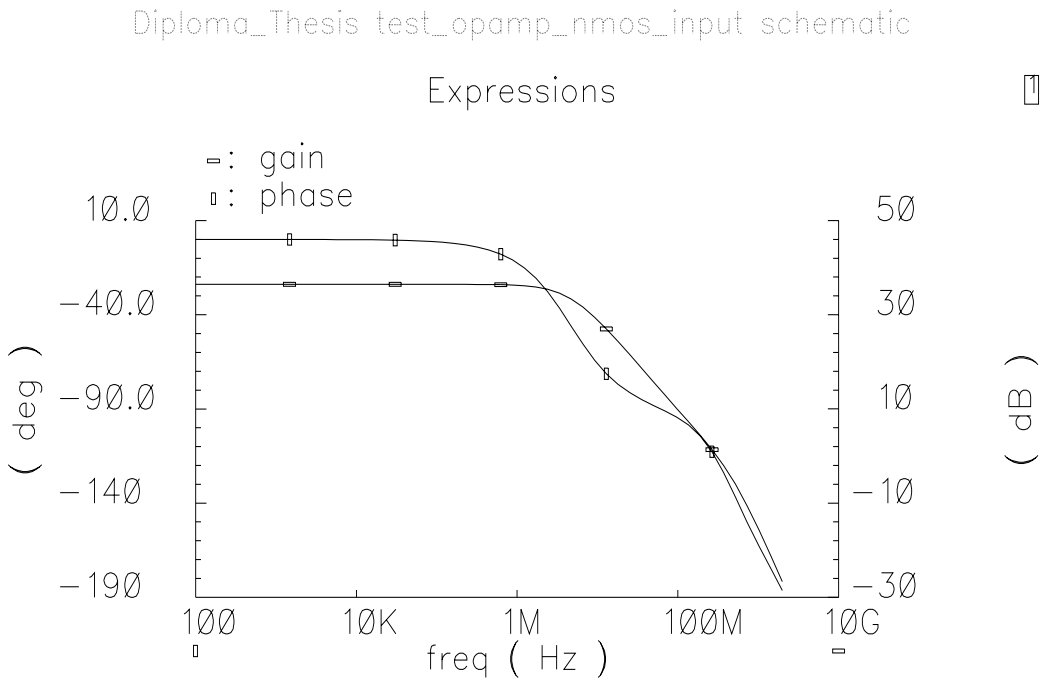

Fig. 4.46 Gain curve with wp model and T=120C

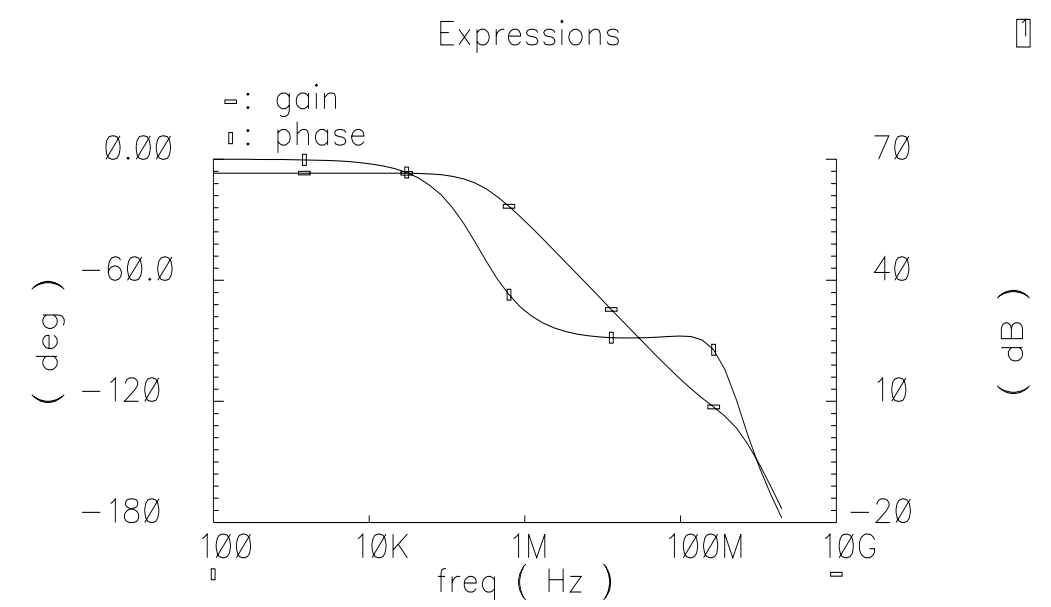

Fig. 4.47 Gain curve with wp model and T=-40C

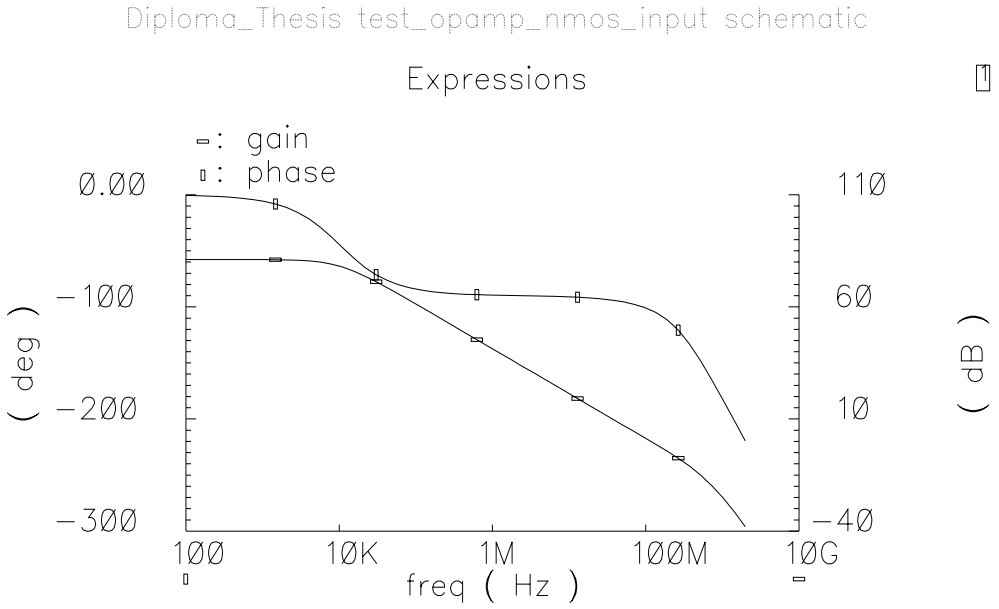

Fig. 4.48 Gain curve with ws model and T=120C

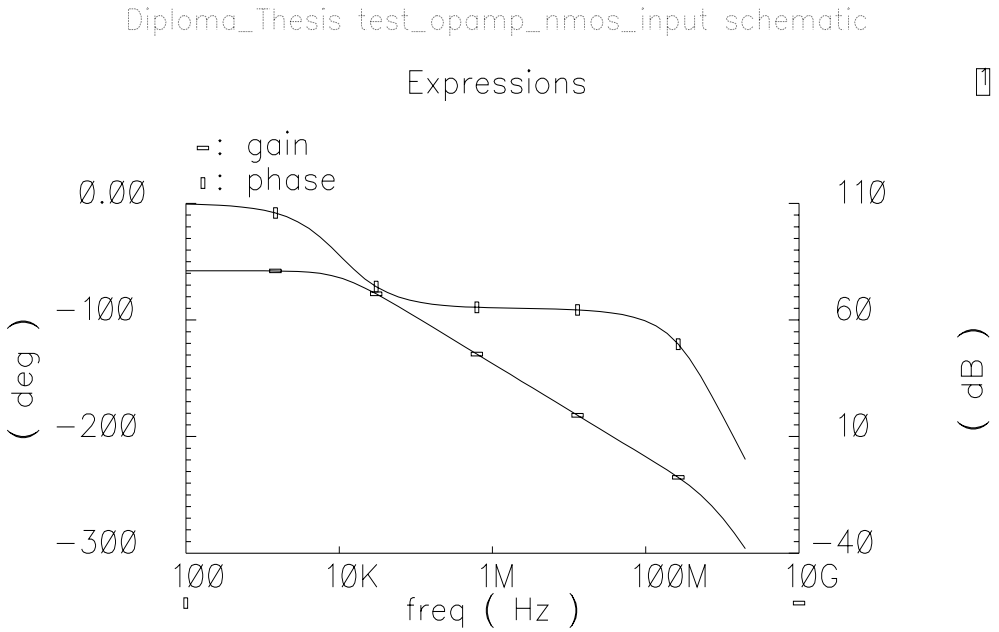

Fig. 4.49 Gain curve with ws model and T=-40C

One can note that the results are contained in a large spectrum of values. The difficulty is contained in the interpretation of these different curves and on their probability.

5. Conclusion and outlook

The topology chosen can match the desired specification. Nevertheless, this full differential operational amplifier consume a lot of power (around 140mW). This is due to the output stage that need a lot of current to charge the big capacitance of the first pipeline stage. This is the only solution I have found to reach high speed with such great load capacitance. In any case, one can ask himself about the solution for high resolution, high speed and low power consumption, when noise is to be filtered and capacitance are to be load.

In order to use this topology for the next stage, one needs to adapt this structure to smaller load capacitance. For a 2 bit per stage, the load capacitance of the second stage is 10pF. The output stage needs less current to charge this capacitance and so the current budget can be decreased. The gain in bandwidth can although be decreased, and the gain boosting can be cancelled.

As seen before, simulations with worst case models let’s appear some great changes concerning the DC gain, phase margin and unity gain frequency. Unlike bipolar transistor, MOSFETs suffer from substential parameter variation from wafer to wafer and from lot to lot. Despite decades of technology advancement, the large variability of CMOS circuits remains a fact with which analog (and digital) designers must cope. This means that for a rubust design, the performance have to be reached with any worst case model.

The idea of decreasing the supply voltage may change the topology of the circuit. For example, staking 5 transistor will, for sure, reduce too much the output swing of the input stage. The idea would perhaps be to higher the gain of the output stage and to use a simple cascode topology without tail transistor. This would mean that only 3 transistors would be stacked. After that, one can espect to control the current directly on the load transistor.

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Appendix A : Matlab use for non-linearity measurements

The spectrum analyse of the signal with the calculator of Analog Artist has shown a certain noise floor. This means that for measuring the third harmonic spike, the spike was near from the resolution of the different windows used to this spectrum analyse. The use of the window defined below, shows more clear results with Matlab.

1. Export of points

The first step is to export the points from Cadence to Matlab. The problem is that the output file from cadence is not directly usable by Matlab. First, Matlab needs two x and y input matrix, and the output file of the Analog Artist calculator gives a file which has to be filtered.
Then the output file have a maximum number of point that is not enough for a high accuracy calculation. This program spilt the data file form opus to a same matlab output file with the desired number of points.

From the calculator, one have to use the command ”printvs” to extract the points from the waveform plotting, save this points in scientific format with the maximum digit, in files named data1.wav, data2.wav...as many files as one’s need Then when the points are extracted in different files, the following command is to type :

Prompt> Wish8.2 ConvertStateToMatlab.tcl data1.wav all_data.m single
Prompt> Wish8.2 ConvertStateToMatlab.tcl data2.wav all_data.m append
Prompt> Wish8.2 ConvertStateToMatlab.tcl data3.wav all_data.m append
...

The filtering program (written by Stephan Thiel) is given below.

Convert_state_to_matlab.tcl :

```
if { $argc==3 } {
set infile [ lindex $argv 0]
set outfile  [ lindex $argv 1]
```

```
set comnd [lindex $argv 2 ]
if [file exists $infile ] {
  set fid [open $infile r]
   while { ! [ eof $fid ] } {
    gets $fid temp
       if { [string first "tmp" $temp]==0 } {
           scan $temp "tmp%i = \" %g %g \"" a x y
        if { ([info exists x]) && ([info exists y]) } {
              lappend xarr $x ; lappend yarr $y
              unset x
              unset y
           }
      }
   }
  close $fid
} else { puts " input file not exists " }
if { ($comnd=="append") && ([file exists $outfile ])} {
 set fid [open $outfile a]
 } else {
 set fid [open $outfile w]
}
set i 0
foreach xelem $xarr {
    if { $i==0 } {
     if { $comnd=="single" } {
         puts $fid "tablex=\[ $xelem \];"
        } else {
         puts $fid "tablex=\[ tablex $xelem \]; "
        }
    } else {
      puts $fid "tablex=\[ tablex $xelem \];"
    }
  incr i 1
}
set i 0
foreach yelem $yarr {
    if {($i==0) && ($comnd=="single")} { puts $fid "tabley=\[
$yelem \];" } else {
      puts $fid "tabley=\[ tabley $yelem \];"
    }
  incr i 1
}
close $fid
} else { puts "Wrong number of arguments"  }
exit
```

2. Matlab data processing

The file all_data contains now the 2 tables in matlab format: tablex and tabley.

Once the tablex and tabley set, one can use the blackman window function programmed for Matlab. The blackman-function window for matlab is given below :

```
function w = blkmhrs7(n)
% blkhrs7(N) returns the N-point 7-Term Blackman-Harris window.

   a(1) =  0.271051400693424;
   a(2) = -0.433297939234485;
   a(3) =  0.21812299954311;
   a(4) = -0.06592544638803099;
   a(5) =  0.010811742098371;
   a(6) = -0.000776584825226;
   a(7) =  0.000013887217352;

   w = (a(1) + a(2)*cos(2*pi*(0:n-1)/(n-1))  + a(3)*cos(4*pi*(0:n-
1)/(n-1)) ...
            + a(4)*cos(6*pi*(0:n-1)/(n-1))  + a(5)*cos(8*pi*(0:n-
1)/(n-1)) ...
            + a(6)*cos(10*pi*(0:n-1)/(n-1)) + a(7)*cos(12*pi*(0:n-
1)/(n-1)) )';
```

Then the matlab program is given below :

```
function fourier()
[tablex,tabley]=all_data;
table_newy=blkmhrs7(length(tabley)).*tabley';
Z=abs(fft(table_newy));
plot(Z);
```

This returns the discrete fourier transformation (dft) of the output signal with more accuracy.

Appendix B : Monte Carlo simulations setting up

SPECTRE Monte Carlo Analysis

1. Introduction

Monte Carlo analysis allows the investigation of both process spread and device mismatch. For this purpose, SPICE-parameters are assumed to have a statistical distribution based on the process statistic or measured device matching statistic. A typical Monte Carlo run generates several multivariate random samples of the parameter vector and performs the desired circuit analysis for each sample. Afterwards, the distribution of the output variables can be analysed by means of descriptive statistics (mean, standard deviation, higher order moments) as well as graphical statistic tools (histograms, approximate distribution function, scatter plots, ..). Statistical sensitivity analysis can be performed by correlating original SPICE parameters (input variables) to circuit output variables. The advantage compared to a worst case analysis is, that an estimation of the probability for specific ranges of output variables is obtained and can be a help for the designer to center their design based on a process dependent statistical distribution and to improve the yield. The problem with standard worst case analysis is that worst cases are assumed to lie on corners of the parameter range and therefore can be very pessimistic in terms of probability.

In the implemented Monte-Carlo procedure for Spectre random parameter variations are defined via the model cards and special update-files. The implemented version allows for both a combined simulation of process and device mismatch as well as single process and single mismatch simulations.

2. Supported processes

Monte-Carlo parameters have been generated for the following processes:

- CXX
- CYX
- BYX
- CUX

- CAX
- CBT
- CXT

Monte-Carlo parameter files are allocated in the device specific sub-directories:

```
$AMS_DIR/spectreS/_process/_device/mc
```

---

3. How to perform Monte Carlo Analysis in SPECTRE/Cadence

The following short tutorial describes the fundamental steps for performing a Monte Carlo Analysis using the `Analog Artist` and the `Spectre-` simulator.

1. **Necessary Setup-definitions**

   In the `Analog Artist` define simulator- and model paths in the following order:

   1. `Setup-Simulator/Directory/Host:`

      Enter the **full path** of your `SIM-directory`. Relative paths will not work with the Cadence Monte Carlo tool !

   2. `Setup-Model Path`:

      Enter the full model paths for all the devices you want a Monte Carlo analysis to be performed. Model paths are of the form:

      ```
      $AMS_DIR/spectreS/_process/_device/mc
      ```

2. **Define environment files for combined process-variation/matching simulations or a single matching simulation**:

   Two environment-files have been created for the definition of process-dependent random variables:

   `update.s` and `matching.s`

   These files are located in the directory:

   ```
   $AMS_DIR/spectreS/_process
   ```

   and have to be defined in the `Analog Artist` depending on which analysis you want to perform.

   - For a combined process/matching or a single process variation-simulation enter

     ```
     $AMS_DIR/spectreS/_process/update
     ```

in the field `Update File` of the `Setup-Environment` - Menu.

- For a single matching simulation enter

  `$AMS_DIR/spectreS/_process/matching`

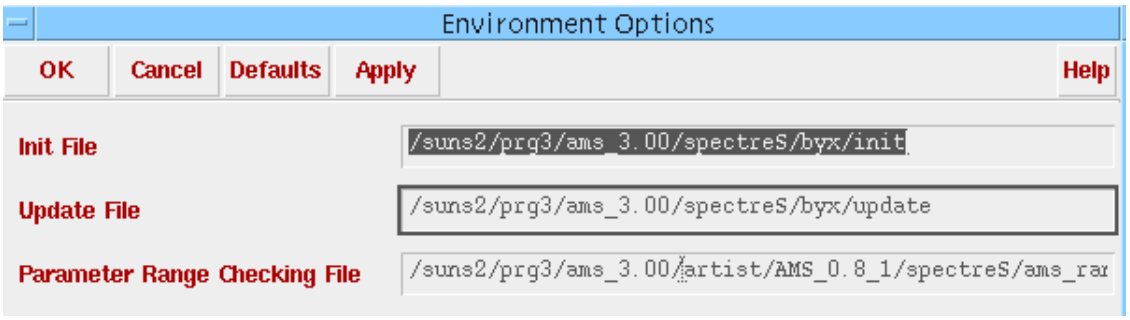
  in the field `Update File` of the `Setup-Environment` - Menu.

Furthermore, an initialization-file has to be defined. This file is necessary in Cadence97 to account for uniformly distributed random variables. The definition of this file will not be necessary in following versions of Cadence.

For definition of the init-File enter

- `$AMS_DIR/spectreS/_process/init`

  in the field `Init File` of the `Setup-Environment` - Menu.



3. **Choose an analysis type and perform a standard simulation of your circuit.**

   Prior to the Monte Carlo simulation a standard analog simulation of the circuit has to be carried out. Be sure to define all the variables you want to be saved, choose your analysis type and run your standard simulation.

4. **Define expressions for the Monte Carlo simulation**

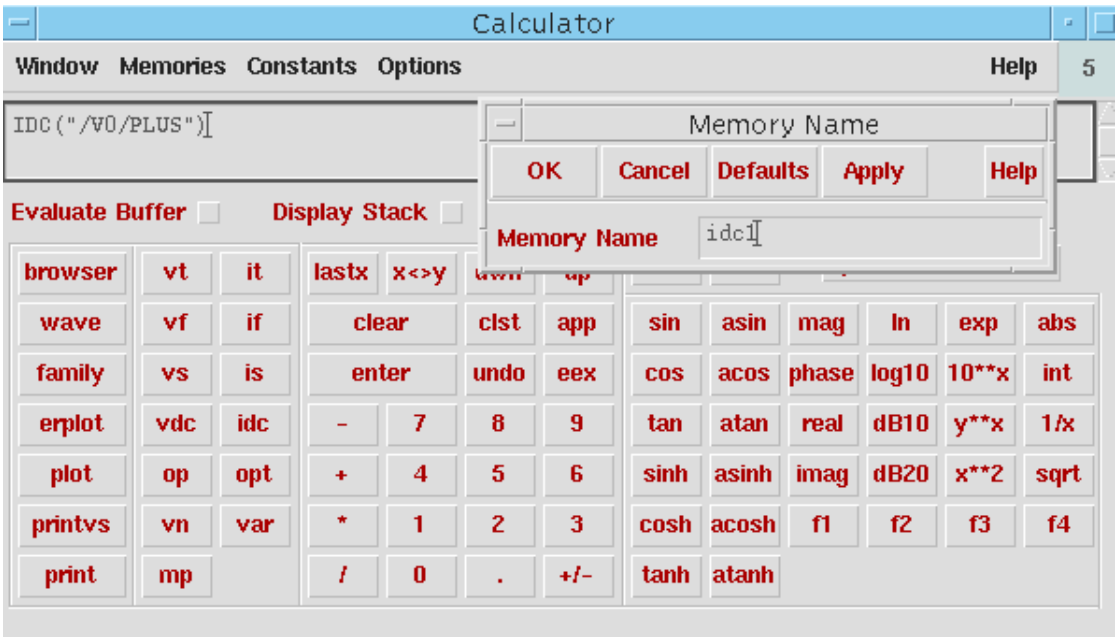
   Expressions to be evaluated during a Monte Carlo run (output variables) have to be defined via the Calculator.

   1. Select `Tools Calculator` and define your output expressions. For this purpose choose the expression in the calculator and select the corresponding instance in your schematic.

   2. Store the defined expressions in the Calculator Memory by selecting

      `Memories Store`

      in the Calculator menu.



5. **Define Monte Carlo Simulation-Setup**

   Select

   `Tools - Monte Carlo`

   from the `Analog Artist`-menu and carry out the following steps:

   1. Copy Monte Carlo expressions from the calculator memory by selecting

      `Edit Add`

      from the Monte Carlo Simulation window.

   2. Define Simulation type and number of runs.

      Select

      `Setup Define`

      from the Monte Carlo Simulation menu. Then the the Analysis Mode and the number of Monte Carlo runs have to be defined.

      Select

      `Random variations with mismatch`

      if you want to perform a single mismatch simulation (Update File = `mismatch`) or a process simulation including device mismatch (Update File = `update`).

Select

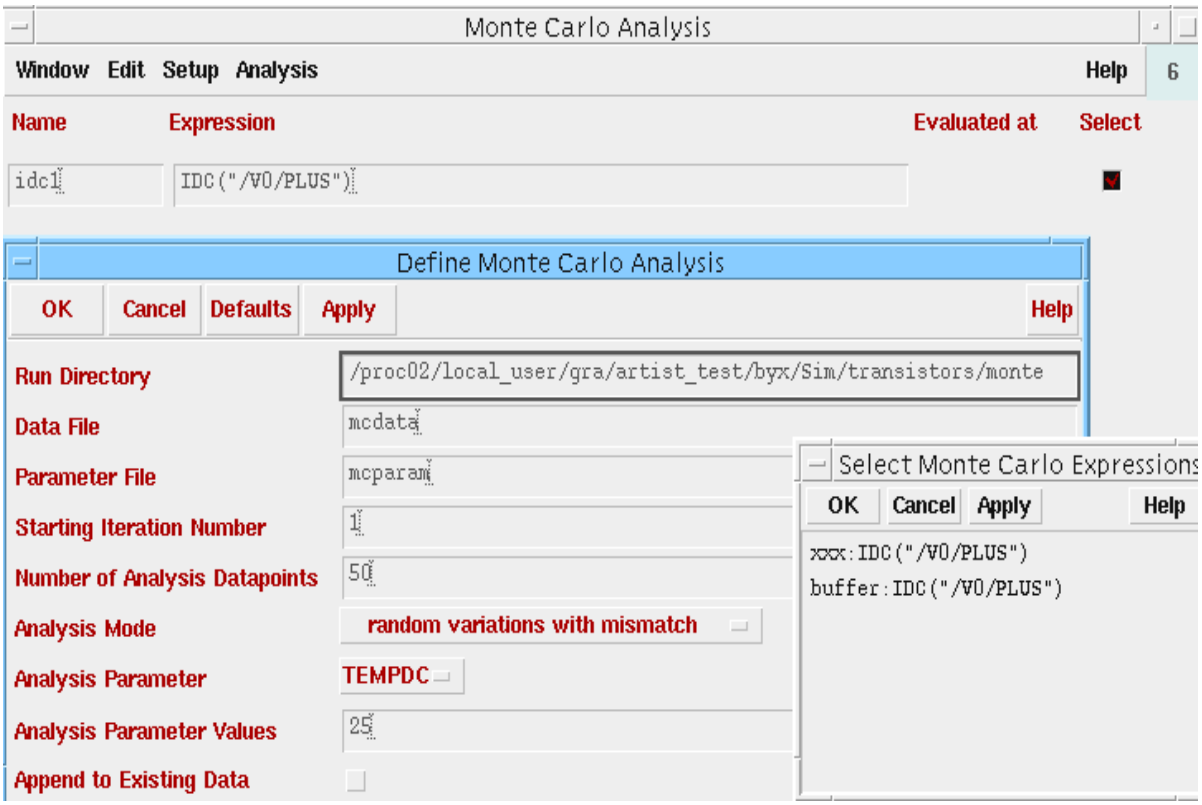
```
Random variations only
```

if you want to perform a single process simulation without device mismatch (Update File = `update`).

Choose number of Monte Carlo runs by selecting

```
Number of Analysis Datapoints
```

Since the quality of a Monte Carlo simulation relies on the central limit theorem, a larger number of samples will lead to a more accurate result. A small sample size will overestimate the weight of outliers in the samples. Check that the mean and standard deviation of your output variables converge, e. g. by considering two runs with different sample sizes.



3. Start Monte Carlo Simulation

   ```
   Analysis Start
   ```

6. **Statistical Analysis of Output Data**

For the statistical analysis of your Monte Carlo expressions select

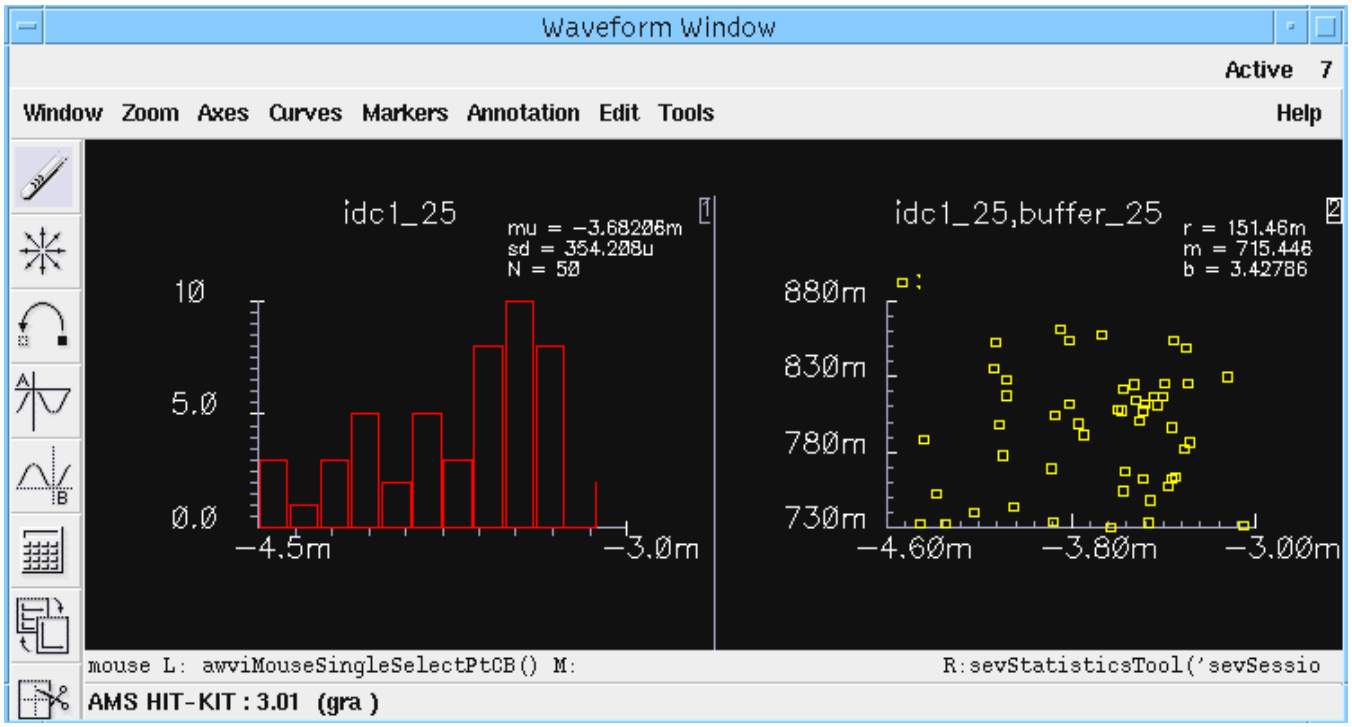
```
Tools Statistics
```

in the `Analog Artist Simulation`-menu. Then you can choose the type of statistical analysis you want to carry out.

E.g., to obtain a histogram of output-variables select

`Plot Histogram`

from the Statistical Analysis Window and add your output variables to the plot list. Similarly you can produce scatter plots and correlation tables.



Appendix C : AMS Device Matching Rules

Device Matching Rules

1. Introduction

Matching tolerances occur from several effects:

1. Random process variations (local matching error)
2. Process gradients across die (distance effect)
3. Systematic influence of adjacent structures (proximity effect)
4. Non-isotropic effects (orientation effect)

Most of these effects can be minimized by appropriate layout techniques. The present state of art is described below for different device types. In addition some basic design techniques should be applied to keep the tolerances low.

Process anisotropies may result from certain processing steps (plasma etching, ion implant angle) or lattice orientation, and affect mainly MOS devices. As a result, it may be important how devices are oriented relative to each other or relative to the die flat.

Finally die stress from packaging or thermal gradients may cause considerable parameter changes or drift. Pre- and post-assembly electrical parameters may be unequal. Partially this can be avoided by symmetric placement of critical components with respect to the main die symmetry axes. It may even become necessary to apply special assembly techniques like coating, or to change the position of the die inside the mold.

2. Design Techniques

Technique	Device Type	Notes
maximize size	all	if possible
unit elements only		
maximize L	MOS	
maximize W		
same L for mirrors		
operate in strong inversion		
maximize W	RES	
match same device type		(e.g. don’t match Rpoly with Rnwell etc.!)

---

2. Layout Techniques

Technique	Device Type	Local	Distance	Proximity	Anisotropy
minimize spacing	all		X		
maximize size		X			
adjacent parallel placement			X		X
surround by dummy elements				X	
split & common centroid		X	X		
split & interleaf		X	X		
unit elements only		X			
maximize L	MOS	X			
maximize W		X			
same Drain-Source orientation					X
constant area/perimeter ratio	CAP	X			
match contacts	RES	X			
match bends (shape)		X			

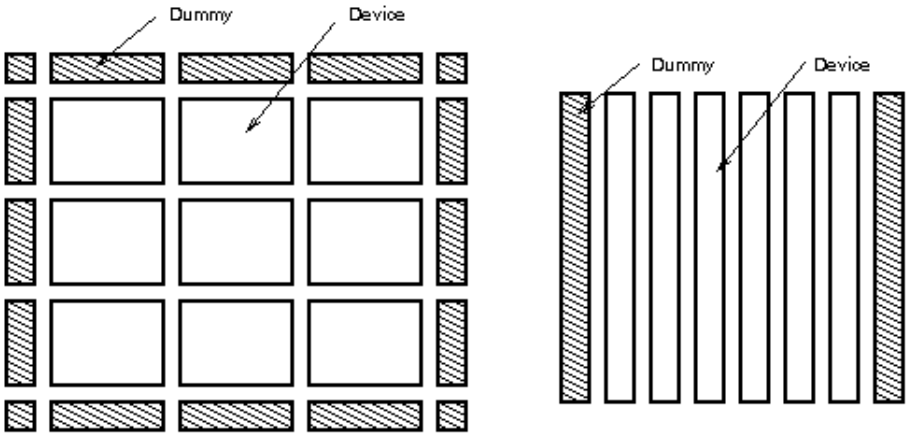
More Recommendations:

- Combinations of above techniques are allowed and recommendable
- Avoid 45° and other rotation angles (mask tolerances)
- Shape capacitor corners at 45° angle
- Shape serpentine resistor corners at 45° angle
- Keep surrounding of critical components uniform (if possible)
- Consider ground bus series resistance for current mirrors
- Consider parasitic wiring and contact series resistances
- Match interconnect wiring (capacitances) for good dynamic balance
- Please refer to our designrule documents for resistor and capacitor layout examples

---

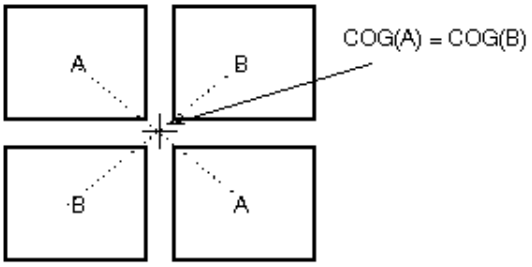
3. Illustrations

Dummy Layout Technique for Capacitor and Resistor Arrays

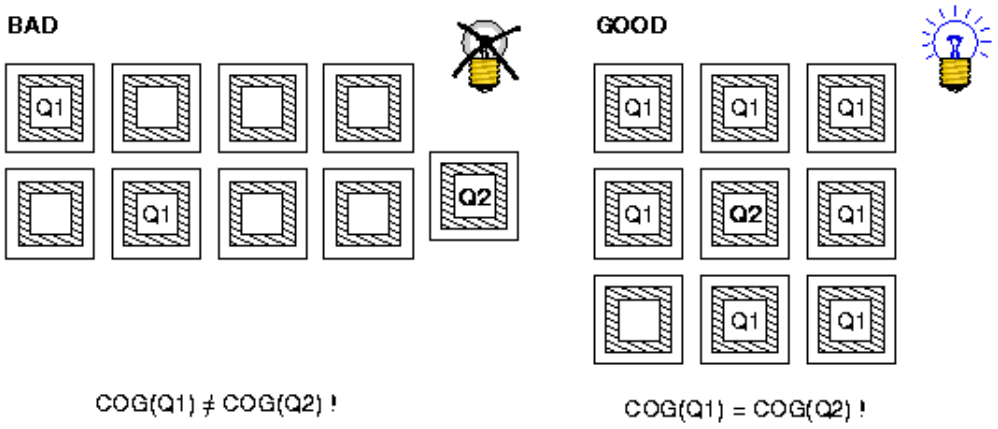


(Back)

Common Centroid Layout Example

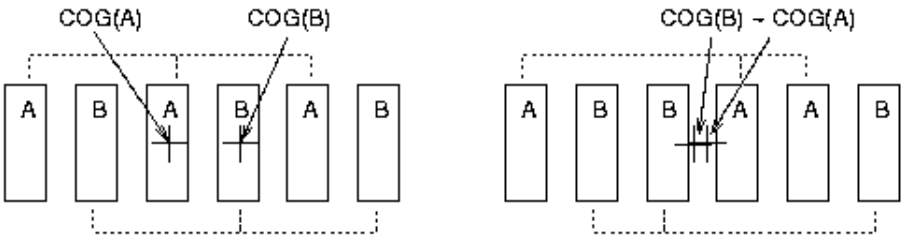


Common Centroid Bipolar Array (e.g. for Bandgap circuit)



(Back)

Interleafed Layout Examples

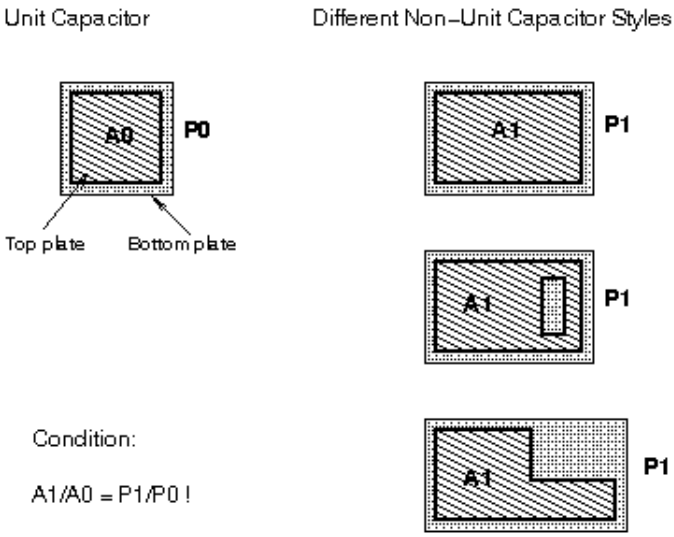


(Back)

MOS Drain Current Orientation

(Back)

Capacitor Unit and Non-unit Layout



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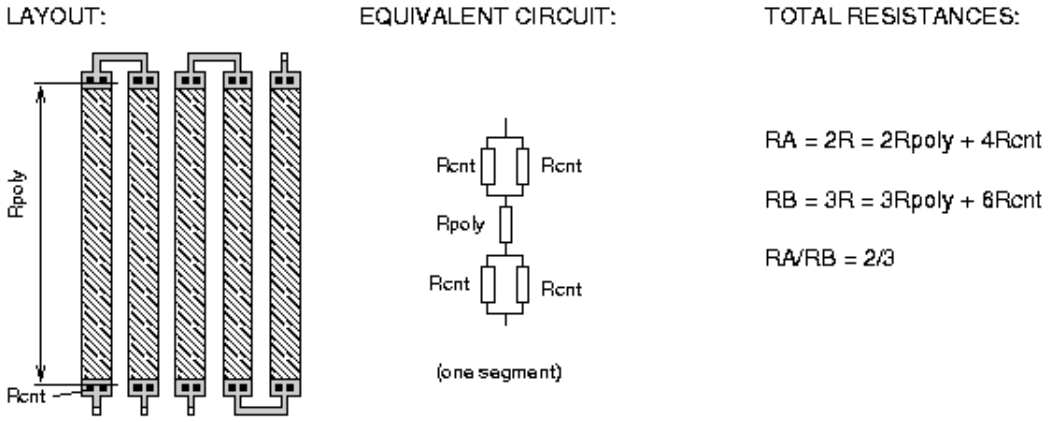
Resistor Contact Matching



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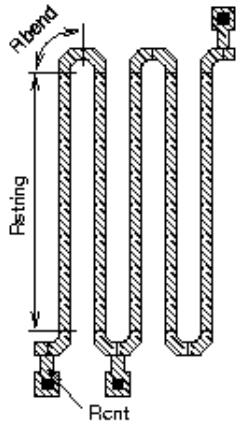
Resistor Bends Matching (Shape Matching)

LAYOUT:



EQUIVALENT CIRCUIT:

(one half-segment)

TOTAL RESISTANCES:

RA = 2R = 2Rstring + 4Rbend + 2Rcnt

RB = 3R = 3Rstring + 6Rbend + 2Rcnt

RA/RB ~ 2/3

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Last Update: March 16, 1998