Spring 2008

6.775 Midterm Project

Spring 2008

A Two Stage Telescopic Amplifier with two speed/power modes operating at 50ns & 200uW or 500ns & 20uW

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Design Methodology

Choice Topology:

Before designing the amplifier, a rough estimation of performance tradeoff is made between different amplifier topologies to help picking a suitable OTA. In the table below, we compared some key parameters that are relevant to our design: gain, swing, noise factor, design complexity, speed and power; for each parameter, we rank them in the order from best to worse. To achieve relatively high gain of 10k, a triple cascode, gain-boosted (GB), or two stage designs are picked for comparison. We eliminate the discussion on regular double cascade amplifier because to achieve the required gain, we need a Length of at least 1um. This would degrade our frequency response due to the high capacitance these transistors create.

Topology	Gain	Swing	n_f	Complexity	Speed	Power
Telescopic Triple Cascode	$(g_m \times r_o)^3$	V_{DD} - 7V*	1	3	3	1
Folded Triple Cascode	$(g_m \times r_o)^3$	V_{DD} - 6V*	2	4	4	2
Telescopic with GB	$(g_m \times r_o)^3$	V_{DD} - 5V*	3	5	1	~3
Folded Cascode with GB	$(g_m \times r_o)^3$	V_{DD} -4V*	4	6	2	~4
Two stage Telescopic	$(g_m \times r_o)^3$	V_{DD} - 2V*	~5	1	5	~3
Two stage Folded Cascode	$(g_m \times r_o)^3$	V_{DD} - 2V*	~6	2	6	~4

The objective for our projection is to design an amplifier with high speed, low power, high output swing, with a target given noise budget in 0.18um technology. Triple cascode is very difficult to design with a limited supply voltage of 1.8V at the given technology. It introduces more complexity in designing the biasing circuitry for the amplifier; the performance of the amplifier will also be more sensitive to the biasing voltage. Second, it provides very little output swing. Thus, we eliminate triple cascode as our consideration.

Two-stage amplifier is slower than a single stage gain boosting amplifier and it also introduces more noise. However, gain boosting (GB) topology is more complicated to design in terms of settling time, stability and noise. For GB topology, extra design care has to be made to ensure all the loops in the amplifier are stable. In addition, pole-zero doublets may be introduced that will cause slow settling time. Third, it is harder to come up with an analytical formula to describe the noise. Although two stage design posed a potential speed penalty, we decide that its benefit on lower complexity, high swing, and comparable noise power to other topologies overshadow the speed penalty. Moreover, with two stage topology it is easier to control the unity gain and second pole position to get the desired phase margin for optimal settling time.

The second stage of the two stage amplifier is chosen to be a common source topology for its high gain and high swing characters. A compensation capacitor is added to split the two poles to achieve good phase margin. A nulling transistor is added to cancel out the zero. The nulling transistor here cannot be implemented using a regular resistor because the two power modes requirement. By using a fixed resistor, it cannot track the transconductance of the second stage when switching from high power mode to low power mode to move the zero away. This could cause stability and can introduce more noise due to the increases in bandwidth from the low frequency zero.

PMOS is chosen for the first stage to improve the slew rate since for the same current, PMOS has lower transconductance and thus higher V* (V* = 2*Ids/gm) compared to NMOS. NMOS input stage is chosen for the second to improve input referred offset and the gain of the overall amplifier.

Specification

Supply Voltage	$V_{DD} := 1.8V$	
Temperature	$Temp := 273.15K + 27K$	
Capacitors	$C_L := 0.75pF$	Load
	$C_f := 0.5pF$	Feedback
	$C_{in} := 0.5pF$	input
Thermal Noise	$N_{budget} := 150 \cdot \mu V$	
Settling Time	$T_S := 50ns$	
Total Power Budget	$P_{tot} := 200 \cdot \mu W$	
Maximum Error	$\varepsilon_{tot} := 0.1\%$	
Minimum Gain	$A_{OL} := 10 \cdot 10^3$	
Boltzmann Constant	$k := 1.38 \cdot 10^{-23} \cdot \frac{m^2 \cdot kg}{s^2 K}$	

Design

Design Vdsat

$V_{dsat1} := 100 \cdot mV$	1st Input Pairs
$V_{dsat1c} := 100 \cdot mV$	1st Input Cascode
$V_{dsat2} := 150mV$	1st CS
$V_{dsat2c} := 100mV$	1st CS Cascode
$V_{dsatT1} := 300mV$	1st Tail CS
$V_{dsat3} := 150mV$	2rd Input
$V_{dsatT2} := 300mV$	2st Tail CS

Design Length

$L_1 := 0.25 \cdot \mu m$	1stTranssitor Length
$L_2 := 0.35 \cdot \mu m$	2rdTranssitor Length
$L_{tail} := 0.35 \mu m$	Tail CS Length

Why pick the design values above?

Ideally, we want to pick a V_{dsat} as small as possible to operate the device more efficiently and improve the output swing. However, by picking too small a V_{dsat} will push the device into subthreshold region, which will have a big speed penalty. In addition, in order to have reasonable noise factor, we cannot pick all the V_{dsat} to be minimum as we want to. To minimize noise factor, we want to have small V_{dsat} for the input devices and high V_{dsat} for the cascoded current source (CS). Therefore, we pick 100mV for input V_{dsat}, 150mV for the first stage CS, and 300mV for the second stage CS. We do not, however, pick a larger V_{dsat} for the first stage CS to reduce noise because its V_{dsat} has to match the V_{dsat} of the input of the second stage to minimize systematic offset. By increasing V_{dsat} of the CS for the first stage (equivalently increasing the V_{dsat} for the second stage input), we will increase the noise from the second stage.

The transistor length is chosen mainly for gain. For the first stage, the length of 0.25um gives us sufficient gain. The current mirror and the second stage length are chosen to be 0.35um because it gives us the optimal gain from simulation. With a bigger length for the current mirror, we can improve the current matching and better power supply rejection ratio.

The below design procedure highlights the design for the high power mode. Here, we are assuming that the lower power mode specification can be achieved by just decreasing the current by 10x. In general, this is a valid assumption. The gain will increase from high power mode to low power mode. The speed should decrease less than 10x because we are not fully limited by slew rate. The noise should be relatively constant because the capacitances are relatively constant.

Additional Values for design convenience

Guessing input cap C_{gs} to be about 10% of the feedback cap as a starting point. This will be revisited later as we get more accurate estimation on C_{gs}

Input Cap

$$C_{gs} := \frac{C_{in}}{10} = 5 \times 10^{-14} F$$

Feedback Factor

$$f := \frac{C_f}{C_f + C_{gs} + C_{in}} = 0.476$$

Closed Loop Gain

$$A_{CL} := -\frac{C_{in}}{C_f} = -1$$

Effective Cap looking at the Output

$$C_{Leff} := C_L + (1 - f) \cdot C_f = 1.012 \times 10^{-12} F$$

Maximum Current

$$I_{max} := \frac{P_{tot}}{V_{DD}} = 1.111 \times 10^{-4} A$$

Noise Analysis

Noise Factor

1st Stage

$$n_{f1} := 1 + \frac{V_{dsat1}}{V_{dsat2}} = 1.667$$

2rd Stage

$$n_{f2} := 1 + \frac{V_{dsat3}}{V_{dsatT2}} = 1.5$$

Total Input Noise Power with Unity Gain configuration

$$N_{tot}(C_c) := \frac{1}{f}\cdot\frac{k\cdot Temp}{C_c}\cdot\frac{1}{\left(1-\frac{f\cdot gm_1}{gm_3}\right)}\cdot\left[2\cdot n_{f1} + f\cdot\frac{C_c}{C_{Leff}}\cdot\left(1+\frac{gm_1}{gm_3}\right)\cdot n_{f2}\right]$$

Noise Voltage

$$N_{vol} := \sqrt{N_{tot}}$$

Assumption

$gm_1 = 0.5\cdot gm_3$ There are a couple of reasons for this assumption. First, from the noise equation above, we can see that by making gm_3 twice as big as gm_1, the noise can be lower. Second, we want to make the total current for the first and second stage to be about the same to improve slew rate (which means that the second stage input has twice the current going through compared to the first stage because the first stage current is sharing between the differential pairs). If assuming V_{dsat} to be the same, gm_3 will come out naturally to be twice of gm_1.

Given

$$N_{tot}(C_c) := \frac{k\cdot Temp}{C_c}\cdot\frac{1}{(1-0.5)}\cdot\left[2\cdot n_{f1} + \frac{C_c}{C_{Leff}}\cdot(1+0.5)\cdot n_{f2}\right]\cdot\frac{1}{1.8}$$

the **1.8** Factor is estimated from simulation

$N_{tot}(C_c) = N_{budget}^2$

$C_c := \text{Find}(C_c) = 1.251\times10^{-12}\,F$

$C_c := 1.4\cdot10^{-12}\cdot F$

We will set C_c to be a little bigger, 1.4pF, to compensate for the additional noise from other transistors, including the noise from the nulling transistor

Settling Error Analysis

Static Settling Error due to finite gain

$$\varepsilon_s := \frac{1}{A_{OL}\cdot f} = 2.1\times10^{-4}$$

Allowable Dynamic Error + 10% of design margin

$$\varepsilon_d := (\varepsilon_{tot} - \varepsilon_s)\cdot 110\% = 8.69\times10^{-4}$$

Steps @ each node

@ thesource of input $V_{s\_step} := 500mV$

@ the Output $V_{out\_step} := 500mV$

@ the input of the amplifier $V_{in\_step} := V_{out\_step}\cdot f = 0.238\,V$

Slew Rate

@ In $SR_{out}(I_{out1}) := \frac{I_{out1}}{C_c}$

@ Out $SR_{in}(I_{out1}) := SR_{out}(I_{out1})\cdot f$

Time during Slewing

$$t_{slew}(I_{out1}) := \frac{V_{in\_step} - V_{dsat1}}{SR_{in}(I_{out1})}$$

Time during linear Settling

$$t_{linear}(I_{out1}) := \frac{V_{dsat1}}{SR_{in}(I_{out1})}\cdot\ln\left(\frac{V_{dsat1}}{V_{in\_step}\cdot\varepsilon_d}\right)$$

Total Settling Time

$$t_{tot}(I_{out1}) := t_{slew}(I_{out1}) + t_{linear}(I_{out1})$$

Given

$I_{out1} := \frac{I_{max}}{2}$

$t_{tot}(I_{out1}) = T_S$

$I_{out1} := \text{Find}(I_{out1}) = 4.446\times10^{-5}\,A$

Transconductance Calculation

$$gm_1 := \frac{1}{2}\cdot\frac{2\cdot I_{out1}}{V_{dsat1}} = 4.446\times 10^{-4}\,\frac{1}{\Omega} \qquad gm_{1c} := \frac{1}{2}\cdot\frac{2\cdot I_{out1}}{V_{dsat1c}} = 4.446\times 10^{-4}\,\frac{1}{\Omega}$$

$$gm_2 := \frac{1}{2}\cdot\frac{2\cdot I_{out1}}{V_{dsat2}} = 2.964\times 10^{-4}\,\frac{1}{\Omega} \qquad gm_{2c} := \frac{1}{2}\cdot\frac{2\cdot I_{out1}}{V_{dsat2c}} = 4.446\times 10^{-4}\,\frac{1}{\Omega}$$

$$gm_3 := 2\cdot gm_1 = 8.892\times 10^{-4}\,\frac{1}{\Omega} \qquad I_{out2} := \frac{1}{2}\cdot gm_3\cdot V_{dsat3} = 6.669\times 10^{-5}\,A$$ The second stage current

$$gm_{1T} := \frac{2\cdot I_{out1}}{V_{dsatT1}} = 2.964\times 10^{-4}\,\frac{1}{\Omega} \qquad gm_{2T} := \frac{2\cdot I_{out2}}{V_{dsatT2}} = 4.446\times 10^{-4}\,\frac{1}{\Omega}$$

Total Power & Bandwidth $P_{real} := V_{DD}\cdot\left(I_{out1} + I_{out2}\right) = 2.001\times 10^{-4}\,W \qquad BW_u := \frac{f\cdot gm_1}{2\cdot\pi\, C_c} = 2.407\times 10^{7}\,\frac{1}{s}$

Second Pole Location

$$w_{p2} := \frac{1}{2\cdot\pi}\,\frac{gm_3\cdot C_c}{C_{Leff}\cdot C_{gs} + C_c\cdot\left(C_{gs} + C_{Leff}\right)} = 1.289\times 10^{8}\,\frac{1}{s} \qquad \frac{w_{p2}}{BW_u} = 5.355$$

Phase Margin $\operatorname{atan}(7.696)\cdot\frac{180}{\pi} = 82.597$

What we have done so far

The power is hitting the limit of 200uW; and we have too much of a phase margin. Having a lot of phase margin would actually hurt the settling time. Therefore, we will decrease the current of the second stage to push the second pole closer to the unity gain frequency to decrease the power consumption and phase margin.

After revising the output current for the second stage, we have the desired current and the V* for all the transistors in the amplifier. By generating a plot with I_{ds} vs. V* (V* = 2*I_{ds}/gm), the width of the transistors can be determined. We notice that in this technology, V* is very different from V_{dsat}. V_{dsat} is less predictable and has no physical meaning. Therefore, it is more desirable to design the amplifier in terms of V*. All of the above V_{dsat} refers to V*.

Design Summary

In the hand calculation, it is very difficult to predict the DC small signal gain and output swing. Therefore, we defer this by guessing the appropriate length first and check our results in simulation later. We begin working with the set of intial values that we calculate from above. After a few iterations, our amplifier's performance is summarized in the table below:
The paracmeters are listed in the order of descending priority as stated in the project specification. While meeting most of the most important specification, my amplifier does not meet the Input Common Mode Range and PSRR. For input common mode, both the high power and low power mode do not meet the specification on the lower end at 0.75V. Both power mode has the lower end of input common mode to be around 0.85V. For PSRR, the low power mode only has 42dB at 50kHz of rejection while the specification requires 50 dB at 50kHz.

Parameters	spec	High Power Mode	Low Power Mode
Settling H -> L	50ns/500ns	41.52ns	488.9ns
Settling L -> H	50ns/500ns	48.93ns	463.27ns
Power	200uW/20uW	199.6u	20u
DC Gain	10k	24k	48k
Noise	150uV	137uV	147uV
Output Swing	0.3 -> 1.5	0.15 -> 1.58	0.12 -> 1.7
Phase Margin	50°	67.75°	78.21°
Input Common Mode	0.9 ± 0.15V	0.85 -> 1.05	0.85 -> 1.05
PSRR	65dB DC, 50dB 50KHz	94dB, 63dB	105dB, 42dB
CMRR	65dB	89dB	99dB

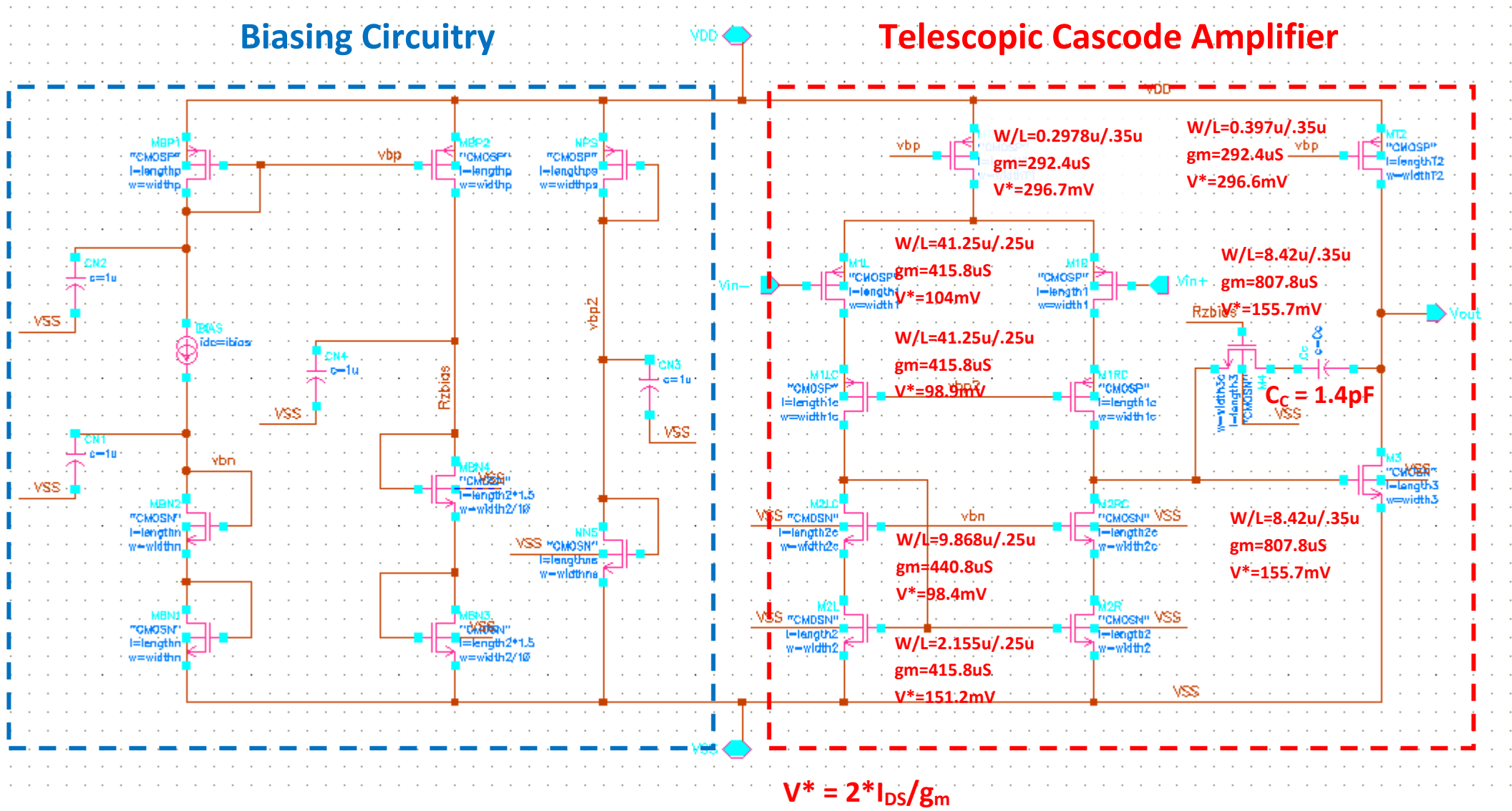
Design Studies and Conclusion

A two stage telescopic amplifier with double speed and power modes are designed using a 0.18um technology. In the high power mode, it is consuming 200uW with a settling time of 500ns; in the low power mode, it is consuming 20uW with settling time of 50ns. All the specification are met except and low common mode range at high and low power mode and the PSRR at 50 KHz in the low power mode.

There are some key design insides that I find through the designing process that I would like to share and discuss below. I separate them into three sections: noise, slew rate, and settling time.

1. Slew Rate:
    a. In order to ensure what is limiting the amplifier settling time during simulation, we have to make sure if our amplifier is slew rate limited or not. The best way to figure this out is by putting in a step that is much smaller than V* and look at the settling time at the output. If not meeting the specification with a small step, it means the designer has to increase the closed-loop bandwidth of the amplifier (usually means burning more power).
    b. Designing a differential input and single-ended output amplifier means the amplifier will have asymmetric output settling behavior due to slew rate. It is important to realize what transition is limited by slew rate and how to design to avoid slewing.
    c. For power limited two-stage OP-amp design, designers are almost force to split the maximum allowable current equally between the two stages to avoid slewing. For example, in our design, the maximum allowable current is 111uA with 1.8V supply voltage. By allocating 10uA for the biasing circuitry, the remaining is split with 4.5:5.5 between the first stage and the second stage.
        i. H → L transition at the output is usually not slew rate limited
        ii. L → H transition requires the second stage current to be comparable to the first stage current; otherwise, the input transistor for the second stage will be completely turned off at the beginning of the step response and result in really slow settling behavior. In addition, in order to push the second pole to be beyond the unity gain frequency. It also requires the current (or gm) for the second stage to be comparable to the first stage.
2. Noise:
    a. It is hard to get an accurate noise hand calculation.
        i. The exact shape of the closed loop transfer function is hard to predict because there are extra poles after the non-dominate poles and there is a zero created by the compensation feedback capacitor.
        ii. We have to be careful on designing the nulling transistors. We can definitely not use a physical resistor in place of the nulling transistor because we need the track the location of 1/gm of the input transistor of the second stage to push the zero out to high frequency. If using a resistor in place of a nulling transistor, the zero can be at low frequency when switching from high to low power mode and increase the noise by 30% (from simulation).
        iii. It is important to design the gate biasing for the nulling resistor to track 1/gm of the input of the second stage.
    b. Output is not taken differentially; therefore, the biasing circuitry can introduce noise at the second stage of the amplifier. I put some big capacitors on the biasing circuitry to cancel out the noise.
3. Settling time:
    a. The biasing voltage on the cascode transistor influences the settling time (mostly because of different slew rate behavior).

Overall Schematics



$V^* = 2*I_{DS}/g_m$

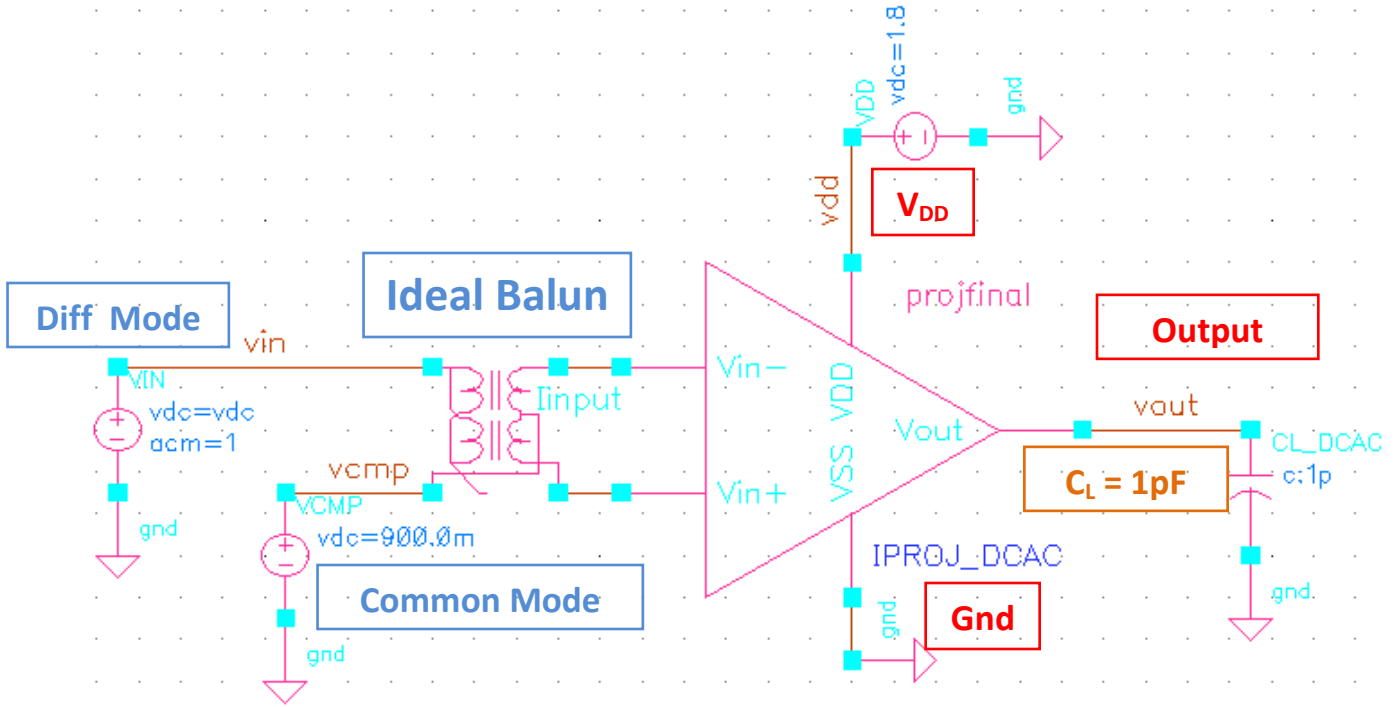
Schematic I

DC Analysis:

2. Power Consumption
3. DC Small Signal Gain
5. Output Swing
7. Common Mode Range

AC Analysis:

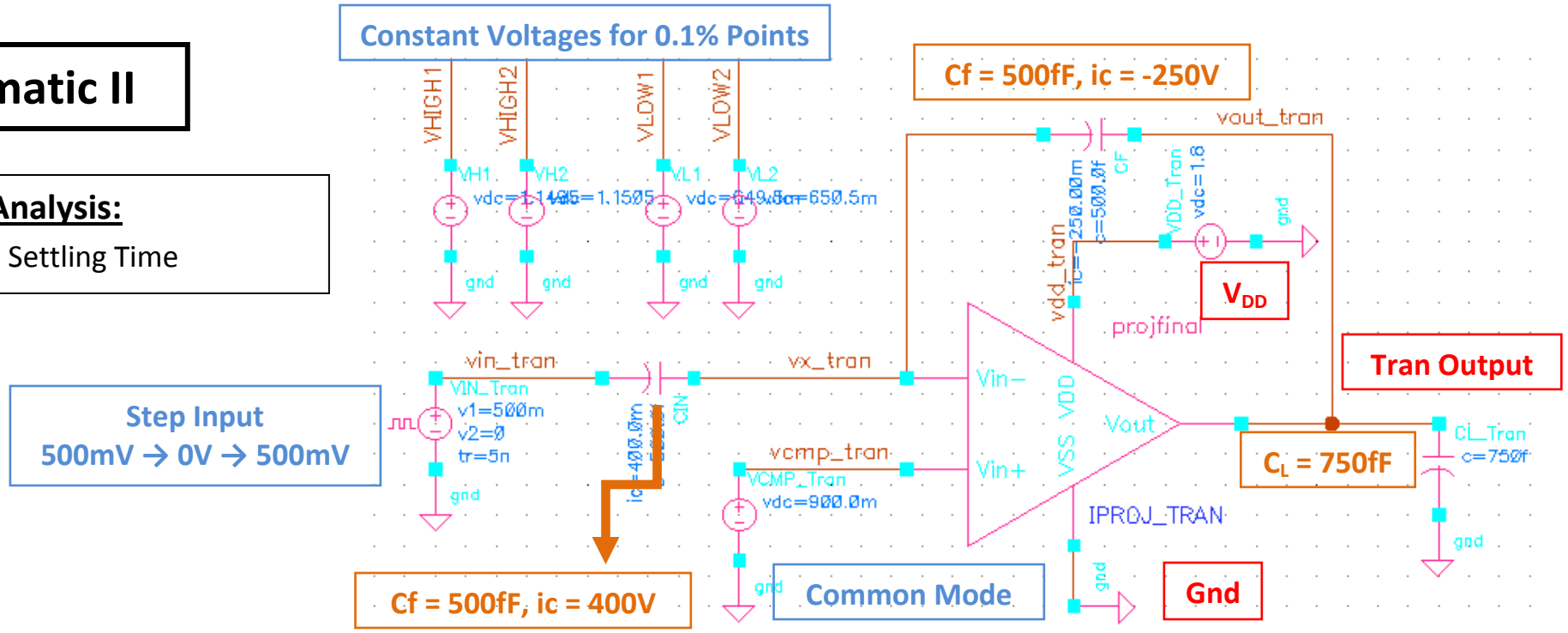
6. Phase Margin
8. PSRR (from V_{DD})
9. CMRR at DC



Schematic II

TRAN Analysis:

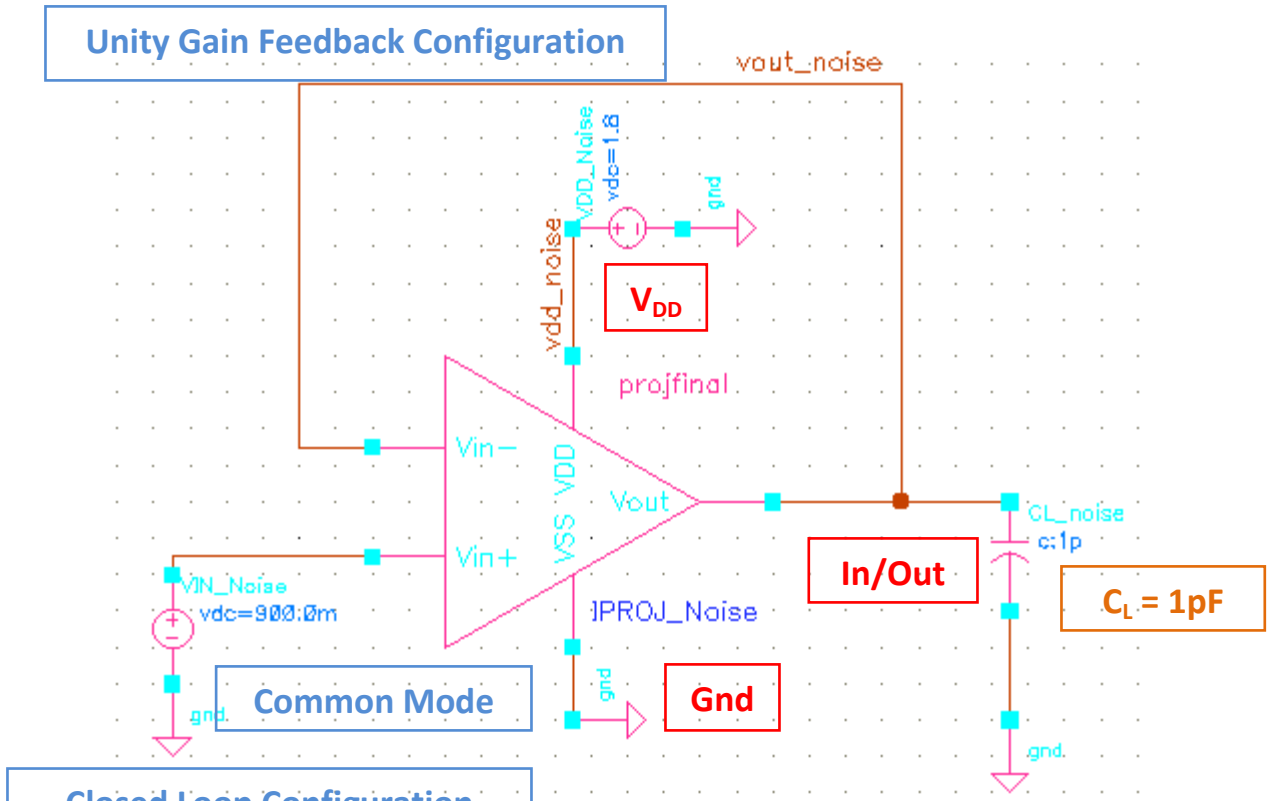
1. Settling Time



Schematic III

NOISE Analysis:

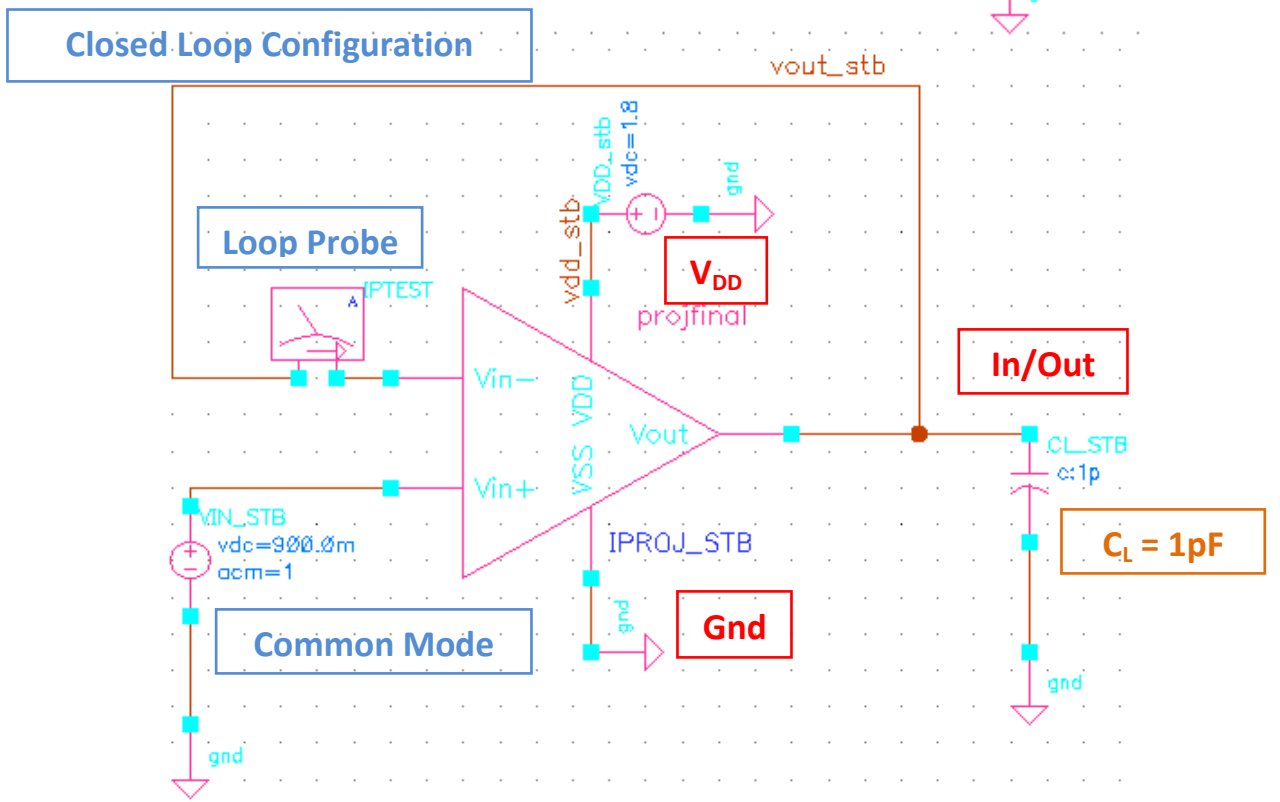
4. Thermal Noise < 150uV, in-band, input referred, unity-gain configuration



Schematic IV

Stability Analysis:

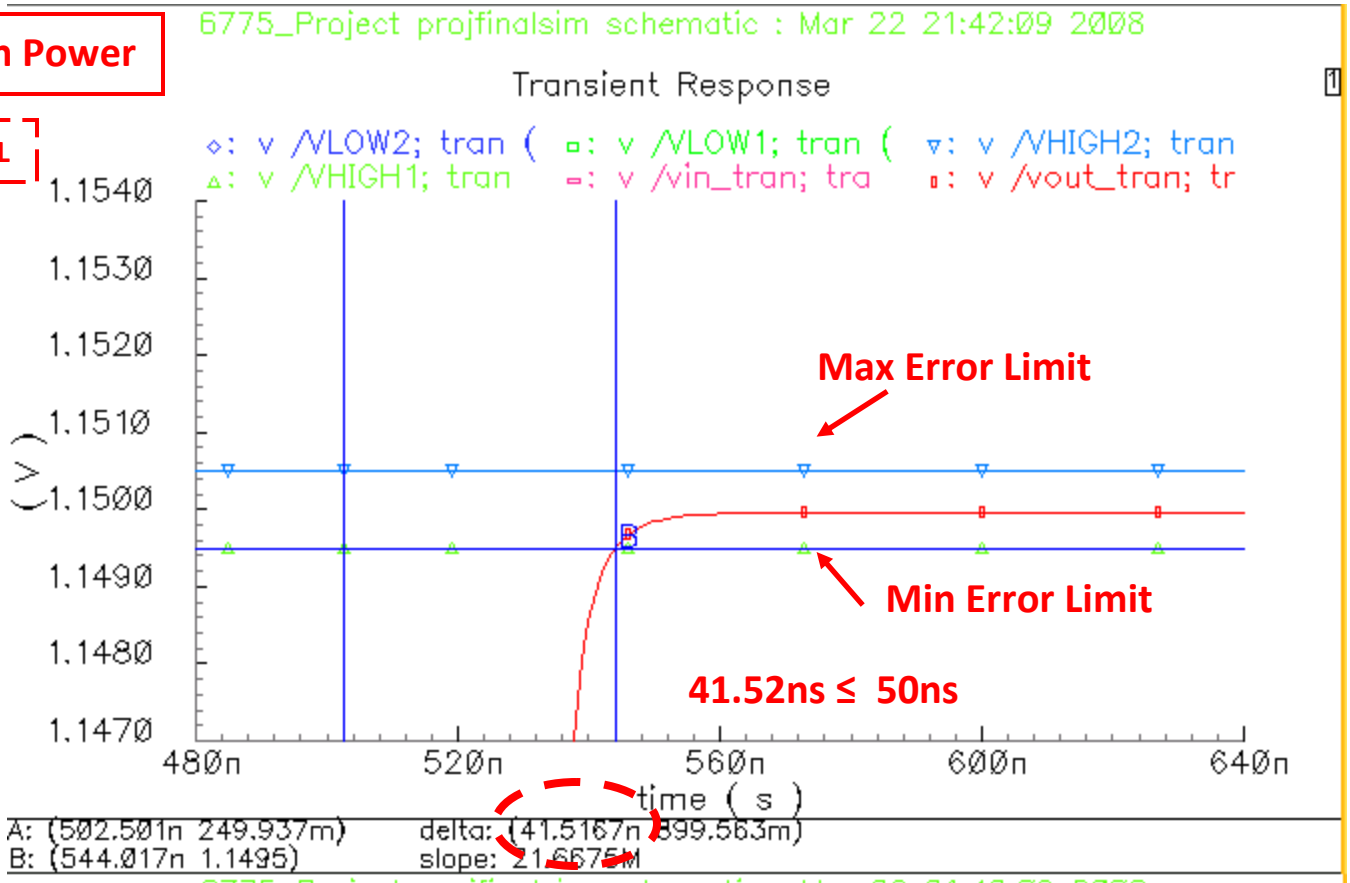
Closed Loop Stability Test



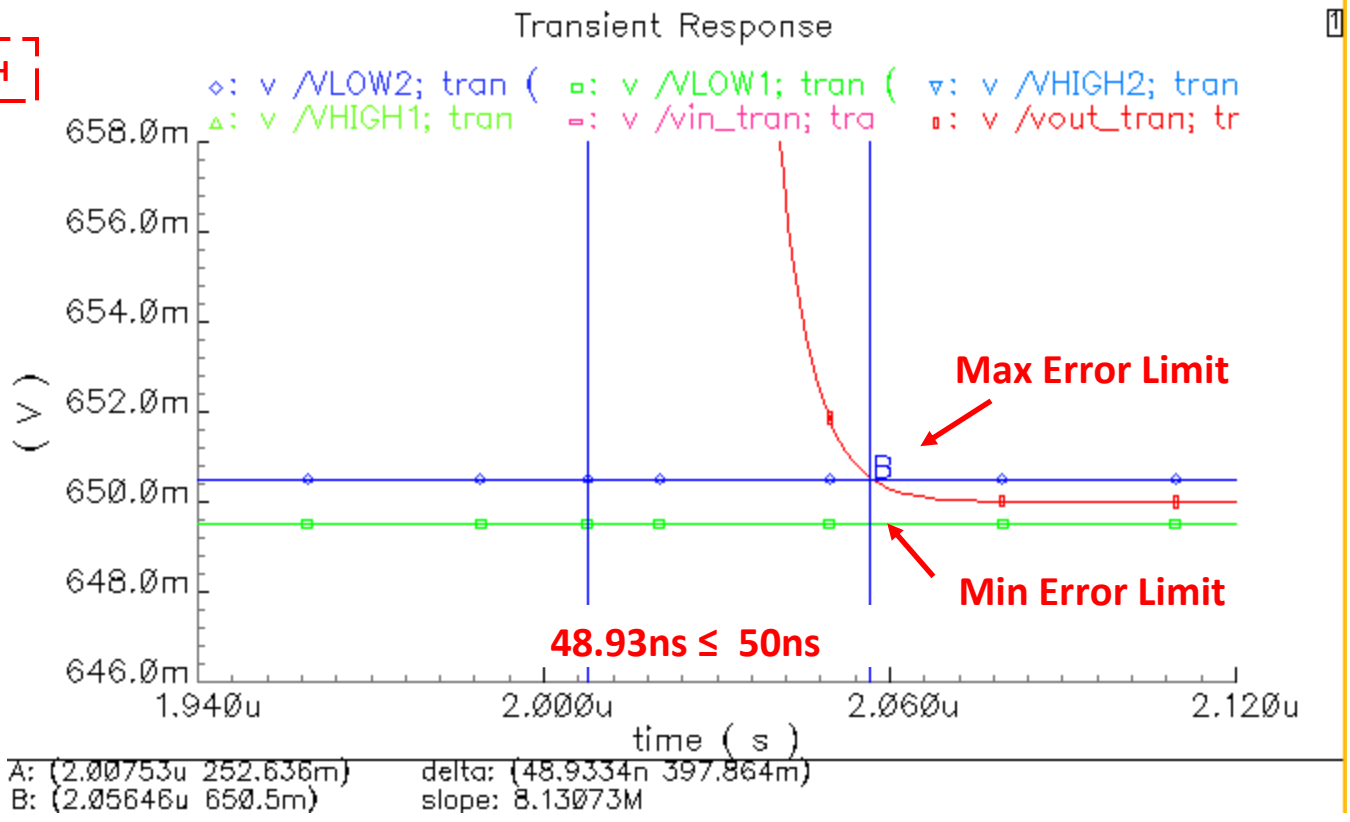
Settling Time

High Power

H → L

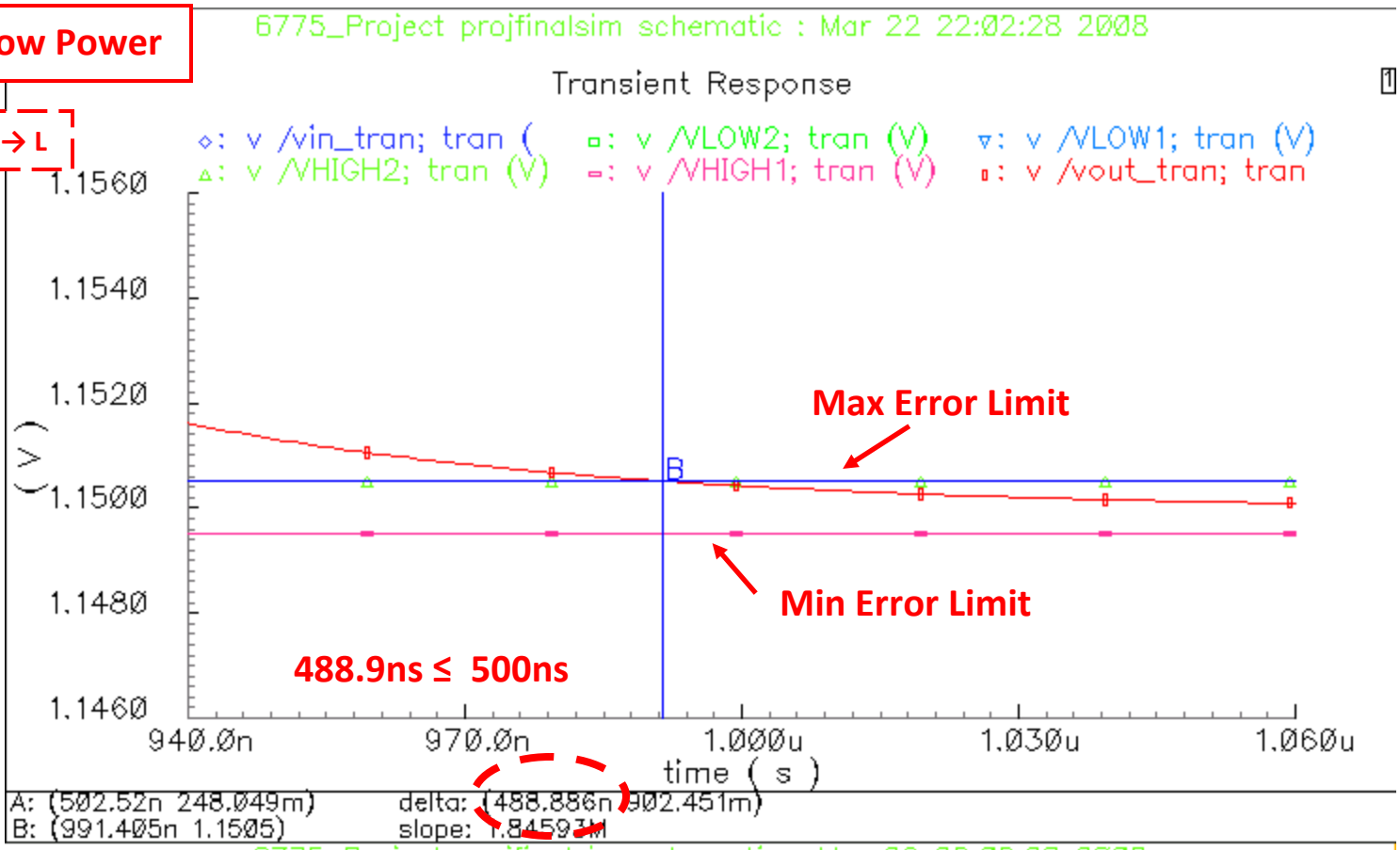


L → H

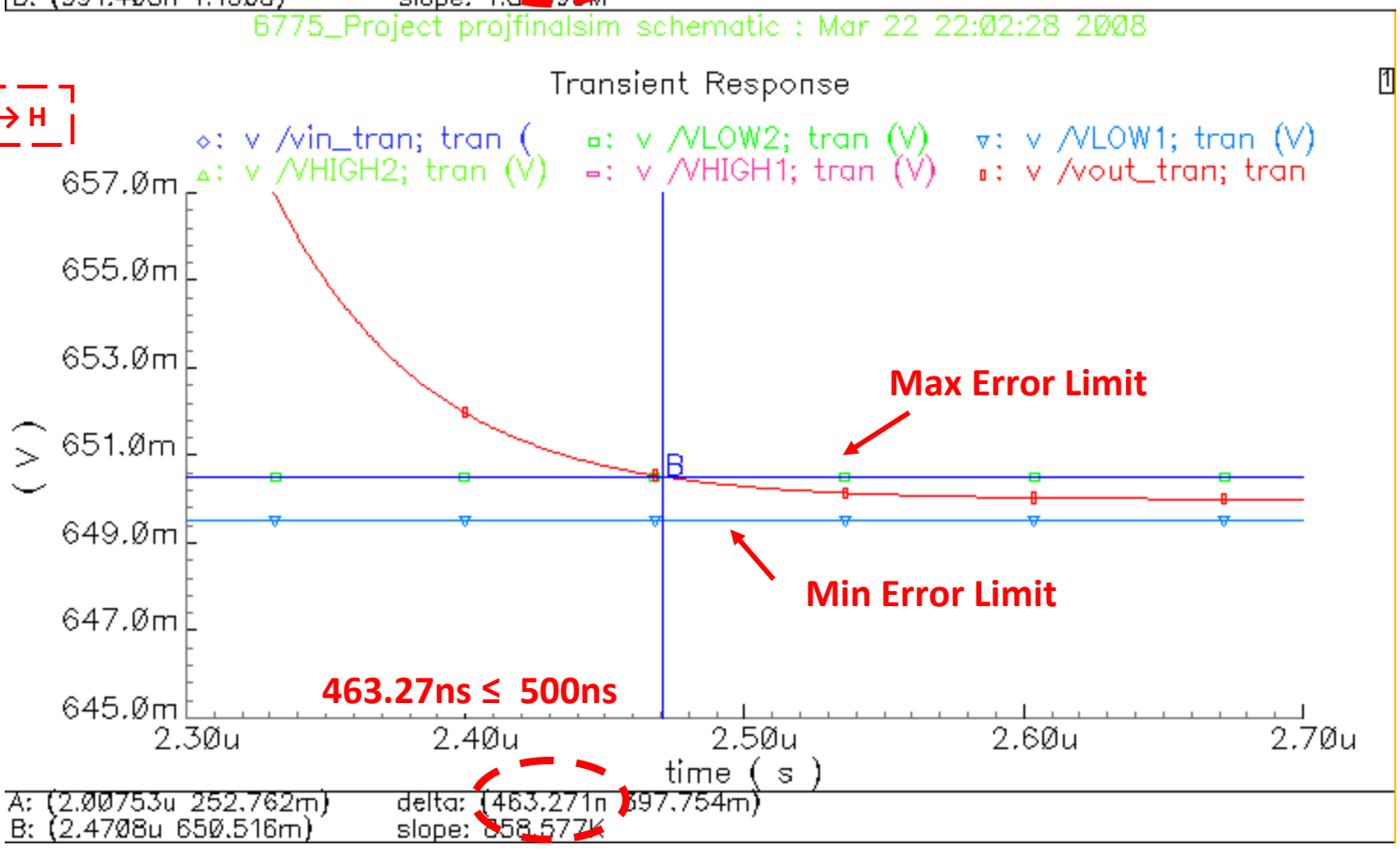


Low Power

H → L

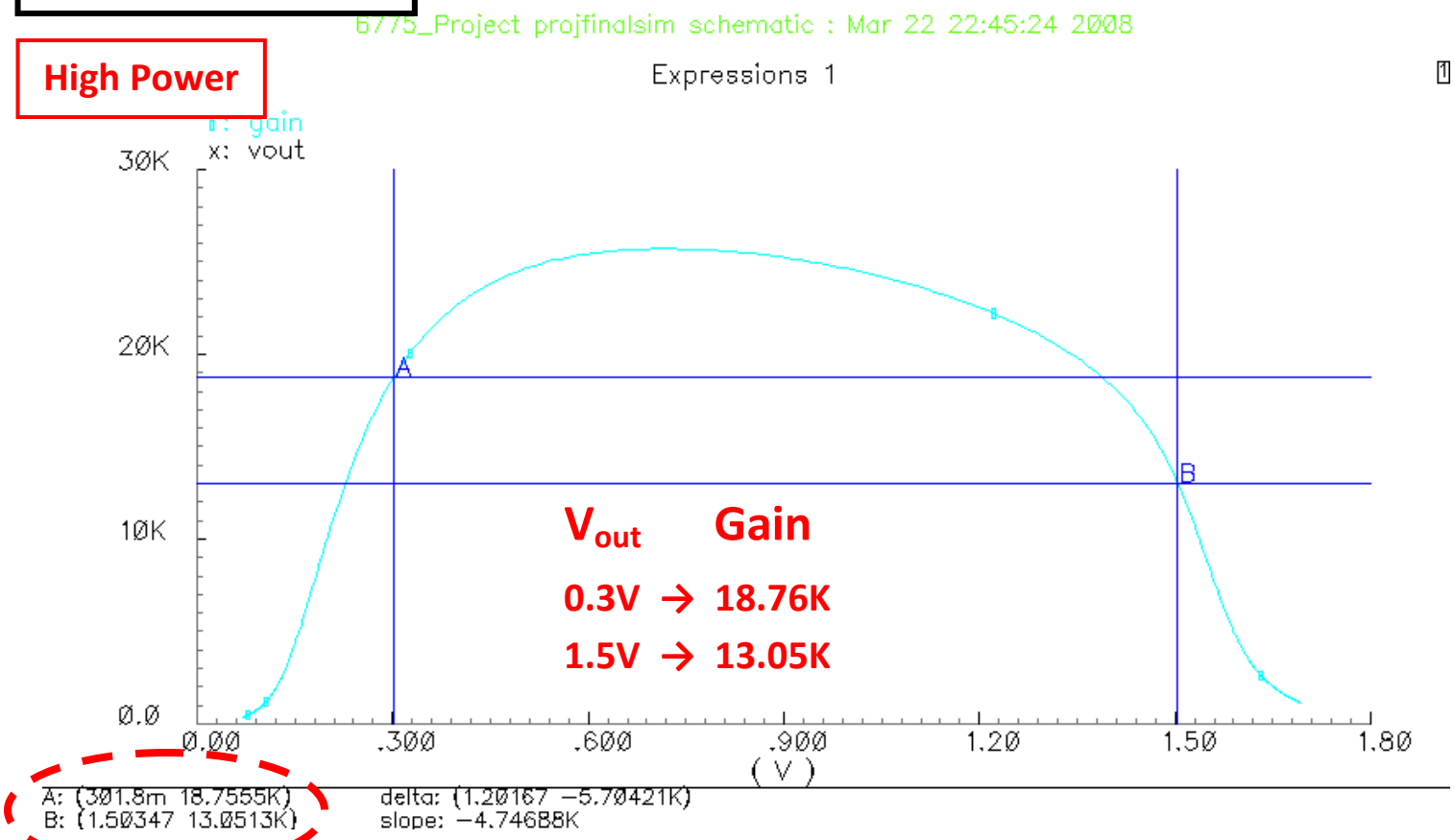


L → H



Output Swing

High Power

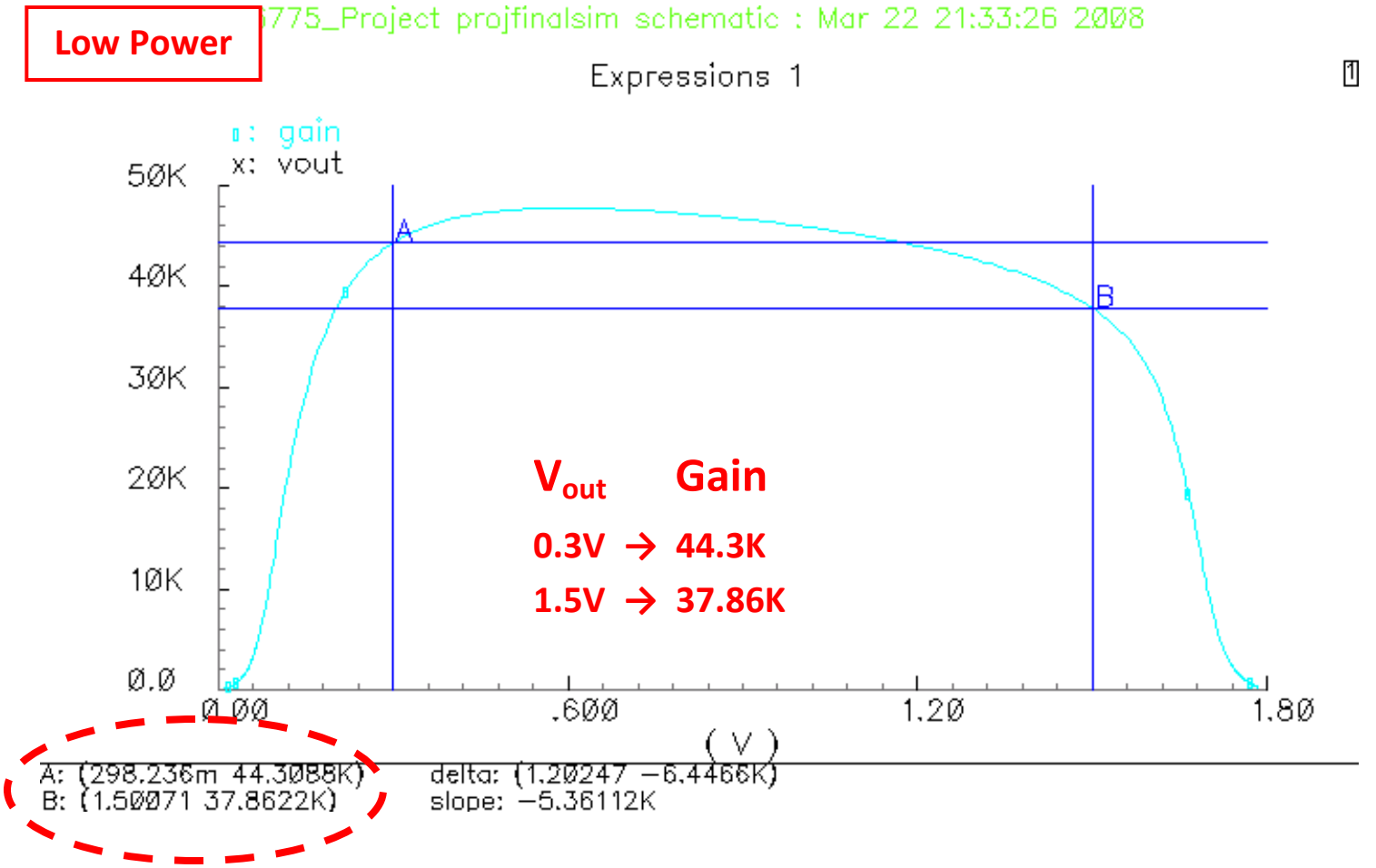


V_{out} Gain

0.3V → 18.76K

1.5V → 13.05K

Low Power



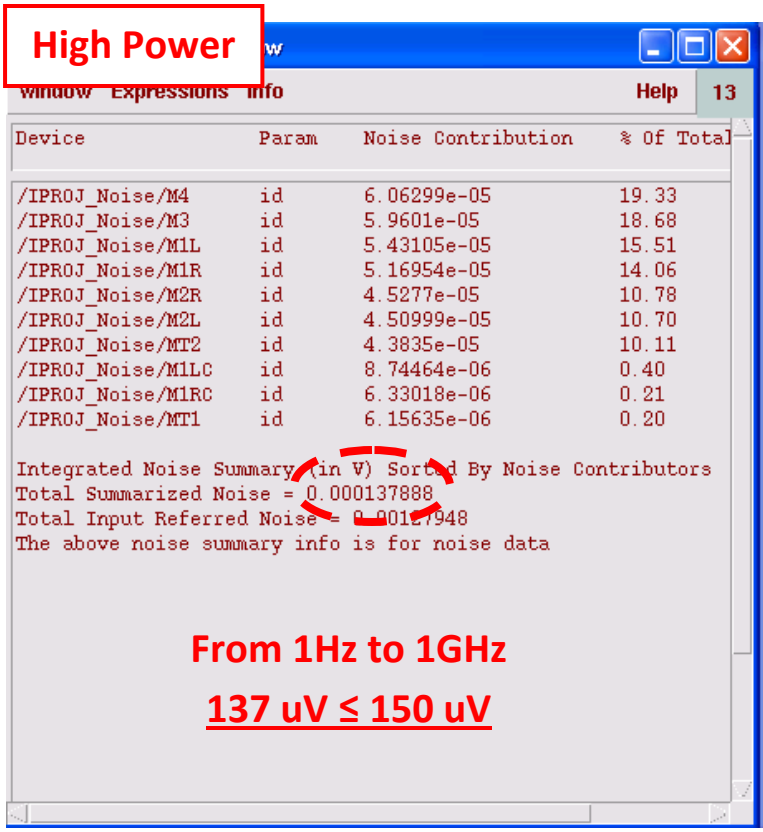
V_{out} Gain

0.3V → 44.3K

1.5V → 37.86K

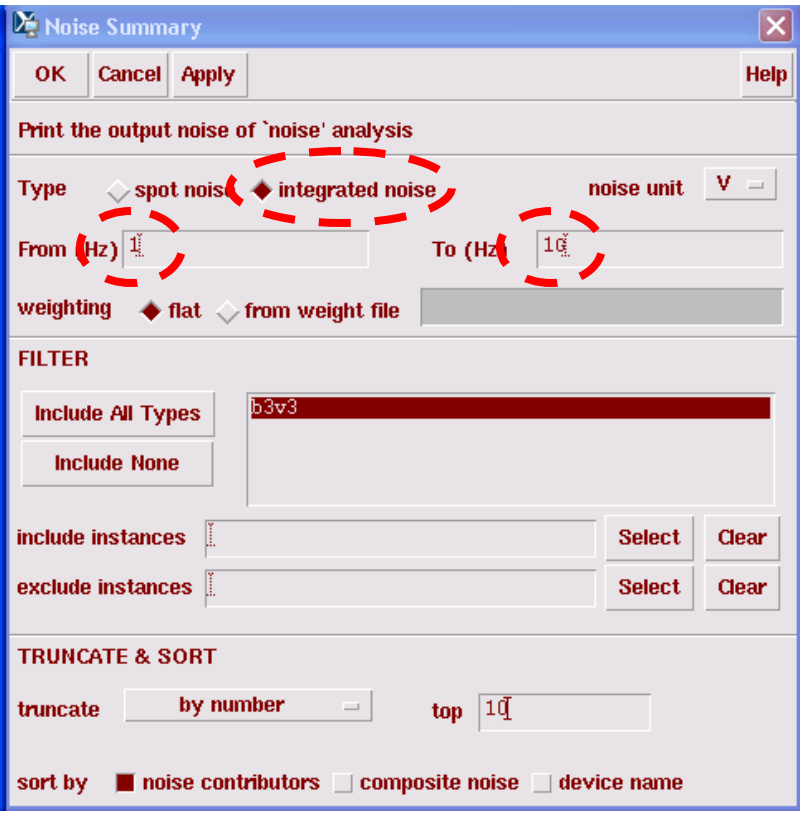
Noise

High Power

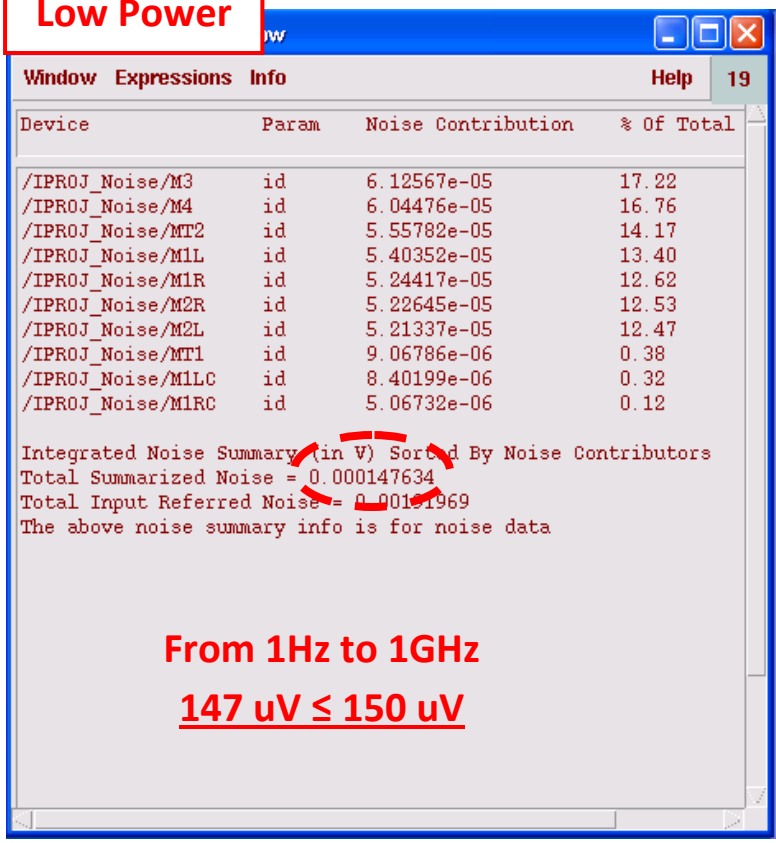


From 1Hz to 1GHz

137 uV ≤ 150 uV

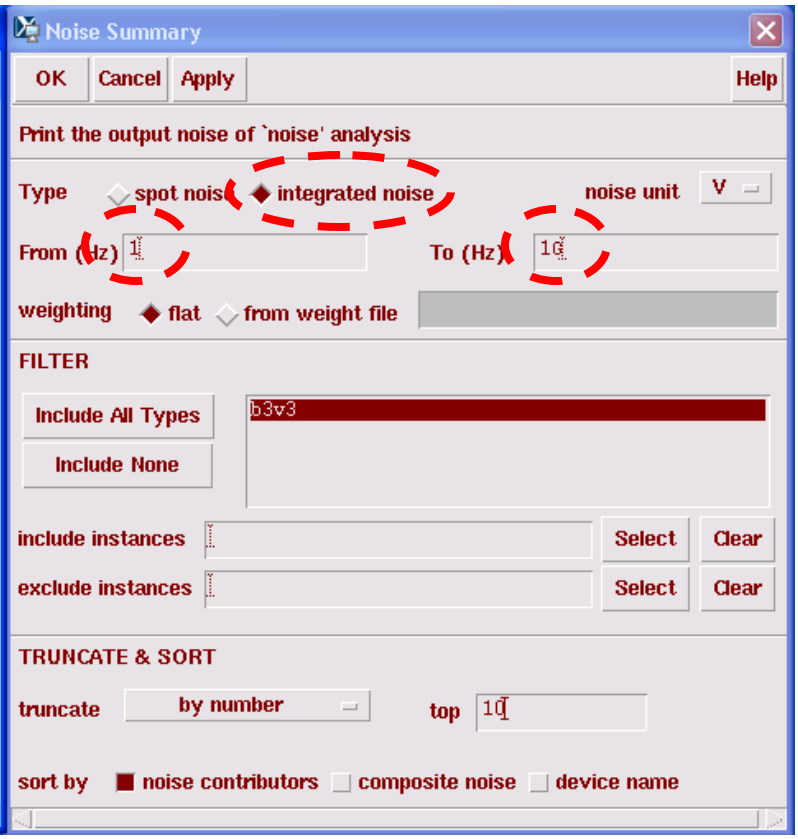


Low Power



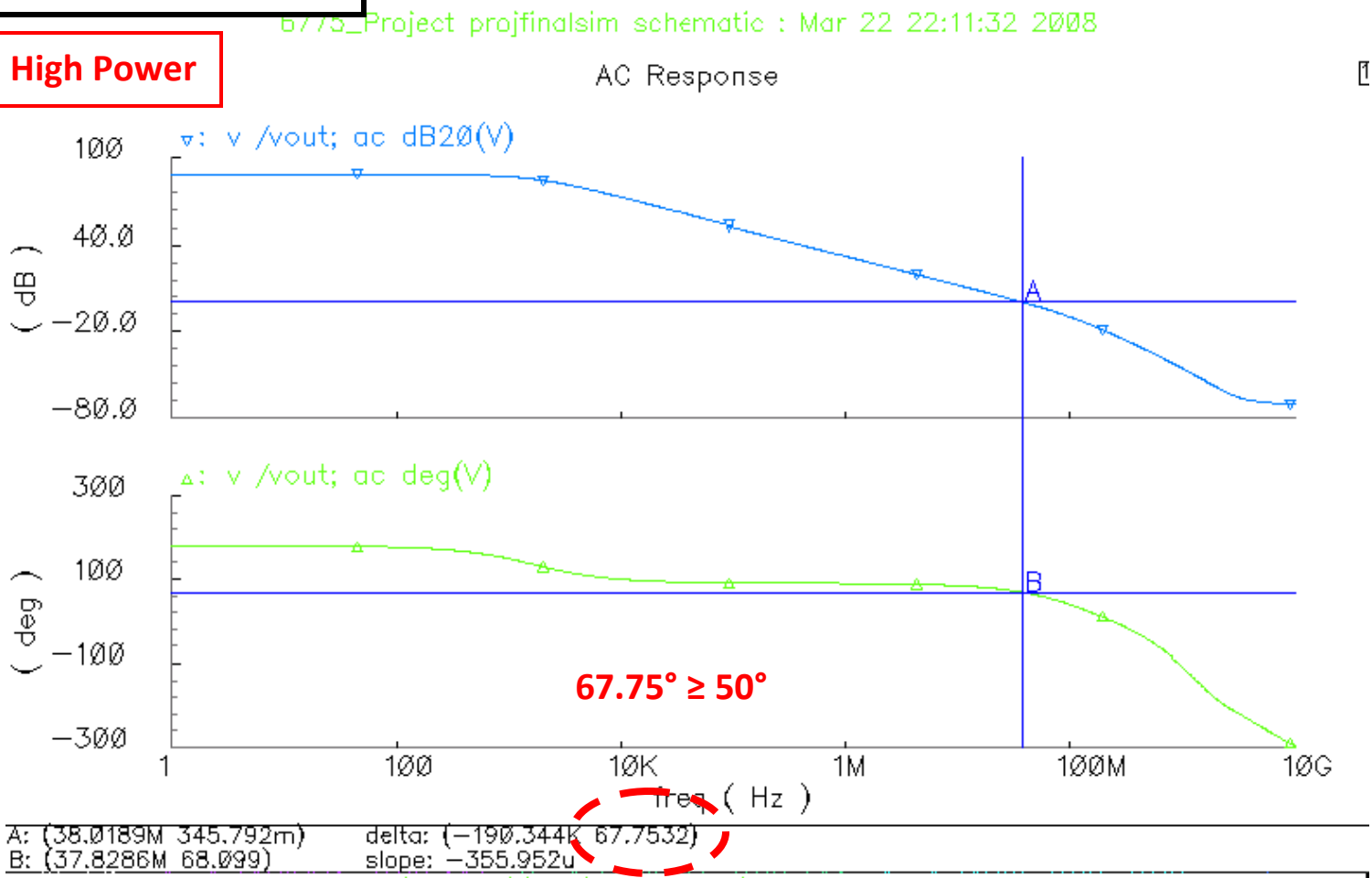
From 1Hz to 1GHz

147 uV ≤ 150 uV

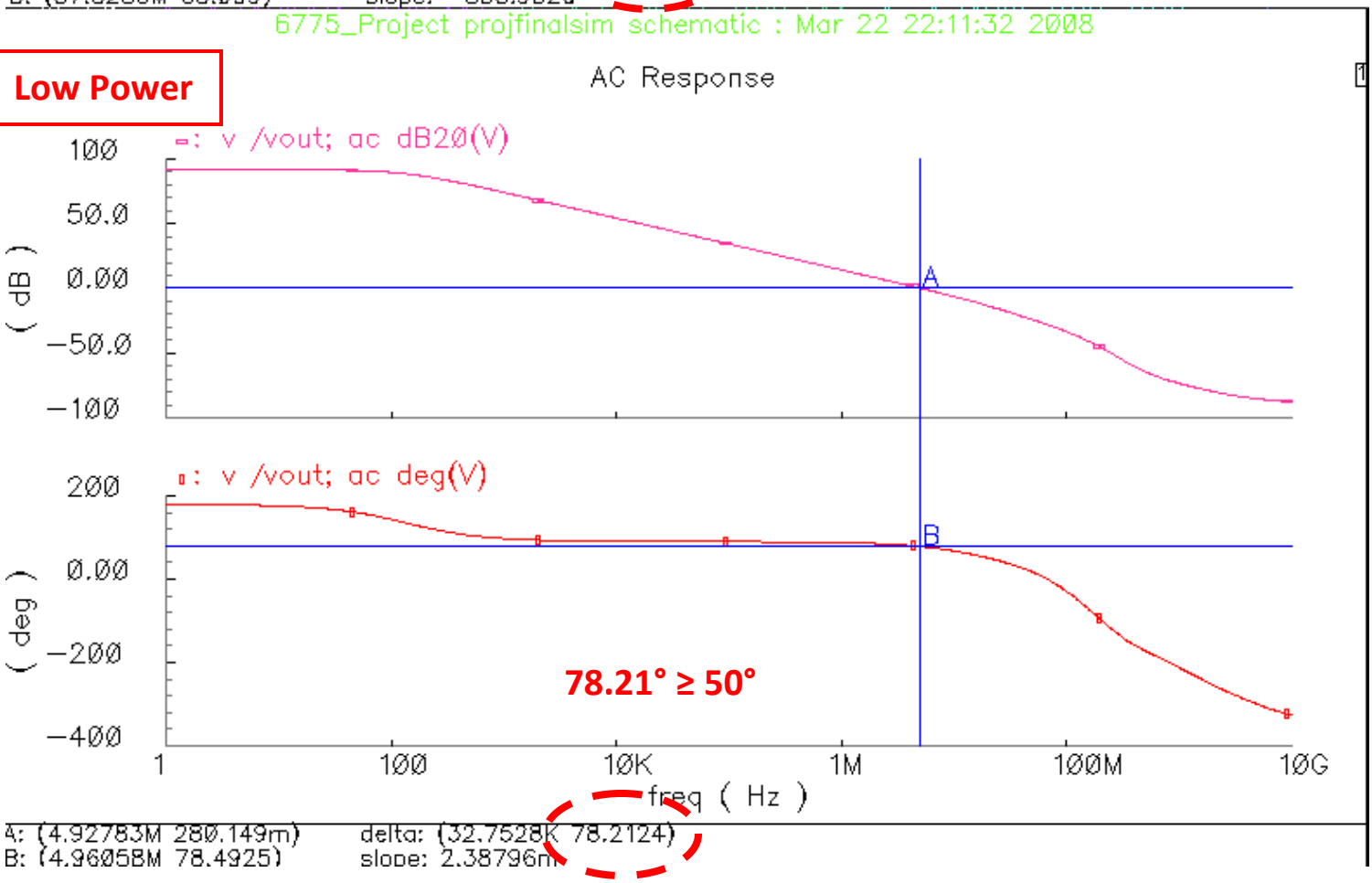


Phase Margin

High Power

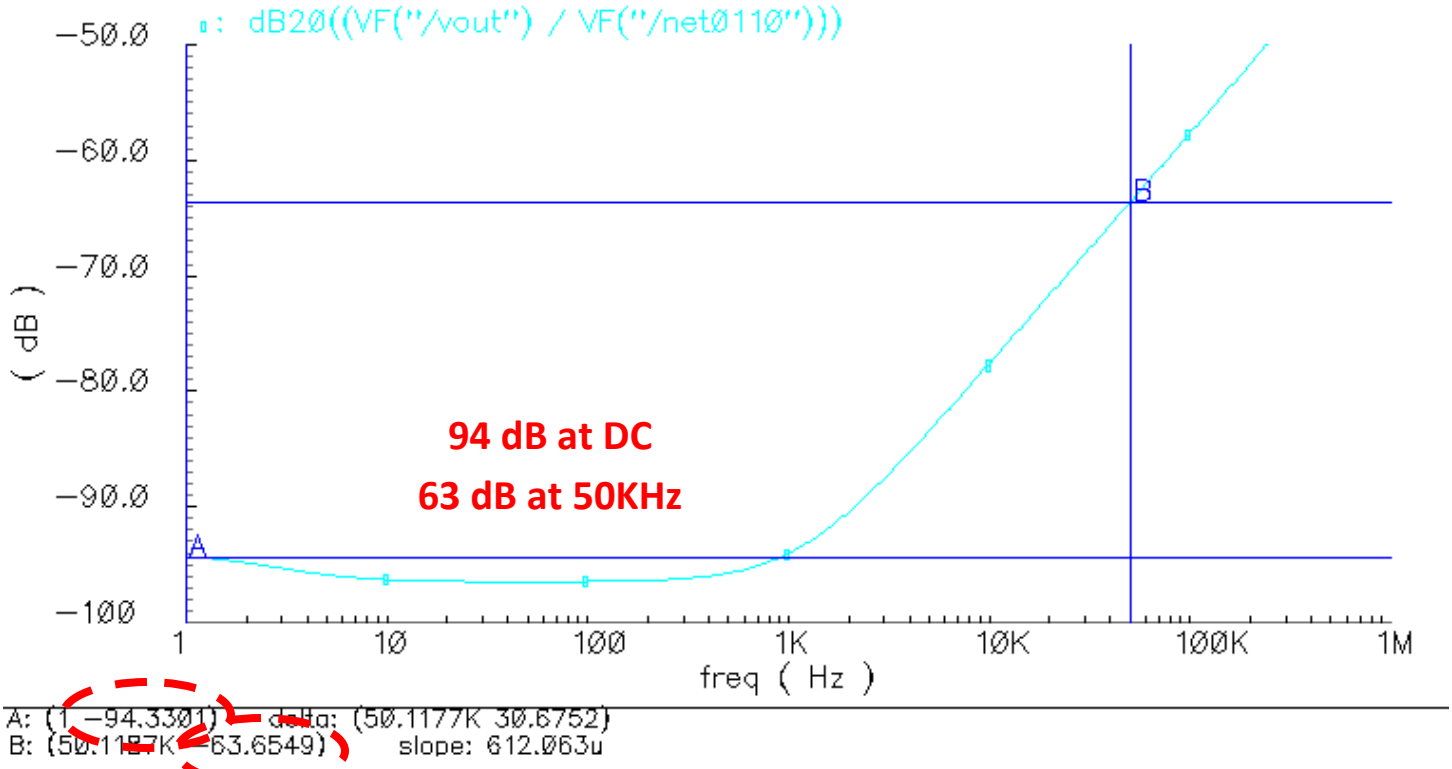


Low Power

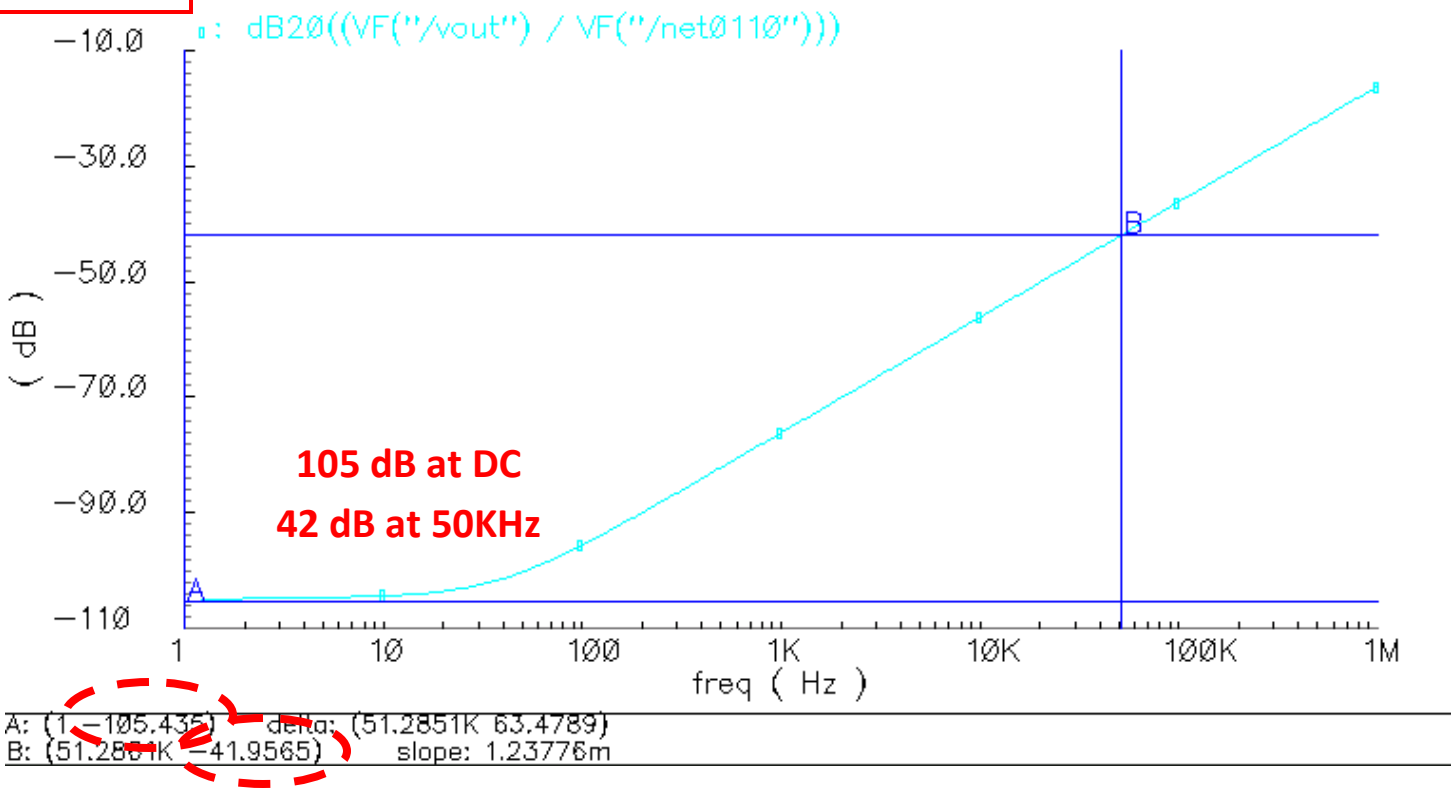


PSRR

High Power

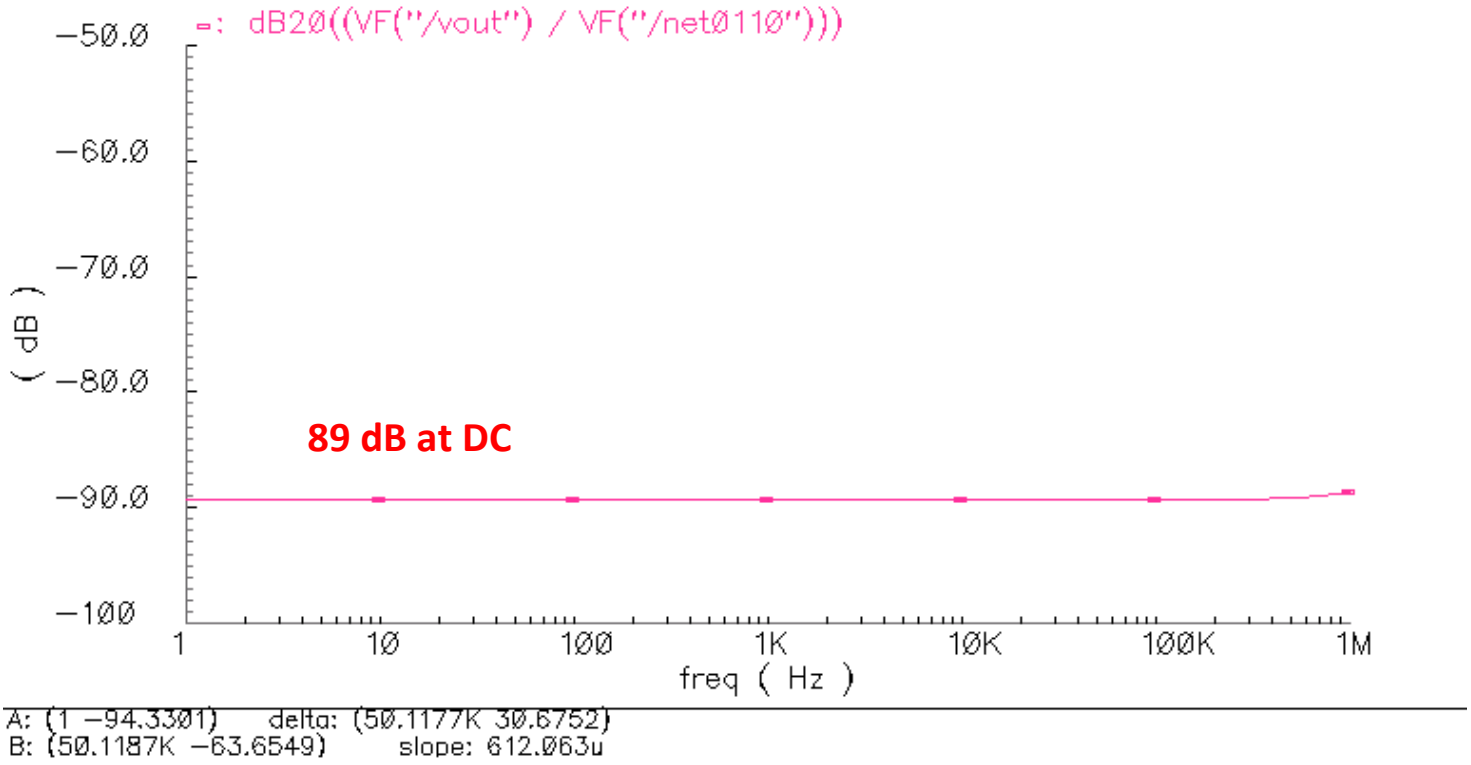


Low Power



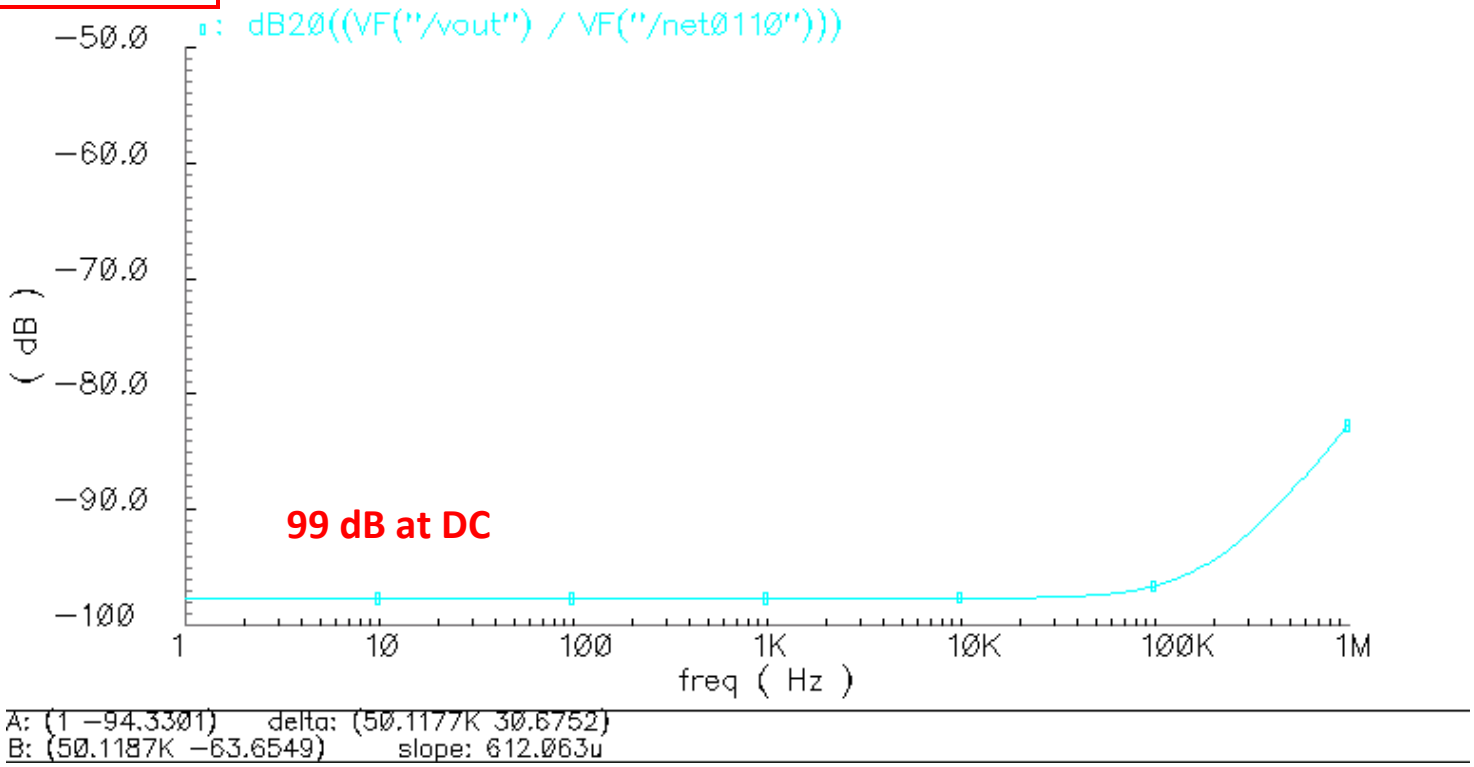
CMRR

High Power



A: (1 −94.3301) delta: (50.1177K 30.6752)
B: (50.1187K −63.6549) slope: 612.063u

Low Power

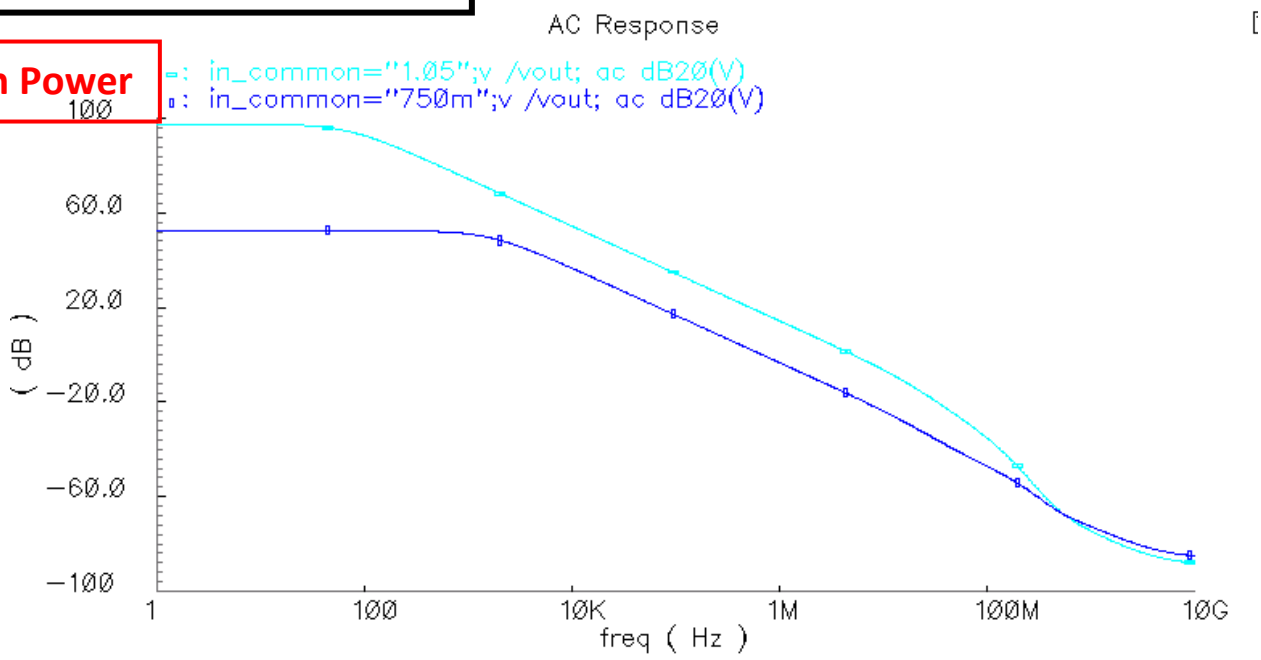


A: (1 −94.3301) delta: (50.1177K 30.6752)
B: (50.1187K −63.6549) slope: 612.063u

Input Common Mode

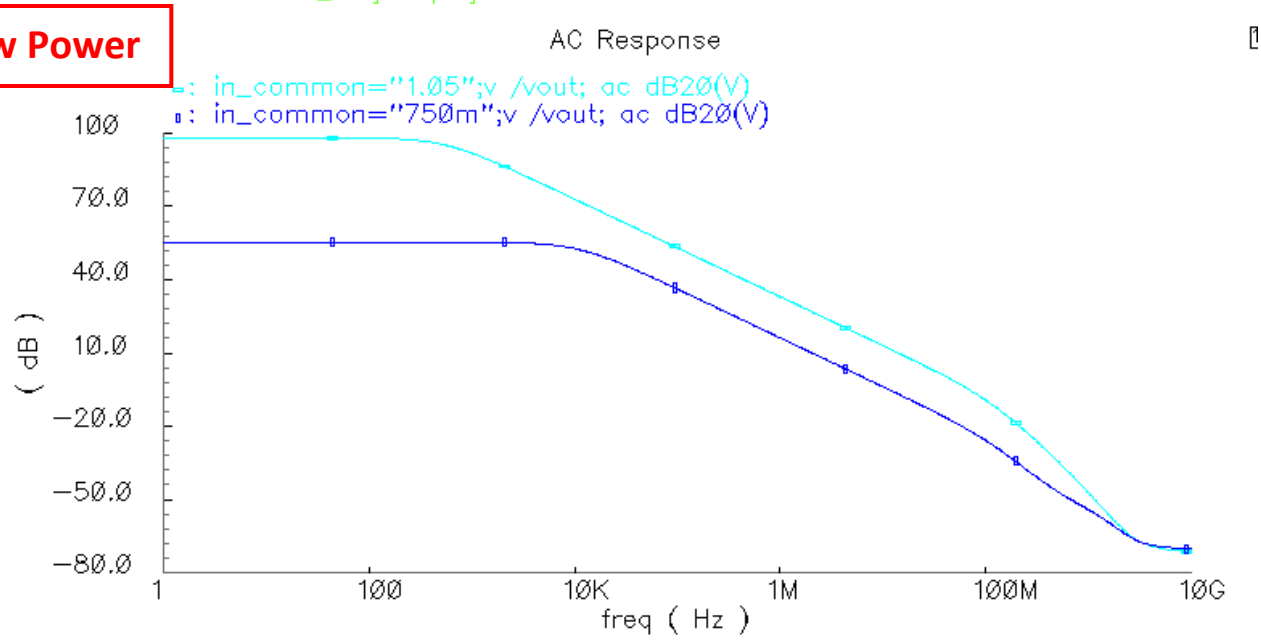
finalsim schematic : Mar 23 10:01:00 2008

High Power



6775_Project projfinalsim schematic : Mar 23 10:03:07 2008

Low Power



Power

Outputs

#	Name/Signal/Expr	Value	Plot	Save	March
1	gain		yes		
2	vout	550.6m			
3	power	199.6u			

High Power

Outputs

#	Name/Signal/Expr	Value	Plot	Save	March
1	gain		yes		
2	vout	266.9m			
3	power	20.01u			

Low Power