Chapter 6

OPERATIONAL AMPLIFIERS

6.1 Ideal Op Amps

6.1.1 Model

As we have learned earlier, any amplifier can be modelled as an equivalent two-port network shown in Fig. 6.1.

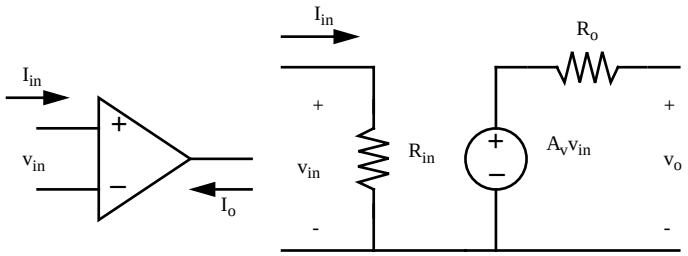

Fig. 6.1 Two-port equivalent circuit of a n operational amplifier

For an ideal op amp, we would like to have and thus can assume that:

$$A_v = \infty \tag{6.1}$$

$$R_{in} = \infty \tag{6.2}$$

$$R_o = 0 \tag{6.3}$$

$$V_{in} = 0 \tag{6.4}$$

$$I_{in} = 0 \tag{6.5}$$

6.1.2 Application

6.1.2.1 Inverting Amplifier

For the inverting amplifier shown in Fig. 6.2, apply the ideal equations listed above to get:

$$I_{R_1} = I_{R_2} = \frac{V_{in}}{R_1} = -\frac{V_o}{R_2} \tag{6.6}$$

Therefore,

$$V_o = -\frac{R_2}{R_1} V_{in} \tag{6.7}$$

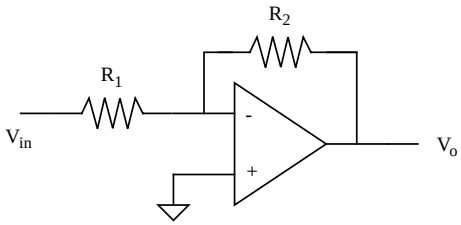

Fig. 6.2 An inverting amplifier using an ideal op amp

6.1.2.2 Non-Inverting Amplifier

For the non-inverting amplifier shown in Fig. 6.3, with the input current being zero, the output voltage can be found by voltage divider.

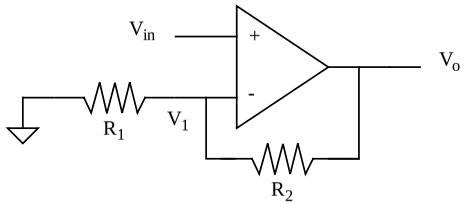

Fig. 6.3 A non- inverting amplifier using an ideal op amp

$$V_{in} = V_1 = \frac{R_1}{R_1 + R_2} V_o \tag{6.8}$$

Therefore,

$$V_o = \left(1 + \frac{R_2}{R_1}\right) V_{in} \tag{6.9}$$

6.1.2.3 Difference Amplifier

Figure 6.4 shows an implementation of a difference amplifier. Assume the op amp is ideal, we get:

$$V_x = V_y = \frac{R_2}{R_1 + R_2} V_{i1} \tag{6.10}$$

$$\frac{V_y - V_{i2}}{R_1} = \frac{V_o - Vy}{R_2} \tag{6.11}$$

Therefore,

$$V_o = R_2\left[\left(\frac{1}{R_1} + \frac{1}{R_2}\right)V_y - \frac{V_{i2}}{R_1}\right] = \frac{R_2}{R_1}(V_{i1} - V_{i2}) \tag{6.12}$$

Alternatively, the output voltage can be found by superimposition as below:

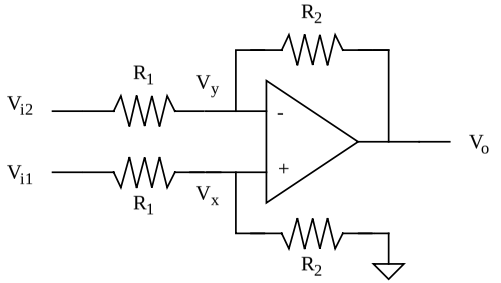

Fig. 6.4 A difference amplifier using an ideal op amp

a) Set $V_{i1} = 0$, the amplifier is an inverting amplifier with $V_{in} = V_{i2}$, and therefore:

$$V_{o_1} = \frac{R_2}{R_1}(-V_{i_2}) \tag{6.13}$$

b) Set $V_{i2} = 0$, the amplifier is a non-inverting amplifier with $V_{in} = V_x$, and therefore:

$$V_{o_2} = \left[1 + \frac{R_2}{R_1}\right]V_x = \left[1 + \frac{R_2}{R_1}\right]\left[\frac{R_2}{R_1 + R_2}\right]V_{i_1} = \frac{R_2}{R_1}V_{i_1} \tag{6.14}$$

c) By principle of superimposition, the output voltage is given by

$$V_o = V_{o_1} + V_{o_2} = \frac{R_2}{R_1}(V_{i1} - V_{i2}) \tag{6.15}$$

6.1.2.4 Integrator

Operational amplifiers are also popular in non-linear applications. As an example, an integrator can be implemented as shown in Fig. 6.5. Again, using characteristic equations for an ideal op amp, we can easily obtain:

$$I_C = C\frac{d}{dt}(-V_o) = \frac{V_{in}}{R} \tag{6.16}$$

It follows that

$$V_o(t) = -\frac{1}{RC}\int_0^t V_{in}(t)dt + V_o(t=0) \qquad (6.17)$$

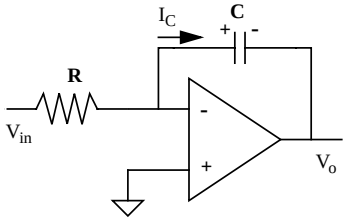

Fig. 6.5 An implementation of an integrator using an ideal op amp

6.2 Case Study

As a case study, let us do a complete analysis on a real commercial product, 741 op amp, whose complete schematic and simplified schematic are shown in Figs. 6.6 and 6.7, respectively.

6.2.1 Qualitative Description

6.2.1.1 Input Stage

The input stage consists of transistors Q_1 - Q_6 and has the following features:

a) High input resistance and high output resistance

b) Level shift to achieve large output swing

c) Differential-to-single-ended conversion

d) Protection of Q_1 and Q_2 from junction breakdown by series connection with Q_3 and Q_4

6.2.1.2 Gain Stage

The transistors Q_{16}, Q_{17}, and Q_{13B} form the gain stage, which has:

a) High input resistance and thus minimum loading effect

b) Large voltage gain

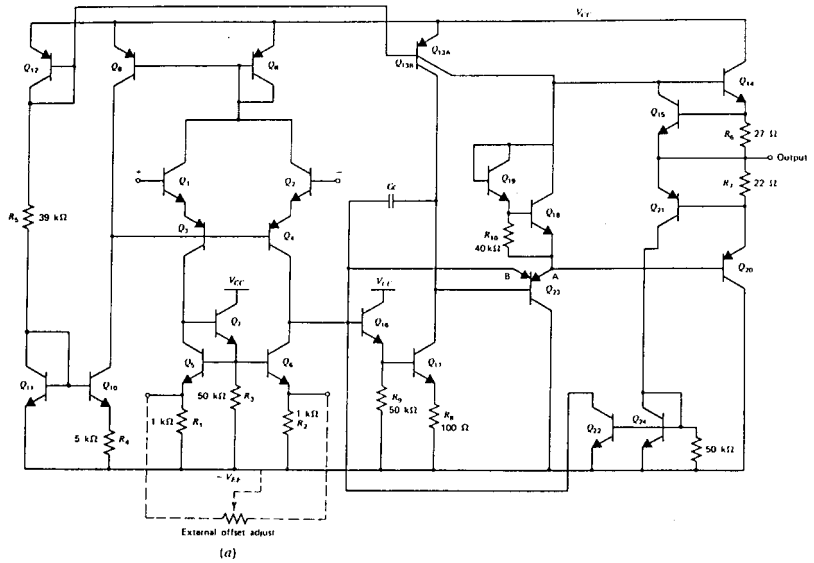

Fig. 6.6 A complete schematic diagram of 741 op amp

6.2.1.3 Output Stage

The output stage is composed of Q_{13A}, Q_{14}, Q_{18}, Q_{19}, Q_{20}, and Q_{23}, with the following characteristics:

a) A class-AB output stage

b) High input resistance and low output resistance

c) High power efficiency

6.2.2 DC Analysis

The dc analysis is much simpler with the following assumptions:

a) The dc output voltage is zero (by some external feedback network)

b) The Early effect of the transistors is negligibly

c) The current gain of npn transistors is large, but that of pnp transistors is small.

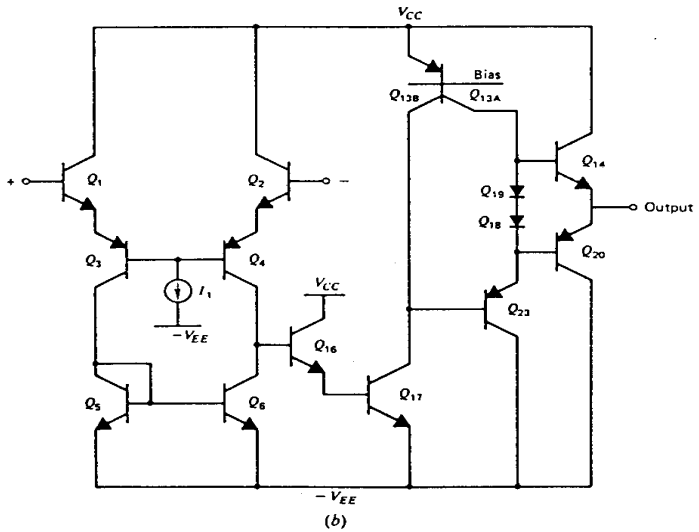

Fig. 6.7 Simplified schematic diagram of 741 op amp

6.2.2.1 Bias Circuitry

The bias circuitry for the 741 op amp is shown in Fig. 6.8. The Widlar current source is given by:

$$I_{ref} = \frac{V_{CC} + V_{EE} - 2V_{BE}}{R_5} = 0.73\text{mA} \tag{6.18}$$

The output current can be found by iterating the equation

$$I_1 R_4 = V_{BE_{11}} - V_{BE_{10}} = V_T \ln\left(\frac{I_{ref}}{I_1}\right) \tag{6.19}$$

This yields $I_1 = 19\ \mu A$. Given that the emitter area of Q_2 is the same as the total emitter area of Q_{13} and Q_{13B} is three times as large as that of Q_{13A}, we have:

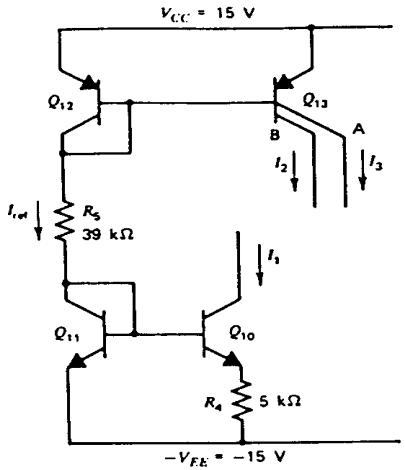

Fig. 6.8 Bias circuitry for the 741 op amp

$$I_2 = 3I_3 \tag{6.20}$$

$$I_2 + I_3 = I_{ref} \tag{6.21}$$

As a result, $I_2 = 0.55$ mA and $I_3 = 0.18$ mA.

6.2.2.2 Input Stage

A simplified schematic to calculate the bias for the op amp is shown in Fig. 6.9. For the input stage,

$$I_{C_8} = I_{C_9}\left(1 + \frac{2}{\beta_{pnp}}\right) \tag{6.22}$$

$$I_{C_1} = I_{C_2} = I_{C_3} = I_{C_4} = \frac{I_{C_8}}{2} = \frac{I_{C_9}}{2}\left(1 + \frac{2}{\beta_{pnp}}\right) \tag{6.23}$$

$$I_{ref} = I_{C_9} + I_{B_3} + I_{B_4} = I_{C_9}\left[1 + \frac{1 + \frac{2}{\beta_{pnp}}}{1 + \beta_{pnp}}\right] \tag{6.24}$$

This forms a common-mode negative-feedback loop: if I_{C9} is smaller than I_{ref}, I_{B3} and I_{B4} become larger, I_{C3} and I_{C4} are larger, which in turn cause I_{C8} to increase and finally I_{C9} to increase as well. Due to this negative feedback, eventually, $I_{C9} = I_{ref} \approx 19\,\mu A$.

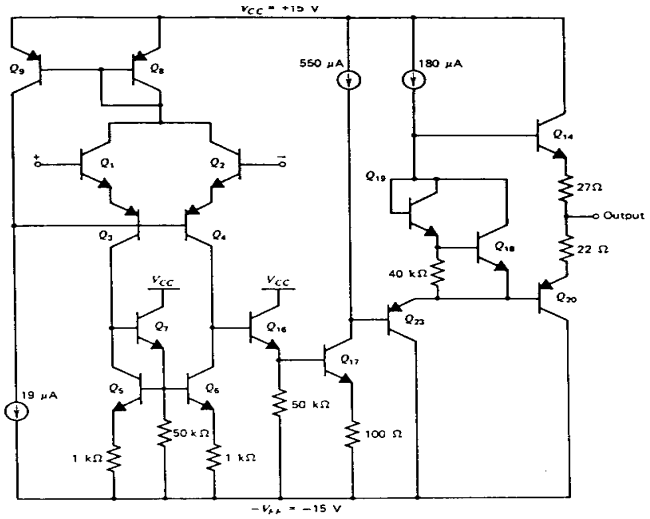

Fig. 6.9 Simplified schematic to calculate the bias for the 741 op amp

6.2.2.3 Gain Stage

$$I_{C_{17}} = 550\mu A \tag{6.25}$$

$$I_{C_{16}} = \frac{V_{BE_{17}} + I_{C_{17}} \times 100}{50k} + I_{B_{17}} = 16\mu A \tag{6.26}$$

6.2.2.4 Output Stage

$$I_{C_{18}} + I_{C_{19}} = 180\mu A = \frac{V_{BE_{18}}}{40k} + I_{C_{18}} = \frac{V_T}{40k}\ln\left(\frac{I_{C_{18}}}{I_S}\right) + I_{C_{18}} \tag{6.27}$$

Iterate to get $I_{C18} = 165\,\mu A$ and $I_{C19} = 15\,\mu A$. It follows that, with an assumption that Q_{14} and Q_{20} are three times as large as Q_{18} and Q_{19},

$$I_{C_{14}} = I_{C_{20}} = \sqrt{I_{C_{18}} I_{C_{19}}}\sqrt{\frac{I_{S_{14}} I_{S_{20}}}{I_{S_{18}} I_{S_{19}}}} = 152\mu A \tag{6.28}$$

6.2.2.5 Protection Circuitry

When the output current is too positive, Q_{15} is turned on and prevents too much current from flowing through the output device Q_{14}. When the output current is too negative, Q_{21}, Q_{22}, and Q_{24} turn on and divert current from the base of Q_{16}. Consequently, the output current is reduced (less negative). Protection transistors Q_{15} and Q_{21} are turned on only if

$$I_{R_6} > \frac{V_{BE(on)}}{R_6} = 20mA \tag{6.29}$$

$$I_{R_7} > \frac{V_{BE(on)}}{R_7} = 25mA \tag{6.30}$$

Note that the transistor Q_{23B}, by diverting the base current of Q_{16}, functions to prevent Q_{17} from operating in the saturation region.

6.2.3 Small-Signal Analysis

The small-signal analysis for the whole op amp can be much simplified by first carrying out the analysis for each of the three main stages (input, gain, and output) and then combining the results together.

6.2.3.1 Input Stage

From Fig. 6.10, the small-signal parameters for the input stage can be obtained as follows.

$$G_{m_1} = \frac{\partial i_o}{\partial v_{id}} = \frac{g_{m_1}}{2} \tag{6.31}$$

That is the transconductance is reduced by half due to the npn-pnp series combination.

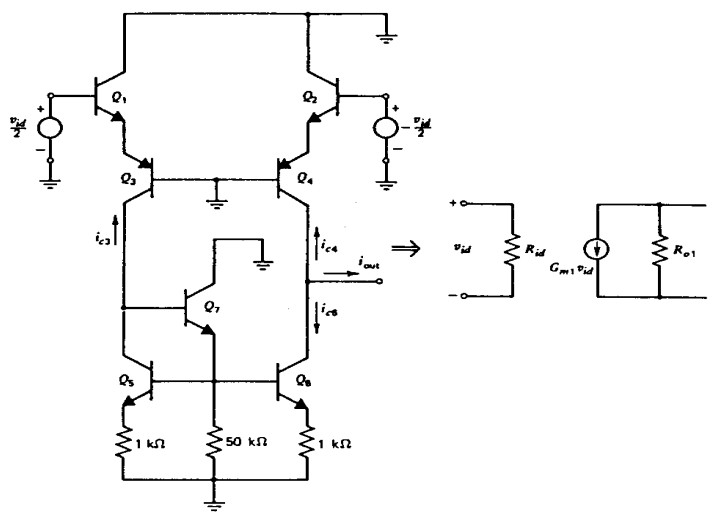

Fig. 6.10 Schematic to calculate small-signal parameters for the input stage

By inspection,

$$R_{id} = 2\left[r_{\pi_1} + (\beta_{pnp} + 1)\frac{1}{g_{m_3}}\right] \approx 4r_{\pi_1} \tag{6.32}$$

Define R_{o4} and R_{o6} as the output resistance looking into the collector of Q_4 and Q_6, respectively, we get:

$$R_{o_4} = r_{o_4}\left[1 + g_{m_4}\left(r_{\pi_4} \| \frac{1}{g_{m_2}}\right)\right] \approx r_{o_4}\left[1 + g_{m_4}\left(\frac{1}{g_{m_2}}\right)\right] \approx 2r_{o_4} \tag{6.33}$$

$$R_{o_6} = r_{o_6}[1 + g_{m_6}(r_{\pi_6} \| 1k)] \tag{6.34}$$

It follows that the output resistance R_{o1} is given by:

$$R_{o_1} = R_{o_4} \| R_{o_6} \tag{6.35}$$

6.2.3.2 Gain Stage

From Fig. 6.11, the small-signal parameters for the gain stage can be obtained as follows.

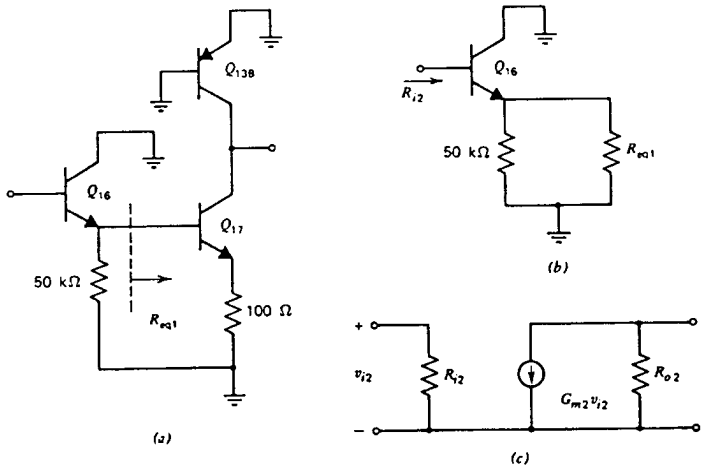

Fig. 6.11 Schematic to calculate small-signal parameters for the gain stage

$$G_{m_2} = \frac{g_{m_{17}}}{1 + g_{m_{17}} \times 100} \approx \frac{1}{147} \tag{6.36}$$

$$R_{eq_1} = r_{\pi_{17}} + (\beta_{pnp} + 1)100 \tag{6.37}$$

$$R_{i_2} = r_{\pi_{16}} + (\beta_{pnp} + 1)(R_{eq_1} \| 50k) \approx 5.7M\Omega \tag{6.38}$$

$$R_{o_2} = r_{o_{13B}} \| \{r_{o_{17}}[1 + g_{m_{17}}(r_{\pi_{17}} \| 100)]\} \approx r_{o_{13B}} \| \{r_{o_{17}}[1 + g_{m_{17}}(100)]\} = 83k\Omega \tag{6.39}$$

6.2.3.3 Output Stage

Since the output stage is a class-AB, it would depend on the operating condition. Assume that Q_{14} is on, I_o = 2mA, and R_L = 2kΩ, we have from Fig. 6.12,

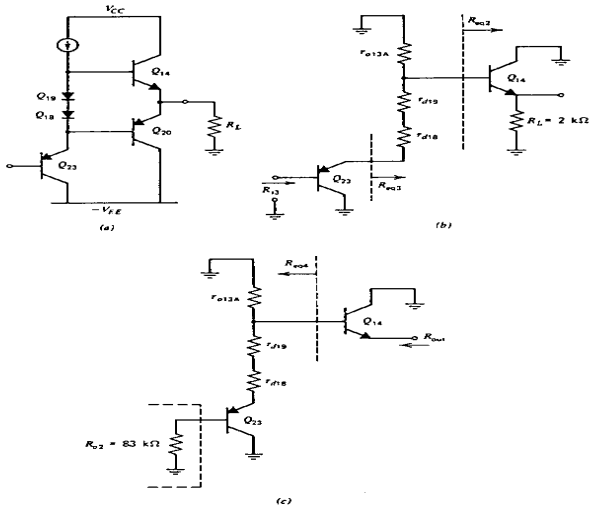

Fig. 6.12 Schematic to calculate small-signal parameters for the output stage

$$A_v \approx 1 \tag{6.40}$$

$$R_{eq_2} = r_{\pi_{14}} + (\beta_{pnp} + 1)2k \tag{6.41}$$

$$R_{eq_3} = r_{d_{18}} + r_{d_{19}} + R_{eq_2} \| r_{o_{13}} \tag{6.42}$$

$$R_{i_3} = r_{\pi_{23}} + (\beta_{pnp} + 1)R_{eq_3} \approx 9.1M\Omega \tag{6.43}$$

$$R_{eq_4} = \left(r_{d_{18}} + r_{d_{19}} + \frac{R_{o_2}}{\beta_{23}}\right) \| r_{o_{13A}} \tag{6.44}$$

$$R_{out} = \frac{R_{eq_4} + r_{\pi_{14}}}{\beta_{14}} \approx 21\Omega \tag{6.45}$$

6.2.3.4 Complete Analysis

The overall small-signal parameters of the whole op amp can be found by combining all the stages together as shown in Fig. 6.13, from which:

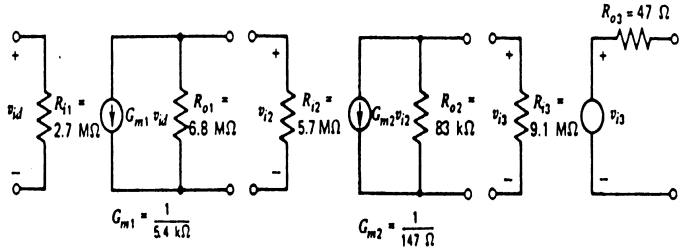

Fig. 6.13 Equivalent circuit to calculate small-signal parameters for the whole op amp

$$A_v = G_{m_1}(R_{o_1} \| R_{i_2})G_{m_2}(R_{o_2} \| R_{i_3}) \approx 324,000 \tag{6.46}$$

$$R_{in} = R_{i_1} = 2.7M\Omega \tag{6.47}$$

$$R_{out} = R_{out} + R_6 = 48\Omega \tag{6.48}$$

Note that as one gets familiar with the small-signal analysis, it would be much faster to do everything together without dividing the op amp into different stages.

6.3 Basic Topology for 2-Stage BJT Op Amp

For relatively small load (small capacitive load or large resistive load), it may not be necessary to include an output stage. For example, two-stage op amplifiers are widely used for on-chip amplification.

Topologically, such two-stage op amp would consist of an input stage and a gain stage, as can be seen in Fig. 6.14. For stability, a big compensation capacitor is normally required.

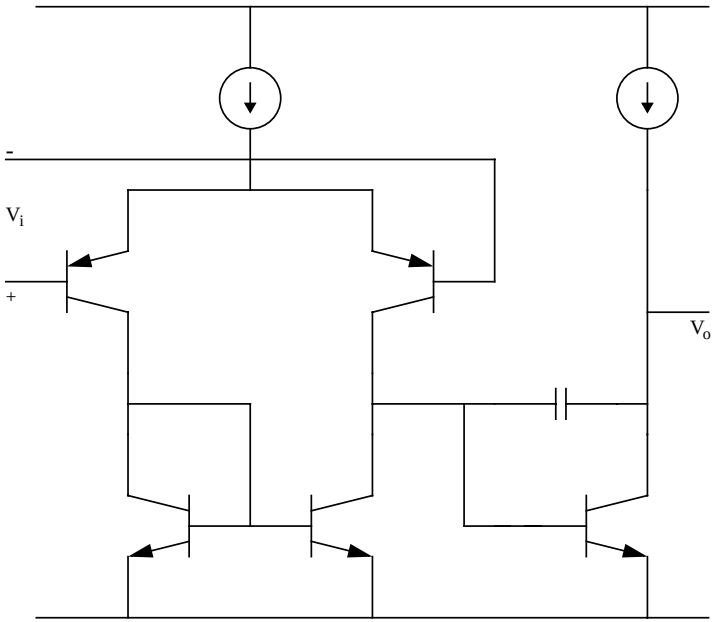

Fig. 6.14 A basic topology for a two-stage BJT op amp

6.4 Basic Topology for 2-Stage CMOS Op Amp

A CMOS counterpart of the basic two-stage BJT op amp is shown in Fig. 6.15.

Reference: See handout on "MOS Op Amp Design - A Tutorial Review," by Gray & Meyer, IEEE JSSC, December 1982.

The intrinsic small-signal voltage gain (without loading) can be derived to be:

$$A_v = \frac{v_o}{v_{in}} = -g_{m_2}(r_{o_2} \parallel r_{o_3})g_{m_5}(r_{o_5} \parallel r_{o_6}) \propto -(g_m r_o)^2 \tag{6.49}$$

where:

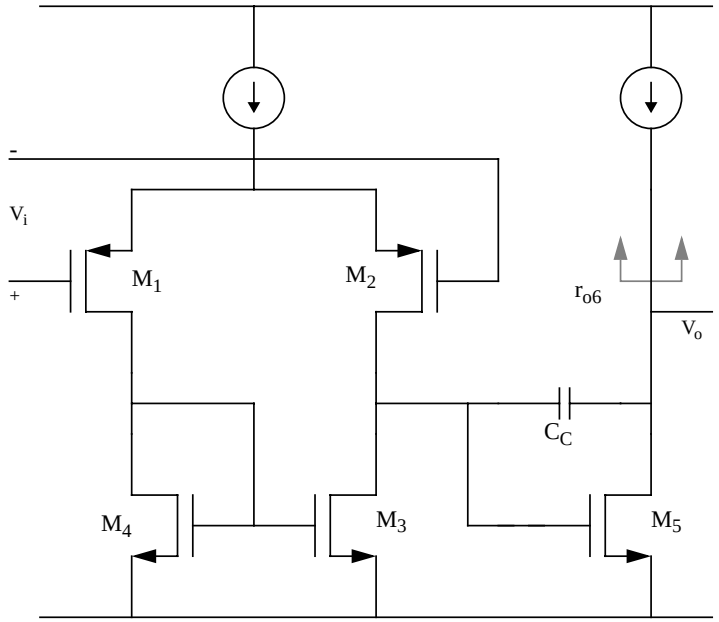

Fig. 6.15 A basic topology for a two-stage CMOS op amp

$$g_m r_o = \frac{2I_D}{V_{GS} - V_T} \cdot \frac{V_A}{I_D} = \frac{2V_A}{V_{GS} - V_T} \tag{6.50}$$

Recall that

$$V_A = L_{eff} \cdot \left[\frac{dX_d}{dV_{DS}}\right]^{-1} \tag{6.51}$$

As a result,

$$A_v \propto -(g_m r_o)^2 \propto -\left[\frac{2L_{eff}}{V_{GS} - V_T} \cdot \left(\frac{dX_d}{dV_{DS}}\right)^{-1}\right]^2 \tag{6.52}$$

Note that *the intrinsic voltage gain is independent of the bias current I_D*. From Eqs. (6.49)-(6.52), to achieve high intrinsic gain, it is desirable to have high g_m and large r_o, which is equivalent to have a small (V_{GS} - V_T) and large V_A.

Since

$$V_{GS} - V_T = \sqrt{\frac{2I_D}{\mu C_{ox}(W/L)}} \tag{6.53}$$

a high gain can be obtained by using a small bias current for a given W/L or using a large W/L for a given bias current.

To achieve a high V_A, we would want to have longer effective channel length. If we have a control on the process, a high substrate doping is also preferred.

As will be discussed later, all the solutions mentioned above would result in a degradation of the amplifier's frequency response. This is as expected since there is always a trade-off between the gain and the bandwidth of an op amp.

6.5 Cascode CMOS Op Amp

As mentioned previously, to increase the output impedance and thus the voltage gain of an amplifier, cascode configuration can be employed. Figure 6.16 shows an example of such a design.

The intrinsic small-signal voltage gain can be derived to be:

$$A_v = \frac{v_o}{v_{in}} = -g_{m_2}(R_{o_1} \| R_{o_2})\left\{\frac{g_{m_9}}{g_{m_9} + g_{b_9} + 1/r_{o_9} + 1/r_{o_{10}}}\right\} g_{m_{11}}(R_{o_3} \| R_{o_4}) \tag{6.54}$$

Typically, this can be approximated as:

$$A_v = \frac{v_o}{v_{in}} = -g_{m_2}(R_{o_1} \| R_{o_2}) g_{m_{11}}(R_{o_3} \| R_{o_4}) \tag{6.55}$$

where:

$$R_{o_1} = r_{o_3}(1 + g_{m_3} r_{o_2}) \tag{6.56}$$

$$R_{o_2} = r_{o_6}(1 + g_{m_6} r_{o_7}) \tag{6.57}$$

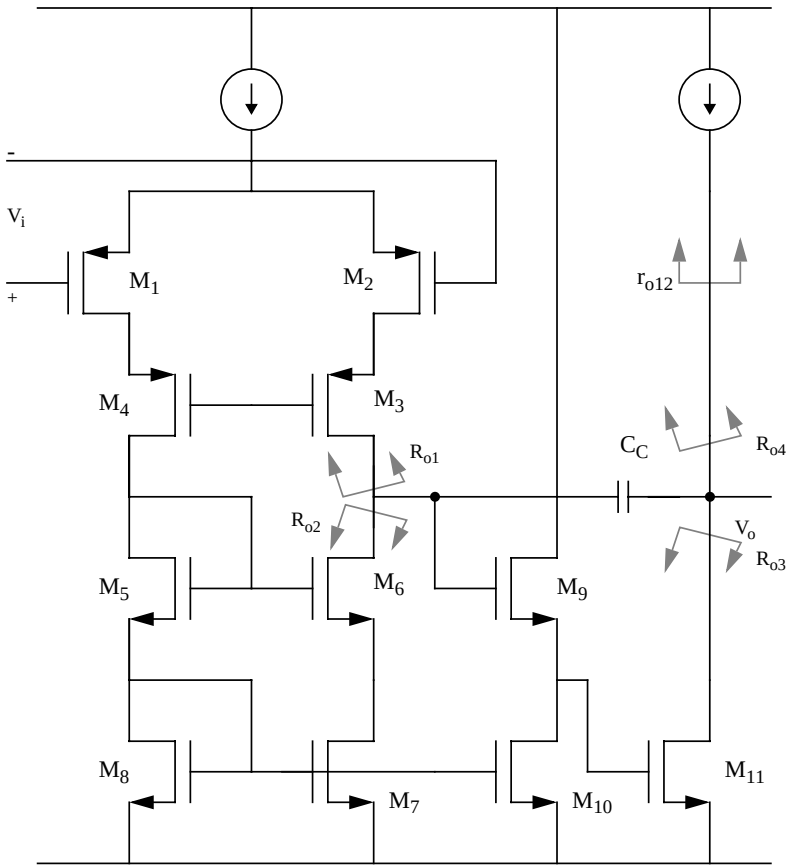

Fig. 6.16 An implementation of a cascode CMOS op amp

As a result, with the first stage being cascoded, the voltage gain becomes:

$$A_v = -g_{m_2}(r_{o_3} \| r_{o_6}) g_{m_{11}}(R_{o_3} \| R_{o_4})(1 + g_m r_o) \tag{6.58}$$

which is an increase by a factor of:

$$\frac{A_v(\text{cascode})}{A_v(\text{regular})} = 1 + g_m r_o \tag{6.59}$$

If the second stage is also cascoded, the gain-enhancement factor becomes:

$$\frac{A_v(\text{cascode})}{A_v(\text{regular})} = [1 + g_m r_o]^2 \tag{6.60}$$

6.6 Folded-Cascode CMOS Op Amp

With a folded-cascode design as shown in Fig. 6.17, it is possible to implement a single-stage op amp that can achieve a gain as high as that of a two-stage amplifier.

Reference: See handout on “Design Procedure of Fully Differential Folded Cascode CMOS Op Amp,” by Mallya, et al, IEEE JSSC, December 1989.

Typically, the transistors’ aspect ratios W/L’s are chosen so that:

$$I_{D_3} = I_{D_4} = I_{D_{11}} = 2I_{D_1} = 2I_{D_2} = 2I_{D_5} = 2I_{D_6} \tag{6.61}$$

The intrinsic small-signal voltage gain can be obtained as:

$$A_v = \frac{v_o}{v_{in}} = -g_{m_2}(R_{o_1} \| R_{o_2}) \tag{6.62}$$

where:

$$R_{o_1} = r_{o_5}\{1 + g_{m_5}(r_{o_1} \| r_{o_4})\} \tag{6.63}$$

$$R_{o_2} = r_{o_8}(1 + g_{m_8} r_{o_9}) \tag{6.64}$$

Again, with cascode, the gain is increased by a factor of:

$$\frac{A_v(\text{cascode})}{A_v(\text{regular})} = 1 + g_m r_o \tag{6.65}$$

Not only does this folded-cascode design have a high gain but it also has a high frequency response due to the elimination of Miller effect by the cascode configuration (as will be shown later).

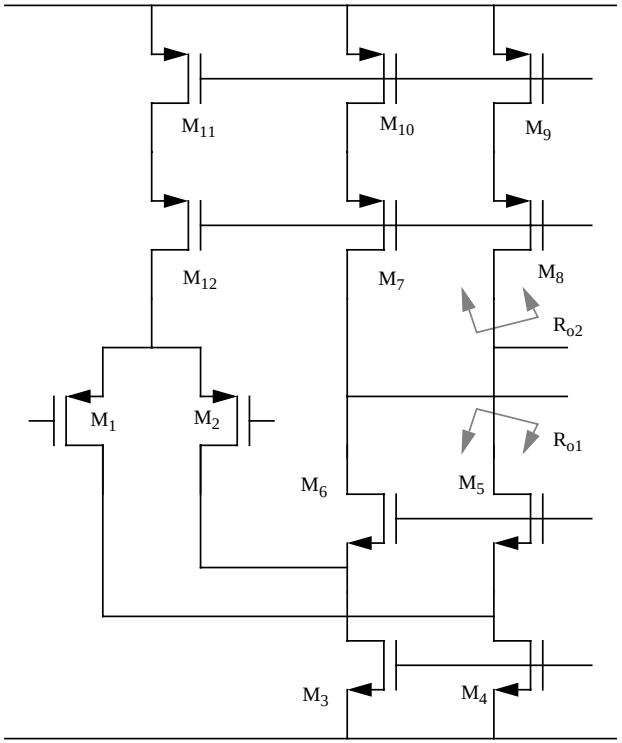

Fig. 6.17 Schematic of a folded-cascode CMOS op amp

In addition, because it is a single-stage implementation, the amplifier is unconditionally stable. As a result, there is no need of compensation, and the design can be much smaller and faster than a conventional two-stage op amp.

In order to achieve a rail-to-rail voltage swing at the output, the output transistors can be biased by a high-swing current source discussed earlier. Figure 6.18 shows an implementation of such a high-swing folded-cascode design.

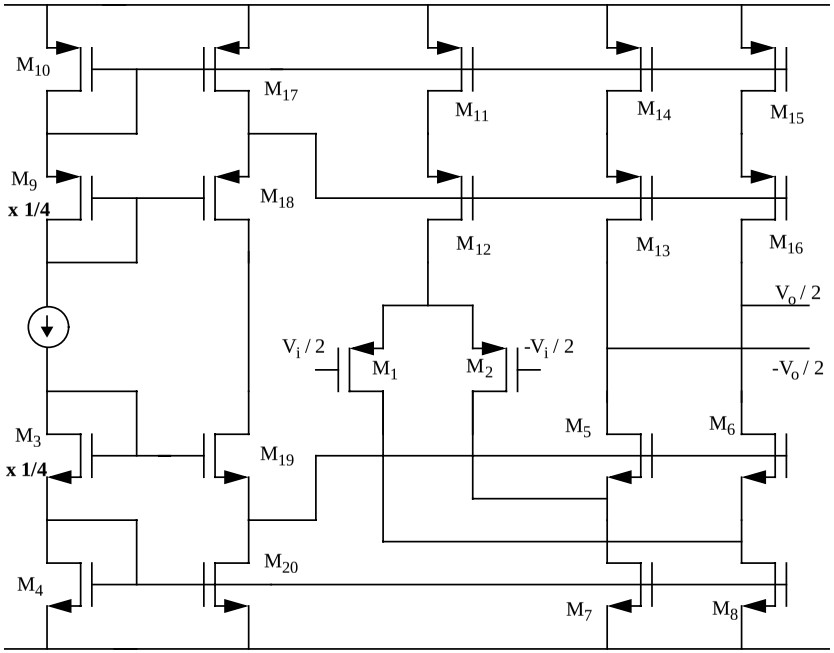

Fig. 6.18 An implementation of a high-swing folded-cascode CMOS op amp