Chapter 5

INPUT OFFSET VOLTAGE

5.1 Introduction

Ideally, for an op amp, the DC output voltage should be zero if there is no input signal applied. That is, the DC transfer curve should cross the origin. However, in practice, due to device mismatches, the output voltage is typically non-zero, and the transfer curve does not intersect the y-axis at the origin.

By applying a small differential voltage at the input, the output voltage can be made zero. This small differential input voltage required to achieve a zero DC output voltage is called the offset voltage and is a measurement of how well the components used in the op amp are matched.

This set of notes will show how the offset voltage is calculated for emitter-coupled pairs with resistive loads, emitter-coupled pairs with active loads, source-coupled pairs with resistive loads, and finally source-coupled pairs with active loads.

5.2 Emitter-Coupled Pair With Resistive Loads

For the emitter-coupled pair with resistive loads shown in Fig. 5.1 below, KVL gives:

$$V_{OS} = V_{BE_1} - V_{BE_2} = V_T \ln\left(\frac{I_{C_1} I_{S_2}}{I_{C_2} I_{S_1}}\right) \tag{5.1}$$

But by definition of the offset voltage,

$$0 = V_{od} = (V_{CC} - I_{C_2}R_2) - (V_{CC} - I_{C_1}R_1) = I_{C_1}R_1 - I_{C_2}R_2 \tag{5.2}$$

As a result,

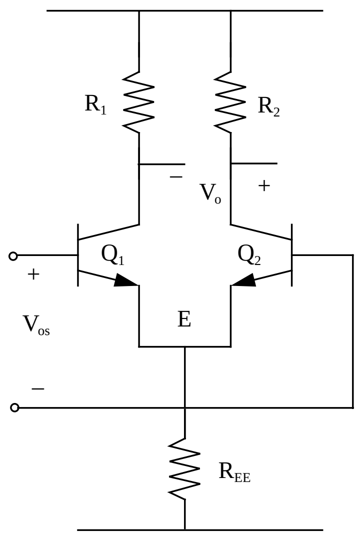

Fig. 5.1 Schematic of an emitter-coupled pair

$$\frac{I_{C_1}}{I_{C_2}} = \frac{R_2}{R_1} \tag{5.3}$$

Define:

$$\Delta I_S = I_{S_1} - I_{S_2} \tag{5.4}$$

$$I_S = \frac{I_{S_1} + I_{S_2}}{2} \tag{5.5}$$

$$\Delta R = R_1 - R_2 \tag{5.6}$$

$$R = \frac{R_1 + R_2}{2} \quad (5.7)$$

We get:

$$V_{OS} = V_T \ln\left\{\frac{R - \frac{\Delta R}{2}}{R + \frac{\Delta R}{2}} \cdot \frac{I_S - \frac{\Delta I_S}{2}}{I_S + \frac{\Delta I_S}{2}}\right\} \quad (5.8)$$

For $\Delta R << R$, $\Delta I_S << I_S$,

$$V_{OS} = V_T \ln\left[\left(1 - \frac{\Delta R}{R}\right) \cdot \left(1 - \frac{\Delta I_S}{I_S}\right)\right] = V_T\left[\ln\left(1 - \frac{\Delta R}{R}\right) + \ln\left(1 - \frac{\Delta I_S}{I_S}\right)\right] \quad (5.9)$$

Taylor series expansion for ln(1+x) gives

$$V_{OS} = V_T\left[-\frac{\Delta R}{R} - \frac{\Delta I_S}{I_S}\right] \quad (5.10)$$

Typically, $\Delta R/R = 1\%$, $\Delta I_S/I_S = 5\%$, which corresponds to a offset voltage V_{OS} of 1.5 mV.

NOTE: As of now, it has been shown that approximation can be used to estimate the offset voltage. Alternatively, the offset voltage can be estimated by directly applying differentiation to the definition of the offset voltage

$$V_{OS} = V_{BE_1} - V_{BE_2} = \Delta V_{BE} = \frac{\partial V_{BE}}{\partial I_C}\Delta I_C + \frac{\partial V_{BE}}{\partial I_S}\Delta I_S \quad (5.11)$$

which turns out to be even more elegant solution!

5.3 Source-Coupled Pair With Resistive Loads

For the source-coupled pair with resistive loads shown in Fig. 5.2,

$$V_{OS} = V_{gs_1} - V_{gs_2} = V_{t_1} + \sqrt{\frac{2I_{D_1}}{\mu_n C_{ox}(W/L)_1}} - V_{t_2} - \sqrt{\frac{2I_{D_2}}{\mu_n C_{ox}(W/L)_2}} \quad (5.12)$$

But by definition of the offset voltage,

$$0 = V_{od} = (V_{DD} - I_{D_2}R_2) - (V_{DD} - I_{D_1}R_1) = I_{D_1}R_1 - I_{D_2}R_2 \quad (5.13)$$

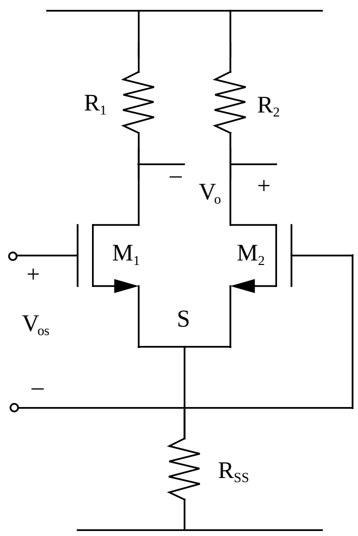

Fig. 5.2 Schematic of a source-coupled pair

As a result,

$$\frac{I_{D_1}}{I_{D_2}} = \frac{R_2}{R_1} \quad (5.14)$$

Define:

$$\Delta I_D = I_{D_1} - I_{D_2} \quad (5.15)$$

$$I_D = \frac{I_{D_1} + I_{D_2}}{2} \quad (5.16)$$

$$\Delta(W/L) = (W/L)_1 - (W/L)_2 \quad (5.17)$$

$$(W/L) = \frac{(W/L)_1 + (W/L)_2}{2} \quad (5.18)$$

$$\Delta V_t = V_{t_1} - V_{t_2} \quad (5.19)$$

$$\Delta V_t = \frac{V_{t_1} + V_{t_2}}{2} \quad (5.20)$$

$$\Delta R = R_1 - R_2 \quad (5.21)$$

$$R = \frac{R_1 + R_2}{2} \quad (5.22)$$

Put all together, it can be shown that:

$$V_{OS} = \Delta V_t + \frac{(V_{GS} - V_t)}{2}\left[-\frac{\Delta R}{R} - \frac{\Delta(W/L)}{(W/L)}\right] \quad (5.23)$$

Assume that ΔV_t = 10 mV, V_{GS}-V_t = 300 mV, $\Delta R/R$ = 1%, $\Delta(W/L)/(W/L)$ = 5%, the offset voltage V_{OS} becomes approximately 20 mV, which is *much larger* than that of an emitter-coupled pair.

NOTE: As for emitter-coupled pairs, the offset voltage of source-coupled pairs can also be estimated by directly applying differentiation to the definition of the offset voltage

$$V_{OS} = \Delta V_{GS} = \frac{\partial V_{GS}}{\partial V_t}\Delta V_t + \frac{\partial V_{GS}}{\partial I_D}\Delta I_D + \frac{\partial V_{GS}}{\partial (W/L)}\Delta(W/L) \quad (5.24)$$

5.4 Emitter-Coupled Pair With Active Loads

The input offset voltage of differential pairs with active loads is defined as the input voltage required to drive the *current* output to zero (contrast to the cases of resistive loads in which the zero output voltage is of concern). For the emitter-coupled pair with a current mirror as an active load shown in Fig. 5.3, the offset voltage can be calculated as follows.

$$V_{OS} = V_{BE_1} - V_{BE_2} = V_T \ln\left(\frac{I_{C_1}}{I_{C_2}}\frac{I_{S_2}}{I_{S_1}}\right) \quad (5.25)$$

But,

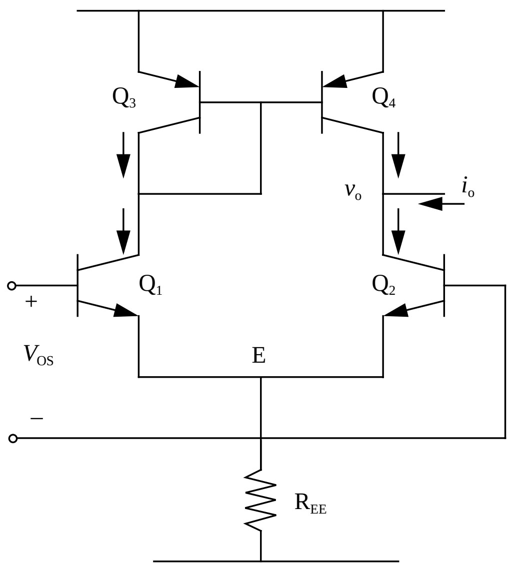

Fig. 5.3 Schematic of an emitter-coupled pair with active loads

$$I_{C_2} = I_{C_4} = I_{C_3} \cdot \frac{I_{S_4}}{I_{S_3}} \quad (5.26)$$

$$I_{C_1} = I_{C_3} \cdot \left(1 + \frac{2}{\beta_3}\right) \quad (5.27)$$

As a result,

$$V_{OS} = V_T \ln\left[\frac{I_{S_3}}{I_{S_4}}\frac{I_{S_2}}{I_{S_1}}\left(1 + \frac{2}{\beta_3}\right)\right] \quad (5.28)$$

Define the average and the difference values for the saturation currents of both npn and pnp transistors and the current gain β in the usual way, that is,

$$\Delta I_S = I_{S_1} - I_{S_2} \quad (5.29)$$

$$I_S = \frac{I_{S_1} + I_{S_2}}{2} \tag{5.30}$$

The offset voltage can be approximated to be:

$$V_{OS} = V_T\left(\frac{\Delta I_{S,\,pnp}}{I_{S,\,pnp}} - \frac{\Delta I_{S,\,npn}}{I_{S,\,npn}} + \frac{2}{\beta_{pnp}}\right) \tag{5.31}$$

For an emitter-coupled pair with $\beta_{pnp} = 50$, $\Delta I_S/I_S = 5\%$, the offset voltage V_{OS} is approximately 4 mV, which is significantly larger than that for resistive loads.

5.5 Source-Coupled Pair With Active Loads

The input offset voltage for a source-coupled pair with active loads as shown in Fig. 5.4 can be approximated to consist of two components, one from mismatches of the input transistors and the other referred to the input from the current mirror.

First, let’s calculate the offset contributed by the mismatch of the current mirror. In defining the difference and average quantities, we will use subscripts N and P to denote the NMOS (input) and PMOS (load) devices, respectively. As an example,

$$\Delta I_{D_P} = I_{D_3} - I_{D_4} \quad \text{and} \quad I_{D_N} = \frac{I_{D_1} + I_{D_2}}{2} \tag{5.32}$$

Referring to Eq. (4.172) on Page 321 in Gray & Meyer, the mismatch of the current mirror can be found to be:

$$\Delta I_{D_P} = I_{D_3} - I_{D_4} = I_{D_P}\frac{\Delta(W/L)_P}{(W/L)_P} - g_{m_P}\Delta V_{t_P} \tag{5.33}$$

Referred to the input, this current mismatch contributes an input offset voltage of

$$V_{OS_P} = \left(-\frac{1}{g_{m_N}}\right)\left(I_{D_P}\frac{\Delta(W/L)_P}{(W/L)_P} - g_{m_P}\Delta V_{t_P}\right) = -\frac{(V_{GS}-V_t)_N}{2}\left[\frac{\Delta(W/L)_P}{(W/L)_P}\right] + (\Delta V_{t_P})\frac{g_{m_P}}{g_{m_N}} \tag{5.34}$$

The offset contributed by the input transistors is given by

$$V_{OS_N} = \Delta V_{t_N} + \frac{(V_{GS}-V_t)_N}{2}\left[-\frac{\Delta(W/L)_N}{(W/L)_N}\right] \tag{5.35}$$

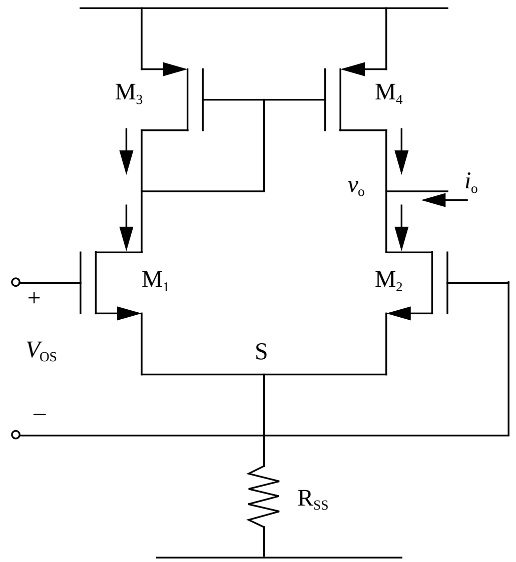

Fig. 5.4 Schematic of a source-coupled pair with active loads

The total input offset voltage V_{OS} contributed by both the input transistors and the current-mirror loads becomes:

$$V_{OS} = V_{OS_N} + V_{OS_P} = \Delta V_{t_N} + (\Delta V_{t_P})\frac{g_{m_P}}{g_{m_N}} + \frac{(V_{GS}-V_t)_N}{2}\left[-\frac{\Delta(W/L)_N}{(W/L)_N} - \frac{\Delta(W/L)_P}{(W/L)_P}\right] \tag{5.36}$$

Assume that $\Delta V_t = 10$ mV, V_{GS}-$V_t = 200$ mV, $\Delta(W/L)/(W/L) = 5\%$, $g_{m,PMOS}/g_{m,NMOS} = 1/2$, the offset voltage V_{OS} becomes approximately 35 mV, which is *much larger* than that of any other configuration!

From Eq. (5.36), it can be inferred that, given a fixed device mismatch, the offset voltage can be reduced by minimizing both the ratio ($g_{m,PMOS}/g_{m,NMOS}$) and the quantity $(V_{GS}\text{-}V_t)_N$. The ratio of the two transconductances can be reduced by choosing the W/L ratios of the load transistors to be much smaller than the W/L ratios of the input transistors. On the other hand, a small gate-to-source voltage requires either that the input devices have large W/L ratios or that the bias current is small.