ROCHESTER INSTITUTE OF TECHNOLOGY
MICROELECTRONIC ENGINEERING

MOSFET DC Models

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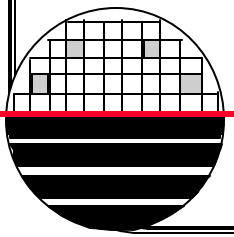
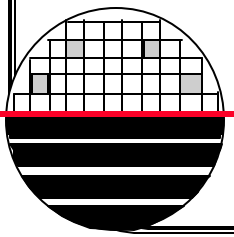


OUTLINE

Measure nMOS and pMOS
- Ids-Vds Family of Curves
- Ids-Vgs, gm and sub threshold plots

SPICE Simulation of
- Ids-Vds Family of Curves
  - Level 1, Level 3, Level 7
- Ids-Vgs, gm and sub threshold plots
  - Level 1, Level 7



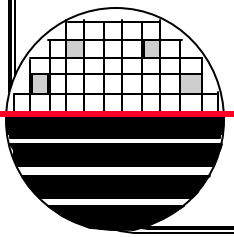
INTRODUCTION

SPICE (Simulation Program for Integrated Circuit Engineering) is a general-purpose circuit simulation program for non-linear DC, non-linear transient, and linear AC analyses. Circuits may contain resistors, capacitors, inductors, mutual inductors, independent voltage and current sources, four types of dependent sources, transmission lines, switches, and several semiconductor devices: including diodes, BJTs, JFETs, MESFETs, and MOSFETs.

PSpice Lite 9.2 is one of the OrCAD family of products offering a complete suite of electronic design tools. These products are available from Cadence Design Systems, Inc. PSpice Lite 9.2 includes limited versions of OrCAD Capture, for schematic capture, PSpice for analog circuit simulation and Pspice A/D for mixed analog and digital circuit simulation. PSpice Lite 9.2 is limited to 64 nodes, 10 transistors, two operational amplifiers and 65 primitive digital devices. See page 35 (xxxv) of the PSpice Users Guide.

SIMULATION PROGRAM FOR INTEGRATED CIRCUIT ENGINEERING

MOSFET Device models used by SPICE (Simulation Program for Integrated Circuit Engineering) simulators can be divided into three classes: First Generation Models (Level 1, Level 2, Level 3 Models), Second Generation Models (BISM, HSPICE Level 28, BSIM2) and Third Generation Models (BSIM3, etc.) The newer generations can do a better job with short channel effects, local stress, transistors operating in the sub-threshold region, gate leakage (tunneling), noise calculations, temperature variations and the equations used are better with respect to convergence during circuit simulation.



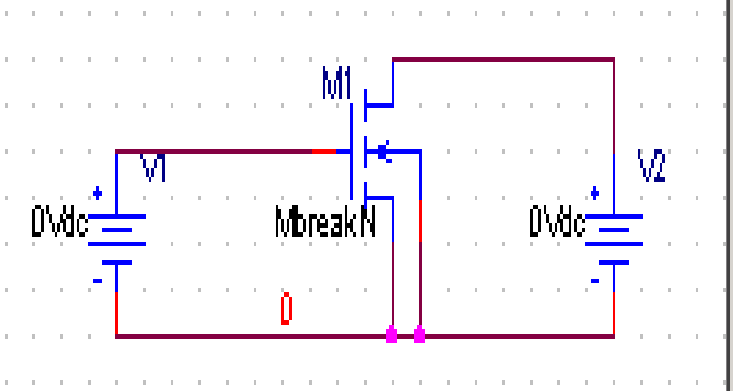
MOSFET SPICE MODEL LEVELS

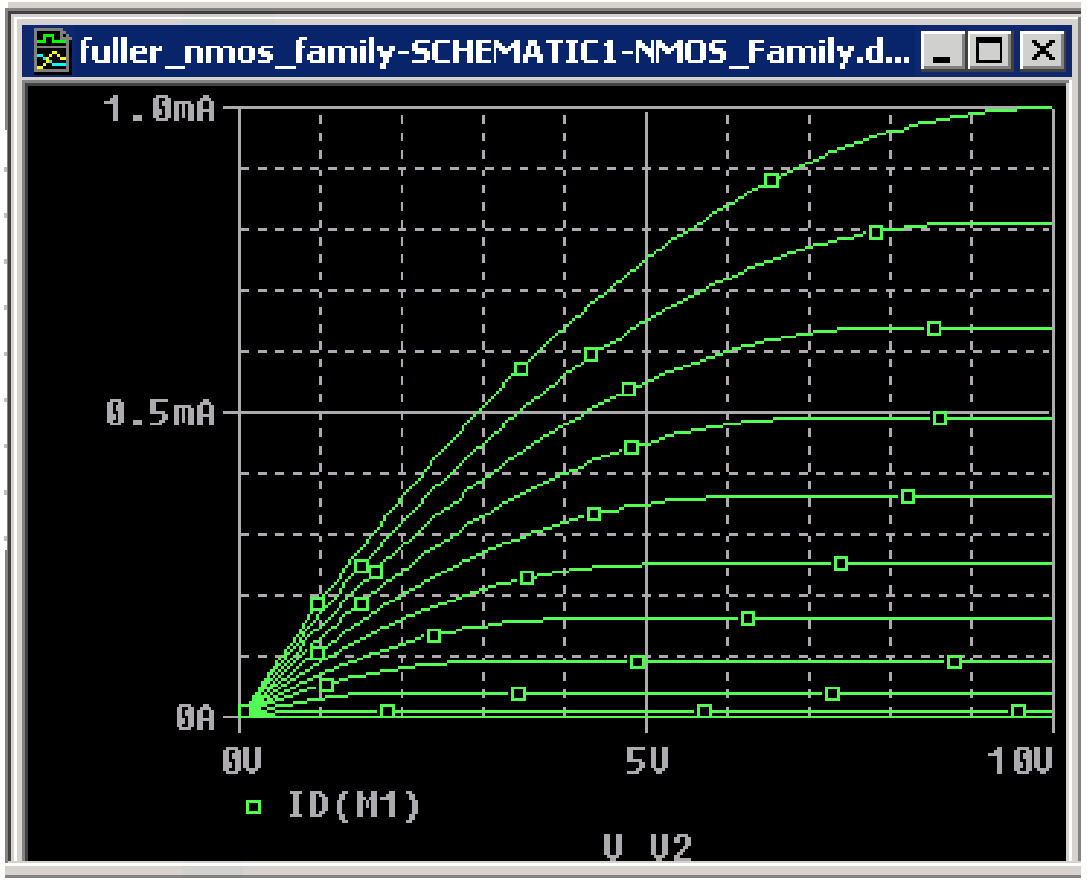
The simulator has:
The simulator provides six MOSFET device models, which differ in the formulation of the I-V characteristic. The LEVEL parameter selects among different models as shown below. For more information, see References.
LEVEL=1 Shichman-Hodges model (see reference [1])
LEVEL=2 geometry-based, analytic model (see reference [2])
LEVEL=3 semi-empirical, short-channel model (see reference [2])
LEVEL=4 BSIM model (see reference [3])
LEVEL=5 EKV model version 2.6 (see reference [10])
LEVEL=6 BSIM3 model version 2.0 (see reference [7])
LEVEL=7 BSIM3 model version 3.1 (see reference [8])

Level 7 is the level 49 of hspice (similar).

Levels 49 and 53 BSIM3v3 MOS Models
The BSIM3v3 MOS model from UC Berkeley is available as Avant! Level 49 and Level 53 models. Level 49 is an Hspice-enhanced version of BSIM3v3 while Level 53 maintains full compliance with the Berkeley release. This compliance includes numerically identical model equations, identical parameter default values, and identical parameter range limits.

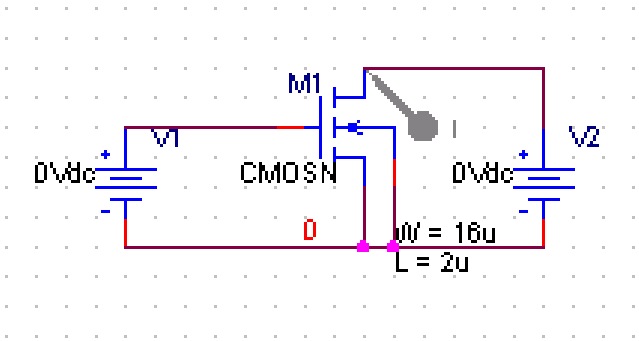
SIMULATION of Id-Vds Family

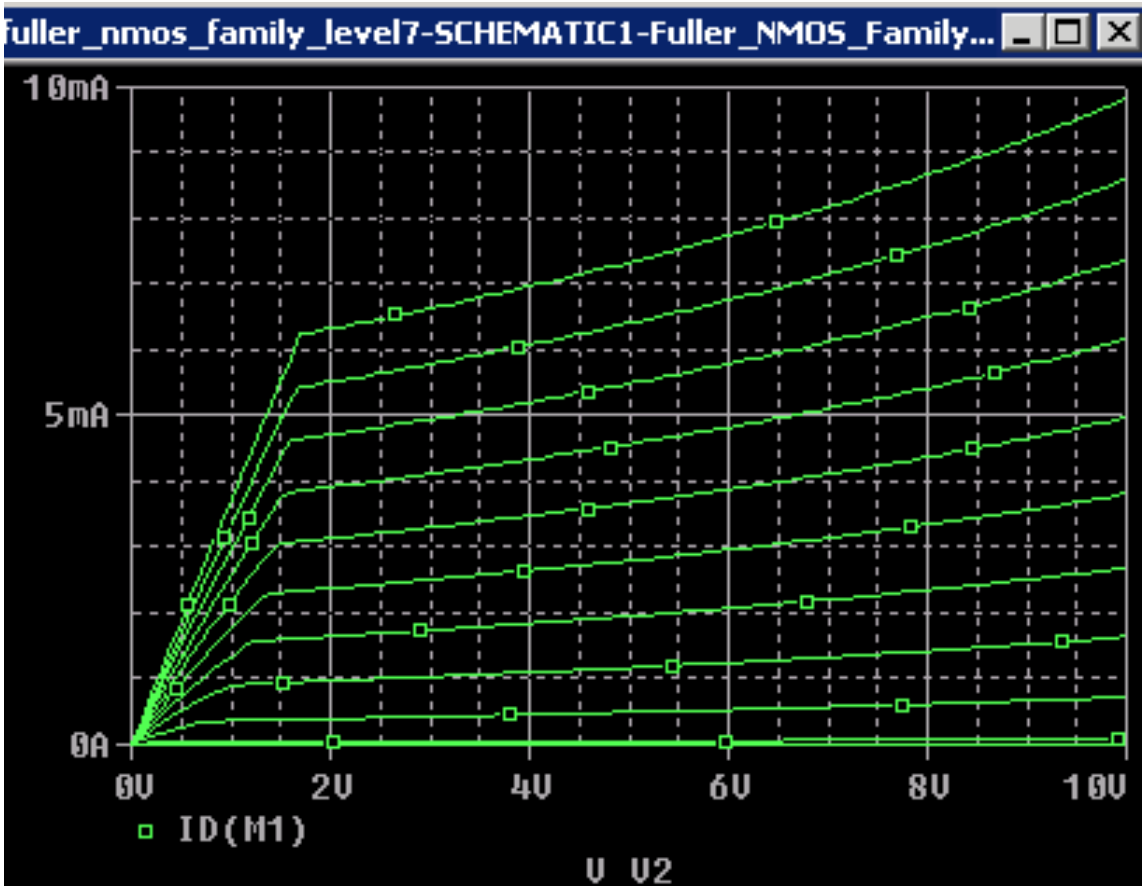




Using Level = 1 transistor models

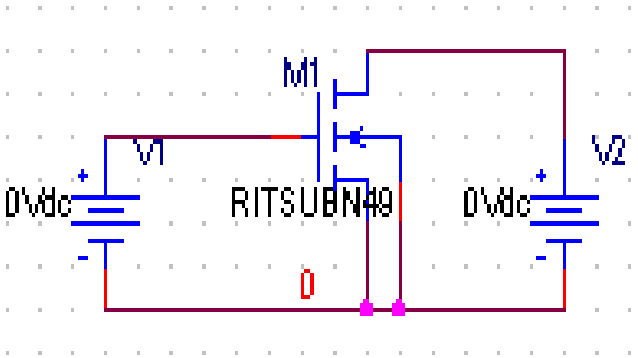
SIMULATION of Id-Vds Family

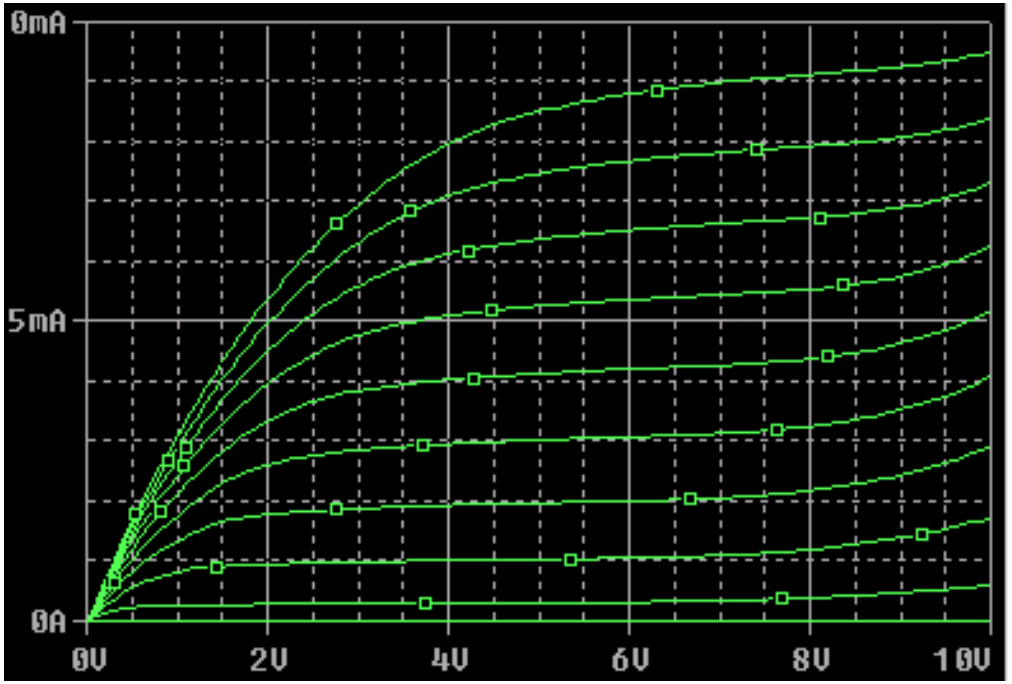




Level=2

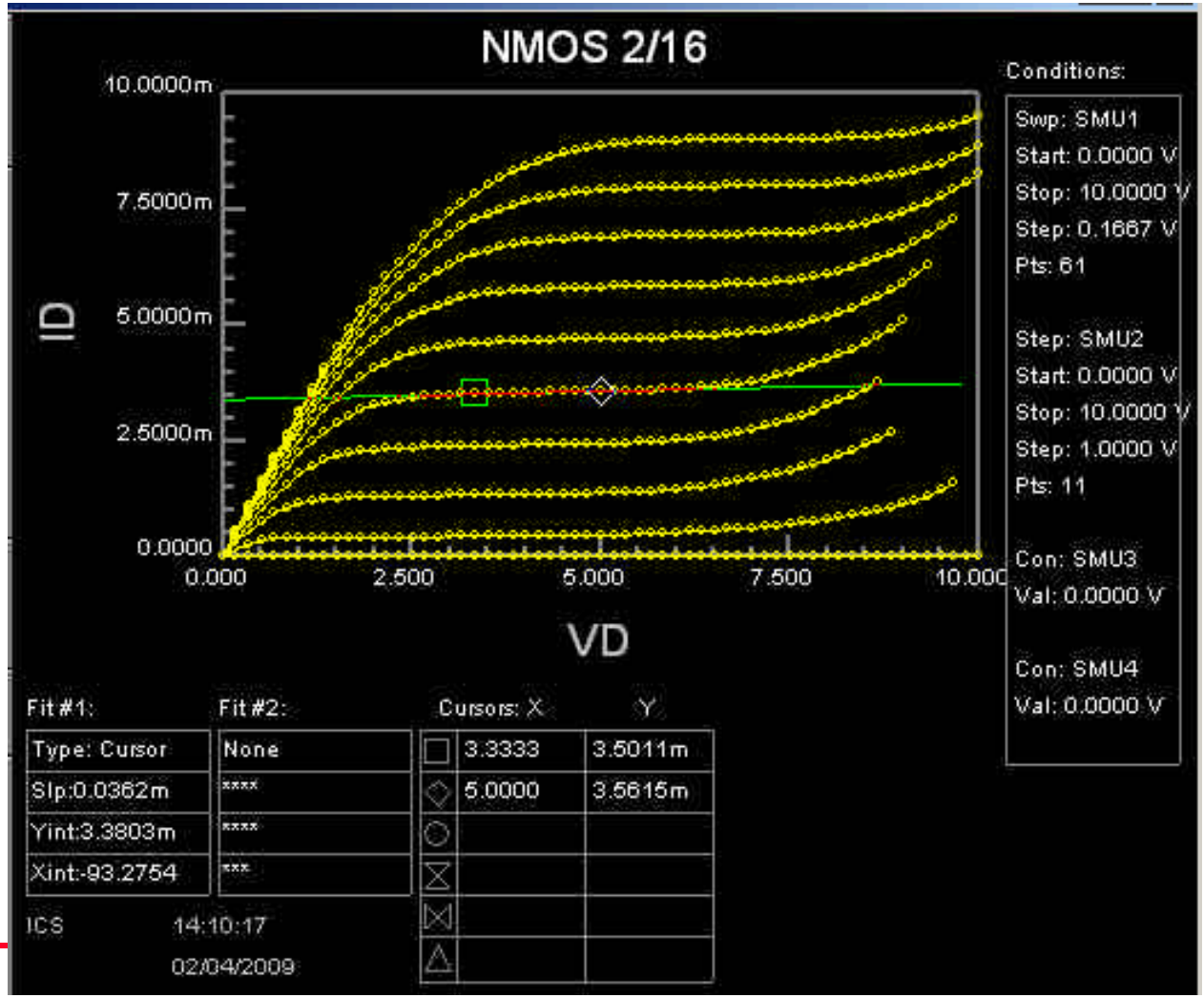
SIMULATION of Id-Vds Family



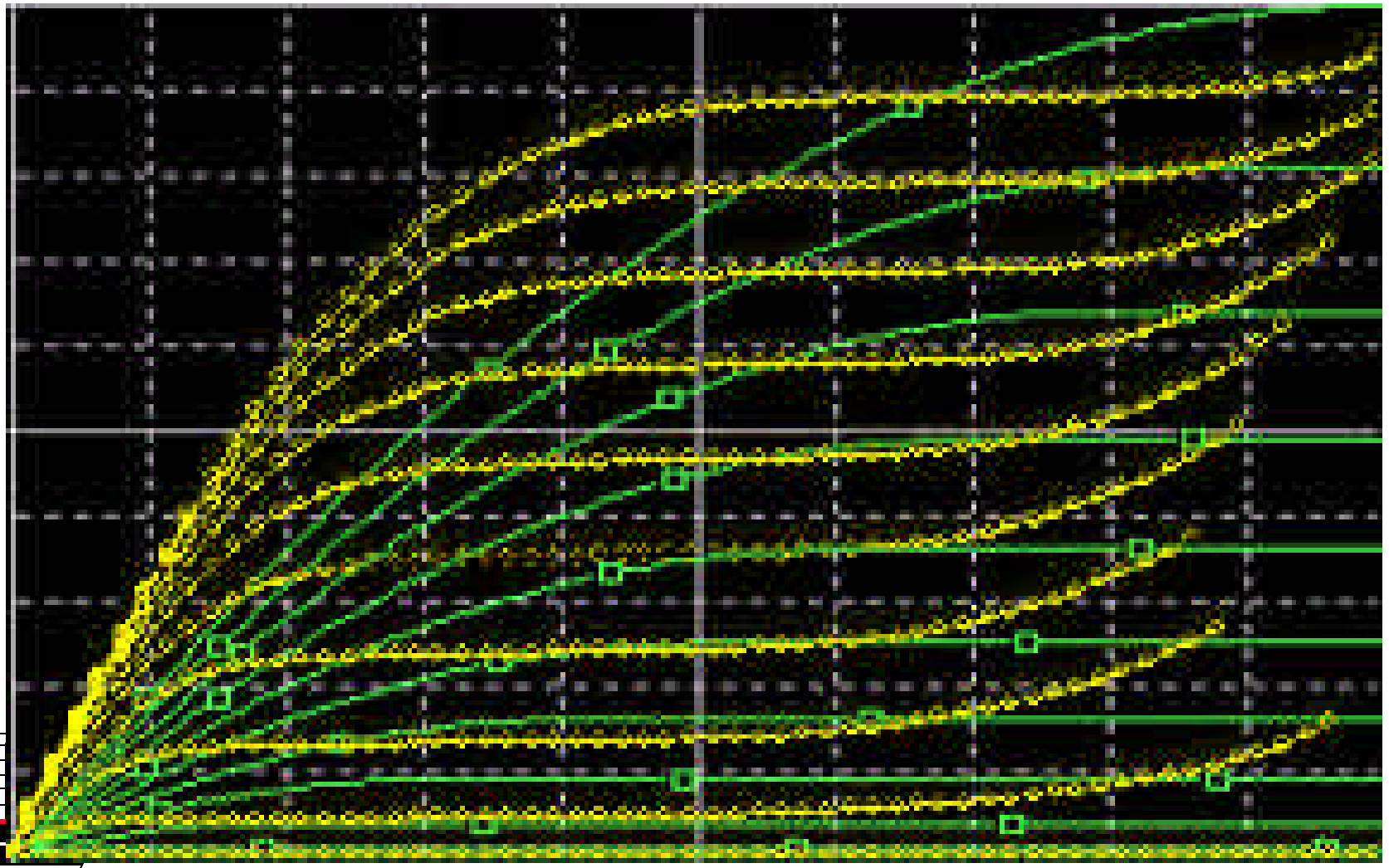


Using Level = 7 transistor models

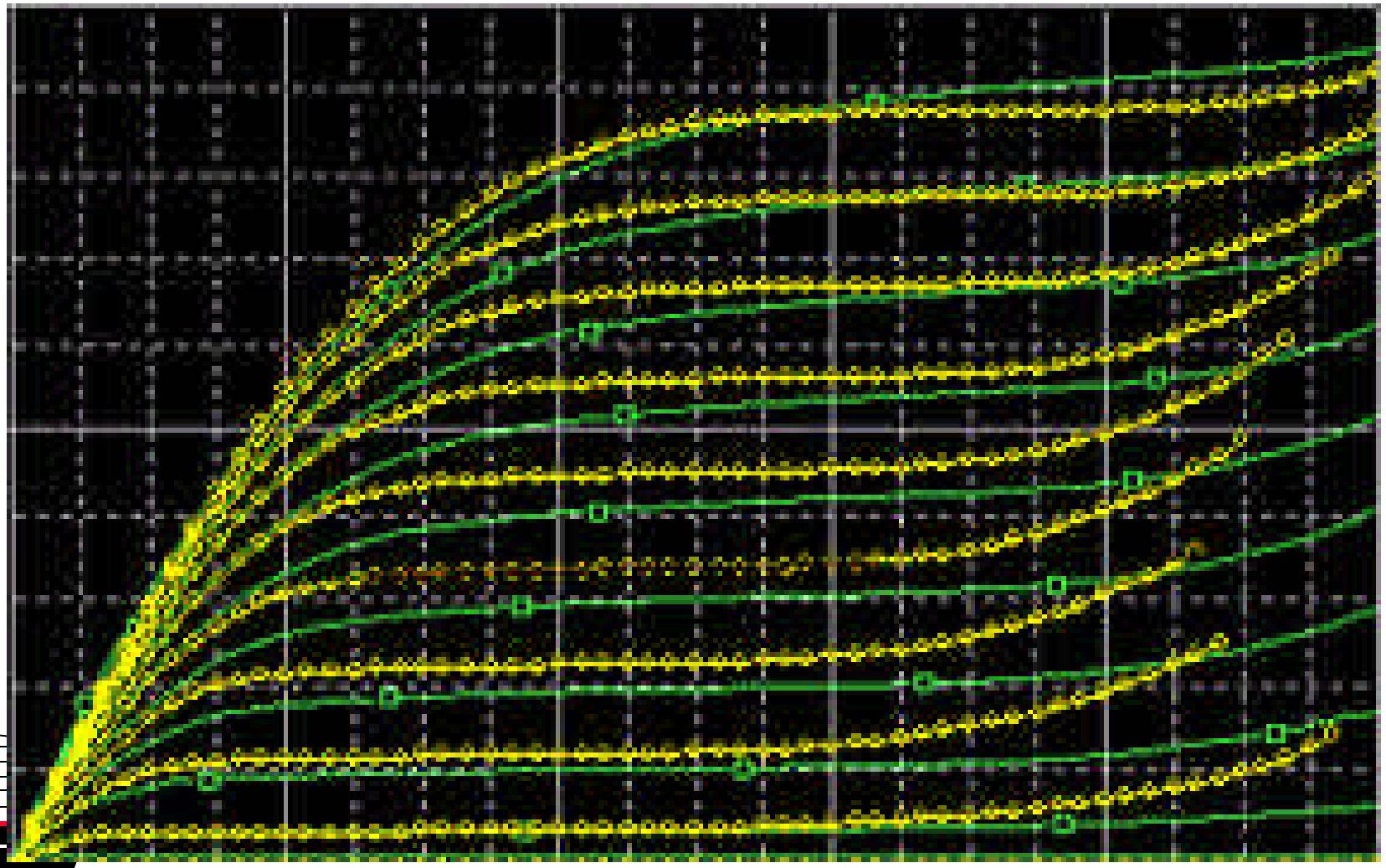
MEASURED Id-Vds Family



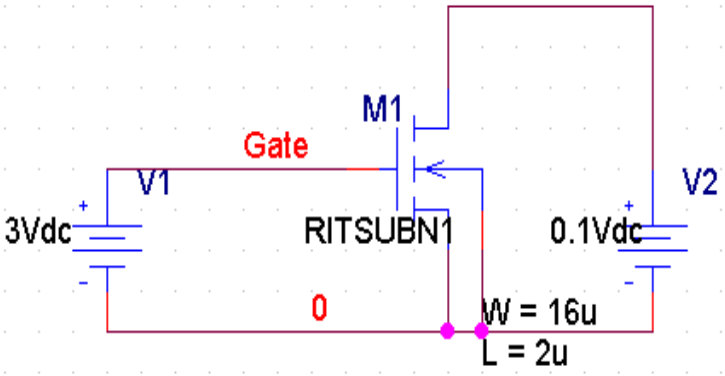
MEASURED SUPERIMPOSED ON LEVEL=1

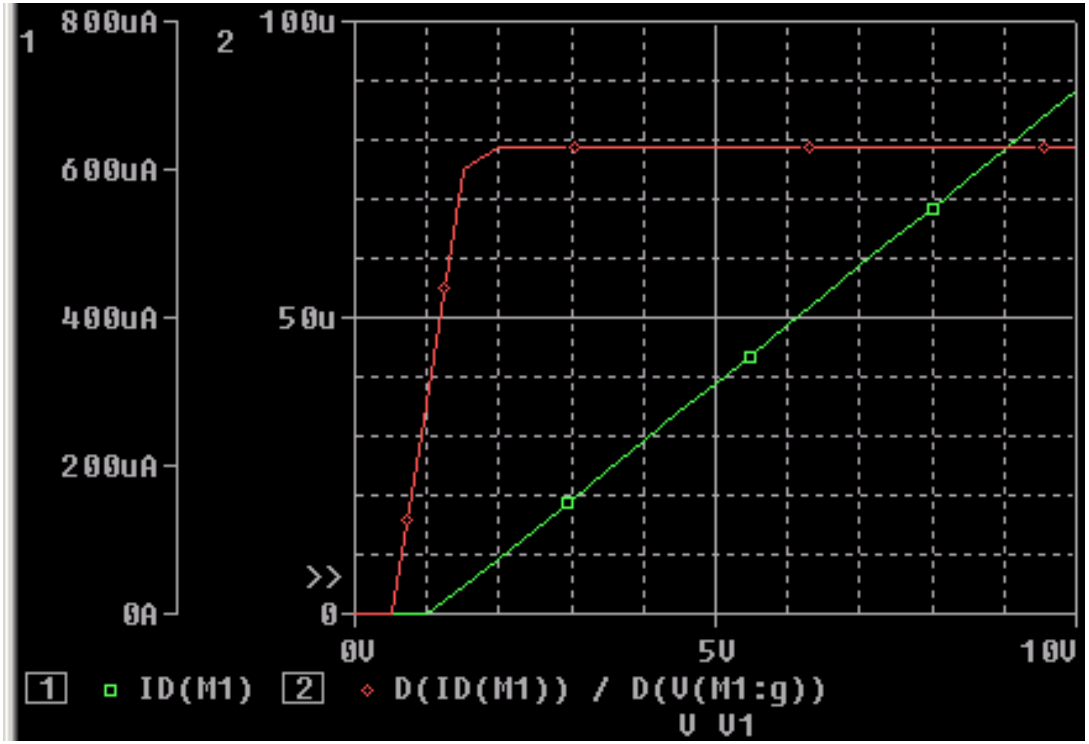


MEASURED SUPERIMPOSED ON LEVEL=7



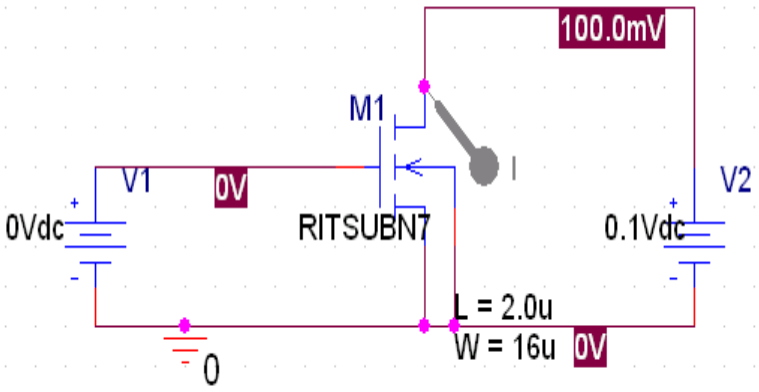
SIMULATION OF Ids – Vgs and gm

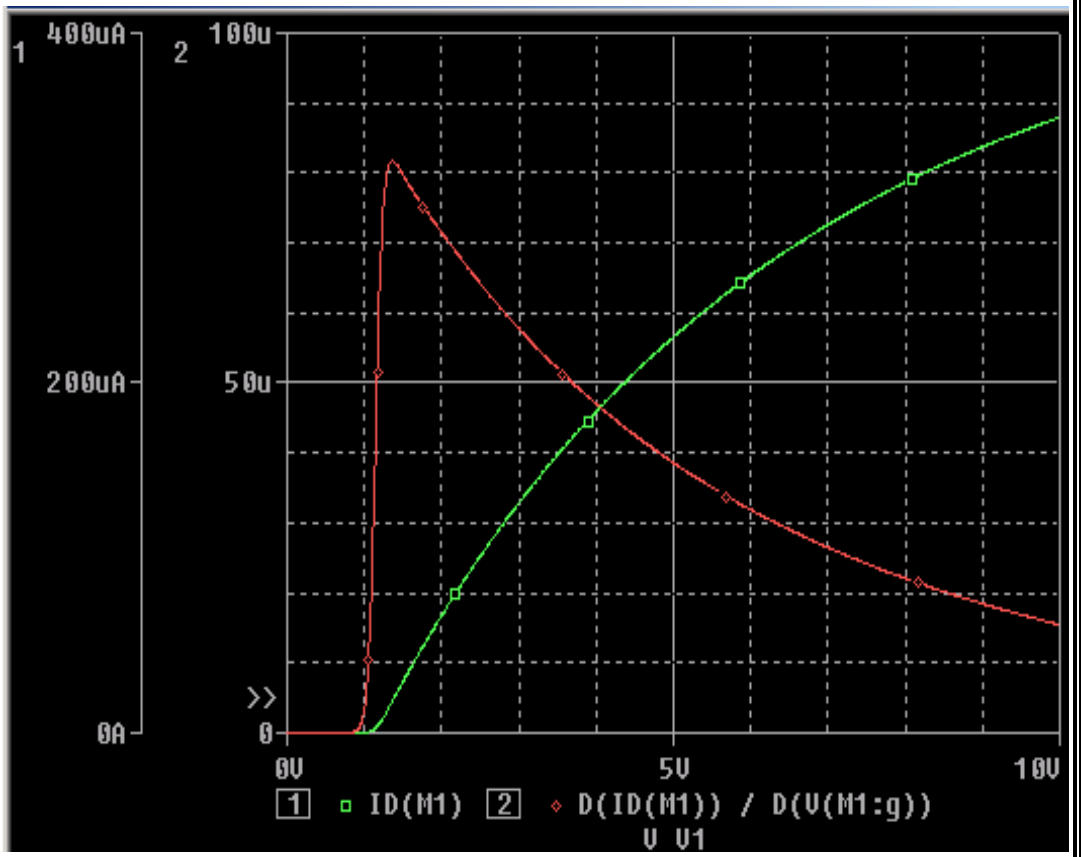




Using Level = 1 transistor models

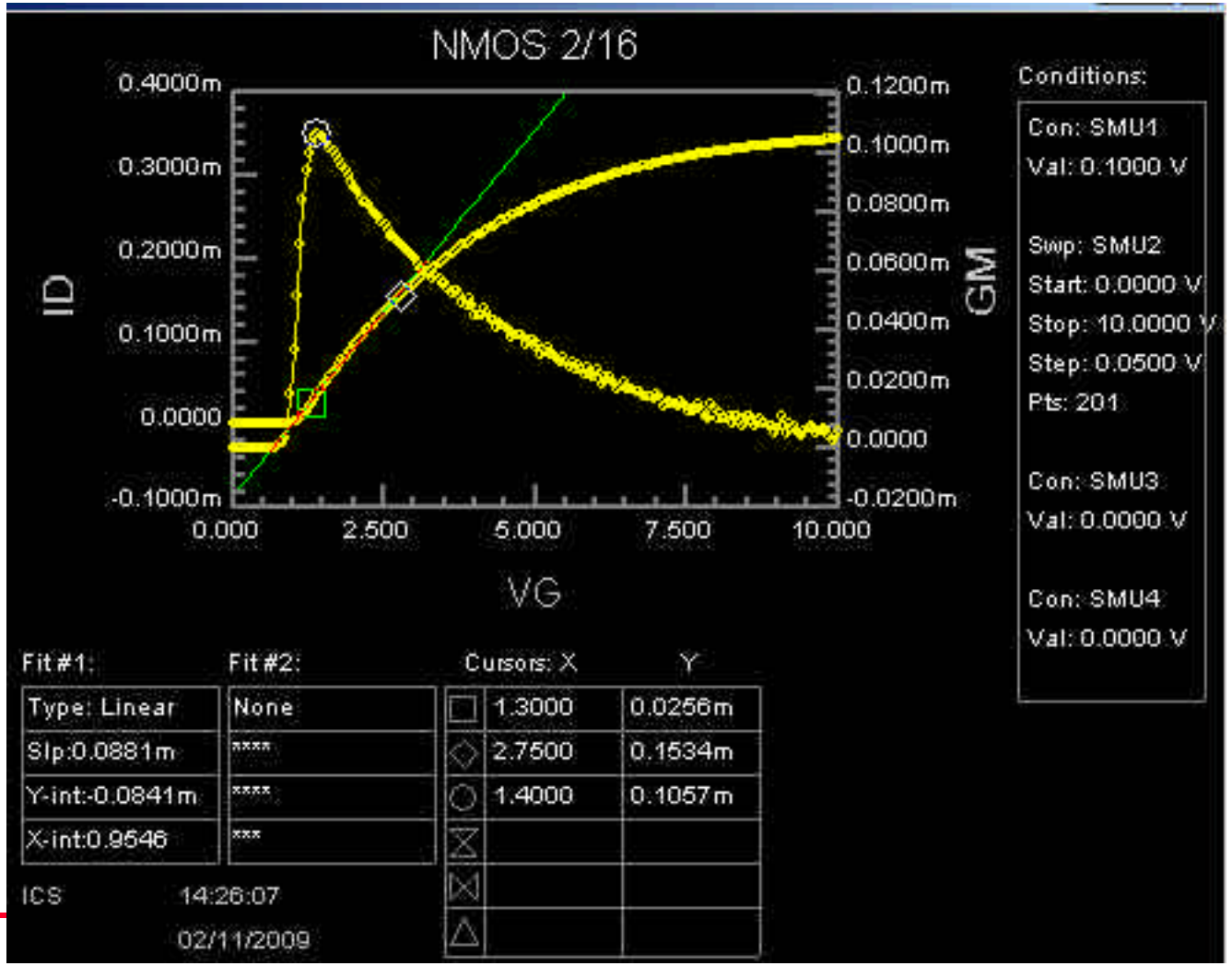
SIMULATION OF Ids – Vgs and gm



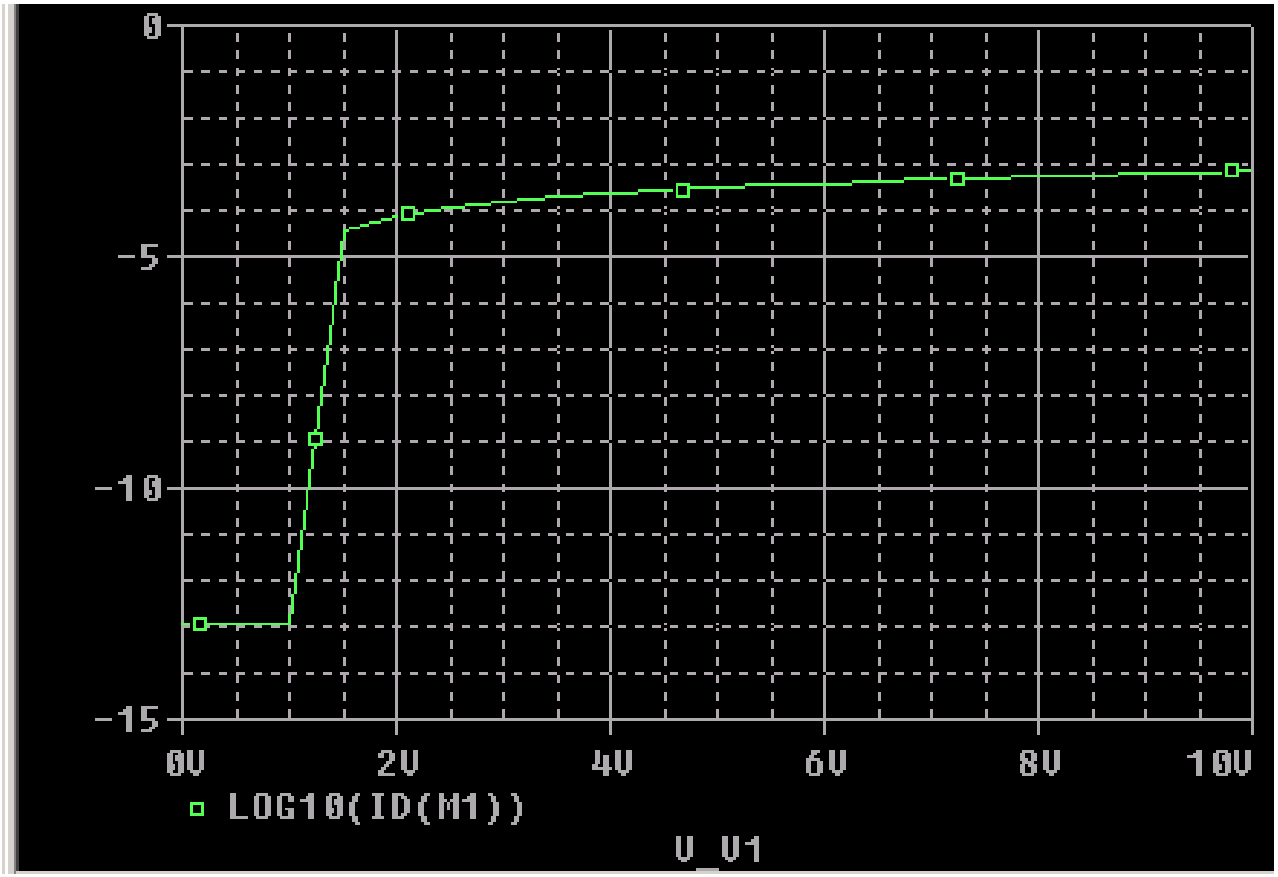


Using Level = 7 transistor models

MEASURED Ids – Vgs and gm

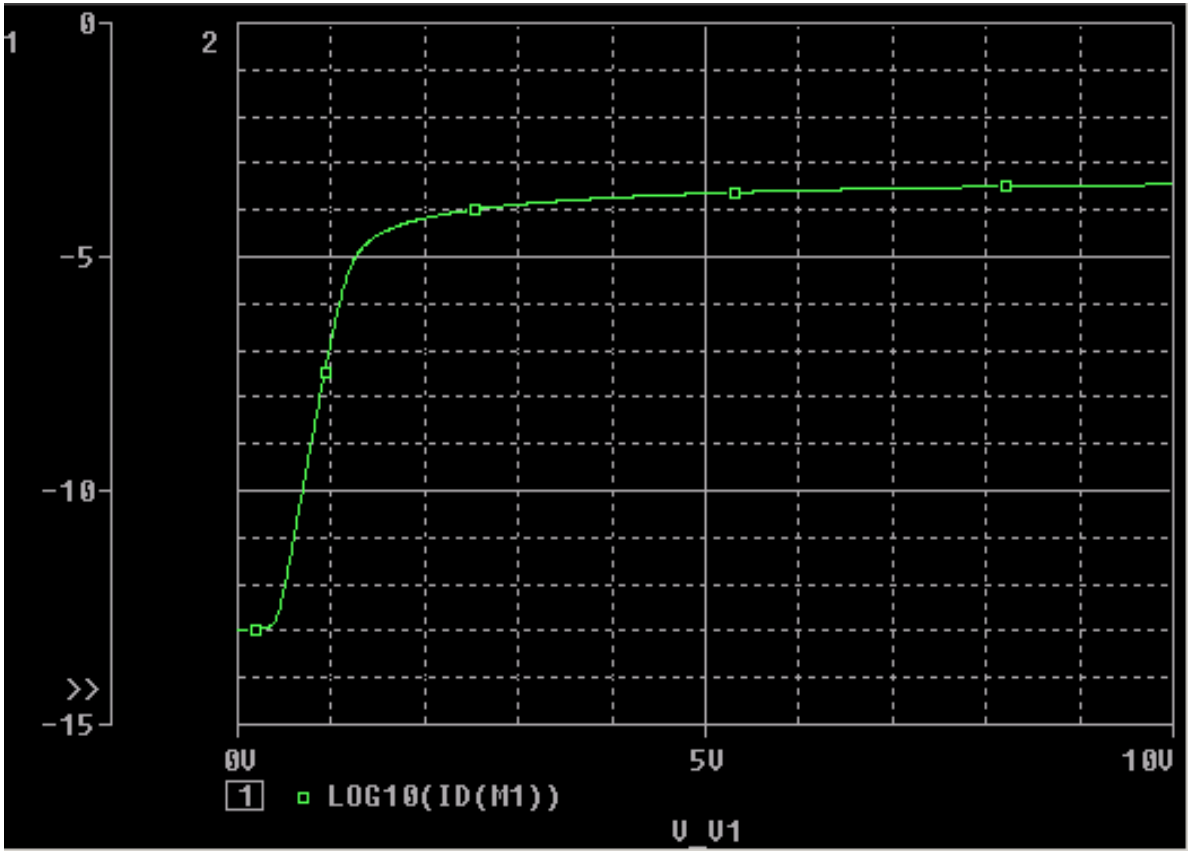


SIMULATION of Sub-Threshold Ids-Vgs Curve



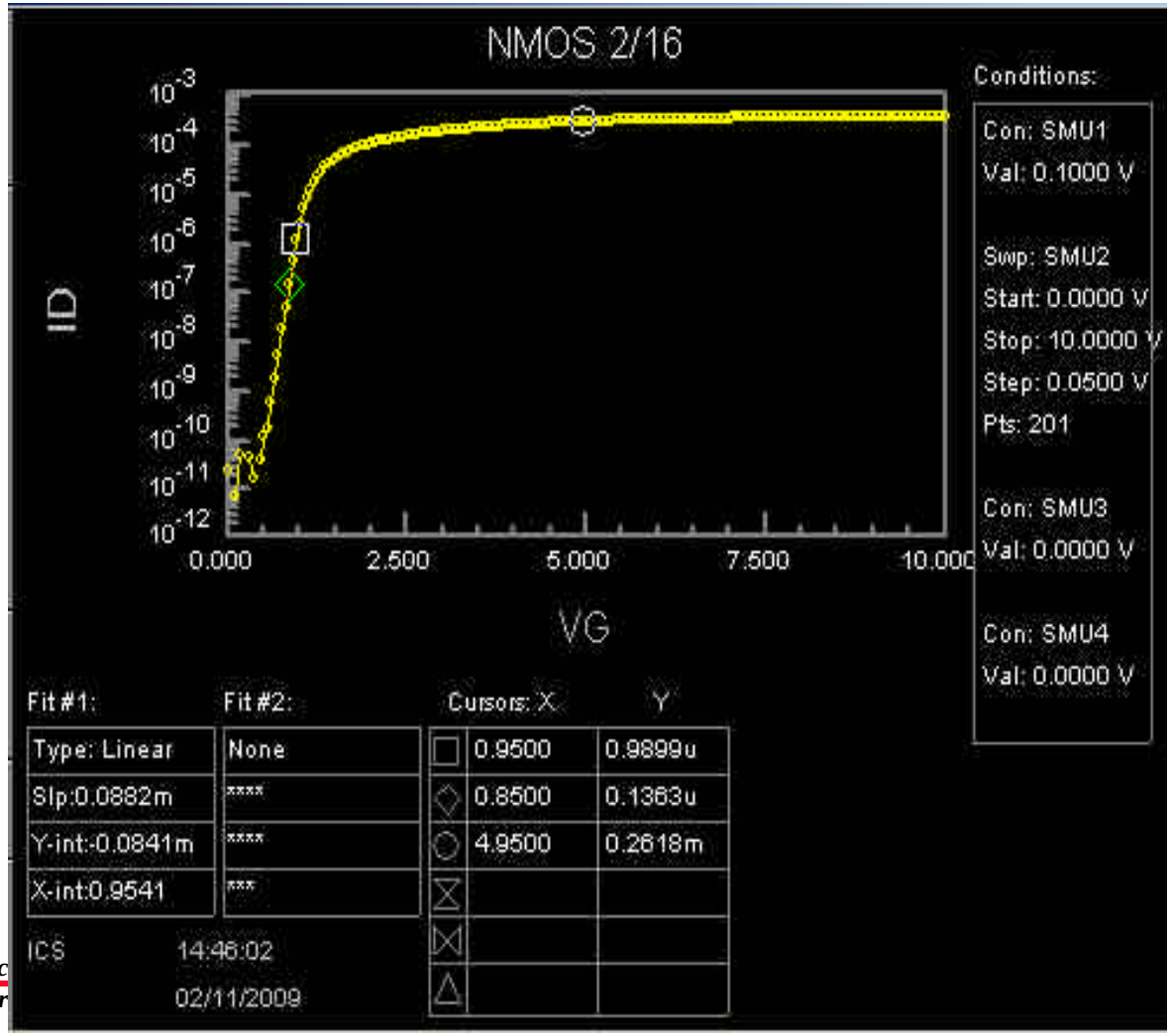
Using Level = 1 transistor models

SIMULATION of Sub-Threshold Ids-Vgs Curve



Using Level = 7 transistor models

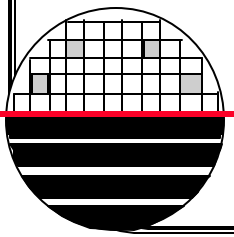
MEASURED Sub-Threshold Ids-Vgs Curve



MOSFET SPICE Models

*SPICE MODELS FOR RIT DEVICES - DR. LYNN FULLER 3-23-2009
*see: http://people.rit.edu/lffeee/SMFLCMOS.htm/
*
*LIST OF DEVICES/MODELS INCLUDED IN THIS LIBRARY
*
* RITPMOS49 LEVEL 49 MODEL FOR PMOSFET MADE IN RIT PMOS PROCESS
* RITSUBN1 LEVEL 1 MODEL FOR NMOSFET MADE IN RIT SUB-CMOS PROCESS
* RITSUBP1 LEVEL 1 MODEL FOR PMOSFET MADE IN RIT SUB-CMOS PROCESS
* RITSUBN3 LEVEL 3 MODEL FOR NMOSFET MADE IN RIT SUB-CMOS PROCESS
* RITSUBP3 LEVEL 3 MODEL FOR PMOSFET MADE IN RIT SUB-CMOS PROCESS
* RITSUBN7 LEVEL 7 MODEL FOR NMOSFET MADE IN RIT SUB-CMOS PROCESS
* RITSUBP7 LEVEL 7 MODEL FOR PMOSFET MADE IN RIT SUB-CMOS PROCESS
* RITSMFLN49 LEVEL 49 MODEL FOR NMOSFET MADE IN RIT SMFL-CMOS PROCESS by ROB SAXER
* RITSMFLP49 LEVEL 49 MODEL FOR PMOSFET MADE IN RIT SMFL-CMOS PROCESS BY ROB SAXER
* CMOSN LEVEL 2 MODEL FOR NMOSFET ORBIT SEMICONDUCTOR
* CMOSP LEVEL 2 MODEL FOR PMOSFET ORBIT SEMICONDUCTOR

see: http://people.rit.edu/lffeee/SMFLCMOS.htm/



LEVEL = 1

```
*2-15-2009
.MODEL RITSUBN1 NMOS (LEVEL=1
+VTO=1.0 LAMBDA= 0.031 PB=0.95 CGSO=3.4E-10 CGDO=3.4E-10
+CGBO=5.75E-10 RSH=1082 CJ=6.8e-4 MJ=0.5  CJSW=1.26e-10
+MJSW=0.5 JS=3.23e-8 TOX=150E-10  NSUB=1.45e17  NSS=3E11
+TPG=+1 XJ=0.18U LD=0.15U UO=363)
*
*2-15-2009
*.MODEL RITSUBP1 PMOS (LEVEL=1
*+VTO=-1.0 LAMBDA= 0.05 PB=0.94 CGSO=5.08E-10 CGDO=5.08E-10
*+CGBO=5.75E-10 RSH=33.7 CJ=5.01e-4 MJ=0.5  CJSW=1.38e-10
*+MJSW=0.5 JS=6.43e-8 TOX=150E-10  NSUB=7.23e16  NSS=1E11
*+TPG=-1 XJ=0.28U LD=0.22U UO=463)
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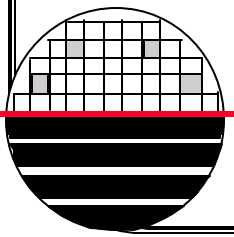
see: http://people.rit.edu/lffeee/SMFLCMOS.htm/



LEVEL = 2

```
*From Dr. Pearson's VLSI Class
*SPICE Level 2 Parameters for Supertex's (formerly Orbit Semiconductor's)
*2.0um MOSIS SCNA20 Process (from N7CK production run)
*
.MODEL CMOSN NMOS LEVEL=2 PHI=0.7 TOX=4.08E-8 XJ=0.2 TPG=1
+VTO=0.8096 DELTA=4.586 LD=2.972E-7 KP=5.3532E-5
+UO=632.5 UEXP=0.1328 UCRIT=3.897E4 RSH=6.202
+GAMMA=0.5263 NSUB=5.977E15 NFS=5.925E11 VMAX=5.83E4
+LAMBDA=3.903E-2 CGDO=3.7731E-10 CGSO=3.7731E-10
+CGBO=3.4581E-10 CJ=1.3679E-4 MJ=0.63238 CJSW=5.1553E-10
+MJSW=0.26805 PB=0.4
*
.MODEL CMOSP PMOS LEVEL=2 PHI=0.7 TOX=4.08E-8 XJ=0.2 TPG=-1
+VTO=-0.8483 DELTA=1.952 LD=3.431E-7 KP=1.779E-5
+UO=210.2 UEXP=0.4659 UCRIT=1.324E5 RSH=0.10960
+GAMMA=0.5263 NSUB=5.977E15 NFS=5.925E11 VMAX=5.83E4
+LAMBDA=6.372E-2 CGDO=4.3558E-10 CGSO=4.3558E-10
+CGBO=3.5957E-10 CJ=3.1646E-4 MJ=0.59954 CJSW=3.4394E-10
+MJSW=0.21153 PB=0.9
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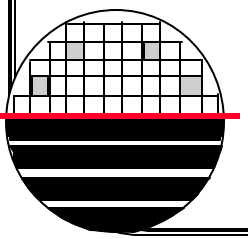
see: http://people.rit.edu/lffeee/SMFLCMOS.htm/



LEVEL = 2 FOR ALD1103

* From Electronics I EEEE481
.model EENMOS NMOS LEVEL=2
+VTO=0.7 KP=25E-6 LAMBDA=0.02 GAMMA=0.9
+TOX=90E-9 NSUB=3.7E15

see: http://people.rit.edu/lffeee/SMFLCMOS.htm/

ADVANCED LINEAR DEVICES, INC.

ALD1103

DUAL N-CHANNEL AND DUAL P-CHANNEL MATCHED MOSFET PAIR

GENERAL DESCRIPTION

The ALD1103 is a monolithic dual N-channel and dual P-channel matched transistor pair intended for a broad range of analog applications. These enhancement-mode transistors are manufactured with Advanced Linear Devices' enhanced ACMOS silicon gate CMOS process. It consists of an ALD1101 N-channel MOSFET pair and an ALD1102 P-channel MOSFET pair in one package.

The ALD1103 offers high input impedance and negative current temperature coefficient. The transistor pair is matched for minimum offset voltage and differential thermal response, and it is designed for precision signal switching and amplifying applications in +2V to +12V systems where low input bias current, low input capacitance and fast switching speed are desired. Since these are MOSFET devices, they feature very large (almost infinite) current gain in a low frequency, or near DC, operating environment. When used in pairs, a dual CMOS analog switch can be constructed. In addition, the ALD1103 is intended as a building block for differential amplifier input stages, transmission gates, and multiplexer applications.

The ALD1103 is suitable for use in precision applications which require very high current gain, beta, such as current mirrors and current sources. The high input impedance and the high DC current gain of the Field Effect Transistors result in extremely low current loss through the control gate. The DC current gain is limited by the gate input leakage current, which is specified at 50pA at room temperature. For example, DC beta of the device at a drain current of 5mA at 25°C is = 5mA/50pA = 100,000,000.

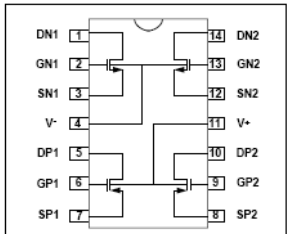
FEATURES

- Thermal tracking between N-channel and P-channel pairs
- Low threshold voltage of 0.7V for both N-channel & P-channel MOSFETS
- Low input capacitance
- Low Vos -- 10mV
- High input impedance -- $10^{15}\Omega$ typical
- Low input and output leakage currents
- Negative current (I_{DS}) temperature coefficient
- Enhancement mode (normally off)
- DC current gain 10^{8}
- Matched N-channel and matched P-channel in one package

APPLICATIONS

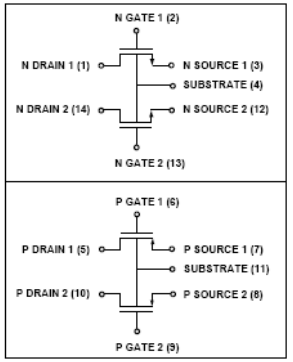
- Precision current mirrors
- Complementary push-pull linear drives
- Analog switches
- Choppers
- Differential amplifier input stage
- Voltage comparator
- Data converters
- Sample and Hold
- Analog inverter
- Precision matched current sources

PIN CONFIGURATION



DB, PB, SB PACKAGE

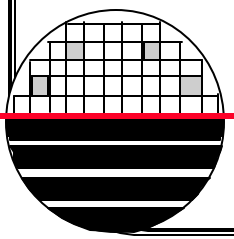
BLOCK DIAGRAM



ORDERING INFORMATION

Operating Temperature Range*		
-55°C to +125°C	0°C to +70°C	0°C to +70°C
14-Pin CERDIP Package	14-Pin Plastic Dip Package	14-Pin SOIC Package
ALD1103 DB	ALD1103 PB	ALD1103 SB

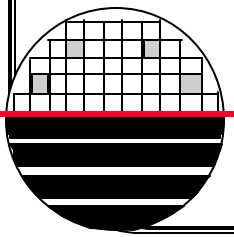
* Contact factory for industrial temperature range.



LEVEL = 3

```
*1-15-2007 FROM DR. FULLER'S SPREAD SHEET
*.MODEL RITSUBN3 NMOS (LEVEL=3
*+TPG=1 TOX=1.5E-8 LD=2.95E-7 WD=3.00E-7
*+UO= 726 VTO=1.0 THETA=0.349 RS=27 RD=27 DELTA=2.27 NSUB=1.45E17
*+XJ=1.84E-7 VMAX=1.10E7 ETA=0.837 KAPPA=0.508 NFS=3E11
*+CGSO=3.4E-10 CGDO=3.48E-10 CGBO=5.75E-10 PB=0.95 XQC=0.4)
*
*1-17-2007 FROM DR. FULLER'S SPREAD SHEET
*.MODEL RITSUBP3 PMOS (LEVEL=3
*+TPG=-1 TOX=1.5E-8 LD=3.61E-7 WD=3E-7
*+UO=377 VT0=-1.0 THETA=0.237 RS=33.7 RD=33.7 DELTA=2.35 NSUB=7.12E16
*+XJ=2.26E-7 VMAX=6.56E6 ETA=0.762 KAPPA=4.481 NFS=3E11
*+CGSO=4.15E-10 CGDO=4.15E-10 CGBO=5.75E-10 PB=0.94 XQC=0.40)
```

see: http://people.rit.edu/lffeee/SMFLCMOS.htm/



LEVEL = 7

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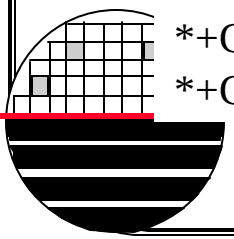
+TOX=1.5E-8 XJ=1.84E-7 NCH=1.45E17 NSUB=5.33E16 XT=8.66E-8 NSS=3E11
*+XWREF=2.0E-7 XLREF=2.95E-7
+VTH0=1.0 U0= 600 WINT=2.0E-7 LINT=1E-7
+NGATE=5E20 RSH=1082 JS=3.23E-8 JSW=3.23E-8 CJ=6.8E-4 MJ=0.5 PB=0.95
+CJSW=1.26E-10 MJSW=0.5 PBSW=0.95 PCLM=5
+CGSO=3.4E-10 CGDO=3.4E-10 CGBO=5.75E-10)
*
*1-17-2007
*.MODEL RITSUBP7 PMOS (LEVEL=7
*+VERSION=3.1 CAPMOD=2 MOBMOD=1
*+TOX=1.5E-8 XJ=2.26E-7 NCH=7.12E16 NSUB=3.16E16 XT=8.66E-8 NSS=3E11 PCLM=5
*+XWREF= 2.0E-7 XLREF=3.61E-7
*+VTH0=-1.0 U0= 376.72 WINT=2.0E-7 LINT=2.26E-7 NGATE=5E20
*+RSH=1347 JS=3.51E-8 JSW=3.51E-8 CJ=5.28E-4 MJ=0.5 PB=0.94
*+CJSW=1.19E-10 MJSW=0.5 PBSW=0.94
*+CGS0=4.5E-10 CGD0=4.5E-10 CGB0=5.75E-10)
```

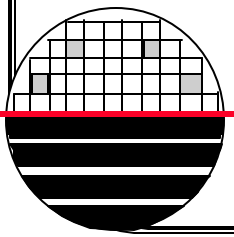
see: http://people.rit.edu/lffeee/SMFLCMOS.htm/



LEVEL = 49

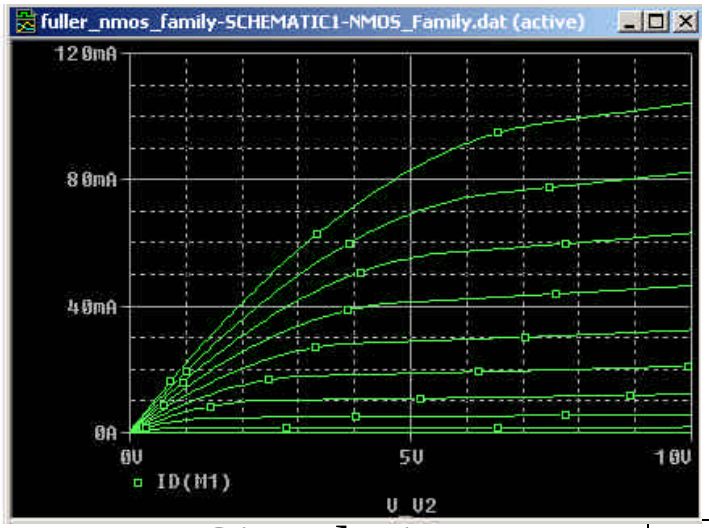
```
*1-15-2007 FROM DR. FULLER'S SPREADSHEET
.MODEL RITSUBN49 NMOS (LEVEL=49 VERSION=3.1 CAPMOD=2 MOBMOD=1
+TOX=1.5E-8 XJ=1.84E-7 NCH=1.45E17 NSUB=5.33E16 XT=8.66E-8 NSS=3E11
+XWREF=2.0E-7 XLREF=2.95E-7 VTH0=0.5 U0= 950 WINT=2.0E-7 LINT=1.84E-7
+NGATE=5E20 RSH=1082 JS=3.23E-8 JSW=3.23E-8 CJ=6.8E-4 MJ=0.5 PB=0.95
+CJSW=1.26E-10 MJSW=0.5 PBSW=0.95 PCLM=5
+CGS0=3.4E-10 CGD0=3.4E-10 CGB0=5.75E-10)
*
*1-17-2007 FROM DR. FULLER'S SPREADSHEET
.MODEL RITSUBP49 PMOS (LEVEL=49 VERSION=3.1 CAPMOD=2 MOBMOD=1
+TOX=1.5E-8 XJ=2.26E-7 NCH=7.12E16 NSUB=3.16E16 XT=8.66E-8 NSS=3E11 PCLM=5
+XWREF= 2.0E-7 XLREF=3.61E-7 VTH0=-1.22 U0= 376.72 WINT=2.0E-7 LINT=2.26E-7
+RSH=1347 JS=3.51E-8 JSW=3.51E-8 CJ=5.28E-4 MJ=0.5 PB=0.94
+CJSW=1.19E-10 MJSW=0.5 PBSW=0.94 NGATE=5E20
+CGS0=4.5E-10 CGD0=4.5E-10 CGB0=5.75E-10)
```

see: http://people.rit.edu/lffeee/SMFLCMOS.htm/

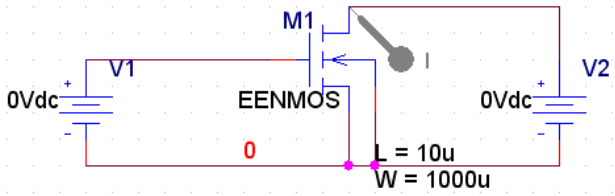


ALD1103

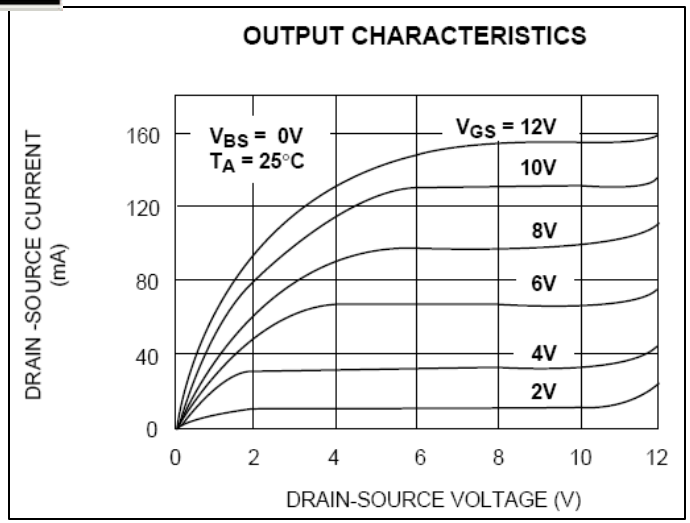
```
        NMOS
LEVEL     2
    L   100.000000E-06
    W   100.000000E-06
  VTO     .7
   KP   25.000000E-06
GAMMA     .9
  PHI     .644002
LAMBDA    .02
   IS   10.000000E-15
   JS    0
   PB     .8
 PBSW     .8
   CJ   195.914300E-06
  CJSW    0
  CGSO    0
  CGDO    0
  CGBO    0
 NSUB     3.700000E+15
  TOX   90.000000E-09
   XJ    0
UCRIT    10.000000E+03
DIOMOD    1
  VFB     0
 LETA     0
 WETA     0
  UO      0
 TEMP     0
  VDD     0
XPART     0
```



From Simulation Given model on left with L=10u and W=1000u



From Data Sheets



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5. ATLAS USERS Manual, From Silvaco International.
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