SIMULATION ELECTRIQUE DES CIRCUITS INTEGRES:
Modélisation et simulation des circuits CMOS

par

Pr. Gaston CAMBON

UNIVERSITE MONTPELLIER II
POLYTECH ' MONTPELLIER

Tel: 04 67 41 85 01
Fax: 04 67 41 85 00
Mel: cambon@lirmm.fr

INTRODUCTION: OUTILS de CAO
Conception Assistée par Ordinateur

SCHEMATIQUE
SPECIFICATION (VHDL…C…C++)

SIMULATEURS (logiques, analogiques….)

SYNTHESE AUTOMATIQUE
DESSIN (cartes, circuits intégrés…)
VERIFICATEURS DE REGLES
TEST – TESTABILITE
PREPARATION DE LA FABRICATION (« back-end »
……

LES DIFFERENTS TYPES DE **SIMULATEURS**
MODELES DE SIMULATION

- **COMPORTEMENTAL**: niveau système
  - VHDL (logique)
  - VHDL_AMS (logique/analogique)

-LOGIQUE : circuits logiques
  - modèles structurels (VHDL)
  - niveaux: 0 1 X Z ……

-ELECTRIQUE: circuits analogiques
  - modèles structurels
  - niveaux: continuum de V et I

SIMULATION ELECTRIQUE

SIMULATEUR **SPICE** (pSpice, hSpice..Eldo, Spectre…)

MODES DE SIMULATION

-REGIME CONTINU : circuits linéaires et non linéaires

- point de polarisation
- courbe de transfert

-DOMAINE FREQUENTIEL: circuits linéaires

- diagramme de BODE
- bruit

-DOMAINE TEMPOREL: circuits linéaires et non linéaires

- retards
- distorsion – analyse de FOURIER

……..

- MONTE CARLO: analyses statistiques

SIMULATION ELECTRIQUE
MODELES STRUCTURELS: PRIMITIVES

-R, L, C, ……transformateurs
- Sources indépendantes: V, I
  - continues
  - fréquentielles (amplitude, phase)
  - temporelles (impulsions, sinusoïdes,..)
-Sources dépendantes: V, I
  - gain, transconductance….
-lignes de transmission : avec ou sans pertes
-Diodes, Transistors bipolaires, MOS, FET
-Amplificateurs Opérationnels
-……
-……en fonction de la TEMPERATURE

SIMULATION ELECTRIQUE
MODELE VIRTUEL

PHYSIQUE

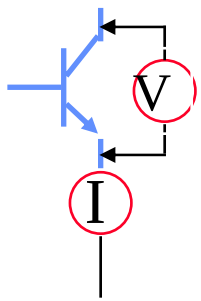
MESURES
caractérisation

MODÈLE

EQUATIONS | PARAMÈTRES

p
n

I=Is(exp(... β=150



SIMULATEUR
MODÈLE "INFORMATIQUE"

Stimulis

Résultats

si V > Vt alors...
sinon...

SIMULATEUR ELECTRIQUE

Eléments du langage de description

Description qualitative des algorithmes de simulation

Simulateurs "de type" SPICE

SIMULATEUR **HSPICE**

Fichier de simulation: xxxx.sp

Titre		
*commentaire		
.model…….	)	paramètres
+suite instruction	)	
.model…….	)	des modèles
…….		
Rxx ……..	)	description
Vxx ……...	)	du circuit
Qxx ……	)	
……		
.DC ……..	)	commandes
.AC ……..	)	de simulation
.TR ……	)	
…..		
.PROBE	)	stockage des résultats
.END	)	fin

SIMULATEUR **HSPICE**
Eléments du langage

Multiplicateurs d'unités

F	femto
P	pico
N	nano
U	micro
M	milli
K	kilo
MEG	méga
G	giga
T	téra

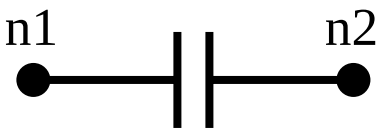
Exemples:

10kohms = 10k = 10 000
10mvolts = 10m = 0,001

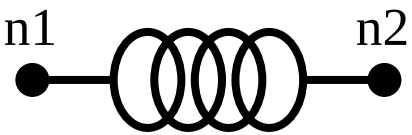
SIMULATEUR **HSPICE**

Description des composants passifs

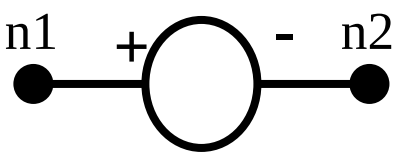
Rxx n1 n2 valeur



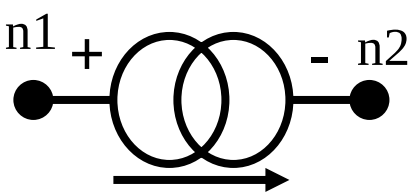
Cxx n1 n2 valeur



Lxx n1 n2 valeur

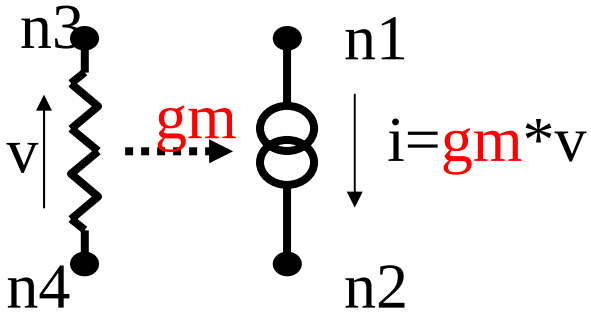


Vxx n1 n2 <DC> valeur

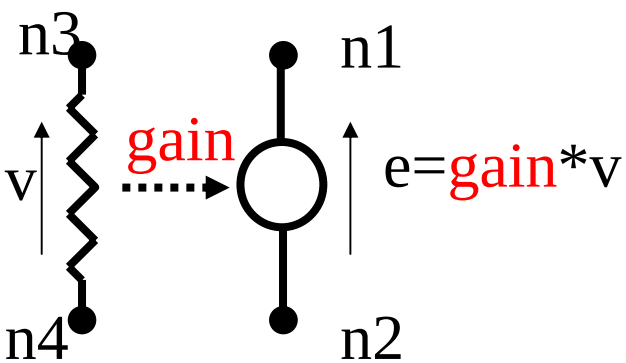


Ixx n1 n2 <DC> valeur

SIMULATEUR **HSPICE**
modélisation d'éléments actifs



Gxx n1 n2 n3 n4 gm



Exx n1 n2 n3 n4 gain

Fxx n1 n2 n3 n4 gain_courant

Hxx n1 n2 n3 n4 transrésistance

SIMULATEUR **HSPICE**

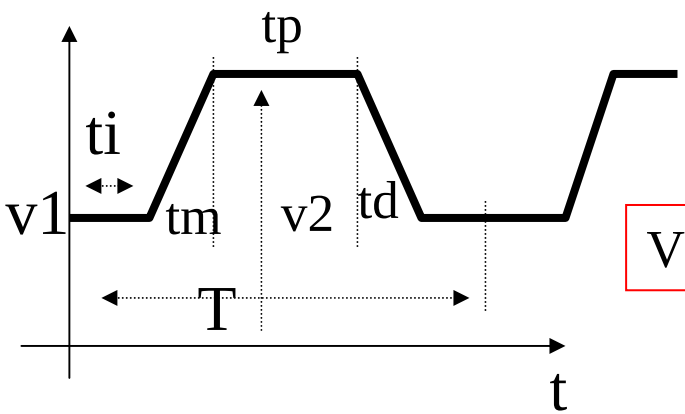
sources sinusoïdales linéaires

Vxx n1 n2 <DC valeur> AC amplitude phase

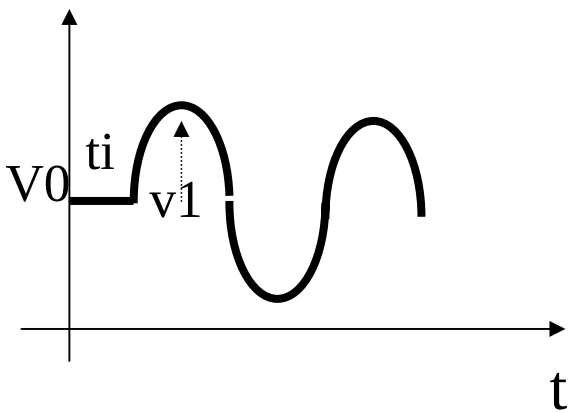
Ixx n1 n2 <DC valeur> AC amplitude phase

variation

SIMULATEUR **HSPICE**
sources dépendant du temps



Vxx n1 n2 <DC val> PULSE (v1 v2 ti tm td tp <T>)



Vxx n1 n2 SIN(v0 v1 fréq <ti> <a> <phase>

SIMULATEUR **HSPICE**
Commandes de simulation

.OP (point de polarisation)

.DC Vxxx Vmin Vmax ΔV (courbe de transfert)
source
variable

.TF V(n1,n2) Vxx (gain en tension
sortie entrée r entrée
r sortie)

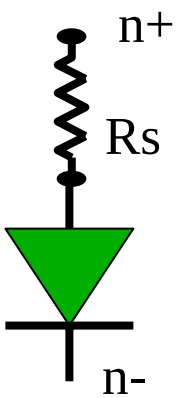
.TRAN δt tstop (analyse temporelle)

.AC DEC nb_pts/dec fmin fmax (analyse fréquentielle)
.AC LIN nb_pts fmin fmax

.TEMP T1 T2 T3 (analyses a différentes températures)

SIMULATEUR **SPICE**

Modèle de la Diode pn: quelques paramètres



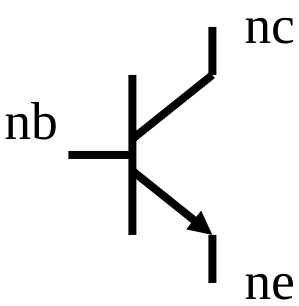
Dxx n+ n- nom_modèle <aire>

.model nom_modèle D <paramètre=valeur > …..

paramètre		valeur défaut	ex
Is	courant de saturation	1e-14	1e-15
N	coéfficient émission	1	1.5
Ikf	fort courant	infini	100mA
Bv	tension claquage	infini	50V
Rs	résistance parasite	0	100ohms
TT	temps de transit	0	100pS
Cjo	capa jonction 0V	0	1pF
Vj	potentiel jonction	1	0.7V

SIMULATEUR **SPICE**

Modèle du transistor bipolaire: quelques paramètres



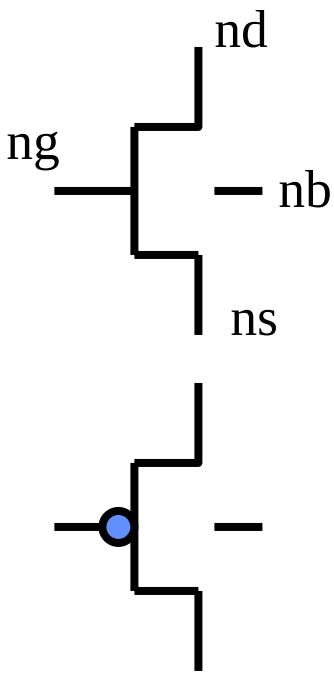
Qxxx nc nb ne nom_modèle

.model nom_modèle [NPN/PNP] <param=valeur> ….

Param		defaut	ex.
Is	courant de saturation	1e-16	1e-16
Bf	gain en courant	100	100
Vaf	tension d'Early	infini	100V
Ikf	fort courant	infini	10mA
Rb	résistance base	0	200
Cje	capa E-B	0	1pF
Cjc	capa B-C	0	2pF
Tf	temps de transit	0	20pS

SIMULATEUR **SPICE**

Modèle du transistor MOS: quelques paramètres



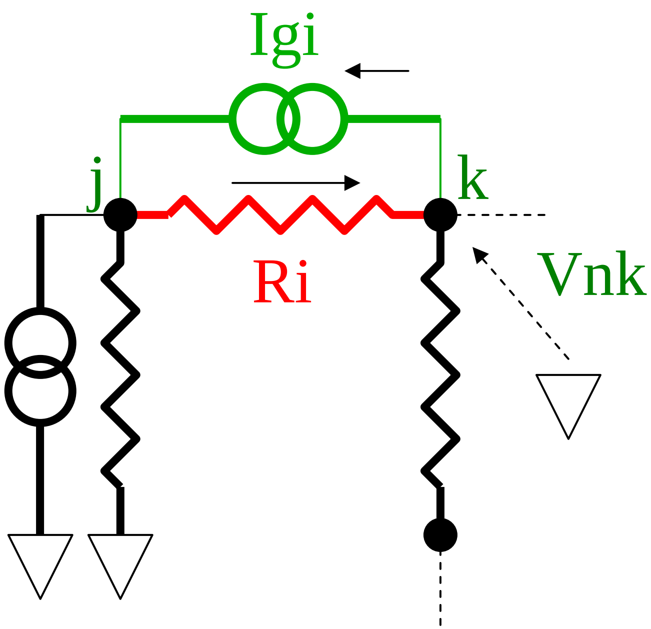
Mxxx nd ng ns nb nom_modèle W=… L=…. ……

.model nom_modèle [NMOS / PMOS] Level=1 <param=…>

param.		Défaut	ex
Vto	tension de seuil	0	0.5 (+-)
Kp	param. Transconductance	2e-5	2e-5
Lambda	modulation L	0	0.02
Gamma	effet substrat		0.5
Tox	épaisseur oxyde grille		10nm
Nsub	dopage substrat		30e15/cm^3

SIMULATION ELECTRIQUE

Régime continu: algorithme de simulation de circuits linéaires



Méthode Nodale

[Yn] [Vn] = [Is]

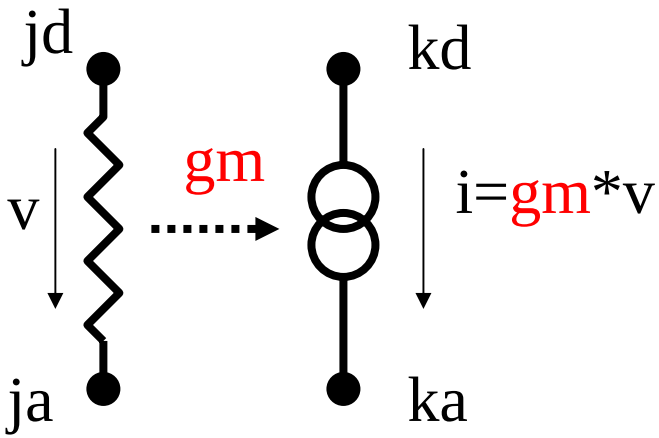
$$
\begin{array}{c}
\\ \\ j \\ \\ k \\ \\ \\
\end{array}
\begin{bmatrix}
\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \\
\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \\
\ldots +1/Ri \ldots\ldots -1/Ri \ldots \\
\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \\
\ldots -1/Ri \ldots\ldots +1/Ri \ldots \\
\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \\
\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots
\end{bmatrix}
\begin{bmatrix}
\ldots \\ \ldots \\ Vnj \\ \ldots \\ Vnk \\ \ldots \\ \ldots
\end{bmatrix}
=
\begin{bmatrix}
\ldots \\ \ldots \\ -Igi \\ \ldots \\ +Igi \\ \ldots \\ \ldots
\end{bmatrix}
$$

j k

SIMULATION ELECTRIQUE

Régime continu: algorithme de simulation de circuits linéaires

Transconductance



[Yn]

	jd	ja
	.....	.....
kd	…+ gm…….- gm ...	.....
ka	….- gm…….+ gm ..	.....
	.....	.....

SIMULATION ELECTRIQUE

Régime continu: algorithme de simulation de circuits linéaires

Description de la structure du circuit

↓

Analyse de la description

↓

Système numérique d'équations : [Yn] [Vn] = [Is]

↓

Résolution numérique du système: méthode du pivot + …

↓

Résultats: Vn1, Vn2,….Vnj….VnN

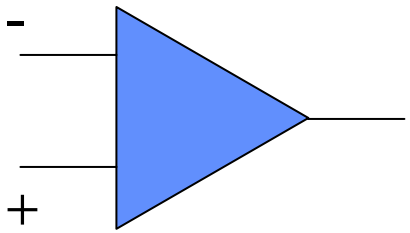
↓

Calcul des courants

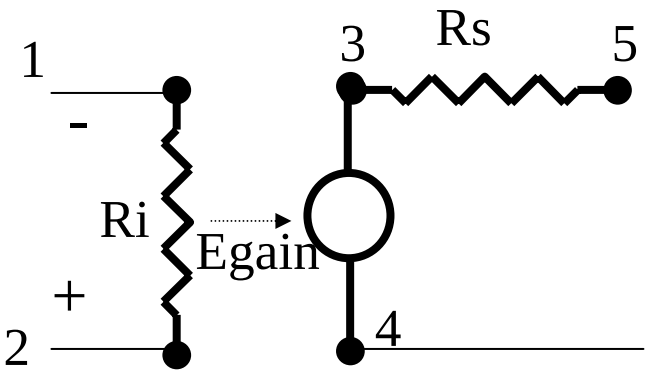
↓

……

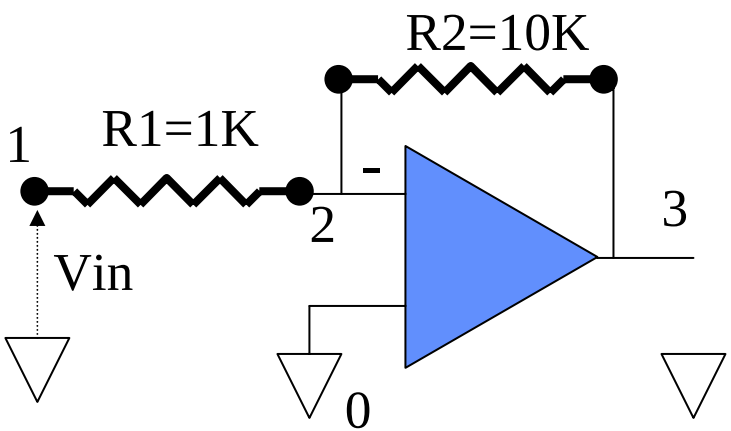
SIMULATION ELECTRIQUE
Exemple: modélisation d'un circuit **linéaire**
Amplificateur Opérationnel




```
Ri 1 2  500K
Egain  3 4 2 1 1e5
Rs  3  5  500
```




```
*macrocomposant
.subckt ampliop 1 2 5 4
Ri 1 2 500K
Egain 3 4 2 1 1e5
Rs 3 5 500
.ends
……
*appel sous-circuit
Xampli 2 0 3 0 ampliop
R1 1 2 1K
R2 2 3 10K
……
```



Exercice: simuler la courbe de transfert de l'amplificateur ci-contre

SIMULATION ELECTRIQUE
Domaine fréquentiel: simulation de circuits linéaires

[Yn (ω)] * [Vn (ω)] = [Is (ω)]

Admitances:
Termes complexes

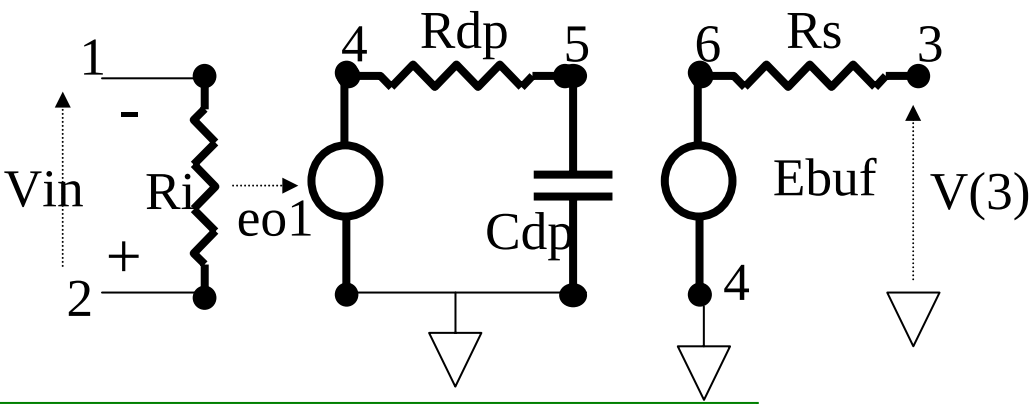
Module Vn (ω) Phase Vn(ω)
« Is (ω) « Is(ω)

```
…….
Vxx  n+  n-  DC  0     AC     1            0
*                                Amplitude  Phase
……….
.AC  DEC    10     fmin    fmax
```

SIMULATION ELECTRIQUE

Domaine fréquentiel: simulation de circuits linéaires

Modélisation d'un amplificateur opérationnel



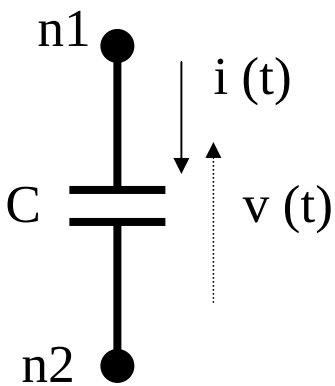
Exercice1:
Simuler l'amplificateur de gain 10
Tracer le diagramme de Bode (amplitude / phase)
Vérifier les résultats « à la main »

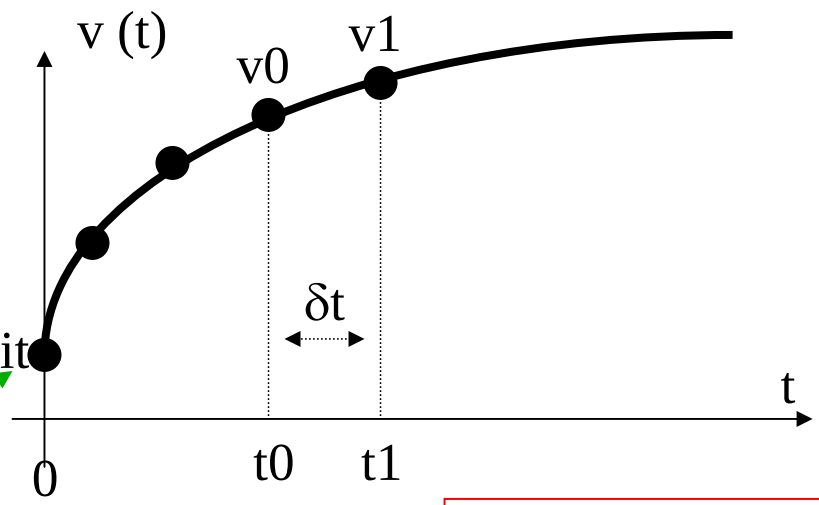
Exercice 2:
Simuler le filtre d'ordre 5 (description fournie)

```
Modele ampli op
*avec fréquence de coupure
*gain boucle ouverte G0= 200K
*produit gain*bande GB= 1 Mhz
*pole dominant a 5 Hz = GB/G0
*                = 1 / ( 2 π Cdp Rdp )
.subckt ampliop 1 2 3
*e-    e+    sortie
Rs 6 3 75
Ri 1 2 2meg
Eo1 4 0 2 1 200K
Rdp 4 5 1meg
Cdp 5 0 32nF
Ebuf 6 0 5 0 1
.ends amplop
……..
```

SIMULATION ELECTRIQUE

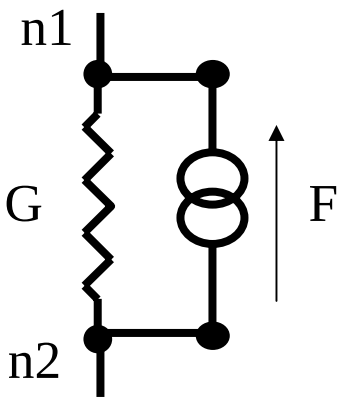
Domaine temporel: algorithme de simulation de circuits linéaires





Simulation DC

circuit équivalent à t1



$i(t) = C\,dv/dt \;\#\; C * (v1-v0) / (t1-t0)$

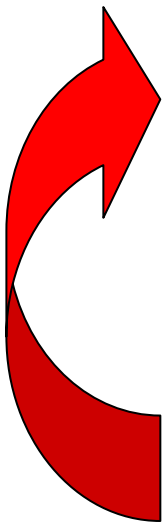
$\#\; C\,v1 / \delta t \; - C\,v0 / \delta t$

$i(t) = G\,v - F$

$G = C / \delta t \quad F = C\,v0 / \delta t$

SIMULATION ELECTRIQUE

Domaine temporel: algorithme de simulation de circuits linéaires



Point de fonctionnement à t=0 (simul. DC automatique (*)):

vinit

Pour chaque valeur de t (incrément δt)

- modèle équivalent des C, L …
- G ➔ [Yn] F ➔ [Is]
- résolution du système linéaire
- solution au temps t
- mémorisation du résultat à t

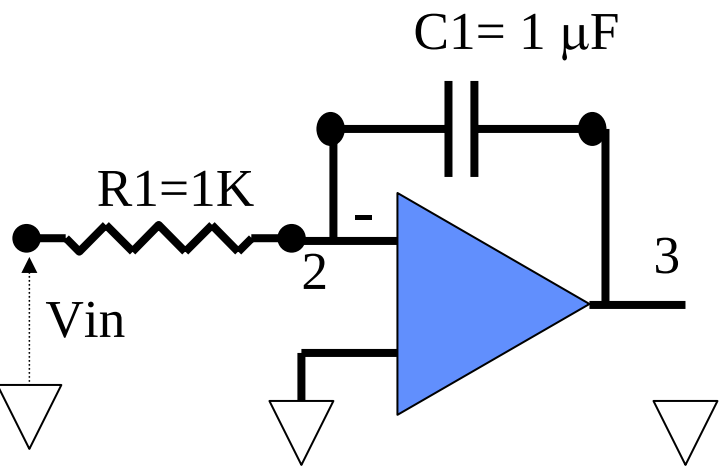
Fin itération

Tracé des courbes Vn(t)

(*): possibilité d'imposer des conditions initiales (Commande .IC)

SIMULATION ELECTRIQUE

Domaine temporel: exemples de simulation de circuits linéaires



Exercice:
Simuler l'intégrateur ci-contre
dans le domaine temporel

1 – vin est un train d'impulsions symétriques
de période T= 2 ms (temps de transition: 1 µs)
Valeur à t=0: 0 Volts
Valeur max: 1 Volt

2 – Valeur à t=0: -1 V
Valeur max: +1 V
?????????commenter!!!!!!!!!!!!

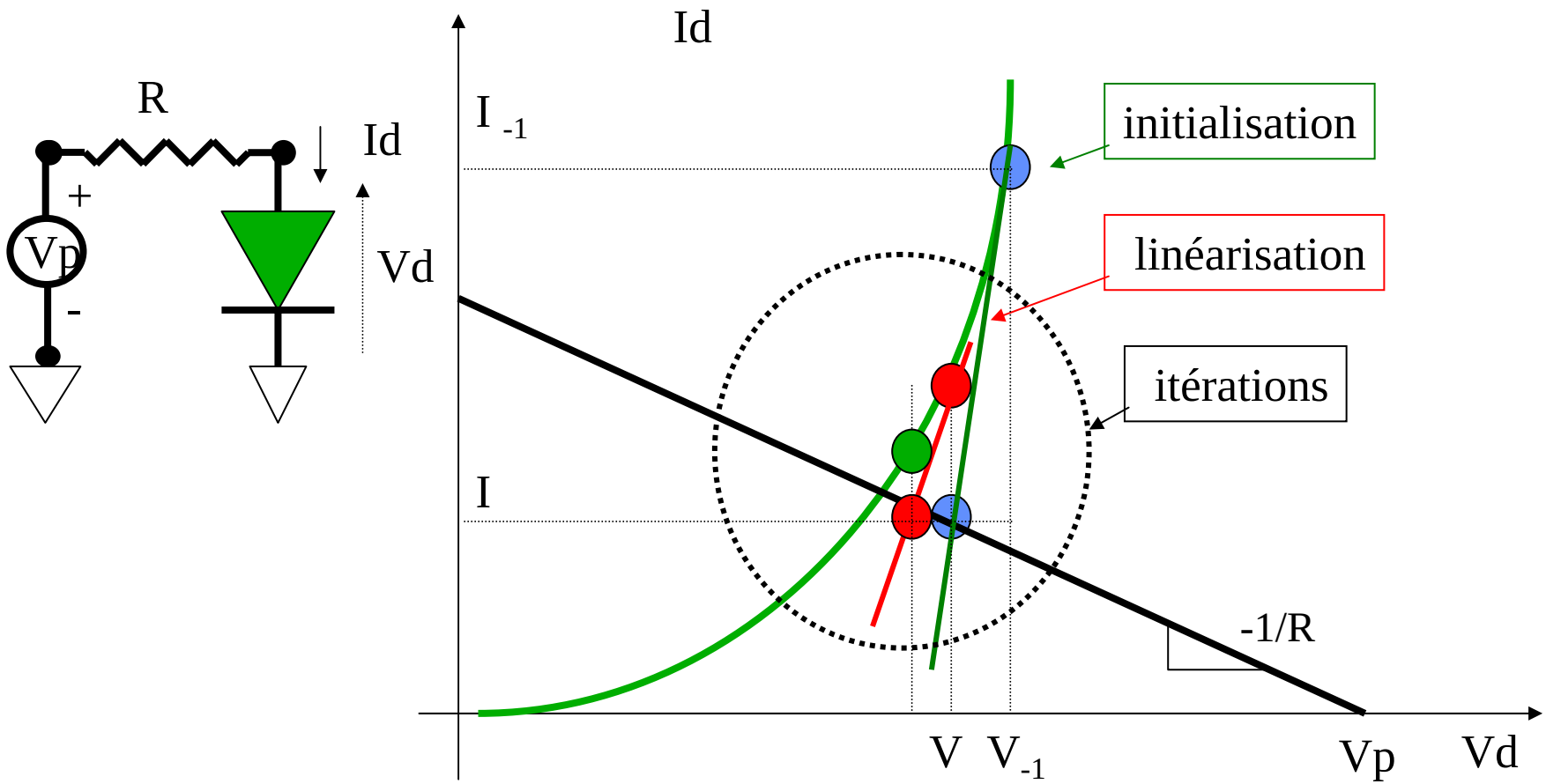
3 – commande d'initialisation
.IC V(x,y)= valeur V(x)= valeur ……

Faire une analyse de FOURIER sur les signaux

SIMULATION ELECTRIQUE

Régime continu: simulation de circuits **non-linéaires**

à partir d'un exemple



SIMULATION ELECTRIQUE

Régime continu: simulation de circuits **non-linéaires**

à partir d'un exemple

Modèle de la diode à jonction pn

$I = Is * \exp (q\ Vd / nkT)$

Dérivée

$d\ I/d\ Vd = Is * q / (nkT) * \exp (q\ Vd/ nkT) \# (I – I_{-1}) * q/(nkT)$

Linéarisation

$I \# I_{-1} + (d\ I / d\ Vd) * (V - V_{-1})$ (développement de Taylor ordre 1)

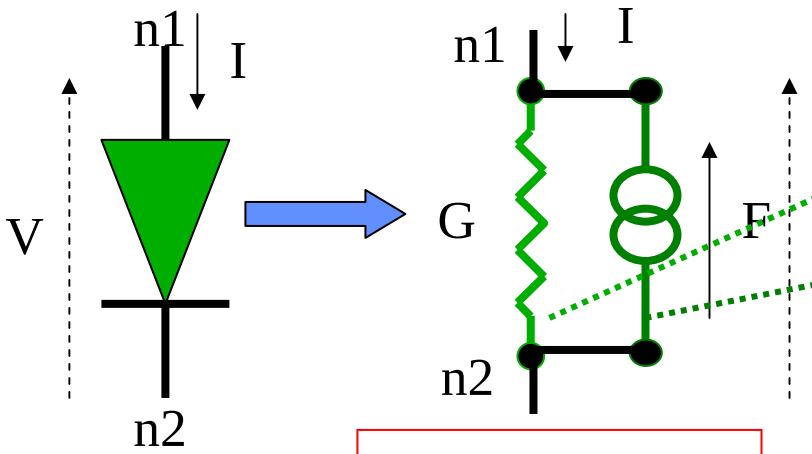
$I \# \underbrace{q/(nkT) * (I_{-1} + Is)}_{G} * V – \underbrace{\{q/(nkT) * (I_{-1} + Is) * V_{-1} - I_{-1}\}}_{F}$

$I \# G * V - F$

SIMULATION ELECTRIQUE

Régime continu: simulation de circuits **non-linéaires**

à partir d'un exemple



modèle linéarisé
en I_{-1} , V_{-1}

$$[\ Yn\ ]\ [\ Vn\ ] = [\ Is\ ]$$

Algorithme

Itération jusqu'à convergence (*)
- recalcule G et F
- résoud le système linéaire
- solution intermédiaire
- compare au modèle réel

Fin itération
- solution (ou non convergence)

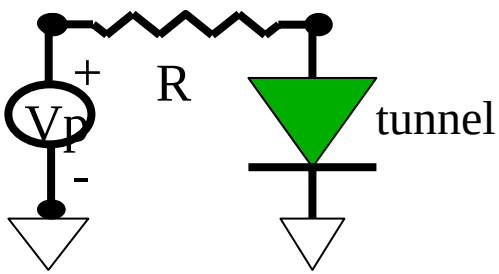
(*) Convergence= les valeurs (I,V) trouvées lors de l'itération vérifient à un epsilon près les équations du modèle réel (non-linéaire)

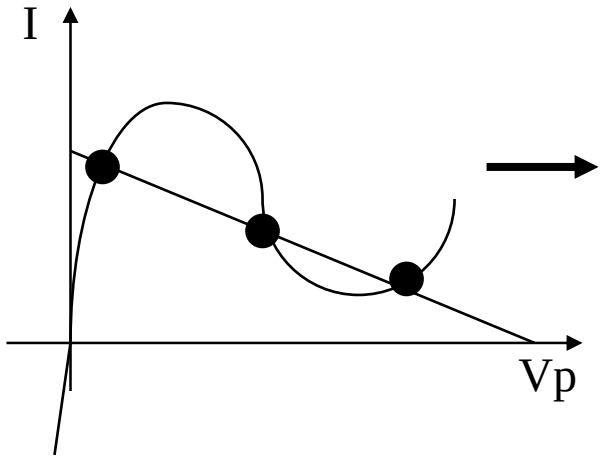
SIMULATION ELECTRIQUE

Régime continu: simulation de circuits **non-linéaires**

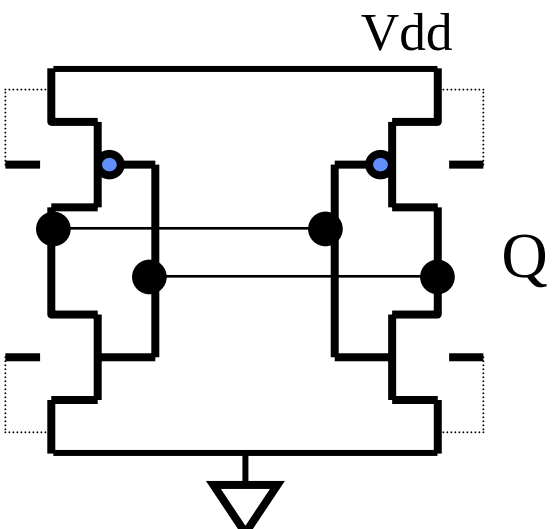
Cas de non-convergence – Plusieurs points stables

Oscillateur: pas de point stable





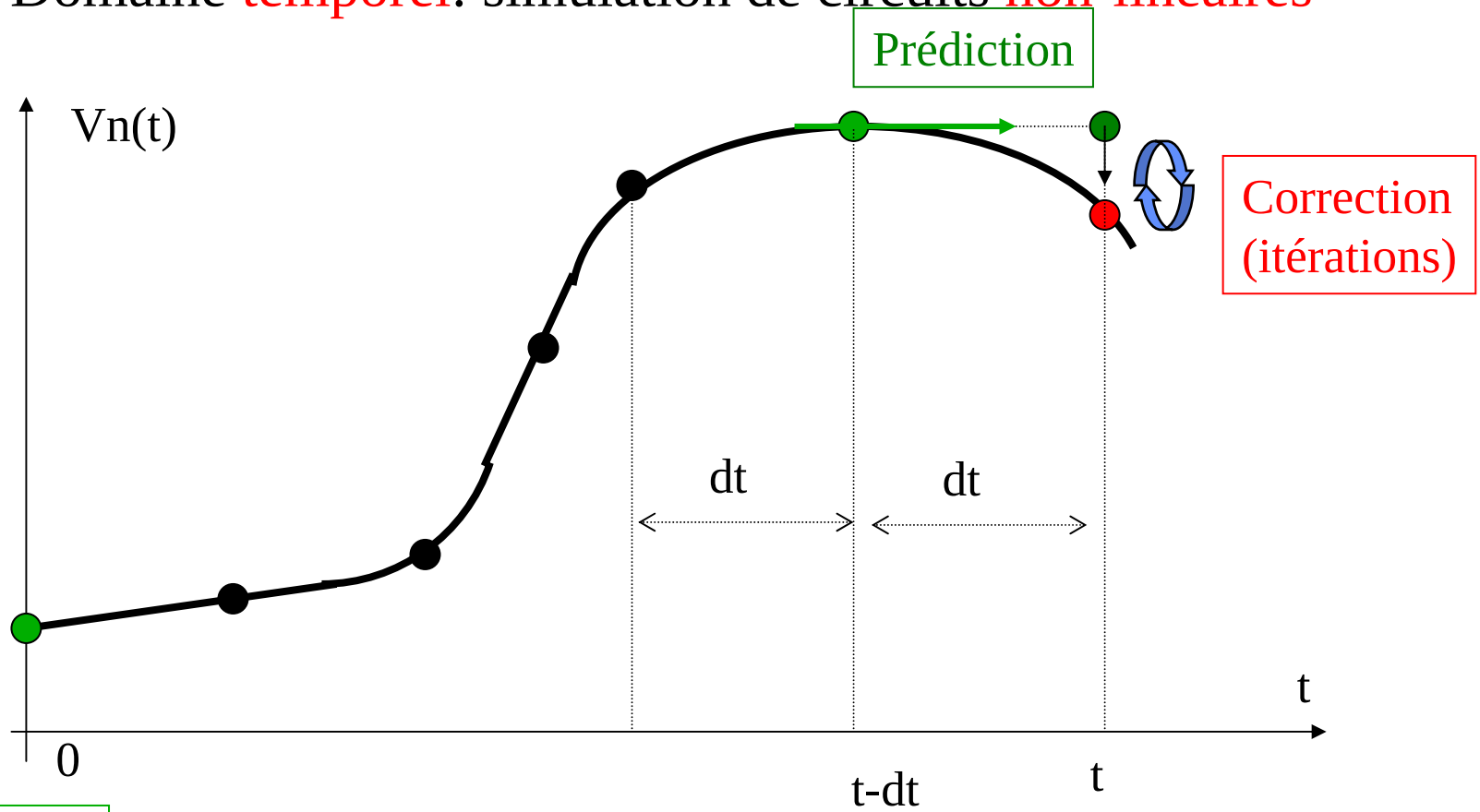
3 solutions!….suivant conditions initiales



Bistable ➔ Q=Vdd ou Q=0 …..
suivant conditions initiales

SIMULATION ELECTRIQUE

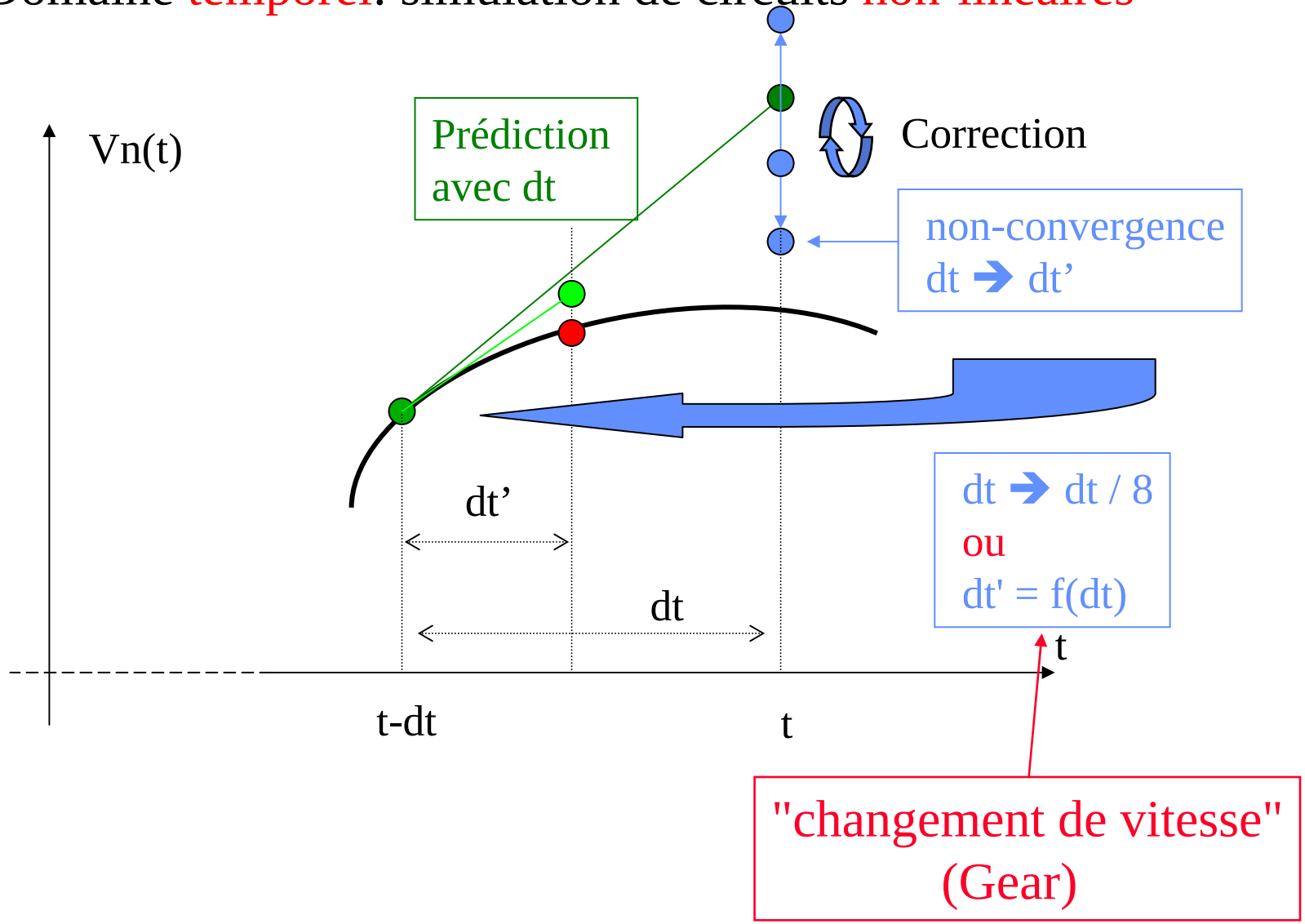
Domaine temporel: simulation de circuits non-linéaires



Simulation DC
Automatique
ou choisie:
.IC …….

SIMULATION ELECTRIQUE

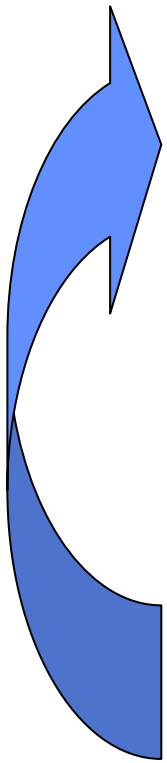
Domaine temporel: simulation de circuits non-linéaires



SIMULATION ELECTRIQUE

Domaine temporel: simulation de circuits non-linéaires

Algorithme de simulation



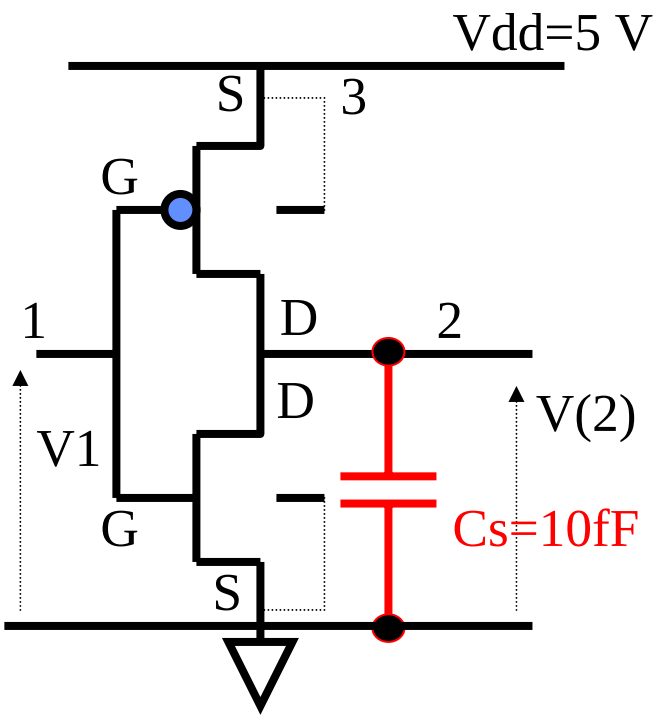
Point de polarisation (simul. DC)
Pour chaque t
- tant que non-convergence et limite non atteinte
  - modèles temporels pour C, L….
  - tant que non-convergence
    - modèles linéarisés
    - résolution système [Yn] [Vn] = [Is]
    - convergence?
  - solution valide? ➔ nouveau dt
- solution au temps t

-t + dt
-Résultats v(t)

SIMULATION ELECTRIQUE

Domaine temporel: simulation de circuits non-linéaires

Variation du pas d'intégration (1/3)

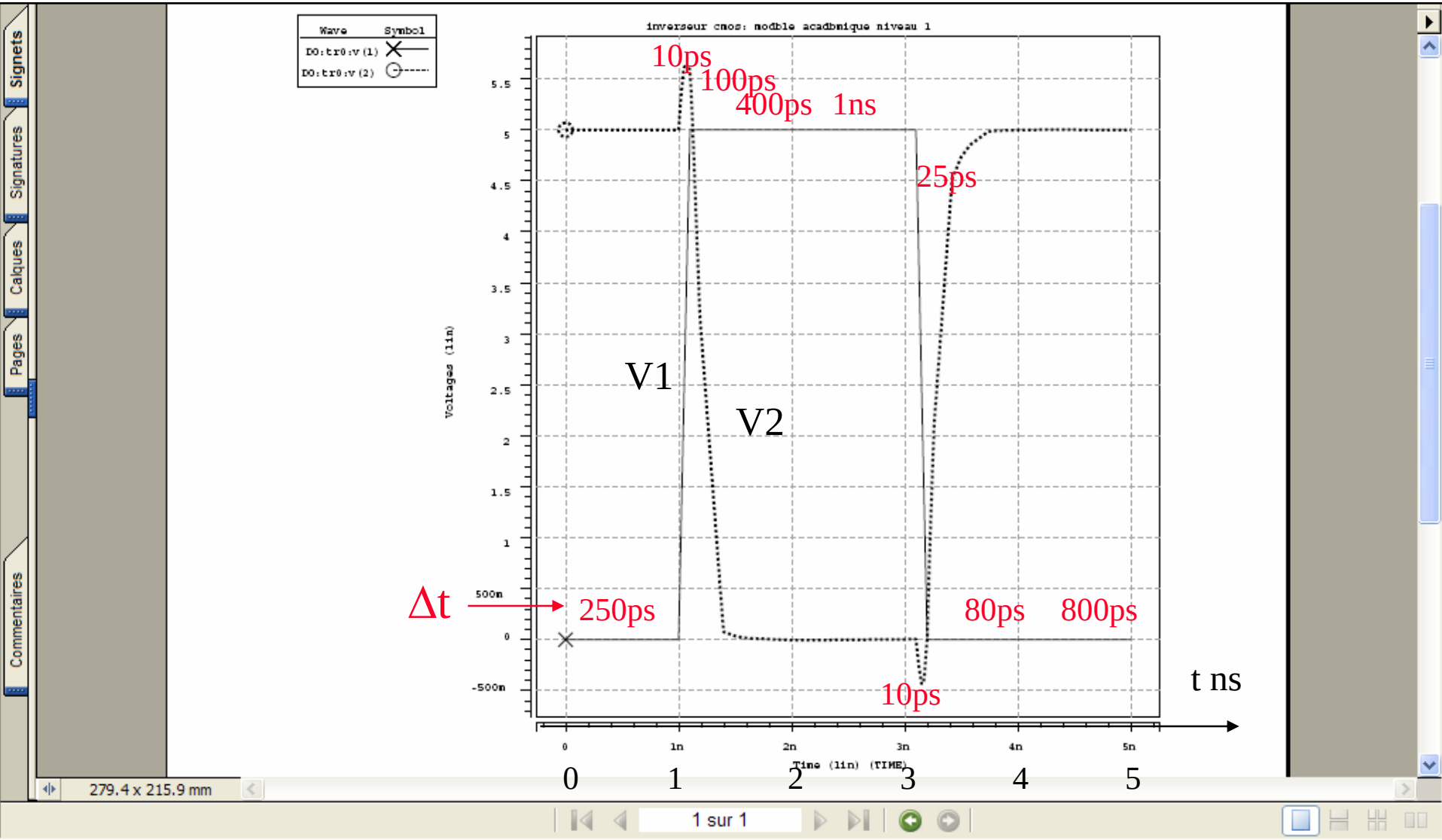



```
INVERSEUR CMOS: modele academique niveau 1
***********espionnage du pas d'integration
***********option itrprt
.options nomod acct post itrprt
.model n nmos level=1 tox=400e-10 vto=0.5
+lambda=0.02 uo=510 cj= 350u cgdo=300p
.model p pmos level=1 tox=400e-10 vto=-0.5
+lambda=0.02 uo=175 cj=540u cgdo=300p
vdd 3 0 dc 5
mp 2 1 3 3 P w=10u l=2u as=20p ad=20p
mn 2 1 0 0 N w=3u l=2u as=10p ad=10p
cs 2 0 10fF
vin 1 0 dc 0 pulse 0 5 1n 0.1n 0.1n 2n
.tran 1n 5n
.print tran v(1) v(2)
.END
```

SIMULATION ELECTRIQUE

Domaine temporel: simulation de circuits non-linéaires

Variation du pas d'intégration (2/3)

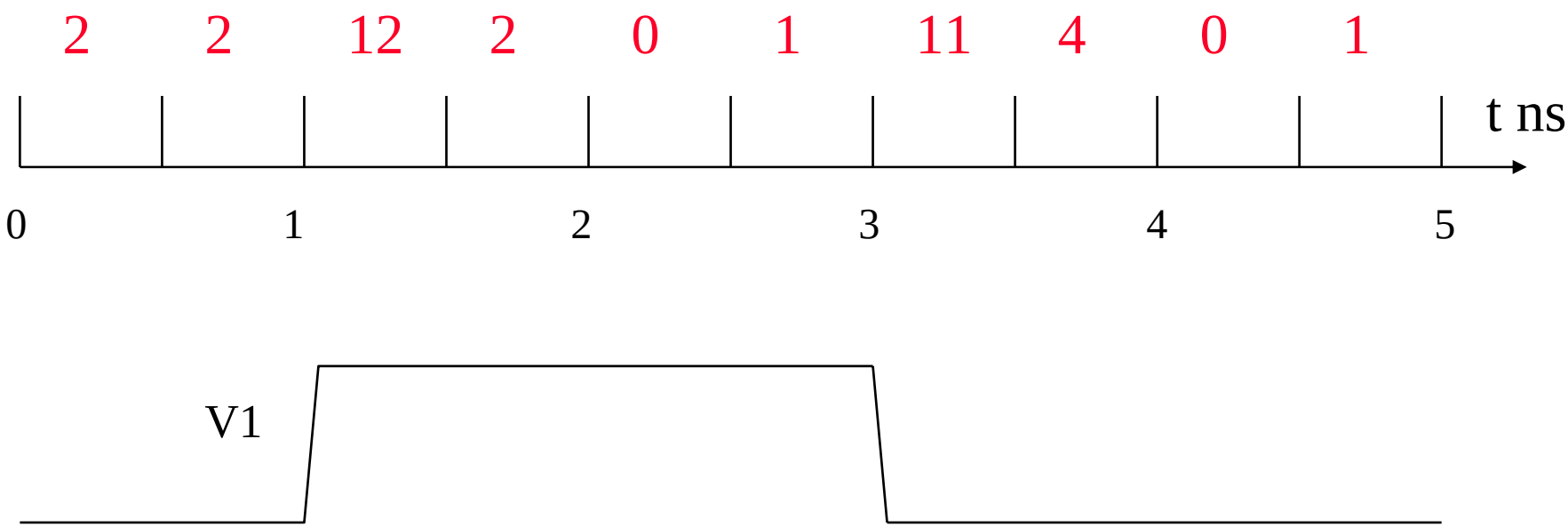


SIMULATION ELECTRIQUE

Domaine temporel: simulation de circuits non-linéaires

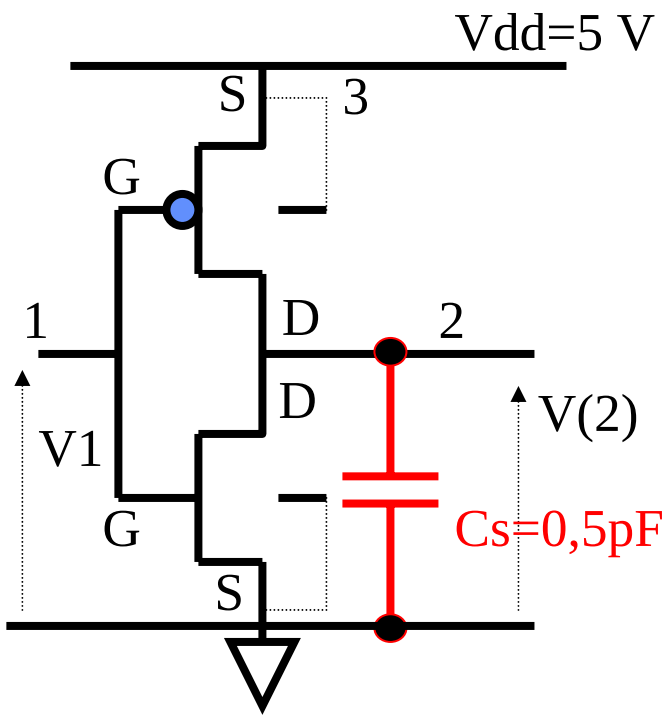
Variation du pas d'intégration (3/3)

Nombre de points calculés par tranches de 0,5 nS



SIMULATION ELECTRIQUE

Exercices: simulations dans le domaine temporel de circuits non-linéaires



Inverseur CMOS

nMOS: W=2µ L= 2µ
pMOS: W=6µ L=2µ

Kp pMOS # Kp nMOS / 3

V1 1 0 PULSE 0 5 ……

Observer: V(2) et V1 en fonction de t

Noter:

- le point de polarisation à t=0
- les retards v(2) par rapport à V1
- faire varier Cs

MODELE ELECTRIQUE STRUCTUREL
DESCRIPTION DES COMPOSANTS
Références aux modèles

DIODE: Description SPICE
(voir guide d'utilisation HSPICE)

.MODEL nom_mod D LEVEL=...IS=... IK=... ....

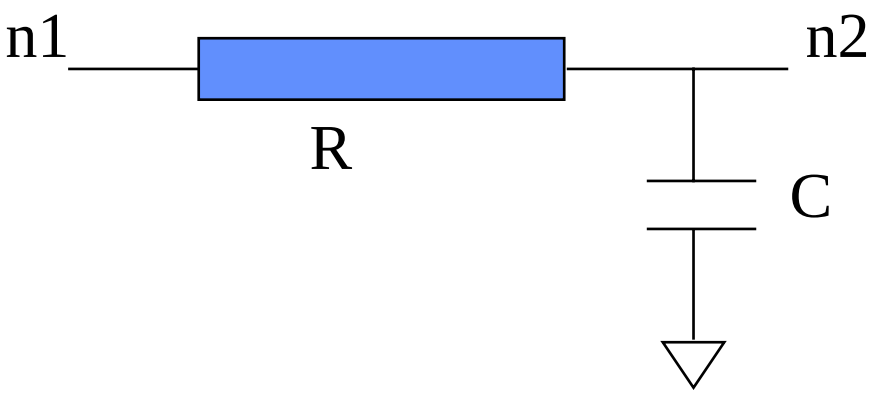
LEVEL= 1 ===> modèle non-géométrique
Dxxx n+ n- nom_mod AREA=... DTEMP=...

LEVEL=3 ===> modèle géométrique
Dxxx n+ n- nom_mod W=... L=... DTEMP=...

AREA (ou WL) : - multiplie courants et capacités
- divise résistances

RESISTANCE : Modèle

Rxxx n1 n2 nom R=... TC1=... TC2=... C=... DTEMP=... AC=....



ou

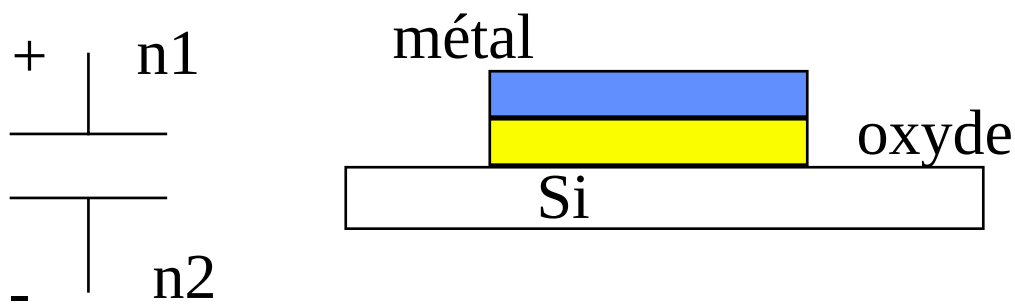
.MODEL nommodel R RSH=... DI =... THICK= ... .

.....

Rxxx n1 n2 nommodel L=... W=...

CAPACITE : Modèle linéaire

Cxxx n1 n2 nom C=... TC1=... TC2=... DTEMP=...



$C=DI\ \varepsilon_0/THICK*W*L$

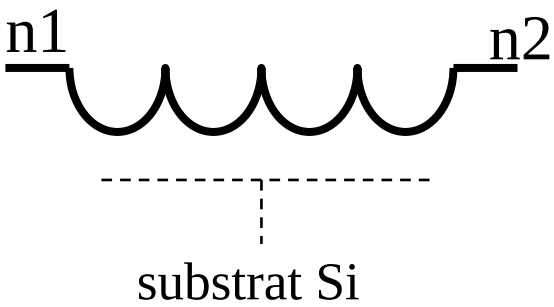
ou

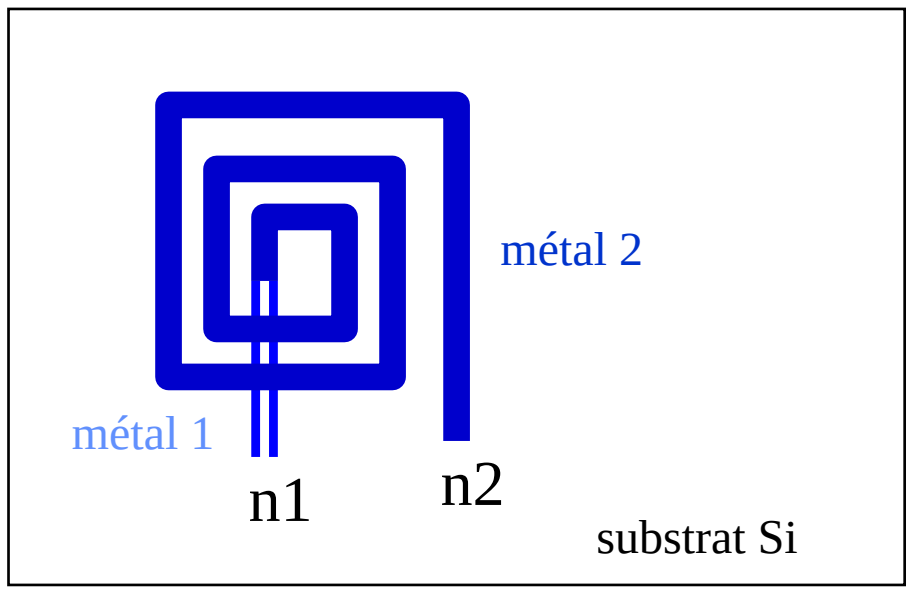
.MODEL nom_model C DI=... THICK=... TC1=...TC2=...
.... COX=... CAPSW=...
.....

Cxxx n1 n2 nom_model L=... W=... ....

SELF intégrée sur Silicium

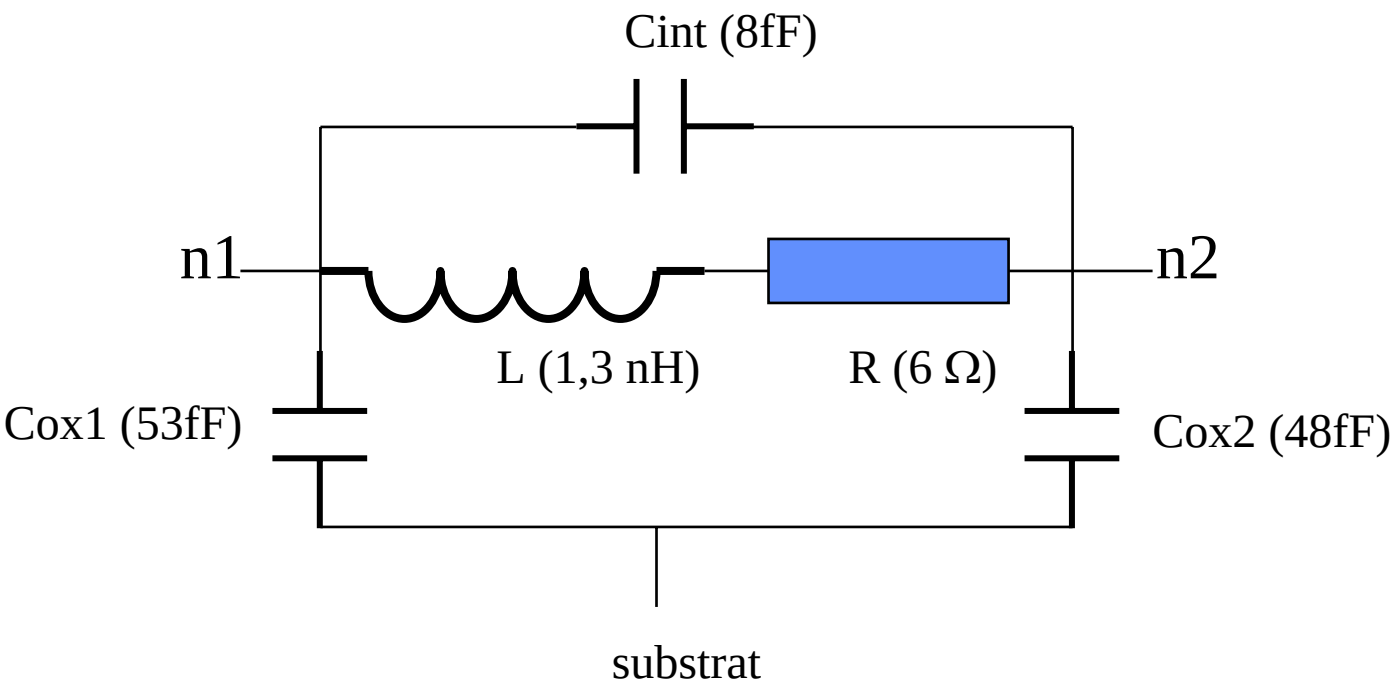
Lxxx n1 n2 val TC1=... TC2=... DTEMP=...

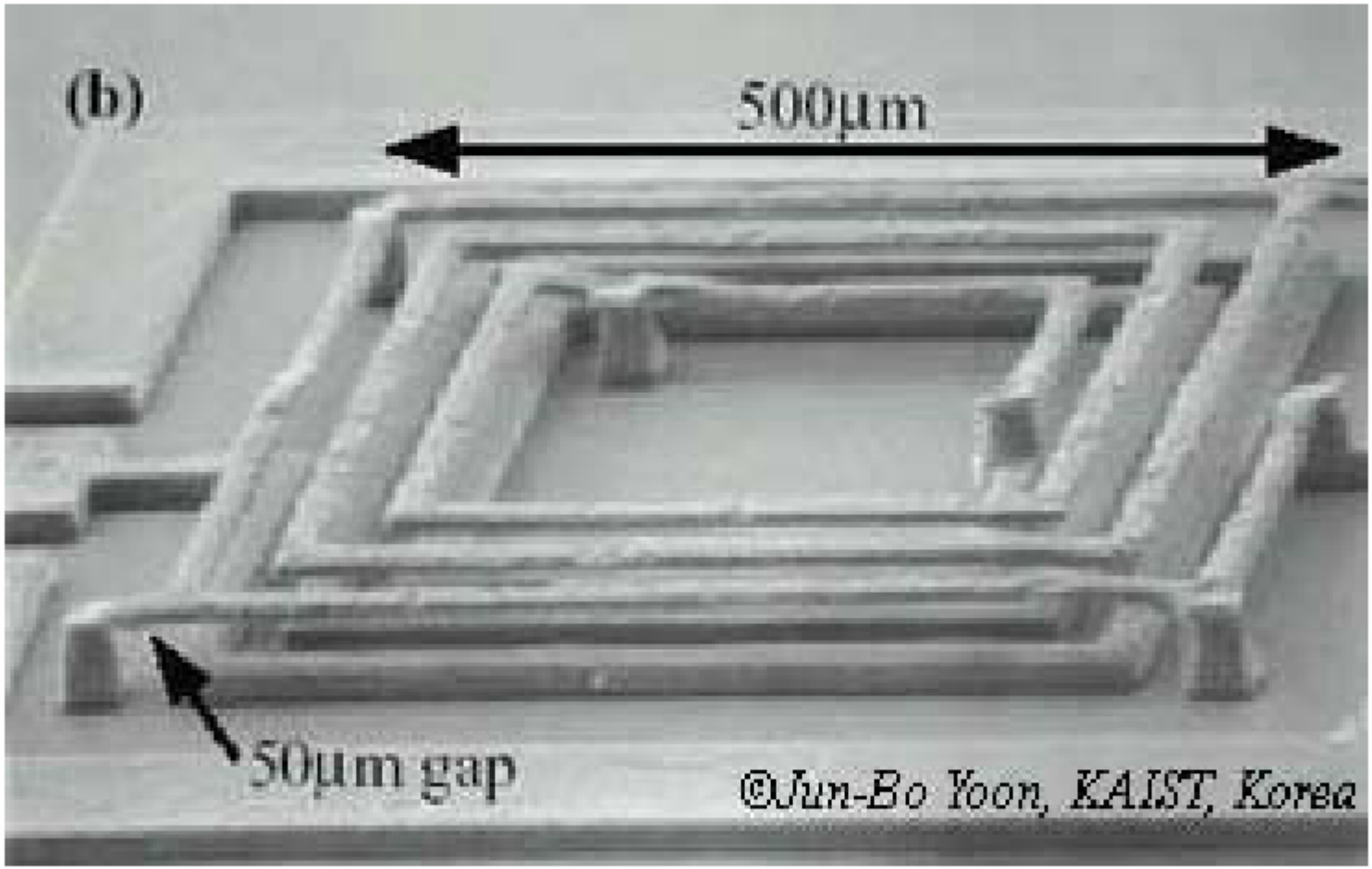




SELF intégrée sur Silicium

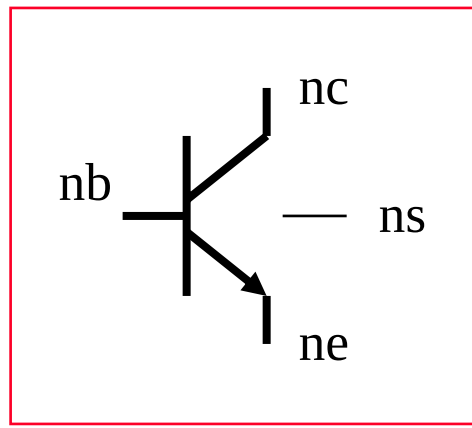
MODELE (simple)





TRANSISTOR BIPOLAIRE: description SPICE (voir guide d'utilisation HSPICE)

.MODEL nom NPN/PNP LEVEL=.. IS=... Vaf=... .....



Qxxx nc nb ne <ns> nom LEVEL=.. <AREA=...>
+ <AREAB=...> <AREAC=...> <DTEMP=...>
+ <OFF> <Vbe=...> < Vce=...>
init. DC init TR

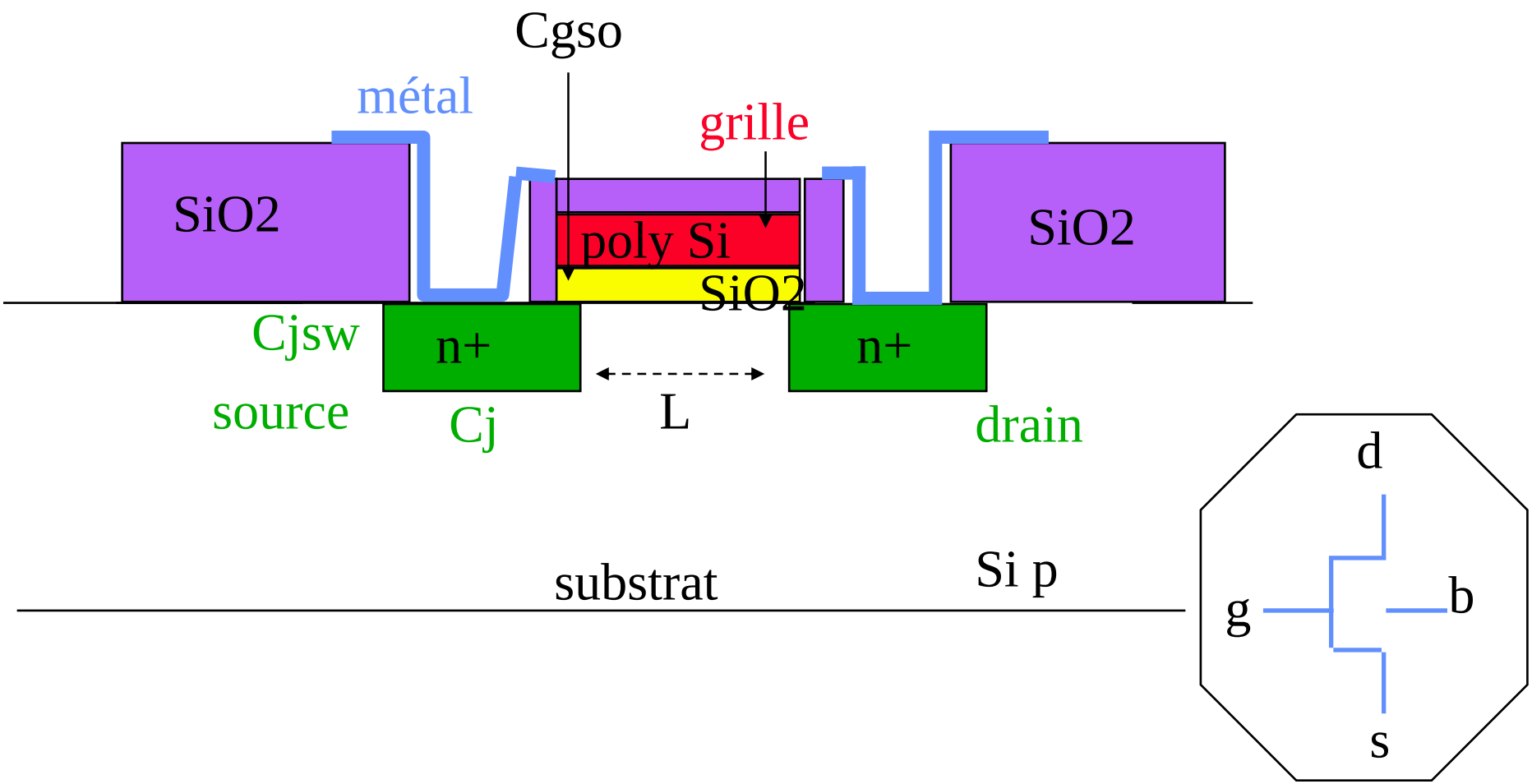
AREA ==> * I et C
" ==> / R

Tr. vertical: AREAB ==> * CJC et Isc
Tr. latéral : AREAC==> * CJC et Isc

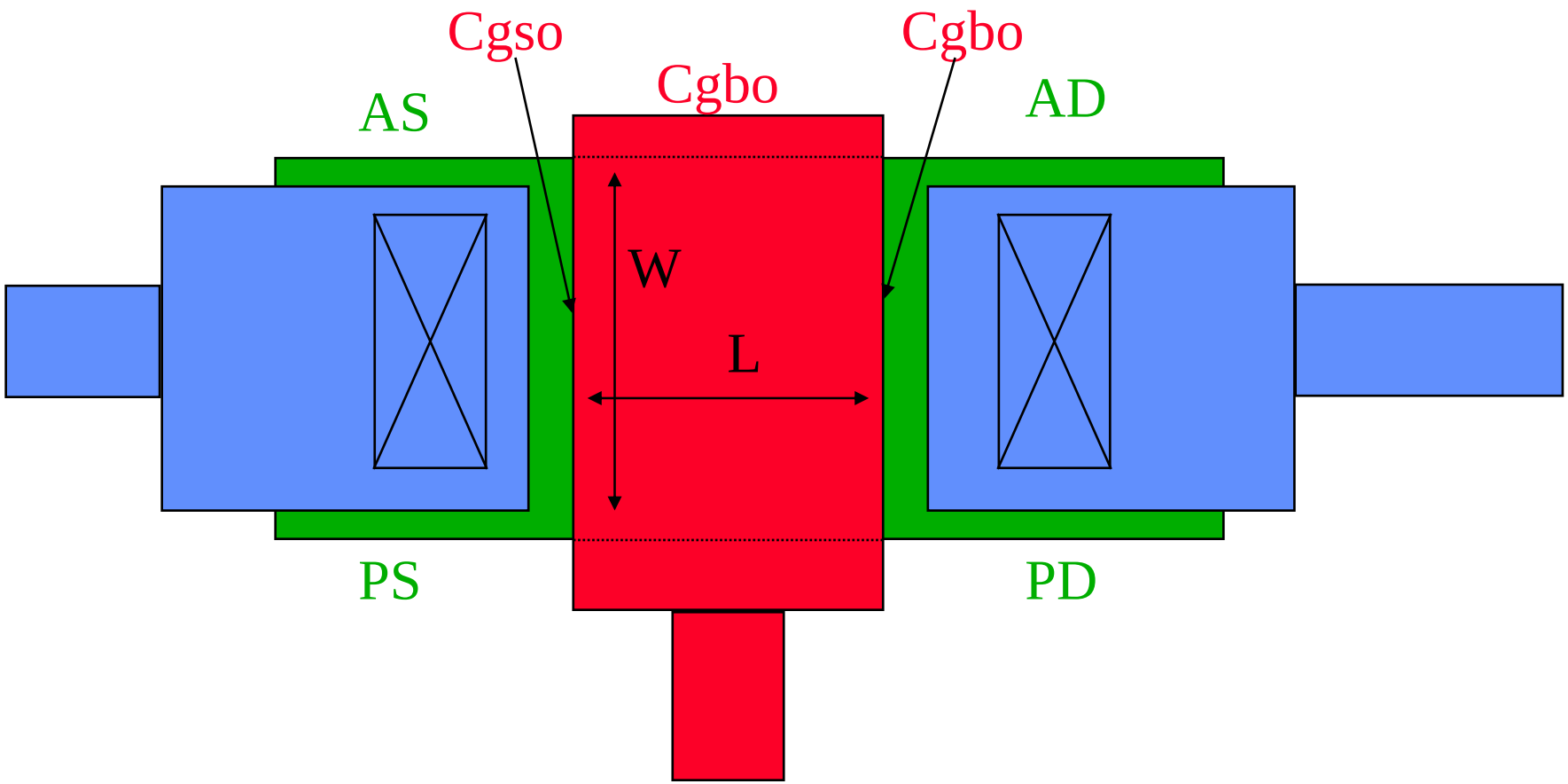
Tr. vertical <== SUBS = 1 (défaut si npn)
Tr. latéral <== SUBS =-1 (défaut si pnp)

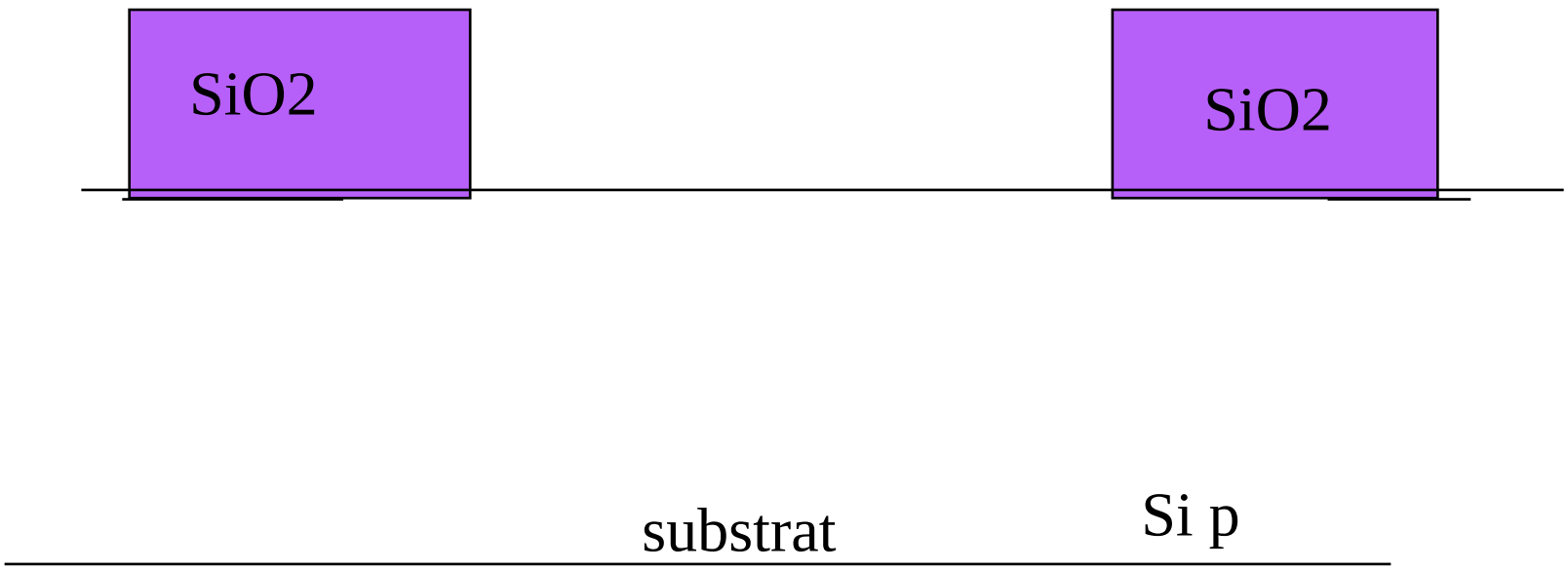
MODELISATION ET SIMULATION
des COMPOSANTS et CIRCUITS
dans les TECHNOLOGIES CMOS

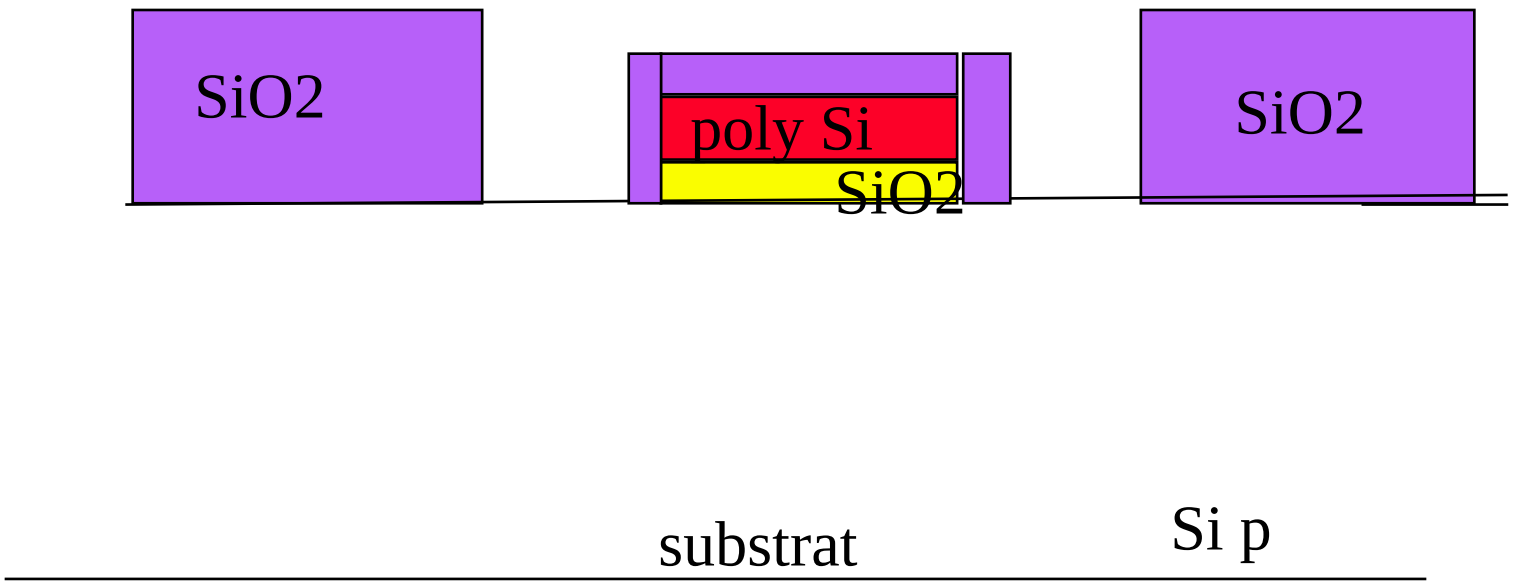
TRANSISTOR MOS : Technologie (canal n)

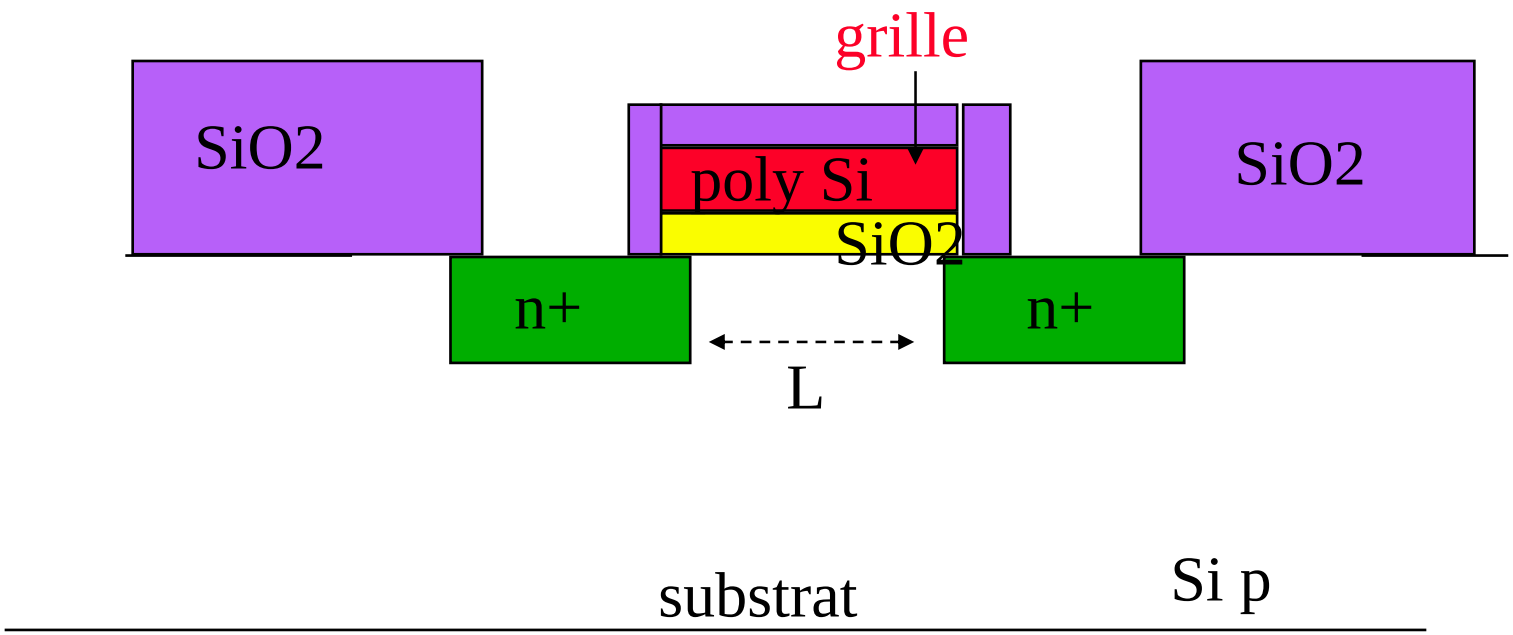


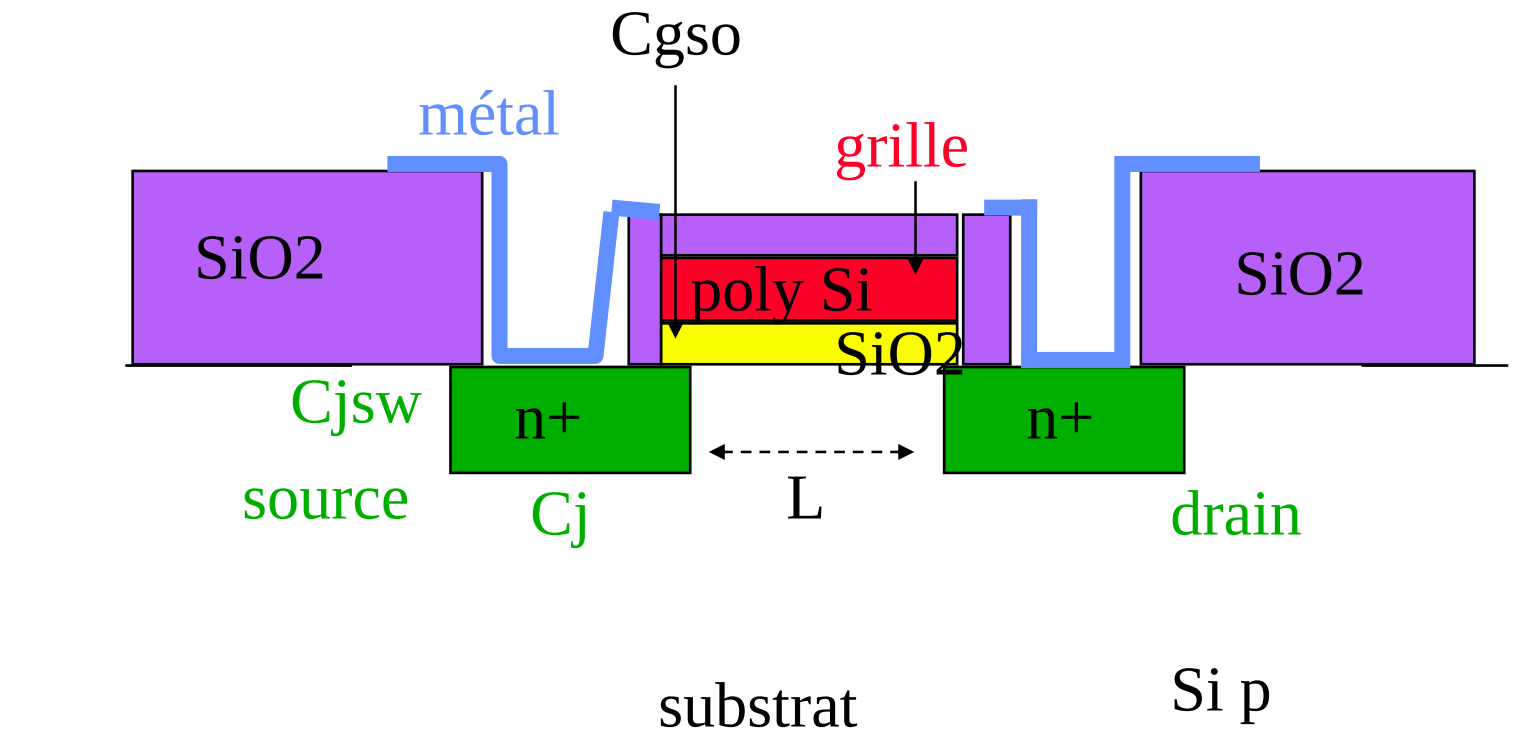
TRANSISTOR MOS : Technologie (canal n)



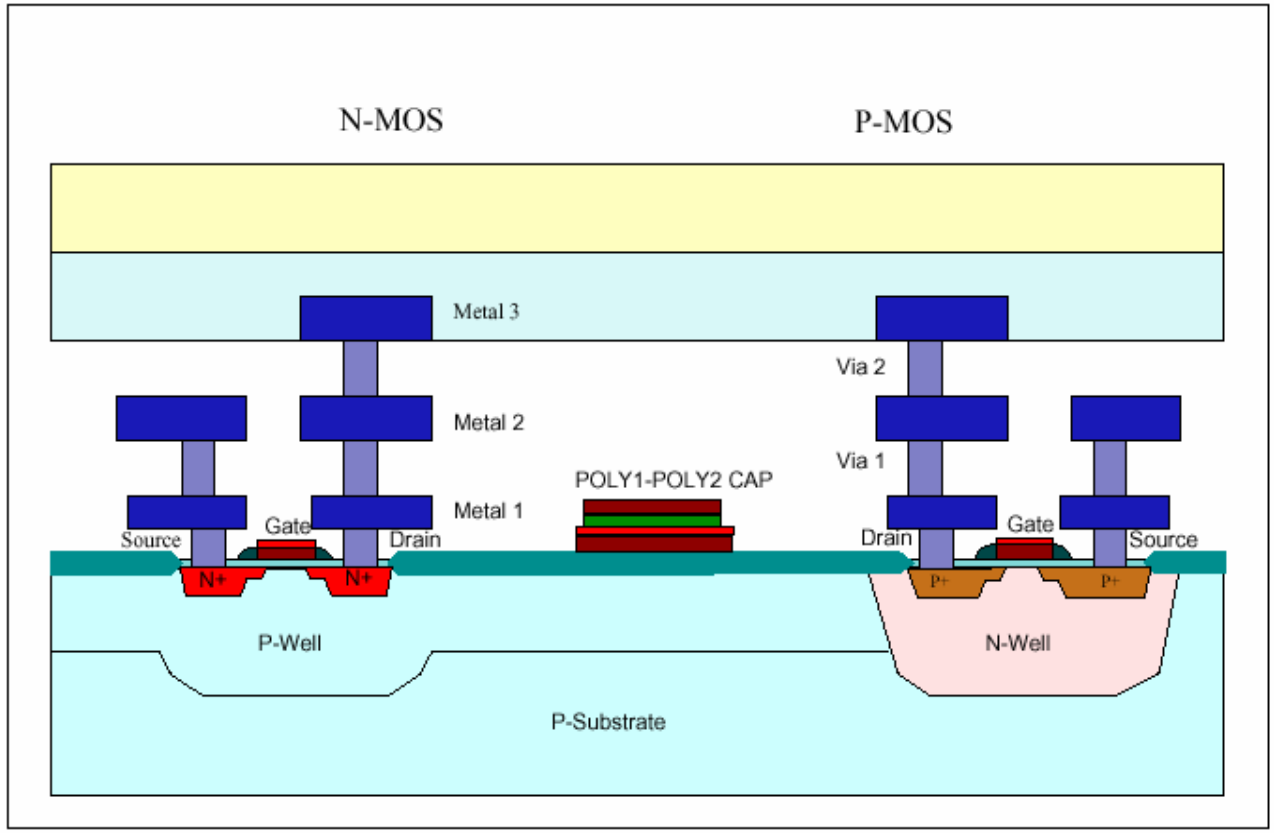

SiO2
SiO2
substrat
Si p


SiO2
poly Si
SiO2
SiO2
substrat
Si p

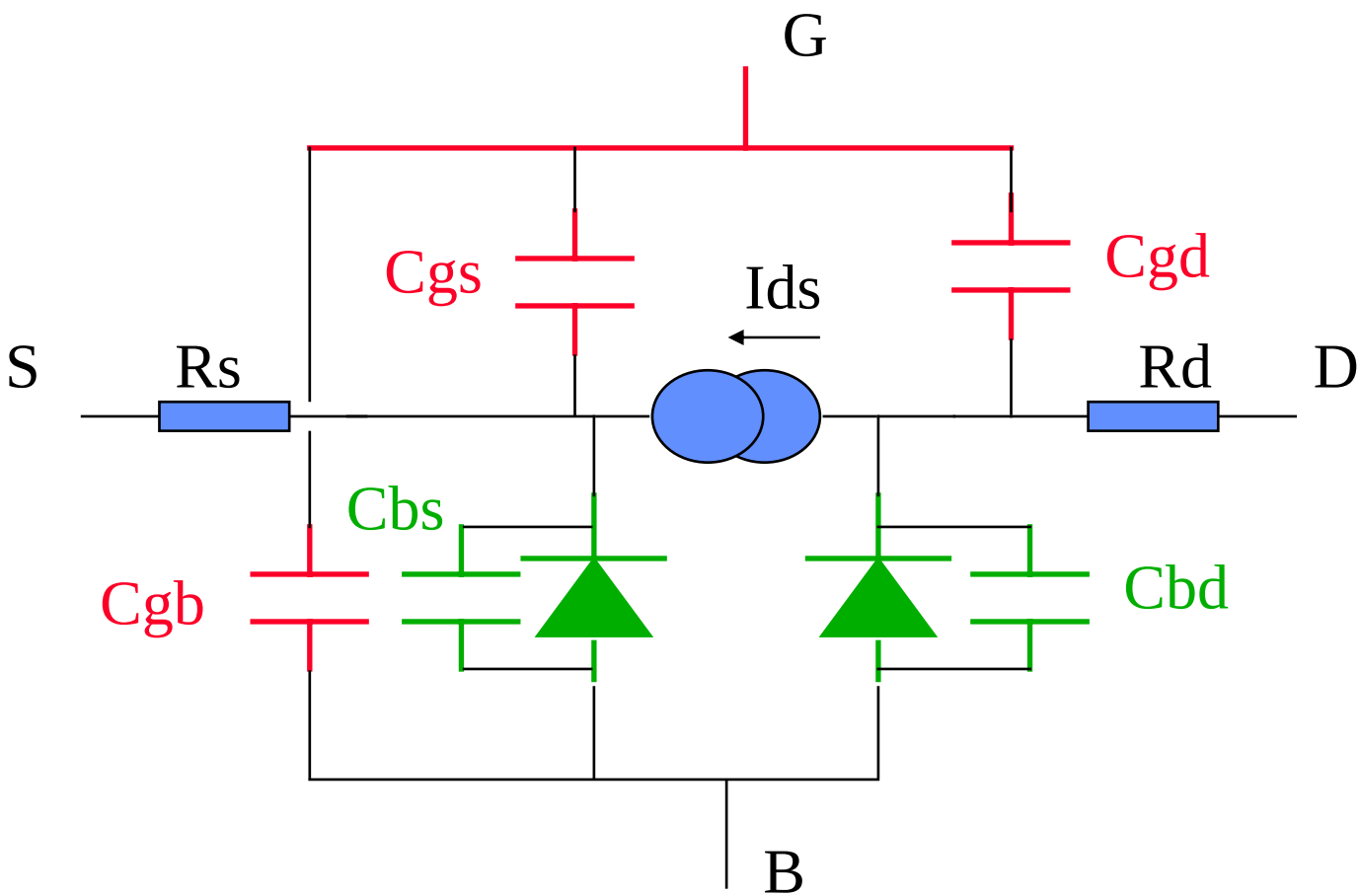

grille
SiO2
poly Si
SiO2
SiO2
n+
n+
L
substrat
Si p


Cgso
métal
grille
SiO2
poly Si
SiO2
SiO2
Cjsw
n+
n+
source
Cj
L
drain
substrat
Si p

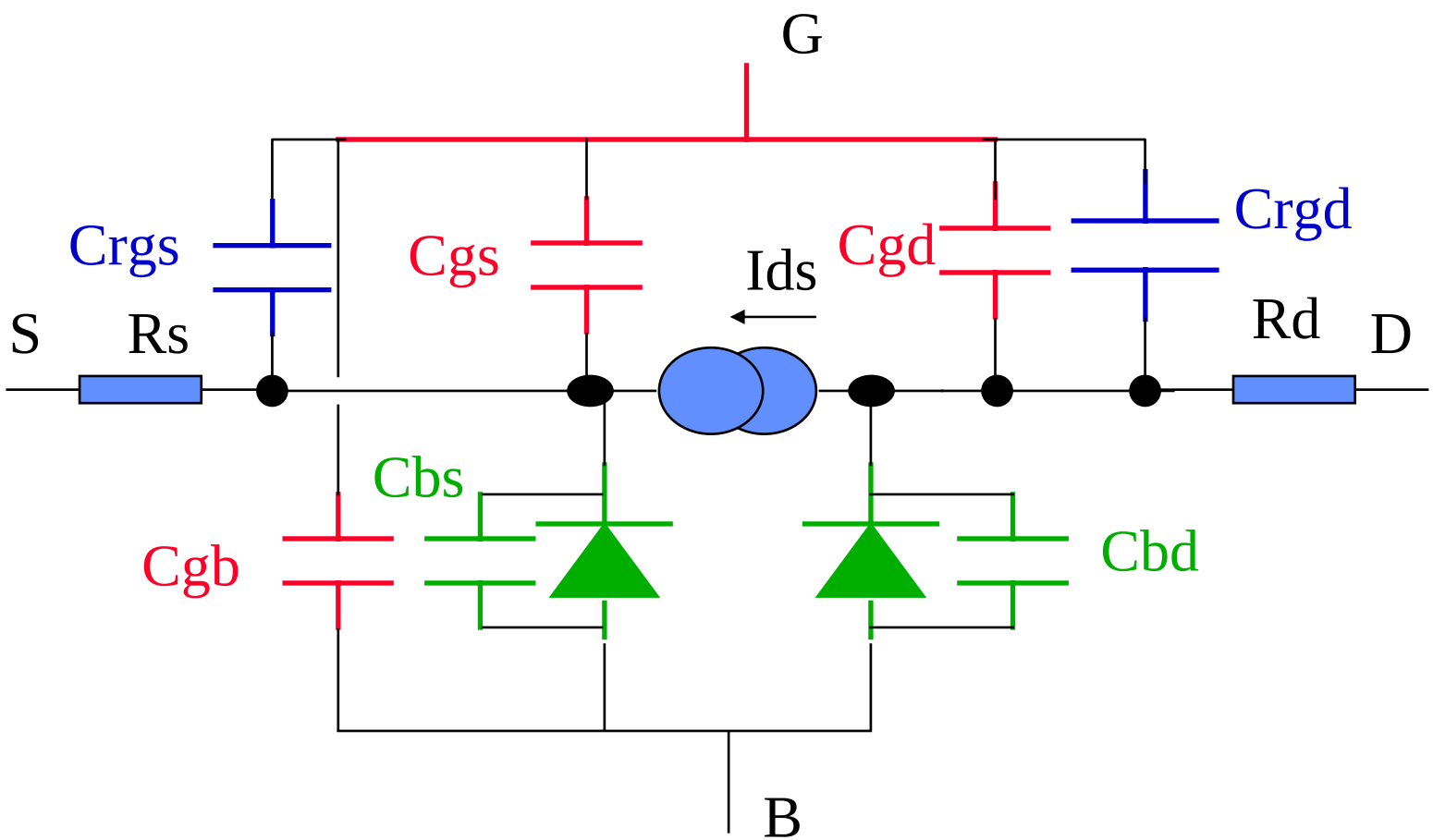
2.1 Wafer Cross – Section



TRANSISTOR MOS : Modèle élémentaire de SCHICHMAN et HODGES (Spice: level=1)



TRANSISTOR MOS : Modèle élémentaire de SCHICHMAN et HODGES (Spice: level=1)



TRANSISTOR MOS : Modèle statique de SCHICHMAN et HODGES (level=1)

BLOQUÉ <==== Vgs < Vt

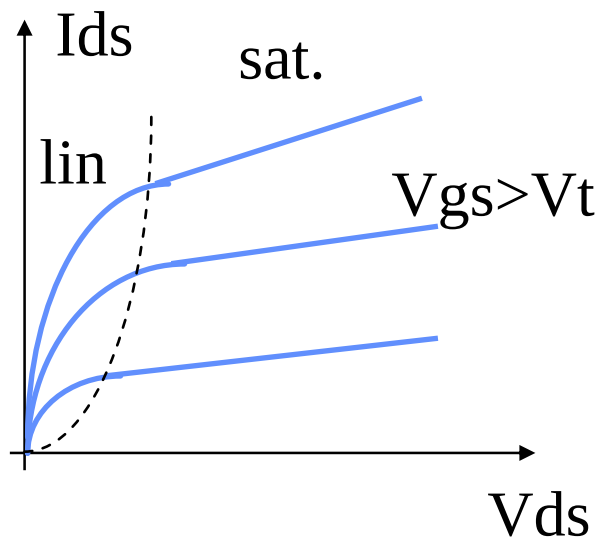
Ids = 0

SATURÉ <==== Vgs > Vt et Vds > Vgs - Vt

$Ids = Kp / 2 * W / L' * [Vgs - Vt]^2$

LINÉAIRE <==== Vgs > Vt et Vds < Vgs - Vt

$Ids = Kp / 2 * W / L' * [2 (Vgs - Vt) Vds - Vds^2]$



TRANSISTOR MOS : Modèle statique de SCHICHMAN et HODGES (level=1)

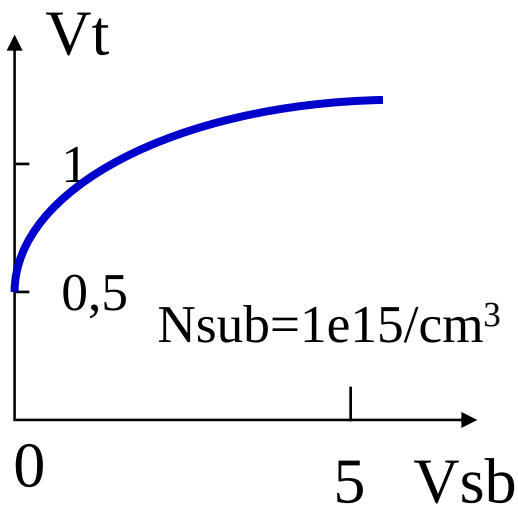
$L' = L (1 - \lambda Vds)$

$Vt = Vt0 + \gamma [sqrt (\Phi i - Vsb) - sqrt (\Phi i)]$

$Kp = \mu Cox \qquad Cox = \varepsilon ox / Tox$

$\gamma = sqrt (2 q \varepsilon_{si} Nsub) / Cox$

$\Phi i = 2 kT/q * Ln (Nsub/ni)$



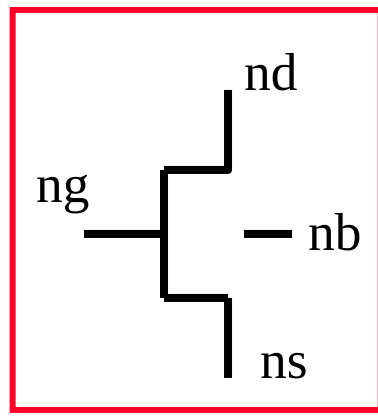
Xj → λ

Ld → λ

TRANSISTOR MOS : description SPICE
(voir guide d'utilisation HSPICE)

Mxxx nd ng ns nb nom_mod L=... W=... <DTEMP=...>
+ <AD=...> <AS=...> <PD=...> <PS=...>
+ <NRD=...> <NRS=...> <RDC=...> <RSC=...>
+ <OFF> <IC= Vds,Vgs,Vbs>

init. DC init. TR

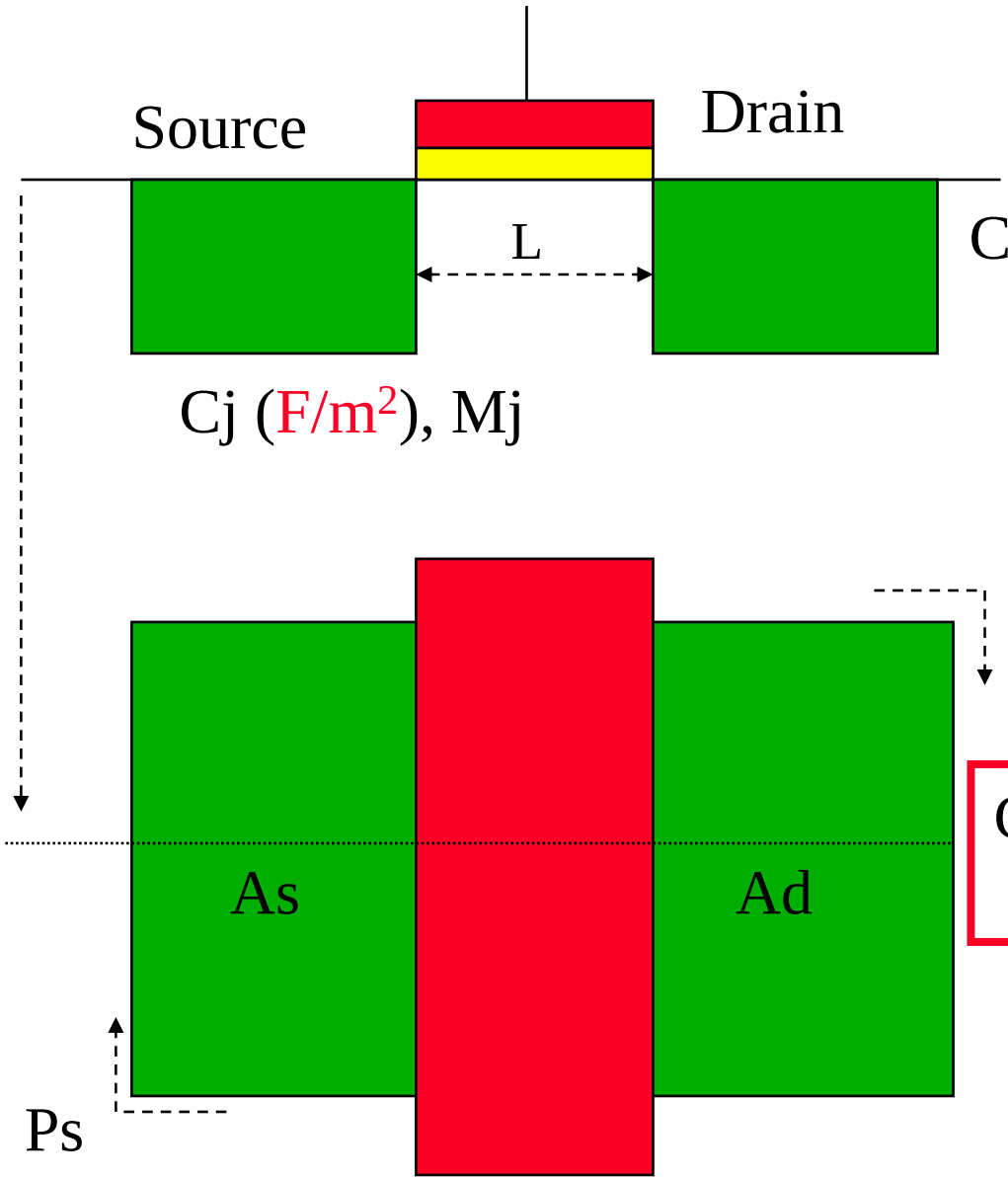


.MODEL nom_model NMOS/PMOS LEVEL=.... VtO=...
+ TOX=... NSUB=... .....RSH=... .....

NMOS ===> enrichissement : Vt > 0
déplétion : Vt < 0
PMOS ===> enrichissement: Vt <0

Rs=NRS*RSH+RSC

Modélisation des capacités de jonction S/B et D/B

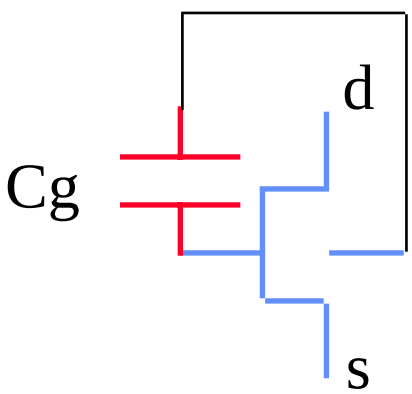


$$Csb = Cj * As / (1- Vbs/Pb)^{Mj} + Cjsw * Ps / (1 - Vbs/Pb)^{Mjsw}$$

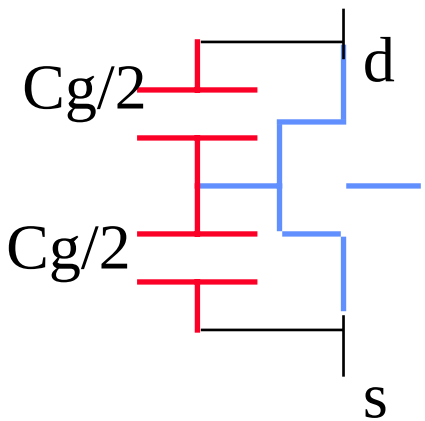
NSUB ➔ Cj et Pb

Modèle dynamique de MEYER: modélisation de la capacité de grille (level=1,2 , capop=0)

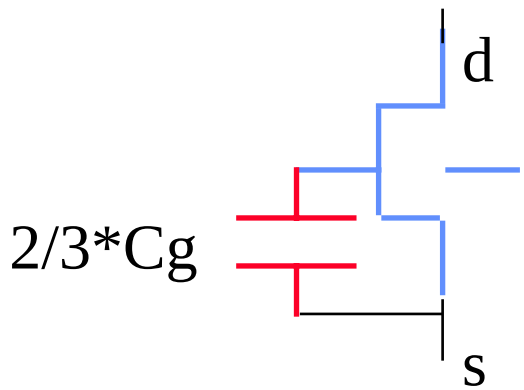
Boqué



Linéaire

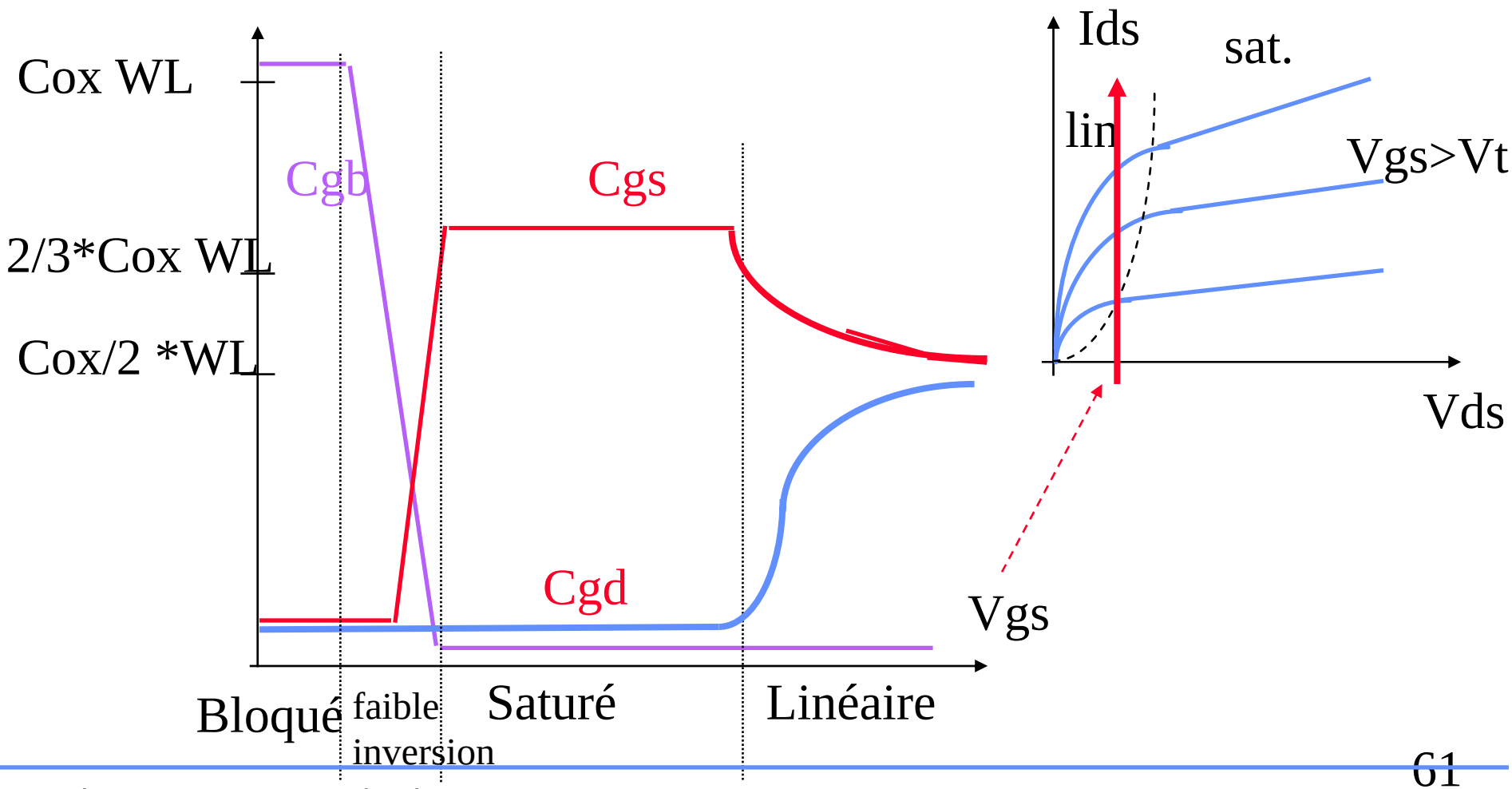


Saturé



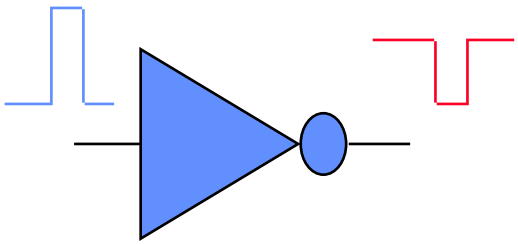
$$Cg = Cox * W * L$$

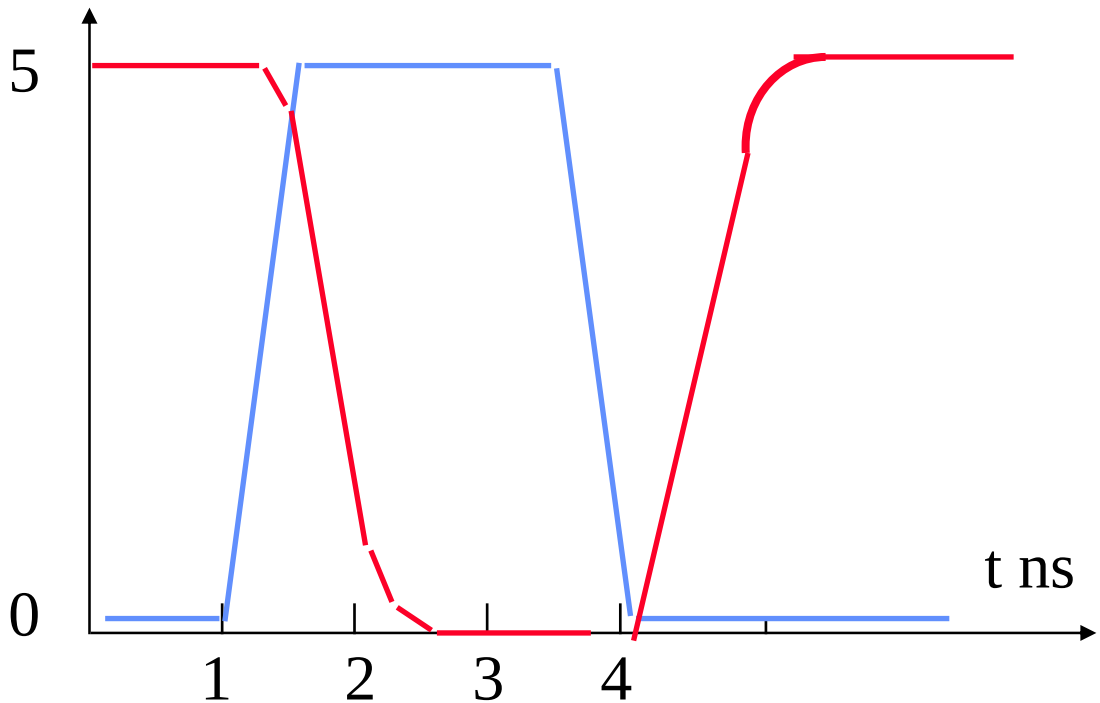
Modèle dynamique de MEYER (level=2 , capop=0)



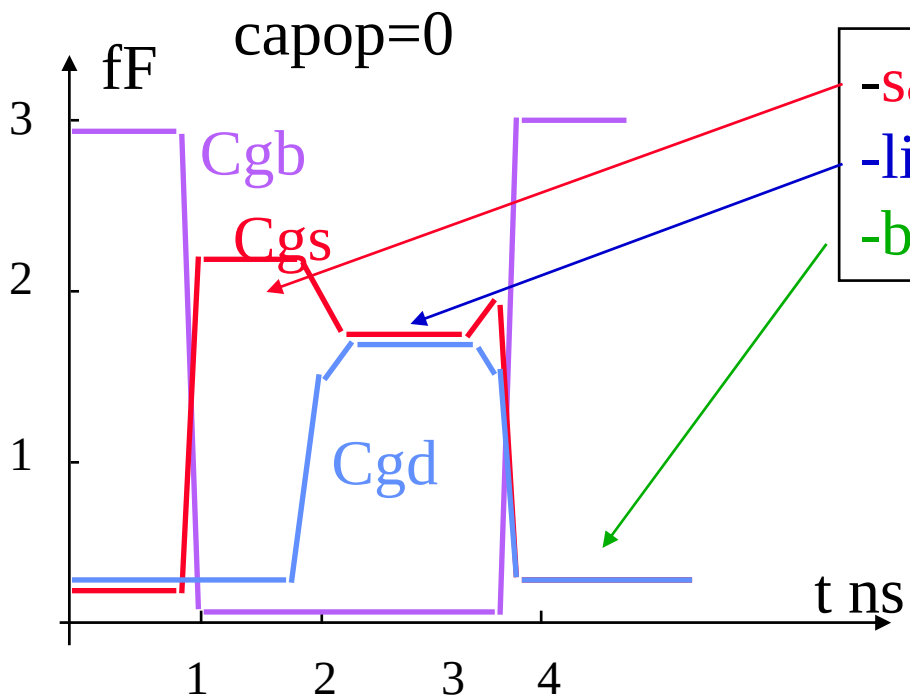
Modèle dynamique de MEYER: exemple de simulation

.probe tran lx19(mn) lx20(mn) lx21(mn)
.print ……..
**********-cgd*****-cgs*****-cgb***

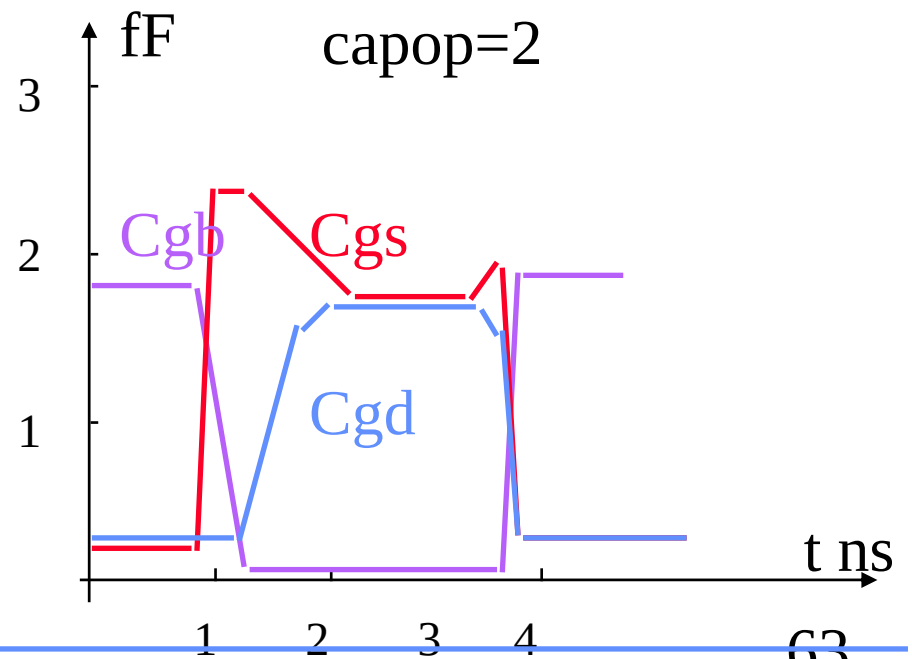




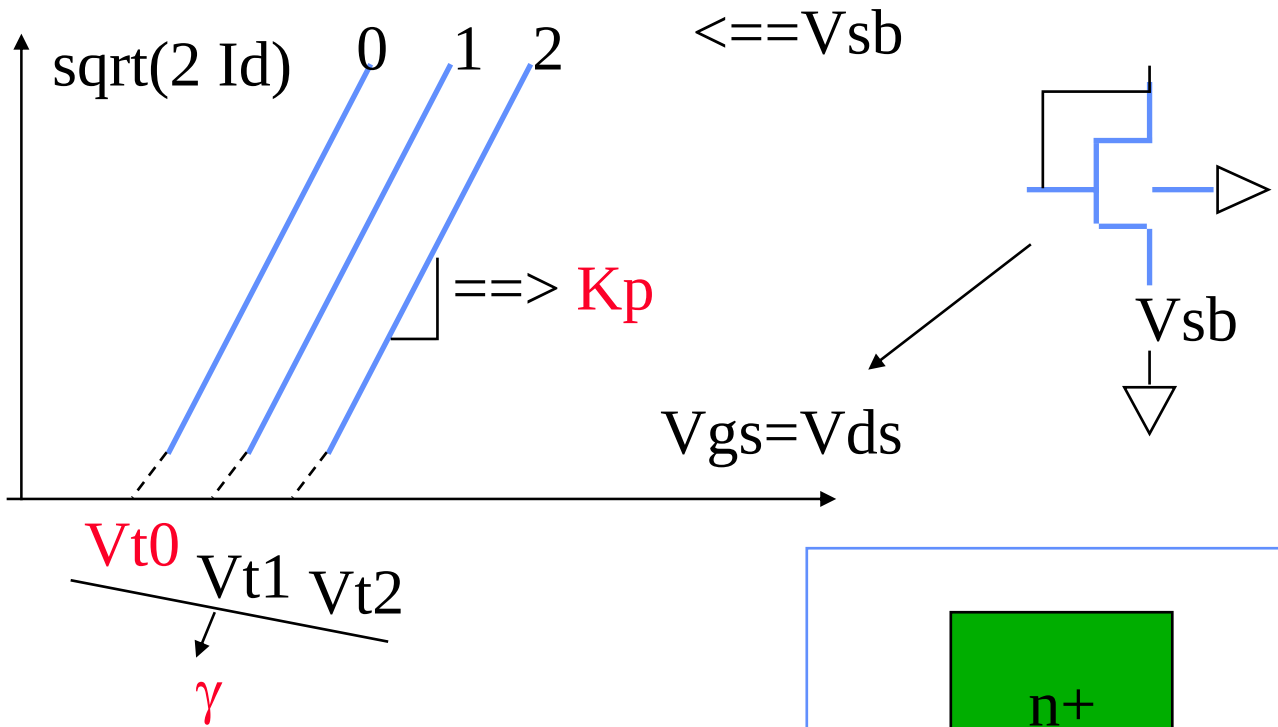
Modèle dynamique de MEYER
Répartition des capacités du modèle du n_MOS

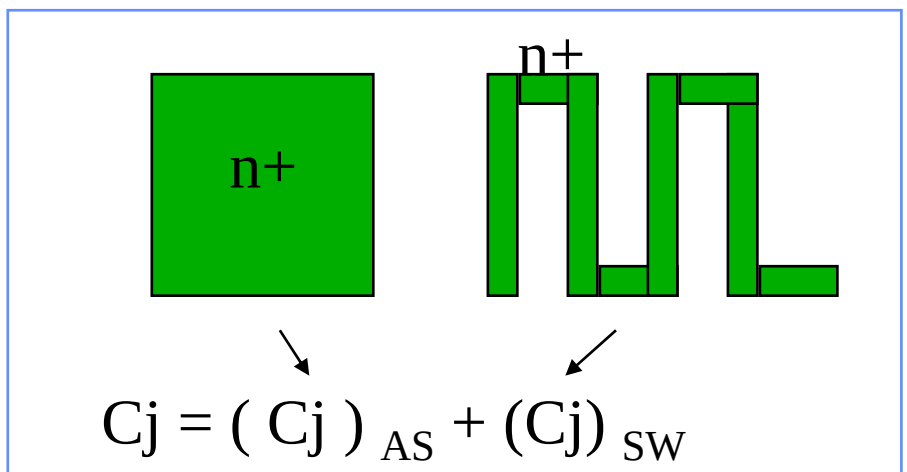


-saturé
-linéaire
-bloqué

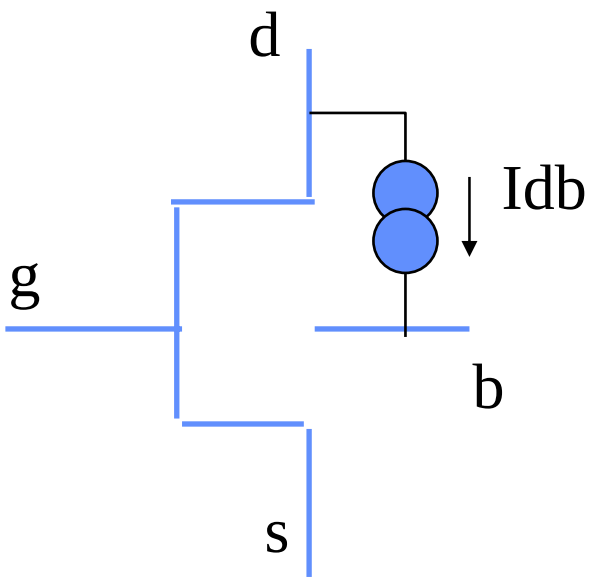


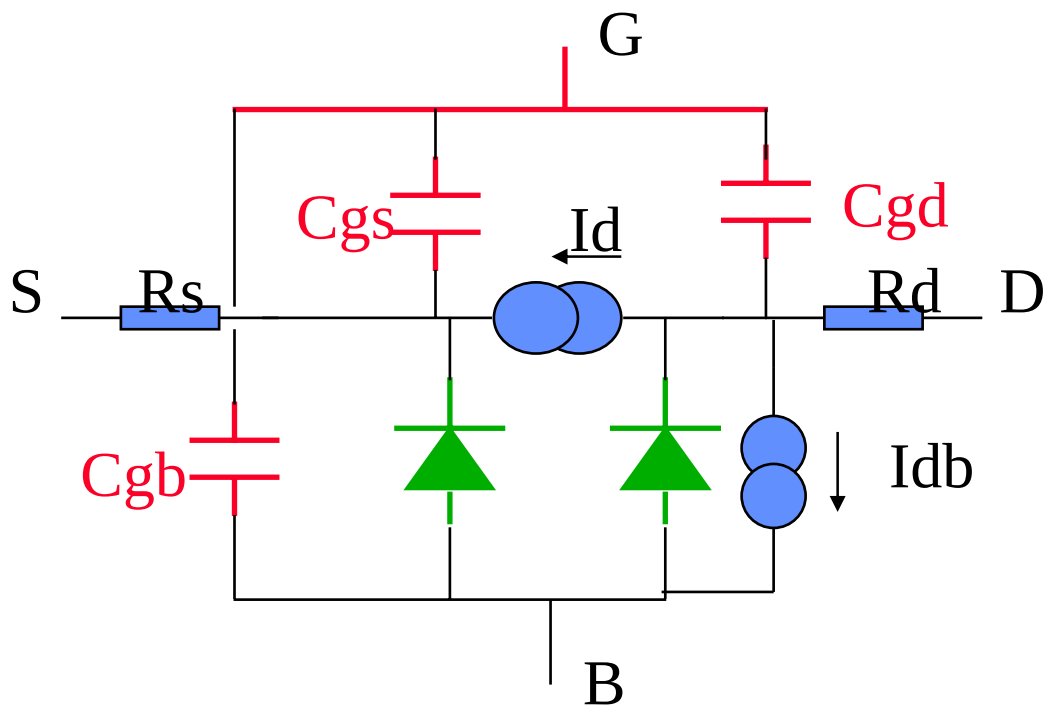
TRANSISTOR MOS: Caractérisation (exemple)
(L, W ~10µ ➔ level = 1)





MODELISATION DU COURANT SUBSTRAT
« Ionisation par impact »



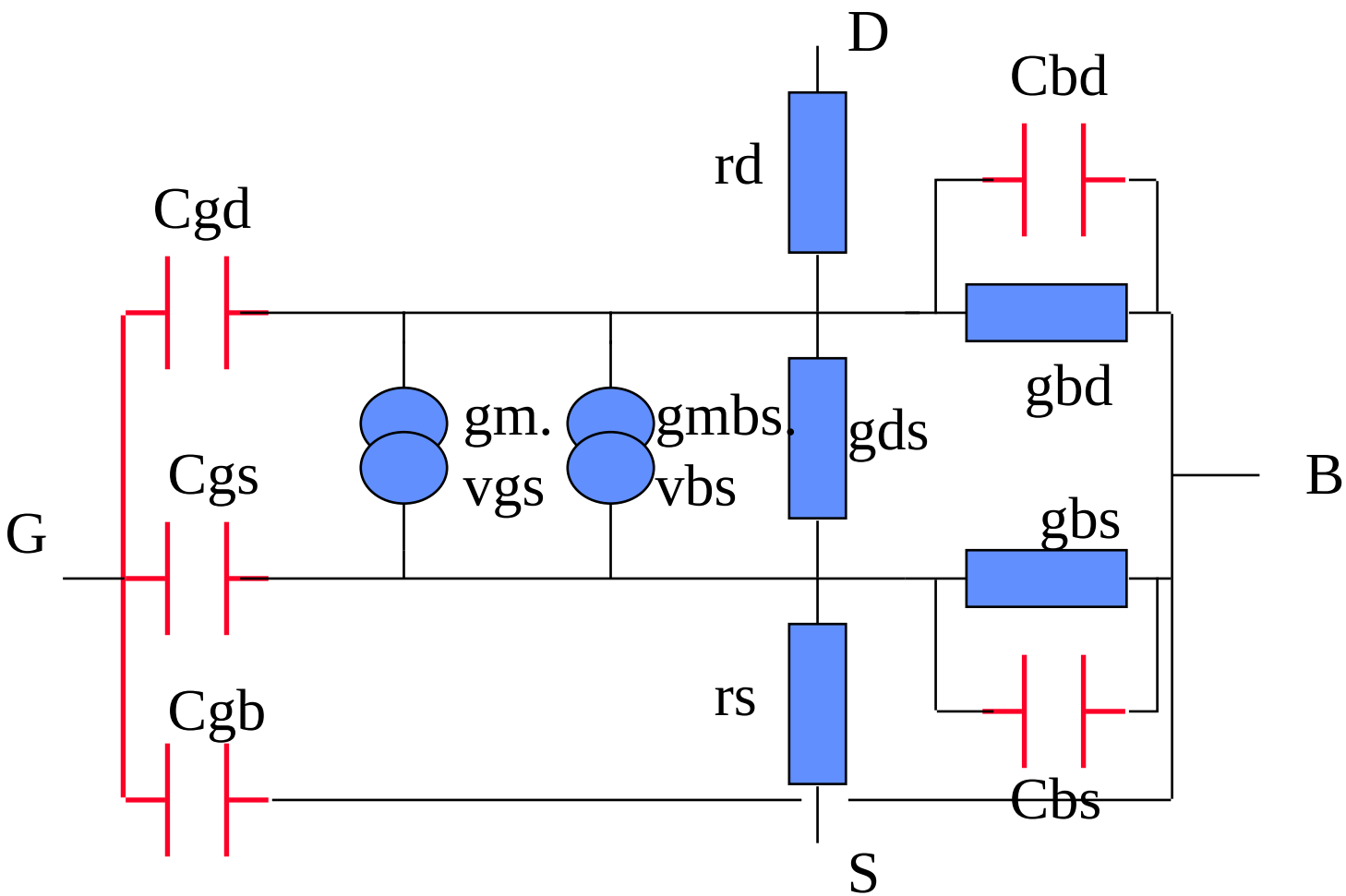


$$Idb = ALPHA * Ids * (Vds - Vdsat) * \exp\{ - [VCR / (Vds - Vdsat)]\}$$

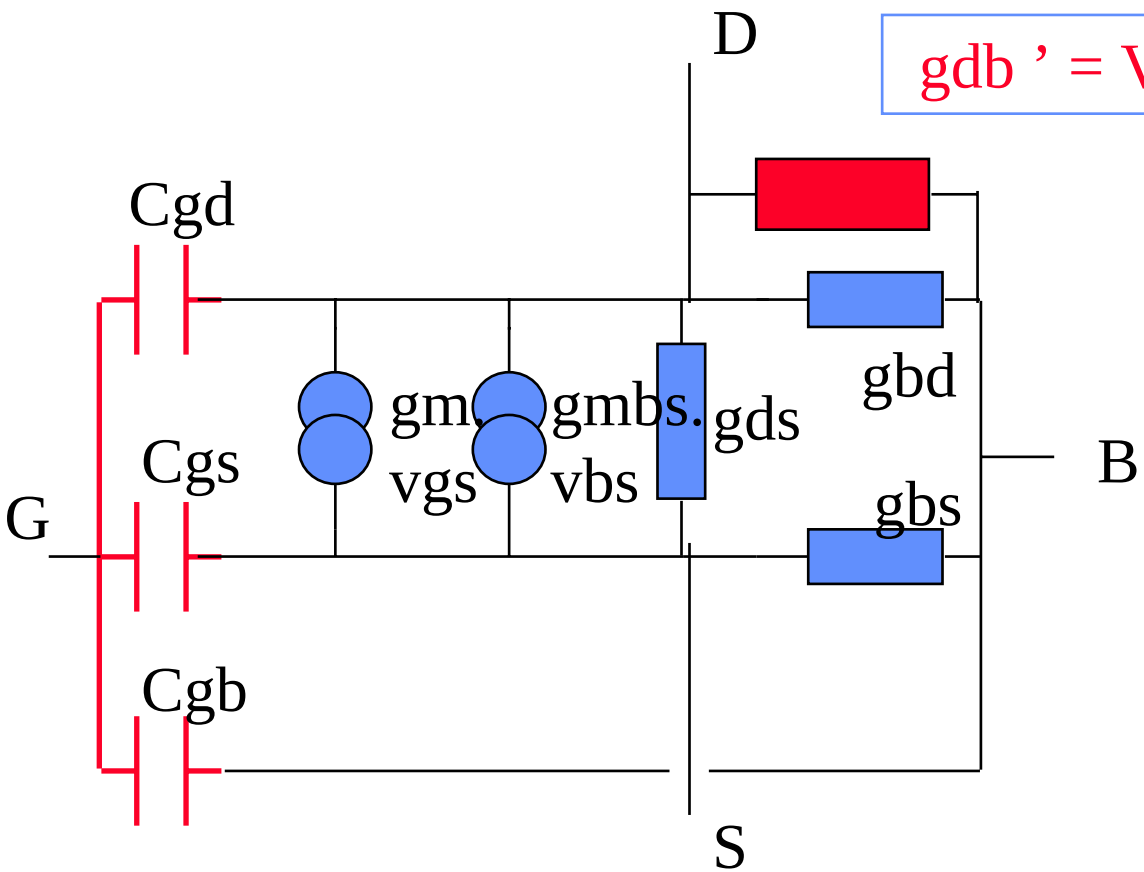
ALPHA (L,W) ex. NMOS ~ 5 V^{-1}

VCR (L,W) ~ 30 V

TRANSISTOR MOS: Modèle linéarisé



TRANSISTOR MOS: Modèle linéarisé
Effet du courant substrat



$gdb' = VCR * Idb / (Vds-Vdsat)^2$

NB:

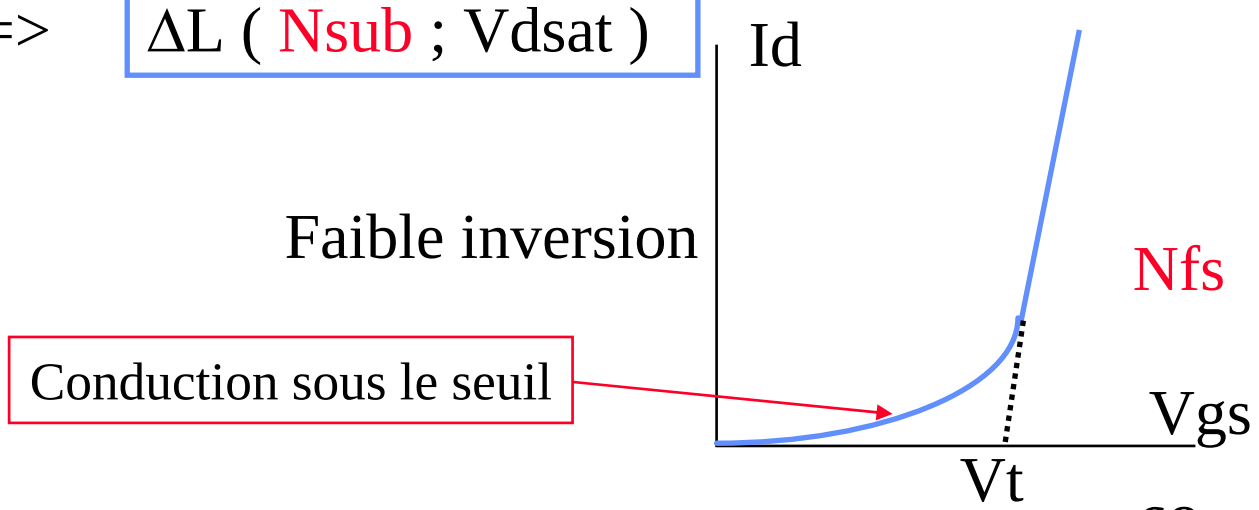
gd ' // gds

Transistors MOS: modèles sub-microniques

L ↘ ==> Vt ↗ W ↘ ==> Vt ↘

Vt' = Vt [Nsub ; Xj ; …..; Vbs ; Vds ; W ; L]

Réduction de L ==> ΔL (Nsub ; Vdsat)



Transistors MOS: modèles sub-microniques (suite)

$\mu(\vec{E})$

$$\mu s = U0 \left[Ucrit * \varepsilon_{si} / \left(Cox \, (Vgs - Vt - Utran * Vds) \right) \right]^{Uexp}$$

Porteurs chauds : Vmax (vitesse limite) ➔ Ids ↘

MOS: Modèle BSIM3v3

Pour les technologies sub-microniques: 0,25µ < L < 1µ

(voir « descriptions par les exemples »)

Pour les technologies nano-métriques: L < 0,15 µ

➔ modèle BSIM4 :

+ modélisation des courants de fuite tunnel,

+ …….

MOS: Modèle BSIM3v3
Phénomènes physiques modélisés

- Effet des faibles W et L sur la tension de seuil
- Dopage non uniforme (latéral et vertical)
- Réduction de la mobilité dû au champ électrique vertical
- Effet de la charge du substrat
- Saturation de la vitesse
- Abaissement de la barrière par le potentiel de drain (DIBL)
- Modulation de la longueur de canal (CLM)
- Courant substrat induit (SCBE)
- Conduction sous le seuil
- Résistances parasites source / drain

```
.MODEL MODN NMOS LEVEL=49
* ---------------------------------------------------------------------
************************ SIMULATION PARAMETERS ************************
* ---------------------------------------------------------------------
* format    : HSPICE
* model     : MOS BSIM3v3
.options nomod post
* process   : CMOS 0.35 microns
* ---------------------------------------------------------------------
*                          TYPICAL MEAN CONDITION
* ---------------------------------------------------------------------
*
*        *** Flags ***
+MOBMOD =1.000e+00 CAPMOD =2.000e+00 NOIMOD =1.000e+00 VERSION=3.11
*        *** Threshold voltage related model parameters ***
+K1      =6.044e-01
+K2      =2.945e-03 K3     =-1.72e+00 K3B    =6.325e-01
+NCH     =2.310e+17 VTH0   =4.655e-01
+VOFF    =-5.72e-02 DVT0   =2.227e+01 DVT1   =1.051e+00
+DVT2    =3.393e-03 KETA   =-6.21e-04
+PSCBE1 =2.756e+08 PSCBE2 =9.645e-06
+DVT0W  =0.000e+00 DVT1W  =0.000e+00 DVT2W  =0.000e+00
*        *** Mobility related model parameters ***
+UA      =1.000e-12 UB     =1.723e-18 UC     =5.756e-11
+U0      =4.035e+02
*        *** Subthreshold related parameters ***
+DSUB    =5.000e-01 ETA0   =3.085e-02 ETAB   =-3.95e-02
+NFACTOR=1.119e-01
```

```
*         *** Saturation related parameters ***
+EM     =4.100e+07 PCLM   =6.831e-01
+PDIBLC1=1.076e-01 PDIBLC2=1.453e-03 DROUT  =5.000e-01
+A0     =2.208e+00 A1     =0.000e+00 A2     =1.000e+00
+PVAG   =0.000e+00 VSAT   =1.178e+05 AGS    =2.490e-01
+B0     =-1.76e-08 B1     =0.000e+00 DELTA  =1.000e-02
+PDIBLCB=2.583e-01
*         *** Geometry modulation related parameters ***
+W0     =1.184e-07 DLC    =2.900e-08
+DWC    =2.676e-08 DWB    =0.000e+00 DWG    =0.000e+00
+LL     =0.000e+00 LW     =0.000e+00 LWL    =0.000e+00
+LLN    =1.000e+00 LWN    =1.000e+00 WL     =0.000e+00
+WW     =0.000e+00 WWL    =0.000e+00 WLN    =1.000e+00
+WWN    =1.000e+00
*         *** Temperature effect parameters ***
+TNOM   =27.0 AT     =3.300e+04 UTE    =-1.80e+00
+KT1    =-3.30e-01 KT2    =2.200e-02 KT1L   =0.000e+00
+UA1    =0.000e+00 UB1    =0.000e+00 UC1    =0.000e+00
+PRT    =0.000e+00
*         *** Overlap capacitance related and dynamic model parameters   ***
+CGDO   =1.120e-10 CGSO   =1.120e-10 CGBO   =1.100e-10
+CGDL   =1.350e-10 CGSL   =1.350e-10 CKAPPA =6.000e-01
+CF     =0.000e+00 ELM    =5.000e+00
+XPART  =1.000e+00 CLC    =1.000e-15 CLE    =6.000e-01
```

```
*        *** Parasitic resistance and capacitance related model parameters ***
+RDSW   =6.043e+02
+CDSC   =0.000e+00 CDSCB  =0.000e+00 CDSCD  =8.448e-05
+PRWB   =0.000e+00 PRWG   =0.000e+00 CIT    =1.000e-03
*        *** Process and parameters extraction related model parameters ***
+TOX     =7.700e-09 NGATE  =0.000e+00
+NLX    =1.918e-07
+XL     =5.000e-08 XW     =0.000e+00
*        *** Substrate current related model parameters ***
+ALPHA0 =0.000e+00 BETA0  =3.000e+01
*        *** Noise effect related model parameters ***
+AF     =1.400e+00 KF     =2.810e-27 EF     =1.000e+00
+NOIA   =1.000e+20 NOIB   =5.000e+04 NOIC   =-1.40e-12
+NLEV   =0
*        *** Common extrinsic model parameters ***
+ACM    =2
+RD     =0.000e+00 RS     =0.000e+00 RSH    =8.200e+01
+RDC    =0.000e+00 RSC    =0.000e+00
+LINT   =8.285e-09  WINT   =2.676e-08
+LDIF   =0.000e+00 HDIF   =6.000e-07 WMLT   =1.000e+00
+LMLT   =1.000e+00 XJ     =3.000e-07
+JS     =2.000e-05 JSW    =0.000e+00 IS     =0.000e+00
+N      =1.000e+00 NDS    =1000. VNDS   =-1.000e+00
+CBD    =0.000e+00 CBS    =0.000e+00 CJ      =9.300e-04
+CJSW    =2.800e-10 FC     =0.000e+00
+MJ      =3.100e-01 MJSW   =1.900e-01 TT     =0.000e+00
+PB      =6.900e-01 PHP    =6.900e-01
* ---------------------------------------------------------------
```

```
.MODEL MODP PMOS LEVEL=49
* ---------------------------------------------------------------------
************************ SIMULATION PARAMETERS ************************
* ---------------------------------------------------------------------
* format    : HSPICE
* model     : MOS BSIM3v3
* process   : CMOS 0.35 microns
* ---------------------------------------------------------------------
*                          TYPICAL MEAN CONDITION
* ---------------------------------------------------------------------
*
*        *** Flags ***
+MOBMOD =1.000e+00 CAPMOD =2.000e+00 NOIMOD =1.000e+00 VERSION=3.11
*        *** Threshold voltage related model parameters ***
+K1      =5.675e-01
+K2      =-4.39e-02 K3     =4.540e+00 K3B    =-8.52e-01
+NCH     =1.032e+17 VTH0   =-6.17e-01
+VOFF    =-1.13e-01 DVT0   =1.482e+00 DVT1   =3.884e-01
+DVT2    =-1.15e-02 KETA   =-2.56e-02
+PSCBE1 =1.000e+09 PSCBE2 =1.000e-08
+DVT0W   =0.000e+00 DVT1W  =0.000e+00 DVT2W  =0.000e+00
*        *** Mobility related model parameters ***
+UA      =2.120e-10 UB     =8.290e-19 UC     =-5.28e-11
+U0      =1.296e+02
*        *** Subthreshold related parameters ***
+DSUB    =5.000e-01 ETA0   =2.293e-01 ETAB   =-3.92e-03
+NFACTOR=8.237e-01
```

```
*         *** Saturation related parameters ***
+EM      =4.100e+07 PCLM    =2.979e+00
+PDIBLC1=3.310e-02 PDIBLC2=1.000e-09 DROUT  =5.000e-01
+A0      =1.423e+00 A1      =0.000e+00 A2     =1.000e+00
+PVAG    =0.000e+00 VSAT    =2.000e+05 AGS    =3.482e-01
+B0      =2.719e-07 B1      =0.000e+00 DELTA  =1.000e-02
+PDIBLCB=-1.78e-02
*         *** Geometry modulation related parameters ***
+W0      =4.894e-08 DLC     =2.900e-08
+DWC     =3.845e-08 DWB     =0.000e+00 DWG    =0.000e+00
+LL      =0.000e+00 LW      =0.000e+00 LWL    =0.000e+00
+LLN     =1.000e+00 LWN     =1.000e+00 WL     =0.000e+00
+WW      =0.000e+00 WWL     =0.000e+00 WLN    =1.000e+00
+WWN     =1.000e+00
*         *** Temperature effect parameters ***
+TNOM    =27.0 AT      =3.300e+04 UTE    =-1.35e+00
+KT1     =-5.70e-01 KT2     =2.200e-02 KT1L   =0.000e+00
+UA1     =0.000e+00 UB1     =0.000e+00 UC1    =0.000e+00
+PRT     =0.000e+00
*         *** Overlap capacitance related and dynamic model parameters   ***
+CGDO    =7.420e-11 CGSO    =7.420e-11 CGBO   =1.100e-10
+CGDL    =1.290e-10 CGSL    =1.290e-10 CKAPPA =6.000e-01
+CF      =0.000e+00 ELM     =5.000e+00
+XPART   =1.000e+00 CLC     =1.000e-15 CLE    =6.000e-01
```

```
*        *** Parasitic resistance and capacitance related model parameters ***
+RDSW    =1.853e+03
+CDSC    =6.994e-04 CDSCB  =2.943e-04 CDSCD  =1.970e-04
+PRWB    =0.000e+00 PRWG   =0.000e+00 CIT    =1.173e-04
*        *** Process and parameters extraction related model parameters ***
+TOX     =7.700e-09 NGATE  =0.000e+00
+NLX     =1.770e-07
+XL      =5.000e-08 XW     =0.000e+00
*        *** Substrate current related model parameters ***
+ALPHA0 =0.000e+00 BETA0  =3.000e+01
*        *** Noise effect related model parameters ***
+AF      =1.290e+00 KF     =1.090e-27 EF     =1.000e+00
+NOIA    =1.000e+20 NOIB   =5.000e+04 NOIC   =-1.40e-12
+NLEV    =0
*        *** Common extrinsic model parameters ***
+ACM     =2
+RD      =0.000e+00 RS     =0.000e+00 RSH    =1.560e+02
+RDC     =0.000e+00 RSC    =0.000e+00
+LINT    =-5.64e-08  WINT   =3.845e-08
+LDIF    =0.000e+00 HDIF   =6.000e-07 WMLT   =1.000e+00
+LMLT    =1.000e+00 XJ     =3.000e-07
+JS      =2.000e-05 JSW    =0.000e+00 IS     =0.000e+00
+N       =1.000e+00 NDS    =1000. VNDS   =-1.000e+00
+CBD     =0.000e+00 CBS    =0.000e+00 CJ      =1.420e-03
+CJSW    =3.800e-10 FC     =0.000e+00
+MJ      =5.500e-01 MJSW   =3.900e-01 TT     =0.000e+00
+PB      =1.020e+00 PHP    =1.020e+00
```

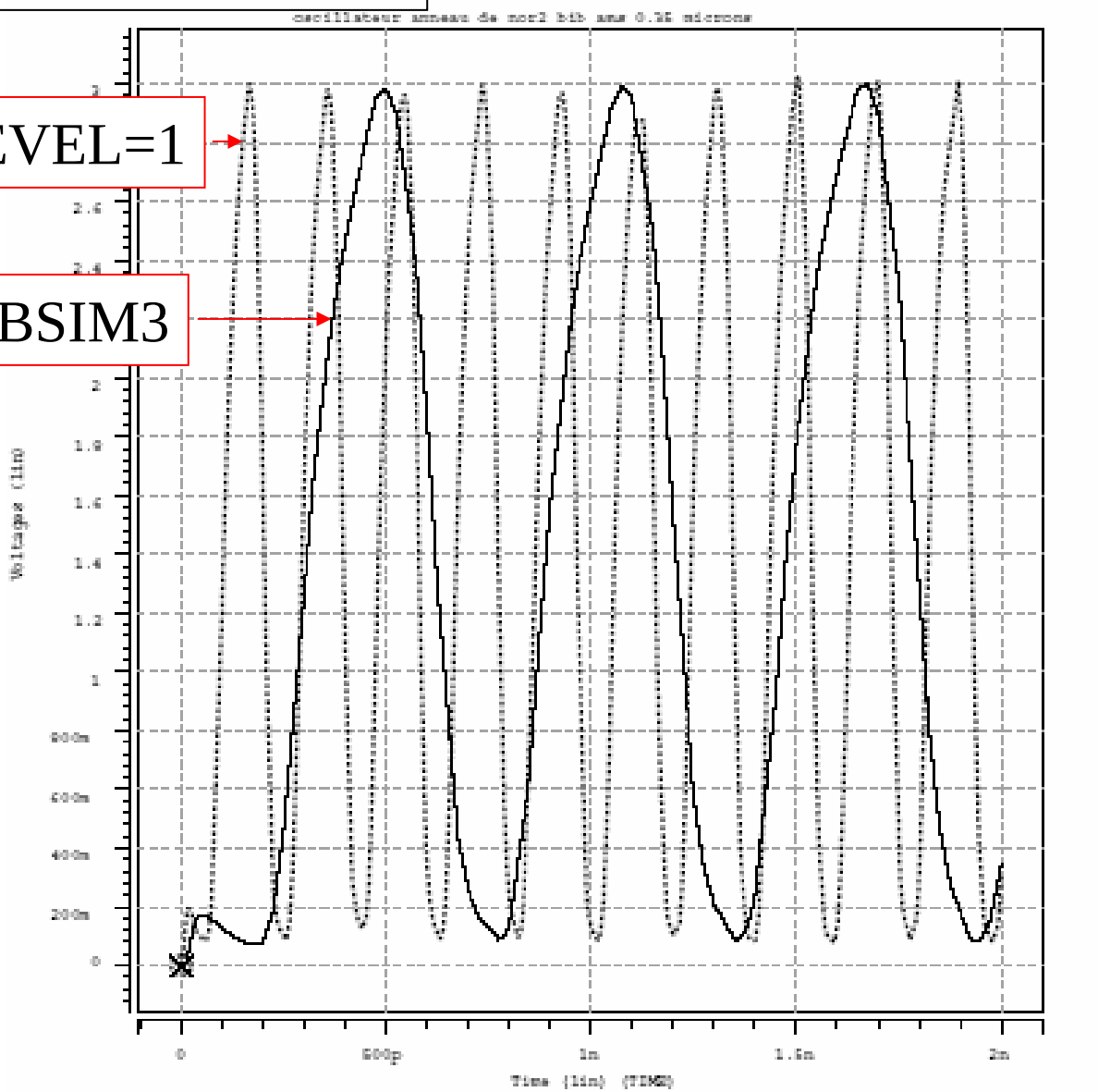
Oscillateur en anneau: 3 portes NOR2

CMOS 0.35µ

Modèles:
- BSIM3
- Level 1

tm+td = T / N

N: nb d'étages (impair)



Edit Options View Orientation Media Help

hp6.prn Page: "3" 3 of 18

Extraction Procedure

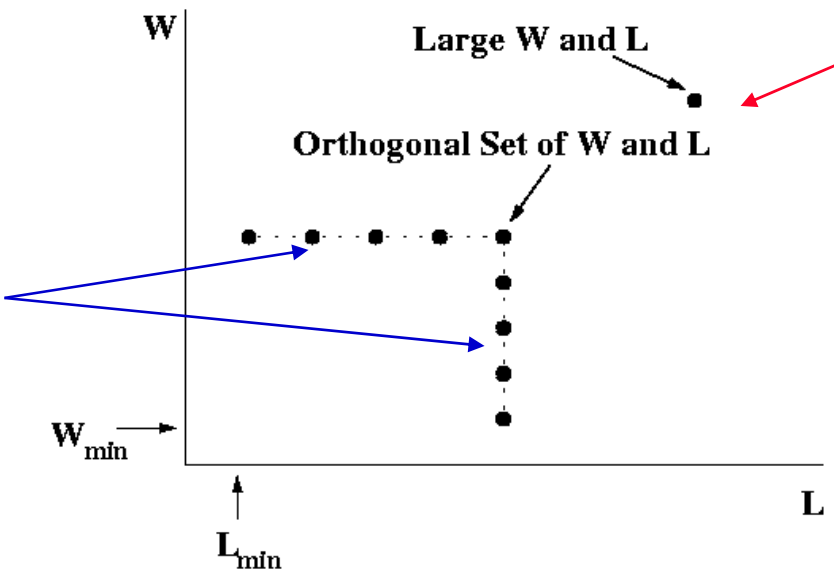
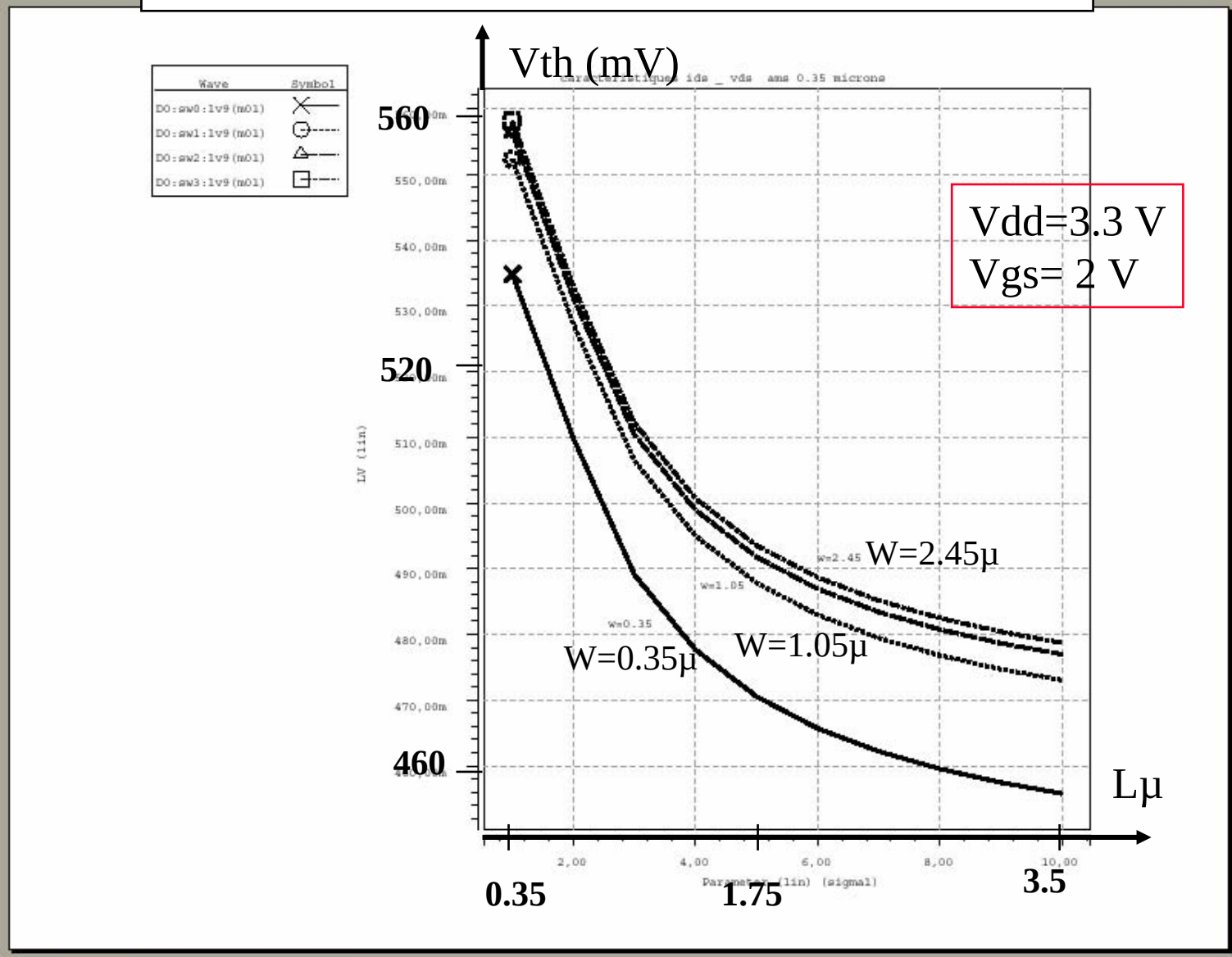


Figure 6-1. Device geometries used for parameter extraction

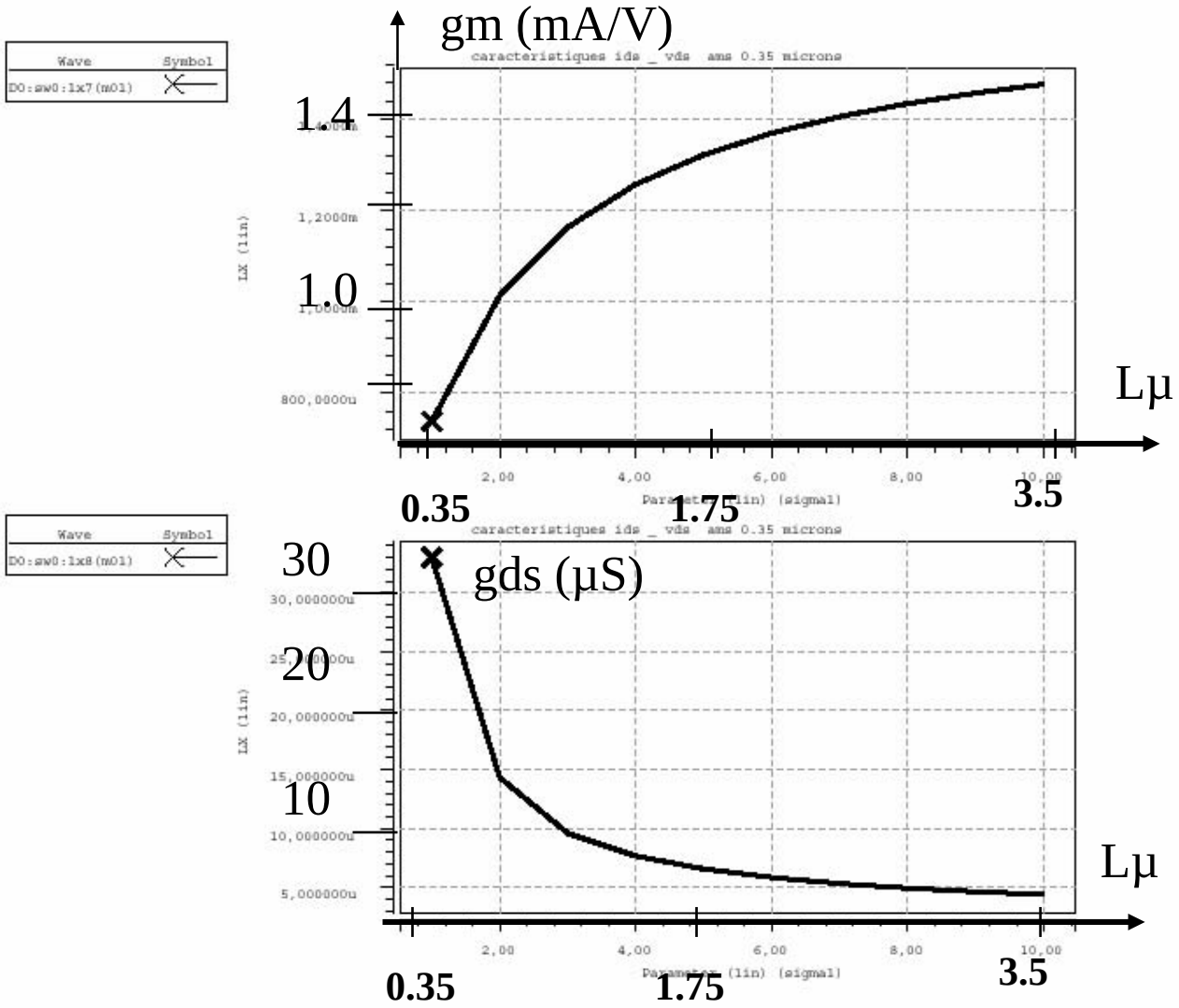
Modèle simplifié
➔ Paramètres de base

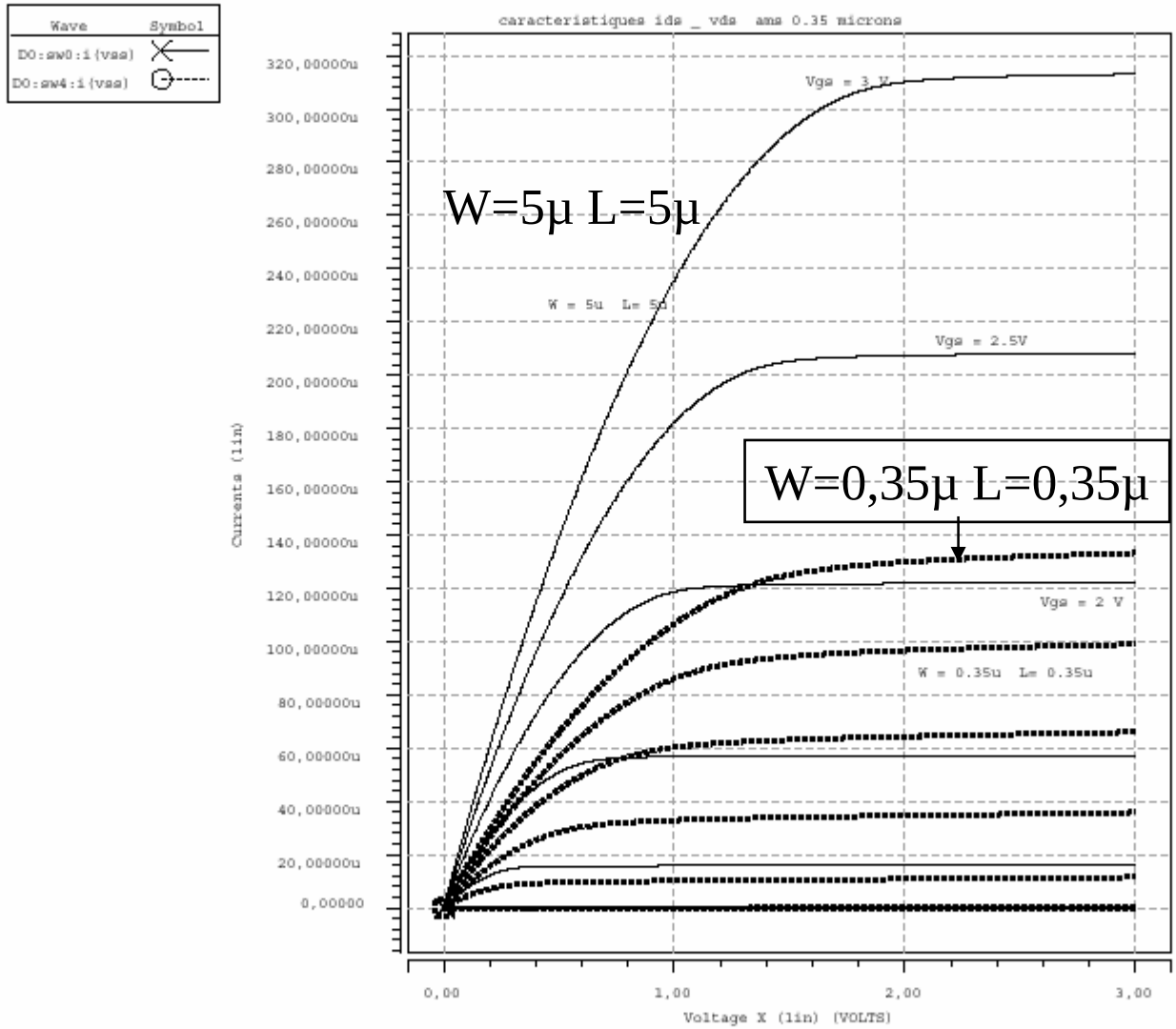
Influence de W et L sur les paramètres
ex: Vt (W,L)

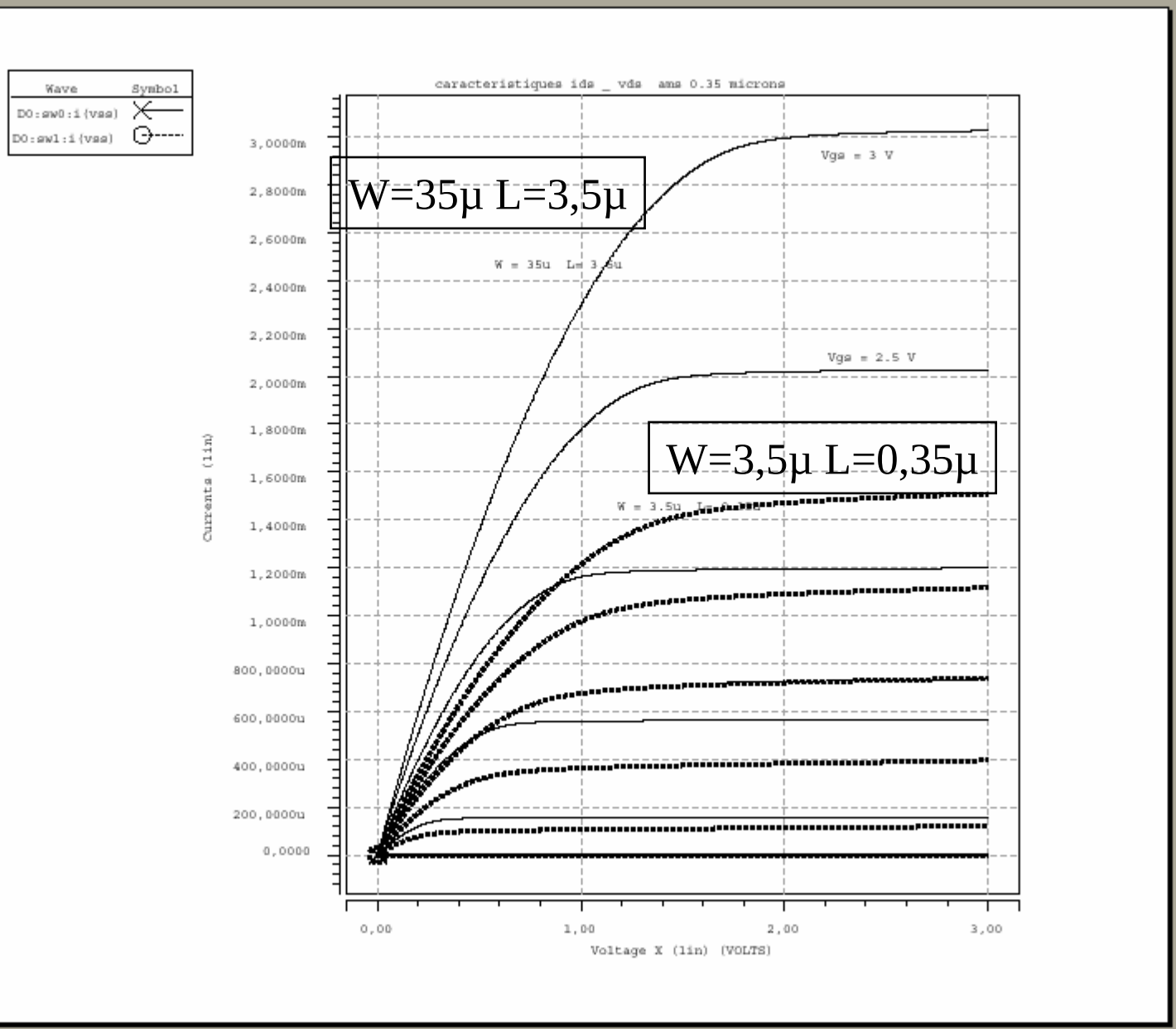
n_MOS (0.35µ) : Modèle BSIM3
Variation de la tension de seuil avec L et W

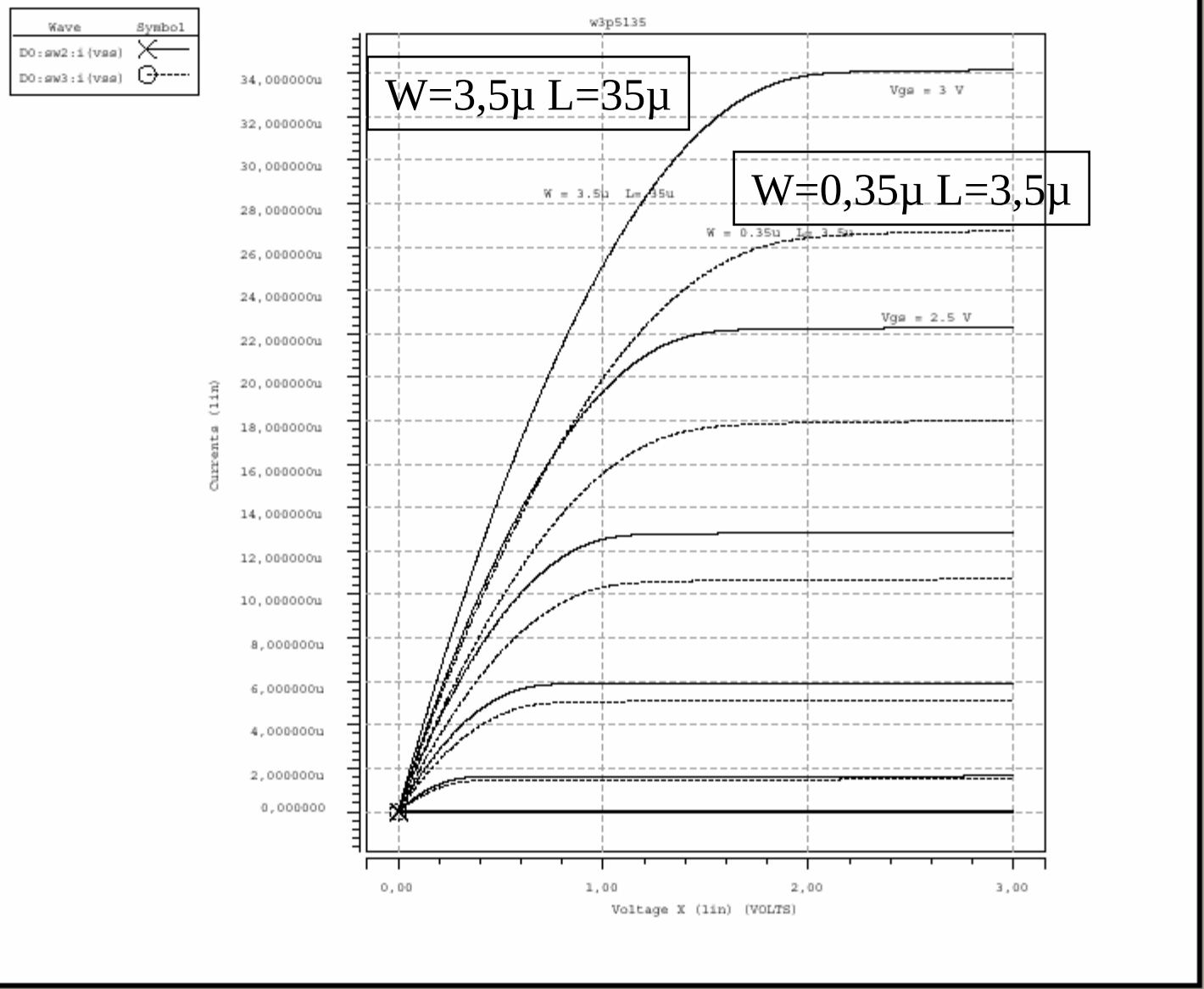


n_MOS (0.35µ) : Modèle BSIM3
Variation de gm et gds avec L (avec W/L=10)



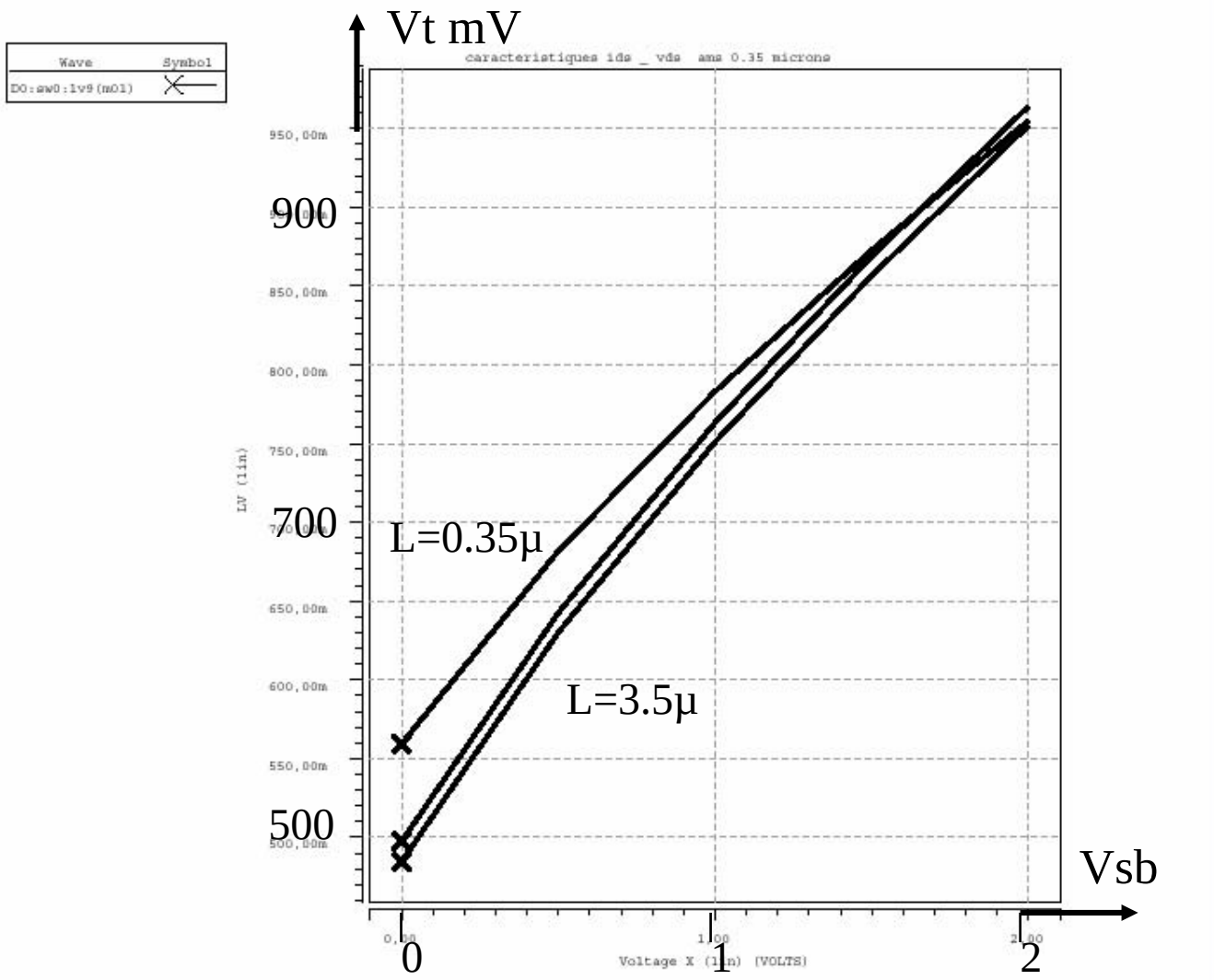


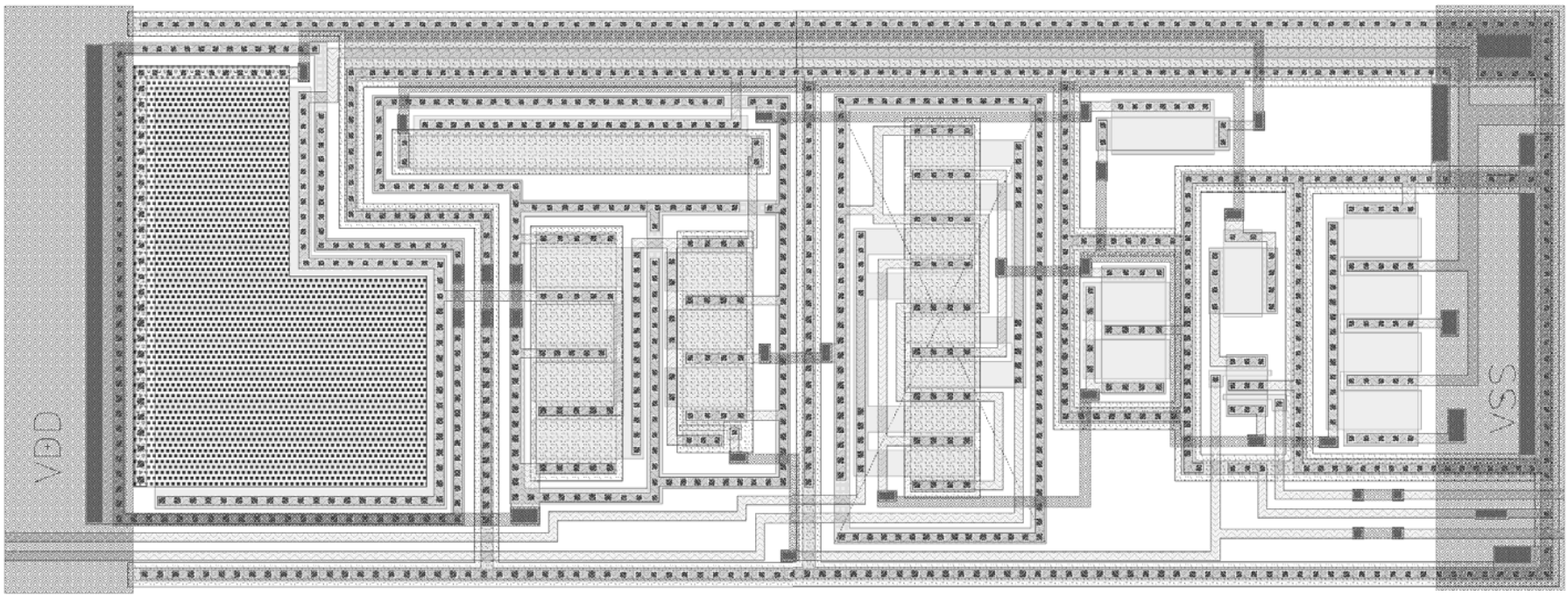

Wave Symbol
DO:sw0:i(vss)
DO:sw1:i(vss)
caracteristiques ids _ vds ams 0.35 microns
W=35µ L=3,5µ
W=3,5µ L=0,35µ
Vgs = 3 V
Vgs = 2.5 V
W = 35u L= 3.5u
W = 3.5u
Currents (lin)
3,0000m
2,8000m
2,6000m
2,4000m
2,2000m
2,0000m
1,8000m
1,6000m
1,4000m
1,2000m
1,0000m
800,0000u
600,0000u
400,0000u
200,0000u
0,0000
0,00
1,00
2,00
3,00
Voltage X (lin) (VOLTS)

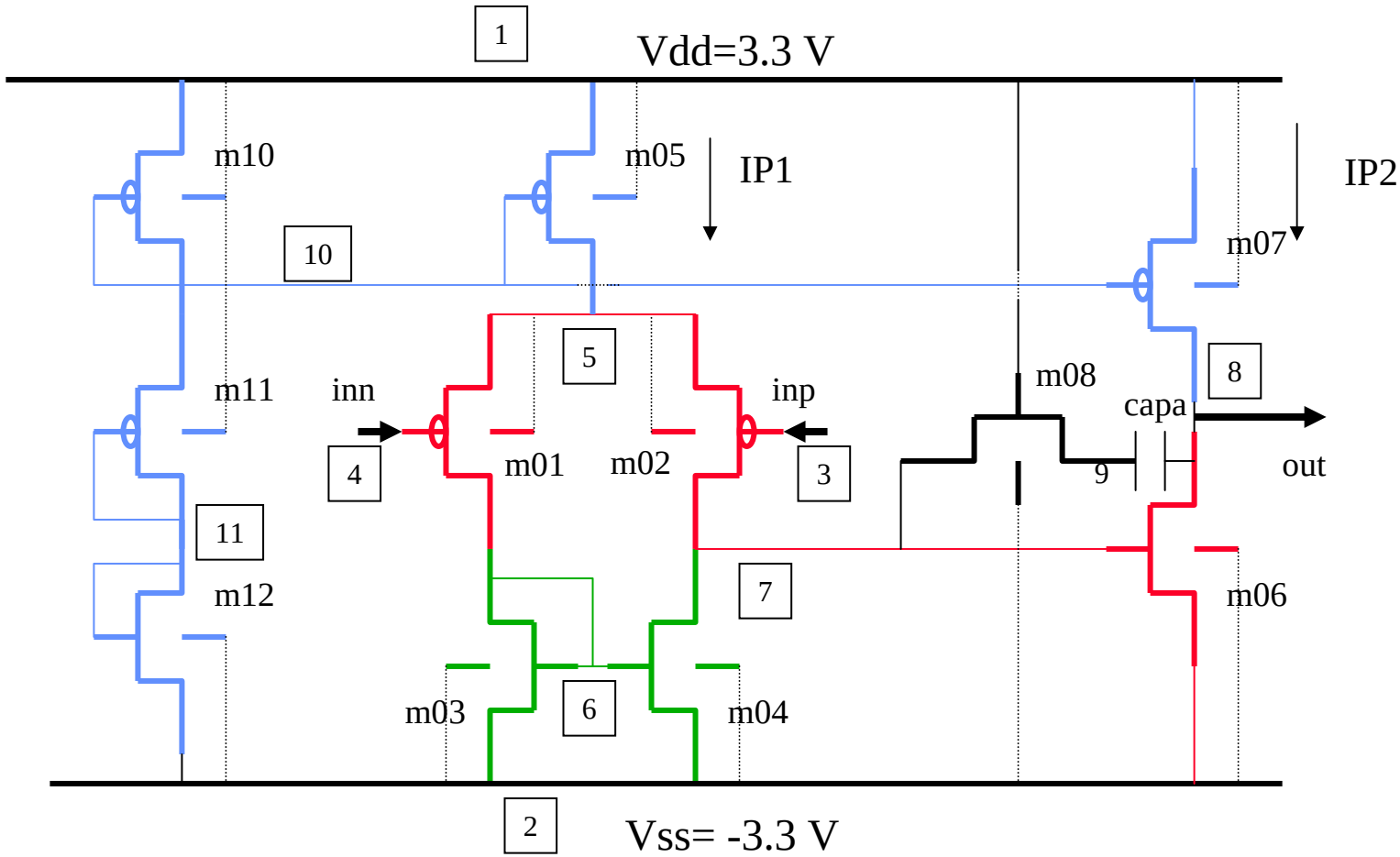


n_MOS (0.35µ) : Modèle BSIM3

Effet substrat: Vt = f(Vsb) (n_MOS, W=3.5u)




VDD
VSS



Lmin = 6µ	IP1= 43µA	IP2= 108µA
Lmin= 0.6µ	IP1= 33µA	IP2= 84µA

Modèle BSIM3V3 CMOS AMS 0.35µ Lmin= 0.6 µ

```
vdd 1 0 dc 3.3
vss 2 0 dc -3.3
m01 6 4 5 5 modp w=4u l=0.4u
m02 7 3 5 5 modp w=4u l=0.4u
m03 6 6 2 2 modn w=0.95u l=0.6u
m04 7 6 2 2 modn w=0.95u l=0.6u
m05 5 10 1 1 modp w=2.0u l=0.6u
m06 8 7 2 2 modn w=4.6u l=0.6u
m07 8 10 1 1 modp w=4.5u l=0.6u
capa 8 9 3.54pF
m08 7 1 9 2 modn w=0.5u l=1.6u
m10 10 10 1 1 modp w=1.0u l=0.6u
m11 11 11 10 1 modp w=0.5u l=5.2u
m12 11 11 2 2 modn w=1.0u l=0.6u
vinp 3 0 dc 0
vinm 4 0 dc 0 ac 1
```

Adobe Acrobat - [AOP.pdf]

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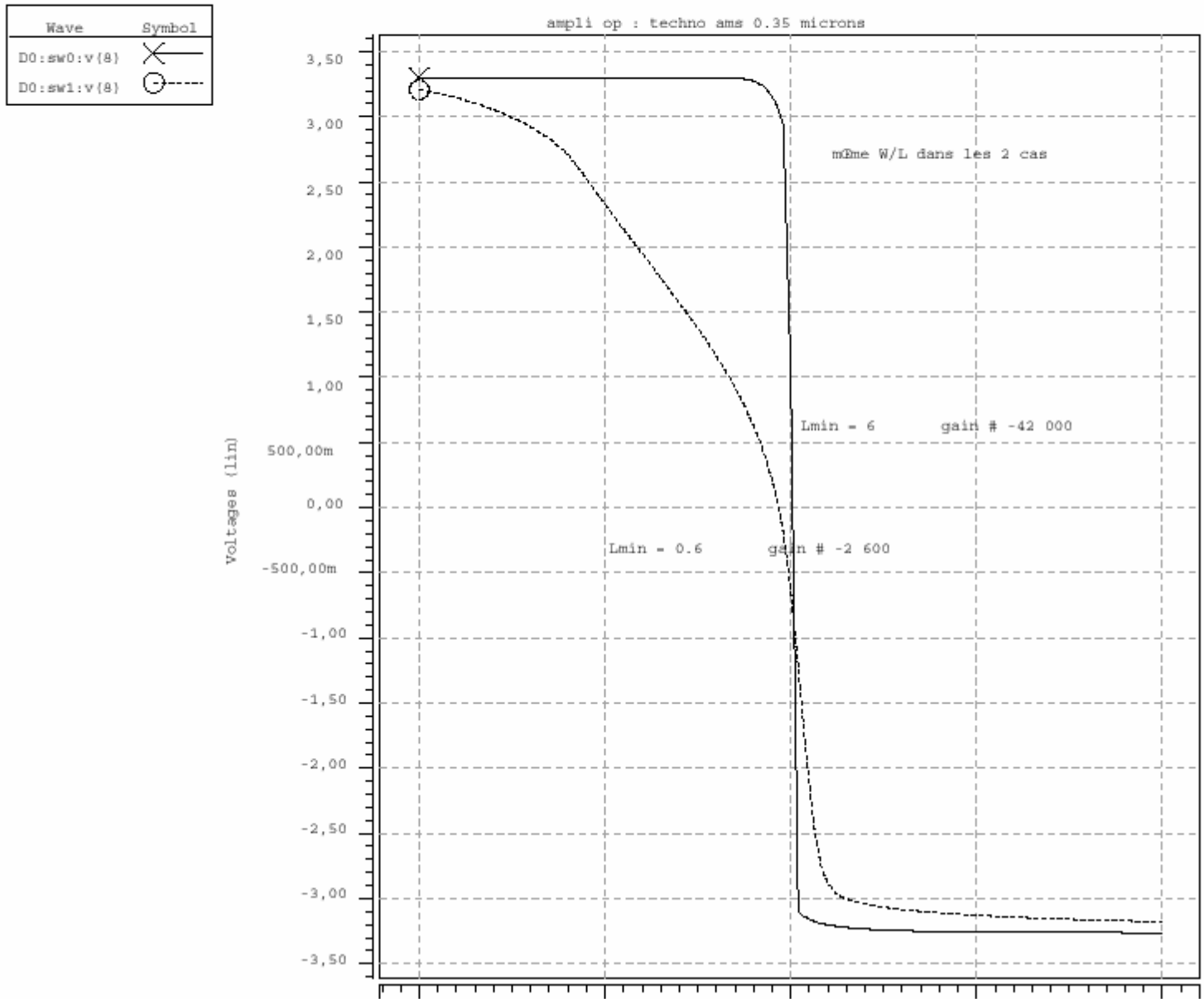
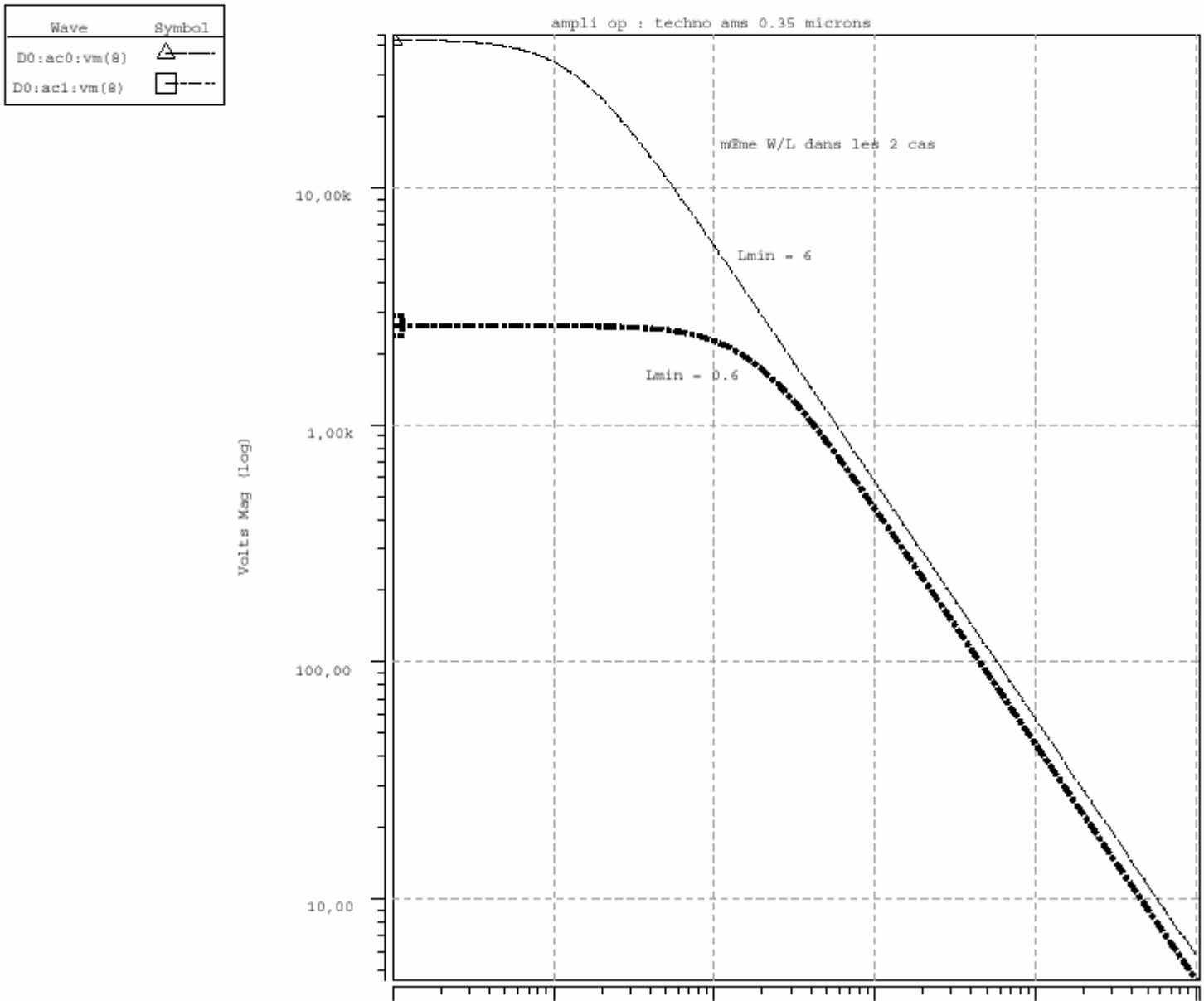




Modèle BSIM3V3 CMOS AMS 0.35µ L = 6 µ

```
vdd 1 0 dc 3.3
vss 2 0 dc -3.3
m01 6 4 5 5 modp w=40u l=4u
m02 7 3 5 5 modp w=40u l=4u
m03 6 6 2 2 modn w=9.5u l=6u
m04 7 6 2 2 modn w=9.5u l=6u
m05 5 10 1 1 modp w=20u l=6u
m06 8 7 2 2 modn w=46u l=6u
m07 8 10 1 1 modp w=50u l=6u
capa 8 9 3.54pF
m08 7 1 9 2 modn w=5u l=16u
m10 10 10 1 1 modp w=10u l=6u
m11 11 11 10 1 modp w=5u l=52u
m12 11 11 2 2 modn w=10u l=6u
vinp 3 0 dc 0
vinm 4 0 dc 0 ac 1
```

CIRCUIT ANALOGIQUE
Amplificateur différentiel CMOS: influence de L

Gain différentiel: ad = gmn / (gon + gop) =

$[2 K (W/L)n]^{1/2} / [(\lambda n + \lambda p)(Ids)^{1/2}]$

(voir cours MEA1)

L diminue (à **W/L=Cte**): L: 5µ ➔ 0,35µ

gmn: 1,5 mA/V ➔ 0,8 mA/V soit gmn / 2

r0 : 200kΩ ➔ 50 kΩ soit r0 * 4

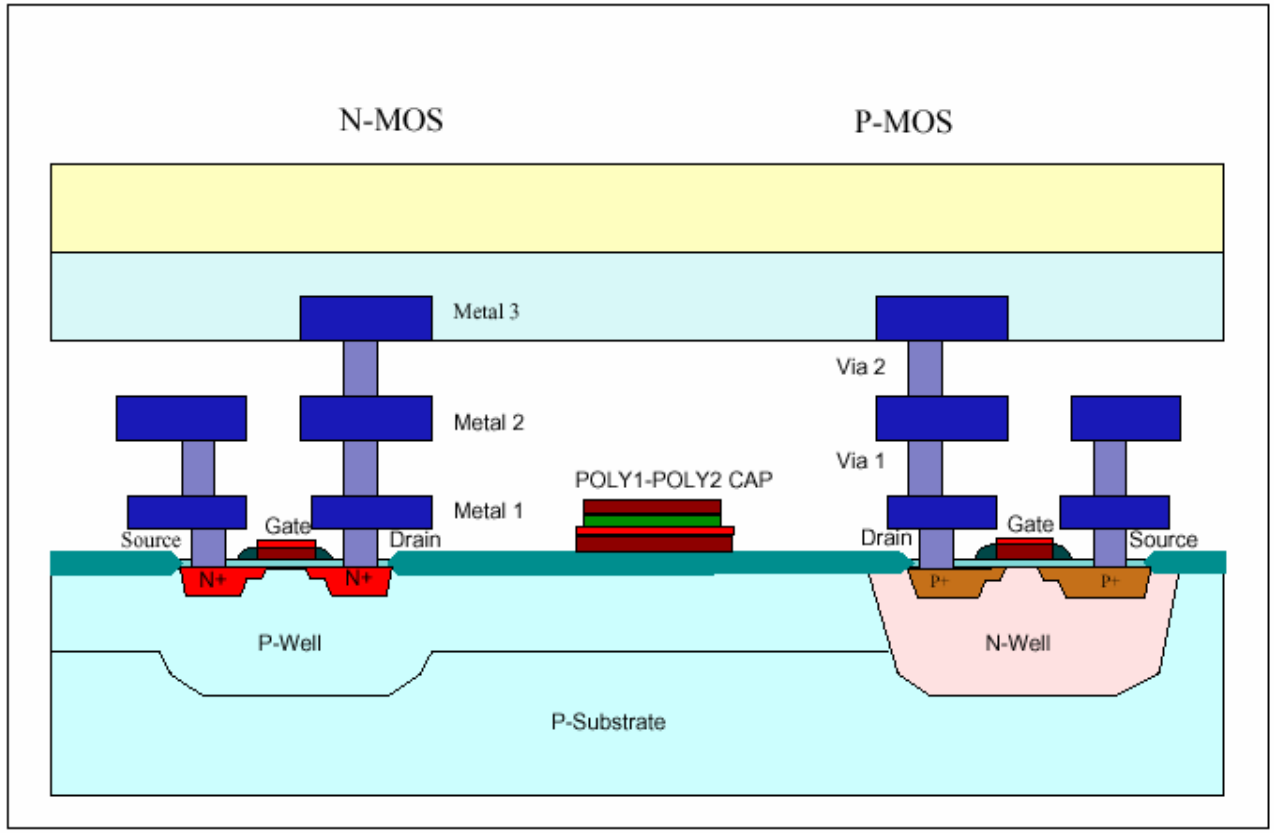
➔ ad / 8 ! (à Ids = Cte)

Amplificateur opérationnel avec 2 étages ➔ **gain / 64!**

Exemple: gain différentiel = 50 000 ➔ gain différentiel ~ 1700 si L~0,35µ !

➔ En analogique: grandes valeurs de L

2.1 Wafer Cross – Section



Adobe Acrobat - [c35_process_2004.pdf]

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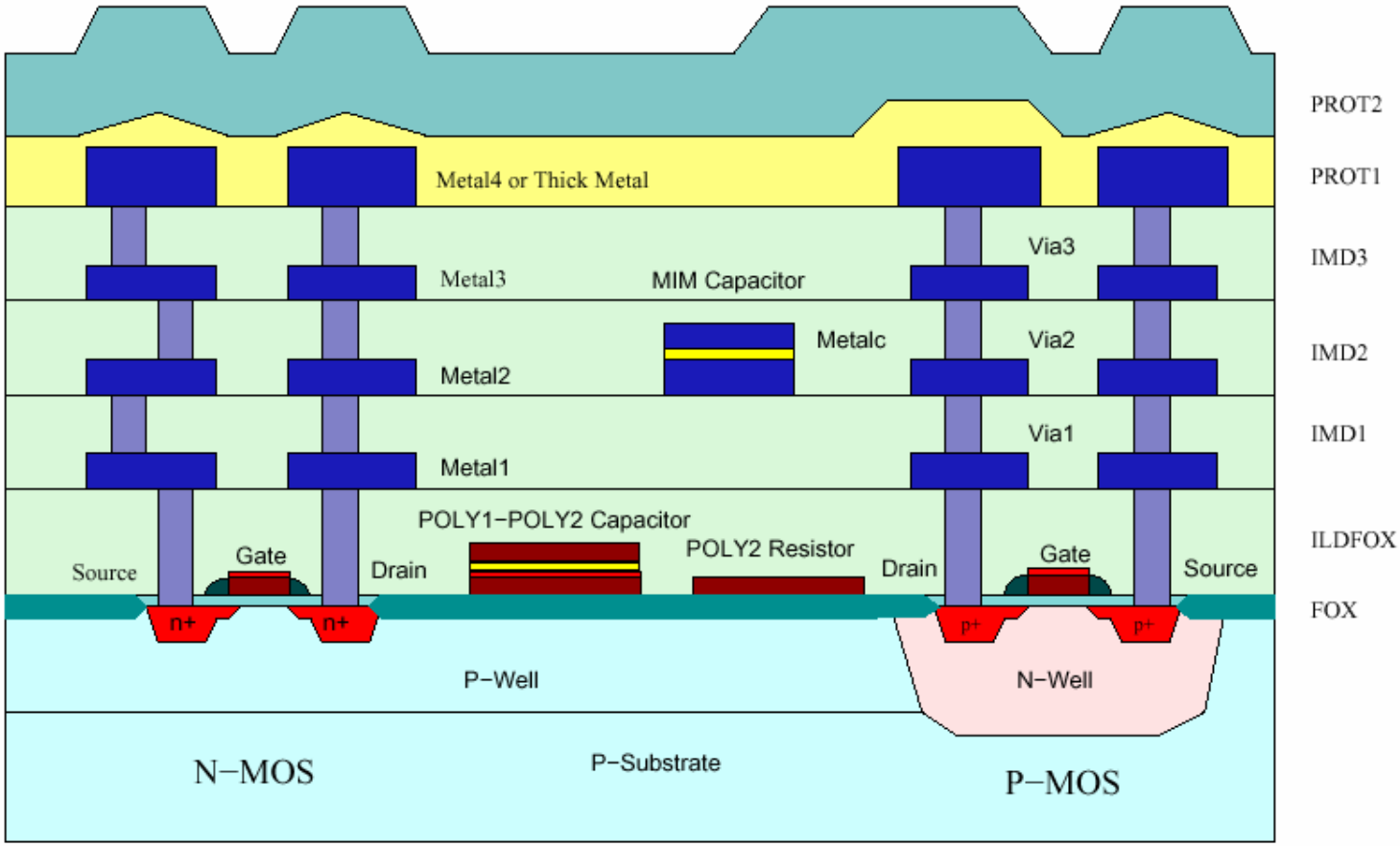
2.1. Wafer Cross – Section

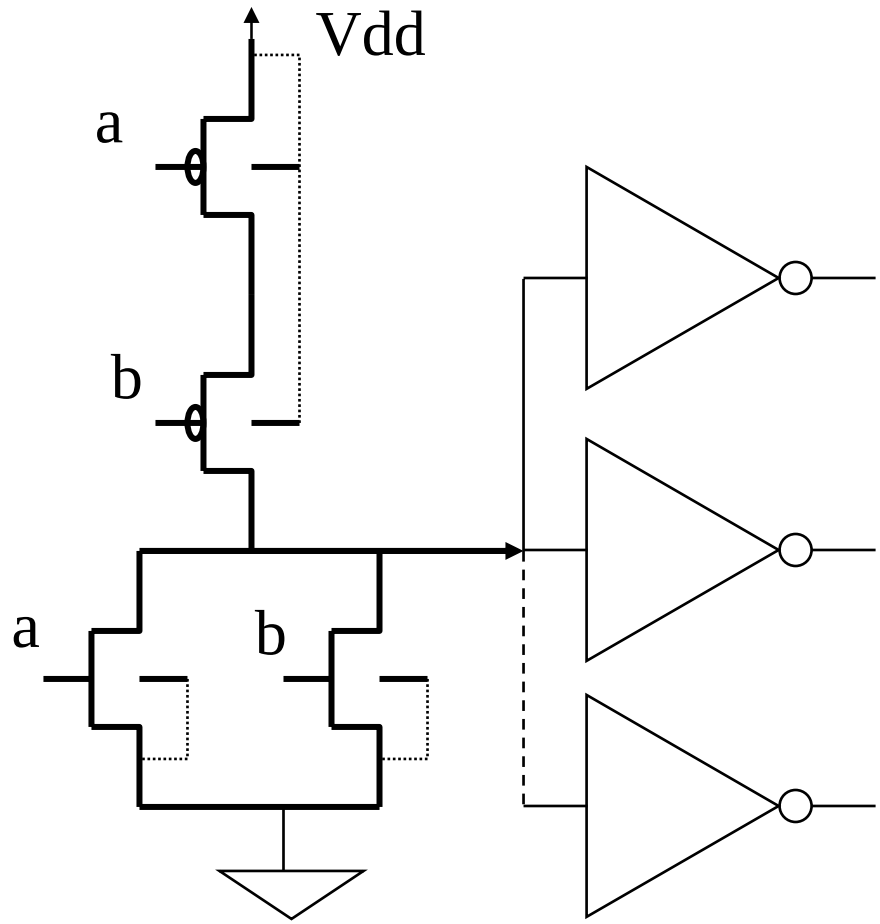


Evolution: C35

161 % 5 of 62 8,26 x 11,69 in

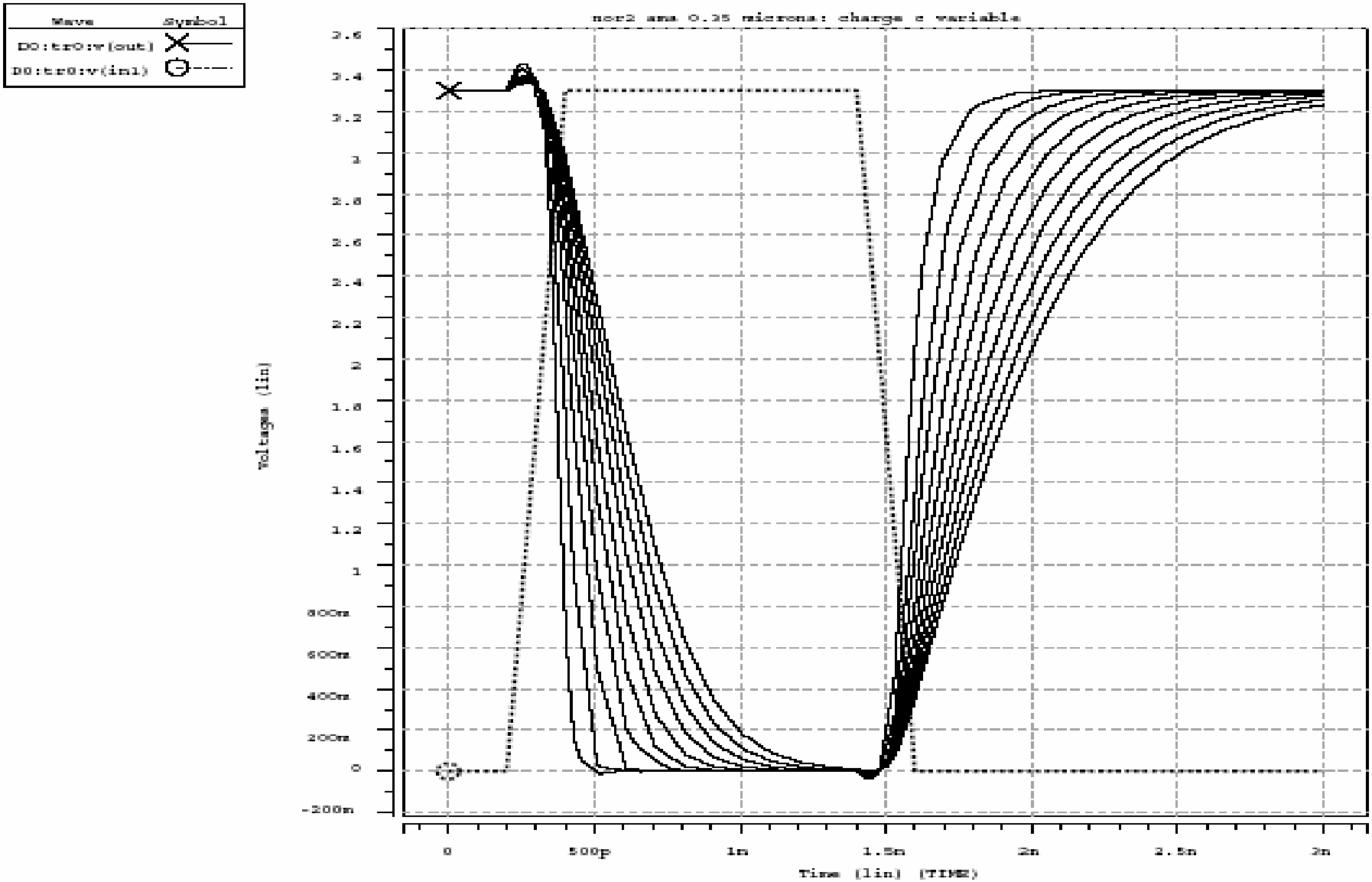
démarrer Eudora Adobe Acrobat - [c35... Microsoft PowerPoint ... FR 15:05

SIMULATION D'UNE PORTE NOR2 CHARGEE PAR N INVERSEURS



Détermination des performances temporelles
***d’une porte NOR2 (technologie AMS 0,35µ)**

```
*chargée par un nombre variable d'inverseurs
.....................
*NOR2 charge par des inverseurs
* modèle BSIM3v3
m1 3 1 0 0 modn w=4u l=0.35u as=4p ad=4p ps=10u pd=10u
m2 3 2 0 0 modn w=4U l=0.35u as=4p ad=4p ps=10u pd =10u
mp1 4 1 3 5 modp w=14U l=0.35u as=14p ad=14p ps=30u pd=30u
mp2 5 2 4 5 modp w=14u l=0.35u  as=14p ad=14p ps =30u pd=30u
mni 6 3 0 0 modn w=4u l=0.35u as=4p ad=4p ps=10u pd=10u
mpi 6 3 5 5 modp w=14u l=0.35u as=14p ad=14p ps=30u pd=30u
mni1 6 3 0 0 modn w=4u l=0.35u as=4p ad=4p ps=10u pd=10u
mpi1 6 3 5 5 modp w=14u l=0.35u as=14p ad=14p ps=30u pd=30u
mn2 6 3 0 0 modn w=4u l=0.35u as=4p ad=4p ps=10u pd=10u
mp3 6 3 5 5 modp w=14u l=0.35u as=14p ad=14p ps=30u pd=30u
mni4 6 3 0 0 modn w=4u l=0.35u as=4p ad=4p ps=10u pd=10u
mpi4 6 3 5 5 modp w=14u l=0.35u as=14p ad=14p ps=30u pd=30u
mn5 6 3 0 0 modn w=4u l=0.35u as=4p ad=4p ps=10u pd=10u
mp5 6 3 5 5 modp w=14u l=0.35u as=14p ad=14p ps=30u pd=30u
vp 5 0 dc 3.3
v1 1 0 pulse 0 3.3 200p 100p 100p 1n
v2 2 0 dc 0
.op
.tran 50p 3n
.......................
==================================================
```




```
.tran 20p 3n sweep capa 1ff 300ff 30ff
```

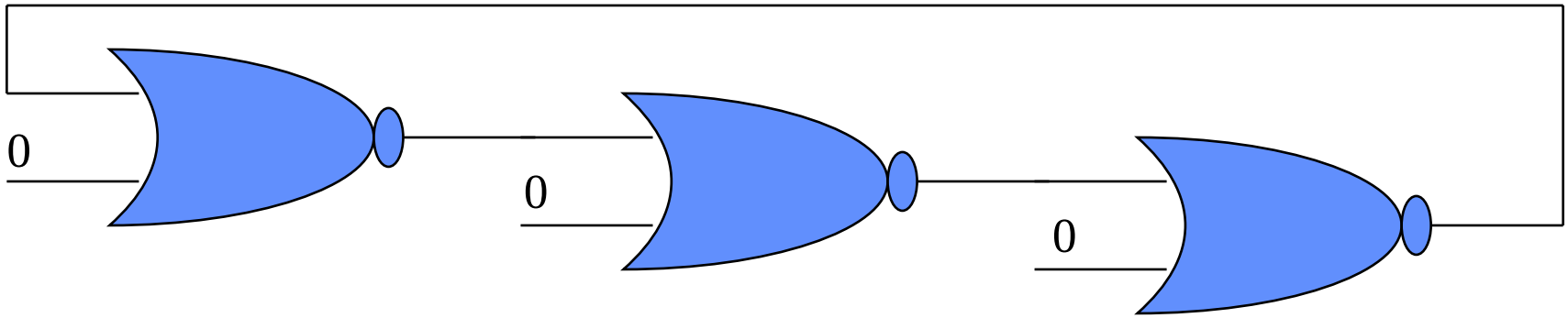
```
CELL(NOR20
// model section
   TIMING_Model(ioDelayRiseModel0
      (Spline
         (INPUT_SLEW_AXIS 0.05 0.5 2 4)
         (LOAD_AXIS 0.0005 0.0025 0.01 0.04 0.16)
            data
               (
                  (0.094 0.115 0.191 0.495 1.704)
                  (0.138 0.161 0.242 0.538 1.742)
                  (0.234 0.27 0.381 0.719 1.895)
                  (0.323 0.368 0.511 0.919 2.135)
               ************************************

    TIMING_Model(SlopeRiseModel0
          (Spline
             (INPUT_SLEW_AXIS 0.05 0.5 2 4)
             (LOAD_AXIS 0.0005 0.0025 0.01 0.04 0.16)
                data
                   (
                      (0.175 0.225 0.414 1.182 4.251)
                      (0.241 0.281 0.443 1.179 4.236)
                      (0.511 0.561 0.713 1.348 4.221)
                      (0.802 0.873 1.08 1.714 4.386)
```

ns
pF

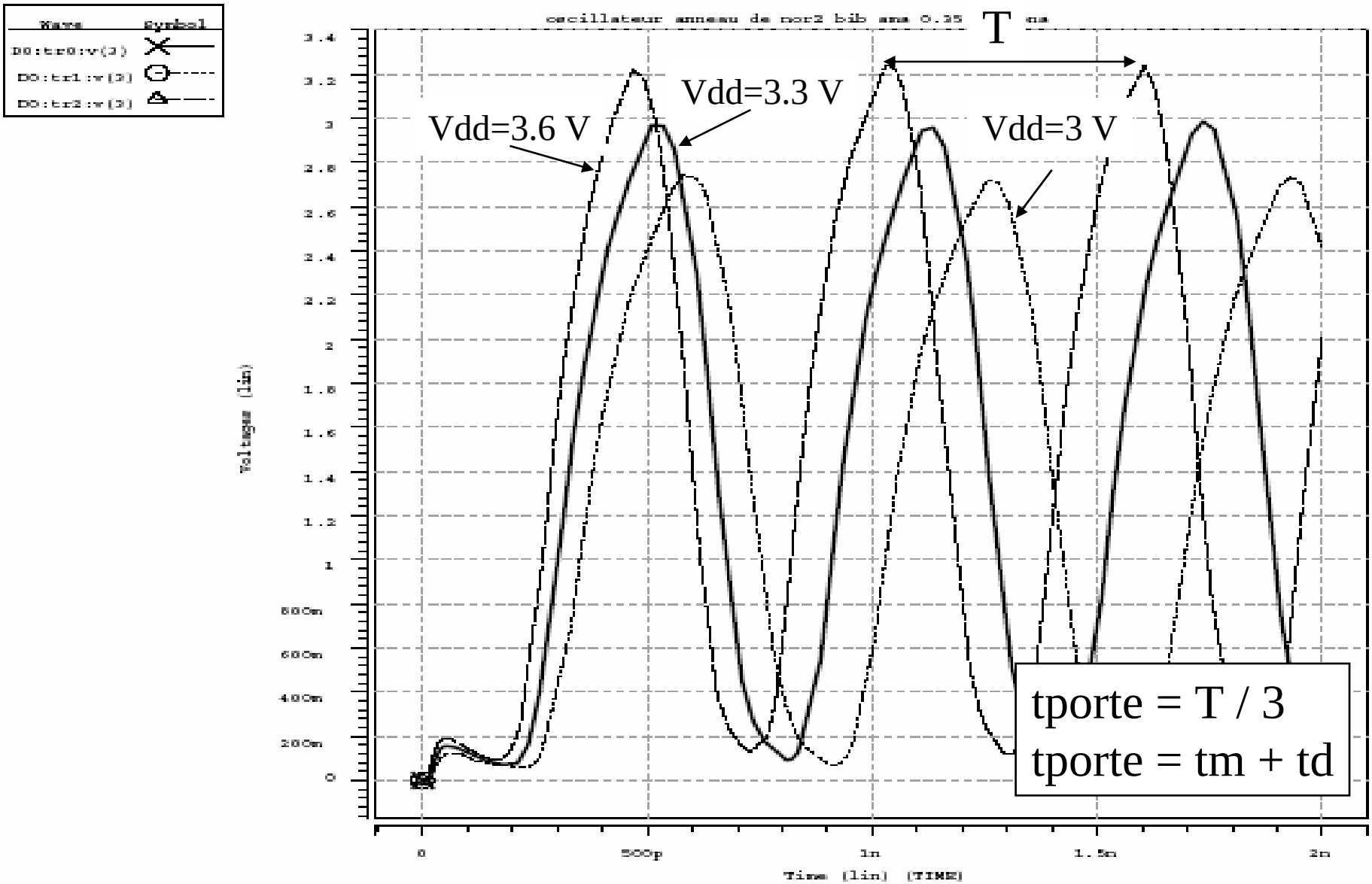
Capa de charge

Temps comm. entrée

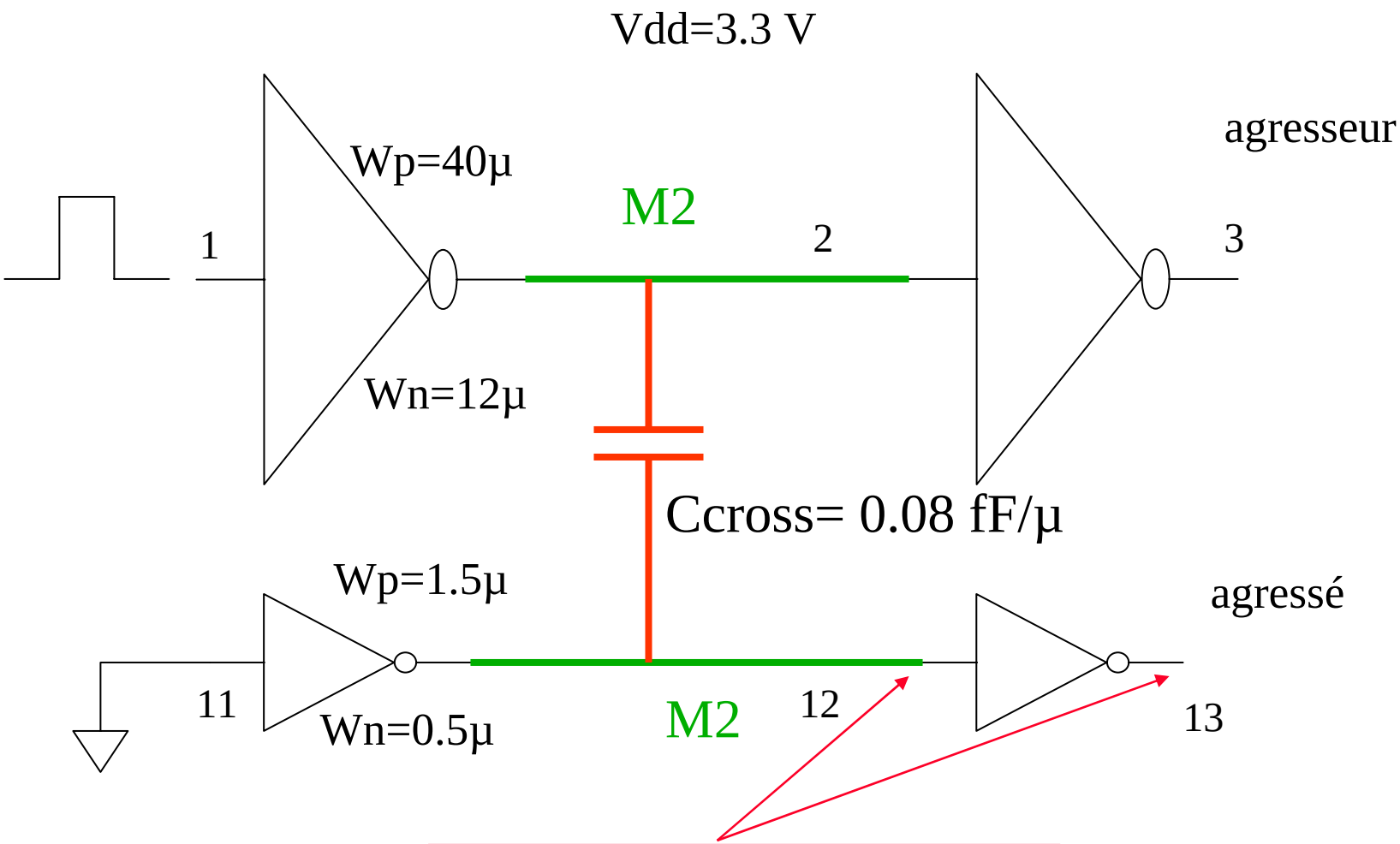
Path(A => Q 10 01 DELAY(ioDelayRiseModel0) SLEW(SlopeRiseModel0))



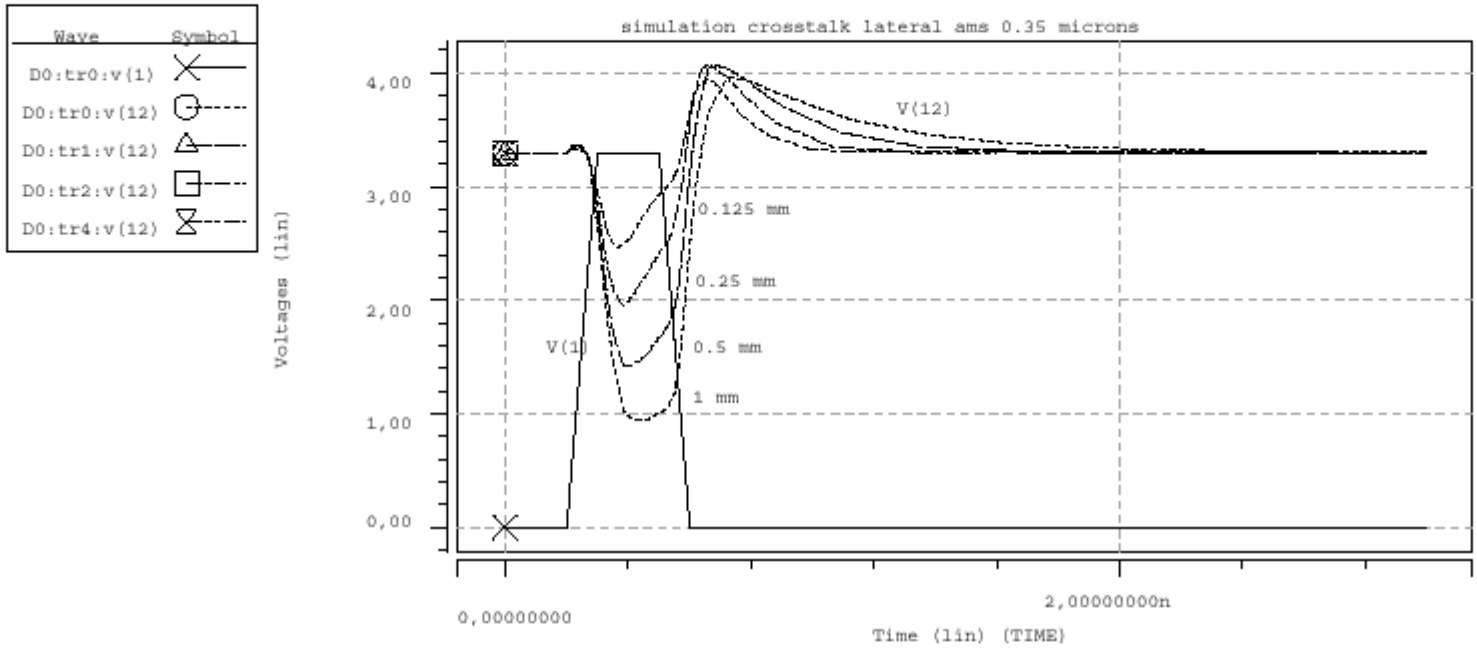

```
.......................
*oscillateur en anneau: 3 NOR2 reboucles
* modèle BSIM3v3
m1 3 1 0 0 modn w=4u l=0.35u as=4p ad=4p ps=10u pd=10u
m2 3 2 0 0 modn w=4U l=0.35u as=4p ad=4p ps=10u pd =10u
mp1 4 1 3 5 modp w=14U l=0.35u as=14p ad=14p ps=30u pd=30u
mp2 5 2 4 5 modp w=14u l=0.35u as=14p ad=14p ps =30u pd=30u

m11 33 3 0 0 modn w=4u l=0.35u as=4p ad=4p ps=10u pd=10u
m22 33 2 0 0 modn w=4U l=0.35u as=4p ad=4p ps=10u pd =10u
mp11 44 3 33 5 modp w=14U l=0.35u as=14p ad=14p ps=30u pd=30u
mp22 5 2 44 5 modp w=14u l=0.35u as=14p ad=14p ps =30u pd=30u

m111 1 33 0 0 modn w=4u l=0.35u as=4p ad=4p ps=10u pd=10u
m222 1 2 0 0 modn w=4U l=0.35u as=4p ad=4p ps=10u pd =10u
mp111 444 33 1 5 modp w=14U l=0.35u as=14p ad=14p ps=30u pd=30u
mp222 5 2 444 5 modp w=14u l=0.35u as=14p ad=14p ps =30u pd=30u
vp 5 0 dc 3.3
v2 2 0 dc 0
.ic v(1)=3.3 v(3)=0
.tran 20p 2ns uic
.....................
```

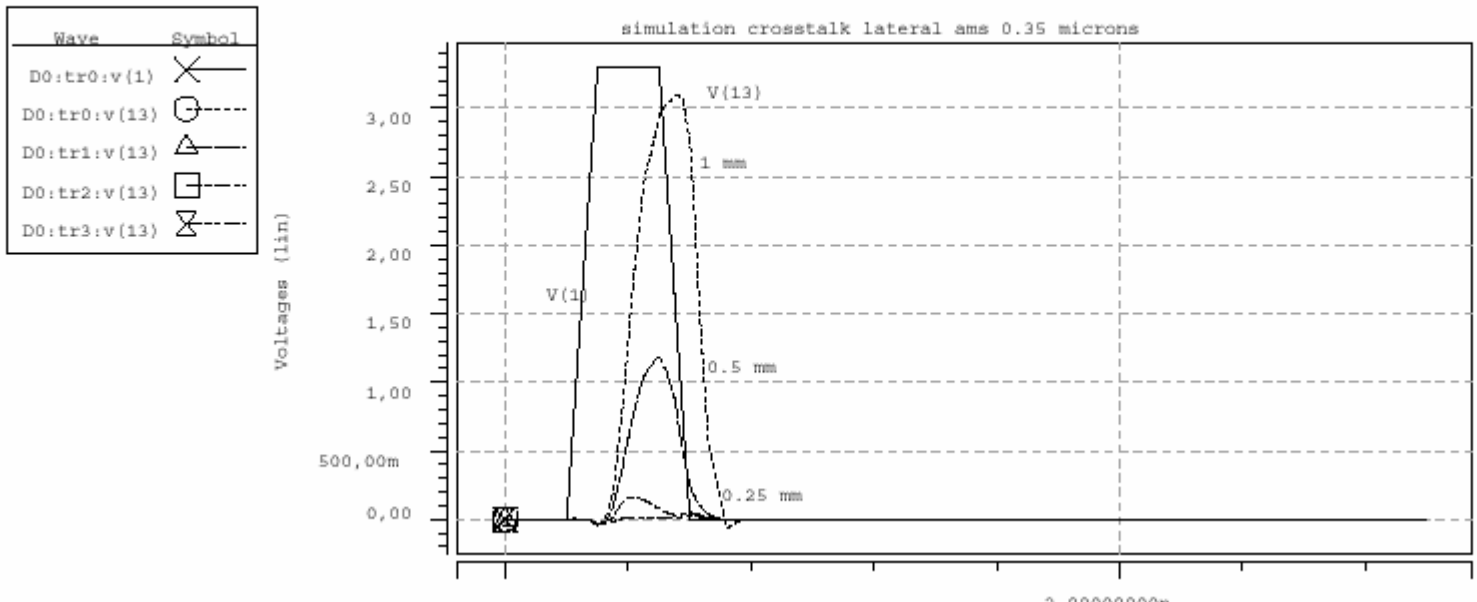

Name
Symbol
D0:tr0:v(3)
D0:tr1:v(3)
D0:tr2:v(3)
oscillateur anneau de nor2 bib ams 0.35
T
ns
Vdd=3.6 V
Vdd=3.3 V
Vdd=3 V
tporte = T / 3
tporte = tm + td
Voltage (lin)
Time (lin) (TIME)
3.4
3.2
3
2.8
2.6
2.4
2.2
2
1.8
1.6
1.4
1.2
1
800m
600m
400m
200m
0
0
500p
1n
1.5n
2n

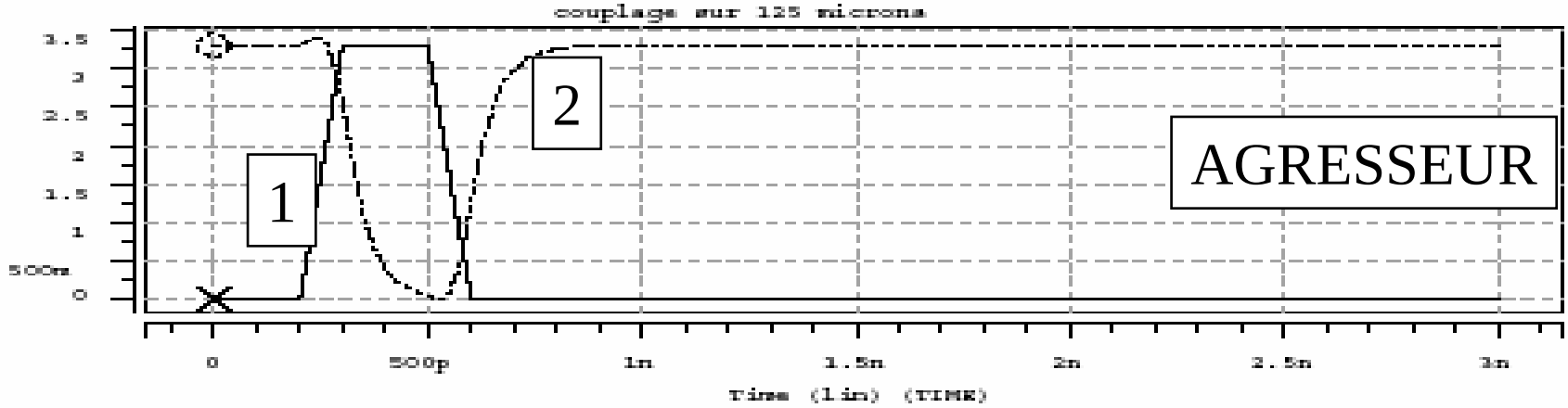
CMOS AMS 0.35µ : crosstalk latéral métal-métal

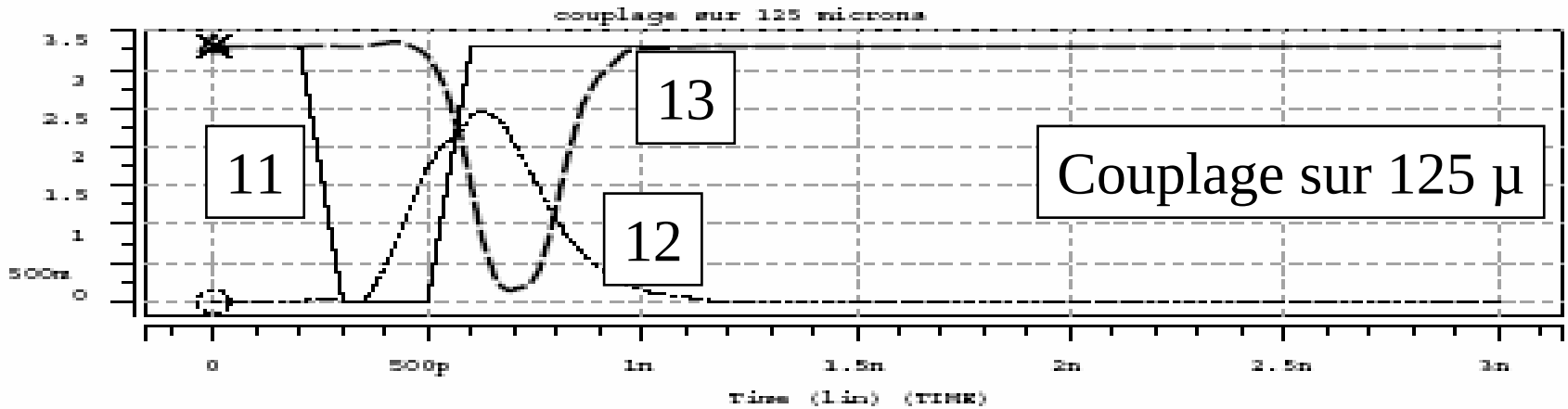


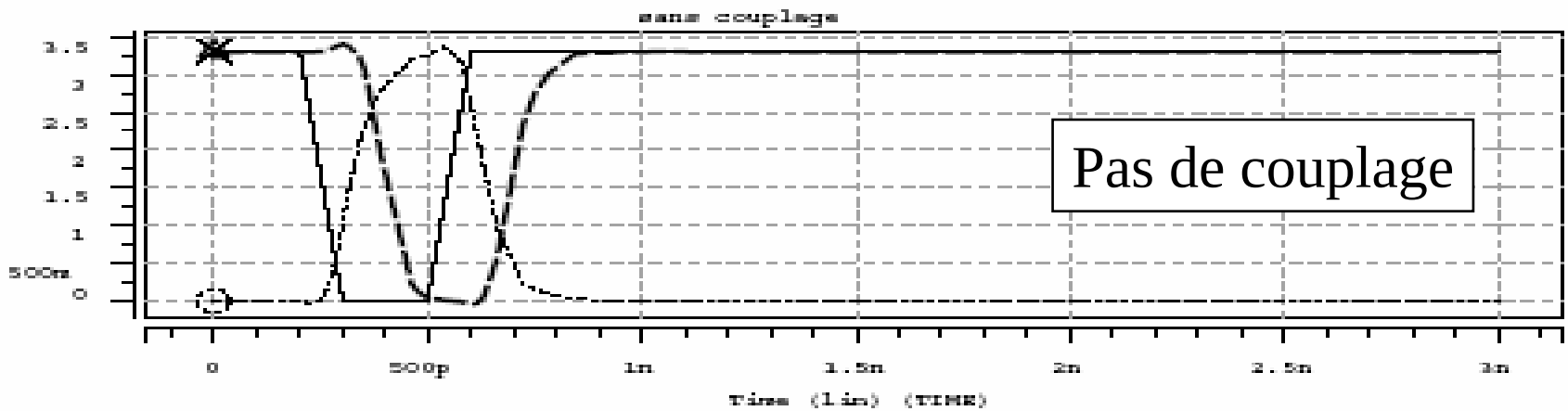
Intégrité du signal !…?



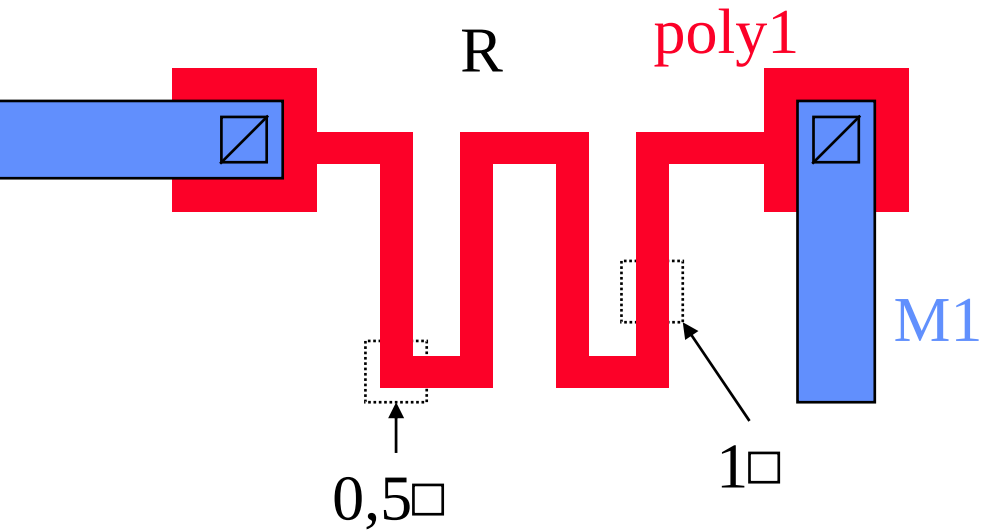


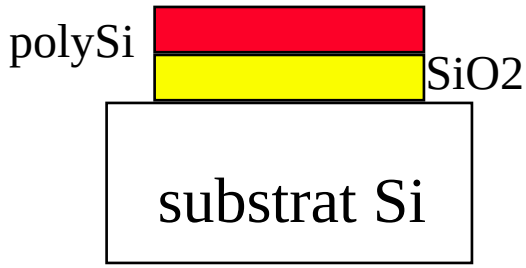

couplage sur 125 microns
1
2
AGRESSEUR
Time (lin) (TIME)


couplage sur 125 microns
11
13
12
Couplage sur 125 µ
Time (lin) (TIME)

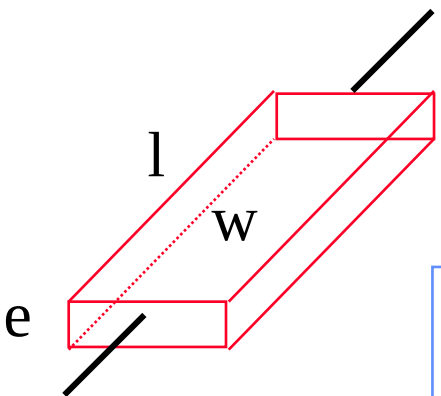

sans couplage
Pas de couplage
Time (lin) (TIME)

RESISTANCE : technologie CMOS (niveau poly1 ou poly2)



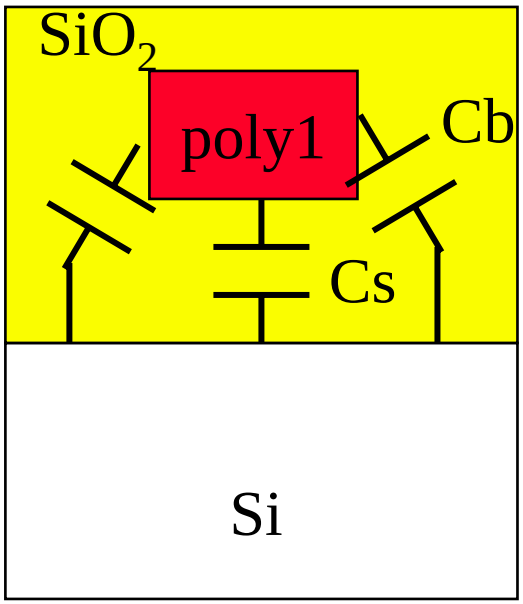


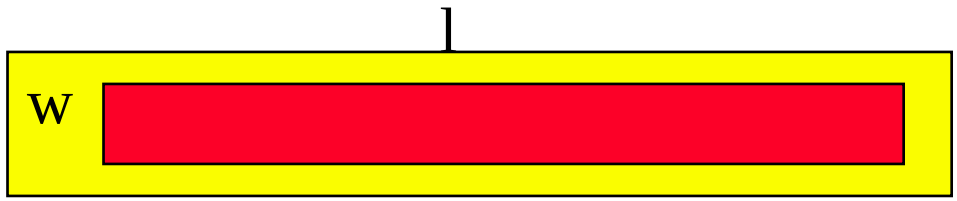
CMOS 0.35µ
Rpoly1 ~ 7 Ω/carré
Rpoly2 ~ 50 Ω/carré



$$R = \rho / e \cdot l / w = R_{\square} \cdot \text{nb carrés}$$

RESISTANCE : technologie CMOS (capacités parasites)



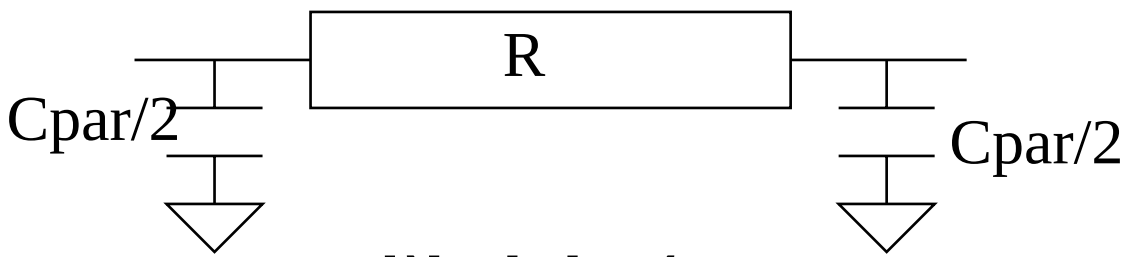


R = nb. carrés * Rcarré

Cpar= w*l* Cs + (2l + 2w)*Cb

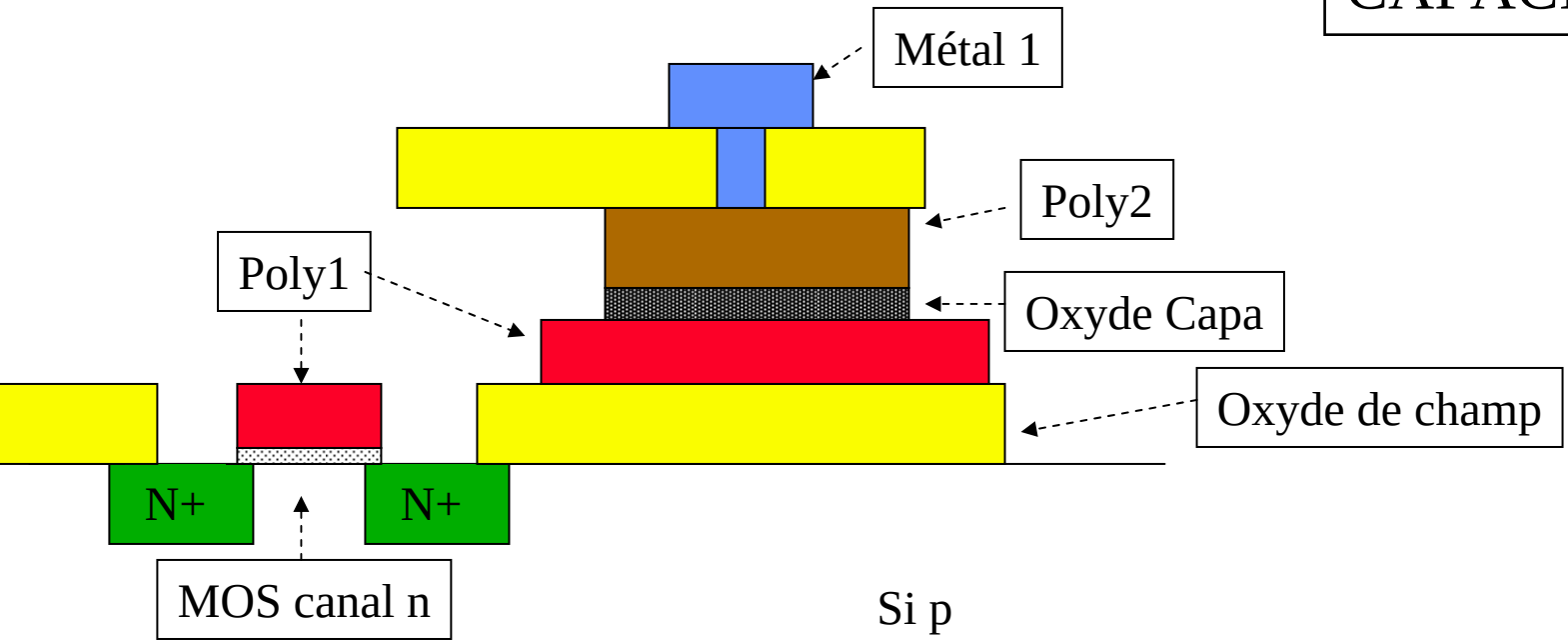
Cs: capacité surfacique
Cb: capacité de bord

CMOS 0.35µ:
Cs ~ 0.12 fF/ µ²
Cb ~ 0.05 fF / µ
Tc1 ~ 1000 ppm/°K



Modèle de la résistance

CAPACITE MOS



$C = Cs * l*l + Cb*4*l$

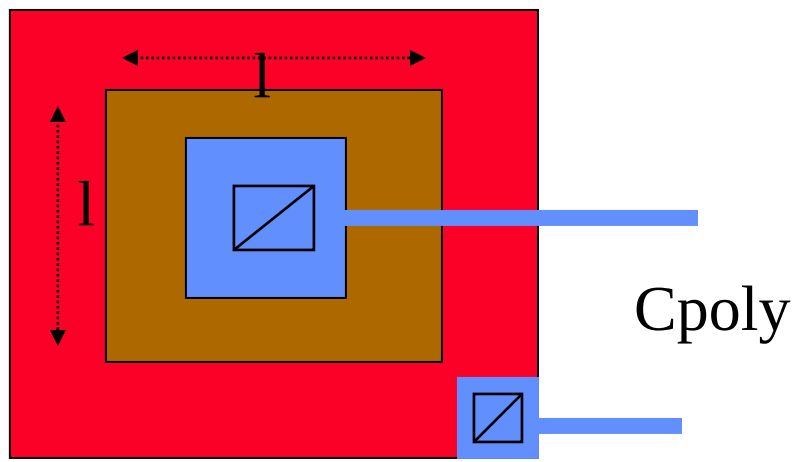
CMOS 0.35µ:

$Cs \sim 0.8\ fF / \mu^2$

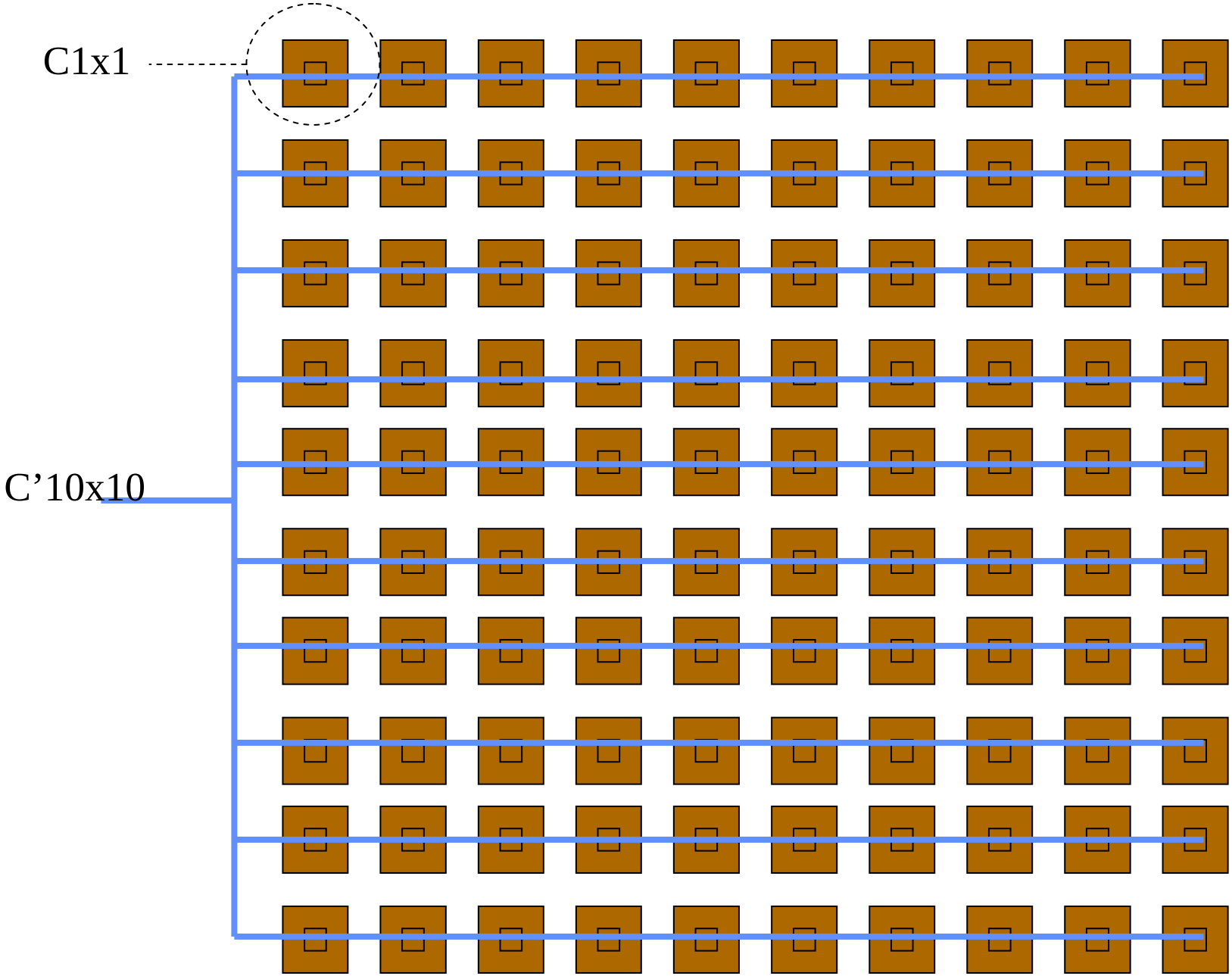
$Cb \sim 0.08\ fF / \mu$

$l=2\mu \rightarrow C= 3.2fF + 0.64fF$

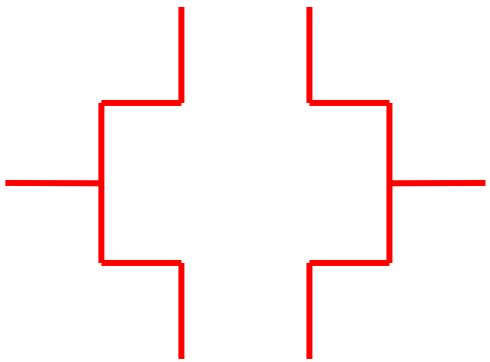
$l=1\mu \rightarrow C= 0.8fF + 0.32fF$

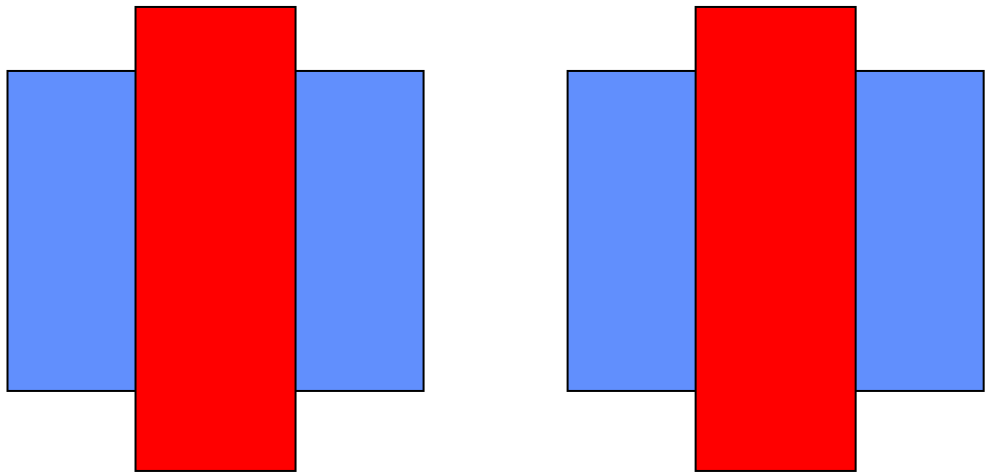


Capacité MOS partitionnée: compensation des capacités de bord

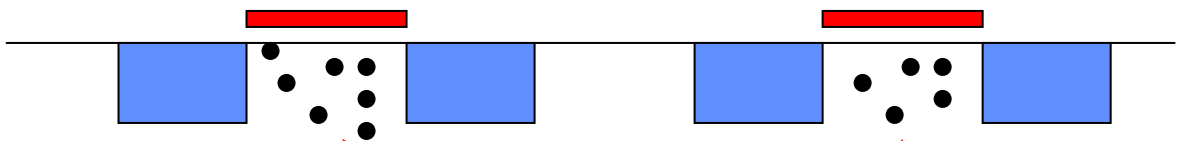


CMOS: dispersion intra-circuit des paramètres des transistors
Exemple:dispersion de la tension de seuil
Simulation monte-carlo





W et L diminuent :
➔ ΔVth augmente



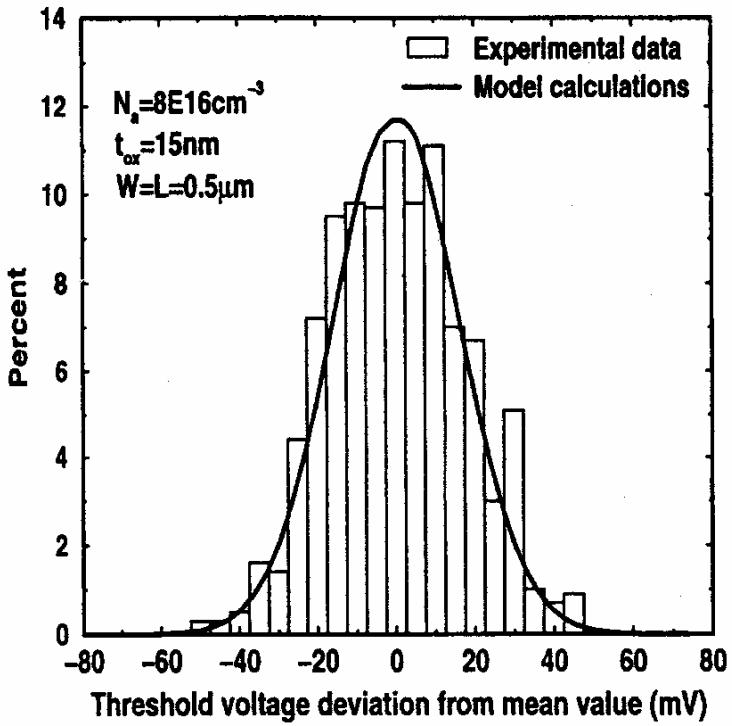
Fluctuation spatiale du dopant
➔ fluctuation de Vth

CMOS: dispersion intra-circuit des paramètres des transistors
Exemple:dispersion de la tension de seuil

TANG *et al.*: INTRINSIC MOSFET PARAMETER FLUCTUATIONS

IEEE trans.on VLSI Systems, vol5, n°4, dec. 1997

Modélisation de Vth:
➔ loi normale (gaussienne)



(a)

L (μm)	W (μm)	$\overline{N_a}$ (cm^{-3})	t_{ox} (nm)	$\delta V_{tsexperimental}$ (mV)	$\delta V_{tsmodel}$ (mV)
0.3	1.0	7.16E16	10	11	13
0.5	1.0	7.16E16	10	7	9

(b)

CMOS: dispersion intra-circuit des paramètres des transistors
dispersion de la tension de seuil pour différentes technologies
(prévisions ITRS)

Wmin et Lmin diminuent :
➔ ΔVth/Vth0 augmente

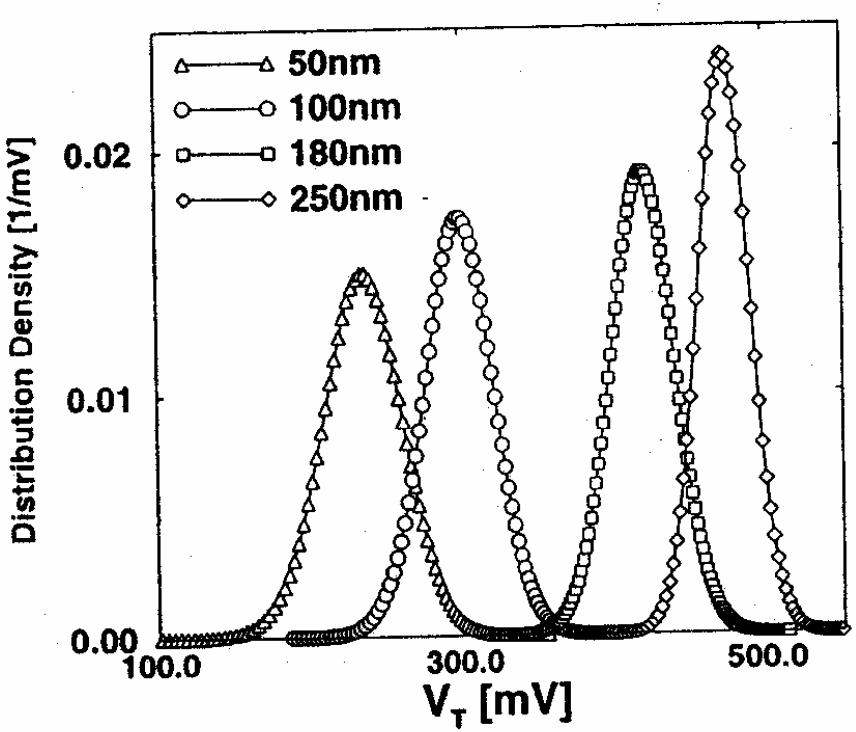


Fig. 7. Distribution density functions for threshold voltage for each of the 1997 NTRS generations using models from [3].

A.J. Bhavnagarwala and al, IEEE J. of Solid State Circuits, Vol 36, n° 4,April 2001

CMOS: dispersion intra-circuit des paramètres des transistors

"Mismatch" dû à la variation spatiale de Vth

Exemple: technologie CMOS 0,35µ

Variation de Vth entre 2 transistors de même dimensions:

$$\sigma^2 (Vth) = (\Delta Vth)^2 / (W*L)$$

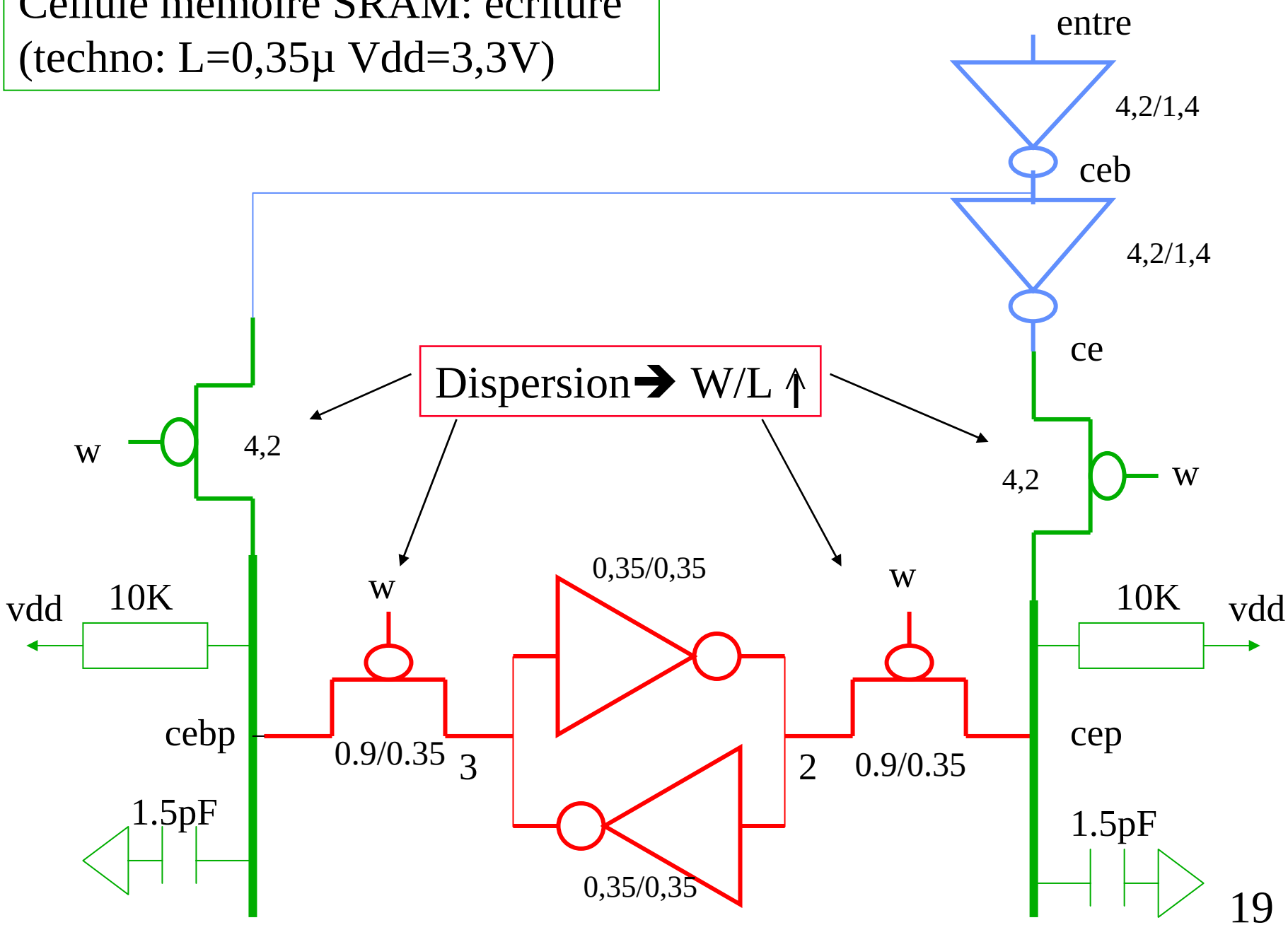
nMOS: $\Delta Vth = 9.6$ mV.µm

pMOS: $\Delta Vth = 16$ mV.µm

Description Hspice:

```
.param dvth='0.0096/(1e6*sqrt(w*l))'
.param vth=agauss (0.465,dvth,1)
```

Cellule mémoire SRAM: écriture (techno: L=0,35µ Vdd=3,3V)



Hspice: description du circuit

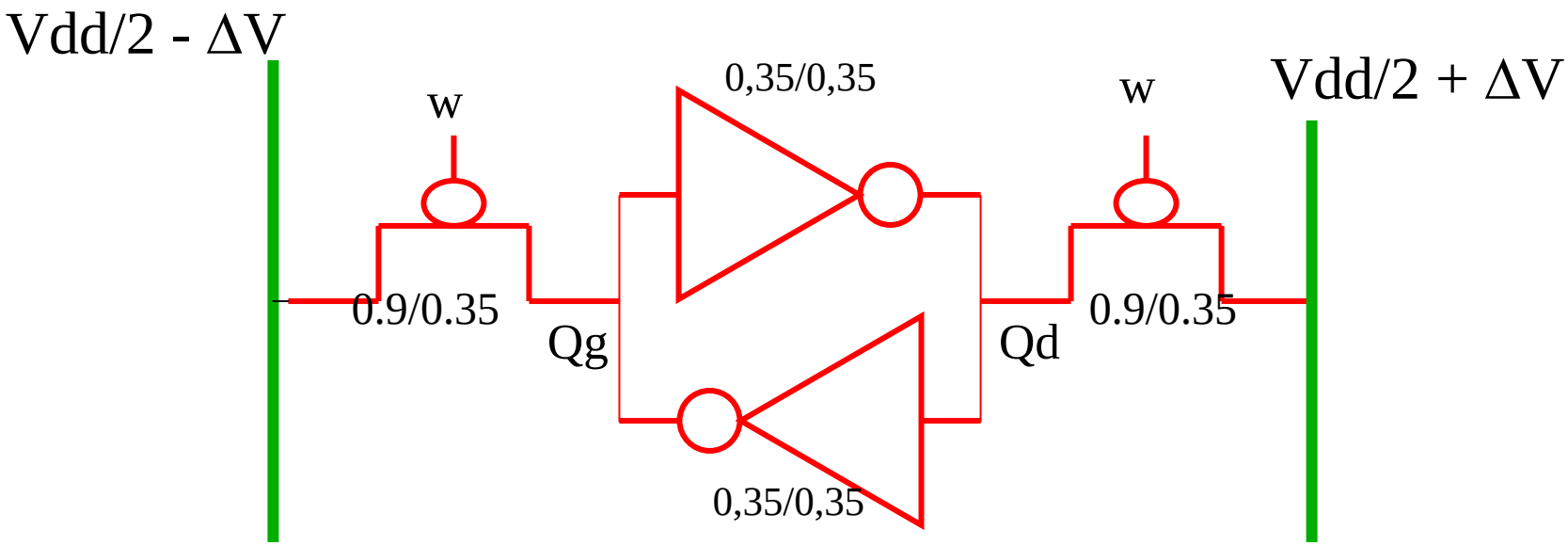
```
xmiwn ceb entre 0 0 mos_n w=1.4u l=0.35u
xmiwp ceb entre vdd vdd mos_p w=4.2u l=0.35u
xmiwnb ce ceb 0 0 mos_n w=1.4u l=0.35u
xmiwpb ce ceb vdd vdd mos_p w=4.2u l=0.35u
*selection de bit
xmbs cep w ce vdd1 mos_p w=4.2u l=0.35u
+as=1p ad=1p
xmbsb cebp w ceb vdd1 mos_p w=4.2u l=0.35u
+as=1p ad=1p
xm1 2 3 0 0 mos_n w=0.35u l=0.35u
+as=1p ad=1p
xm3 2 3 vdd1 vdd1 mos_p w=0.35u l=0.35u
+as=1p ad=1p
xm2 3 2 0 0 mos_n w=0.35u l=0.35u
+as=1p ad=1p
xm4 3 2 vdd1 vdd1 mos_p w=0.35u l=0.35u
+as=1p ad=1p
xmw cep w 2 vdd1 mos_p w=0.9u l=0.35u
+as=1p ad=1p
xmwb 3 w cebp vdd1 mos_p w=0.9u l=0.35u
+as=1p ad=1p
*precharge
rcep vdd cep 10k
rcebp vdd cebp 10k
*charge des colonnes
ccep cep 0 1500fF
ccebp cebp 0 1500fF
vpolar vdd 0 dc 3.3
vpolarcell vdd1 0 dc 3.3
v1 entre 0 pulse 3.3 0 5ns 200ps 200ps 5ns 10.4ns
vw w 0 pulse 3.3 0 1n 200p 200p 3n 5ns
.tran 5p 15ns sweep monte=40
```

Simulation monte-carlo: variation de Vth

```
.subckt mos_n d g s b
+ w= 0.35u l=0.35u
* param pour monte carlo
* variation vth
.param dvth='0.0096/(1e6*sqrt(w*l))'
.param vth=agauss (0.465,dvth,1)
m1 d g s b modn w='w' l='l'

.MODEL MODN NMOS LEVEL=49
……
```

```
.subckt mos_p d g s b
+ w= 0.35u l=0.35u
* param pour monte carlo
* variation vth
.param dvth='0.016/(1e6*sqrt(w*l))'
.param vth=agauss (-0.617,dvth,1)
m1 d g s b modp w='w' l='l'

.MODEL MODP PMOS LEVEL=49
……
```

Simulation monte carlo de la cellule SRAM
Dispersion intra-circuit



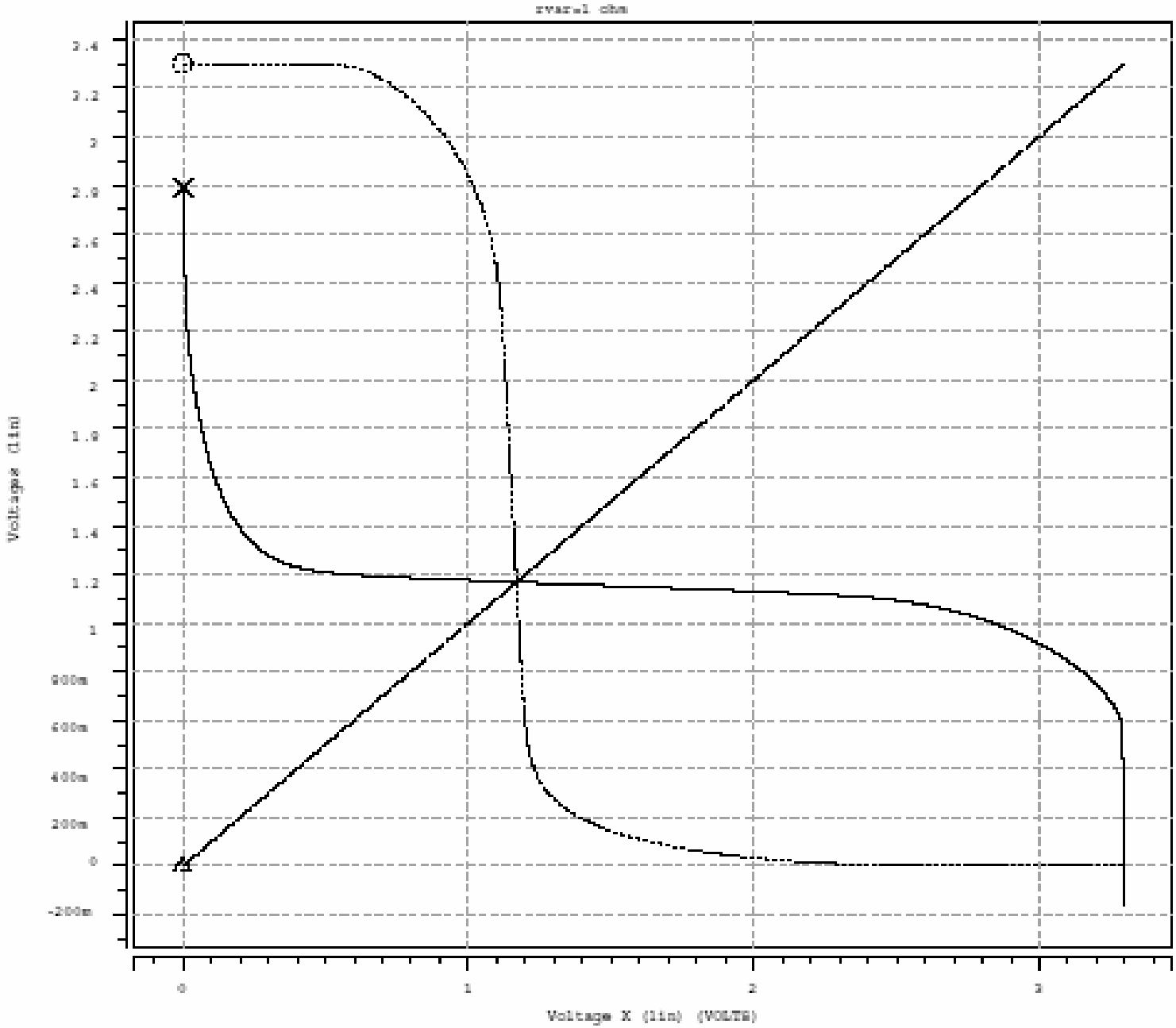
Variation de Vth pour les 4 transistors de la cellule SRAM avec:

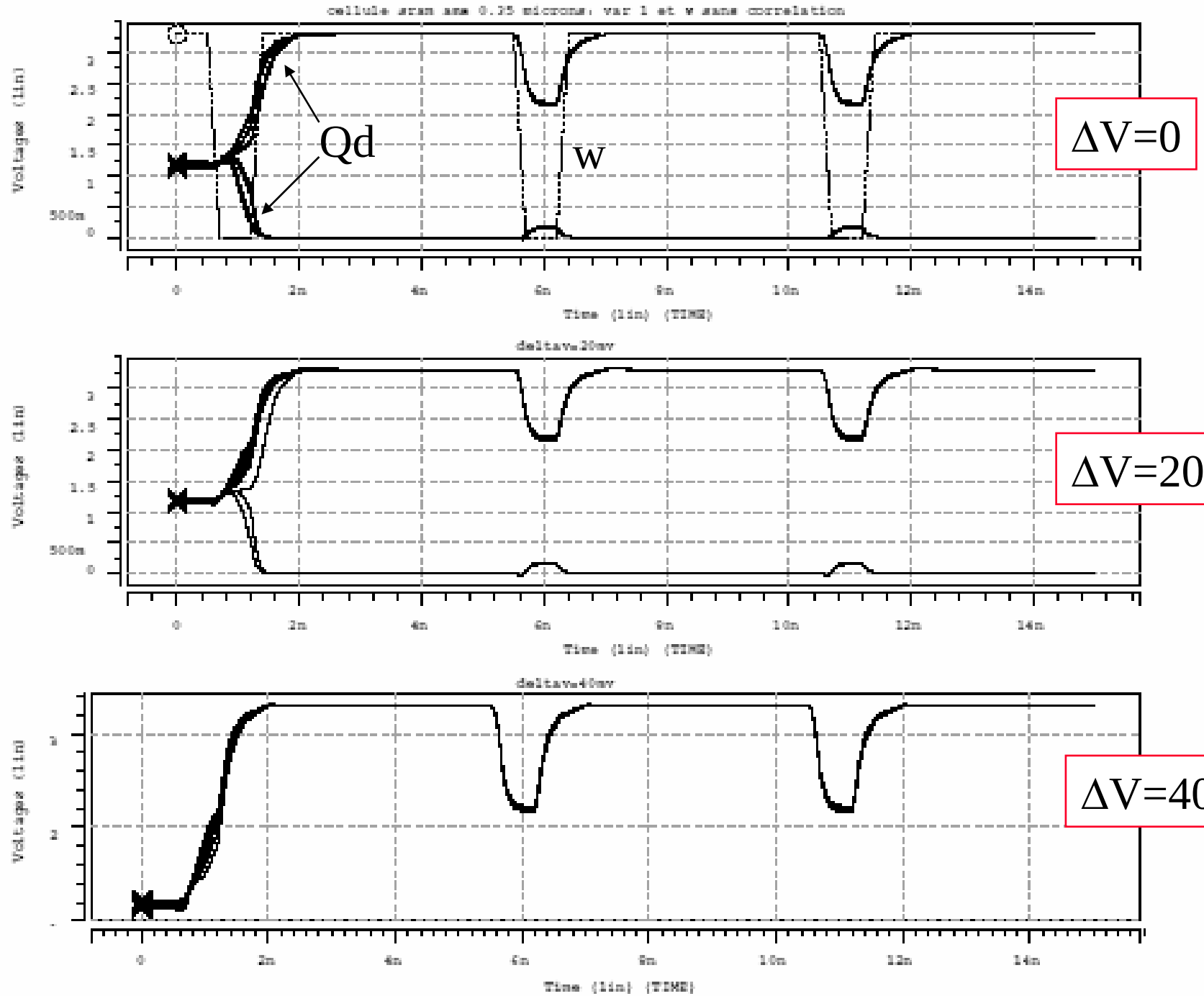
dvth_n = 9.6 mV . µ
dvth_p = 16 mV.µ

σ^2 (Vth) = $dvth^2$ / (W.L)

➔Hspice:

```
* variation vth
.param dvth='0.0096/(1e6*sqrt(w*l))'
.param vth=agauss (0.465,dvth,1)

* variation vth
.param dvth='0.016/(1e6*sqrt(w*l))'
.param vth=agauss (-0.617,dvth,1)
```

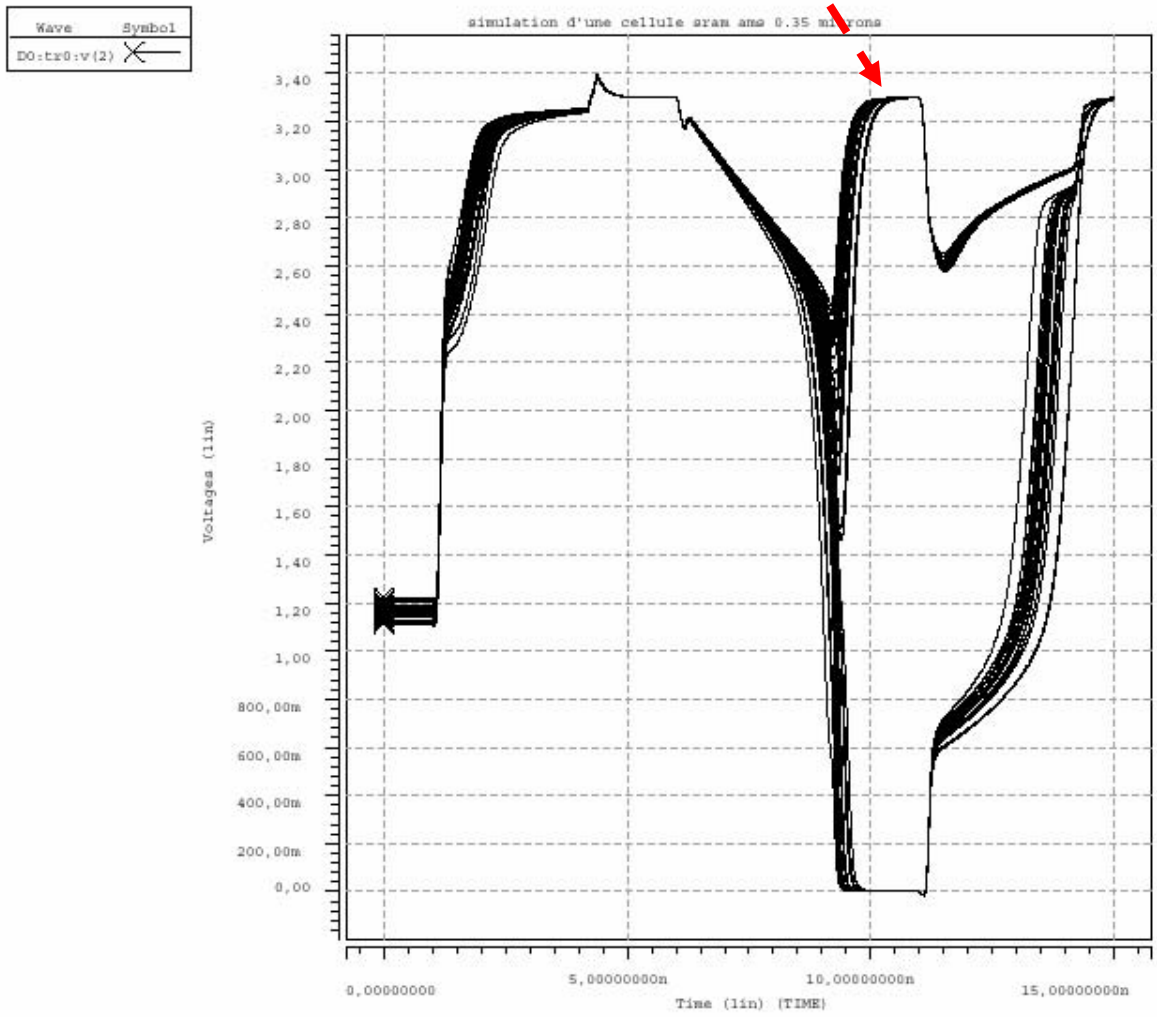

rvarsl ohm
Voltage (lin)
2.4
2.2
2
1.8
1.6
1.4
1.2
1
800m
600m
400m
200m
0
-200m
0
1
2
3
Voltage X (lin) (VOLTS)


cellule sram sans 0.35 microns: var l et w sans correlation
Voltage (lin)
Qd
w
Time (lin) (TIME)
ΔV=0
deltavw20mv
Voltage (lin)
Time (lin) (TIME)
ΔV=20mV
deltavw40mv
Voltage (lin)
Time (lin) (TIME)
ΔV=40mV

Adobe Acrobat - [SRAM_mc.pdf]

File Edit Document Tools View

Variation de Vth ➔ erreurs d'écriture



100% 1 of 1 11 x 8,5 in

démarrer Eud... Ges... Mes... Imgr... ava... hspui RA... awa... Micr... Ado... FR 15:12

"tirage Vth"	xm1.m1	xm2.m1	xm3.m1	xm4.m1
1.00000	506.1860m	569.6769m	660.4251m	759.2076m
2.00000	547.7160m	530.0537m	688.8446m	819.8547m
3.00000	486.0505m	540.9631m	760.3990m	687.6930m
4.00000	532.2356m	530.3305m	661.8463m	750.8987m
5.00000	533.9101m	519.3695m	739.6328m	692.7718m
6.00000	475.4419m	569.9119m	769.7759m	793.6493m
7.00000	527.7004m	517.2839m	720.9544m	661.5358m
8.00000	529.0042m	556.2920m	785.2109m	696.6253m
9.00000	547.6925m	555.7047m	701.3580m	712.0388m
10.00000	516.7749m	540.8499m	589.4095m	724.5000m
11.00000	551.1574m	519.3478m	750.7220m	666.4364m
12.00000	590.1073m	535.4432m	664.1268m	655.4386m
13.00000	546.8246m	595.0915m	748.2672m	672.8256m
14.00000	526.3400m	573.6029m	632.6057m	768.6731m
15.00000	479.8723m	585.7528m	651.3573m	689.2450m
16.00000	505.3356m	491.4370m	658.5848m	633.1565m
17.00000	544.5494m	556.1118m	682.4670m	688.5867m
18.00000	540.6009m	540.6431m	719.8721m	669.1501m
19.00000	564.1464m	530.2135m	636.2724m	768.6739m
20.00000	510.2905m	510.4259m	734.0742m	684.4521m
21.00000	550.6866m	550.0961m	737.7279m	679.8985m
22.00000	555.1859m	529.0596m	670.2136m	794.9981m
23.00000	595.5088m	524.4076m	646.6189m	722.7618m
24.00000	561.1176m	514.8222m	716.0907m	663.3536m
25.00000	555.6943m	557.1089m	653.0521m	731.8418m
26.00000	551.6132m	554.8919m	701.0050m	705.8358m
27.00000	480.7487m	544.4024m	710.7359m	694.7525m
28.00000	496.2214m	540.0151m	741.6872m	614.8267m
29.00000	522.2887m	532.5908m	745.3846m	761.8139m
30.00000	531.7932m	531.2412m	774.4159m	741.4534m

Variation de Vth pour les 4 transistors de la cellule SRAM avec:

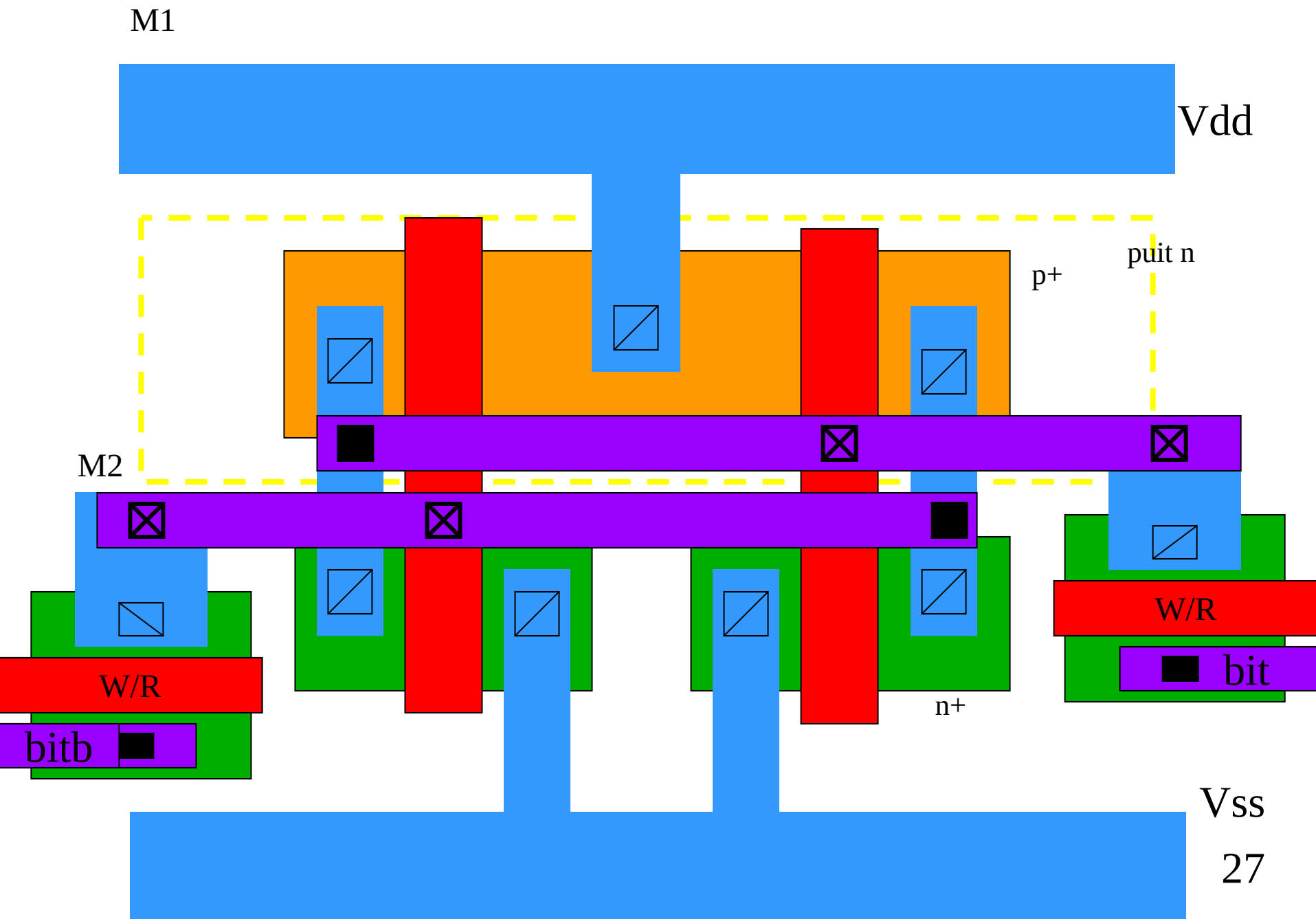
dvth_n = 9.6 mV . µ
dvth_p = 16 mV.µ

σ^2 (Vth) = $dvth^2$ / (W.L)

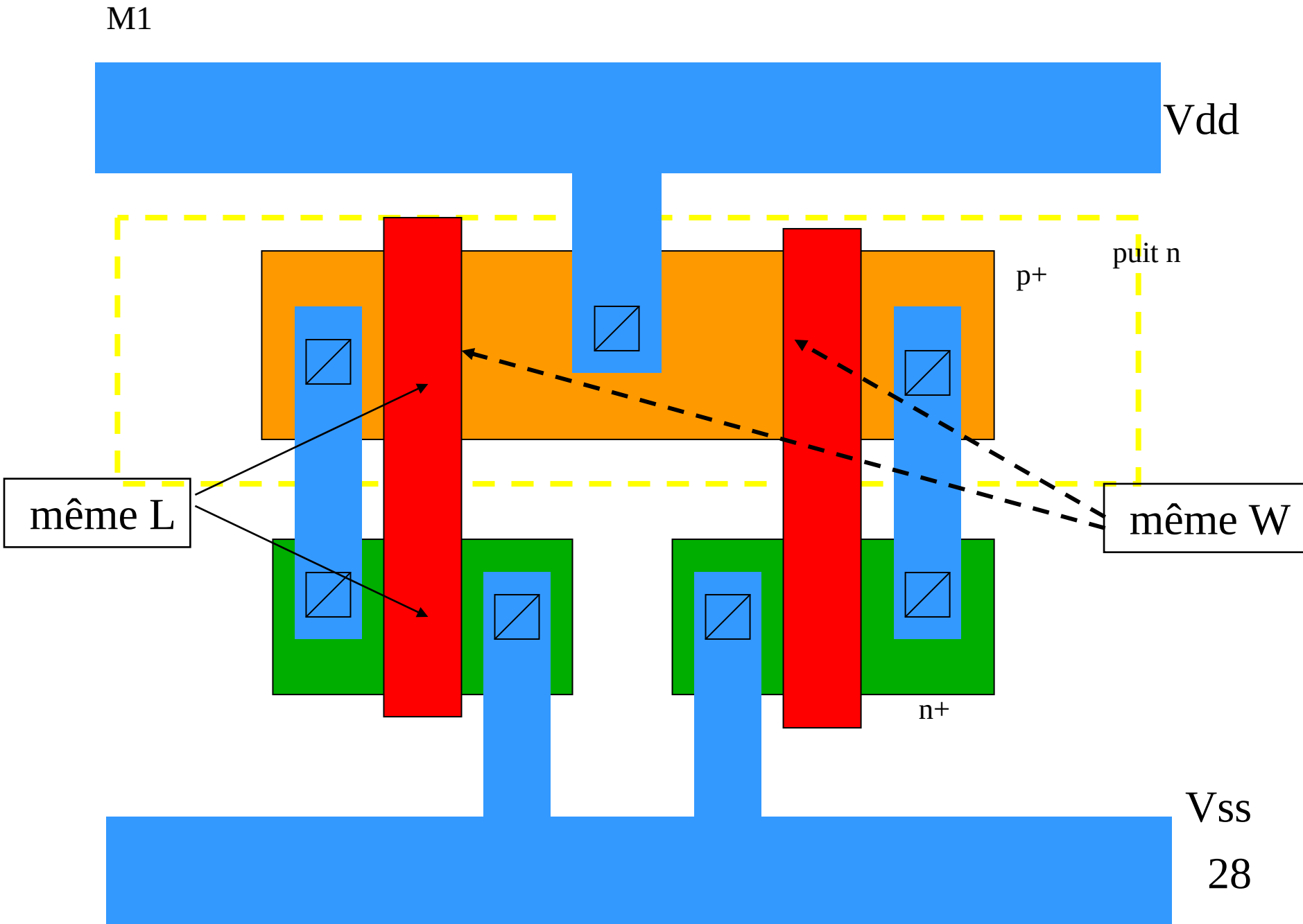
➔Hspice:

```
* variation vth
.param dvth='0.0096/(1e6*sqrt(w*l))'
.param vth=agauss (0.465,dvth,1)

* variation vth
.param dvth='0.016/(1e6*sqrt(w*l))'
.param vth=agauss (-0.617,dvth,1)
```

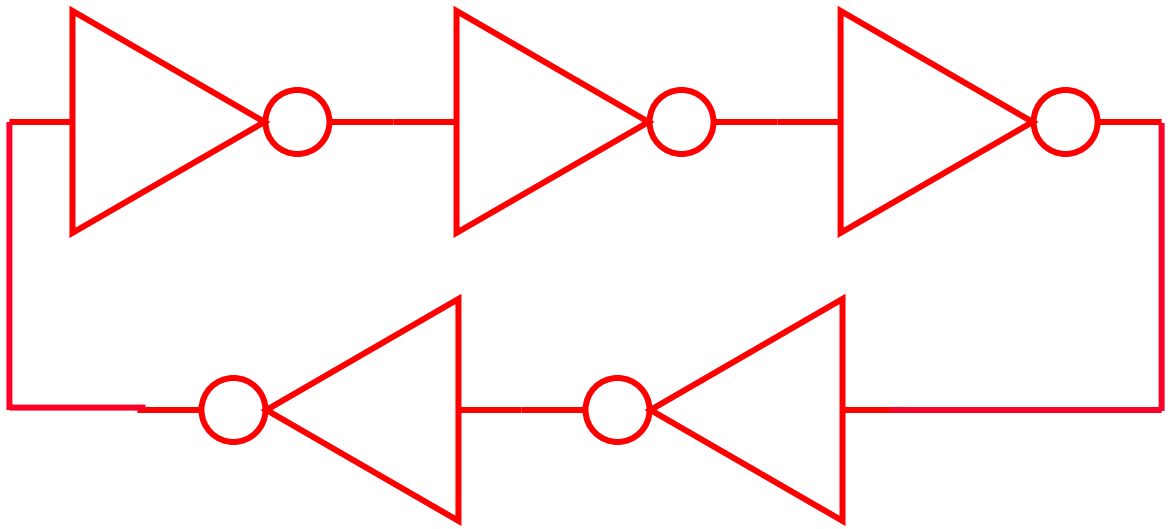
Cellule SRAM



Cellule SRAM (corrélations)

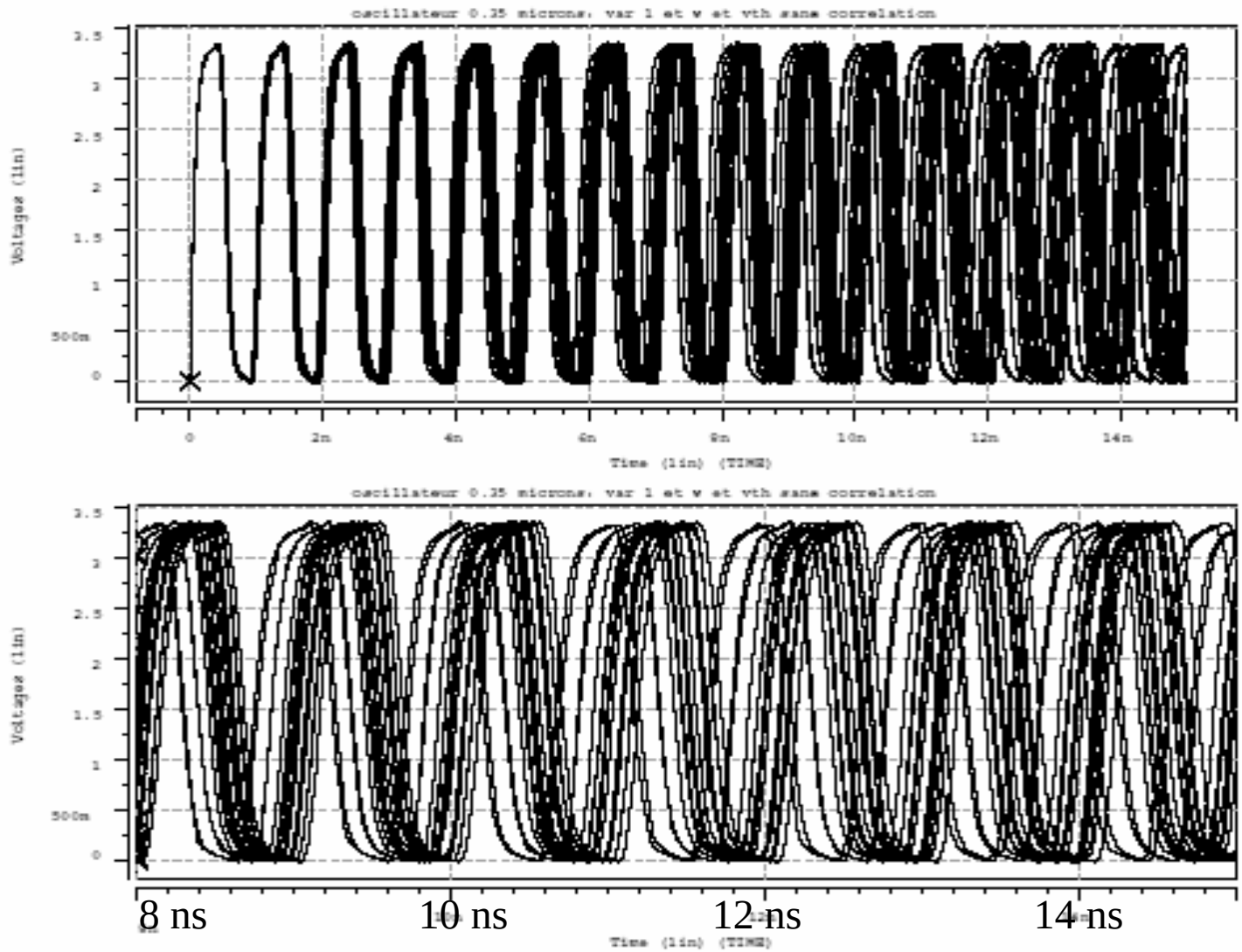


Simulation monte carlo de l'oscillateur en anneau 5 étages (0,35µ)
Variation de L, W, Vth (intra-circuit ou "mismatch")



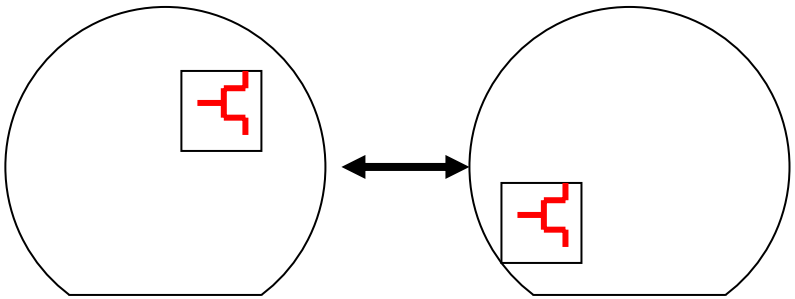
Wn=0.35µ
Wp=3*Wn

Simulation monte carlo de l'oscillateur en anneau 5 étages (0,35µ) (intra-circuit ou "mismatch")



CMOS: dispersion inter-circuit des paramètres des transistors (bon / pas bon)

Différents circuits, tranches ou lots de fabrication



Simulations pire cas (Worst case)

Attention: corrélation entre paramètres!

n_MOS (0.35µ)

	min.	typ	max	
tox	7	7.5	8	nm
Vth	0.35	0.45	0.55	V
Lmin	0.30	0.38	0.45	µm
Wmin	0.20	0.35	0.50	µm
Kp	150	170	190	$\mu A/V^2$

……

p_MOS (0.35µ)

	min.	typ	max	
tox	7	7.5	8	nm
Vth	-0.5	-0.7	-0.8	V
Lmin	0.40	0.5	0.6	µm
Wmin	0.20	0.35	0.50	µm
Kp	50	60	70	$\mu A/V^2$

……..

CMOS: dispersion inter-circuit des paramètres des transistors
Simulations "corner": cas extrêmes

Modèles différents pour:

- SS : slow-slow
- TT : typical-typical
- FF : fast-fast
- ……

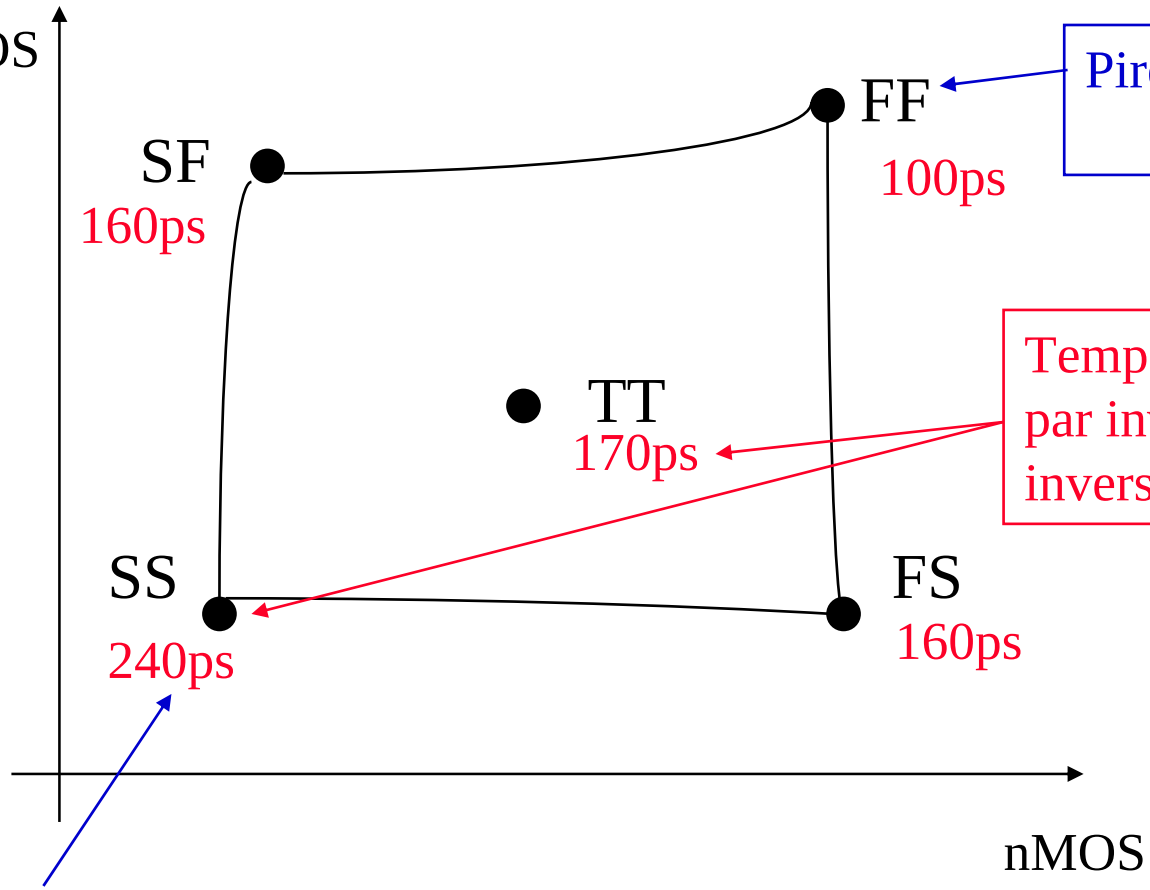
et/ou, utilisation de sigma:

.param vth='vth0 + sigma * dvth'

……..

.tran …….sweep sigma –3 3 1

Inverseur CMOS 0.35µ (Wn=0.35µ, Wp=3*Wn)
(simulation: oscillateur en anneau 5)

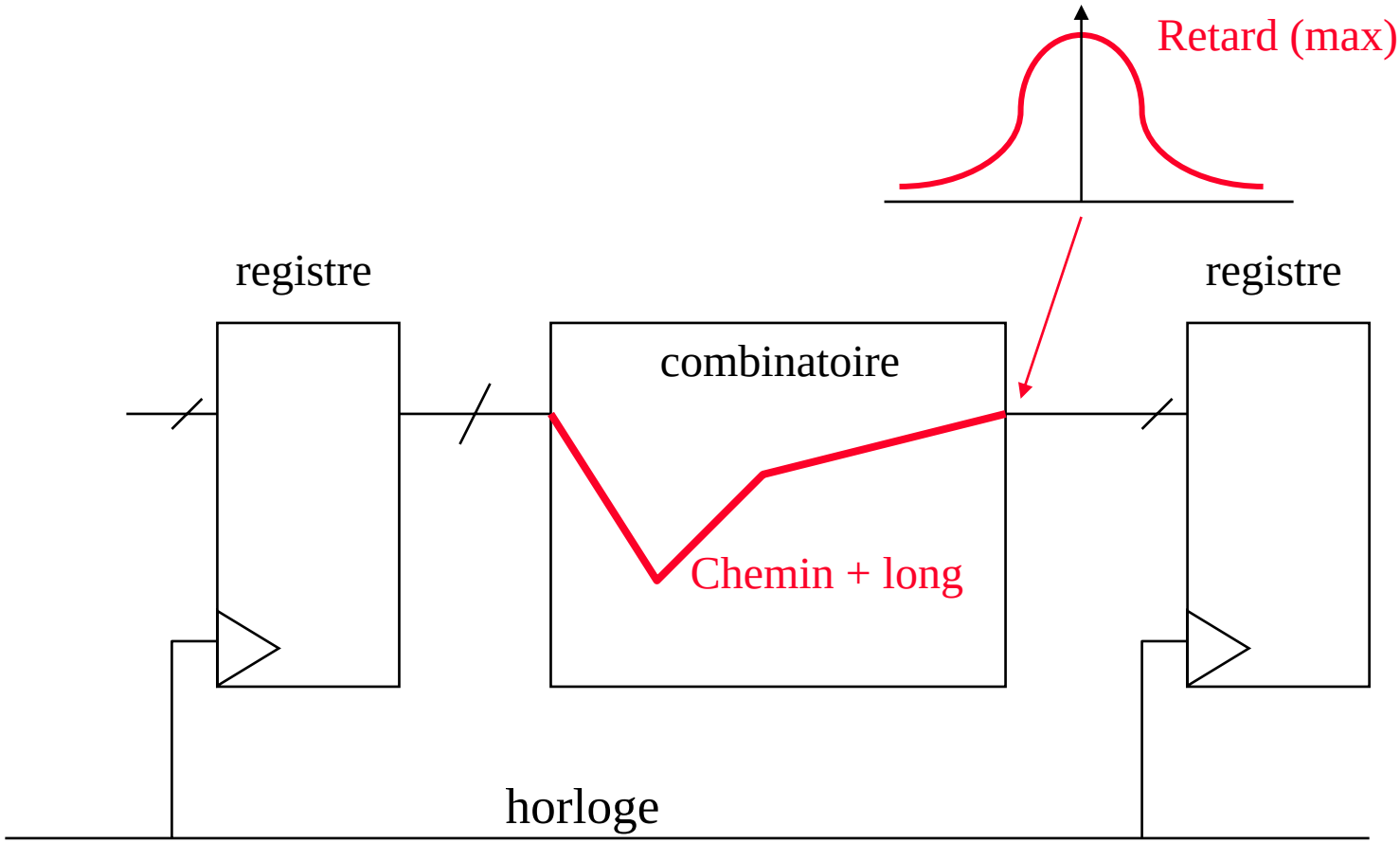


Pire cas en puissance!
Vth min

Temps de propagation par inverseur (chargé par inverseur identique)

Meilleur cas en puissance!
Vth max

Prise en compte de la dispersion inter(intra)-circuits



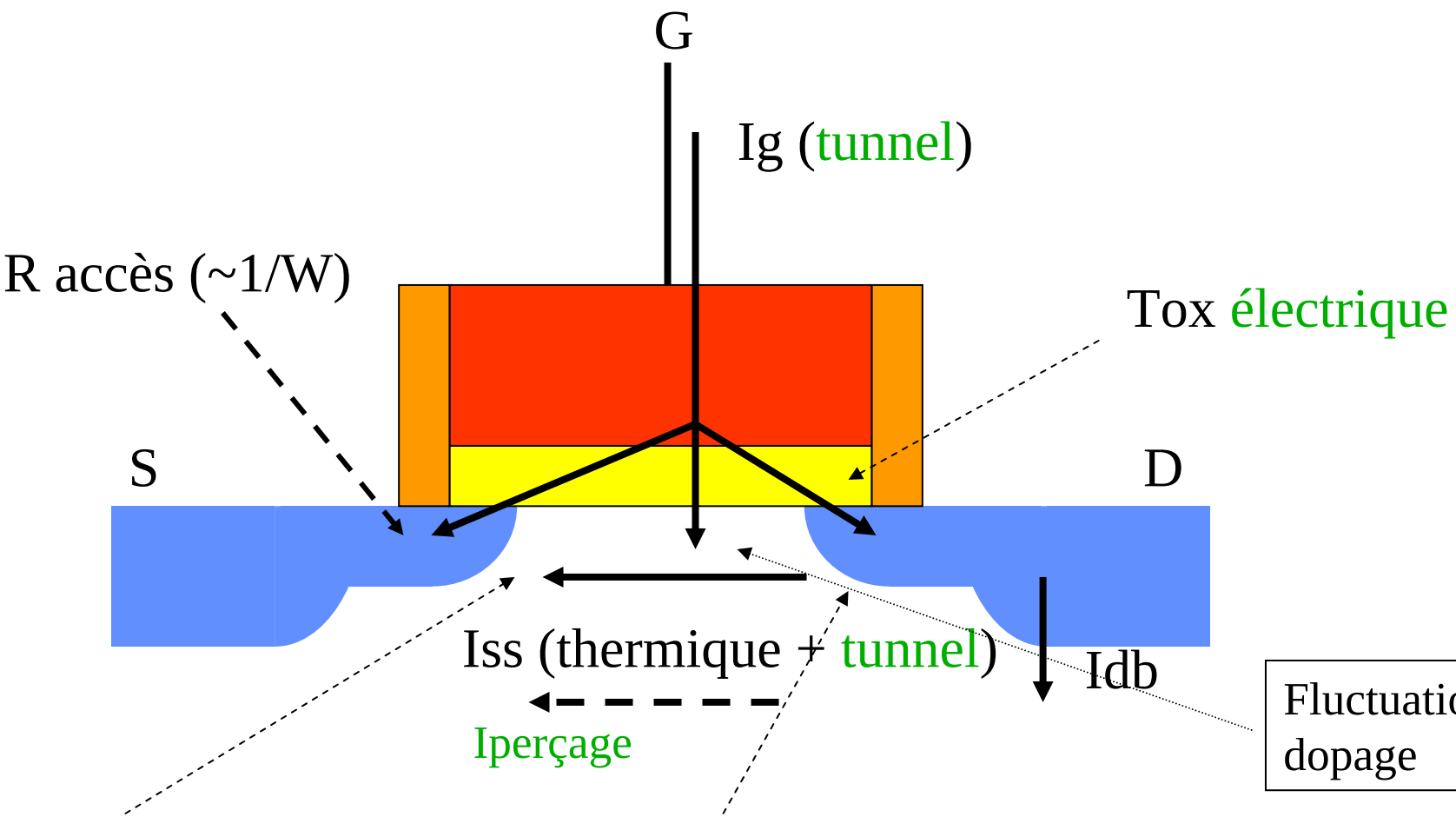
➔ Prise en compte pour f_{hmax}

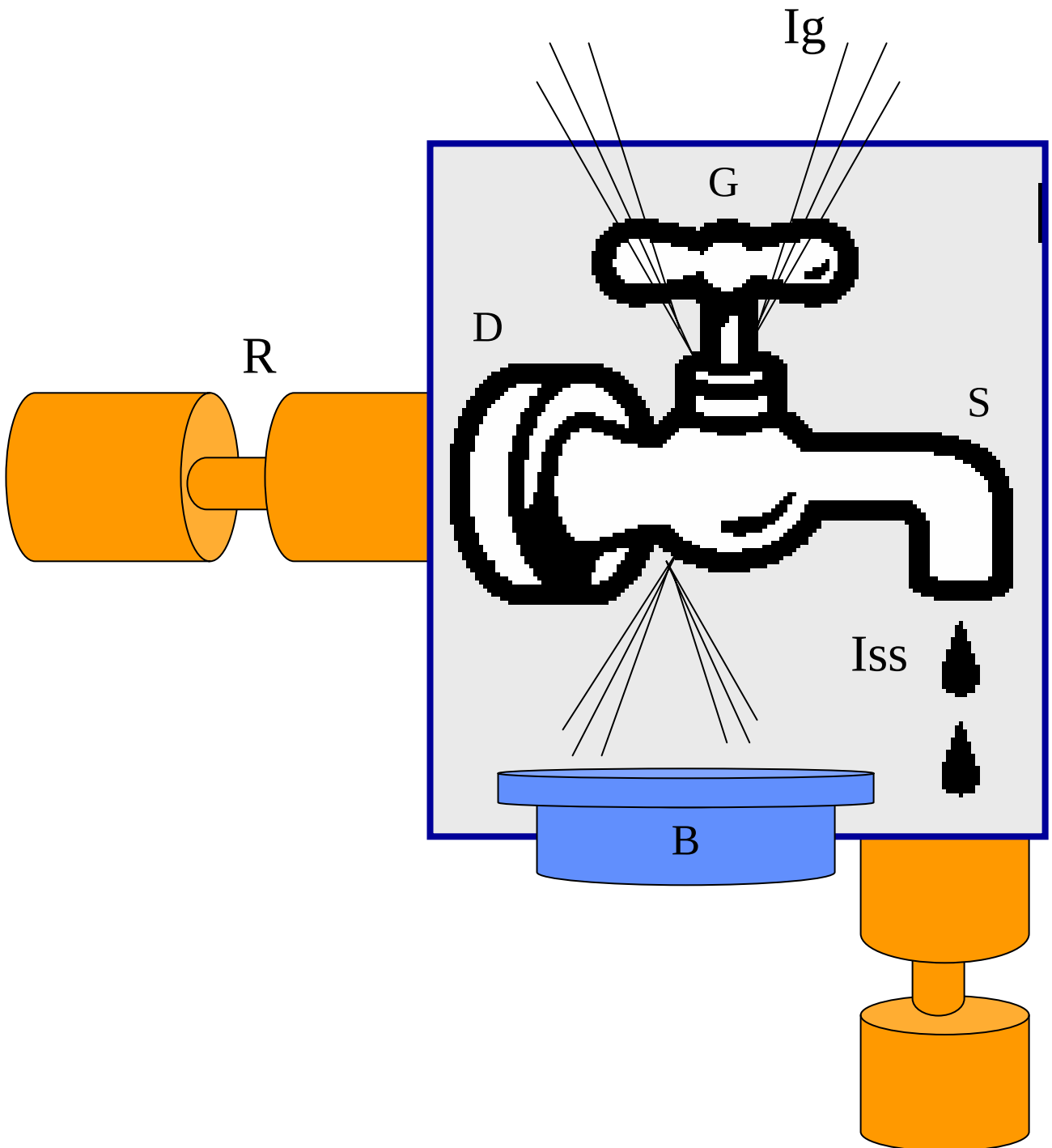
MODELISATION et SIMULATION
des
TRANSISTORS MOS NANO-METRIQUES
(Lgrille < 100 nm)

Modèles des transistors MOS nano-métriques

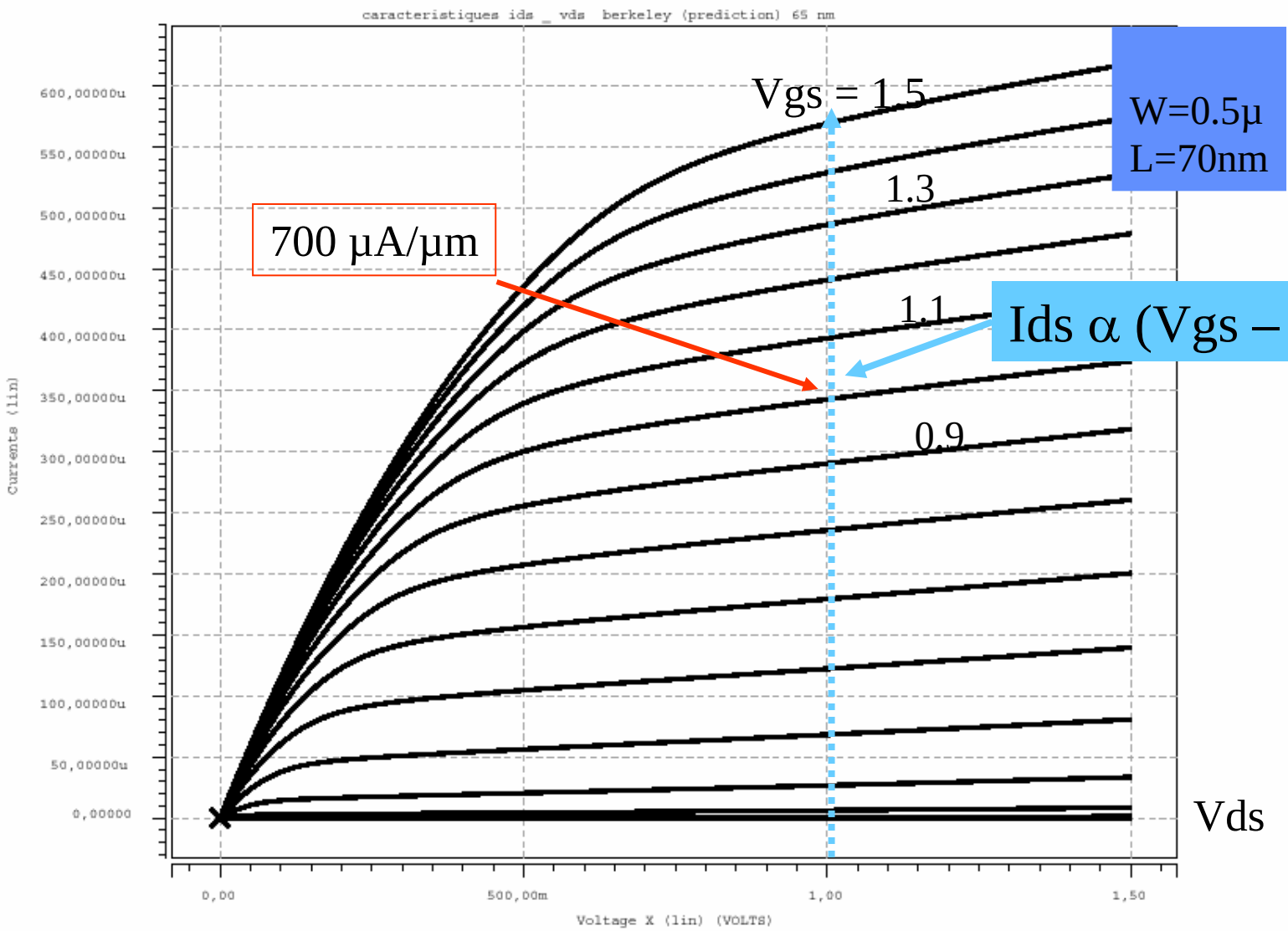
BSIM4 (Berkeley), EKV(EPF Lausanne), MM11 (Philips)

Prise en compte d'effets physiques nouveaux

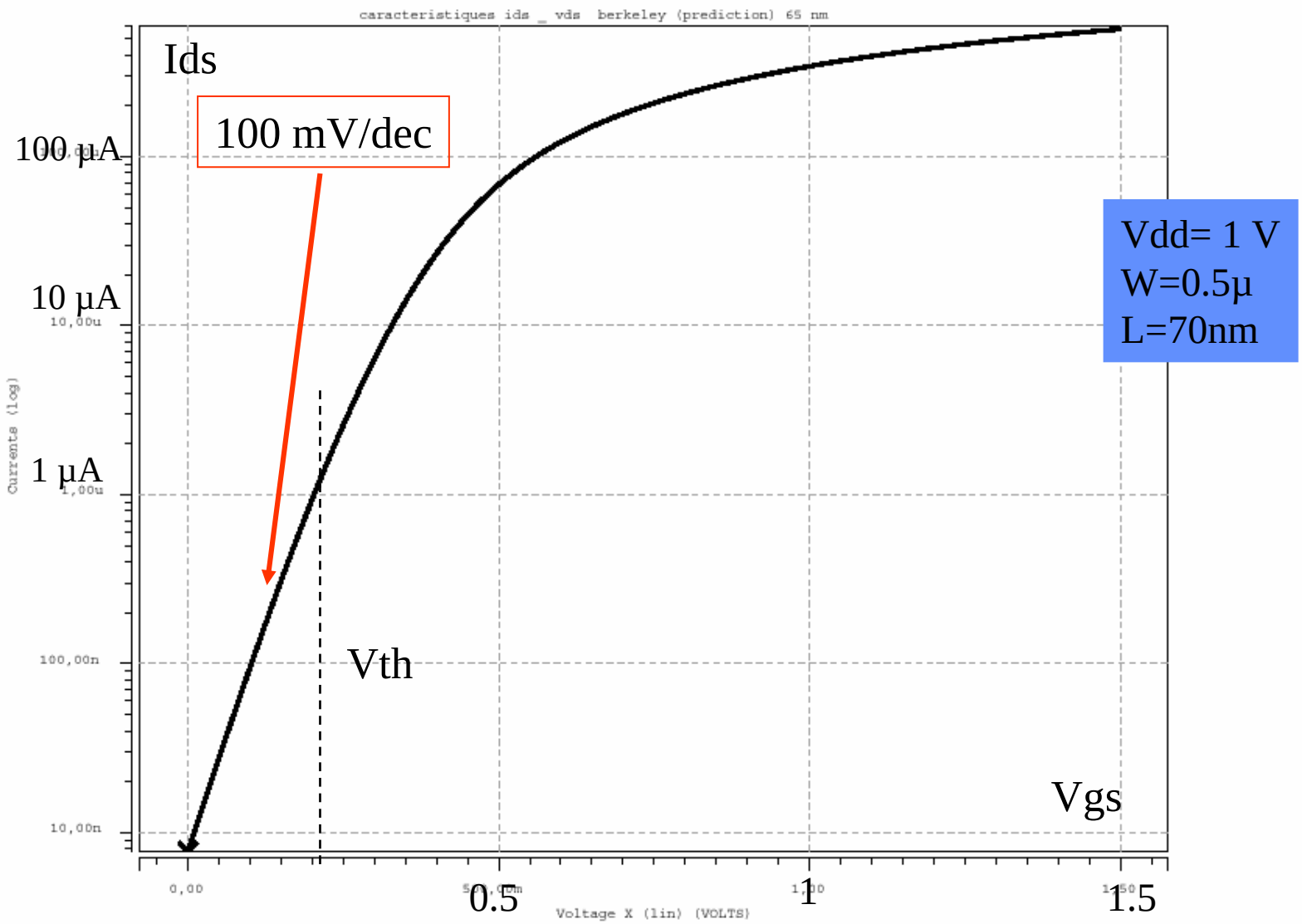



Ig
G
D
R
S
Iss
B

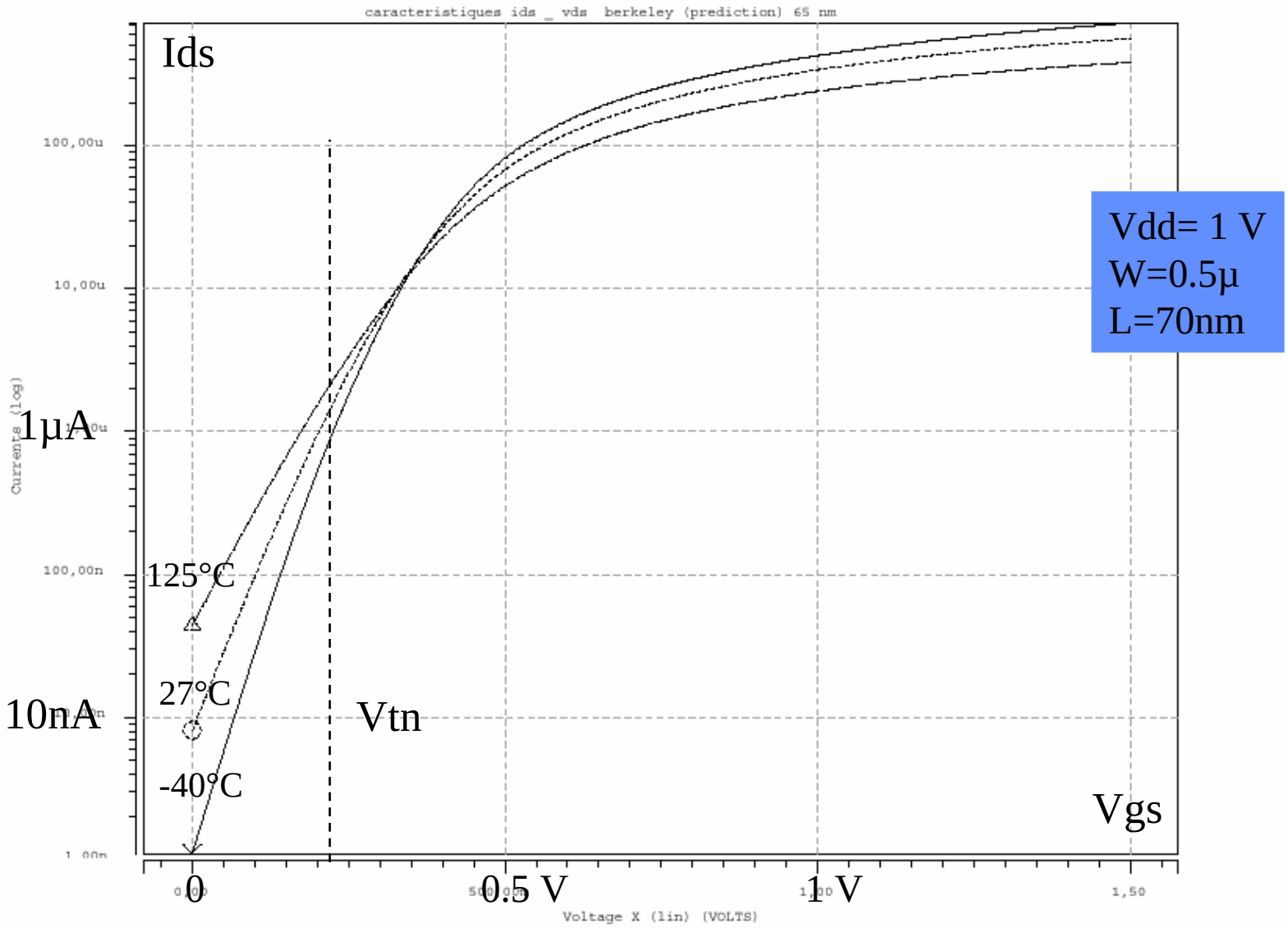
BSIM4 technologie prédictive 65 nm (Berkeley)



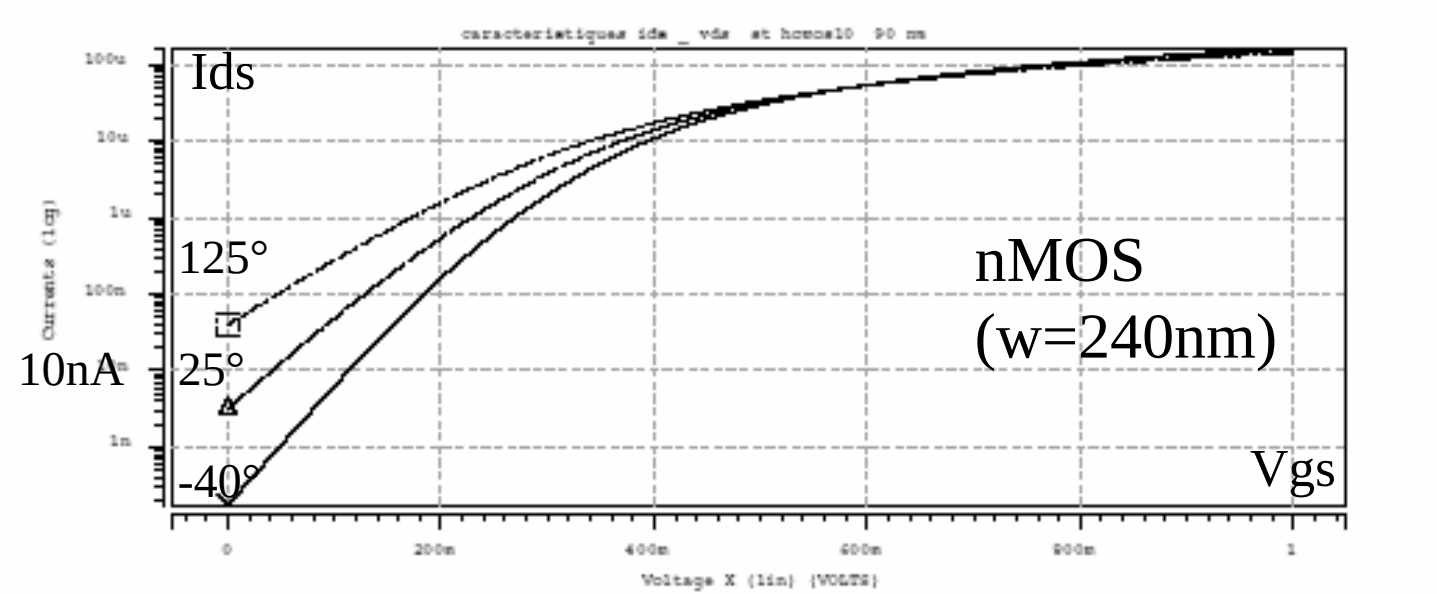
nMOS: BSIM4 technologie prédictive 65 nm (Berkeley)

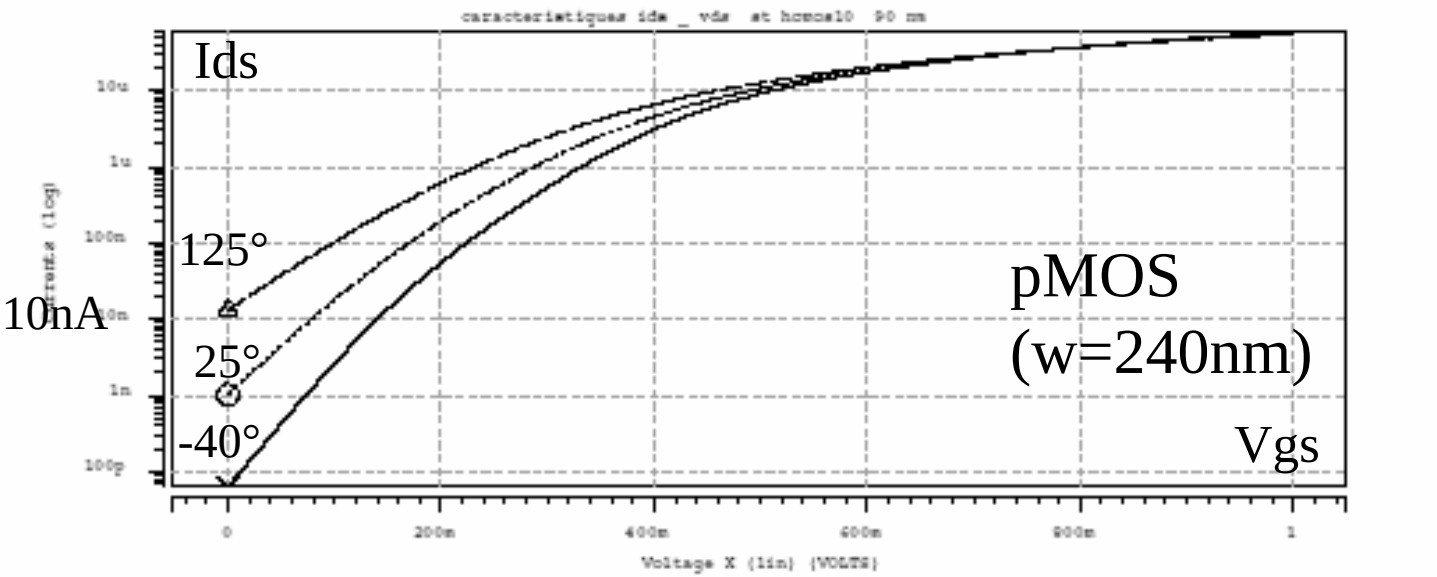


nMOS: BSIM4 technologie prédictive 65 nm (Berkeley)

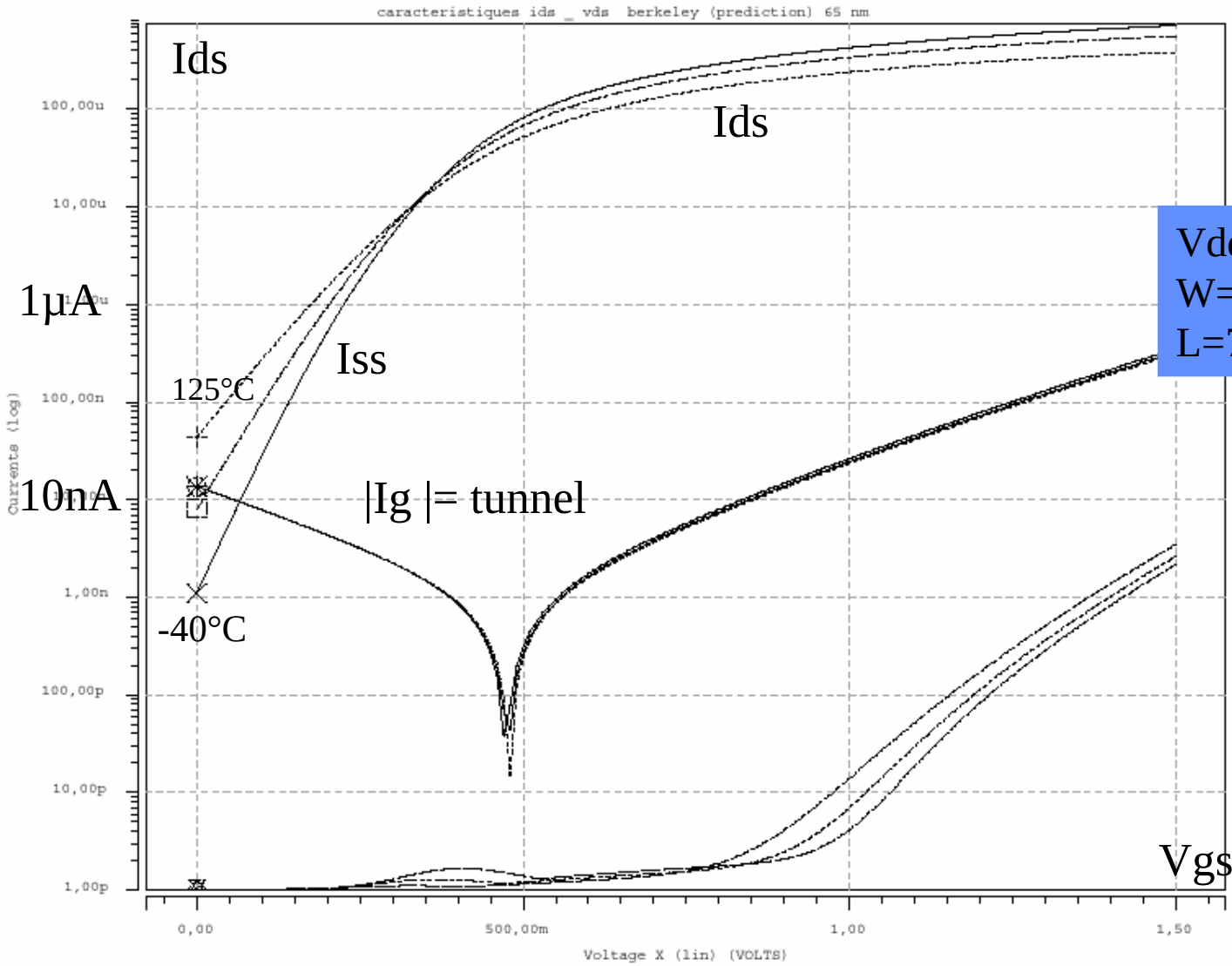


CMOS 90nm: Ids-Vgs (Vdd=1 V) (Modèle BSIM3+)

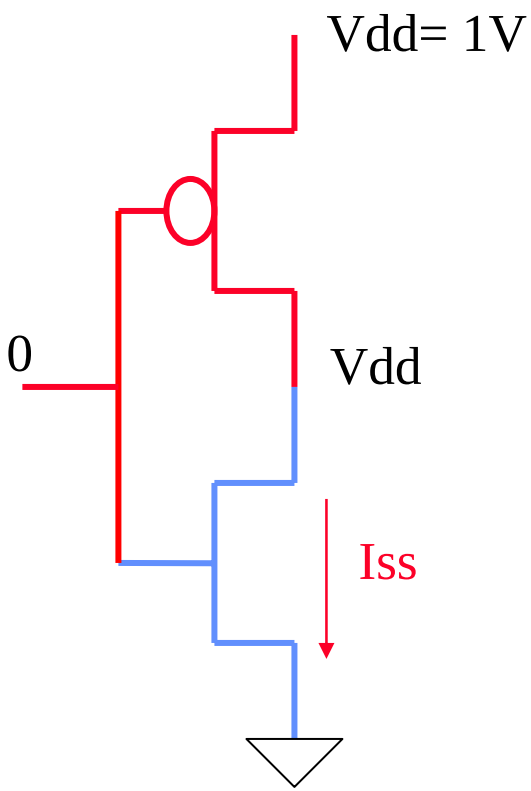




BSIM4 technologie prédictive 65 nm (Berkeley)



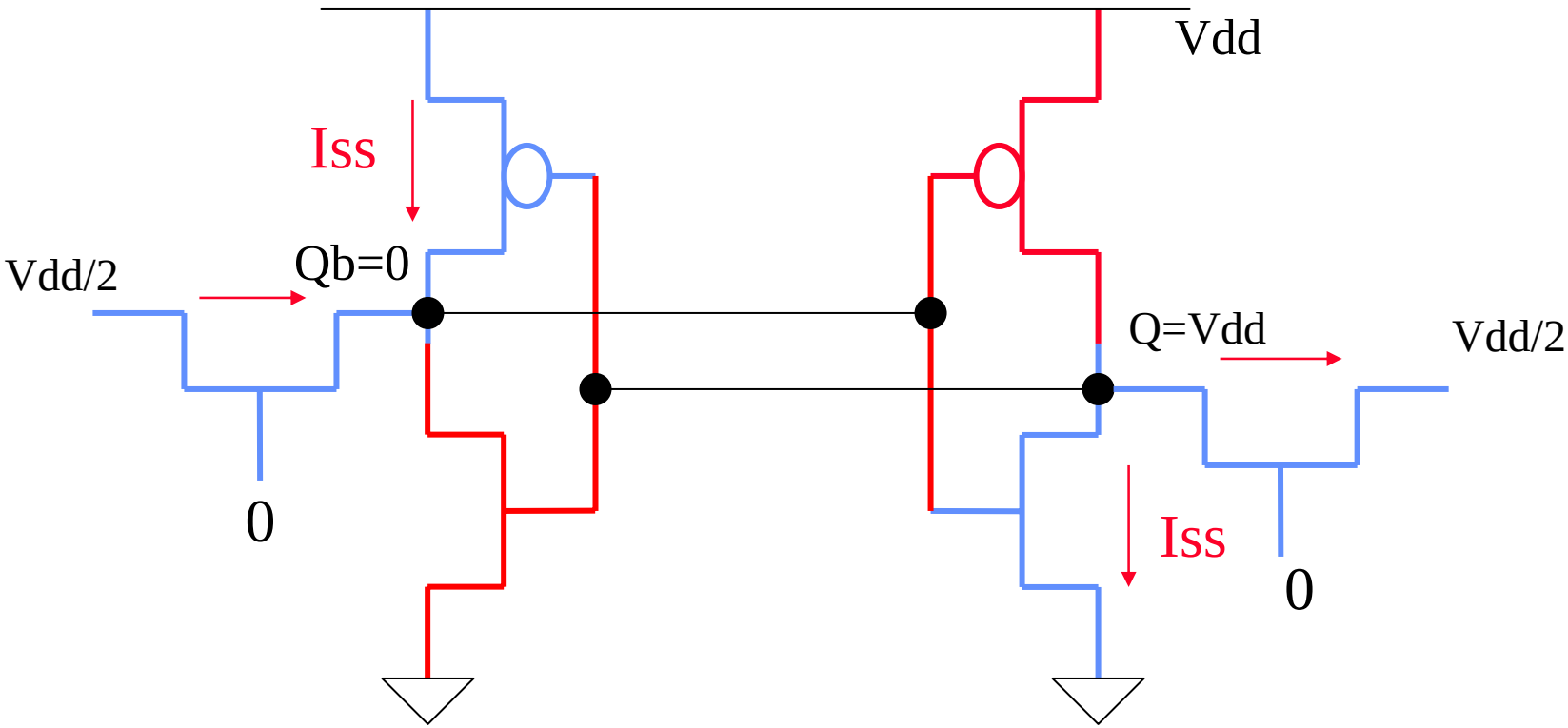
Courant sous le seuil = consommation statique!



En attente pendant 1s:
Iss= 30nA (125°C) ➔ P= 30 nW
Efuite = 30 nJoules

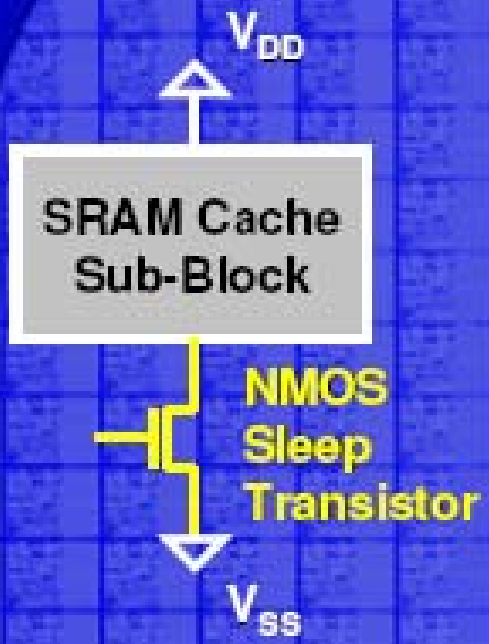
En fonction pendant 100 µs :
Si Imoyen = 30 µA ➔ P= 30 µW
E = 3 nJ

Courant sous le seuil = consommation statique
Ex: SRAM

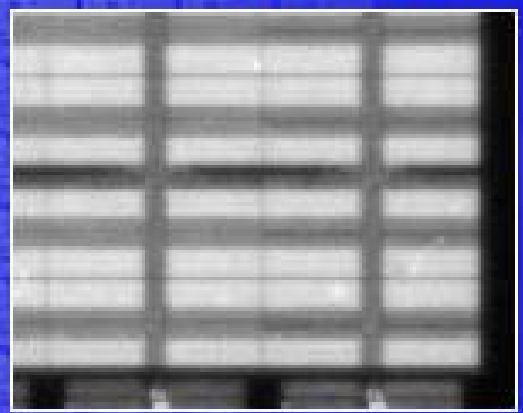


Température!!!

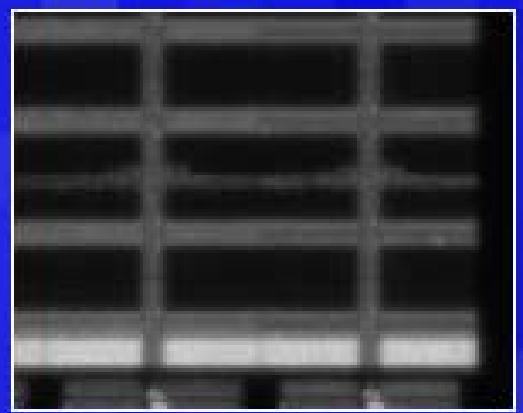
Sleep Transistors Reduce Leakage Power



70 Mbit SRAM IR photos



Normal SRAM sub-block leakage

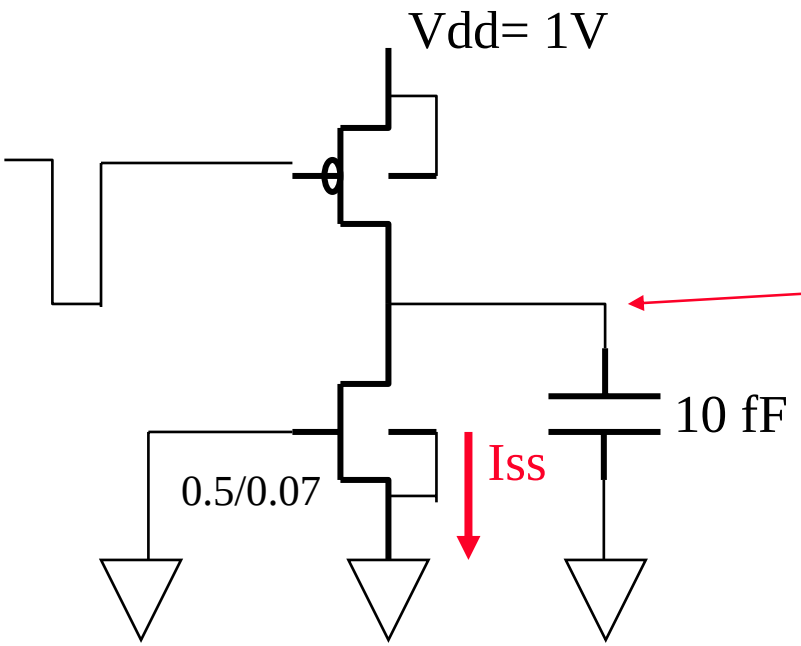


Sleep transistors shut off leakage in inactive sub-blocks

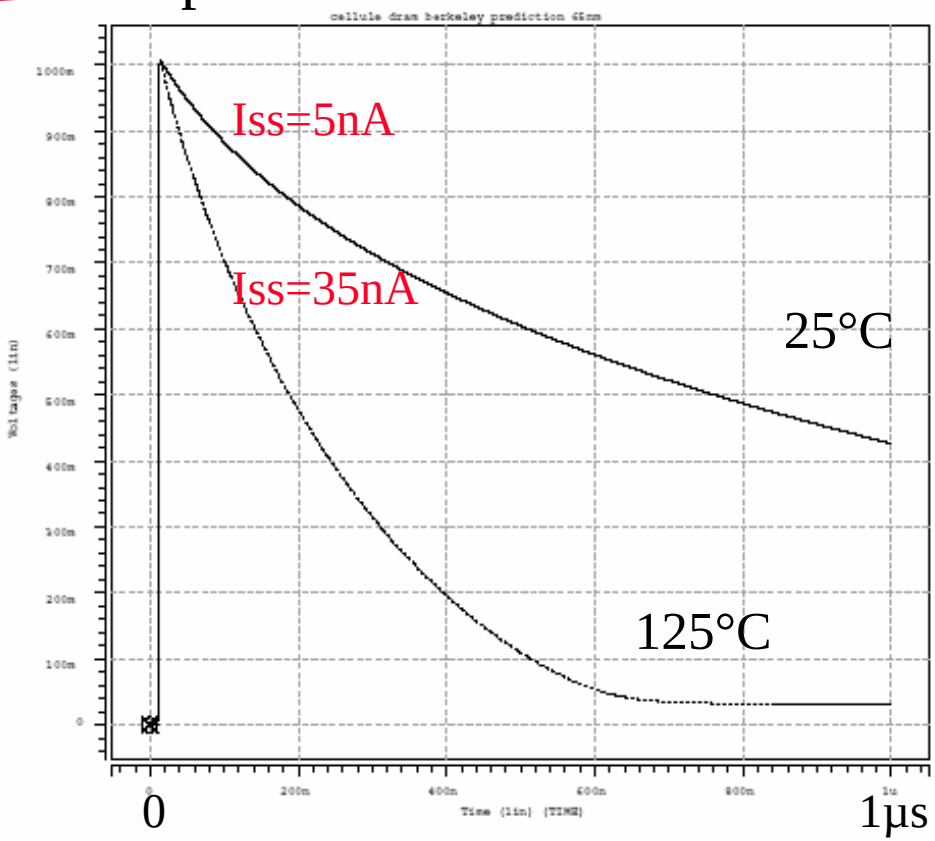
>3x SRAM leakage reduction with use of sleep transistors

Power Saving Feature

Courant de fuite en logique dynamique (CMOS 65nm)
Exemple: "DRAM"

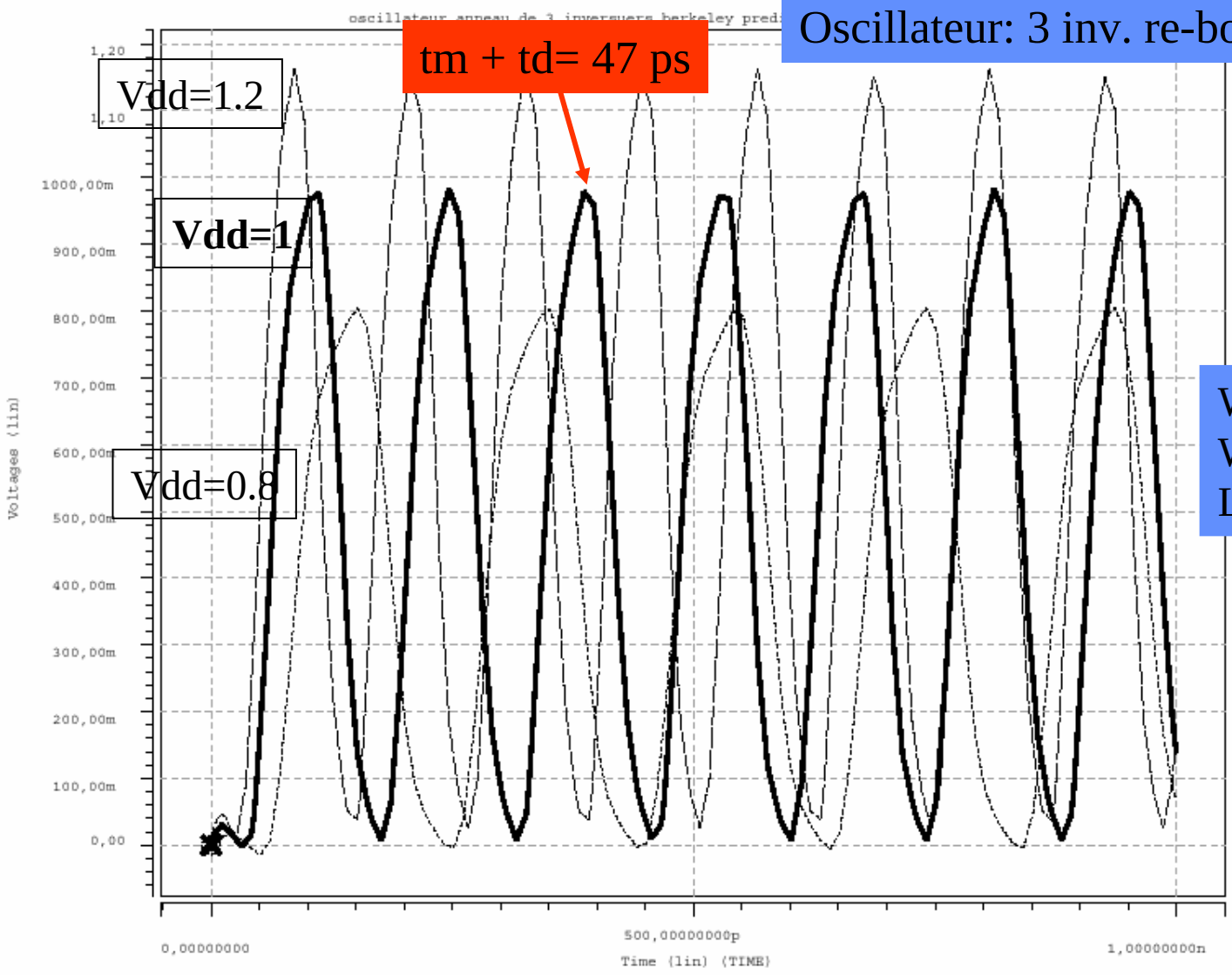


Vcap

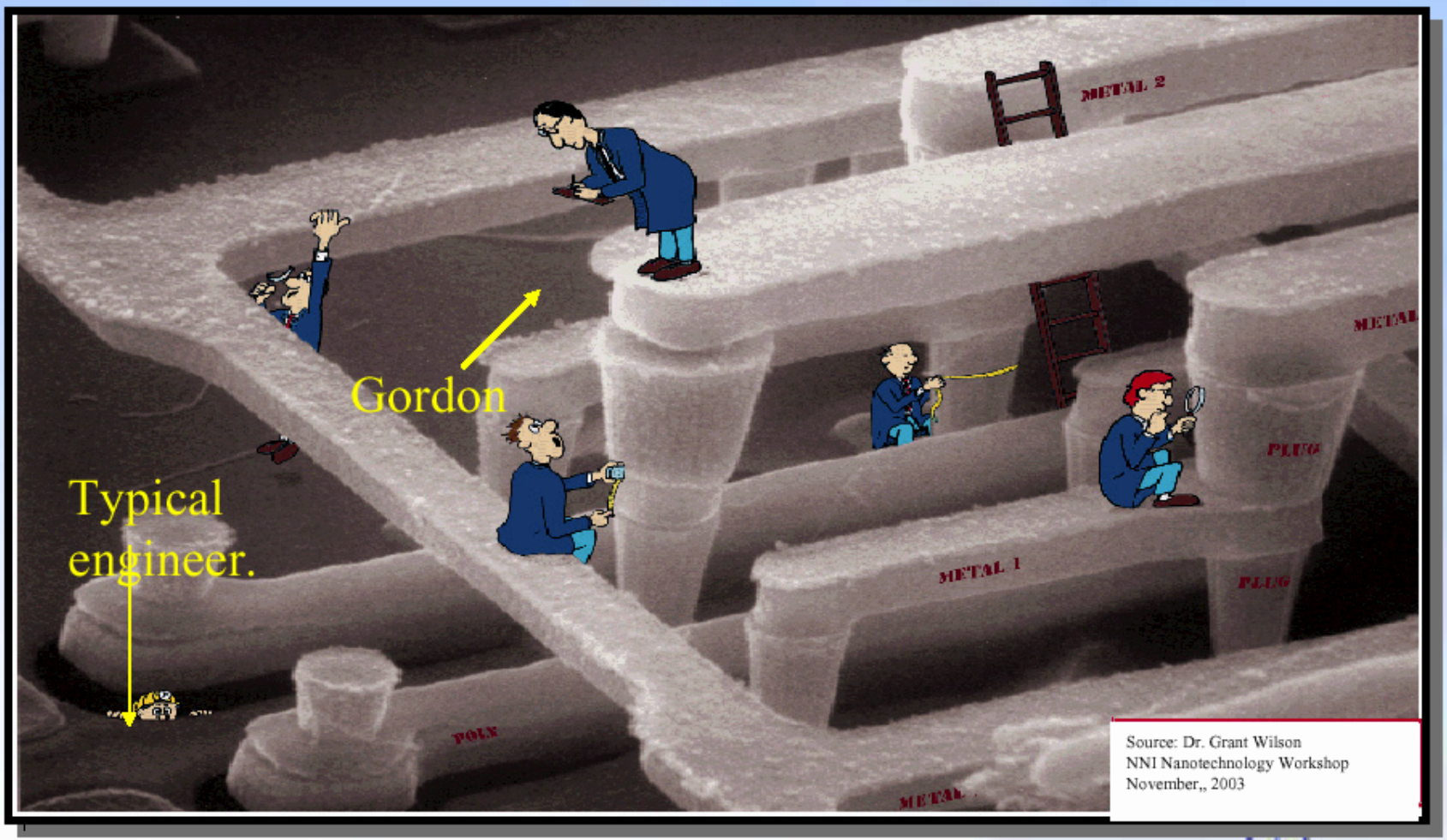


```
*oscillateur en anneau: 3 inverseurs reboucles
m1 3 1 0 0 nmos w=0.14u l=0.07u
+as=0.02p ad=0.02p ps=0.6u pd=0.6u
mp1 5 1 3 5 pmos w=0.28U l=0.07u
+as=0.04p ad=0.04p ps=0.9u pd=0.9u

m11 33 3 0 0 nmos w=0.14u l=0.07u
+as=0.02p ad=0.02p ps=0.6u pd=0.6u
mp11 5 3 33 5 pmos w=0.28U l=0.07u
+as=0.04p ad=0.04p ps=0.9u pd=0.9u

m111 1 33 0 0 nmos w=0.14u l=0.07u
+as=0.02p ad=0.02p ps=0.6u pd=0.6u
mp111 5 33 1 5 pmos w=0.28U l=0.07u
+as=0.04p ad=0.04p ps=0.9u pd=0.9u
```

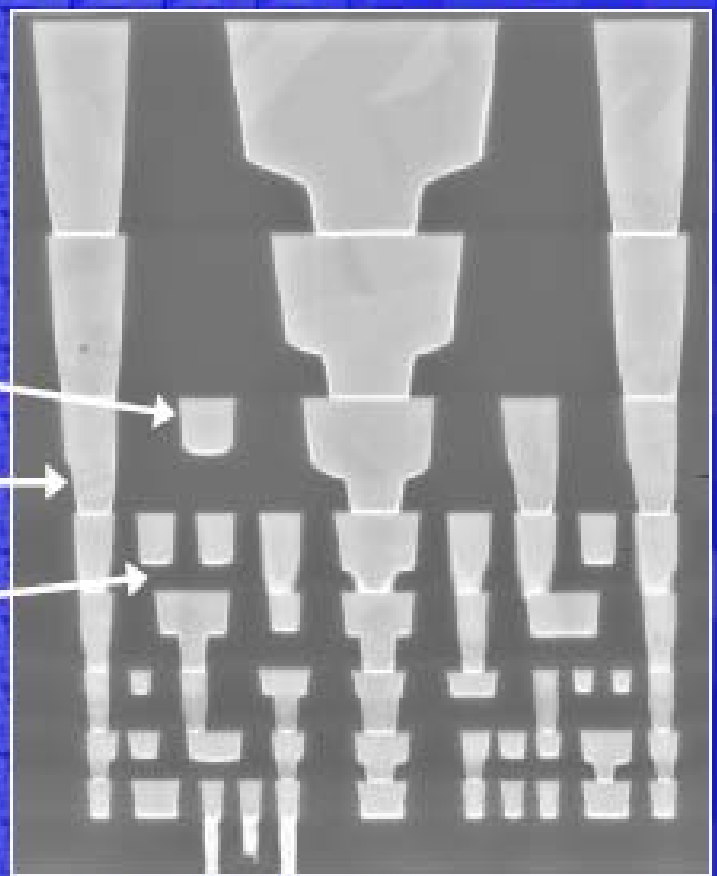
BSIM4 technologie prédictive 65 nm (Berkeley)



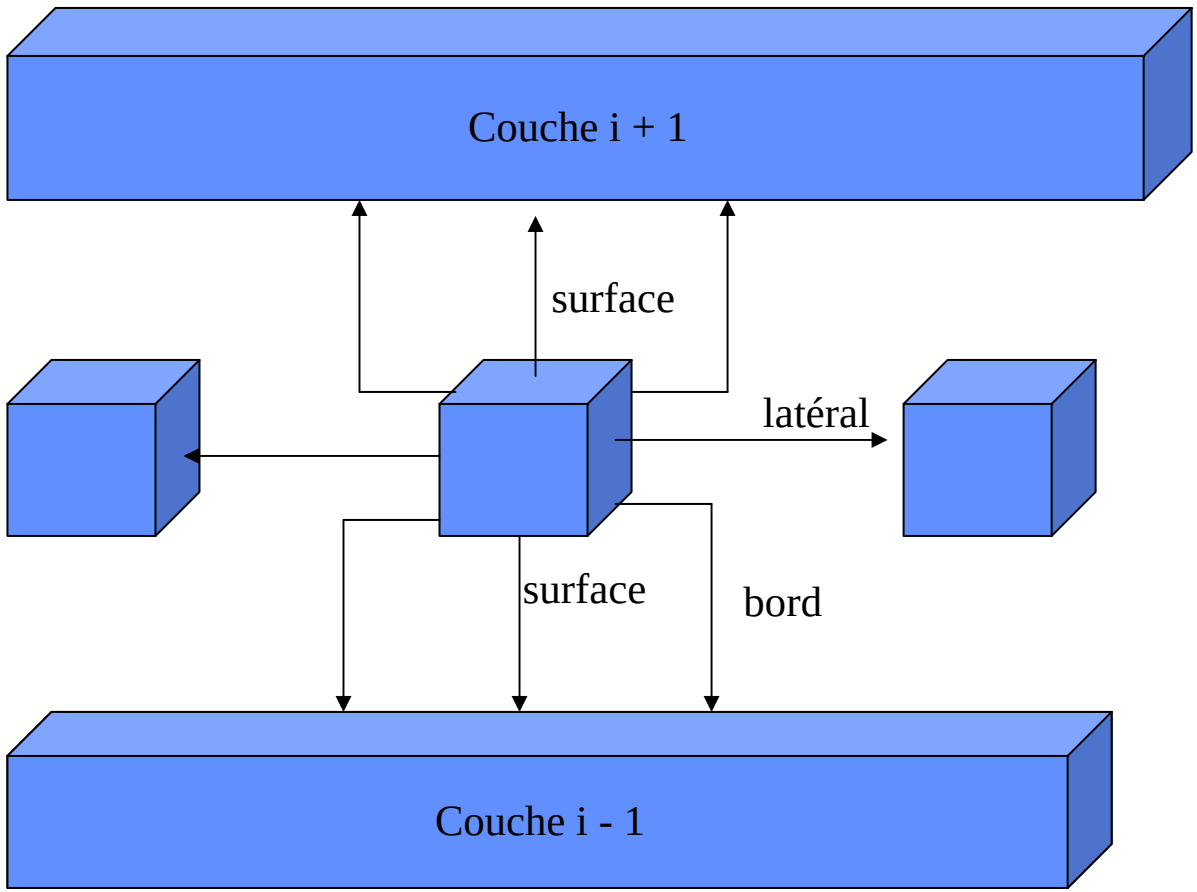
Moore's Law



65 nm Generation Interconnects



Capacités d'interconnexion : technologie 0.13µ (ordres de grandeur)



Capacités d'interconnexion : technologie 0.13µ (ordres de grandeur ➔ Placement-Routage)

Niveau métal	Surface (fF/µm)	Bord (fF/µm)	Latéral (fF/µm)
M1	0.031	0.24	0.1
M2	0.039	0.2	0.11
M3	0.039	0.21	0.1
M4	0.045	0.23	0.11
M5	0.046	0.25	0.11
M6	0.44	0.22	0.14
Moyenne	11%	59%	30%