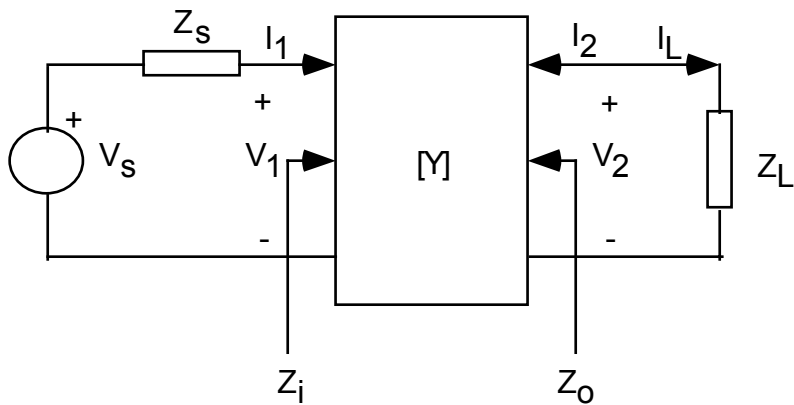


## TWO-PORT PARAMETERS



The two-port current equations are given by:

$$I_1 = y_{11}V_1 + y_{12}V_2 \text{ --- (1)}$$

$$I_2 = y_{21}V_1 + y_{22}V_2 \text{ --- (2)}$$

Its Y-parameter matrix is

$$Y = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix}$$

### Voltage Gain

$$A_v = \frac{V_2}{V_1}$$

The constraint due to load is:

$$V_2 = -Z_L I_2 \text{ or } I_2 = -Y_L V_2 \text{ --- (3)}$$

Substitute (3) to (2)

$$\begin{aligned}
-Y_L V_2 &= y_{21} V_1 + y_{22} V_2 \\
0 &= y_{21} V_1 + (y_{22} + Y_L) V_2 \\
A_V &= \frac{V_2}{V_1} = -\frac{y_{21}}{y_{22} + Y_L} \text{---(4)}
\end{aligned}$$

### Current Gain

$$A_i = \frac{I_L}{I_1} = -\frac{I_2}{I_1} ; I_L = -I_2$$

Substitute (3) to (1) and (2),

$$I_1 = y_{11} V_1 - y_{12} Z_L I_2 \text{---(5)}$$

$$I_2 = y_{21} V_1 - y_{22} Z_L I_2 \text{---(6)}$$

From (5) solve for  $V_1$

$$V_1 = \frac{I_1 + y_{12} Z_L I_2}{y_{11}} \text{---(7)}$$

Substitute (7) to (6)

$$I_2 = y_{21} \left( \frac{I_1 + y_{12} Z_L I_2}{y_{11}} \right) - y_{22} Z_L I_2$$

$$y_{11} I_2 = y_{21} I_1 + y_{12} y_{21} Z_L I_2 - y_{11} y_{22} Z_L I_2 = y_{21} I_1 - \det Y Z_L I_2$$

$$(y_{11} + \det Y Z_L) I_2 = y_{21} I_1$$

$$A_i = -\frac{I_2}{I_1} = -\frac{y_{21}}{\det Y Z_L + y_{11}} = -\frac{y_{21} Y_L}{\det Y + y_{11} Y_L} \text{---(8)}$$

### Input Impedance

$$Z_i = \frac{V_1}{I_1}$$

Substitute (3) to (2)

$$I_2 = -Y_L V_2 = y_{21} V_1 + y_{22} V_2$$

$$V_2 = \frac{-y_{21} V_1}{y_{22} + Y_L} \text{---- (9)}$$

Substitute (9) to (1)

$$I_1 = y_{11} V_1 - \frac{y_{12} y_{21} V_1}{y_{22} + Y_L} = \left( \frac{y_{11} y_{22} - y_{12} y_{21} + y_{11} Y_L}{y_{22} + Y_L} \right) V_1 = \left( \frac{\det Y + y_{11} Y_L}{y_{22} + Y_L} \right) V_1$$

$$Z_i = \frac{V_1}{I_1} = \frac{y_{22} + Y_L}{\det Y + y_{11} Y_L} \text{---- (10)}$$

### Output Impedance

$$Z_o = \left. \frac{V_2}{I_2} \right|_{V_s=0}$$

$$V_1 = -Z_s I_1 = -\frac{1}{Y_s} I_1 \text{---- (11)}$$

Substitute (11) to (1)

$$I_1 = -\frac{y_{11}}{Y_s} I_1 + y_{12} V_2$$

$$I_1 = \frac{y_{12} Y_s V_2}{y_{11} + Y_s} \text{---- (12)}$$

Substitute (11) and (12) to (2)

$$\begin{aligned} I_2 &= -\frac{y_{21}}{Y_s} I_1 + y_{22} V_2 \\ &= -\frac{y_{21} y_{12} Y_s V_2}{Y_s (y_{11} + Y_s)} + y_{22} V_2 = \frac{-y_{21} y_{12} + y_{11} y_{22} + y_{22} Y_s}{y_{11} + Y_s} V_2 = \frac{\det Y + y_{22} Y_s}{y_{11} + Y_s} V_2 \end{aligned}$$

$$Z_o = \frac{V_2}{I_2} = \frac{y_{11} + Y_s}{\det Y + y_{22} Y_s} \text{---- (13)}$$

Summarizing the network functions in term of Y-parameter.

$$Z_i = \frac{V_1}{I_1} = \frac{y_{22} + Y_L}{\det Y + y_{11} Y_L}$$

$$Z_o = \frac{V_2}{I_2} = \frac{y_{11} + Y_S}{\det Y + y_{22} Y_S}$$

$$A_1 = -\frac{I_2}{I_1} = -\frac{y_{21} Y_L}{\det Y + y_{11} Y_L}$$

$$A_v = \frac{V_2}{V_1} = -\frac{y_{21}}{y_{22} + Y_L}$$

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## Simple Current Sink

Figure 1(a) shows a single NMOS transistor as a simple current sink. It is implemented by biasing the transistor at saturation. The current equation at saturation region is given by:

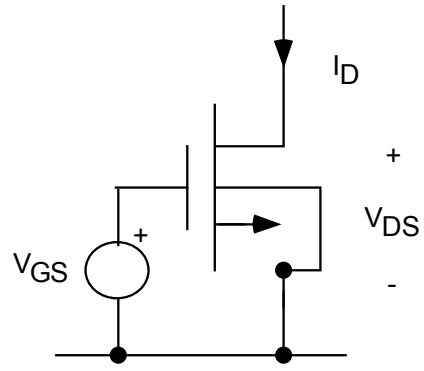
$$I_D = \frac{K_n}{2} \left( \frac{W}{L} \right) (V_{GSn} - V_{Tn})^2 (1 + \lambda V_{DS}) \approx \frac{K_n}{2} \left( \frac{W}{L} \right) (V_{GSn} - V_{Tn})^2 ; V_{GSn} - V_{Tn} \leq V_{DS}$$

The parameter  $\lambda$  is the spice parameter LAMBDA, which typically is a small number. From the Spice parameters file, LAMBDA=.02 (NMOS); .02 (PMOS). The slope of the transfer characteristic represents the ac output conductance of the simple current sink.

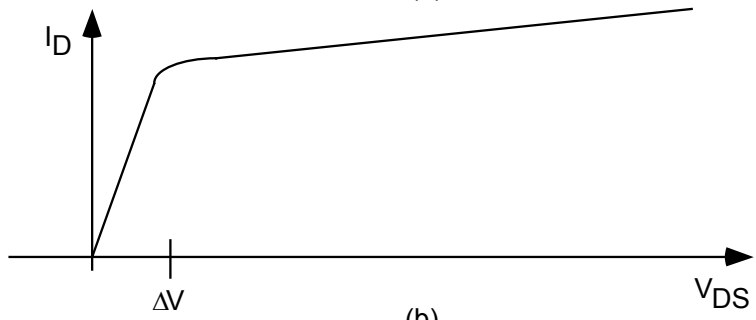
The conductance depends on the parameter  $\lambda$  and its value is derived as follows:

$$g_{ds} = \frac{\partial I_D}{\partial V_{DS}} = \lambda \frac{K_n}{2} \left( \frac{W}{L} \right) (V_{GSn} - V_{Tn})^2 \approx \lambda I_D$$

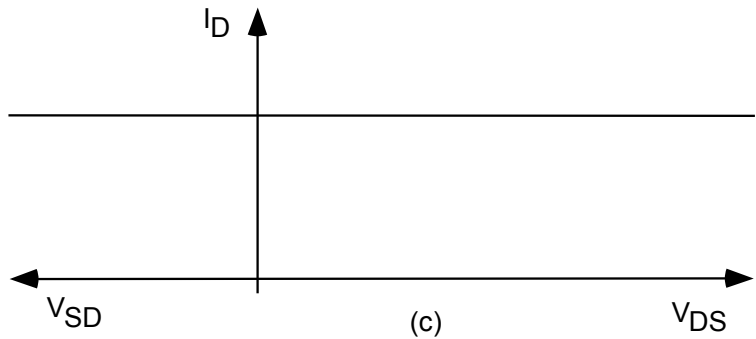
The minimum output voltage of the simple current sink occurs when  $V_{DS} = V_{GSn} - V_{Tn} = \Delta V$ . The characteristic of the simple current sink is shown in Figure 1(b). The ideal current sink shown in Figure 1(c) has a horizontal transfer characteristic, indicating that the current is constant for any output voltage  $V_{DS}$ . That is, an ideal current sink has infinite output impedance (or zero output conductance), and the minimum output voltage is zero. In addition, the output voltage swing both positive and negative. The nmos implementation actually capture both positive and negative output voltage swing, but only the positive swing is normally shown. The reason can be explained using Figure 1(d) and (e). An nmos device is a symmetrical device the source (S) and drain (D) are physically indistinguishable. The designation is not known until the output voltage  $V_{DS}$  is applied. The positive side is always the drain(D) side of the nmos transistor.



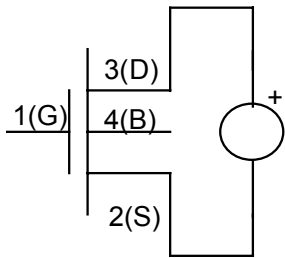
(a)



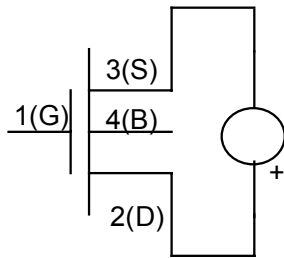
(b)



(c)



(d)



(e)

Figure 1. Simple Current Sink.

## Cascode Current Sink

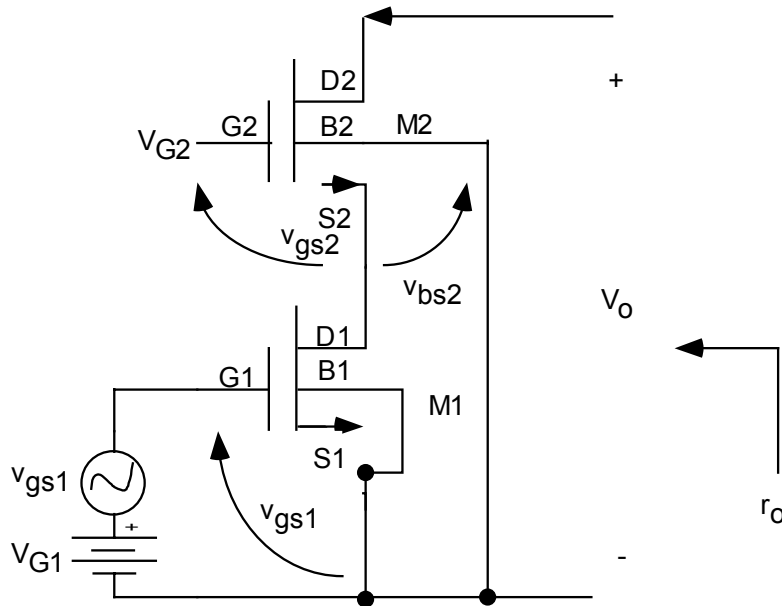


Figure 2. Cascode current sink.

To achieve a more ideal current sink, one needs to increase the output impedance. This can be achieved by adding a cascode (common gate) stage at the output of the simple current sink. The cascode is an impedance converter. It magnifies the output impedance of the simple current sink by the gain of the cascode stage. This will be derived shortly. The cascode current sink is shown in Figure 2. Two reference voltages ( $V_{G1}$  and  $V_{G2}$ ) are required to establish the operating point of the common source and cascode stage respectively. To determine the ac output impedance, one needs to perturb the input signal by adding (super-imposing)  $v_{gs1}$  to  $V_{G1}$ , this is shown in Figure 2. The small signal equivalent circuit shown in Figure 3 is used to determine the output impedance of the cascode current sink. Figure 3(a) is transformed to Figure 3(b) using the following ac voltage signal equivalent derived from Figure 2:

$$V_{gs2} = -V_{ds1}$$

$$V_{bs2} = -V_{ds1}$$

A two-port analysis method will be used to achieve this. The current equation of network is obtained as follows:

$$I_1^a = 0$$

$$I_2^a = g_{m1} V_1^a + g_{ds1} V_2^a$$

The corresponding Y-parameter matrix is :

$$Y^a = \begin{bmatrix} 0 & 0 \\ g_{m1} & g_{ds1} \end{bmatrix}$$

$$\det Y^a = 0$$

The current equation of network b is:

$$I_1^b = (g_{m2} + g_{mb2} + g_{ds2}) V_1^b - g_{ds2} V_2^b$$

$$I_2^b = -(g_{m2} + g_{mb2} + g_{ds2}) V_1^b + g_{ds2} V_2^b$$

The corresponding Y-parameter matrix is:

$$Y^b = \begin{bmatrix} (g_{m2} + g_{mb2} + g_{ds2}) & -g_{ds2} \\ -(g_{m2} + g_{mb2} + g_{ds2}) & g_{ds2} \end{bmatrix}$$

$$\det Y^b = 0$$

To calculate the output impedance, one needs to first calculate the output impedance of network a. That is,

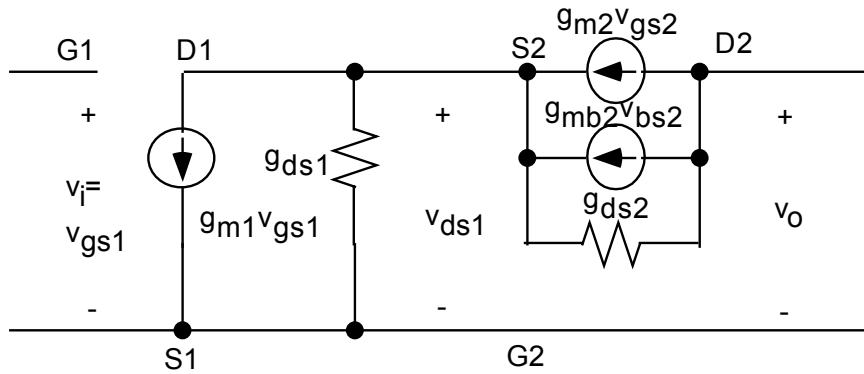
$$Z_o^a = \frac{y_{11}^a + Y_S^a}{\det Y^a + y_{22}^a Y_S^a} = \frac{1}{y_{22}^a} = \frac{1}{g_{ds1}}; \text{ since } Y_S^a = \infty \text{ or } Z_S^a = 0$$

The output impedance is computed as follows:

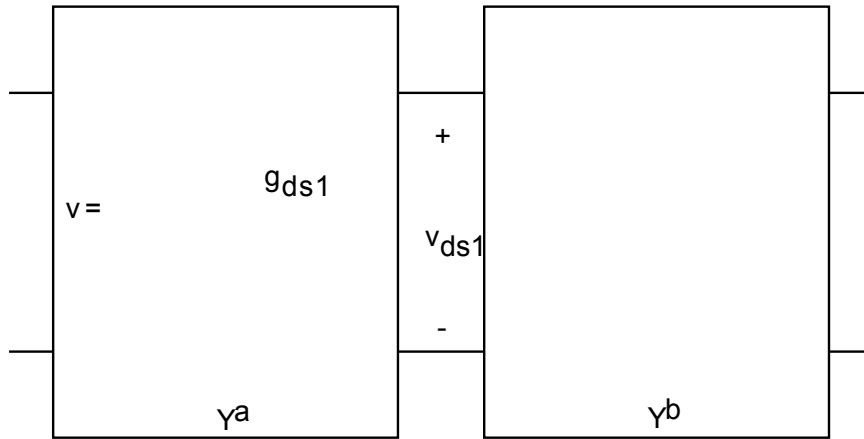
$$\begin{aligned} r_o = Z_o^b &= \frac{y_{11}^b + Y_S^b}{\det Y^b + y_{22}^b Y_S^b} = \frac{(g_{m2} + g_{mb2} + g_{ds2}) + g_{ds1}}{g_{ds2} g_{ds1}}; \text{ since } Y_S^b = Y_o^a = g_{ds1} \\ &= r_{ds2} r_{ds1} (g_{m2} + g_{mb2} + g_{ds2}) + r_{ds2} = r_{ds2} [r_{ds1} (g_{m2} + g_{mb2} + g_{ds2}) + 1] \approx (g_{m2} r_{ds2}) r_{ds1} \end{aligned}$$

That is, the output impedance is equal to the output impedance of the simple current sink magnified by the gain of the common gate stage.

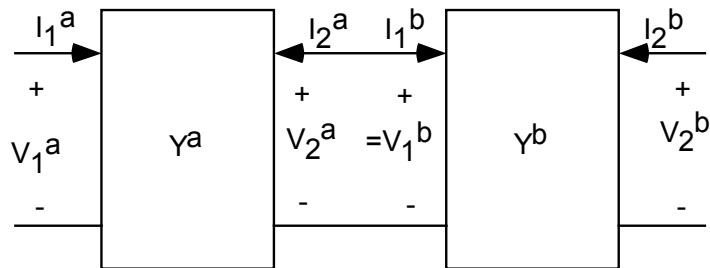
NOTE:  $v_{gs2} = -v_{ds1}$ ;  $v_{bs2} = -v_{ds1}$



(a)



(b)



(c)

Figure 3. Cascode current sink small signal equivalent circuit.

## Single Voltage Reference

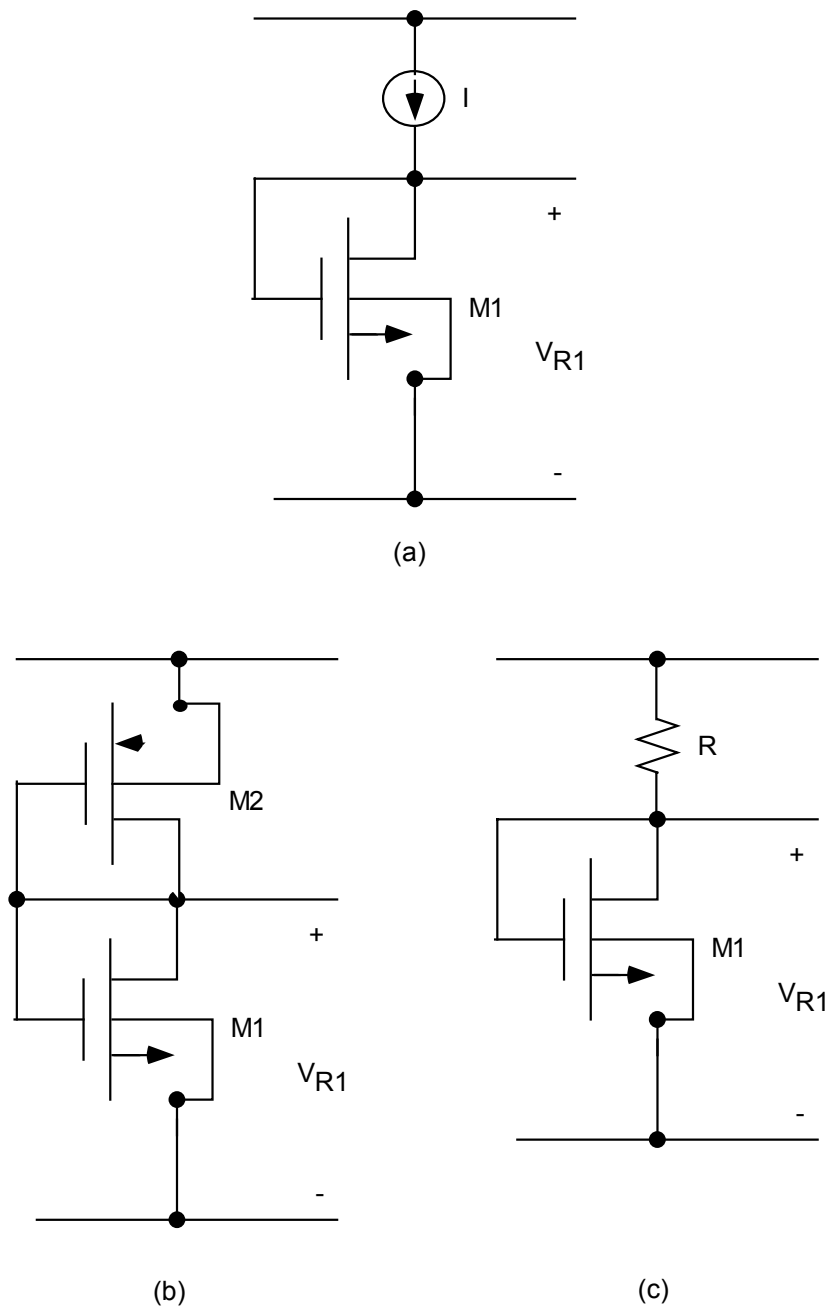


Figure 4. Single voltage reference circuit.

The voltage reference is achieved by passing a current through a resistor, implemented by a diode connected transistor, shown in Figure 4 (a). There are two ways of implementing the current source. In Figure 4(b), a current source is implemented by a pmos transistor with a constant gate to source voltage. The gate is connected to the constant voltage reference,  $V_{R1}$ , and the source is connected to the constant positive power supply  $V_{DD}$ . The pmos and nmos are connected in series in Figure 4(b). That is,

$$I_p = I_n$$

$$\frac{K_p}{2} \left( \frac{W}{L} \right)_2 (V_{DD} - V_{R1} - |V_{Tp}|)^2 = \frac{K_n}{2} \left( \frac{W}{L} \right)_1 (V_{R1} - V_{Tn})^2$$

$$\frac{\beta_p}{2} (V_{DD} - V_{R1} - |V_{Tp}|)^2 = \frac{\beta_n}{2} (V_{R1} - V_{Tn})^2$$

Solving for  $V_{R1}$ ,

$$V_{R1} = \frac{\sqrt{\frac{\beta_n}{\beta_p}} V_{Tn} + (V_{DD} - |V_{Tp}|)}{1 + \sqrt{\frac{\beta_n}{\beta_p}}}$$

The design parameter is given by:

$$\frac{\beta_n}{\beta_p} = \left( \frac{V_{DD} - V_{R1} - |V_{Tp}|}{V_{R1} - V_{Tn}} \right)^2$$

This determine the transconductance ratio for a given reference voltage. The power dissipation of this circuit is:

$$P = I_D V_{DD} = \left[ \frac{\beta_n}{2} (V_{R1} - V_{Tn})^2 \right] V_{DD}$$

In Figure 4 (c), the current source is implemented by resistor R with constant voltage applied across it. That is,

$$I = \frac{V_{DD} - V_{R1}}{R} = \frac{\beta_n}{2} (V_{R1} - V_{Tn})^2$$

The reference voltage is given by:

$$V_{R1} = \sqrt{\frac{2I}{\beta_n}} + V_{Tn}$$

Figure 5 shows the circuit combining the single voltage reference and simple current sink. PSpice simulation will be shown in the last section.

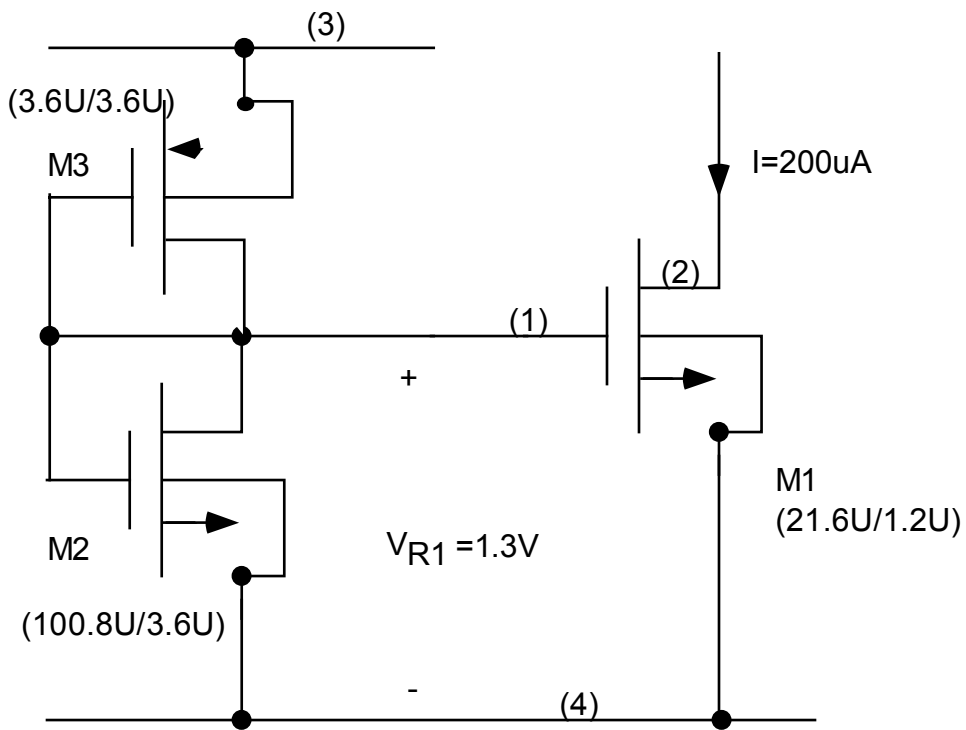


Figure 5. Single voltage reference circuit and current sink.

## Multiple-Voltage Reference Circuit

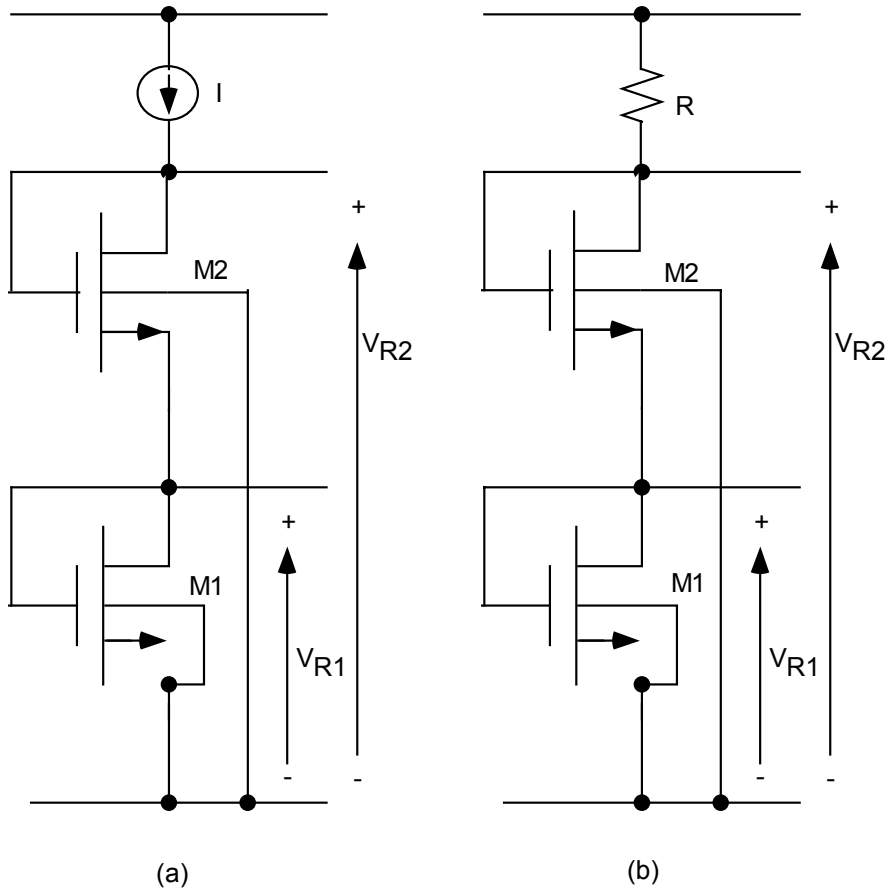


Figure 6. Dual voltage reference circuit.

Multiple-voltage reference is achieved by cascading a number of resistors equal to the number desired of voltage references. The resistor is implemented by diode connected nmos transistor. The dual -voltage reference is shown in Figure 6(a). The current source is implemented by resistor R in Figure 6(b) with constant voltage applied across it. The resistor and the two nmos transistors are connected in series, hence the currents in the elements are equal. That is,

$$I = \frac{V_{DD} - V_{R2}}{R} = \frac{\beta_{n2}}{2} (V_{R2} - V_{R1} - V_{Tn2})^2 = \frac{\beta_{n1}}{2} (V_{R1} - V_{Tn1})^2$$

Solving for  $V_{R1}$ ,

$$V_{R1} = \sqrt{\frac{2I}{\beta_{n1}}} + V_{Tn1}$$

Solving for  $V_{R2}-V_{R1}$ ,

$$V_{R2} - V_{R1} = \sqrt{\frac{2I}{\beta_{n2}}} + V_{Tn2}$$

Substituting  $V_{R1}$ , and solving for  $V_{R2}$

$$V_{R2} = \sqrt{\frac{2I}{\beta_{n2}}} + \sqrt{\frac{2I}{\beta_{n1}}} + V_{Tn1} + V_{Tn2}$$

Where:

$$V_{Tni} = V_{Ton} + \gamma(\sqrt{\phi - V_{BS}} - \sqrt{\phi})$$

The corresponding nmos SPICE parameters are:

$$V_{Ton} = V_{TO} = 1.0V$$

$$\gamma = \text{GAMMA} = 1.0V^{1/2}$$

$$\phi = \text{PHI} = 0.6V$$

$$\lambda = \text{LAMBDA} = 0.02 \text{ 1/V}$$

$$V_{Tn1} = V_{Ton} = 1; \quad V_{BS1} = 0$$

$$V_{Tn2} = V_{Ton} + \gamma(\sqrt{\phi - V_{BS}} - \sqrt{\phi}) = 1.0 + 1.0(\sqrt{0.6 + V_{R1}} - \sqrt{0.6}) = 1.0 - \sqrt{0.6} + \sqrt{0.6 + V_{R1}}; \quad V_{BS} = -V_{R1}$$

Note the bulk to source bias increases the threshold voltage. That is,  $V_{Tn2} > V_{Tn1}$ .

## Biasing Cascode Current Sink

The principle used in biasing MOS transistor. The minimum  $V_{DS}$  for which the device remain in saturation is:

$$V_{DSmin} = V_{GS} - V_T = \Delta V$$

$$I_D = \frac{K}{2} \left( \frac{W}{L} \right) (\Delta V)^2$$

If transistors M1 and M2 are in series or have the same current then:

$$I_{D1} = I_{D2}$$

$$\frac{K_1}{2} \left( \frac{W}{L} \right)_1 (\Delta V_1)^2 = \frac{K_2}{2} \left( \frac{W}{L} \right)_2 (\Delta V_2)^2$$

If M1 and M2 are of the same type either both are nmos or pmos. Then the expression reduces to:

$$\left(\frac{W}{L}\right)_1 (\Delta V_1)^2 = \left(\frac{W}{L}\right)_2 (\Delta V_2)^2$$

If  $\Delta V_1 = n\Delta V_2$

$$\left(\frac{W}{L}\right)_1 (n\Delta V_2)^2 = \left(\frac{W}{L}\right)_2 (\Delta V_2)^2$$

then

$$\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2 / n^2$$

That is,  $(W/L)$  can be used to control the values of  $\Delta V$ . If the transistors are in parallel or  $\Delta V_1 = \Delta V_2$ , then:

$$\Delta V_1 = \Delta V_2$$

$$\sqrt{\frac{2I_{D1}}{K_1(W/L)_1}} = \sqrt{\frac{2I_{D2}}{K_2(W/L)_2}}$$

$$\frac{I_{D1}}{K_1(W/L)_1} = \frac{I_{D2}}{K_2(W/L)_2}$$

If transistor M1 and M2 are of the same type ( $K_1 = K_2$ ), the expression reduces to:

$$I_{D1} \left(\frac{W}{L}\right)_2 = I_{D2} \left(\frac{W}{L}\right)_1$$

Applying the above biasing principle to the cascode current sink shown in Figure 7. All the transistors are assumed to be operating in saturation, have the same  $(W/L)$  and all are of the nmos type. Since all transistor have the same  $(W/L)$  and are of the same type means  $(\Delta V)_i = \Delta V$ . That is, the gate to source  $V_{GS}$  of each transistor must be  $V_T + \Delta V$  to be in saturation. This is shown in Figure 7(a). M3 and M4 operate as voltage divider, each transistor is diode connected. The voltage at the gate of M4,  $V_{G4}$ , is the sum of  $V_{GS}$  (or  $V_{DS}$ ) of transistor M3 and M4. That is,

$$V_{G4} = V_{G2} = (V_T + \Delta V) + (V_T + \Delta V) = 2V_T + 2\Delta V$$

The minimum output voltage is determined as follows:

$$V_{\text{out}}(\text{min}) = V_{\text{DS1}}(\text{min}) + V_{\text{DS2}}(\text{min})$$

$$V_{\text{DS1}}(\text{min}) = V_{\text{G2}} - V_{\text{GS2}} = 2V_{\text{T}} + 2\Delta V - (V_{\text{T}} + \Delta V) = V_{\text{T}} + \Delta V$$

$$V_{\text{DS2}}(\text{min}) = \Delta V$$

$$V_{\text{out}}(\text{min}) = V_{\text{T}} + 2\Delta V$$

The transfer characteristic is illustrated in Figure 7(b). The value of  $V_{\text{T}}$  is typically about 1 V, while  $\Delta V$  is typically about 0.2 to 0.3 V, the sum is about 1.4 to 1.6. This value will significantly limit the dynamic range of the output voltage, specially in low voltage application.

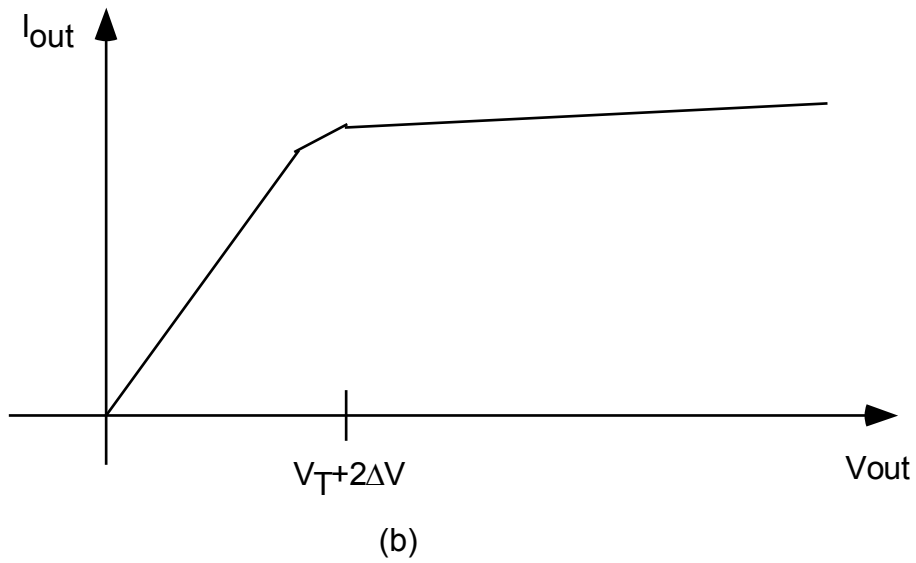
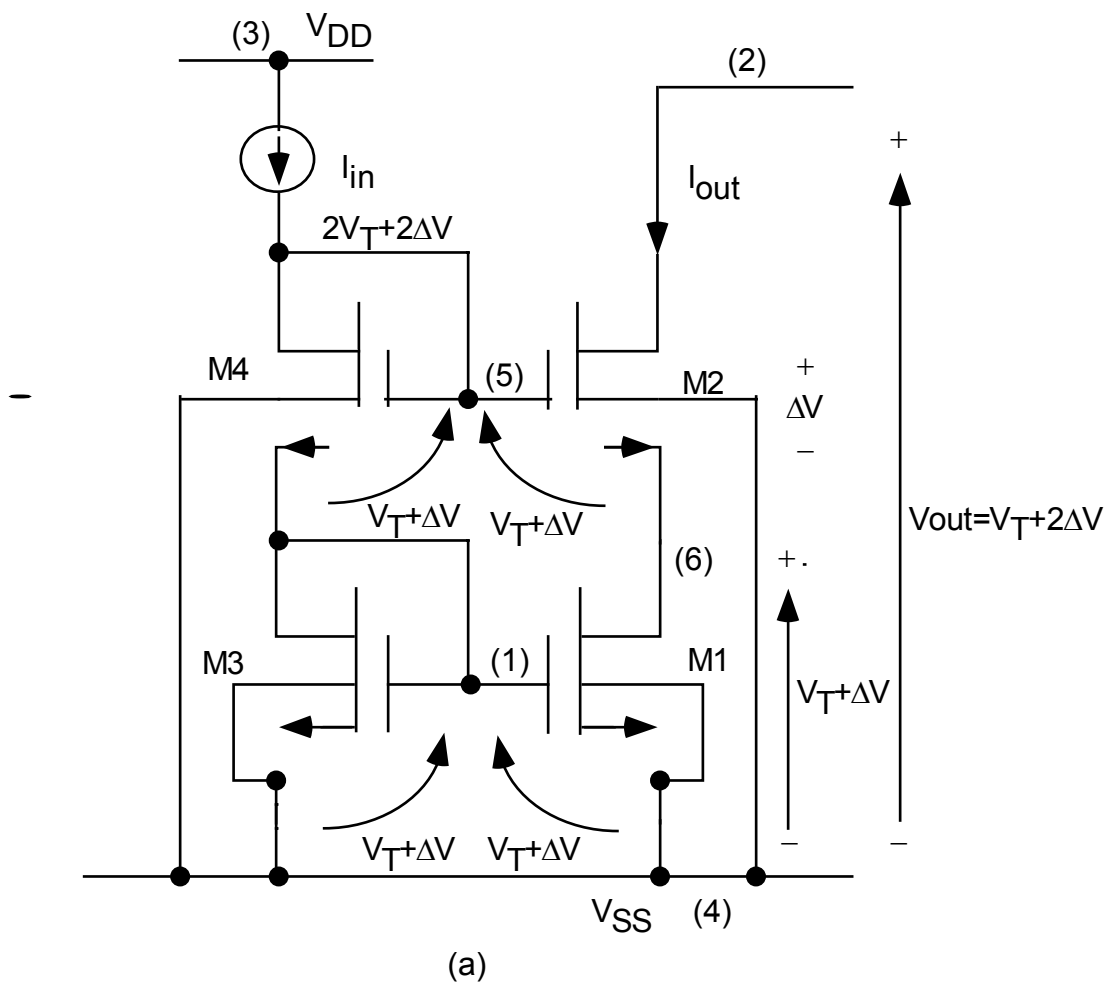


Figure 7. Cascode current sink bias requirement.

## Simple Current Mirror

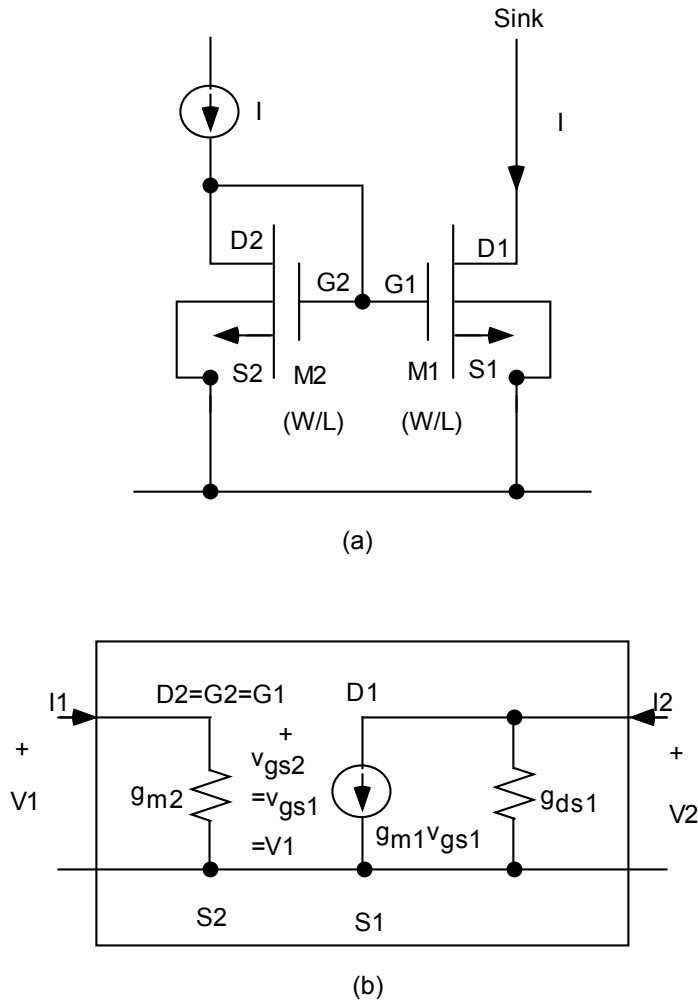


Figure 8. Simple current mirror and its small signal equivalent circuit.

The purpose of current mirror is to generate another current sources or sinks from a stabilized current source or sink. Figure 8 shows how to create a current sink from a known current source  $I$ . The diode connected transistor  $M2$  is connected to the current source. The gate and source of both transistor are connected to each other; hence,  $V_{GS1} = V_{GS2} = V_{GS}$ . The current ratio is given by:

$$\frac{I_1}{I_2} = \frac{K(W/L)_1(V_{GS} - V_T)^2}{K(W/L)_2(V_{GS} - V_T)^2}$$

$$\frac{I_1}{I_2} = \frac{(W/L)_1}{(W/L)_2}$$

$$I_1 = \frac{(W/L)_1}{(W/L)} I; I_2 = I, (W/L)_2 = (W/L)$$

$$I_1 = I; (W/L)_1 = (W/L)$$

$$I_1 = nI; (W/L)_1 = n(W/L)$$

Figure 9 (a) shows current mirrors generating current sinks of different values from a single current source.

Figure 9 (b) shows current mirrors generating current sources of different values from a single current sink. These generated current sinks or sources are usually used as load of the various circuits. It is of interest to know what is the impedance of the mirrored source or sink. Figure 8(b) shows the small signal equivalent circuit. The output impedance is computed using the two-port analysis. The current equations are computed:

$$I_1 = g_{m2} V_1$$

$$I_2 = g_{m1} V_1 + g_{ds1} V_2$$

The corresponding Y-parameter matrix is:

$$Y = \begin{bmatrix} g_{m2} & 0 \\ g_{m1} & g_{ds1} \end{bmatrix}$$

$$\det Y = g_{m2} g_{ds1}$$

The output impedance is calculated as follows:

$$Z_o = r_o = \frac{y_{11} + Y_S}{\det Y + y_{22} Y_S} = \frac{1}{g_{ds1}} ; \text{ since } Y_S = \infty \text{ or } Z_S = 0$$

That is, the mirrored current sink impedance is  $r_{ds1}$  only.

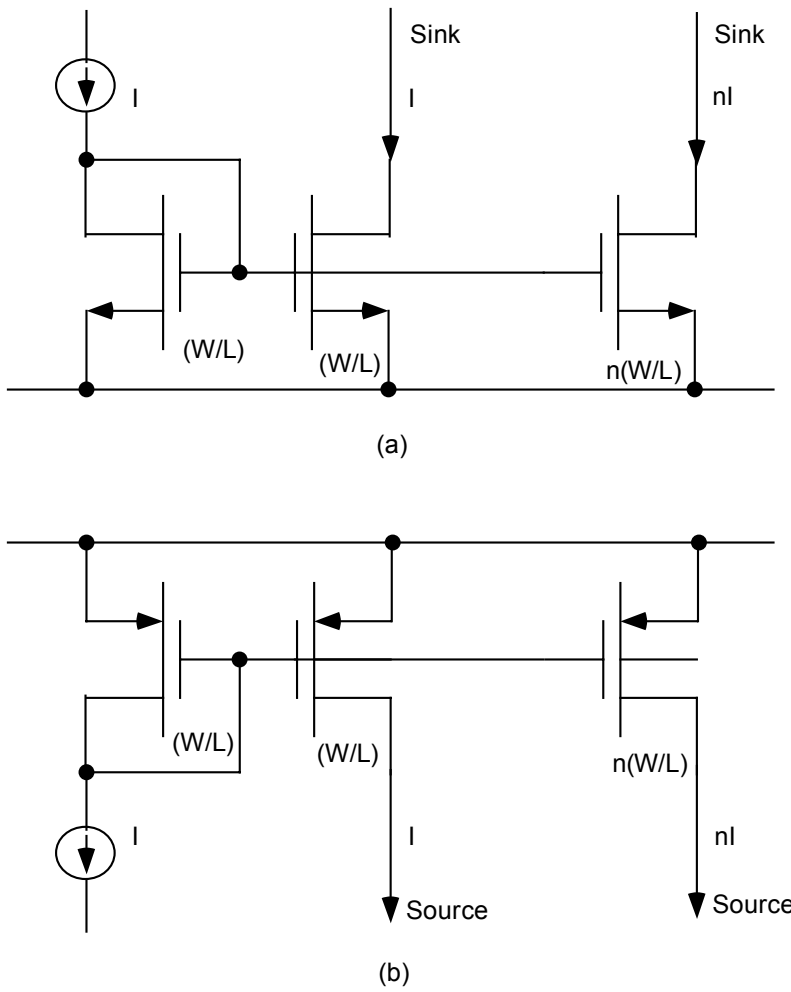


Figure 9. Using simple current mirror to generate multiple current sinks and current sources.

## Cascode Current Mirror

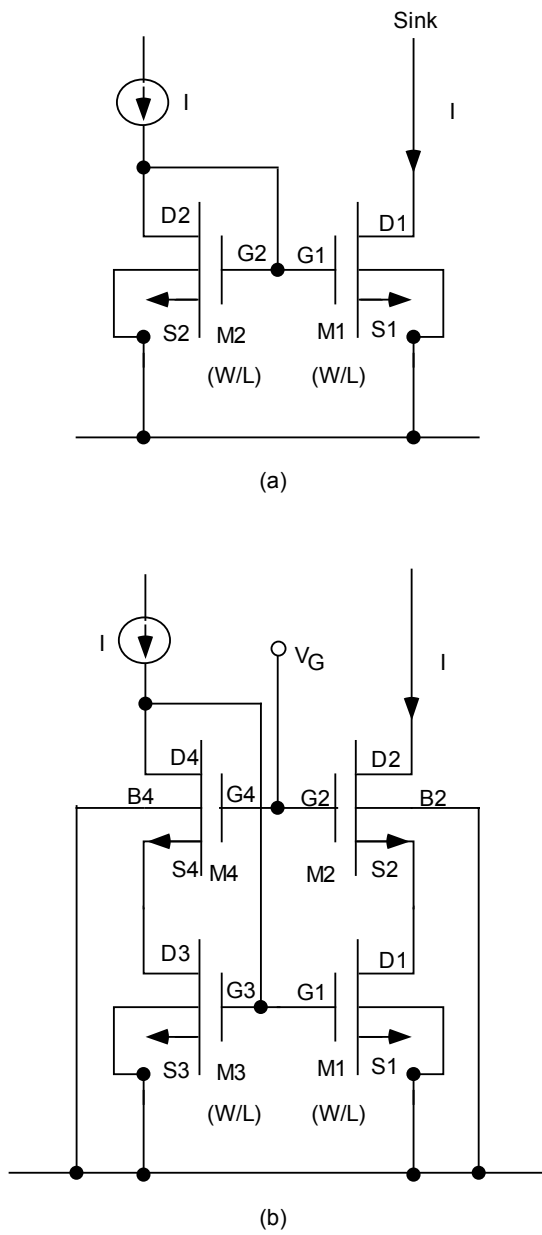


Figure 10. Cascode current mirror.

Although the current source is ideal with  $\infty$  impedance, the mirrored impedance is  $r_{ds}$  only. Since the mirrored current sink or source are used as load of gain stages, it is desired that the impedance be as high as possible. Figure 10 shows the corresponding cascode current mirror by adding cascode (common gate) stage at the diode connected stage and the mirror stage. As in the earlier analysis, the output impedance is magnified by the gain of the cascode stage. That is,

$$Z_o = r_o = (g_{m1} r_{ds2}) r_{ds1}$$

Transistor M3 and M4 is the two-transistor version of diode connected transistor. In the cascode current mirror, the voltage at gate of M2 or M4 must be biased properly to produce minimum output voltage. Figure 11 shows the biasing requirement to achieved a wide-swing cascode current mirror. That is, to achieve minimum output voltage,  $V_{DS1(\min)} = \Delta V$ . This can be achieved, if the gate voltage of M2 is  $V_T + (n+1)\Delta V$ . This voltage is also the gate to source voltage of transistor M5. It is generated by controlling the  $(W/L)$  of M5,  $(W/L)_5 = (W/L)/(n+1)^2$ , see Figure 11(a). To guarantee that the transistor M4 is in saturation, one must guarantee that  $V_{DS4} > n \Delta V$ ; since  $(W/L)_4 = (W/L)/n^2$ . The diode connection with M3 also put another constraint on  $V_{DS4}$ . That is,

$$V_{DS4} = V_{G3} - V_{DS3} = (V_T + \Delta V) - (\Delta V) = V_T$$

$$V_{DS4} = V_T > n(\Delta V)$$

That is, one must guarantee that  $V_T > n \Delta V$  for M4 to be in saturation. For  $V_T = 1V$  and  $\Delta V = 0.2$ , then  $n < 5$  to guarantee that M4 will operate in saturation. In the special of  $n=1$ , the minimum output voltage is  $2 \Delta V$ .

In the above analysis, the effect of the bulk to source voltage on the threshold voltage of M2 and M4 were ignored. The threshold voltage of both M2 and M4 are significantly higher than that of M1 and M3. In the PSpice simulation, it will be shown that the bulk to source voltage can not be ignored.

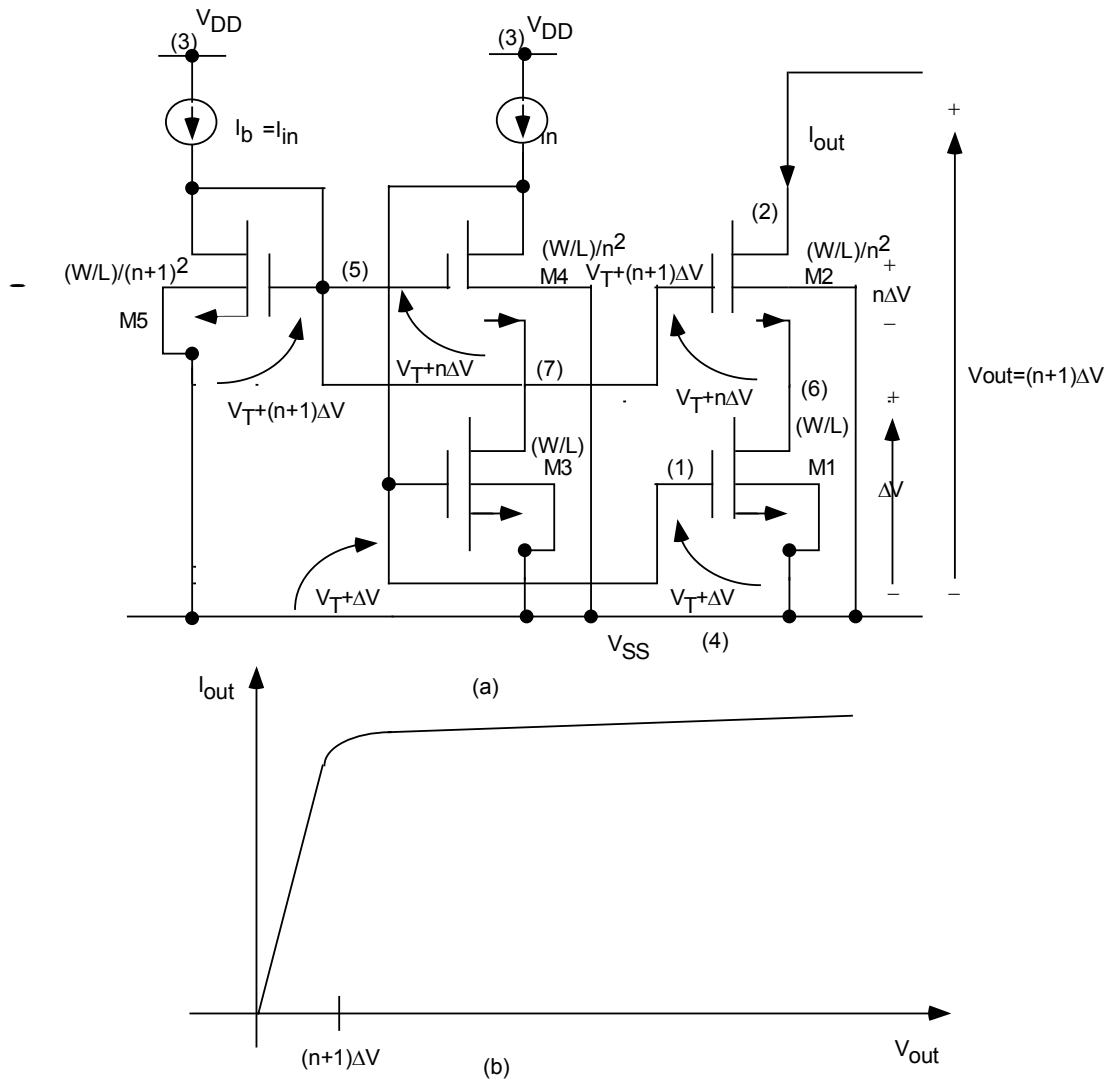


Figure 11. Generalized wide-swing cascode current mirror.

## Experiments on Current Sink/Source and Voltage Reference

### Simple Current Sink

A current sink or source can be obtained by operating the MOS transistor in the saturation mode with fixed gate to source bias,  $V_{GS}$ . Current sink is implemented using NMOS transistor as shown in Figure 5.

A design of 200 uA current sink will be illustrated in the following. To prevent going to weak inversion region,  $V_{GS} - V_T > 0.2$  V. For  $V_T = 1$ , this can be satisfied by selecting  $V_{GS} = 1.3$ .

$$I_D = (\beta_N / 2)(V_{GS} - V_T)^2$$

where:

$$\beta_N = K_N (W / L)$$

Solve for W/L,

$$\frac{W}{L} = \frac{2I_D}{K_N (V_{GS} - V_T)^2} = \frac{2I_D}{K_N (V_G - V_{SS} - V_T)^2}$$

Substituting the given design parameters,

$$\frac{W}{L} = \frac{2(200E - 6)}{(40E - 6)(1.3 - 0 - 1)^2} = 111.1$$

Let  $L=1.2\mu$  (the minimum feature length), its effective length is  $L_{eff} = L - 2LD = 1.2\mu - 2(0.5\mu) = 0.2\mu$ . The W is calculated from  $W = 111.1 * L_{eff} = 111.1 * (0.2\mu) = 22.22\mu$ , rounded to say 21.6u (or 36  $\lambda$ ).

In the design of 200uA current sink, to establish the gate to source voltage of  $V_{GS} = 1.3$  requires a gate voltage of  $V_G = 1.3$  to be generated from the available supply voltages. Figure 5 shows a voltage divider circuit, it consists of two diode connected transistors, acting as two resistors connected in series. Each transistor is design to operates in the saturation mode. Its current equation must satisfy:

$$I_P = I_N$$

where:

$$I_P = (\beta_P / 2)(|V_{GSP}| - |V_{TP}|)^2, \text{ and } \beta_P = K_P (W_P / L_P)$$

$$I_N = (\beta_N / 2)(V_{GSN} - V_{TN})^2, \text{ and } \beta_N = K_N (W_N / L_N)$$

Equating and solving for W/L ratio:

$$\frac{W_N / L_N}{W_P / L_P} = \frac{K_P (|V_{GSP}| - |V_{TP}|)^2}{K_N (V_{GSN} - V_{TN})^2}$$

When laying out the voltage divider, the lengths of both transistors are usually made equal,  $L_P = L_N$ . Thus the equation simplify to width ratio.

$$\frac{W_N}{W_P} = \frac{K_P (|V_{GSP}| - |V_{TP}|)^2}{K_N (V_{GSN} - V_{TN})^2} = \frac{K_P (|V_G - V_{DD}| - |V_{TP}|)^2}{K_N (V_G - V_{SS} - V_{TN})^2}$$

Substituting for the given parameters:

$$\frac{W_N}{W_p} = \frac{(15E-6)(|1.3-0|-|-1|)^2}{(40E-6)(1.3-0-1)^2} = 30.375$$

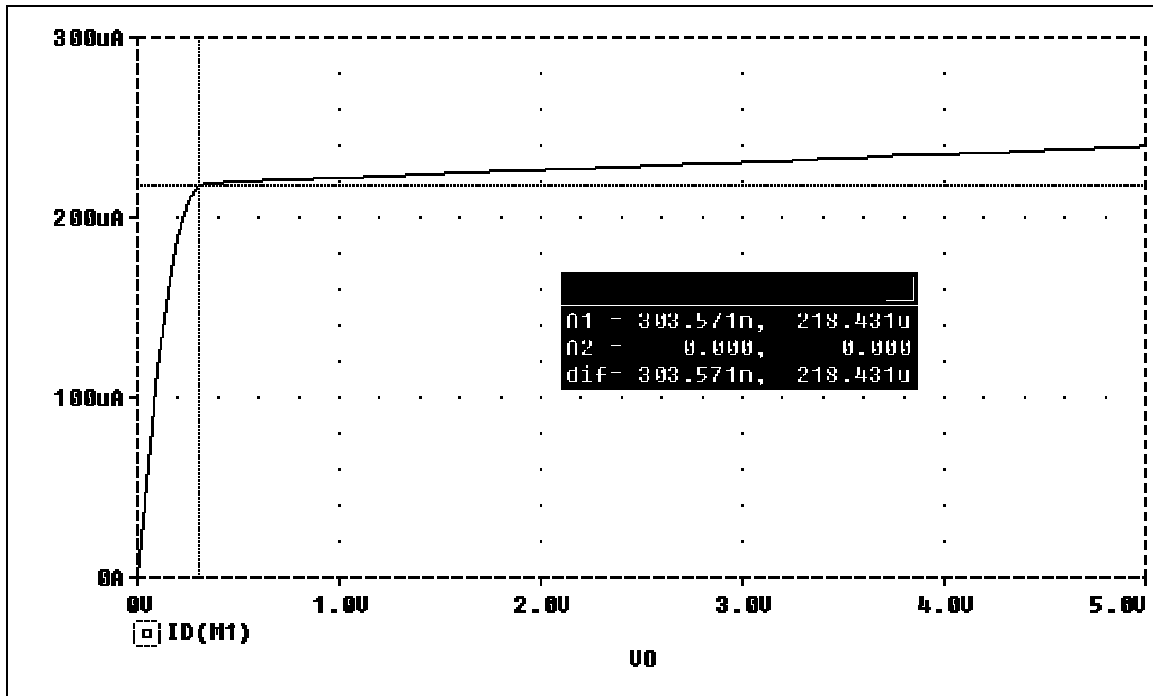
The minimum gate length (L) is  $2\lambda$ , while the minimum gate width (W) is  $6\lambda$ . The computed W/L ratio of the voltage divider is rounded to 30. Let  $W_p=6\lambda$ ,  $W_N=30*W_p=180\lambda$ . Some fine tuning was found necessary to achieved the desired voltage of 1.3v , the resulting  $W_N=168\lambda=100.8\mu$ . The output resistance is computed as follows:

$$r_o = r_{ds} = \frac{1}{\lambda I_{DQ}} = \frac{1}{(.02)(200E-6)} = 0.25M \text{ or } 2.5 \times 10^5$$

This is within 3% of the value obtained from PSpice simulation,  $2.572 \times 10^5$ .

```
*Pspice file for 200uA Current Source
* Filename="c200fg4.cir"
VDD 3 0 DC 5VOLT
VSS 4 0 DC 0VOLT
VO 2 4 DC 1.5VOLT
M1 2 1 4 4 MN W=21.6U L=1.2U
M2 1 1 4 4 MN W=100.8U L=3.6U
M3 1 1 3 3 MP W=3.6U L=3.6U

.MODEL MN NMOS VTO=1.0 KP=40U
+ GAMMA=1.0 LAMBDA=0.02 PHI=0.6
+ TOX=0.05U LD=0.5U CJ=5E-4 CJSW=10E-10
+ U0=550 MJ=0.5 MJSW=0.5 CGSO=0.4E-9 CGDO=0.4E-9
.MODEL MP PMOS VTO=-1.0 KP=15U
+ GAMMA=0.6 LAMBDA=0.02 PHI=0.6
+ TOX=0.05U LD=0.5U CJ=5E-4 CJSW=10E-10
+ U0=200 MJ=0.5 MJSW=0.5 CGSO=0.4E-9 CGDO=0.4E-9
.DC VO 0 5.0 0.05
.TF V(2) VO
.PROBE
.END
```



NODE VOLTAGE:

( 1) 1.3000 ( 2) 1.5000 ( 3) 5.0000 ( 4) 0.0000

OUTPUT RESISTANCE AT VO = 2.572E+05

## Cascode Current Sink

The biasing formula derive earlier assume that the effect of the bulk to source voltage can be ignored. This is the not case in the cascode current sink, the threshold voltage of M2 and M4 are significantly higher than M1 and M3. From Figure 7, the source of M2 is connected at a potential of  $V_{T0} + \Delta V = 1 + 0.3 = 1.3$ , and the bulk at  $V_{SS} = 0$ . That is,  $V_{BS} = -1.3$ . The threshold voltage is calculated as follows:

$$V_T = V_{T0} + \gamma(\sqrt{\phi - V_{BS}} - \sqrt{\phi}) = 1 + 1(\sqrt{0.6 - (-1.3)} - \sqrt{0.6}) = 1.6$$

The gate voltage of M2 need to be modified from:

$$V_{G2} = 2V_T + 2\Delta V$$

to :

$$V_{G2} = V_T + V_{T0} + 2\Delta V = 1.6 + 1 + 2(0.3) = 3.2$$

The calculated value is within .09% of the actual value obtained from PSpice simulation, which is the voltage at node 5 of 3.203V. The minimum output voltage of M1 is given by:

$$V_{DS1}(\text{min}) = V_T + \Delta V = V_{TO} + \Delta V = 1 + 0.3 = 1.3$$

This voltage correspond to node 6 in the PSpice simulation of 1.2989V, which is within 0.08% of the calculated value. The minimum output voltage is given by:

$$V_{\text{out}}(\text{min}) = V_T + 2\Delta V = V_{TO} + 2\Delta V = 1 + 2(0.3) = 1.6$$

The PSpice transfer characteristic shows that the output current stabilized at 200uA when the output voltage is about 1.6V

The output impedance can be calculated as follows:

$$g_{m2} = \sqrt{2K(W/L)I_{DQ}} = \sqrt{2(40E-6)(21.6/(1.2-1))(200E-6)} = 1.3145 \times 10^{-3} \text{ mho}$$

$$g_{mb2} = \frac{\gamma}{2\sqrt{\phi - V_{BS}}} g_{m2} = \frac{1}{2\sqrt{0.6 - (-1.3)}} (1.3145E-3) = 0.4768 \times 10^{-3} \text{ mho}$$

$$g_{ds2} = g_{ds1} = g_{ds} = \lambda I_{DQ} = (.02)(200E-6) = 4E-6$$

or

$$r_{ds2} = r_{ds1} = r_{ds} = \frac{1}{g_{ds}} = 0.25E+6$$

$$r_O = r_{ds2} [r_{ds1} (g_{m2} + g_{mb2} + g_{ds2}) + 1] \\ = (.25E+6)[(.25E+6)(1.3145E-3 + .4768E-3 + 4E-6) + 1] = 1.122 \times 10^8$$

The PSpice simulation output impedance is  $1.195 \times 10^8$  which is 6% of the calculated value. If one substitutes the Pspice output impedance of the simple current sink  $r_o = r_{ds} = .2572 \times 10^6$ , the calculated results is  $1.185 \times 10^8$ . This value is now within 0.83% of the PSpice result.

```
* Pspice file for 200uA Current Source
* Filename="c200fg7.cir"
VDD 3 0 DC 5VOLT
VSS 4 0 DC 0VOLT
VO 2 4 DC 2.5VOLT
I 3 5 DC 200UA
M1 6 1 4 4 MN W=21.6U L=1.2U
M2 2 5 6 4 MN W=21.6U L=1.2U
M3 1 1 4 4 MN W=21.6U L=1.2U
M4 5 5 1 4 MN W=21.6U L=1.2U
```

```

.MODEL MN NMOS VTO=1.0 KP=40U
+ GAMMA=1.0 LAMBDA=0.02 PHI=0.6
+ TOX=0.05U LD=0.5U CJ=5E-4 CJSW=10E-10
+ U0=550 MJ=0.5 MJSW=0.5 CGSO=0.4E-9 CGDO=0.4E-9
.MODEL MP PMOS VTO=-1.0 KP=15U
+ GAMMA=0.6 LAMBDA=0.02 PHI=0.6
+ TOX=0.05U LD=0.5U CJ=5E-4 CJSW=10E-10
+ U0=200 MJ=0.5 MJSW=0.5 CGSO=0.4E-9 CGDO=0.4E-9
.DC VO 0 5.0 0.05
.TF V(2) VO
.PROBE
.END

```

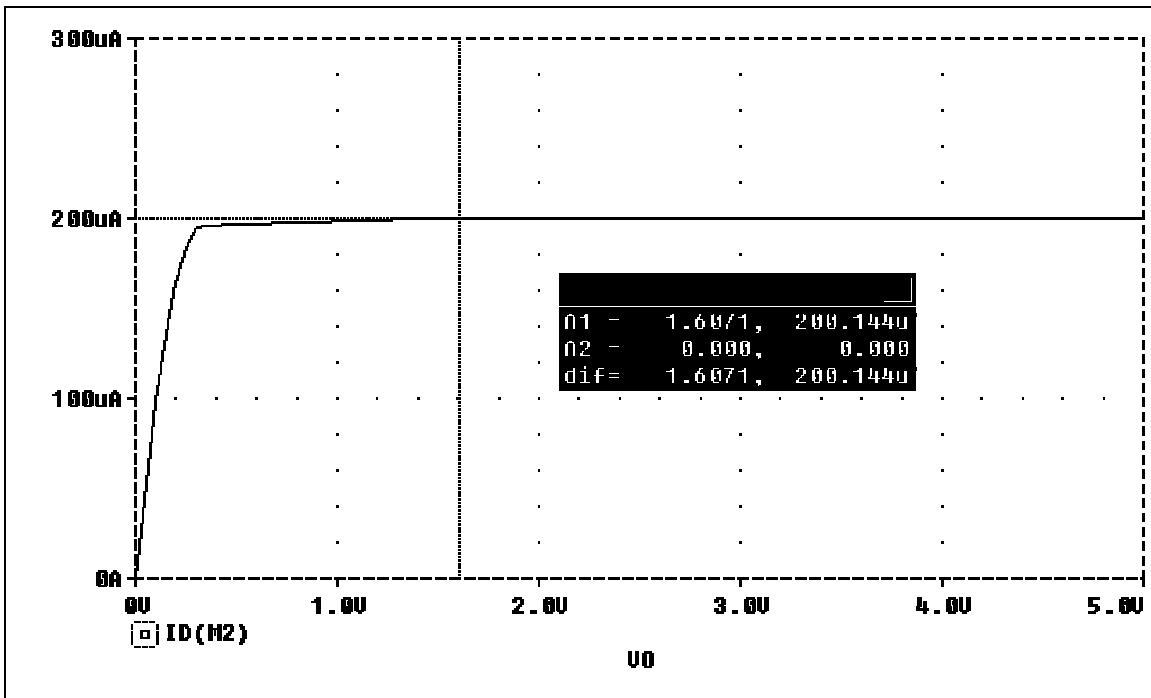
NODE VOLTAGE:

( 1) 1.3004 ( 2) 2.5000 ( 3) 5.0000 ( 4) 0.0000  
( 5) 3.2030 ( 6) 1.2989

\*\*\* SMALL-SIGNAL CHARACTERISTICS

V(2)/VO = 1.000E+00

OUTPUT RESISTANCE AT VO = 1.195E+08



## Wide-Swing Cascode Current Mirror

The analysis in Figure 11 assumed that the effect of the bulk to source is negligible. That is, all the transistor have the same voltage of  $V_{TO}$ . The threshold voltage of M2/M4 will be calculated, based on the knowledge that the source of M2 is at a potential of  $\Delta V$ , when M1 is at saturation, and the bulk is at  $V_{SS}=0$ . That is,  $V_{BS2}=V_{BS4}=-\Delta V=0.3$ . The threshold is given by:

$$V_{T2} = V_{TO} + \gamma(\sqrt{\phi - V_{BS}} - \sqrt{\phi}) = 1 + 1(\sqrt{0.6 - (-0.3)} - \sqrt{0.6}) = 1.174$$

$$V_{G2} = V_{T2} + 2\Delta V = 1.174 + 2(0.6) = 1.774$$

The calculated threshold voltage is 17% more than  $V_{TO}$ . Its effect can not be ignored. In fact transistor M5 can no longer be used to generate the required voltage of  $V_{G2}$ , because the threshold voltage of M5 is  $V_{TO}$ . Its gate to source voltage can only generate  $V_{TO}+2\Delta V=1.6$ , which is less than 1.774. That is, the required W/L of M5 to generate 1.774 is computed using the simple voltage reference formula with constant bias current  $I_B=200\mu A$ .

$$V_{R1} = \sqrt{\frac{2I}{\beta}} + V_{TO} = \sqrt{\frac{2I}{K(W/L)}} + V_{TO}$$

$$W/L = \frac{2I}{K(V_{R1} - V_{TO})^2} = \frac{2(200E - 6)}{(40E - 6)(1.774 - 1)^2} = 16.69$$

Selecting  $L=1.2\mu$ , results in  $W=16.69(1.2-1)=3.338\mu$ . This is less than the minimum width of  $6\lambda=6(0.6)=3.6\mu$ . Let  $L=2.4\mu$ , then  $W=16.69(2.4-1)=23.37\mu$ . That is, the ratio  $(W/L)_1/(W/L)_5 = (21.6/(1.2-1))/16.69=6.47$  rather than 4 (for  $n=1$ ) as shown in the analysis in Figure 11. The realized voltage using M5 at node 5 is 1.7607 rather 1.774. The wide-swing cascode current mirror is simulated using voltage source to supply the required gate voltage of 1.774 and using M5 to generate it with  $(W/L)/6.47$  rather than  $(W/L)/4$  used in the ideal analysis. The transfer characteristic is practically the same for both simulations.

```
* Pspice file for 200uA Current Source
* Filename="c200fgl1.cir"
VDD 3 0 DC 5VOLT
VSS 4 0 DC 0VOLT
VO 2 4 DC 1.5VOLT
VG2 5 0 DC 1.774VOLT
IR 3 1 DC 200UA
M1 6 1 4 4 MN W=21.6U L=1.2U
M2 2 5 6 6 MN W=21.6U L=1.2U
M3 7 1 4 4 MN W=21.6U L=1.2U
M4 1 5 7 4 MN W=21.6U L=1.2U
```

```

.MODEL MN NMOS VTO=1.0 KP=40U
+ GAMMA=1.0 LAMBDA=0.02 PHI=0.6
+ TOX=0.05U LD=0.5U CJ=5E-4 CJSW=10E-10
+ U0=550 MJ=0.5 MJSW=0.5 CGSO=0.4E-9 CGDO=0.4E-9
.MODEL MP PMOS VTO=-1.0 KP=15U
+ GAMMA=0.6 LAMBDA=0.02 PHI=0.6
+ TOX=0.05U LD=0.5U CJ=5E-4 CJSW=10E-10
+ U0=200 MJ=0.5 MJSW=0.5 CGSO=0.4E-9 CGDO=0.4E-9
.DC VO 0 5.0 0.05
.TF V(2) VO
.PROBE
.END

```

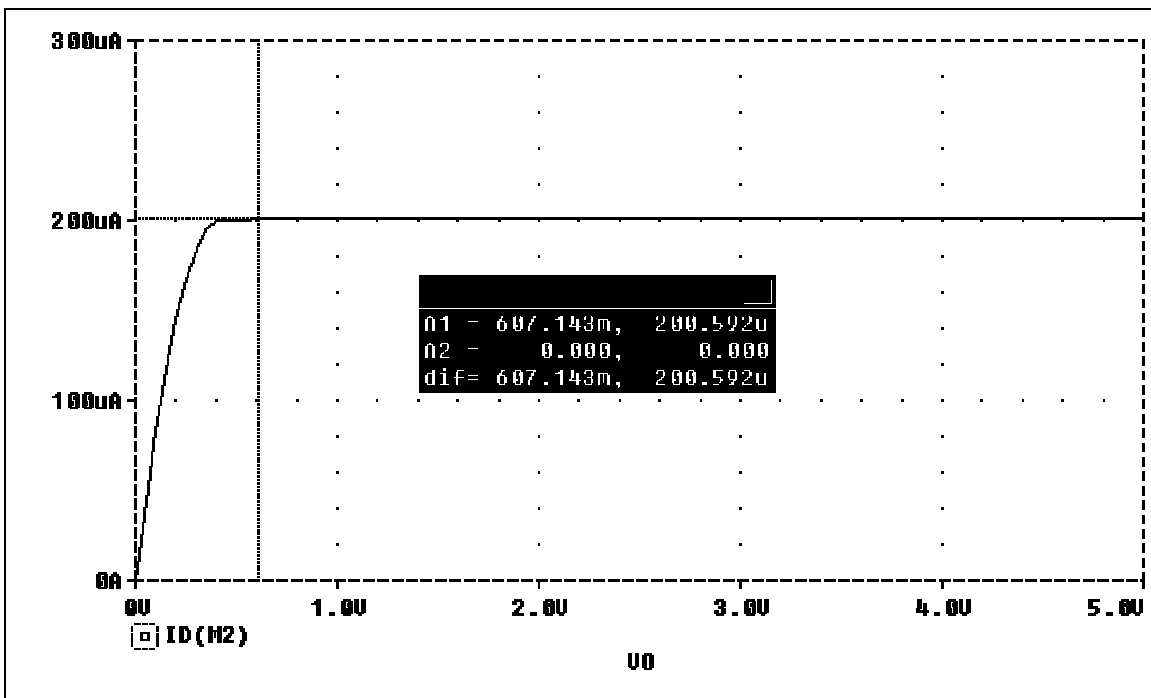
**Node 5 is generated using a voltage source.**

NODE VOLTAGE:

( 1) 1.3034 ( 2) 1.5000 ( 3) 5.0000 ( 4) 0.0000  
( 5) 1.7740 ( 6) .4722 ( 7) .2991

\*\*\*\* SMALL-SIGNAL CHARACTERISTICS

OUTPUT RESISTANCE AT VO = 8.554E+07



**Node 5 is generated by transistor M5.**

NODE VOLTAGE:

( 1) 1.3037 ( 2) 1.5000 ( 3) 5.0000 ( 4) 0.0000

( 5) 1.7607 ( 6) .4587 ( 7) .2904