Improved Cascode Current Mirror

The ‘classic’ cascode current sink is shown in Figure 1.

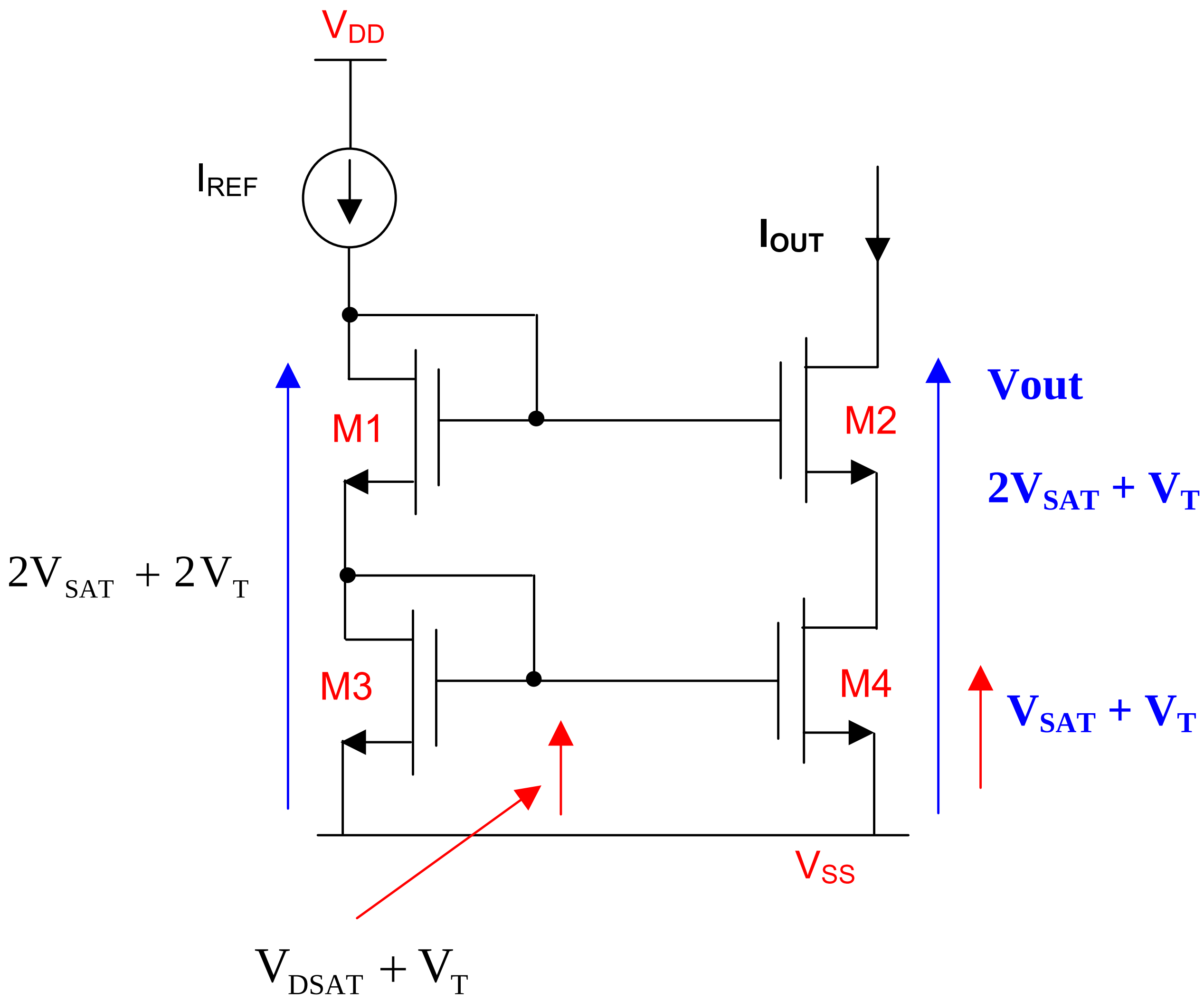


Figure 1 Cascode current source, showing that the minimum voltage output is $2V_{SAT}+V_T$ above the rail VSS (in this case 0V). M1 and M3 are wired as diodes and each have a voltage drop of $V_{SAT}+V_T$ across the drain-source junction.

M1 & M2 are effectively two diodes in series with a total voltage drop of $2V_{SAT}+2V_T$, which is fairly independent of current I_{REF}. I_{REF} can be set using a resistor or band-gap/resistor network. As we have seen the voltage on the drain of M2 is:

The diode voltage is always $V_{SAT} + V_T$

M1 gate voltage $= 2V_{SAT} + 2V_T$

Drain voltage on M2 $= V_G - V_T$ sub in $2V_{SAT} + 2V_T$ for VG

$$= (2V_{SAT} + 2V_T) - V_T = 2V_{SAT} + V_T$$

It is possible to remove the VT (which is typically ~ 0.7 – 1V) by the use of the modified cascode current sink shown in **Figure 2**.

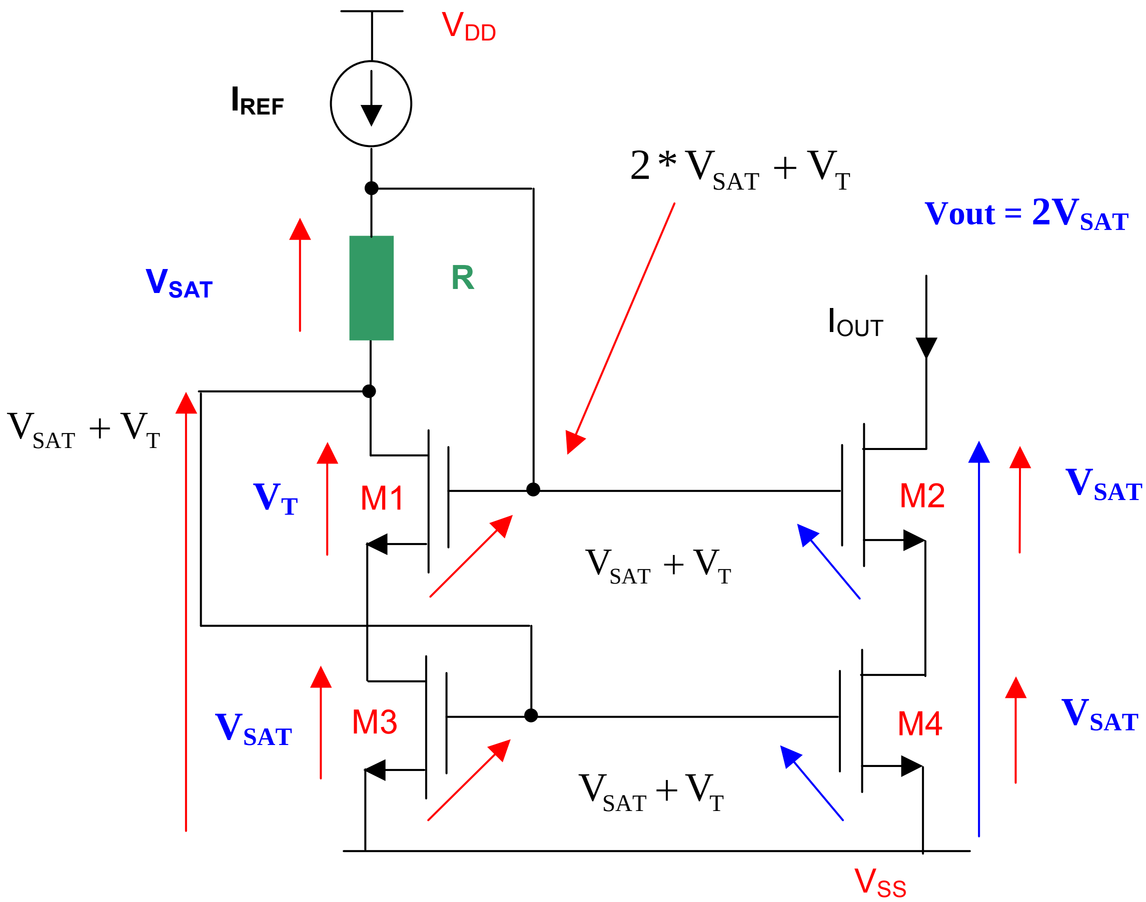


Figure 2 Modified cascode current sink to reduce the voltage drop across the two output FET's of M2 & M4.

To calculate the value of the resistor we decide on the minimum output voltage we require, for example 0.6V, this will now set V_{SAT} to 0.3V, on M2 & M4 and decide on the current required say 100uA.

Now we can calculate $V_T + V_{SAT}$

$$V_{DS} = \sqrt{\frac{2.I_{ref}}{\beta}} + V_T = V_{SAT} + V_T$$

$$V_{SAT} = \sqrt{\frac{2.I_{ref}}{\beta}} \quad V_{SAT}^{\ 2} = \frac{2.I_{ref}}{\beta}$$

$$\beta = \frac{K_N.W}{L} = \frac{2.I_{ref}}{V_{SAT}^{\ 2}} \quad \therefore \frac{W}{L} = \frac{2.I_{ref}}{K_N.V_{SAT}^{\ 2}}$$

Using the following device data K_N=110uA/V^2, V_T=0.7V, I_D set to 100uA.

Set VSAT to be 0.3V

$$\beta = \frac{K_N.W}{L} = \frac{2.I_{ref}}{V_{SAT}^{\ 2}} \quad \therefore \frac{W}{L} = \frac{2.I_{ref}}{K_N.V_{SAT}^{\ 2}}$$

$$\frac{W}{L} = \frac{2.100E^{-6}}{110E^{-6}.0.3^2} = 20.2$$

Gate voltage calculations

VG3 = V_{SAT}+V_T = 0.3+0.7 = **1V** and

VG4 = 2V_{SAT}+V_T = 2*0.3 +0.7 = **1.3V**

So the resistor R = V_{SAT}/Iref = 0.3/100E^{-6} = **3KΩ**

The ADS simulation setup for analysing this example is shown in Figure 3 with the resulting graph and tabulated data on Figure 4.

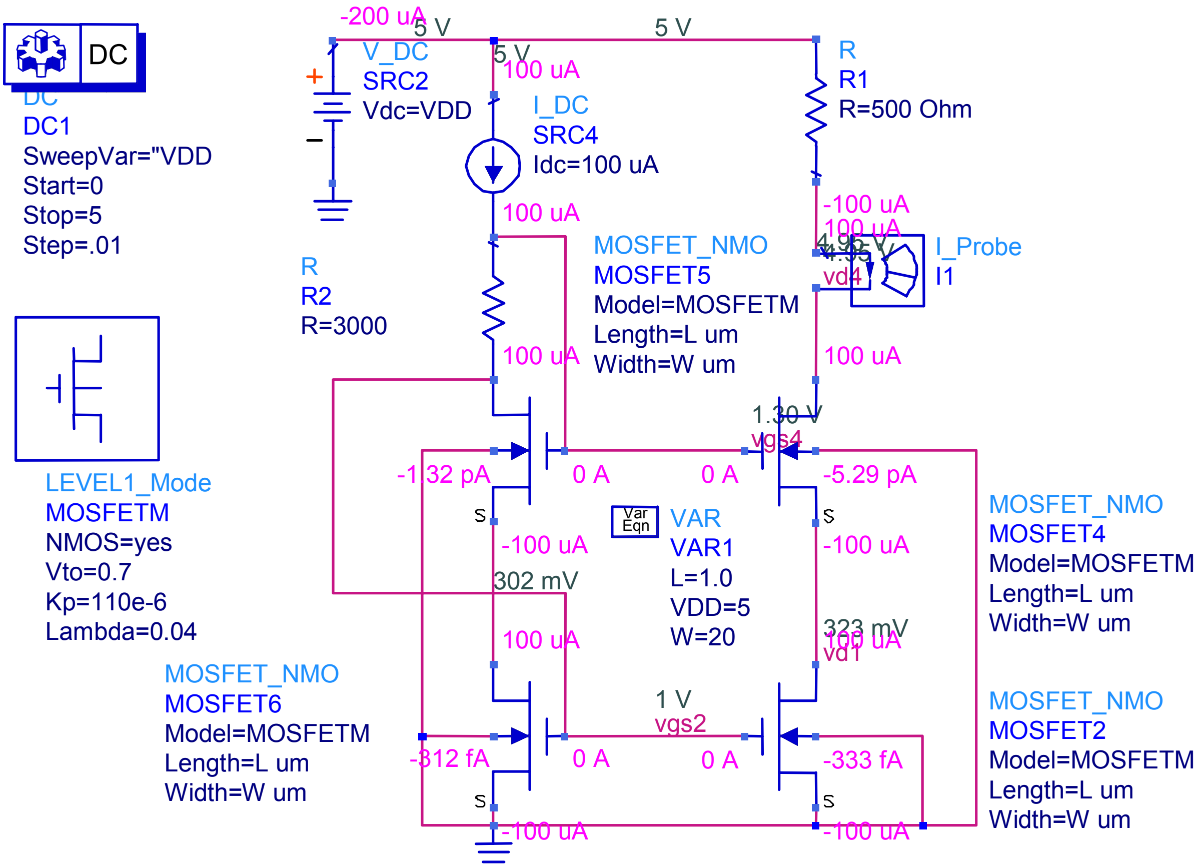
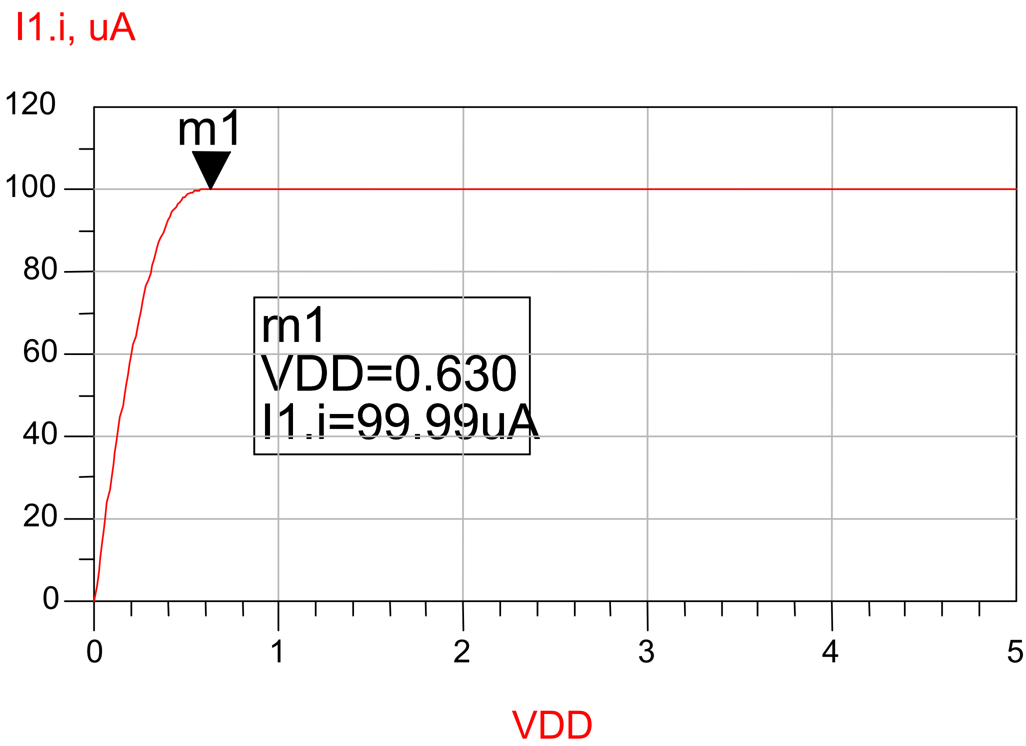


Figure 3 ADS Simulation for the self-biased high swing cascode current source.



vd1[70]	vd4[70]	vgs2[70]	vgs4[70]
0.300	0.650	1.000	1.300

Figure 4 Result of the ADS simulation of Figure 3. From the plot we can see that the minimum output voltage (for current regulation) is ~ 0.6V. The table shows the 70 data point (out of 500) where the output voltage is 0.65V the gate voltages agree with the hand calculations given earlier.

Similarly we can design a current sink in the same way.

Using the following device data K_P=50uA/V^2, V_T=0.7V, I_D set to 100uA.

Set VSAT to be 0.3V

$$\beta = \frac{K_N.W}{L} = \frac{2.I_{ref}}{V_{SAT}^{\,2}} \quad \therefore \quad \frac{W}{L} = \frac{2.I_{ref}}{K_N.V_{SAT}^{\,2}}$$

$$\frac{W}{L} = \frac{2.100E^{-6}}{50E^{-6}.0.3^2} = 44$$

Gate voltage calculations

$Vg1 = V_{SAT}+V_T = 0.3+0.7 = \mathbf{1V}$ and

$Vg2 = 2V_{SAT}+V_T = 2*0.3 + 0.7 = \mathbf{1.3V}$

So the resistor $R = V_{SAT}/Iref = 0.3/100E^{-6} = \mathbf{3K\Omega}$

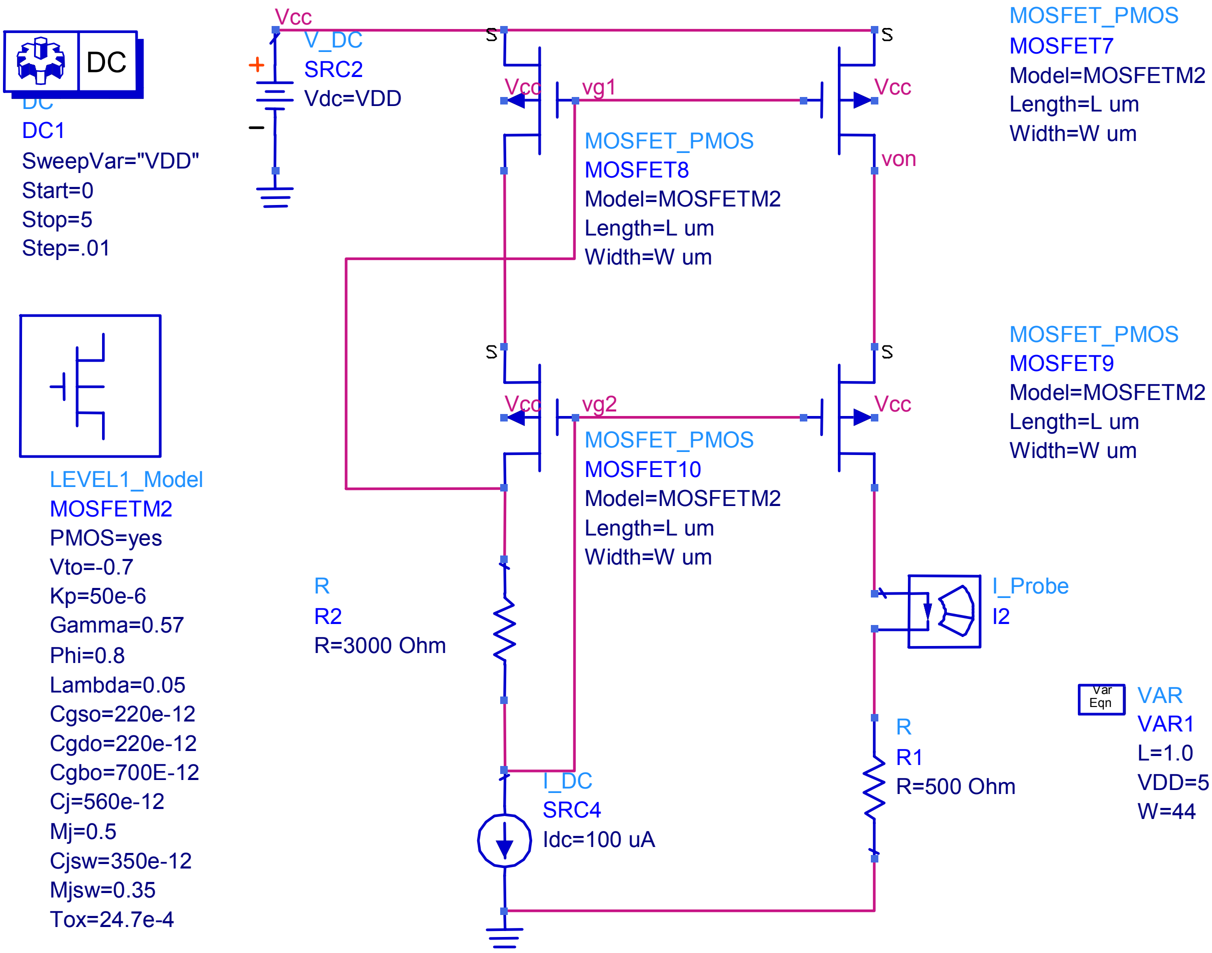
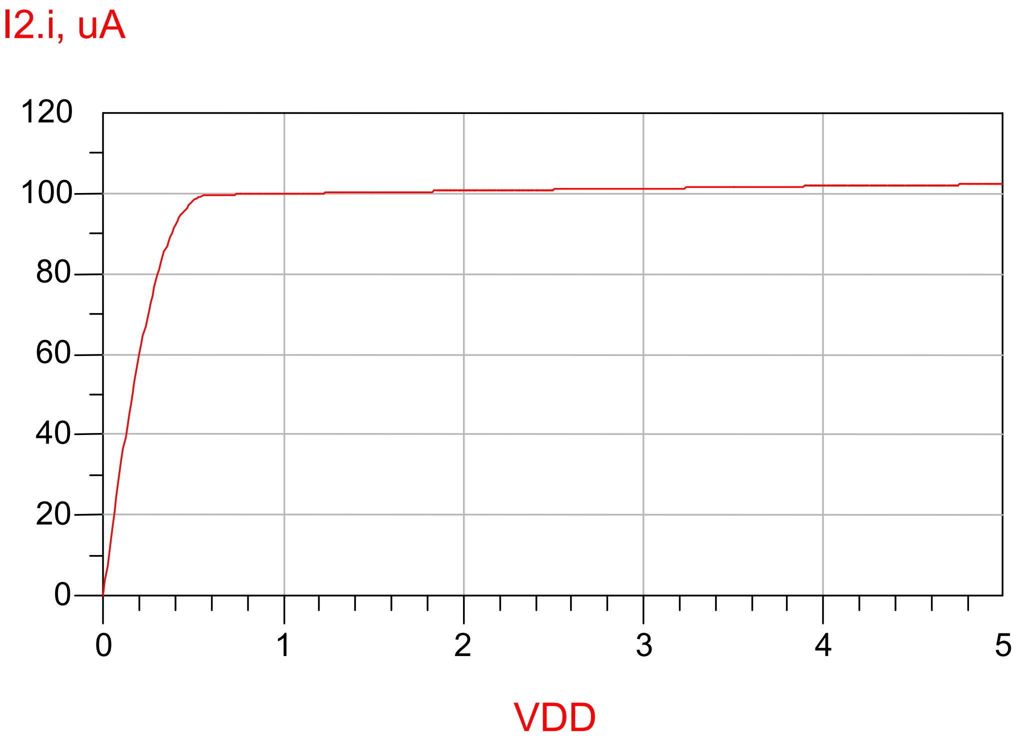


Figure 5 Self biased cascode high swing current sink circuit using P-MOS devices. Note that as this circuit is using P-type MOSFETS, VTO is set to –0.7V in the spice model parameter list MOSFETM2.



Eqn g1=Vcc[500]-vg1[500]

Eqn vsat=Vcc[500]-von[500]

Eqn g2=Vcc[500]-vg2[500]

g1	g2	vsat
1.007	1.307	0.257

Figure 6 Resulting plot and node voltages of the current sink shown in Figure 5. For this example the gate voltages are subtracted from VDD to make them referenced to VDD. The [500] signifies the 500 data point which will be the parameter sweep of VDD at 5V.