

EL326 CMOS OP-AMP

Report to : อ. อธิธิภูมิ บุญพิงค์ (3C)

อ. วรากร เกษมสุวรรณ(2R)

Requirement: 1. Objective

- 2. การทดลอง**
- 3. ผลการทดลอง(รวมกราฟ)**
- 4. วิเคราะห์ผลการทดลอง**
- 5. สรุปผลการทดลอง**
- 6. ตอบคำถามท้ายบททุกข้อ**

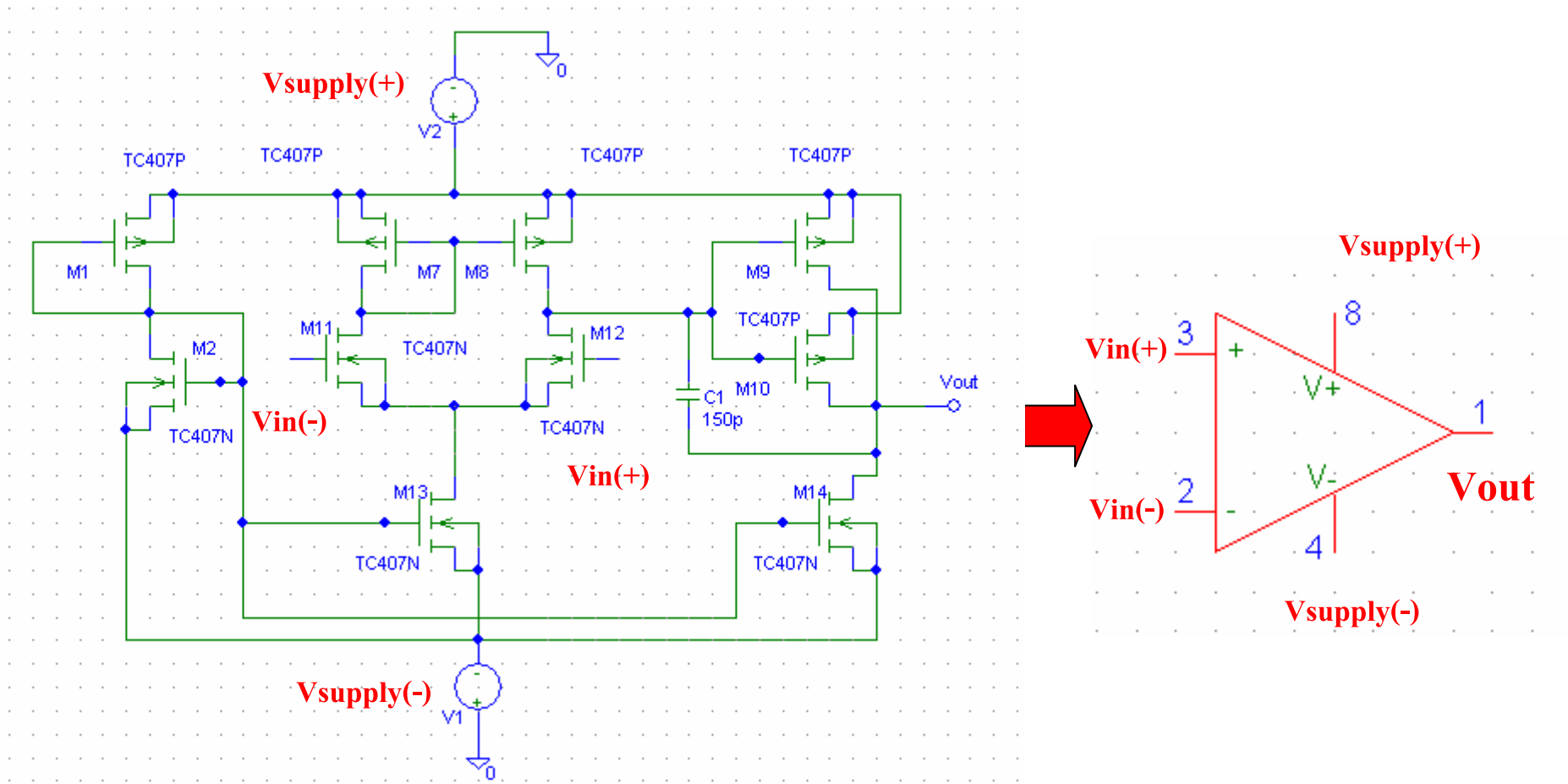


Fig. CMOS OP-Amp Circuit

Working steps

Create Library สร้าง **Library** สำหรับ **NMOS** และ **PMOS**



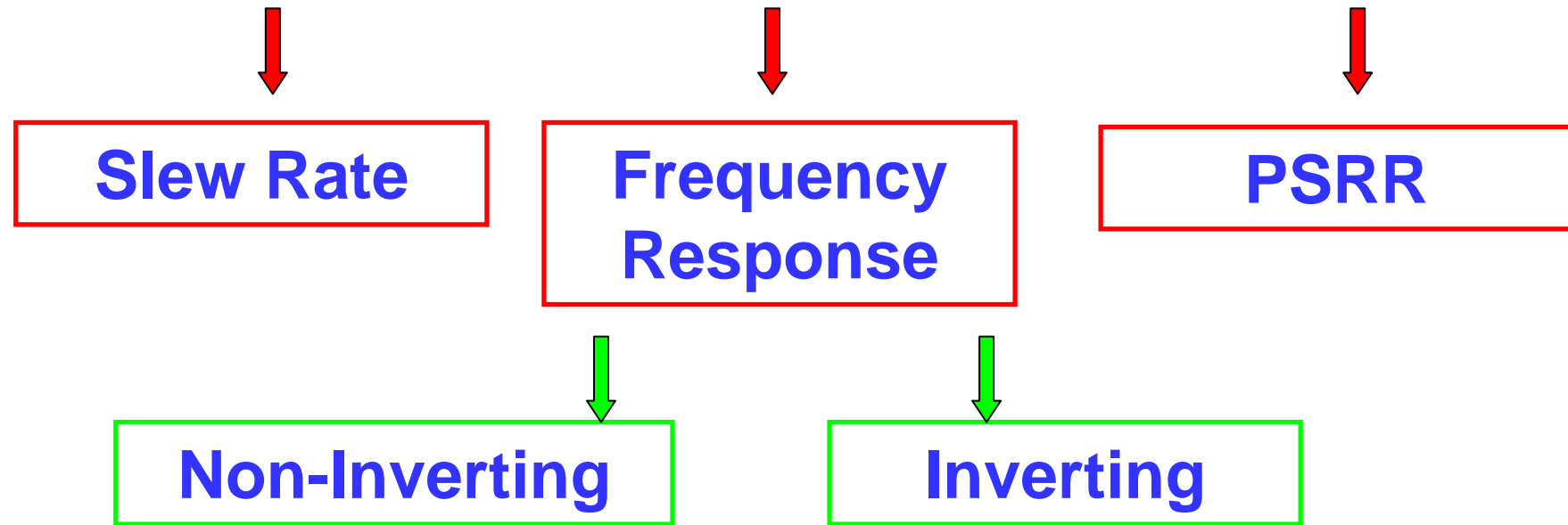
เพิ่ม **NMOS** และ **PMOS** ไว้ใน **Library** ของ **PSPICE**



วาดรูปวงจร เพื่อสร้าง **Op-Amp**

วาดรูปวงจร ทดสอบ **Op-Amp**

วาดรูปวงจร ทดสอบ Op-Amp



Note: PSRR: Power Supply Rejection Ratio

Create Library สร้าง **Library** สำหรับ **NMOS** และ **PMOS**

```
cmos.lib - Notepad
File Edit Format View Help

.model TC407N NMOS(LEVEL=3 LD=1.2U VTO=0.7 KP=1.73E-5 GAMMA=1.0
+ TOX=1.0E-7 TPG=0 NSUB=5E15 L=8U
+ W=290U WD=1.4U RD=2.0 RS=2.0 RG=2.0
+ CGSO=4.14E-10 CGDO=4.14E-10 CGBO=1.61E-10 TT=100n)
* CMOS IC(TC4007 UBP) CMOS LOCCOS 8U PROCESS

.model TC407P PMOS(LEVEL=3 LD=1.2U VTO=-0.6 KP=0.69E-5 GAMMA=0.9
+ TOX=1.0E-7 TPG=0 NSUB=2E15 L=8U
+ W=480U WD=1.4U RD=2.0 RS=2.0 RG=2.0
+ CGSO=4.14E-10 CGDO=4.14E-10 CGBO=1.61E-10 TT=80n)
* CMOS IC(TC4007 UBP) CMOS LOCCOS 8U PROCESS
```

Fig. Library File for NMOS and PMOS

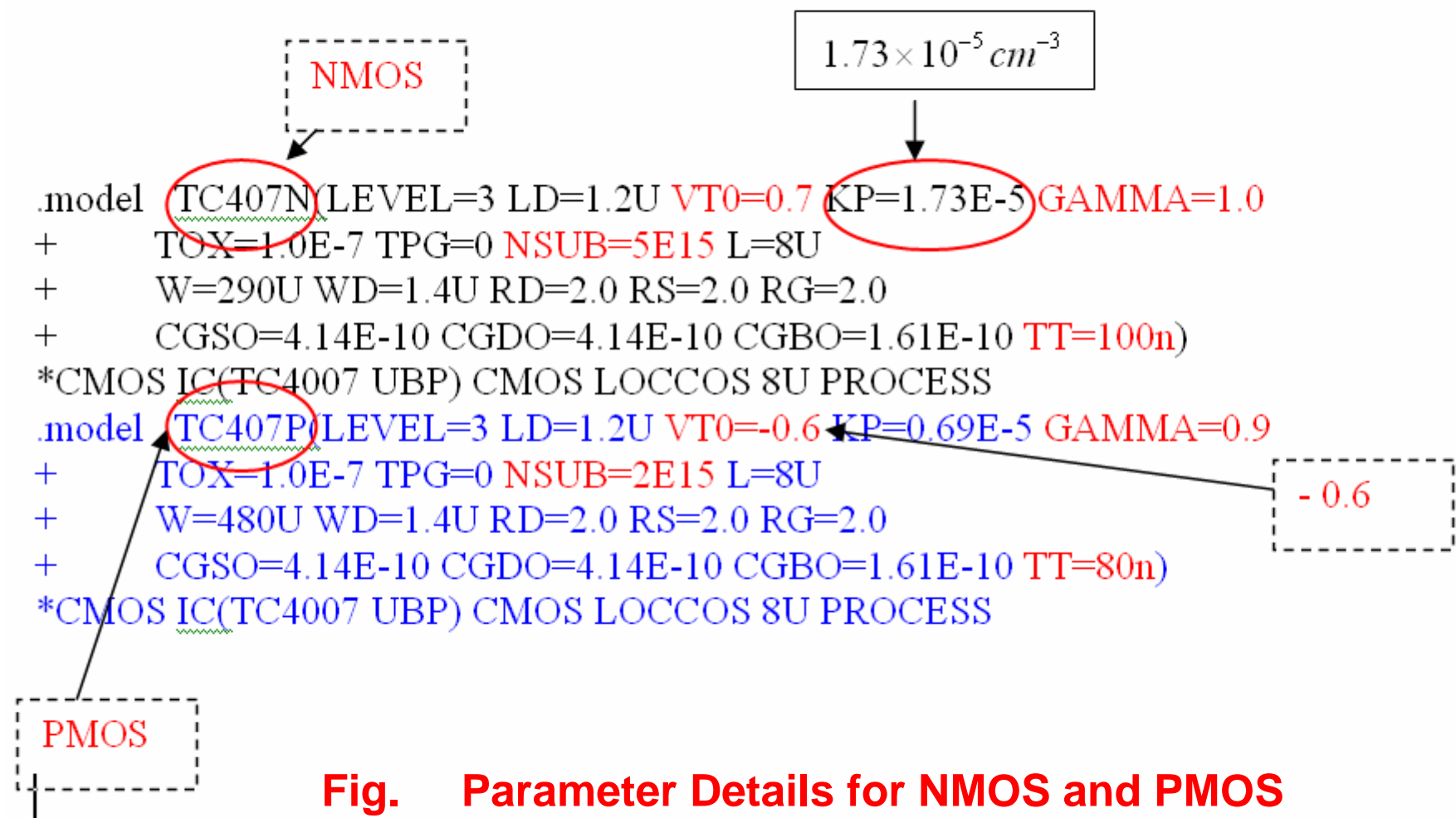
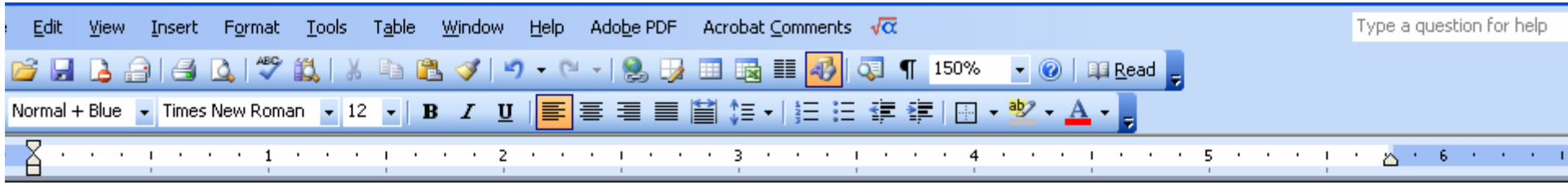
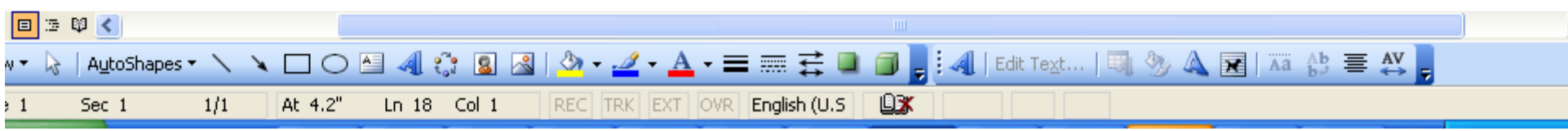


Fig. Parameter Details for NMOS and PMOS



เพิ่ม **NMOS** และ **PMOS** ไว้ใน **Library** ของ **PSPICE**

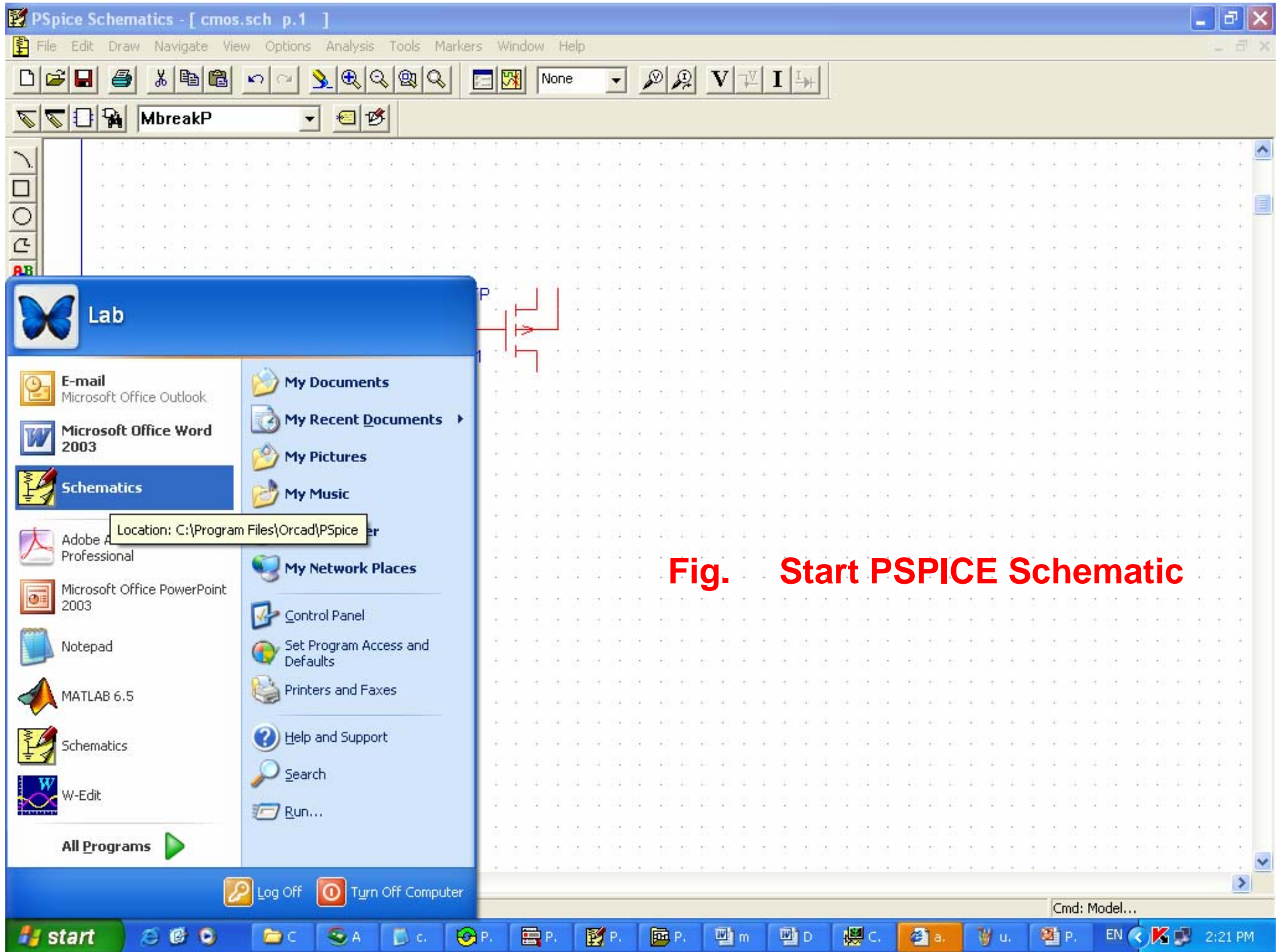


Fig. Start PSPICE Schematic

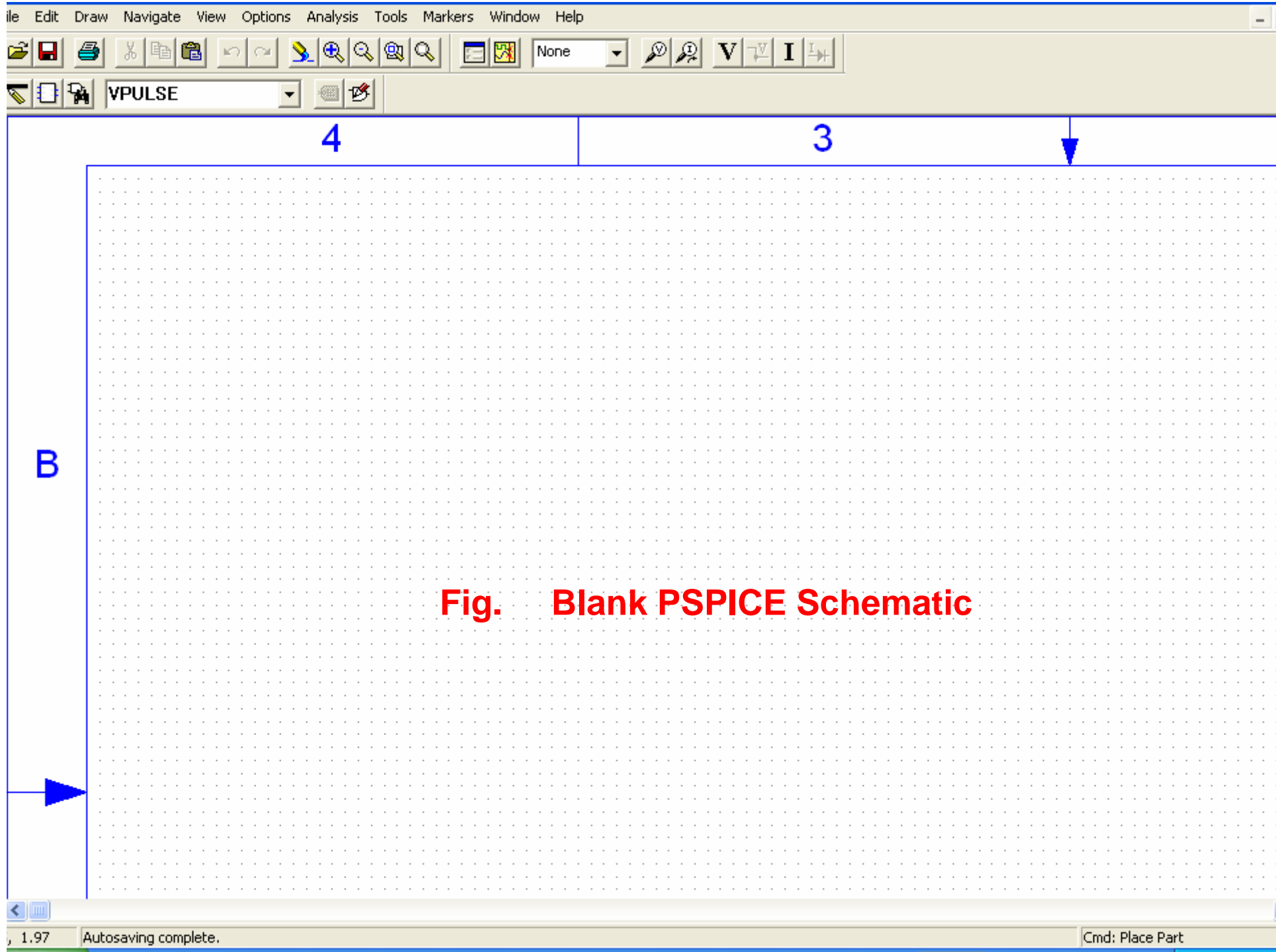


Fig. Blank PSPICE Schematic

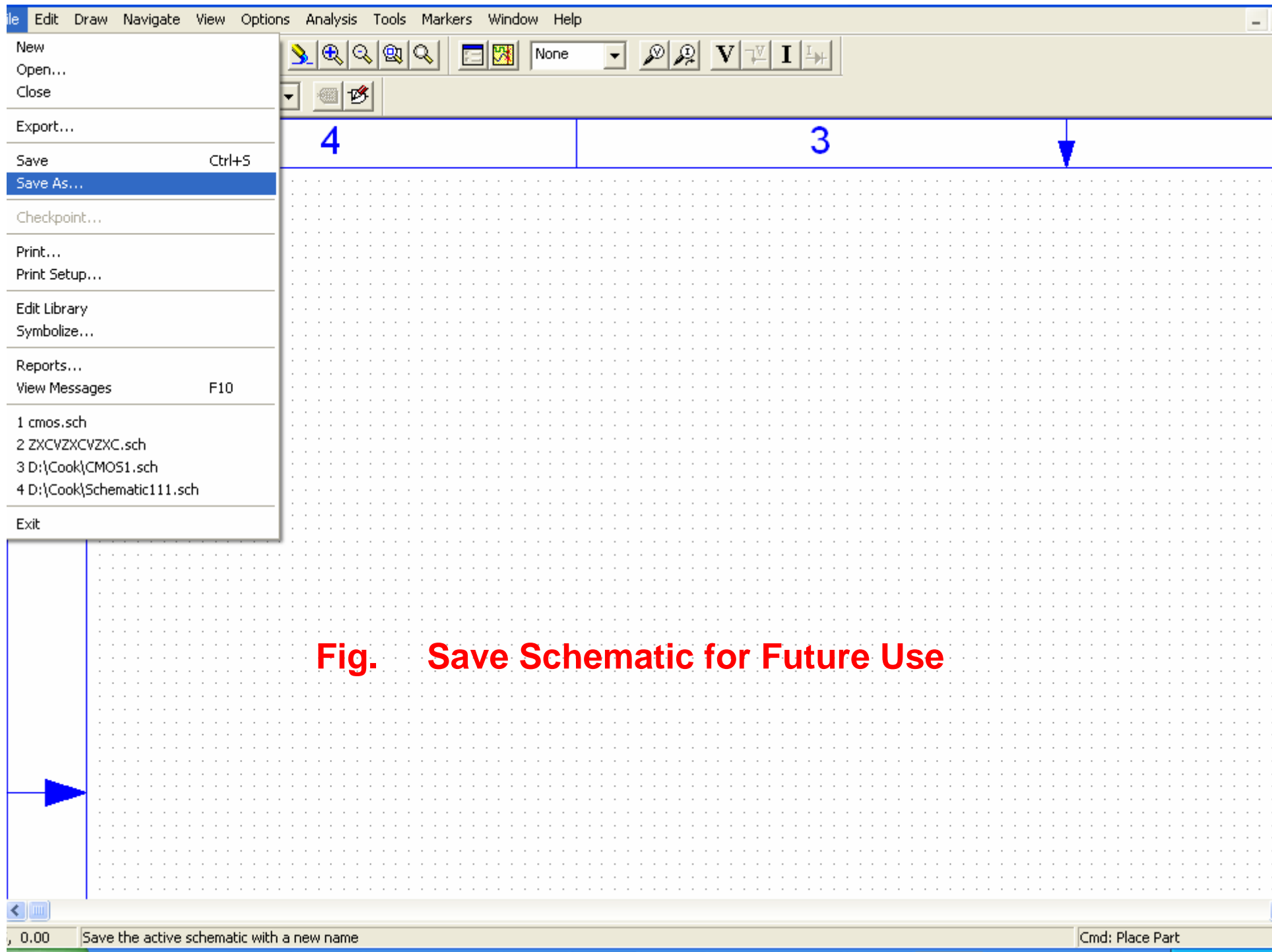


Fig. Save Schematic for Future Use

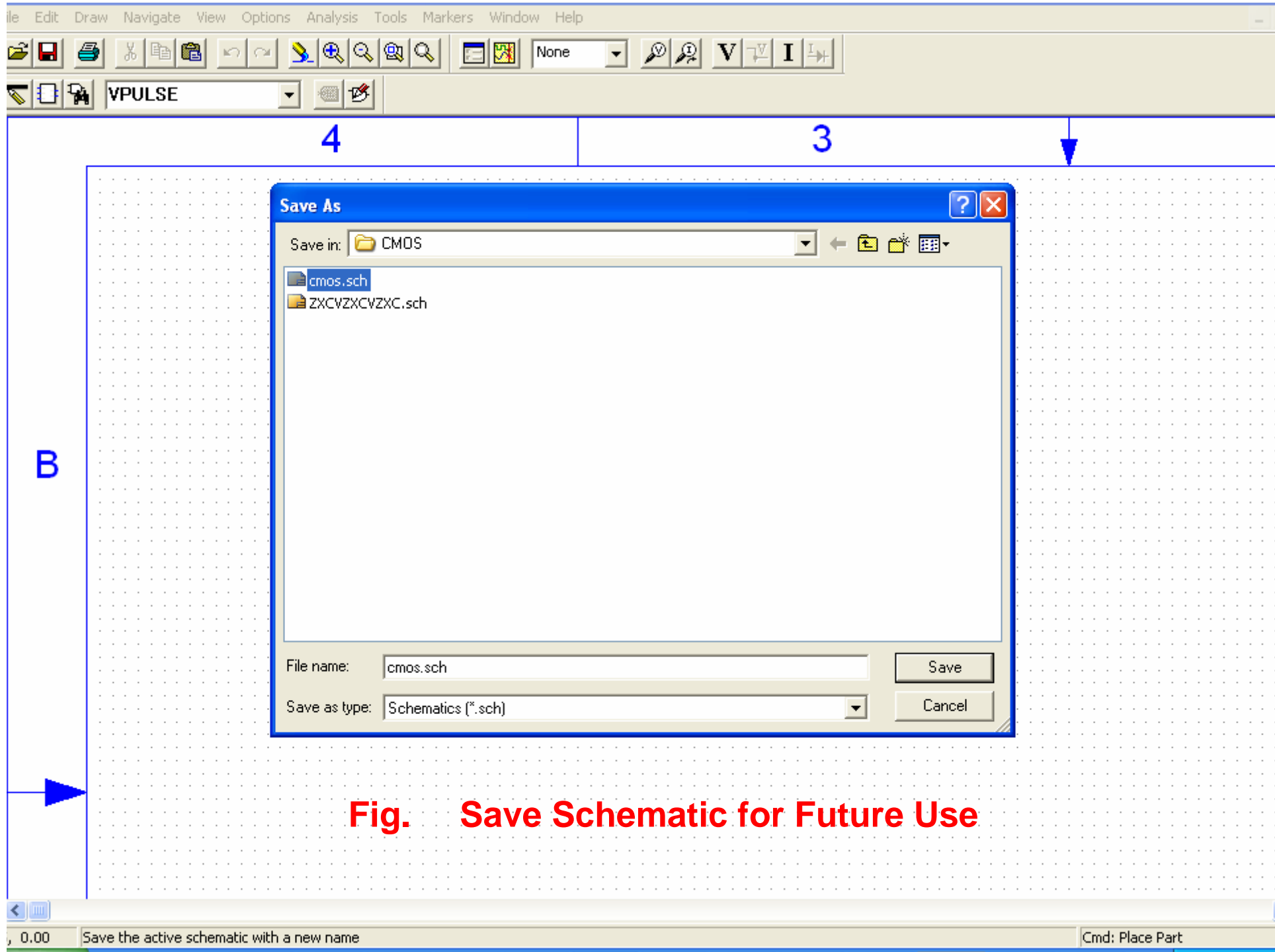


Fig. Save Schematic for Future Use

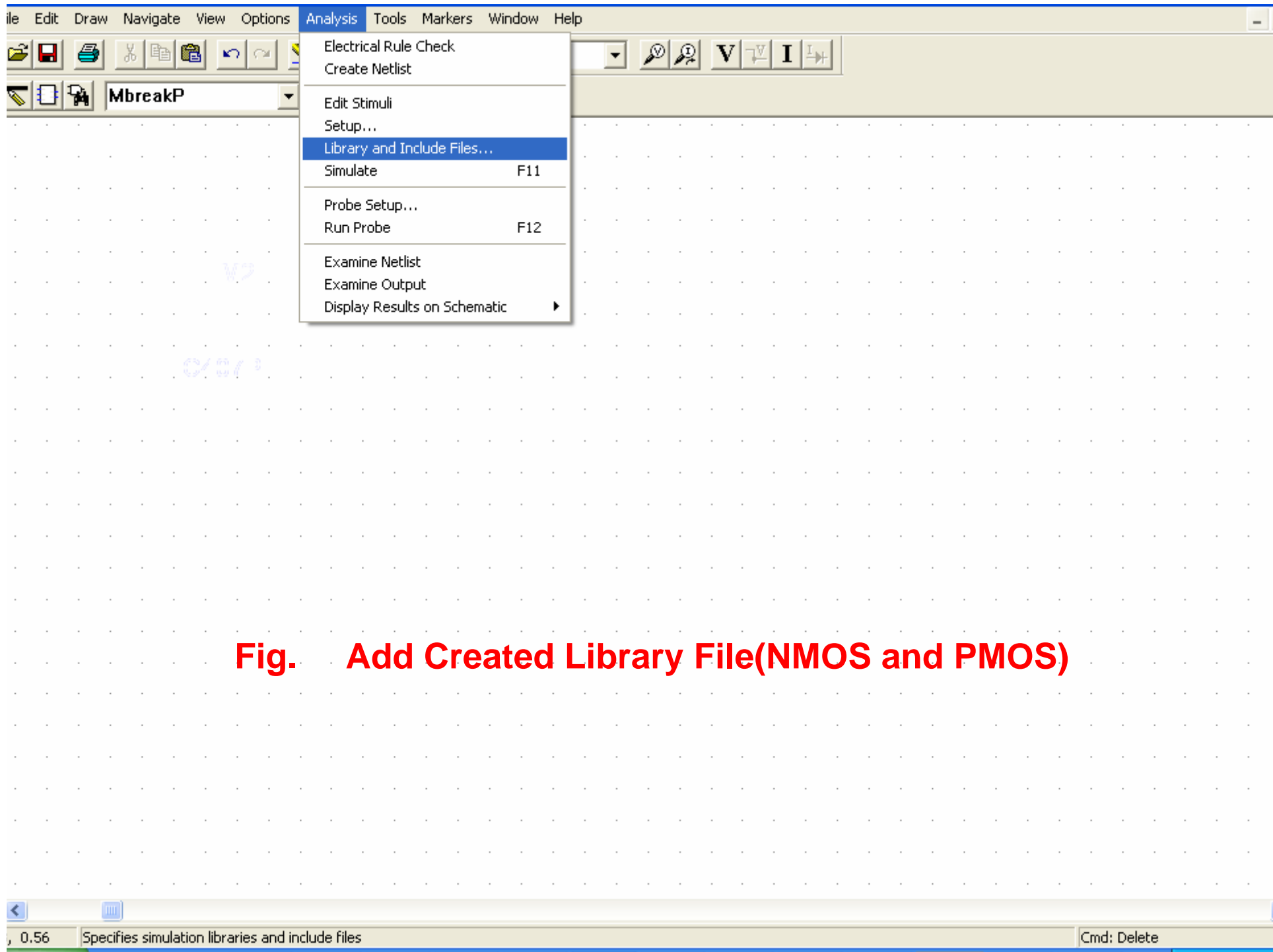


Fig. Add Created Library File(NMOS and PMOS)

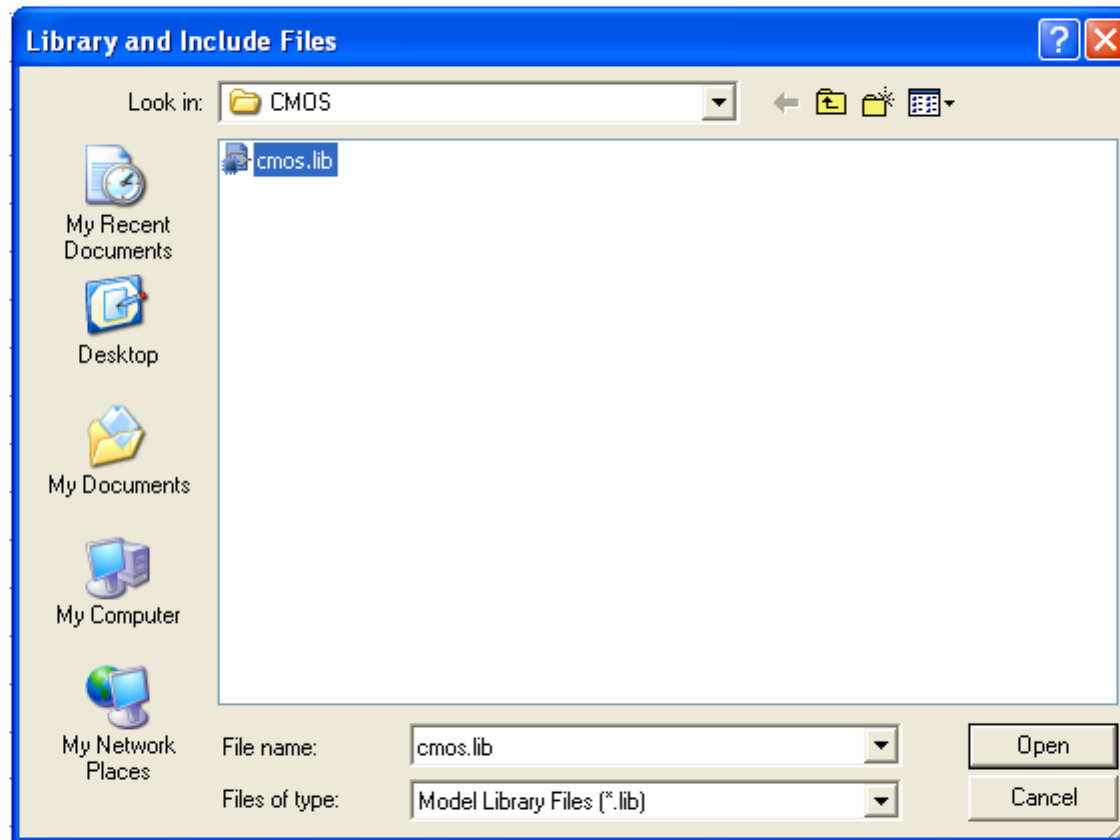
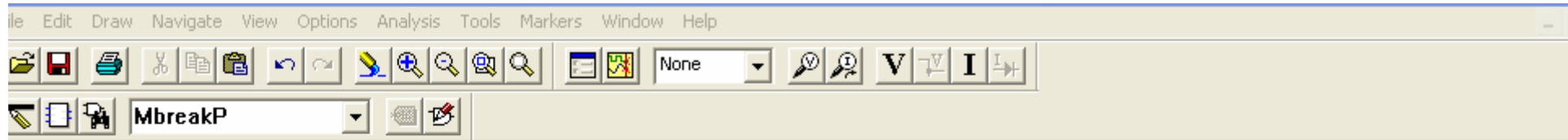
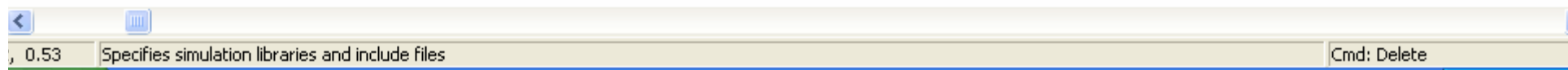


Fig. Add cmos.lib file to PSPICE



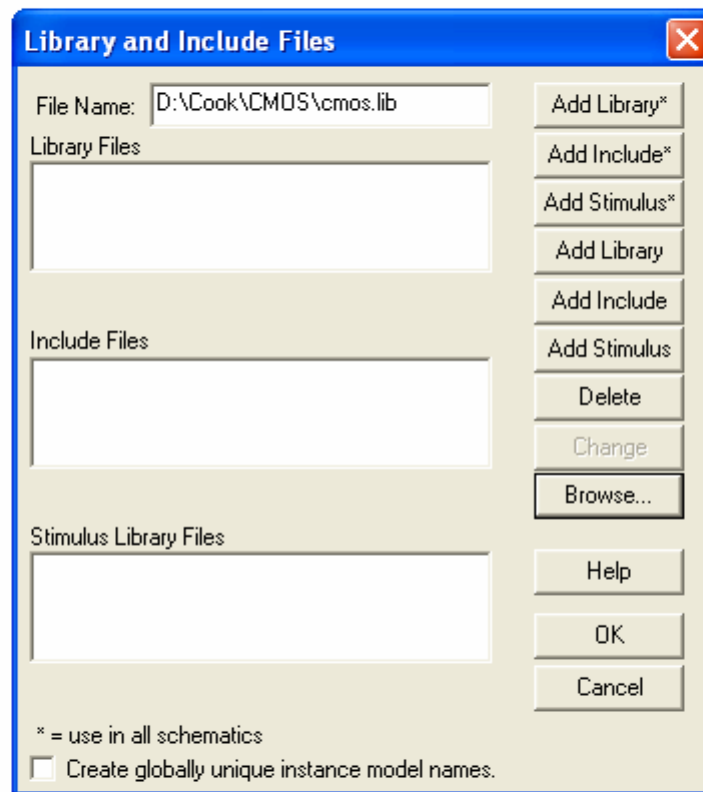
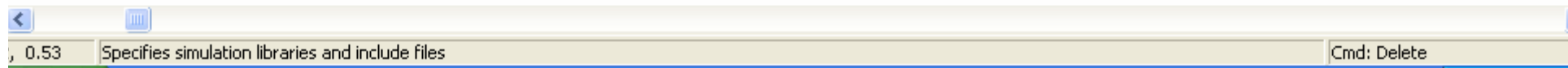


Fig. Add cmos.lib file to PSPICE



วาดรูปวงจร เพื่อสร้าง **Op-Amp**

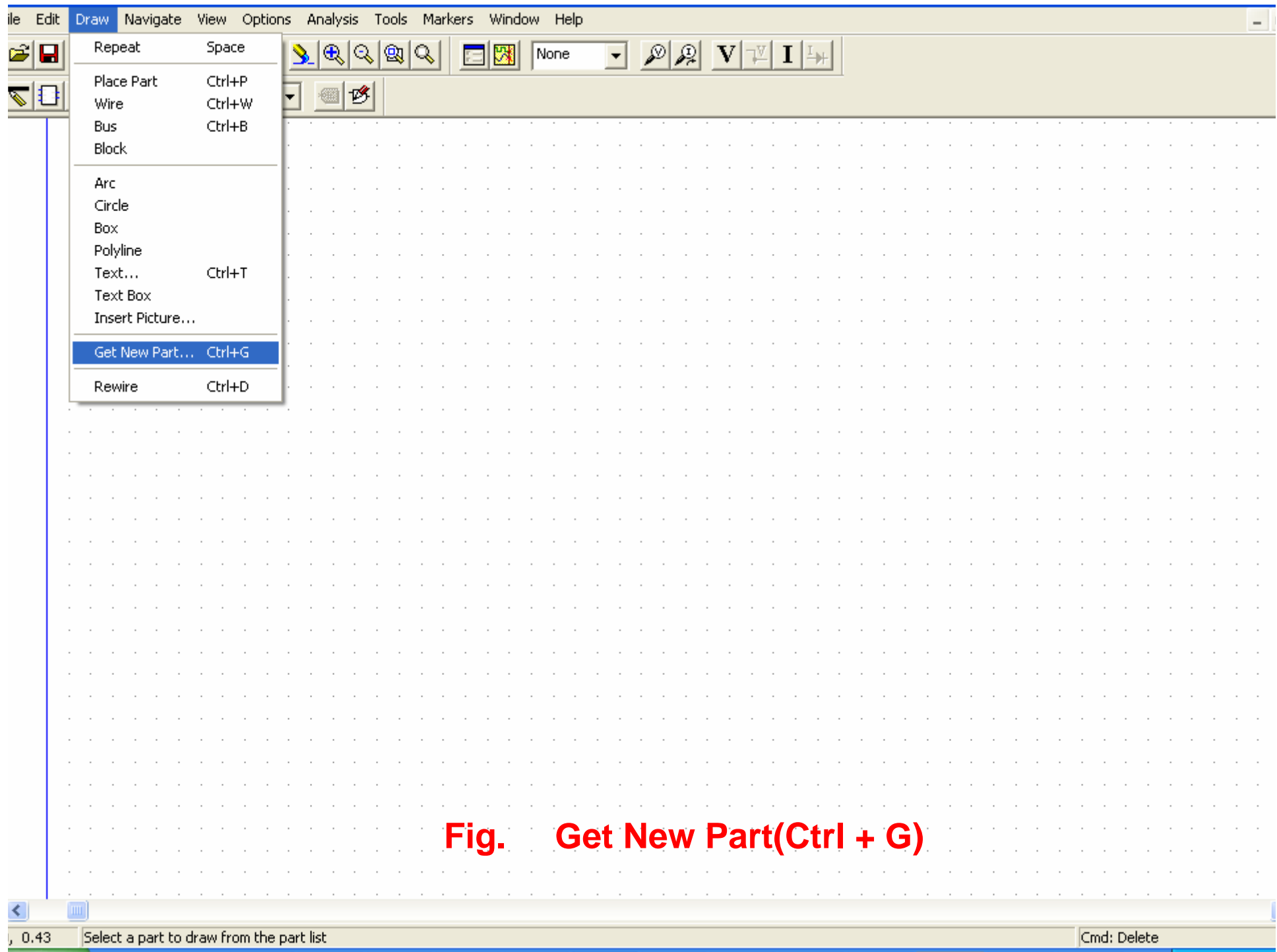


Fig. Get New Part(Ctrl + G)

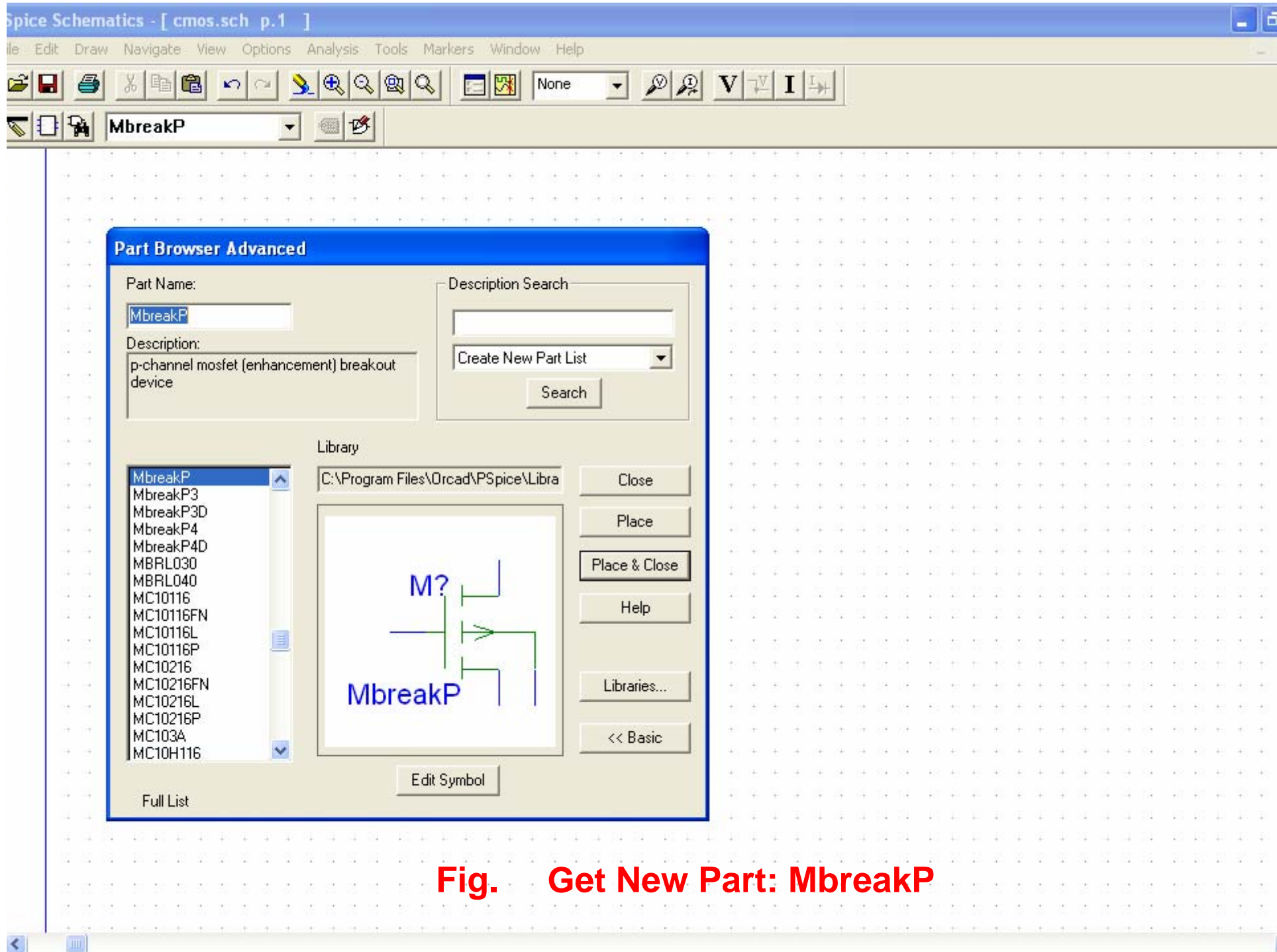


Fig. Get New Part: MbreakP

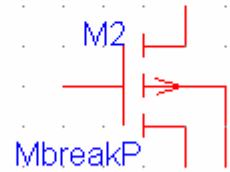
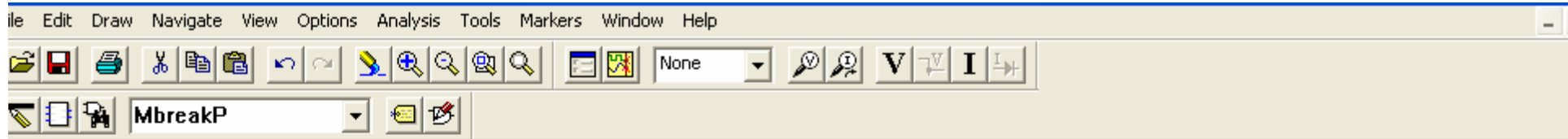
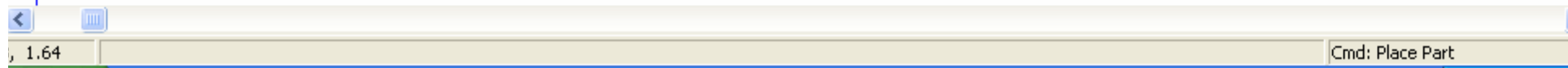


Fig. Part MbreakP for Circuit Drawing



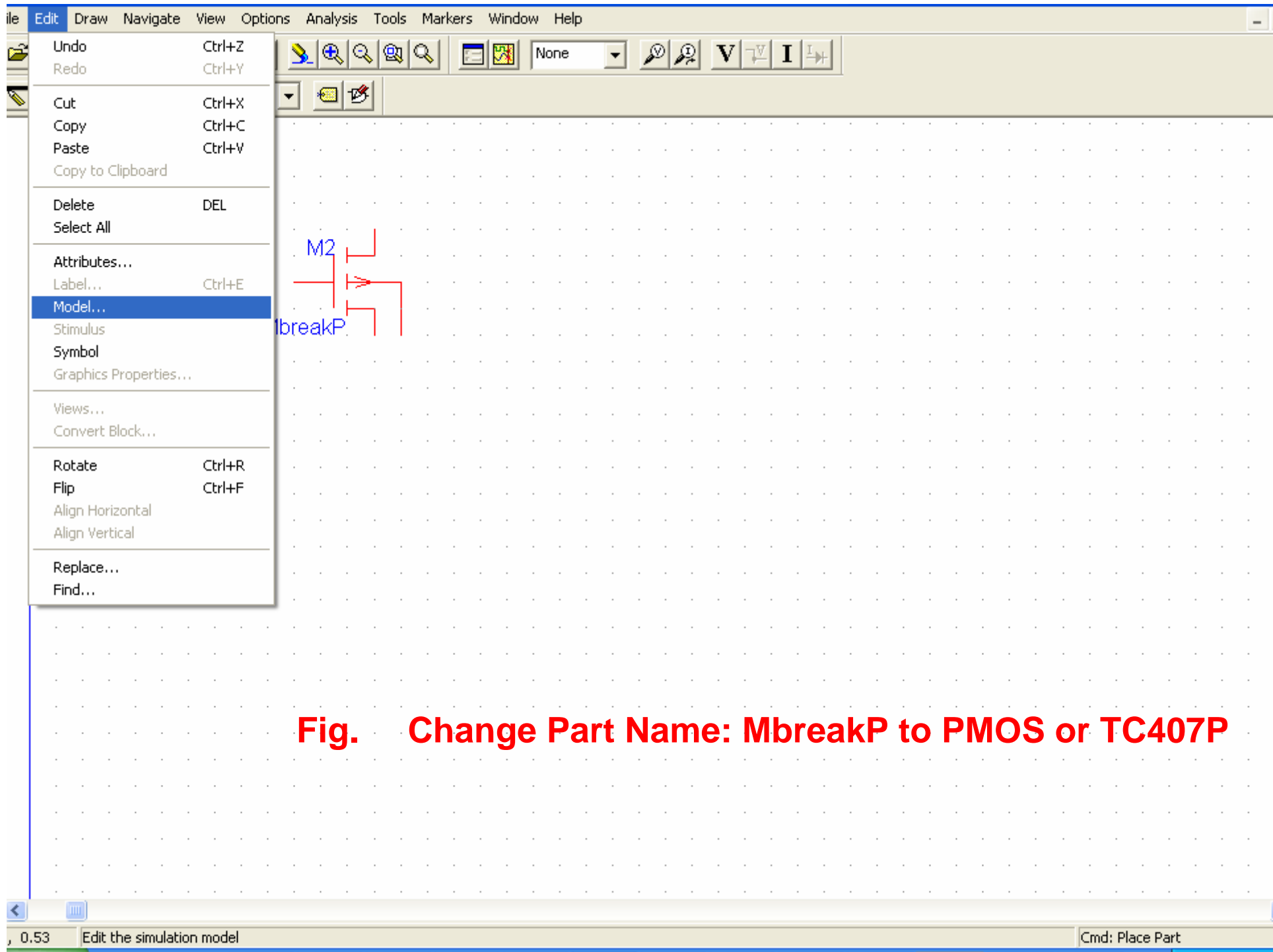


Fig. Change Part Name: MbreakP to PMOS or TC407P

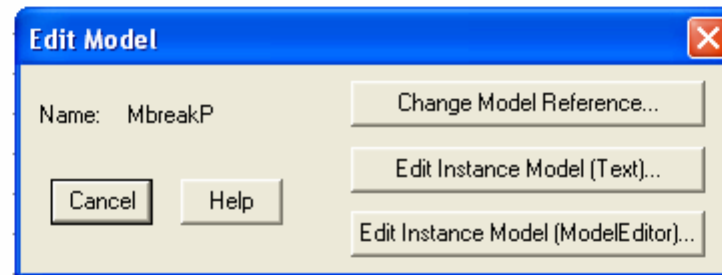
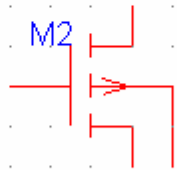
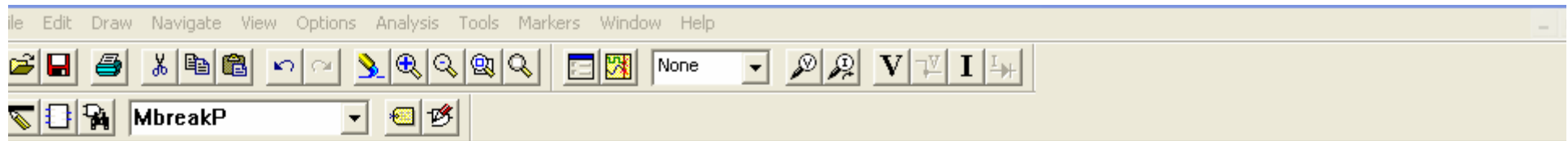
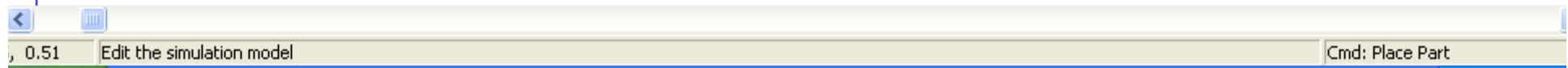
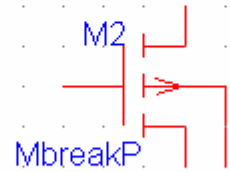
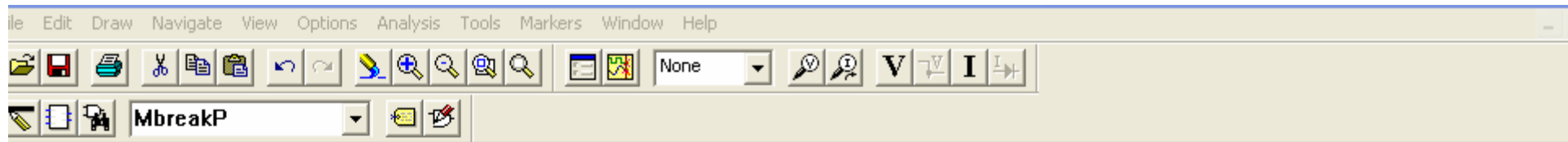


Fig. Change Part Name: MbreakP to PMOS or TC407P





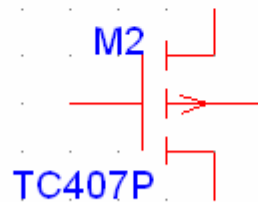
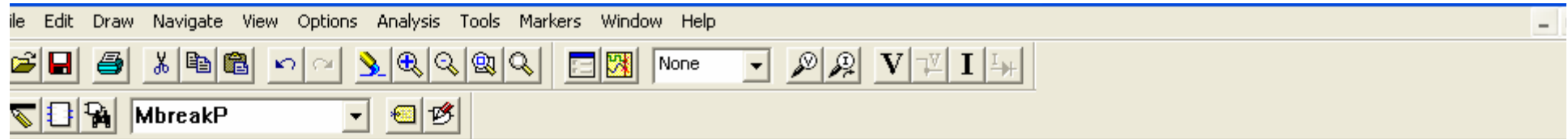
Enter New Model Name: ✕

Model Name

TC407P

OK Cancel

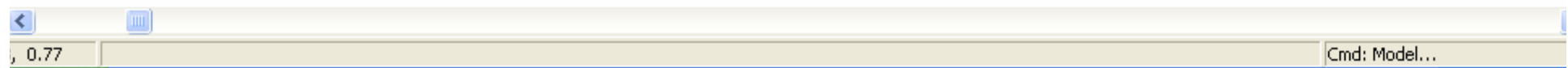
Fig. Change Part Name: MbreakP to PMOS or TC407P



```
cmos.lib - Notepad
File Edit Format View Help
.model TC407N(LEVEL=3 LD=1.2U VT0=0.7 KP=1.73E-5 GAMMA=1.0
+ TOX=1.0E-7 TPG=0 NSUB=5E15 L=8U
+ W=290U WD=1.4U RD=2.0 RS=2.0 RG=2.0
+ CGSO=4.14E-10 CGDO=4.14E-10 CGBO=1.61E-10 TT=100n)
*CMOS IC(TC4007 UBP) CMOS LOCCOS 8U PROCESS

.model TC407P(LEVEL=3 LD=1.2U VT0=-0.6 KP=0.69E-5 GAMMA=0.9
+ TOX=1.0E-7 TPG=0 NSUB=2E15 L=8U
+ W=480U WD=1.4U RD=2.0 RS=2.0 RG=2.0
+ CGSO=4.14E-10 CGDO=4.14E-10 CGBO=1.61E-10 TT=80n)
*CMOS IC(TC4007 UBP) CMOS LOCCOS 8U PROCESS]
```

Fig. Part Name TC407P or PMOS for Op-Amp Circuit Drawing





Part Browser Advanced

Part Name: MbreakN

Description: n-channel mosfet (enhancement) breakout device

Description Search: Create New Part List

Search

Library: C:\Program Files\Orcad\PSpice\Libra

- MbreakN
- MbreakN3
- MbreakN3D
- MbreakN4
- MbreakN4D
- MbreakP
- MbreakP3
- MbreakP3D
- MbreakP4
- MbreakP4D
- MBRL030
- MBRL040
- MC10116
- MC10116FN
- MC10116L
- MC10116P
- MC10216

Full List

M?

MbreakN

Edit Symbol

Close

Place

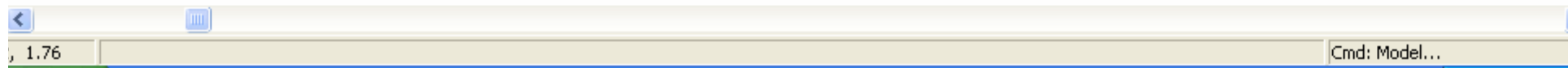
Place & Close

Help

Libraries...

<< Basic

Fig. Part MbreakN for Circuit Drawing



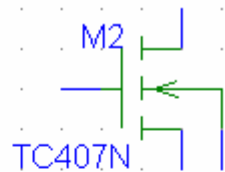
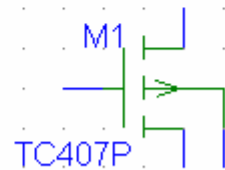
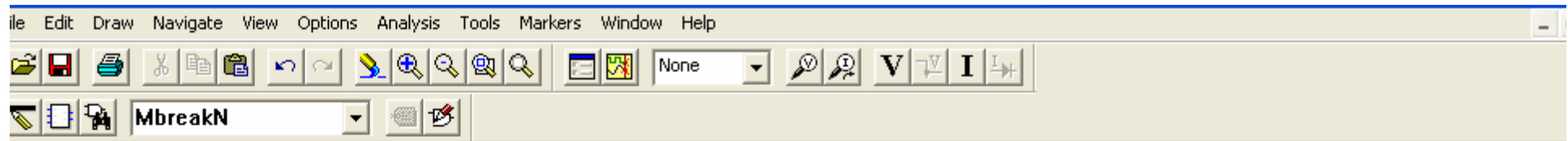
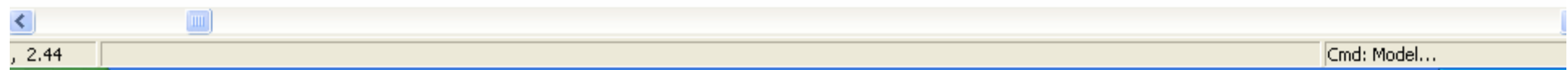


Fig. Part Name TC407P or PMOS and TC407N or NMOS for Op-Amp Circuit Drawing



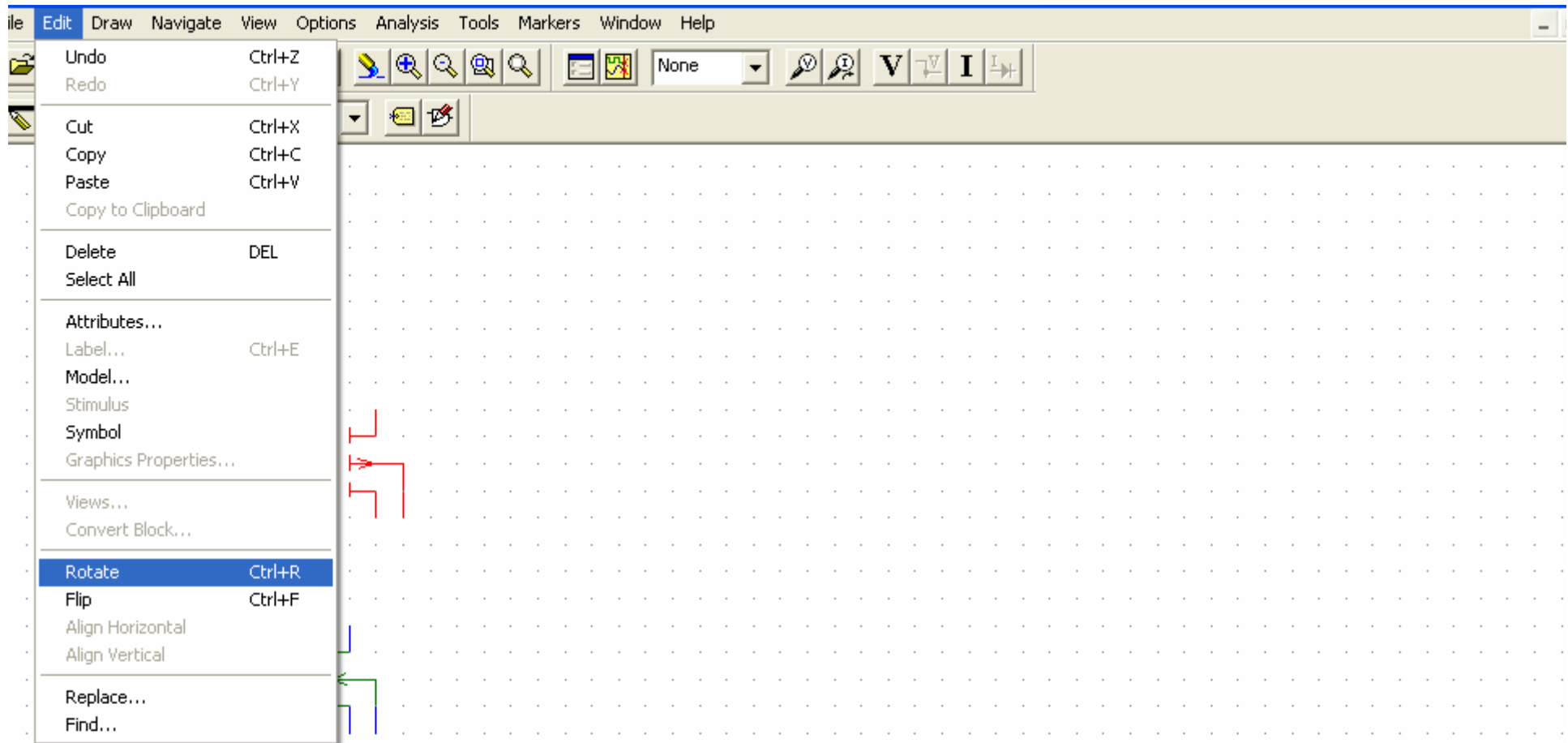
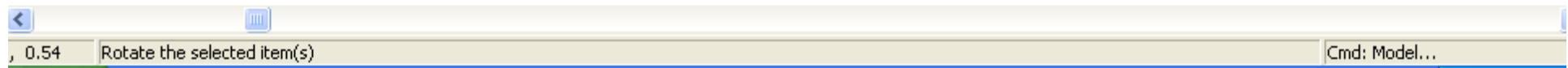


Fig. Rotate Part for Op-Amp Circuit Drawing



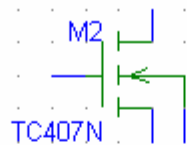
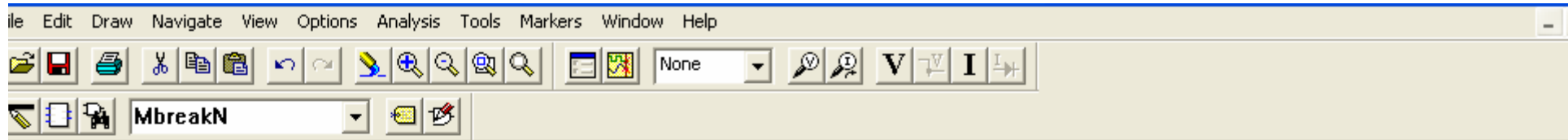
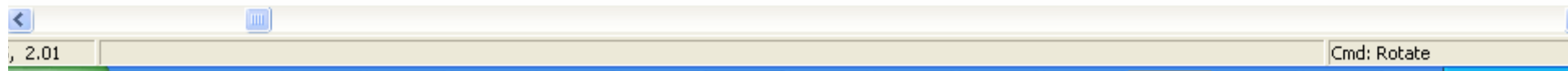


Fig. Rotated Part for Op-Amp Circuit Drawing



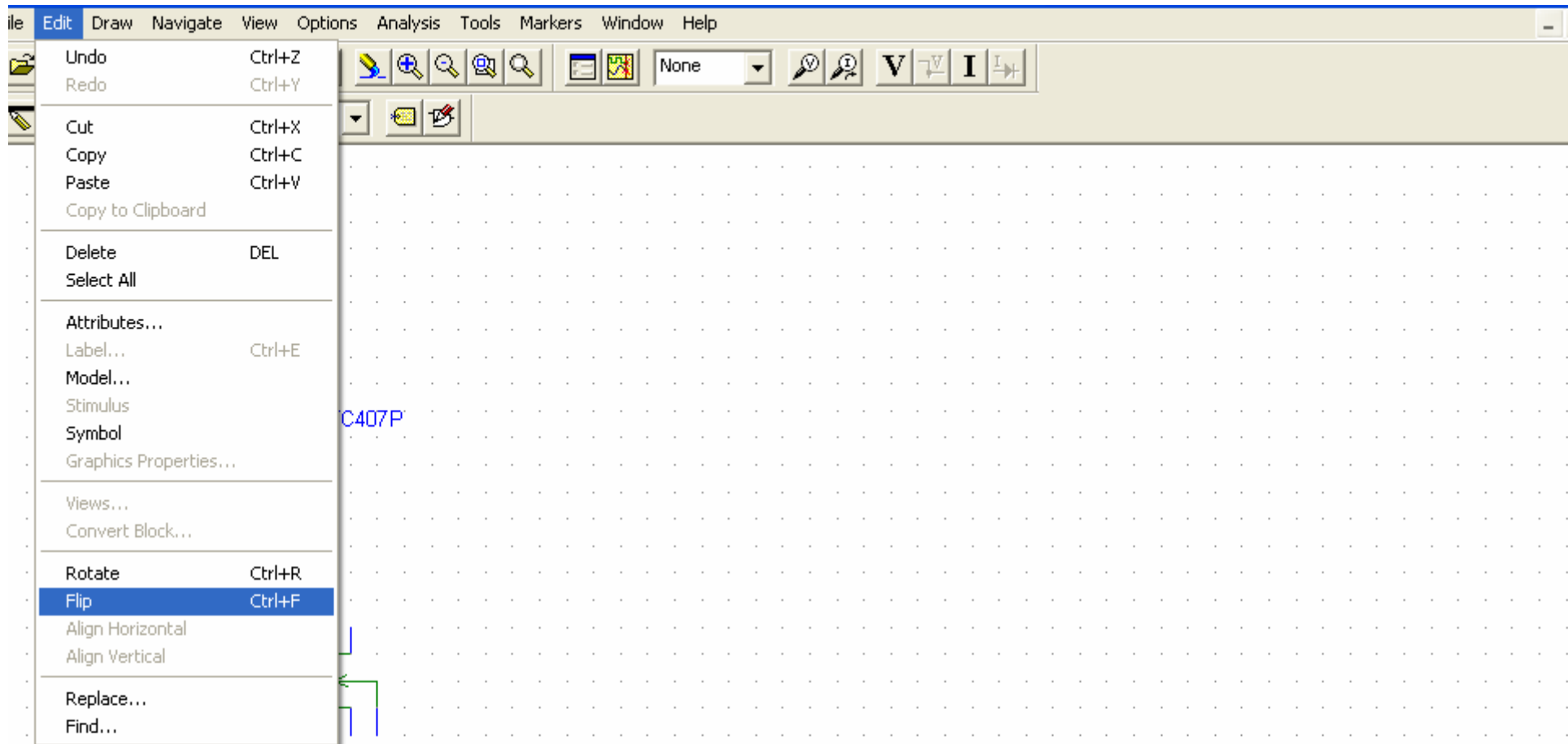
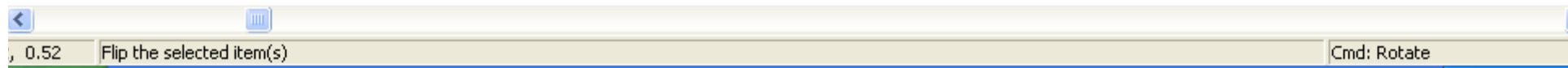


Fig. Flip Part for Op-Amp Circuit Drawing



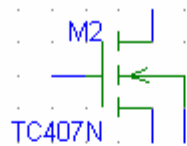
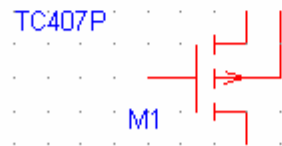
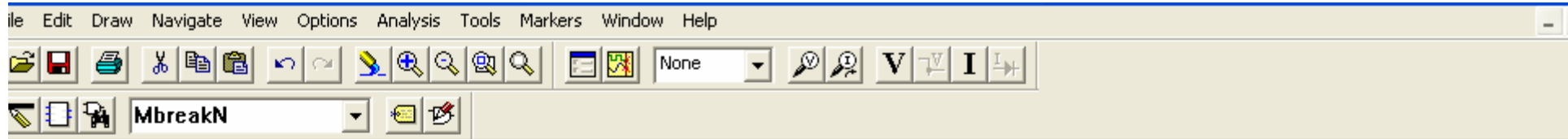
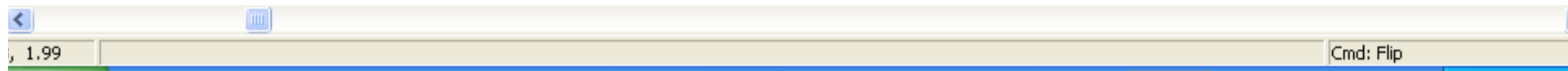


Fig. Flipped Part for Op-Amp Circuit Drawing



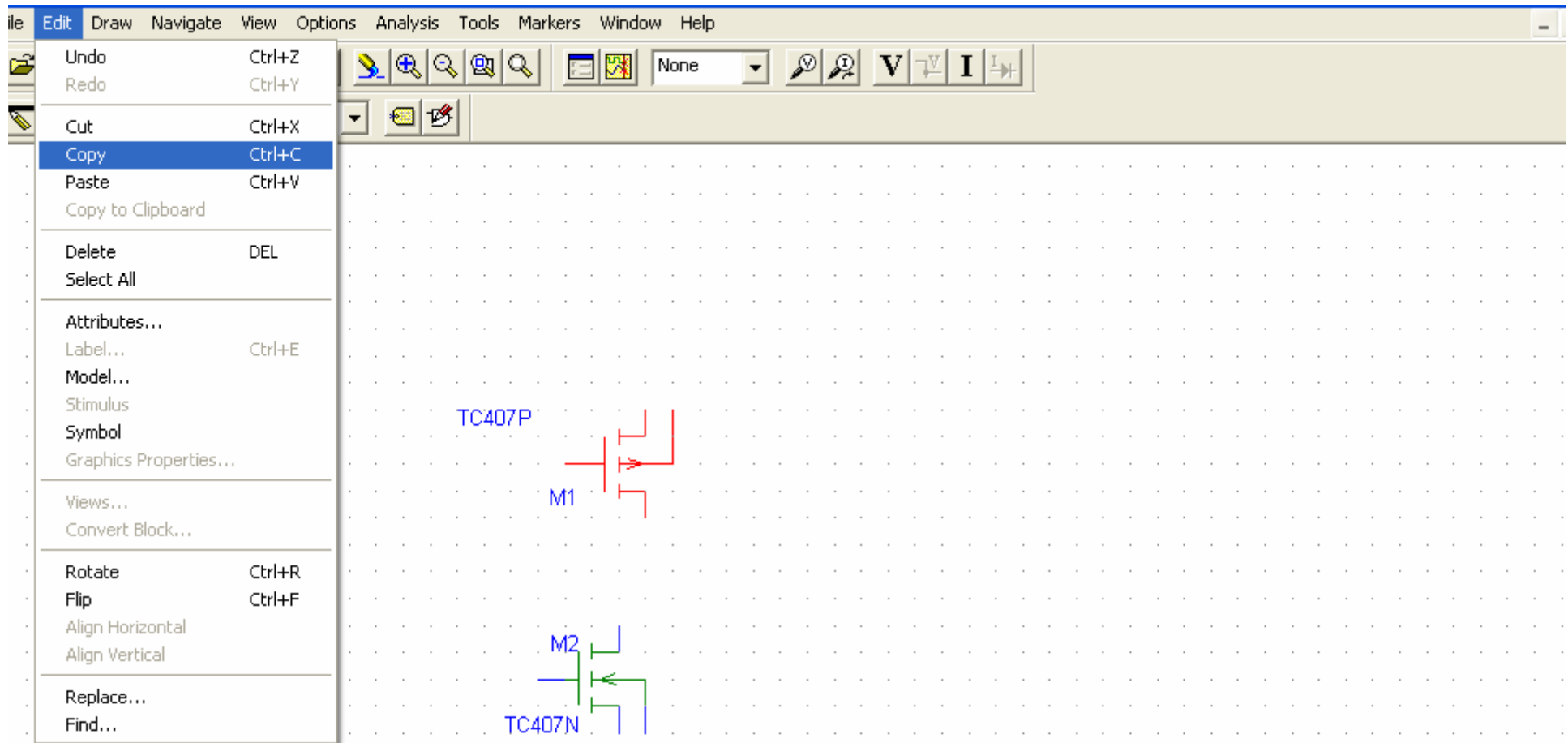
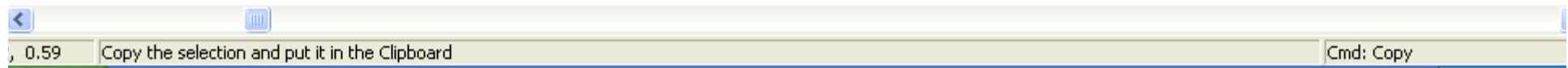


Fig. Copy Part for Op-Amp Circuit Drawing



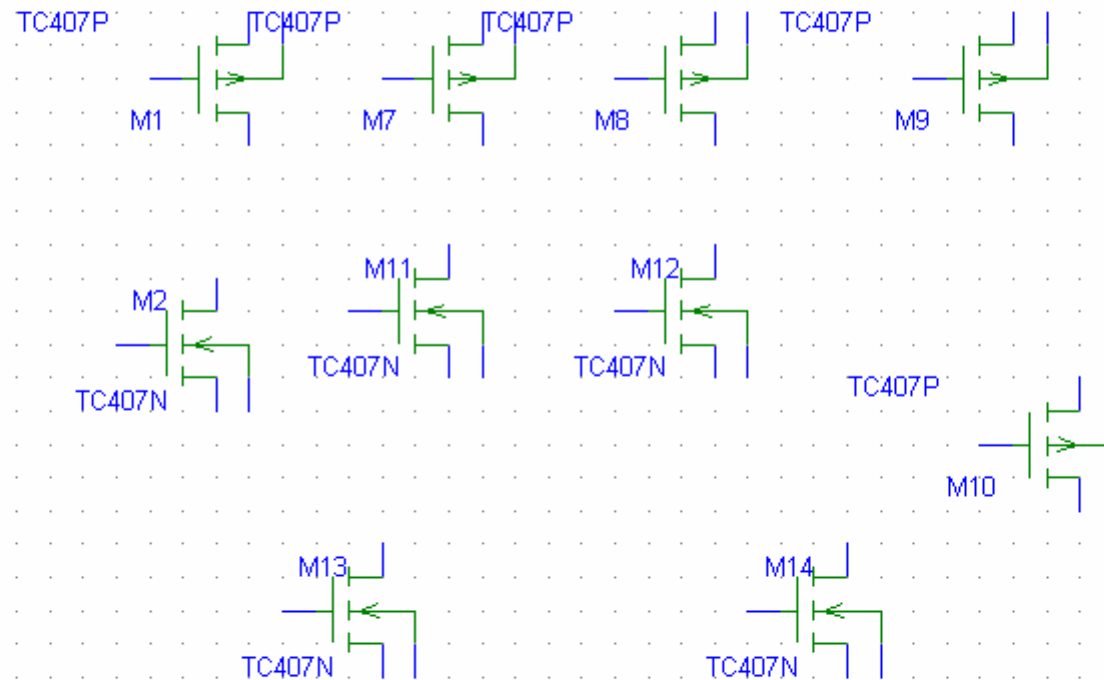
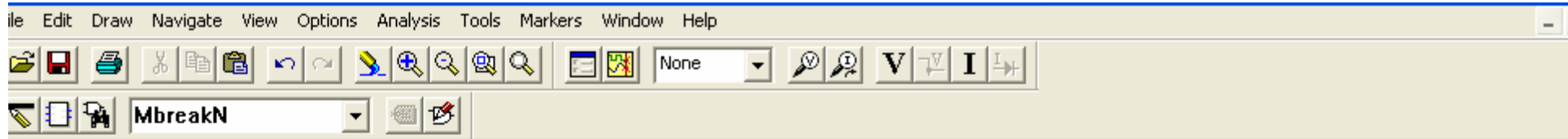
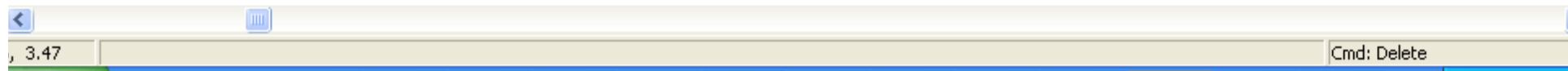


Fig. NMOS and PMOS for Op-Amp Circuit Drawing



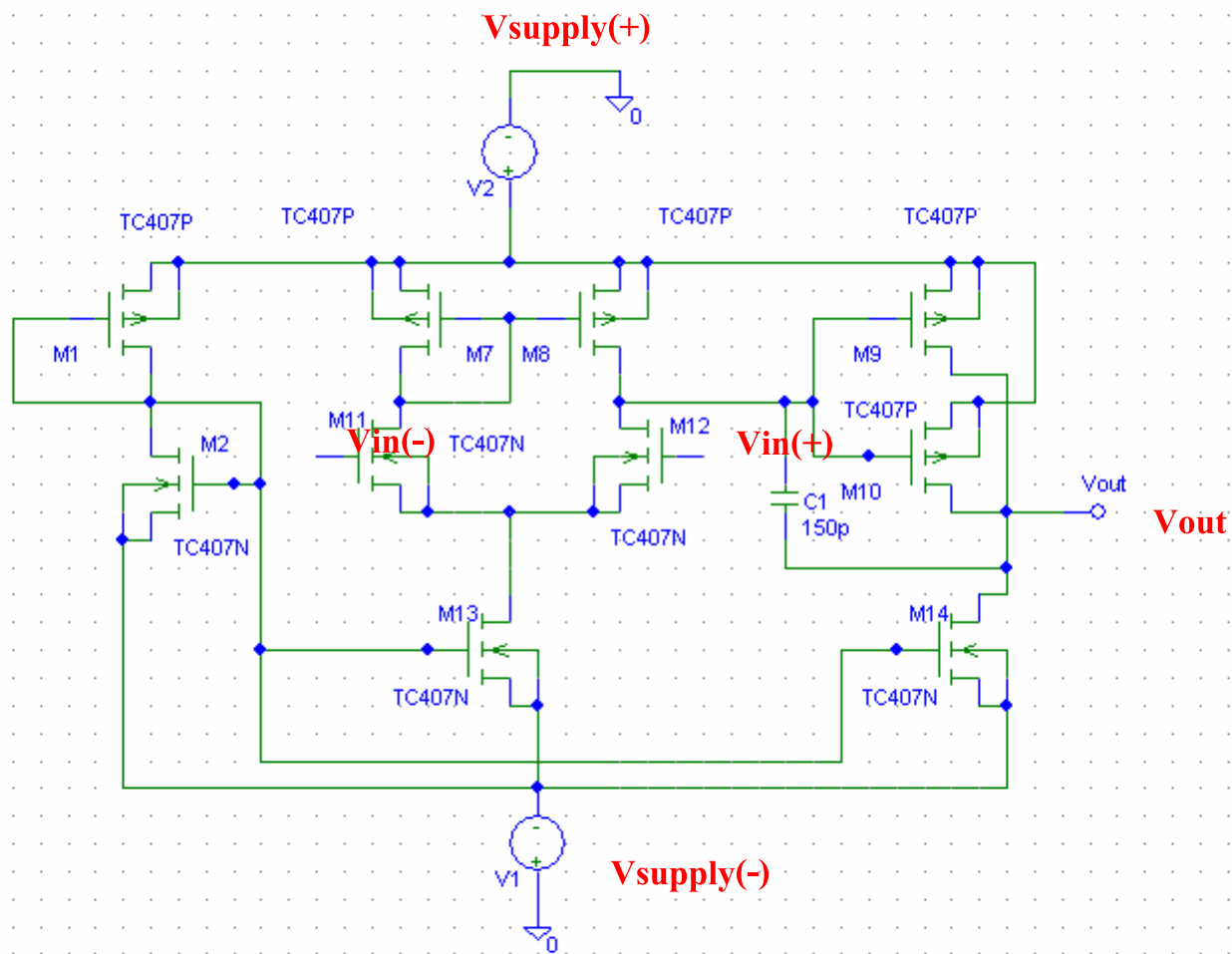
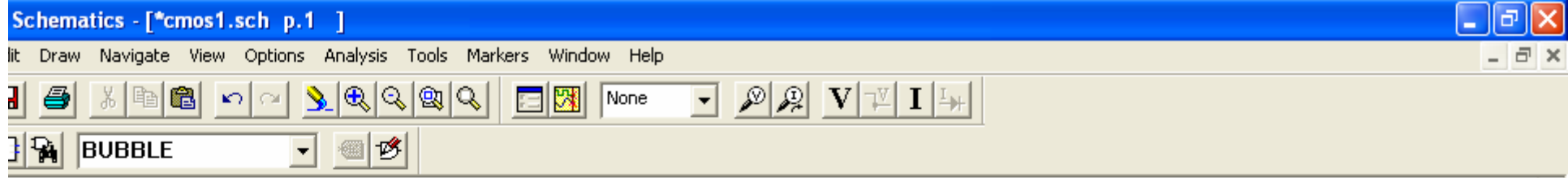


Fig. CMOS- OP-Amp Circuit

วาดรูปวงจร ทดสอบ **Op-Amp**

Slew Rate

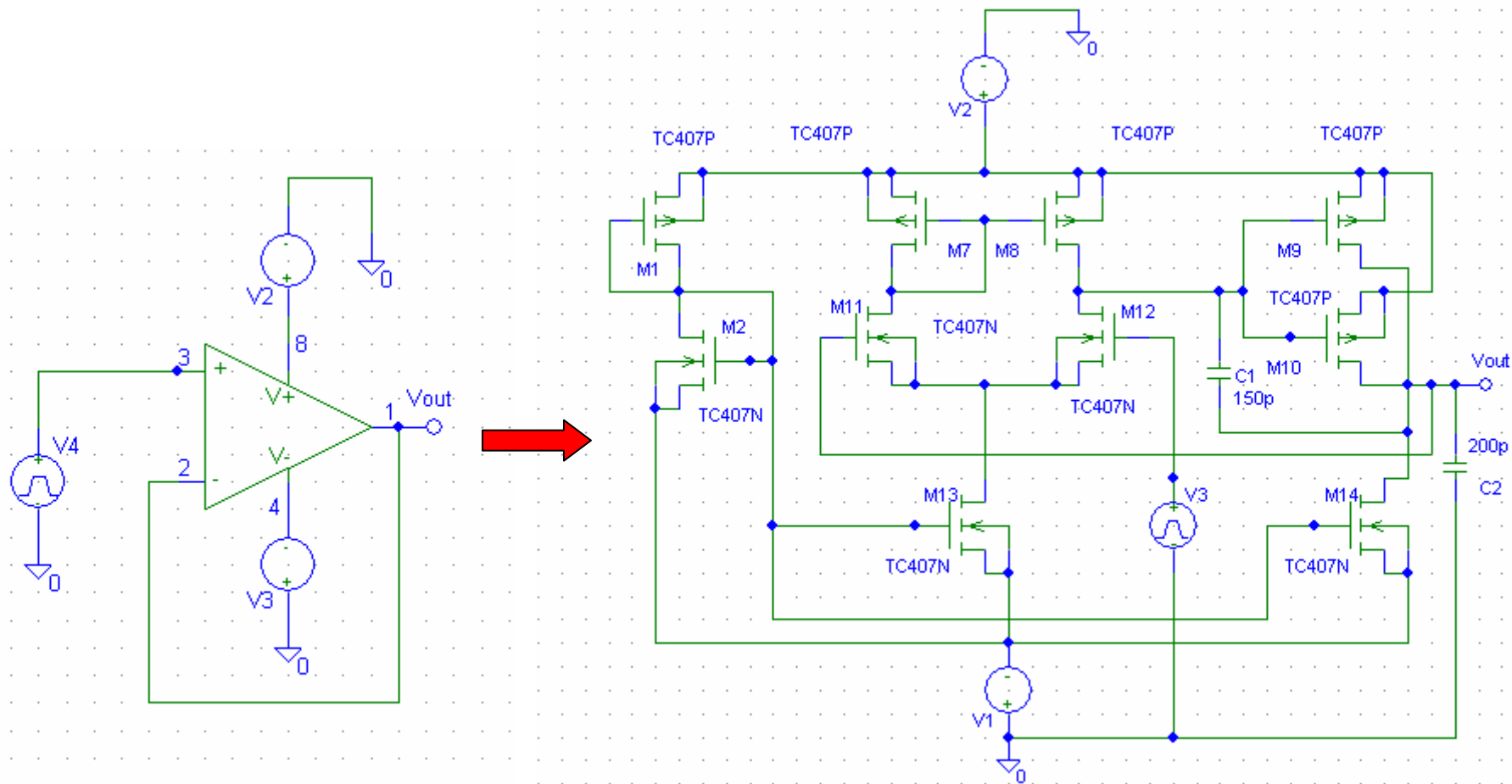
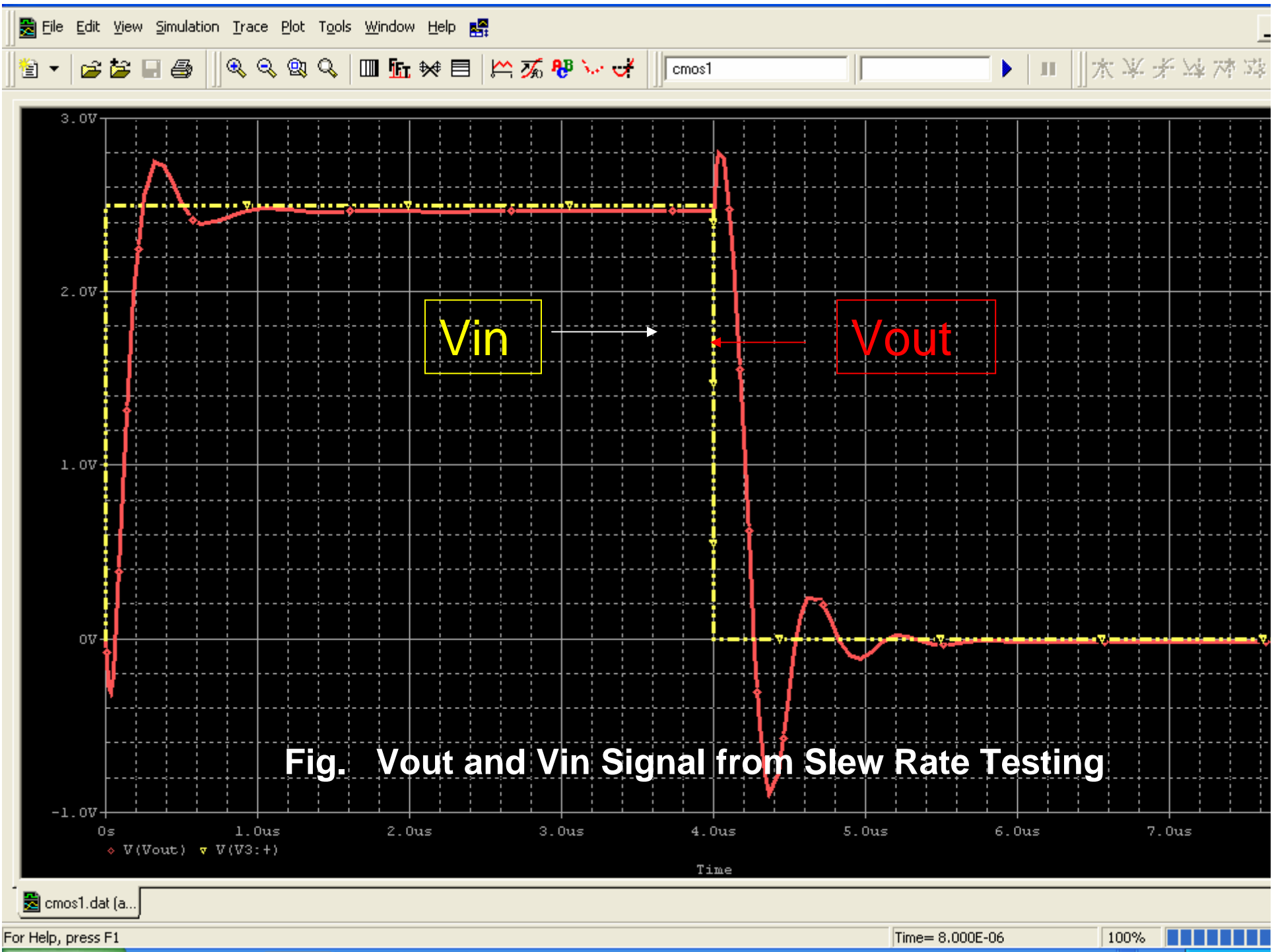


Fig. SLEW RATE TESTING CIRCUIT



การทดลองที่ 1: Slew Rate ของ Op Amp

ช่วง	ค่า
Slew Rate ขาขึ้น	$\frac{\Delta V}{\Delta t} = \frac{2.5}{\Delta t} = \dots\dots\dots \text{Volt} / \mu\text{sec}$
Slew Rate ขาลง	$\frac{\Delta V}{\Delta t} = \frac{2.5}{\Delta t} = \dots\dots\dots \text{Volt} / \mu\text{sec}$
Settling Time	$\dots\dots\dots \mu\text{sec}$

Fig. Record for Results



Part Browser Advanced

Part Name:

Description:

Description Search:
Create New Part List

Library: C:\Program Files\Orcad\PSpice\Libra

- VP1310
- VPLOT1
- VPLOT2
- VPRINT1
- VPRINT2
- VPULSE**
- VPWL
- VPWL_ENH
- VPWL_F_RE_FORE
- VPWL_F_RE_N_TIM
- VPWL_FILE
- VPWL_RE_FOREVE
- VPWL_RE_N_TIMES
- VSFFM
- VSIN
- VSRC
- VSTIM

Full List

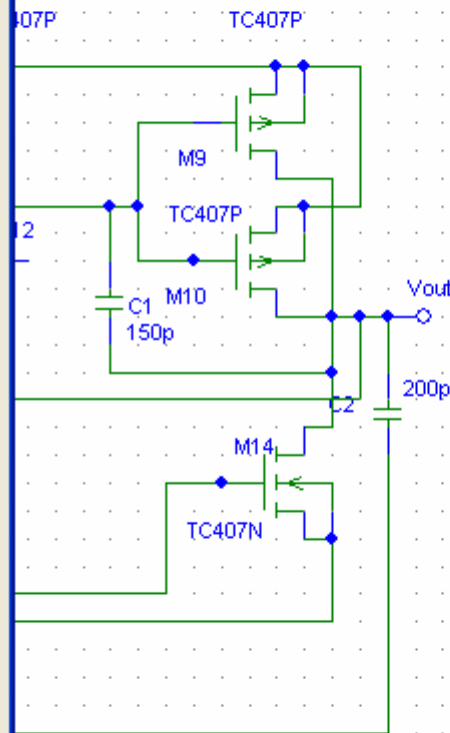


Fig. Vpulse Sep Up for Slew Rate Testing

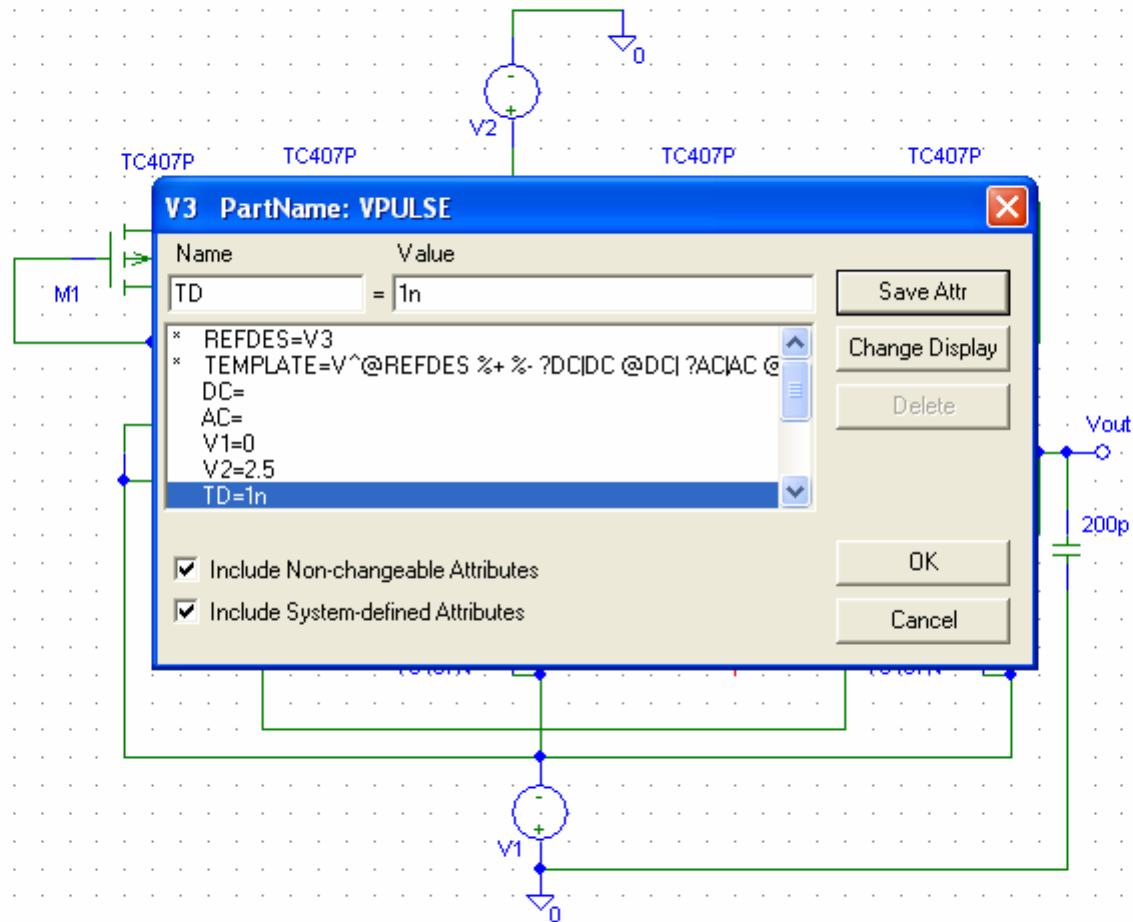
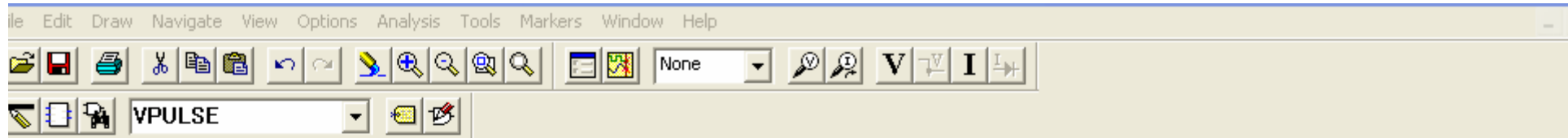


Fig. Vpulse Sep Up for Slew Rate Testing

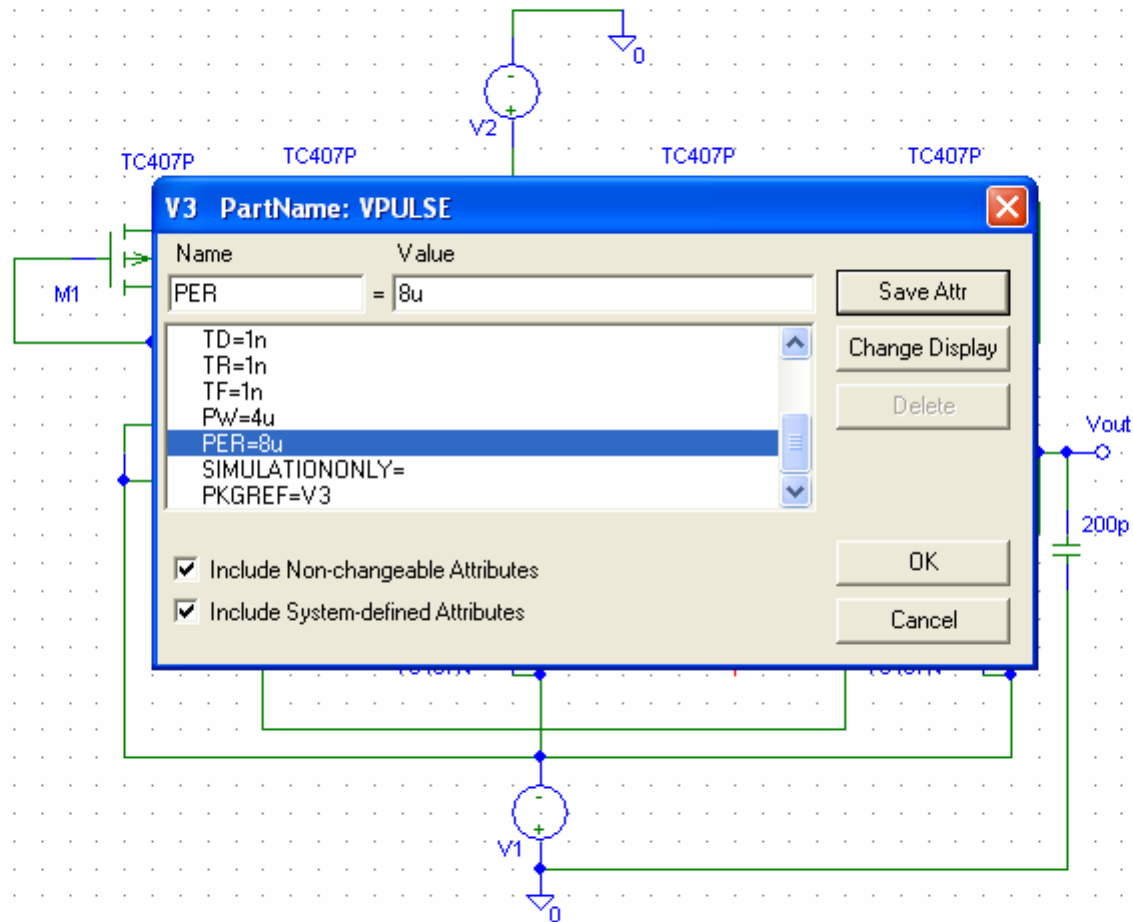


Fig. Vpulse Sep Up for Slew Rate Testing

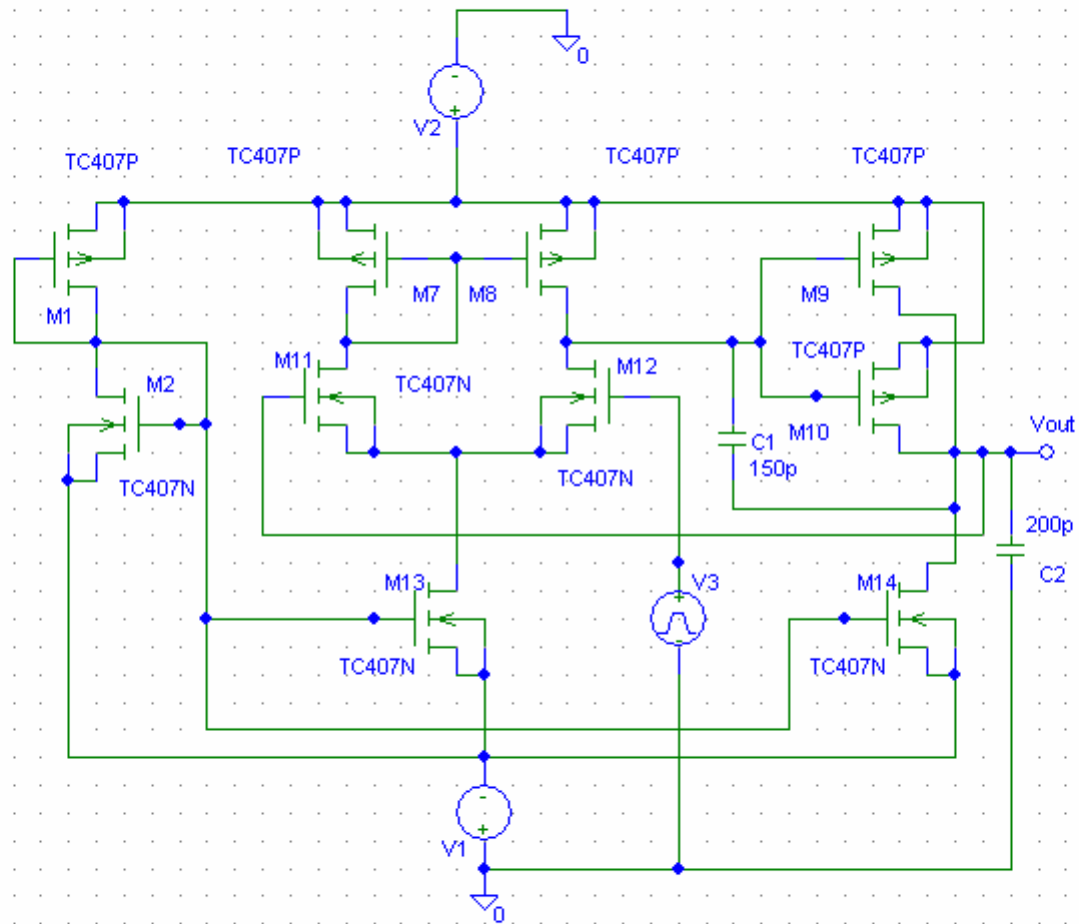
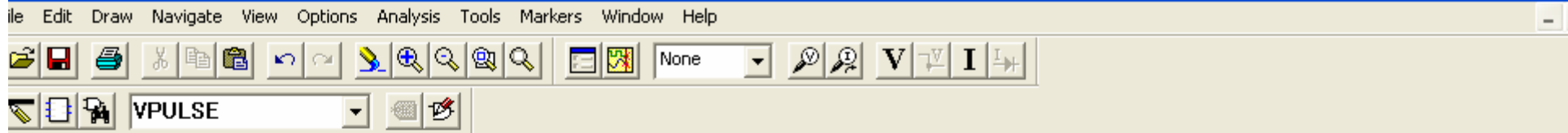


Fig. Slew Rate Testing Complete Circuit

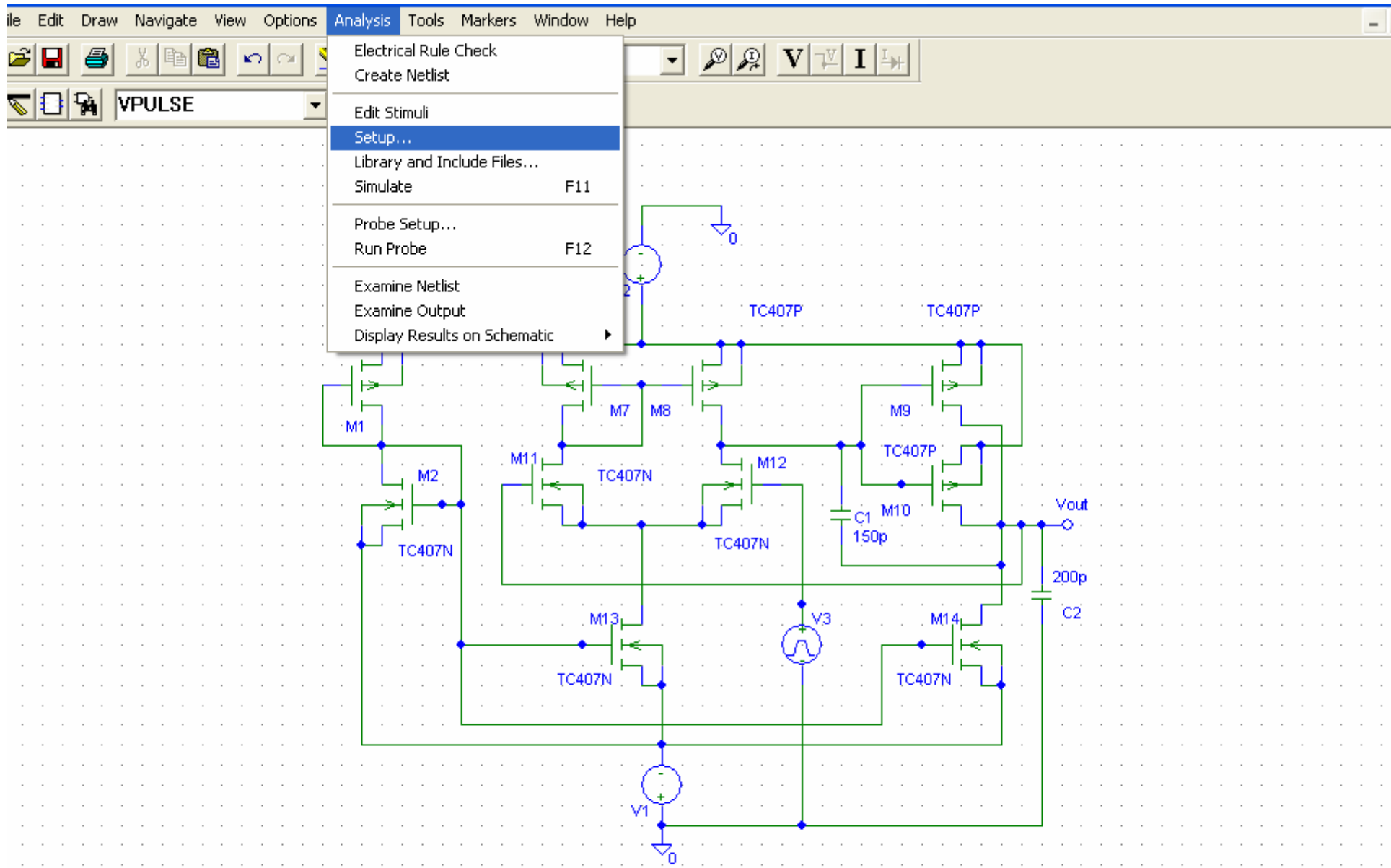


Fig. Sep Up for Slew Rate Testing

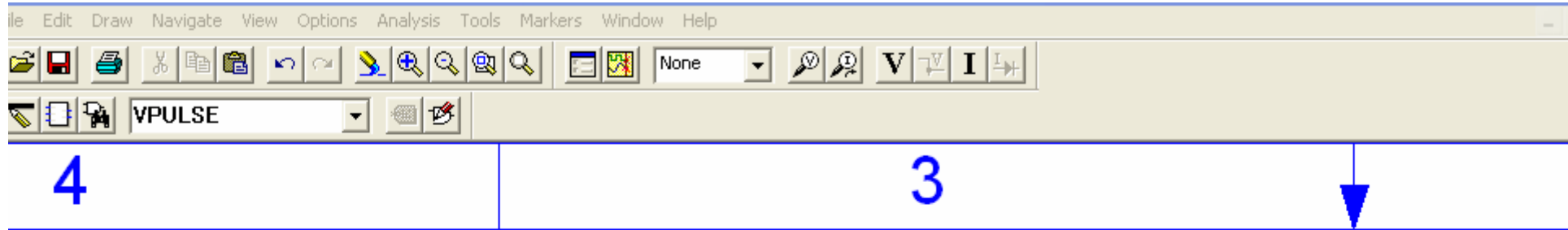
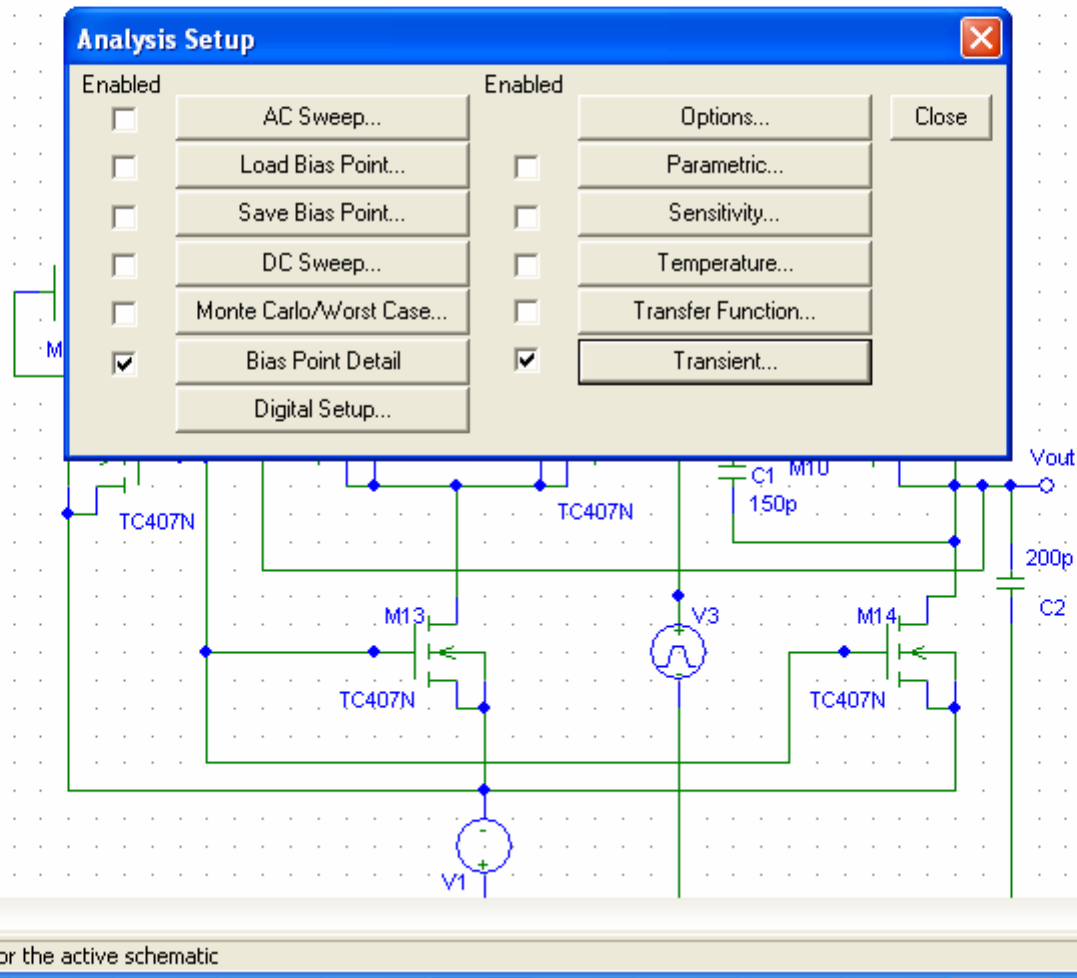


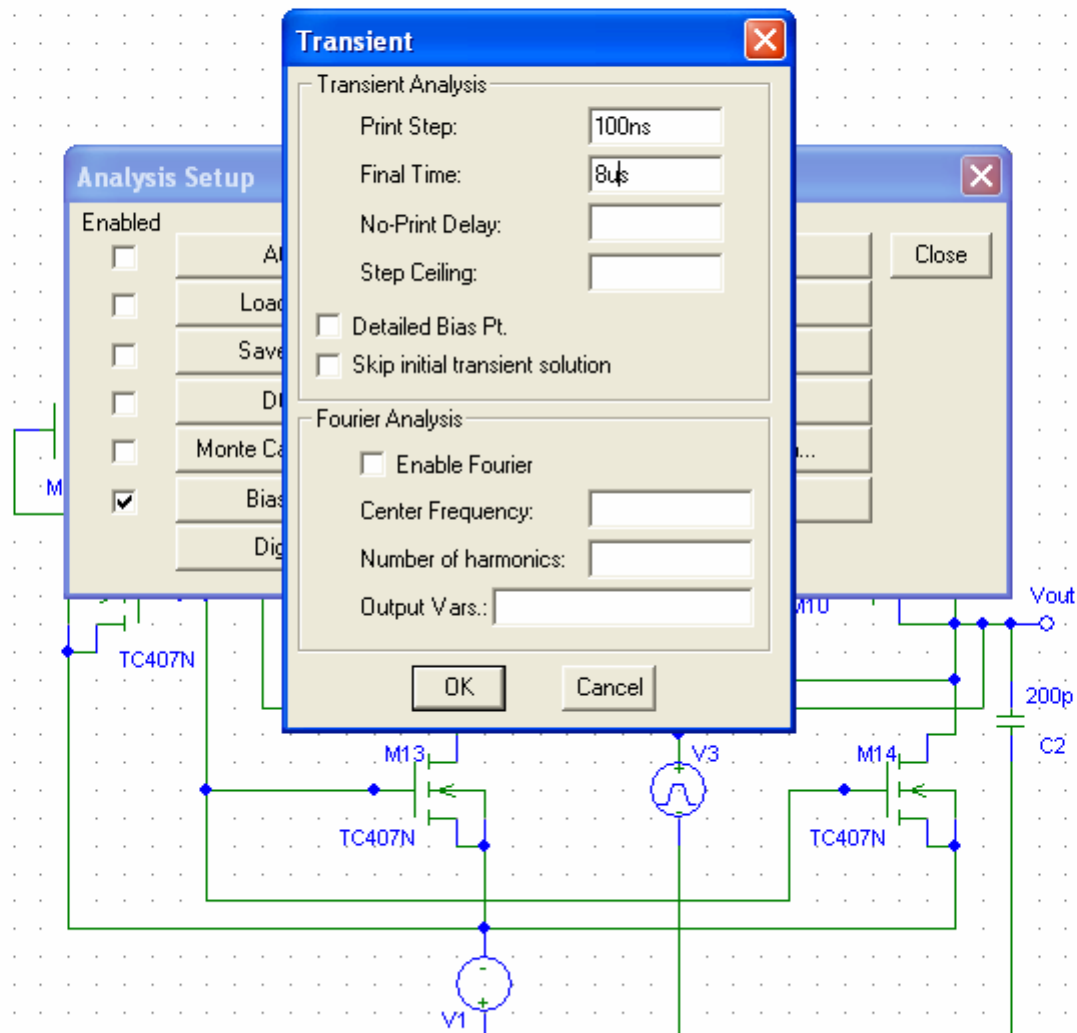
Fig. Transient Sep Up for Slew Rate Testing





4

Fig. Transient Sep Up for Slew Rate Testing



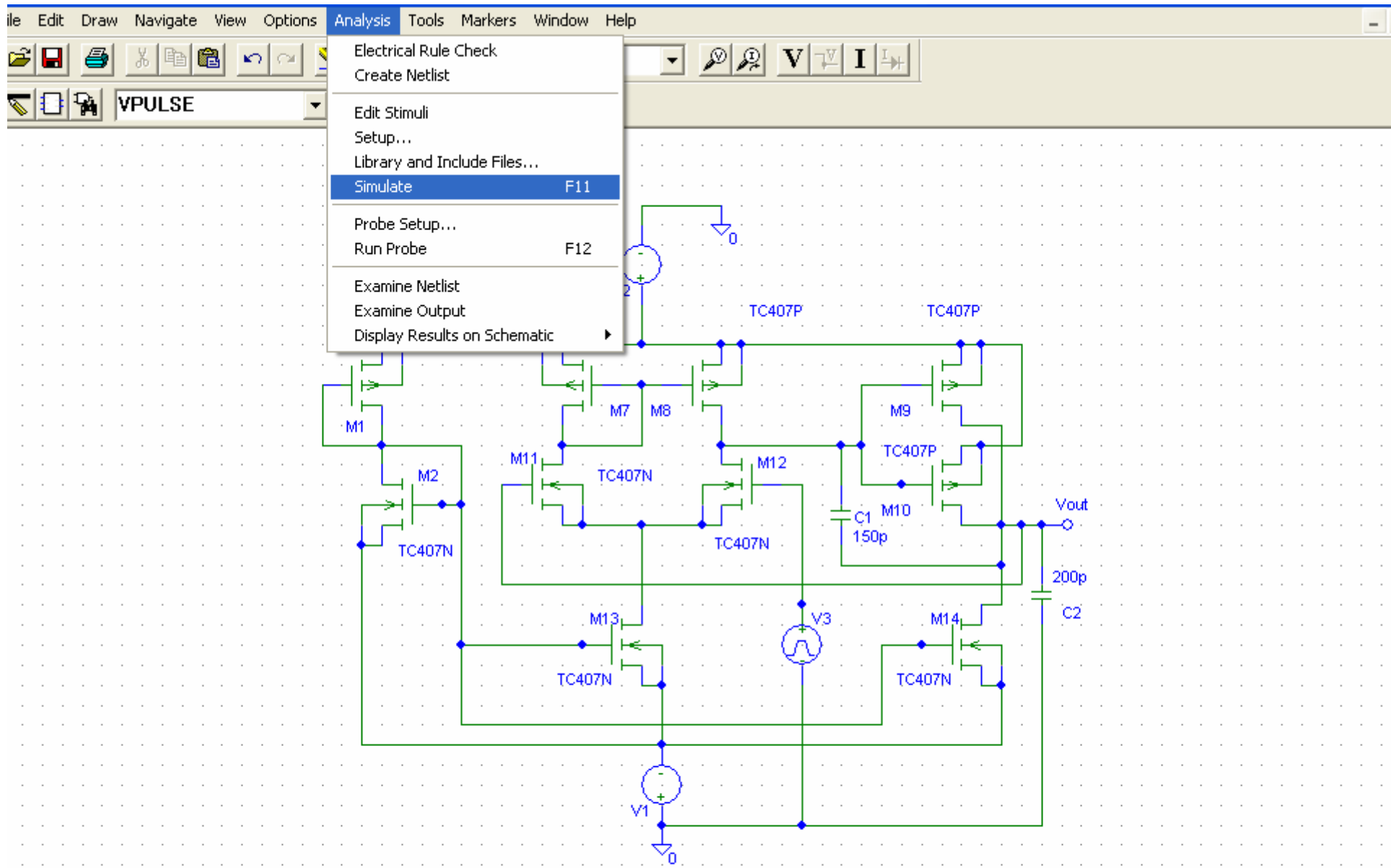


Fig. Simulate PSpice for Slew Rate Testing

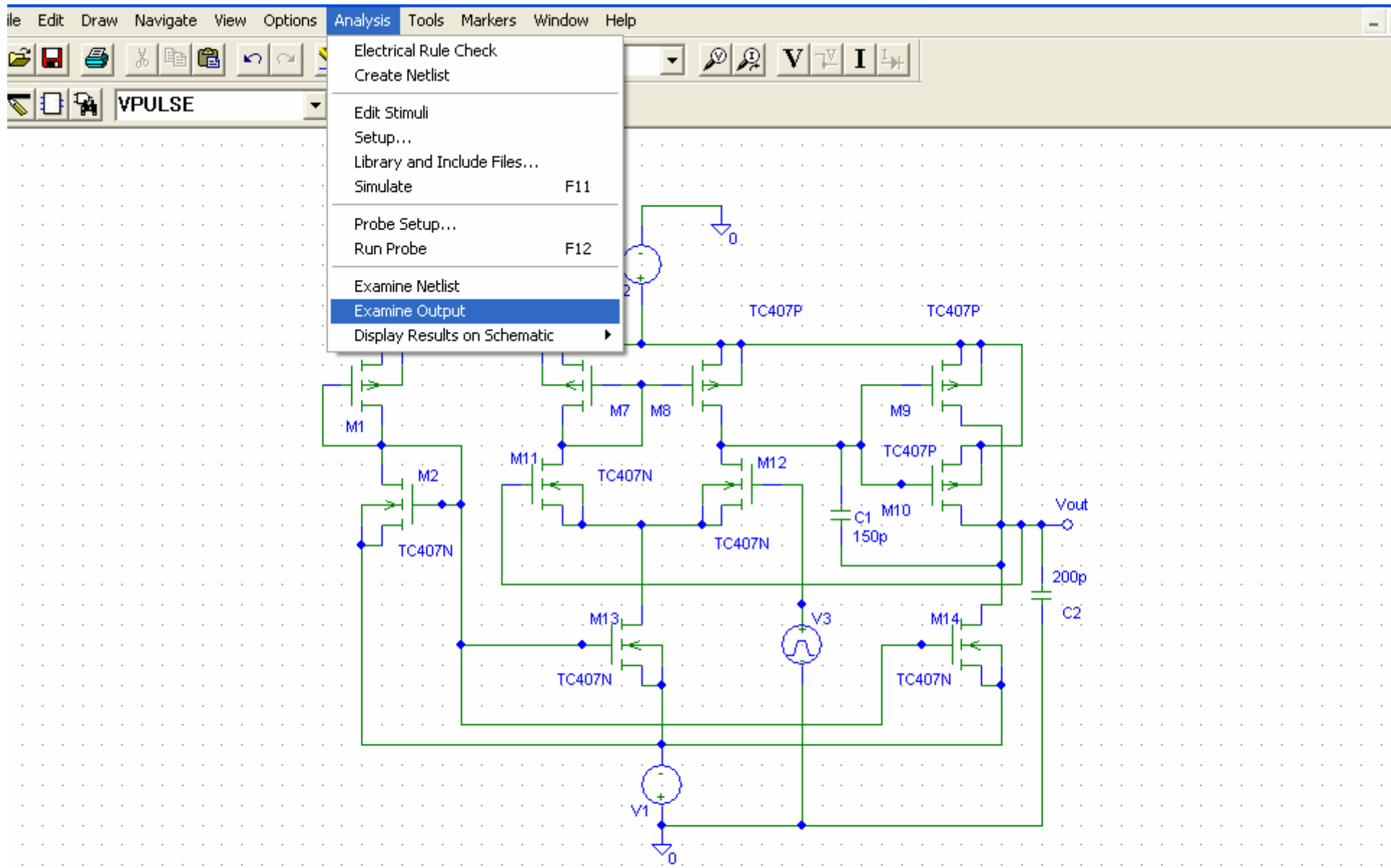
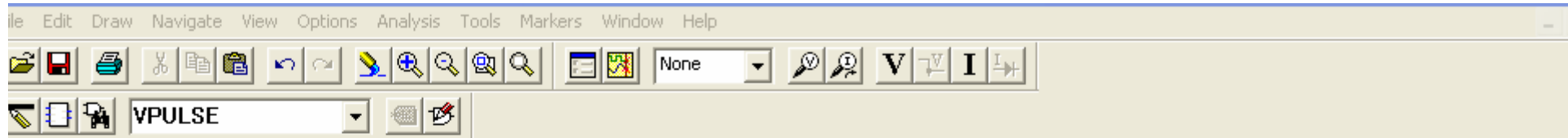


Fig. Open Output File for Error Checking



```
cmos1.out - Notepad
File Edit Format View Help
**** RESUMING cmos1.cir ****
.PROBE V(*) I(*) W(*) D(*) NOISE(*)

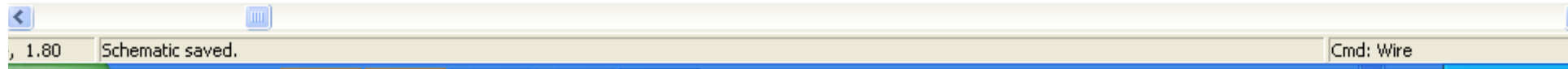
.END

WARNING -- Library file D:\Cook\CMOS\cmos.lib has changed since index file cmos.ind was created.
WARNING -- The timestamp changed from Sat Dec 08 13:30:35 2007 to Sat Dec 08 16:49:12 2007.
Making new index file cmos.ind for library file cmos.lib.model TC407N(LEVEL=3 LD=1.2U VT0=0.7 KP=1.73E-5
GAMMA=1.0
-----$
ERROR -- Model type unknown
+ TOX=1.0E-7 TPG=0 NSUB=5E15 L=8U
+ W=200U WD=1.4U RD=2.0 RS=2.0 RG=2.0
+ CGSO=4.14E-10 CGDO=4.14E-10 CGBO=1.61E-10 TT=100n)
*CMOS IC(TC4007 UBP) CMOS LOCCOS 8U PROCESS

.model TC407P(LEVEL=3 LD=1.2U VT0=-0.6 KP=0.69E-5 GAMMA=0.9
-----$
ERROR -- Model type unknown

Index has 0 entries from 1 file(s).
+ TOX=1.0E-7 TPG=0 NSUB=2E15 L=8U
+ W=480U WD=1.4U RD=2.0 RS=2.0 RG=2.0
+ CGSO=4.14E-10 CGDO=4.14E-10 CGBO=1.61E-10 TT=80n)
```

Fig. Error from Library File



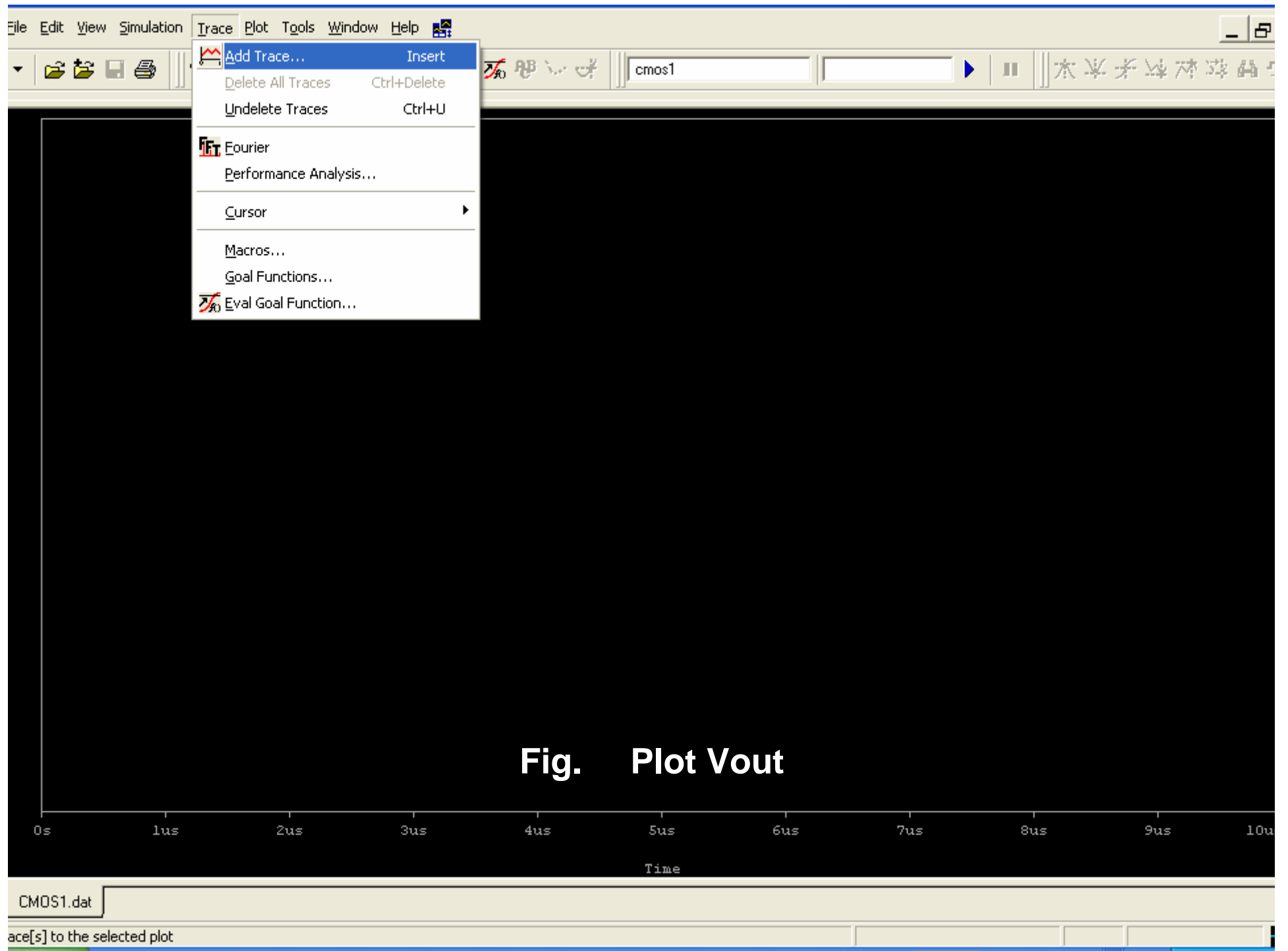


Fig. Plot Vout

Add Traces

Simulation Output Variables

*

- V(M9:d)
- V(M9:g)
- V(M9:s)
- V(V1:+)
- V(V1:-)
- V(V2:+)
- V(V2:-)
- V(V4:+)
- V(V4:-)
- V(Vout)**
- V1(C1)
- V1(V1)
- V1(V2)
- V1(V4)
- V2(C1)
- V2(V1)
- V2(V2)
- V2(V4)
- VB(M1)
- VB(M10)
- VB(M11)
- VB(M2)
- VB(M3)
- VB(M4)

165 variables listed

Functions or Macros

Analog Operators and Functions

- #
- ()
- *
- +
-
- /
- @
- ABS()
- ARCTAN()
- ATAN()
- AVG()
- AVGX(.)
- COS()
- D()
- DB()
- ENVMAX(.)
- ENVMIN(.)
- EXP()
- G()
- IMG()
- LOG()
- LOG10()
- M()
- MAX()

Trace Expression: V(Vout)

OK Cancel Help

Fig. Select Vout for Plotting

**Frequency
Response**

```
graph TD; A[Frequency Response] --> B[Non-Inverting]; A --> C[Inverting];
```

**Non-
Inverting**

Inverting

**Frequency
Response**

Non-Inverting

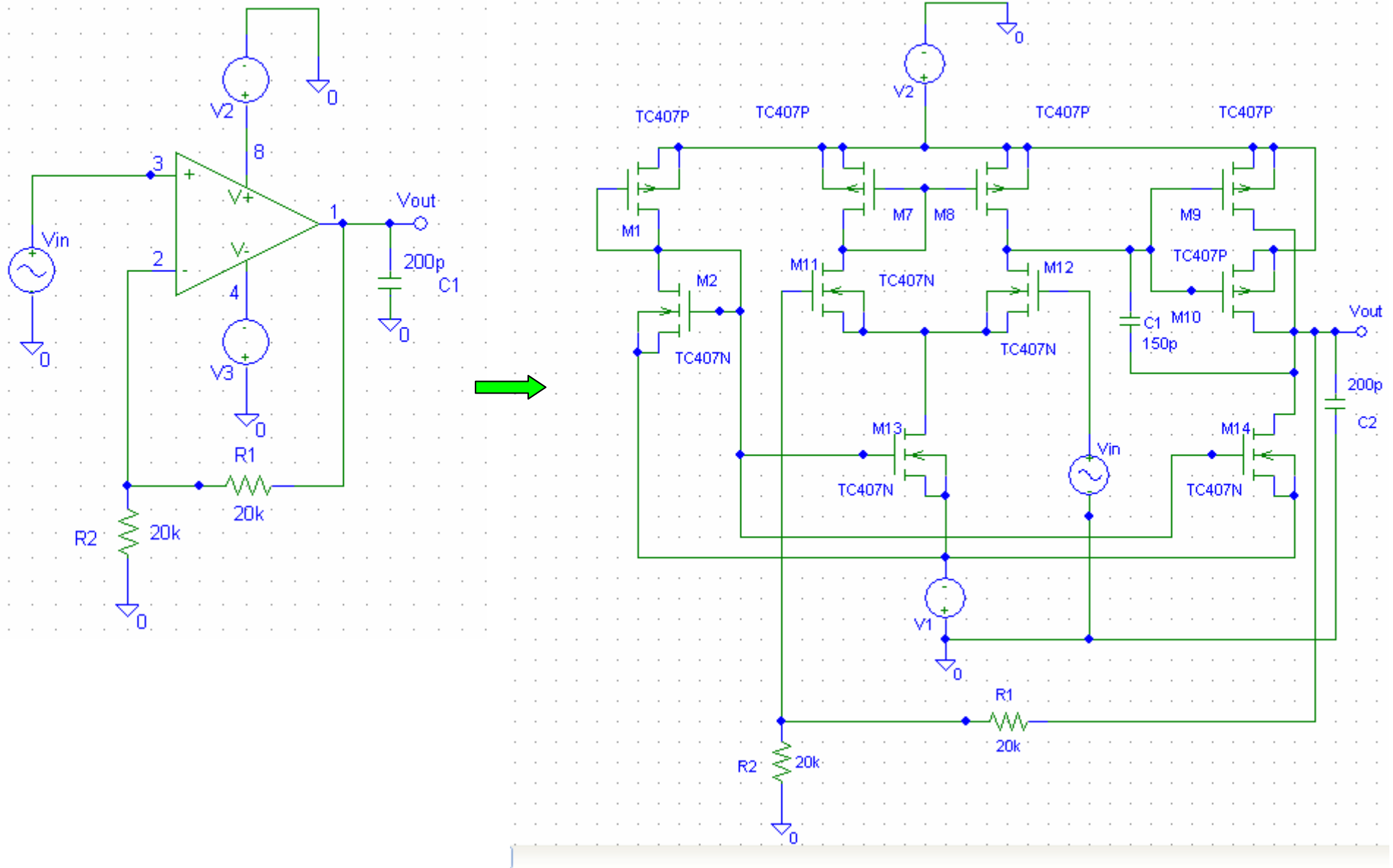


Fig. Frequency Response Testing for Non-Inverting Amplifier

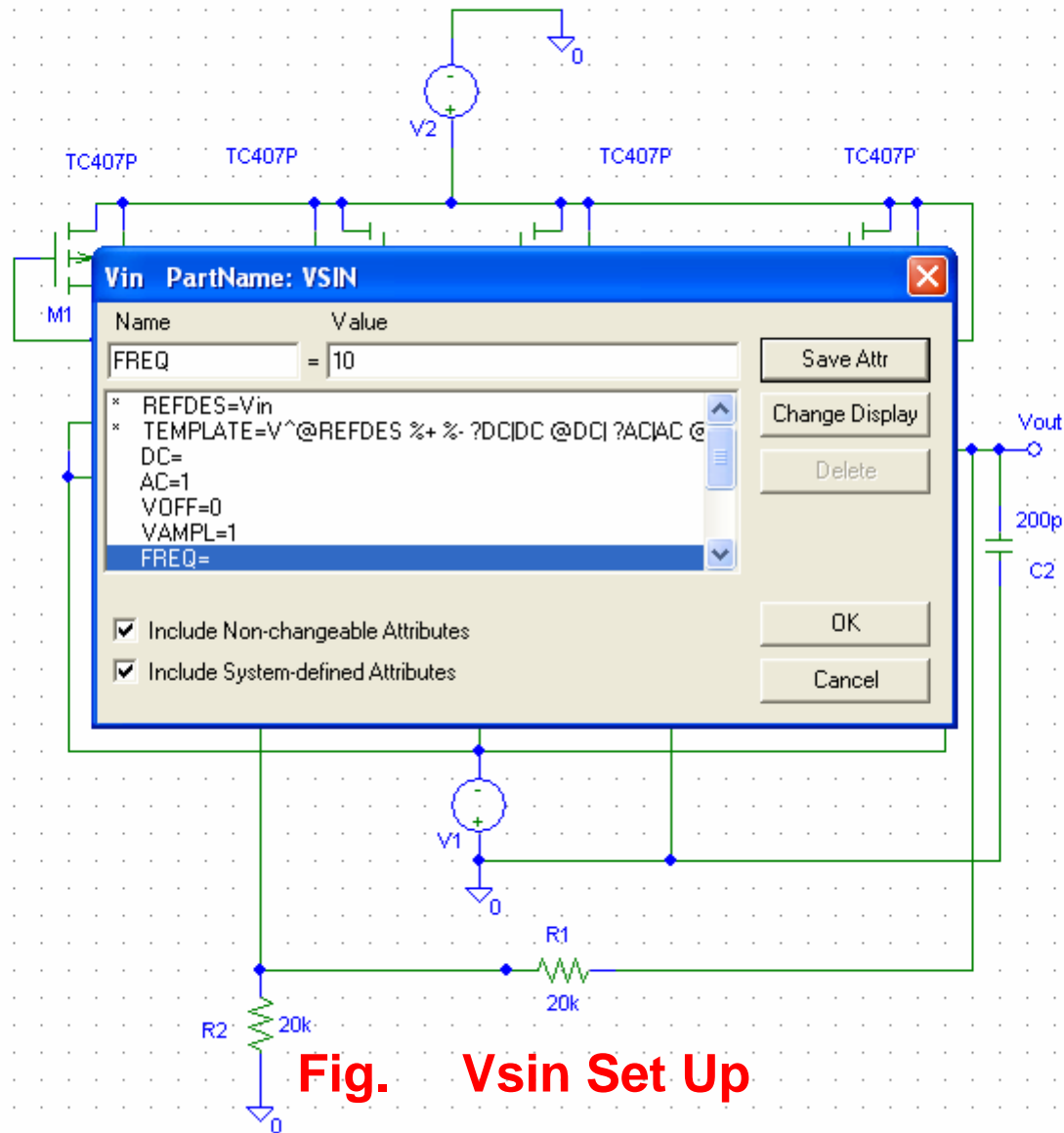


Fig. Vsin Set Up

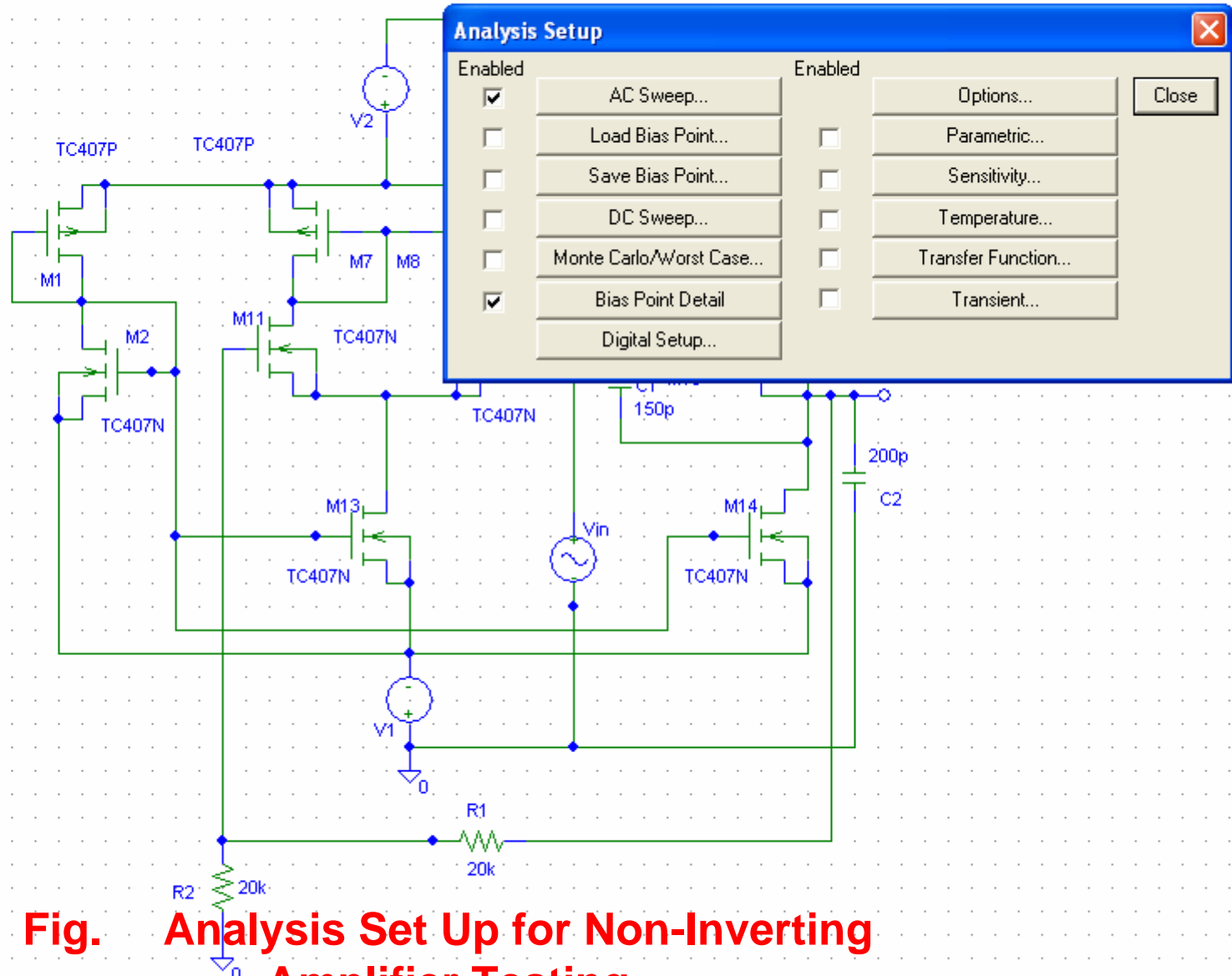


Fig. Analysis Set Up for Non-Inverting Amplifier Testing

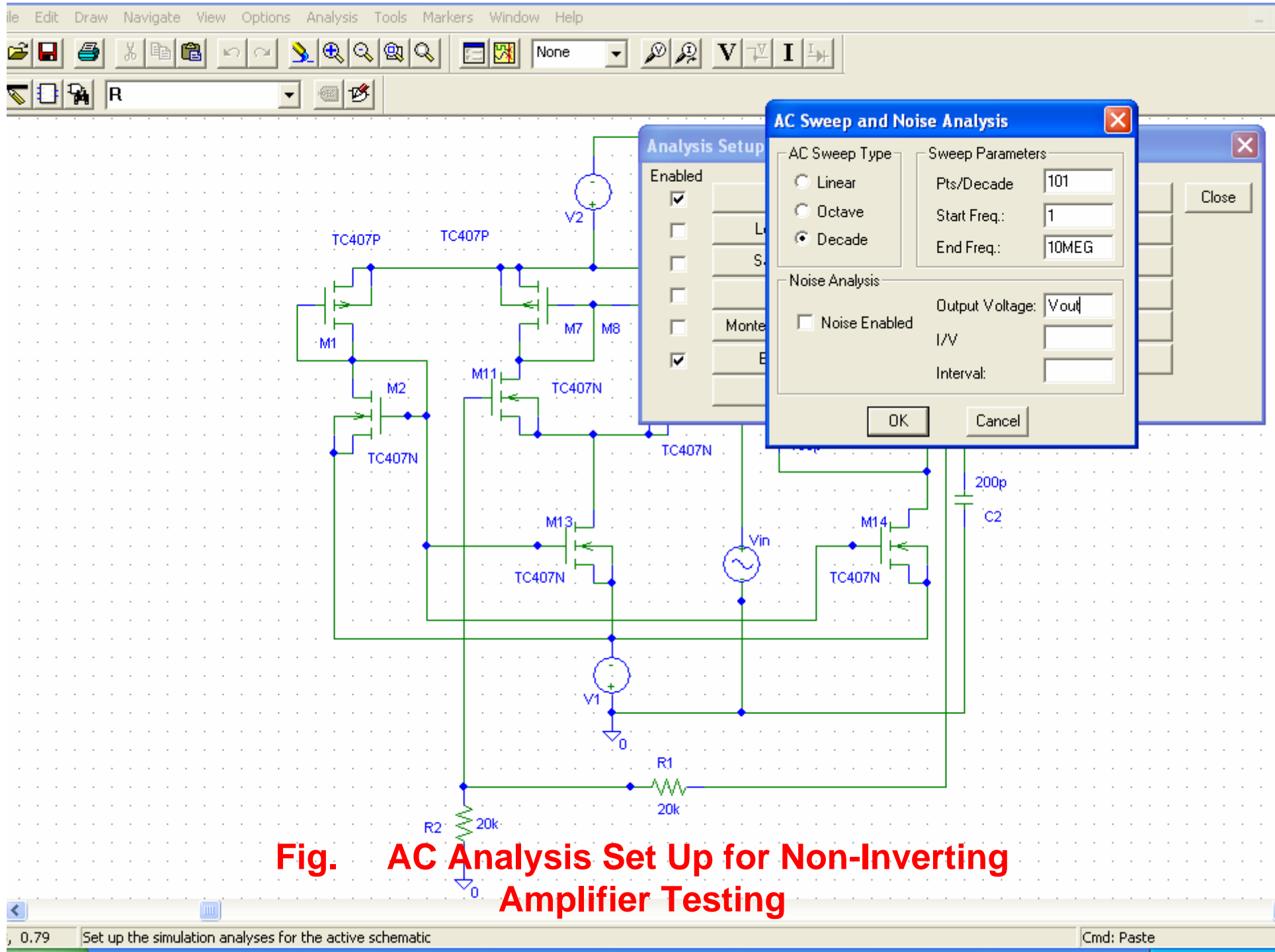
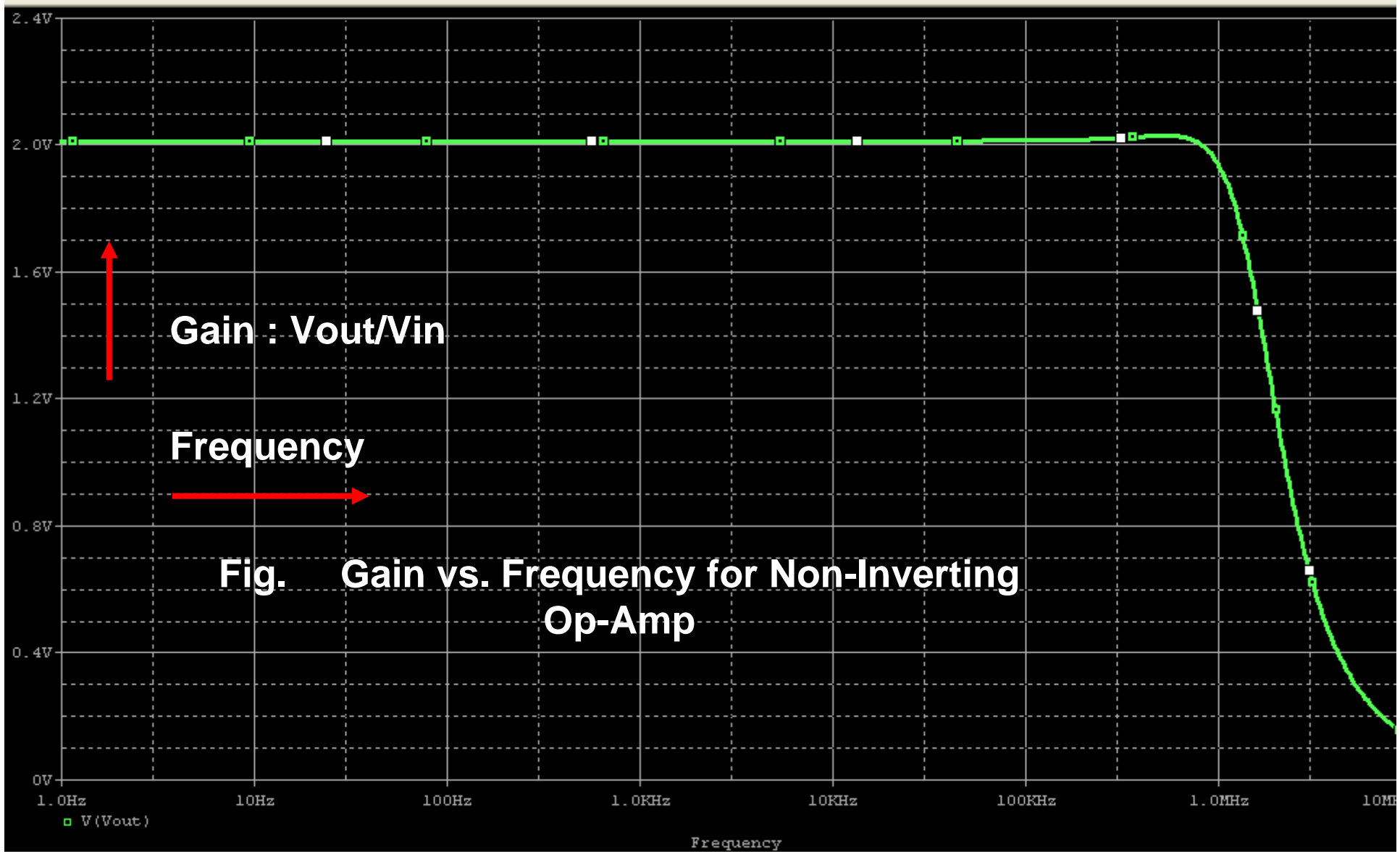


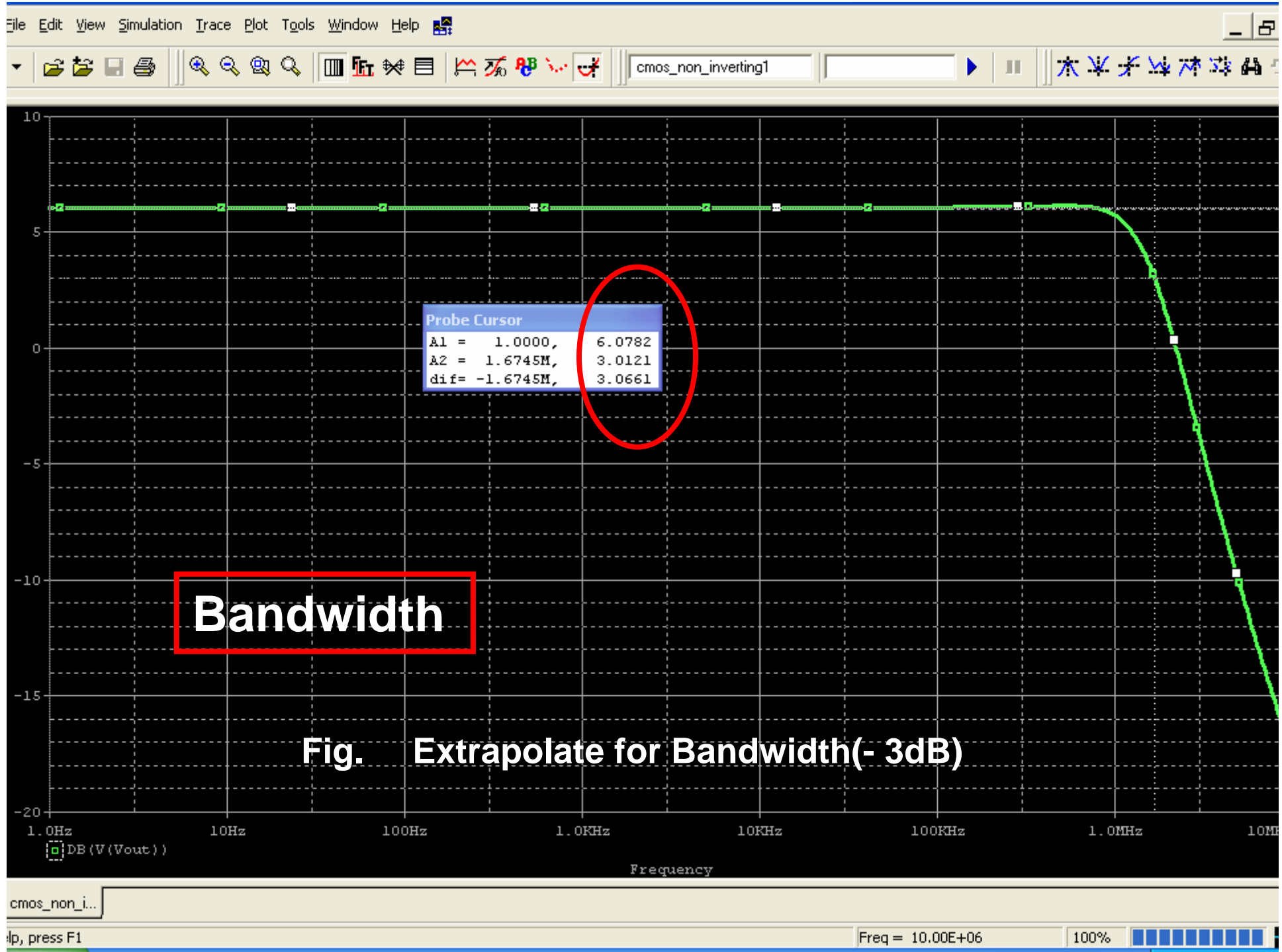
Fig. AC Analysis Set Up for Non-Inverting Amplifier Testing

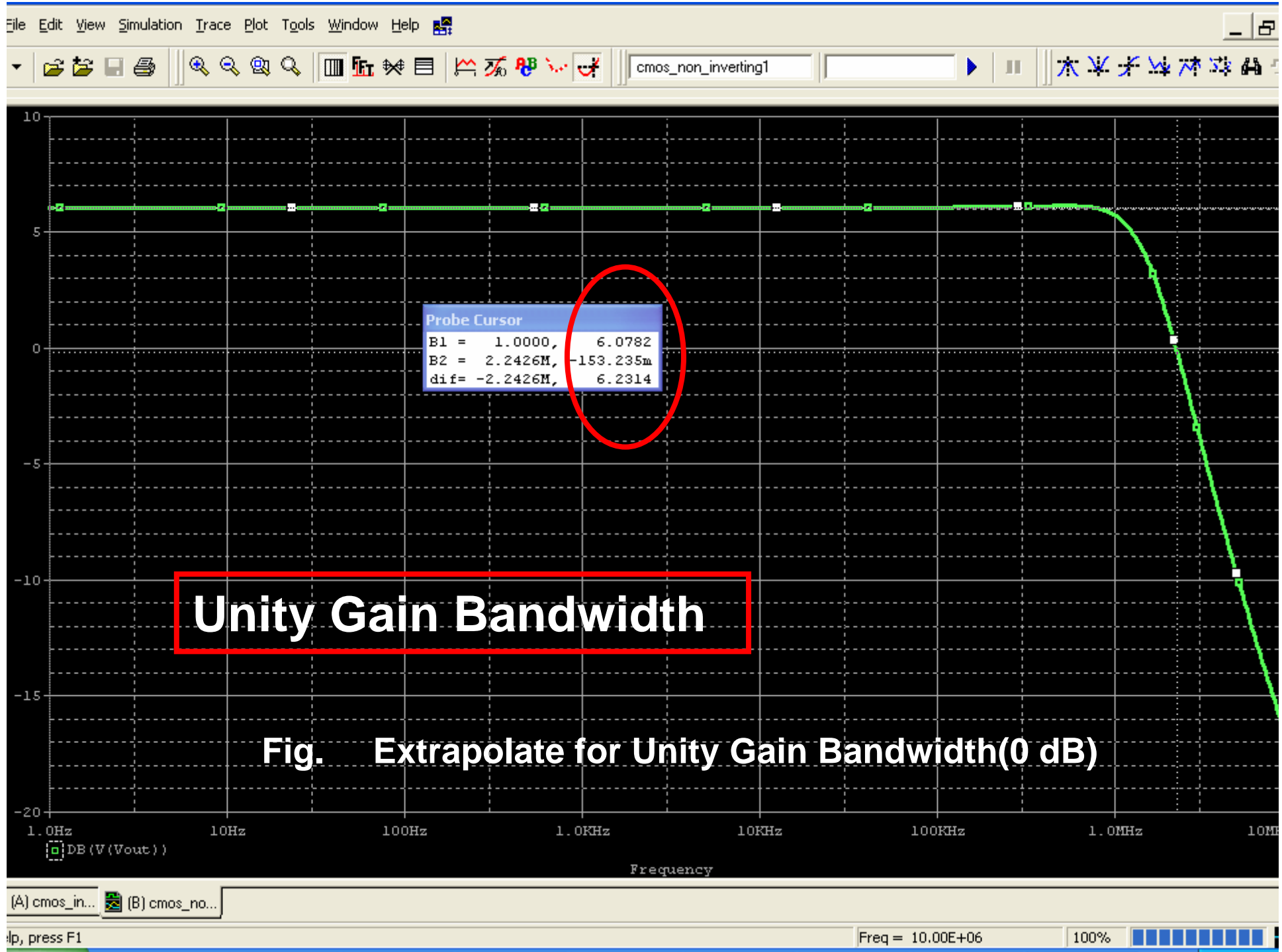


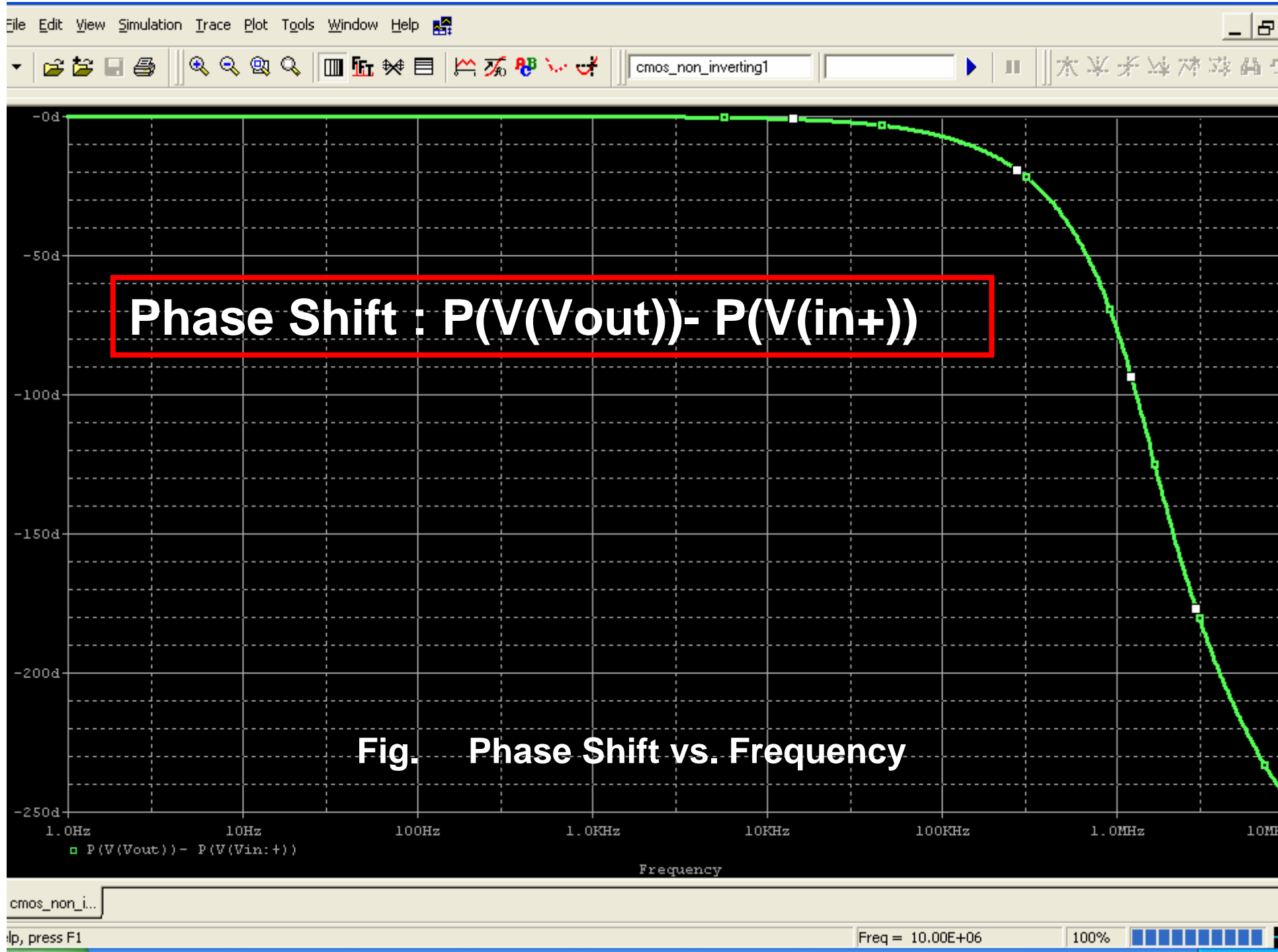
Gain : V_{out}/V_{in}

Frequency

Fig. Gain vs. Frequency for Non-Inverting Op-Amp







การทดลองที่ 2: การตอบสนองการขยายและ Phase ต่อความถี่

2.1 Non-Inverting Amplifier

<u>Frequency(Hz.)</u>	1	10	100	1k	10k	100k	1M	10M
<u>Gain(dB)</u>								
<u>Phase Shift(Degree)</u>								

จาก Bode Plot ได้ค่า

Bandwidth(f_{-3dB}) Hz

Unity Gain Bandwidth(f_T) Hz

Unity Gain Phase Shift Degree

Fig. Record Test for Non-Inverting Amplifier Testing

**Frequency
Response**

Inverting

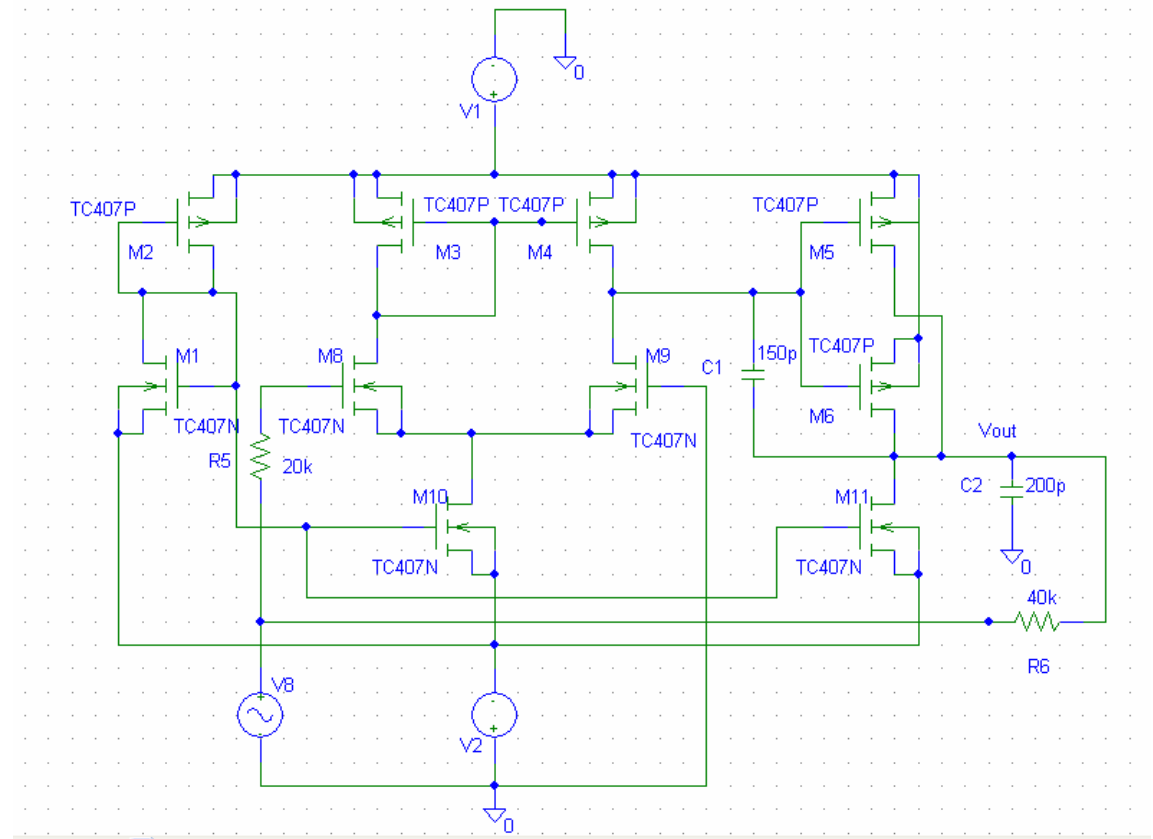
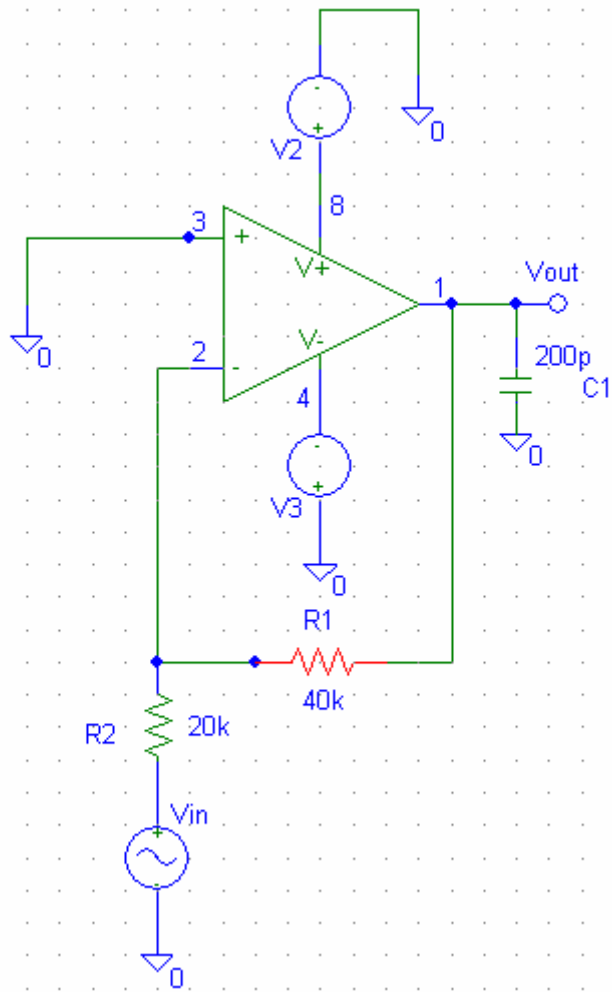


Fig. Inverting Amplifier

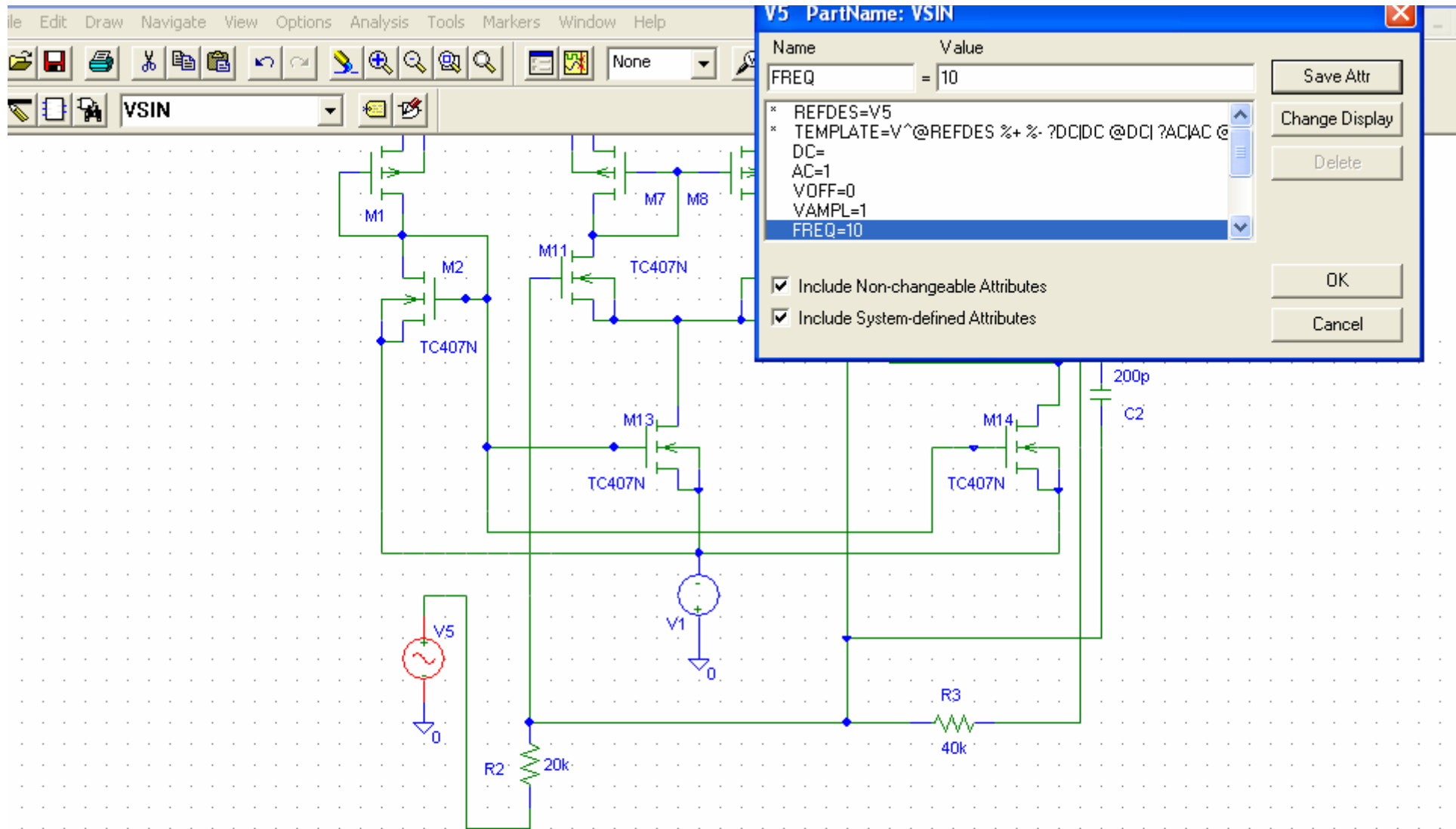


Fig. Vsin Set Up

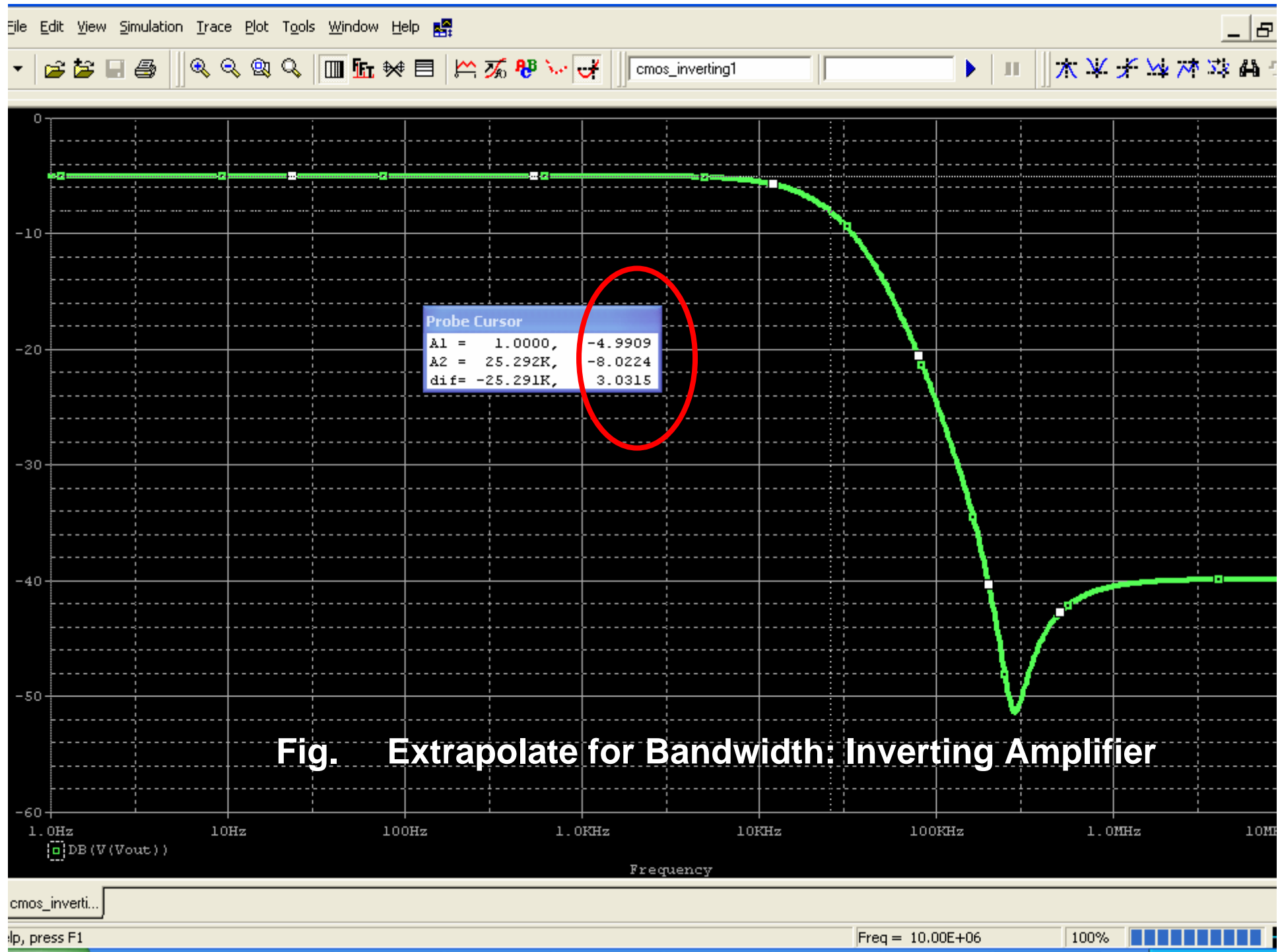


Fig. Extrapolate for Bandwidth: Inverting Amplifier

2.2 Inverting Amplifier

<u>Frequency(Hz.)</u>	1	10	100	1k	10k	100k	1M	10M
<u>Gain(dB)</u>								
<u>Phase Shift(Degree)</u>								

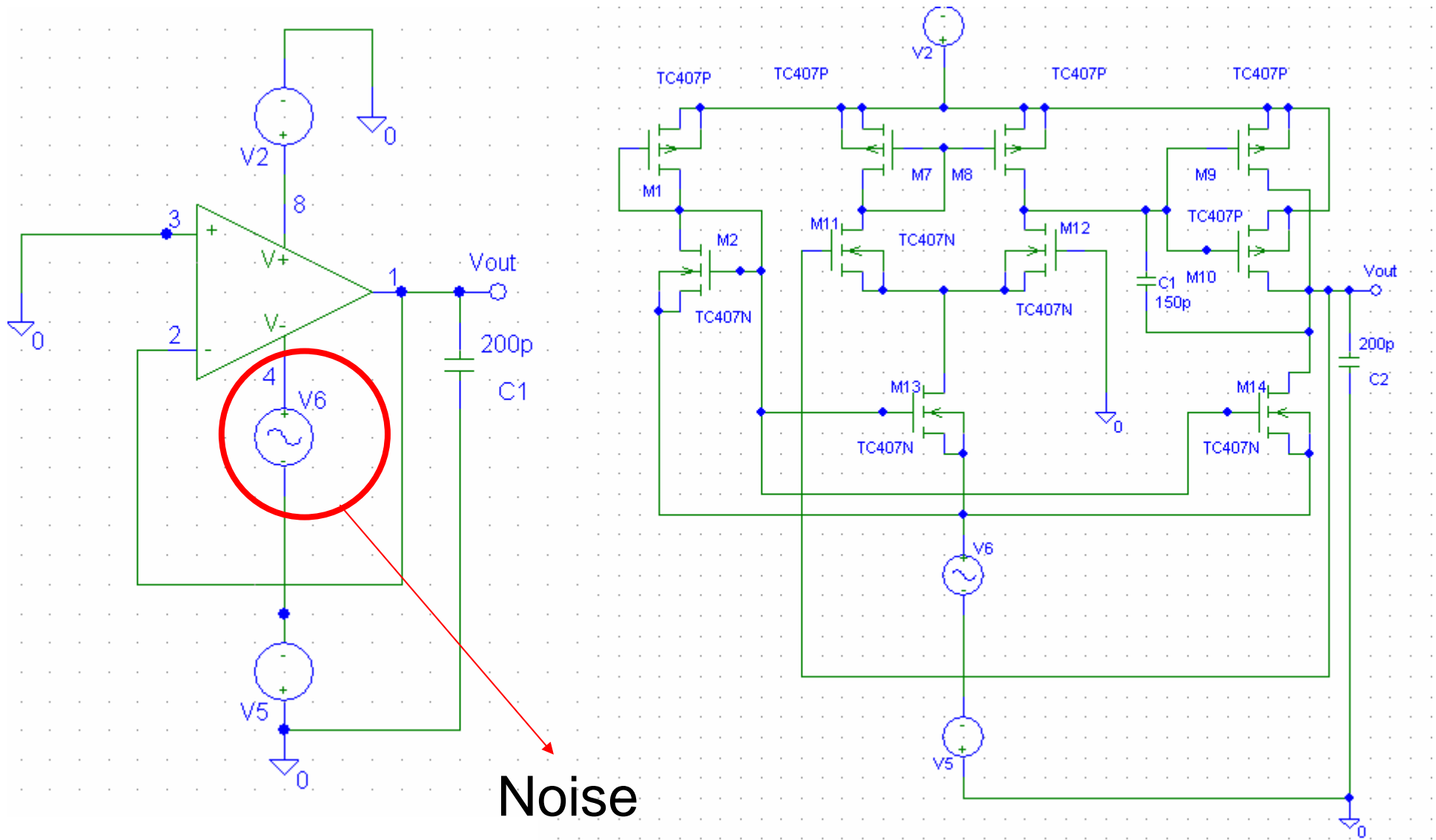
จาก Bode Plot ได้ค่า

Bandwidth(f_{-3dB}) Hz

Unity Gain Bandwidth(f_T) Hz

Fig. Record Test for Non-Inverting Amplifier Testing

**PSRR: POWER SUPPLY
REJECTION RATIO**



Noise

Fig. PSRR Testing

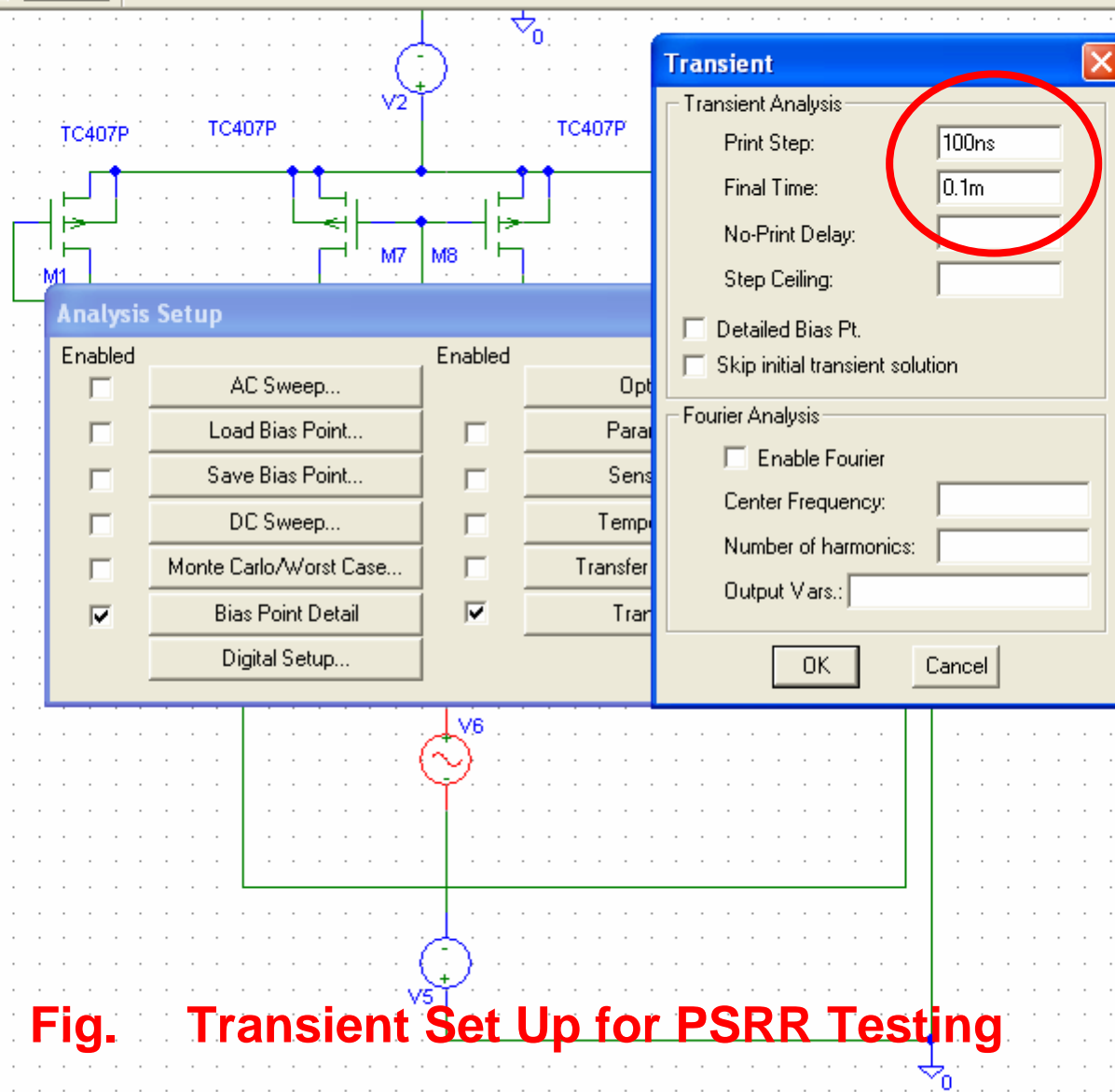
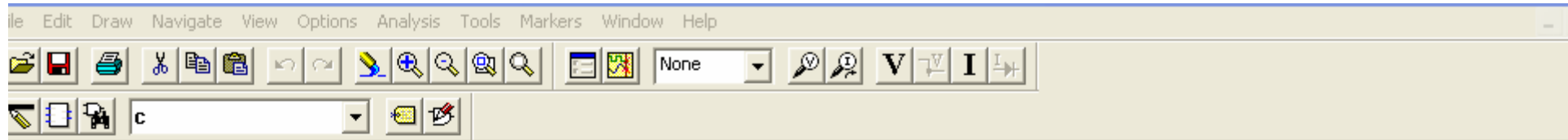
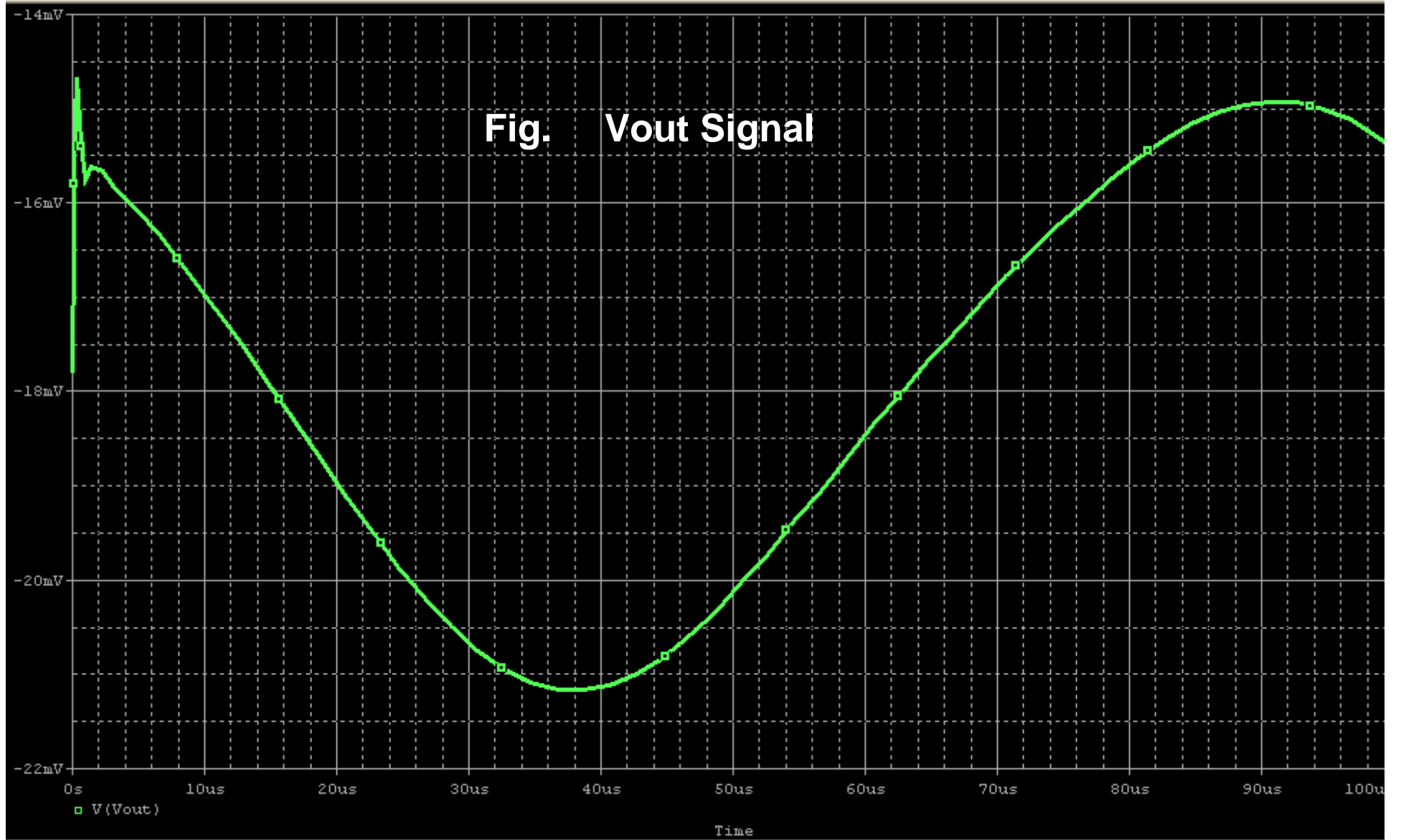
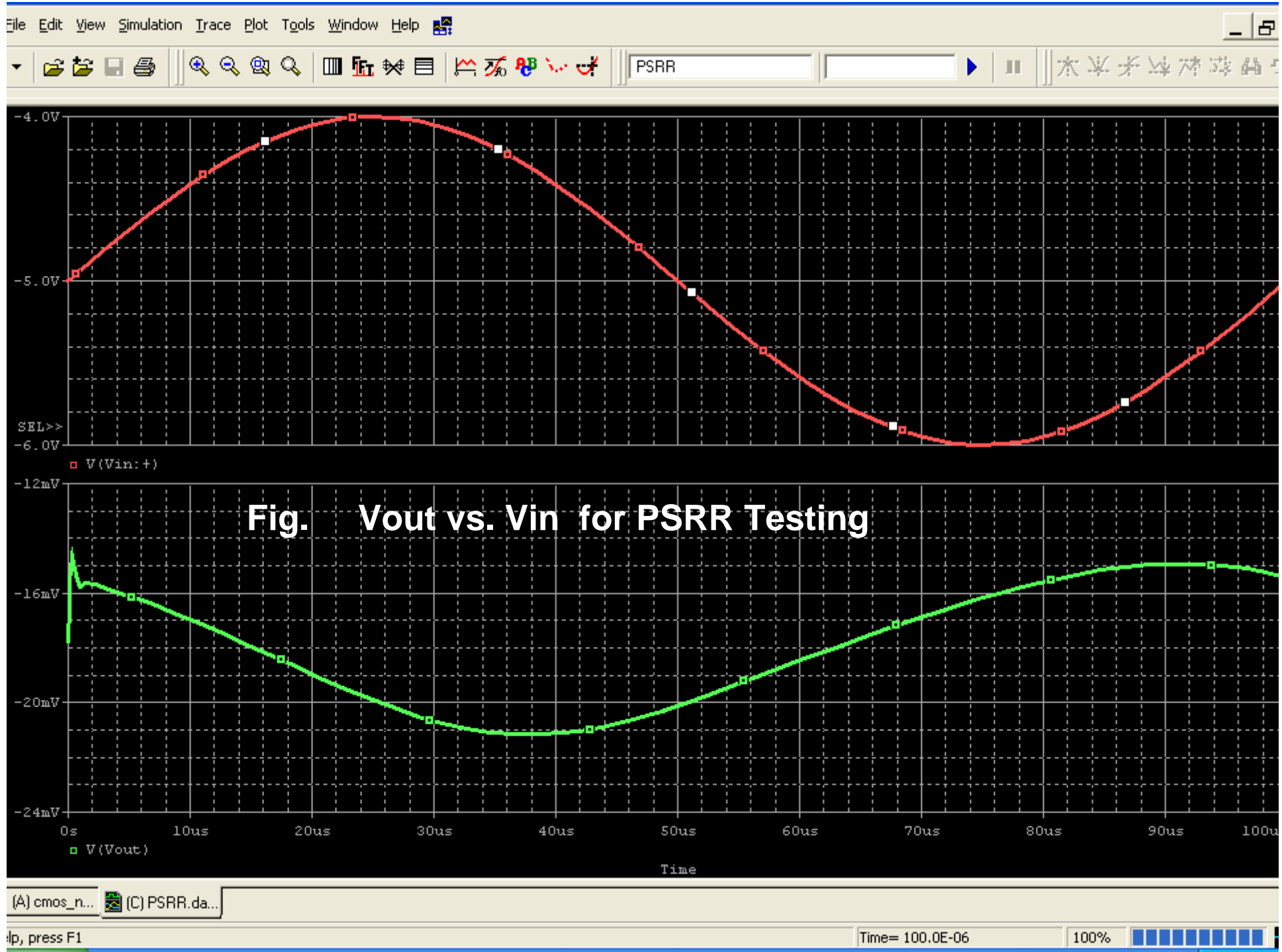


Fig. Transient Set Up for PSRR Testing





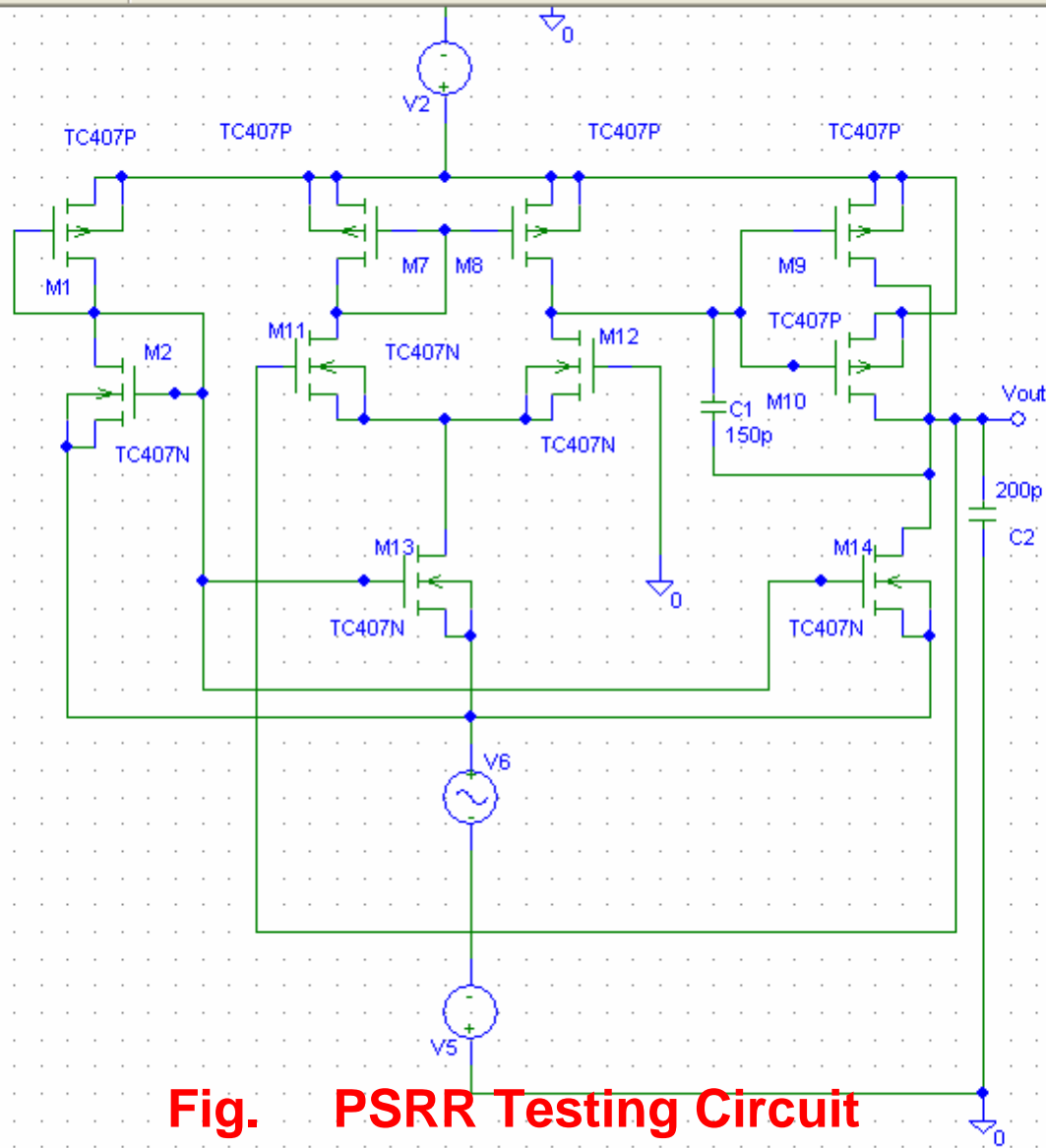
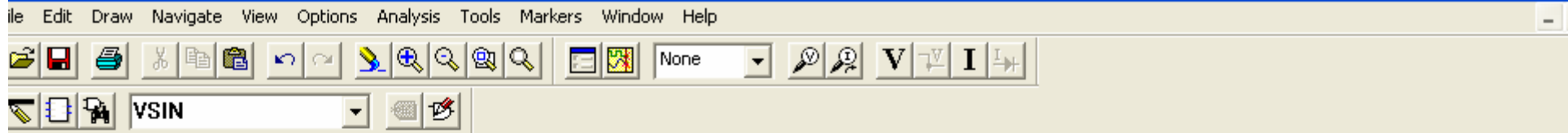


Fig. PSRR Testing Circuit

การทดลองที่ 3: คุณสมบัติในการขจัดสัญญาณรบกวนที่ผ่านเข้าทางไฟเลี้ยงของ Op Amp(PSRR)

ขนาดของสัญญาณ input(peak to peak) =*Volt*

ขนาดของสัญญาณ output(peak to peak) =*Volt*

ค่า PSRR(V_{out}/V_{in})

Fig. Record Test for PSRR Testing

END