PRACTICE PROBLEMS FOR *CMOS ANALOG CIRCUIT DESIGN*, 2ND EDITION

TECHNOLOGY

Problem 1 – (044430E3P5)

The following questions pertain to a standard npn BJT process.

a.) Give the relative doping levels of the emitter, base and collector for the vertical npn transistor.

Emitter doping >> base doping > collector doping

b.) Give the relative doping levels of the emitter, base and collector for the lateral pnp transistor.

Emitter doping ≈ Collector doping > base doping

c.) How is on vertical npn BJT electrically isolated from another?

By reverse biasing the collector-substrate pn junction

What is the purpose of the n^+ buried layer?

To reduce the value of the collector bulk resistance, *RC*.

d.) Why is a p^+ diffusion region used to contact the base?

To form an ohmic contact, otherwise a schottky diode is formed between the metal and the base region.

e.) What dimension is important for high β and f_t?

Small base width – the distance from the emitter to the collector

f.) Of the parasitic bulk resistances (*RE*, *RB*, and *RC*) for a vertical npn transistor, which is usually the largest? Smallest?

RC is the largest and*RE* is the smallest

g.) Of the depletion capacitors (C_{BE}, C_{BC}, and C_{CS}) for a vertical npn transistor, which is usually the largest? Smallest?

C_{CS} is largest and C_{BE} is the smallest

h.) Of the parasitic bulk resistances (*RE*, *RB*, and *RC*) for a lateral pnp transistor, which is usually the largest? Smallest?

RB is the largest and *RE* is the smallest

i.) Of the depletion capacitors (C_{BE}, C_{BC}, and C_{BS}) for a lateral pnp transistor, which is usually the largest? Smallest?

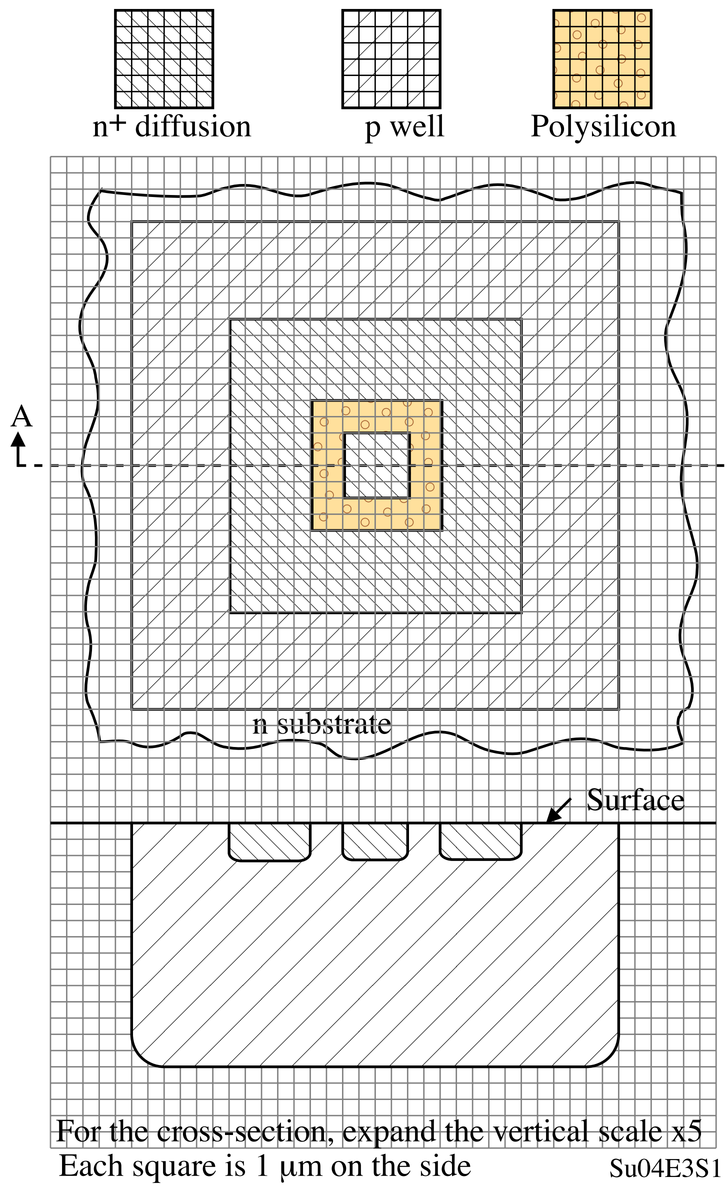
C_{BS} is the largest and C_{BE} is the smallest

LAYOUT AND PARASITICS

Problem 1 (044430E3P1)

A top view of a npn lateral BJT built in a typical *p*-well CMOS technology is shown. The metal connections have been left out for purposes of clarity. a.) Using the information from the table on the following page, carefully sketch a cross-section along the indicated line A-A'. Show only the structures that are diffused into the substrate and none of the structures above the substrate. b.) Find the zero-bias depletion capacitors C_{bc0}, C_{be0}, and C_{bs0} using the information on the previous page. c.) If the resistivity of the polysilicon used is 12.5x10^{-4} Ω·cm, what is its thickness?

a.) See plot below.



b.) C_{be0} =

$0.33\text{fF}/\mu\text{m}^2(16\mu\text{m}^2)$

$+0.9\text{fF}/\mu\text{m}(16\mu\text{m}) =$

$5.28\text{fF} + 14.4\text{fF}$

$= \underline{\underline{19.7\text{fF}}}$

$C_{bc0} = 0.33\text{fF}/\mu\text{m}^2(18^2\mu\text{m}^2 - 8^2\mu\text{m}^2) + 0.9\text{fF}/\mu\text{m}(4\text{x}18\mu\text{m}+4\text{x}8\mu\text{m})$

$= 85.8\text{fF} + 93.6\text{fF}$

$= \underline{\underline{179.4\text{fF}}}$

C_{bs0} =

$0.2\text{fF}/\mu\text{m}^2(900\mu\text{m}^2)$

$+1.6\text{fF}/\mu\text{m}(120\mu\text{m})$

$= 180\text{fF} + 192\text{fF}$

$= \underline{\underline{372\text{fF}}}$

c.) $\frac{\rho}{T} = 25\Omega/\text{sq.}$

$$\therefore T = \frac{\rho}{25\Omega} = \frac{12.5\text{x}10^{-4}}{25\Omega}$$

$T = \underline{\underline{0.5\mu\text{m}}}$

Some process parameters for a typical *p*-well CMOS process.

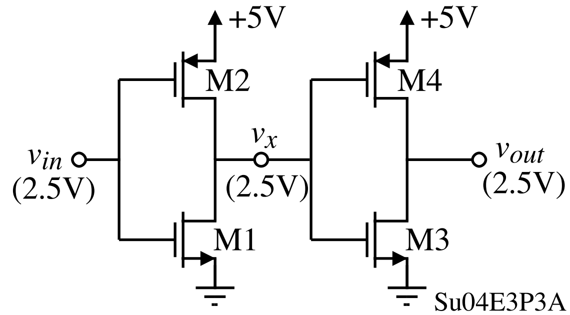
Physical feature sizes			
T_{ox} (gate oxide thickness)	500	±100	Å
Total lateral diffusion			
n-channel	0.45	±0.15	μm
p-channel	0.6	±0.3	μm
Diffusion depth			
n^+ diffusion	0.45	±0.15	μm
p^+ diffusion	0.6	±0.3	μm
p -well	3.0	±30%	μm
Capacitances			
C_{ox} (gate oxide capacitance, *n*- and *p*-channel)	0.7	±0.1	fF/μm^2
n^+ diffusion to *p*-well (junction, bottom)	0.33	±0.17	fF/μm^2
n^+ diffusion to *p*-well (junction, sidewall)	0.9	±0.45	fF/μm
p^+ diffusion to substrate (junction, bottom)	0.38	±0.12	fF/μm^2
n^+ diffusion to substrate (junction, sidewall)	1.0	±0.5	fF/μm
p-well to substrate (junction, bottom)	0.2	±0.1	fF/μm^2
p-well sidewall (junction, sidewall)	1.6	±1.0	fF/μm
Resistances			
Substrate	25	±20%	Ω-cm
p-well	5000	±2500	Ω/sq.
n^+ diffusion	35	±25	Ω/sq.
p^+ diffusion	80	±55	Ω/sq.
Poly	25	±25%	Ω/sq.
Metal 1 contact to p^+ or n^+ (2μm x 2μm)	4		Ω

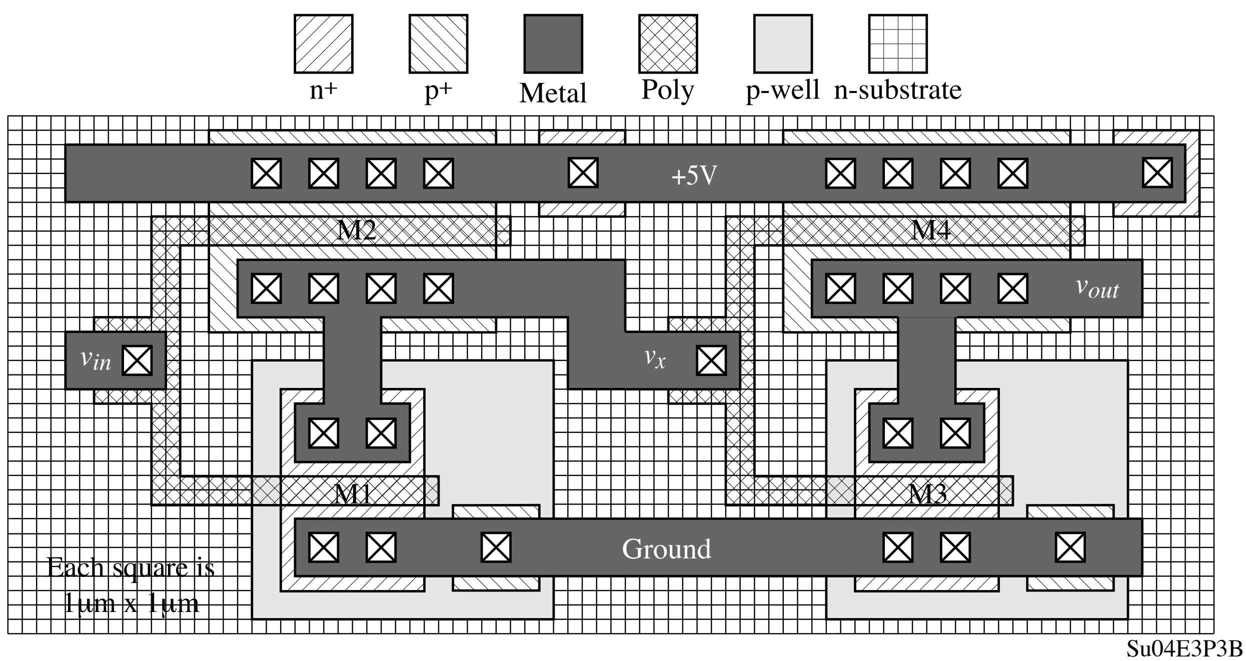
Problem 2 – (044430E3P3)

A CMOS inverter is shown along with the top view of the circuit layout assuming a *p*-well CMOS technology. If this inverter is driving and identical inverter with the same layout, find magnitude of the pole at the output of the first inverter (v_x) and the input of the second inverter which is equal to the reciprocal product of the sum of all capacitances connected to this node and the output resistance which is assumed to be 1MΩ. Express this pole magnitude in Hz. Use the table below to calculate the capacitances.

Type	P-Channel	N-Channel	Units
CGSO	220×10^{-12}	220×10^{-12}	F/m
CGDO	220×10^{-12}	220×10^{-12}	F/m
CGBO	700×10^{-12}	700×10^{-12}	F/m
CJ	560×10^{-6}	770×10^{-6}	F/m^2
CJSW	350×10^{-12}	380×10^{-12}	F/m
MJ	0.5	0.5	
MJSW	0.35	0.38	

Based on an oxide thickness of 140 Å or $C_{ox}=24.7 \times 10^{-4}$ F/m^2





$$\Sigma C_i = C_{gd1} + C_{gd2} + C_{bd1} + C_{bd2} + C_{gs3} + C_{gs4} + C_{gd3} + C_{gd4}$$

$$C_{gd1} = C_{gd3} = 220\text{x}10^{-12} \cdot 10\text{x}10^{-6} = 2.2\text{fF}$$

$$C_{gd2} = C_{gd2} = 220\text{x}10^{-12} \cdot 20\text{x}10^{-6} = 4.4\text{fF}$$

Next, we must find the area and perimeter of each drain.

AD1 = AD3 = 60µm^2 & PD1 = PD3 = 32µm

AD2 = AD4 = 120µm^2 & PD2 = PD4 = 52µm

Problem 2 – (044430E3P3) Continued

$$C_{bd1} = \frac{CJ\cdot AD1}{\left(1+\frac{2.5V}{2|\phi F|}\right)^{MJ}} + \frac{CJSW\cdot PD1}{\left(1+\frac{2.5V}{2|\phi F|}\right)^{MJSW}} = \frac{770x10^{-6}\cdot 60x10^{-12}}{\left(1+\frac{2.5V}{0.8}\right)^{0.5}} + \frac{380x10^{-12}\cdot 32x10^{-6}}{\left(1+\frac{2.5V}{0.8}\right)^{0.38}}$$

$C_{bd1} = C_{bd3}$ = 22.75fF + 7.10fF = 29.84fF

$$C_{bd2} = \frac{CJ\cdot AD2}{\left(1+\frac{2.5V}{2|\phi_F|}\right)^{MJ}} + \frac{CJSW\cdot PD2}{\left(1+\frac{2.5V}{2|\phi_F|}\right)^{MJSW}} = \frac{560x10^{-6}\cdot 120x10^{-12}}{\left(1+\frac{2.5V}{0.7}\right)^{0.5}} + \frac{350x10^{-12}\cdot 52x10^{-6}}{\left(1+\frac{2.5V}{0.7}\right)^{0.35}}$$

$C_{bd2} = C_{bd4}$ = 31.43fF + 10.69fF = 42.12fF

$C_{gs3} = C_{gd1} + 0.67(C_{ox}\cdot W_3\cdot L_3)$ = 2.2fF + 0.67(24.7x10^{-4}x20x10^{-12}) = 35.13fF

$C_{gs4} = C_{gd2} + 0.67(C_{ox}\cdot W_4\cdot L_4)$ = 4.4fF + 0.67(24.7x10^{-4}x40x10^{-12}) = 70.2fF

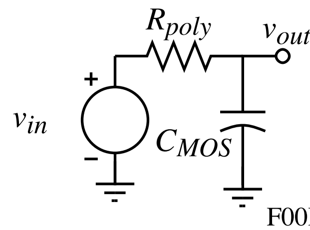
Now,

ΣC_i = 2.2fF + 4.4fF + 29.84fF + 42.12fF + 35.13fF + 70.2fF + 2.2fF + 4.4fF

= 190.45fF.

$$\therefore \quad |p| = \frac{1}{(\Sigma C_i)}10^6 = \frac{1}{190.45x10^{-15}10^6} = 5.25x10^6 \quad \rightarrow \quad |p| = \underline{\underline{835.7\ kHz}}$$

Problem 3 – (004430E2P3)



F00E2P2

A simple first-order filter shown is to be built with a polysilicon resistor and a MOS capacitor. The polysilicon resistor has a sheet resistance of 50Ω/sq. ± 30% and is 5μm wide. The MOS capacitor is 2fF/μm^2 ± 10%. The -3dB frequency of the lowpass filter is 1MHz. (a.) Choose the size of the resistor (the number of squares, *N*) to minimize the total area of the filter including both the resistor and the capacitor. Find the area of the resistor and the capacitor in μm^2 and their values. (b.) Using the worst-case tolerance of the resistor and capacitor, find the maximum and minimum -3dB frequencies.

Solution

(a.)

Value of R = 50Ω/sq.xN sq. = 50N Ω

Value of C = 2fF/μm^{2}xA_C μm^2 = 2A_C fF

Area of C = A_C

Area of R = A_R = 25μm^{2}xN = 25N μm^2

Total Area = A_T = (25N + A_C) μm^2

We know that the RC product is given as

$$RC = \frac{1}{2\pi x10^6} = (50N)(2A_C x10^{-15}) = NA_C x10^{-13}$$

$$\therefore\ A_C = \frac{1}{2\pi x10^{-7}N}$$

Thus, $A_T = 25N + \frac{1}{2\pi x10^{-7}N}$ $\rightarrow$ $\frac{dA_T}{dN} = 25 - \frac{1}{2\pi x10^{-7}N^2} = 0$

$\therefore\ N = \frac{1}{\sqrt{50\pi x10^{-7}}} = 252$ $\Rightarrow$ A_R = 252x25μm^2 = 6308μm^2 and A_C = 6308μm^2

Also, R_{poly} = R = 252x50Ω = 12.6kΩ and C_{MOS} = 6308μm^{2}x2fF/μm^2 = 12.6pF

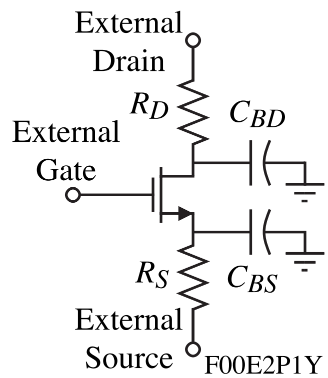
(b.)

$$\text{Maximum -3dB frequency} = \frac{1}{2\pi(0.7)(12.6k\Omega)(0.9)(12.6pF)} = 1.6\text{MHz}$$

$$\text{Minimum -3dB frequency} = \frac{1}{2\pi(1.3)(12.6k\Omega)(1.1)(12.6pF)} = 0.7\text{MHz}$$

Problem 4 - (004430E3P1)

A layout of a NMOS transistor is shown below. (a.) Find the values of *RD*, and *RS* in the schematic shown if the sheet resistance of the n$^+$ is 35 Ω/sq. and the resistance of a single contact is 1Ω. (b.) Find the values of C_{BD} and C_{BS} assuming the transistor is cutoff and the drain and source are at ground potential if *CJ* and *CJSW* for an NMOS transistor are 770x10^{-6} F/m^2 and 380x10^{-12}F/m. Assume the capacitors are lumped and appear on the source/drain side of the bulk resistors in part (a.). (c.) What is the W and L of this transistor? (d.) If the overlap capacitor/unit length is 220x10^{-12}F/m, what is C_{GD}?



F00E2P1Y

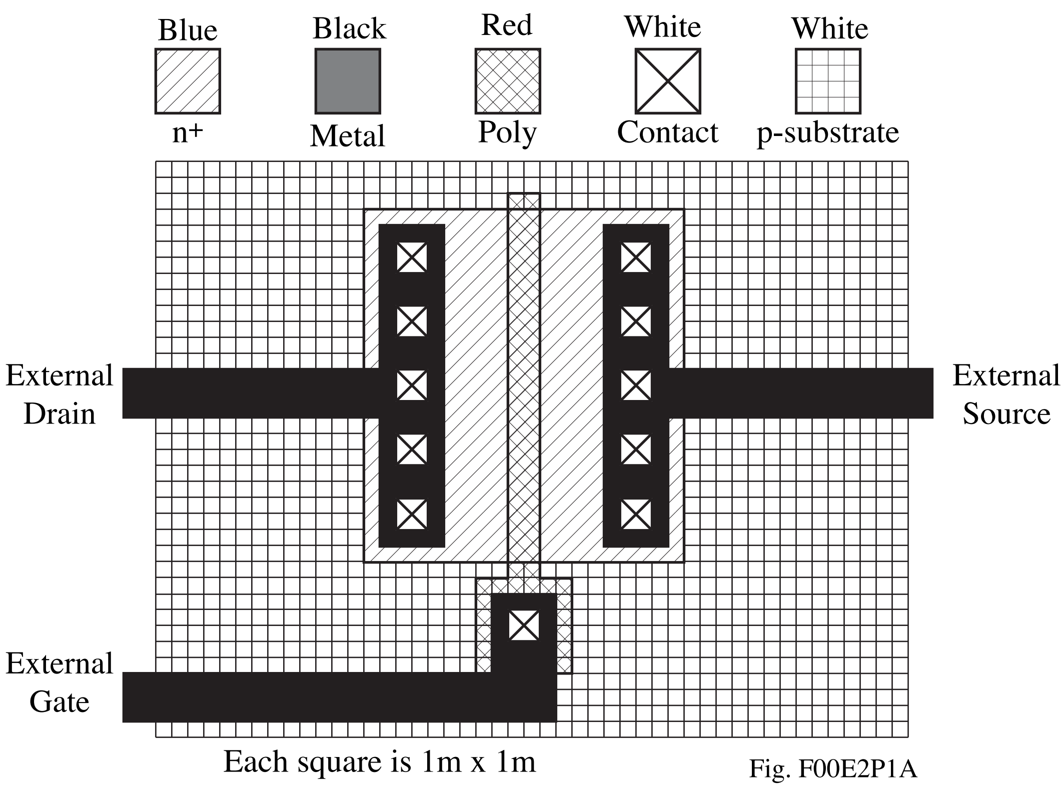


Fig. F00E2P1A

Solution

(a.) The area between the edge of the contacts to the polysilicon is 5µm by 22µm. This represents a bulk resistance of (5/22)x35 Ω/sq. = 7.95Ω. Adding 5 contacts in parallel gives *RD* = *RS* = 7.95Ω+0.2Ω = 8.15Ω.

(b.) The area or the source and drain are equal and are 9µm by 22µm or 198µm^2. The perimeter of the source and drain are 2(9µm+22µm) or 62µm. Therefore,

$$C_{BD} = C_{BS} = 770\text{x}10^{-6}\text{F/m}^2 \text{ x}198\text{x}10^{-12}\text{m}^2 + 380\text{x}10^{-12}\text{F/m x } 62\text{x}10^{-6}\text{m}$$

$$C_{BD} = C_{BS} = 152\text{fF} + 24\text{fF} = 176\text{fF}$$

(c.) The W = 22µm and the L = 2µm.

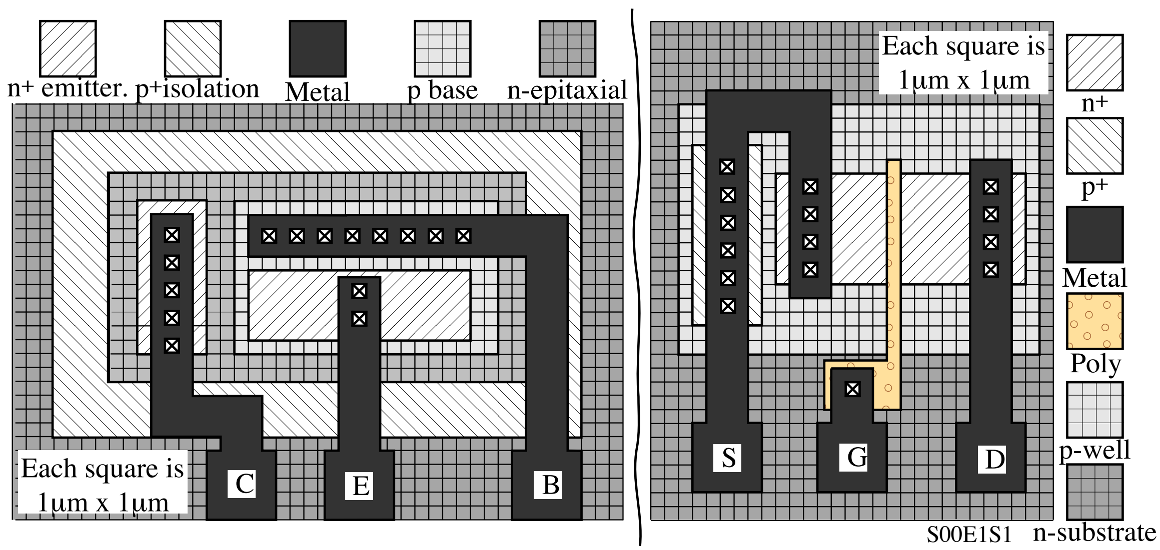
(d.) The overlap capacitor is

$$C_{GD} = 220\text{x}10^{-12}\text{F/m x } 22\text{x}10^{-6}\text{m} = 4.8\text{fF}$$

Problem 5 - (006412E1P1)

This problem concerns the influences of the physical implementations of BJT and MOS transistors on their small-signal electrical performance, namely, the transconductance parameter, g_m.

(a.) The layouts below are for an NPN bipolar transistor and an NMOS field-effect transistor. It is desired to increase the transconductance, g_m, by a factor of two. Show how to do this by changing the shape of *only one* geometry (i.e. rectangle) for each of the transistors. The resolution of any changes is restricted to 1μm. First describe in words how you would do this, then illustrate the changes on the layouts below. Use red ink on the layouts below to indicate the changes you would make. Identify which terminal is collector, base and emitter for the BJT and drain, gate and source for the MOSFET.



Solution

The g_m of a BJT is given as $g_m = \dfrac{I_C}{V_t} = \dfrac{I_s}{V_t}\exp(V_{BE}/V_t)$. Noting that I_s is proportional to the emitter area tells us that the way to double g_m is to double the emitter area as shown.

The g_m of the MOSFET is given as $\sqrt{\dfrac{2K_N{'}WI_D}{L}}$. g_m can only be doubled by quadrupling the Wi/L ratio. Since there is not enough room to make W 4 times larger, we make L four times smaller as shown.

(b.) If the dc currents in both NPN BJT and NMOS MOSFET are equal and 100μA, find the W/L ratio of the MOSFET that will make the small-signal transconductance of the MOSFET equal to the BJT. Assume that the large signal parameters for these transistors are $\beta_o = 100$, $V_t = 0.026\text{V}$, $K_N{'} = 100\mu\text{A/V}^2$ and $V_T = 0.7\text{V}$ (ignore the bulk effect and assume that $V_A = \infty$ and $\lambda_N = 0$).

Solution

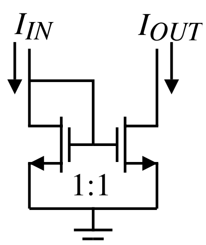
To make the transconductances equal means that

$$\sqrt{\frac{2K_N{'}WI_D}{L}} = \frac{I_C}{V_t} \quad \Rightarrow \quad \frac{W}{L} = \frac{I_D}{2K_N{'}V_t} = \frac{10^{-4}}{10^{-4}\cdot 0.026^2} = \underline{\underline{1479}}$$

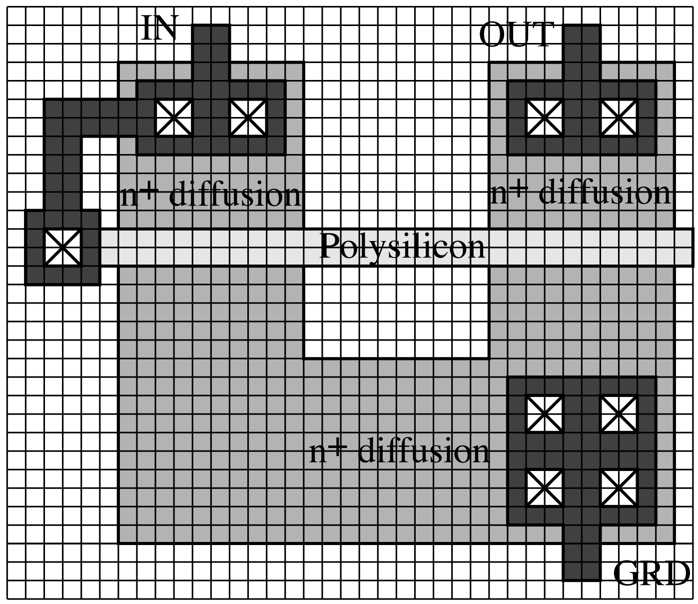
CURRENT MIRRORS

Problem 1 – (044430E3P2)

A CMOS 1:1 current mirror layout is shown. Assuming both transistors are in saturation and that $V_{DS1} = V_{DS2}$. a.) If I_{in} = 100μA, the value of I_{out} should be 100μA. Due to the layout, find the actual value of I_{out}. Use the information in the table for a typical CMOS process on the front page of this exam and assume that $K' = 100\mu A/V^2$ and $V_T = 0.5V$. b.) How would you improve the error caused by the layout?



Su04E3P2A

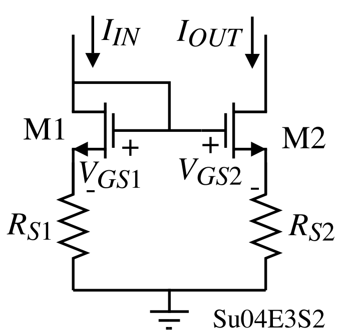


One square is 1µm x 1µm Su04E3P2

a.) We can see from the layout that the source bulk resistances are not equal. Designating these resistors as R_{S1} for M1 and R_{S2} for M2, we can find the values as follows.

R_{S1} = 35Ω/sq.(0.5 + 0.5 + 1 + 0.2) = 77Ω and R_{S2} = 35Ω/sq.(0.5 + 0.2) = 24.5Ω

Therefore the current mirror can be modeled as,



Su04E3S2

Thus,

$$\sqrt{\frac{2\cdot 100\mu A}{200\mu A/V^2\cdot 5}} + V_T + 100\mu A(77\Omega)$$

$$= \sqrt{\frac{2\cdot I_{OUT}}{200\mu A/V^2\cdot 5}} + V_T + 24.5\, I_{OUT}$$

Assuming the V_T's cancel, gives

$$0.640156 = 63.2456\sqrt{I_{OUT}} + 24.5\, I_{OUT}$$

or

$$I_{OUT} + 2.58145\sqrt{I_{OUT}} - 0.026129 = 0$$

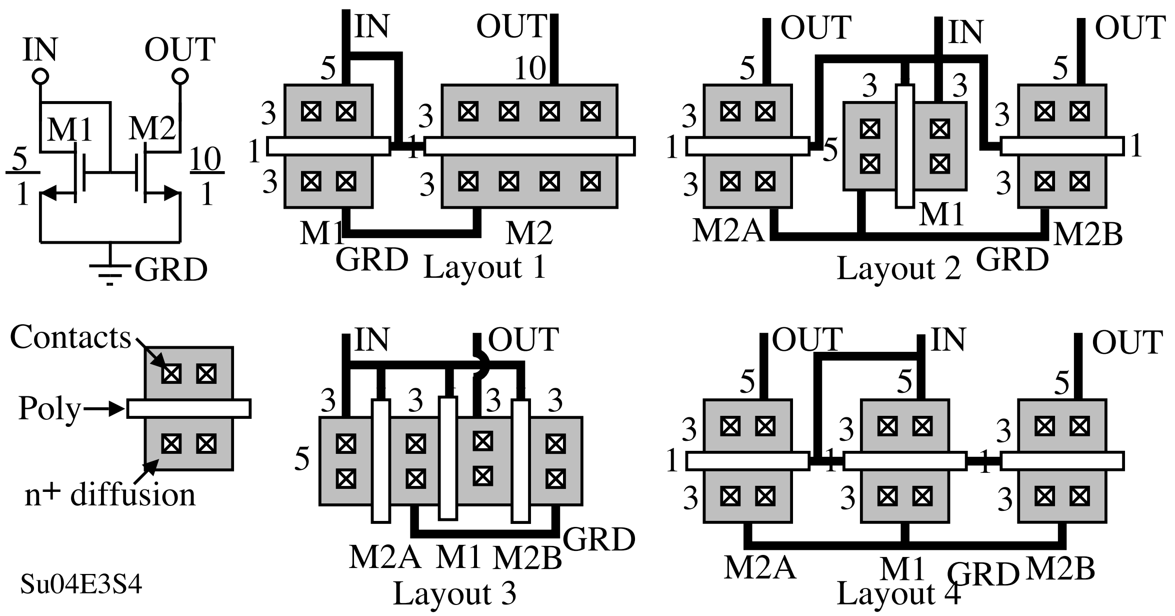
$$\sqrt{I_{OUT}} = -1.290726 \pm 1.30081 = 0.01008 \quad \rightarrow \quad I_{OUT} = \underline{\underline{102\mu A}}$$

b.) Move the GRD contacts and metal to the left 10 microns so that $R_{S1} = R_{S2}$.

Problem 2 – (044430E3P4)

Four different layouts for a CMOS 1:2 current mirror are shown. a.) Show how to connect the n^+ regions and the poly regions to form the current in mirror in each layout. Label the IN, OUT, and GRD nodes. (Just draw a line from the region to wherever to indicate the connection.) b.) Which of the four layouts has the most accurate current gain? Why? c.) Which of the four layouts is has the least accurate current gain from physical parasitic considerations? Why?

a.) See below.



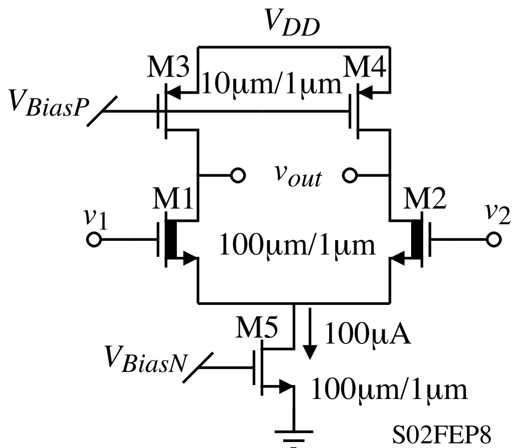
b.) Layout 4 is the most accurate because it uses a common centroid geometry, all gates are oriented in the same direction and it uses the replication principle.

c.) Layout 3 is the least accurate due to physical parasitics. The bulk source resistors of M1 and M2A are different than M2B. Also, the bulk-drain capacitors of M1 and M2B are different than M2A.

DIFFERENTIAL AMPLIFIERS

Problem 1 - (046412E3P4)

A differential CMOS amplifier using depletion mode input devices is shown. Assume that the normal MOSFETs parameters are K_N' =110V/μA^2, V_{TN} = 0.7V, λ_N=0.04V^{-1} and for the PMOS transistors are K_P' =110V/μA^2, V_{TP} = 0.7V, λ_P=0.04V^{-1}. For the depletion mode NMOS transistors, the parameters are the same as the normal NMOS except that V_{TN} = -0.5V. (a.) What is the maximum input common-mode voltage, V_{icm}^+(max)? (b.) What is the minimum input common-mode voltage, V_{icm}^-(min)? (c.) What value of V_{DD} gives an $ICMR = 0.5V_{DD}$?



Solution

(a.) $V_{icm}^+(\max) = V_{DD} - V_{SD3}(\text{sat}) - V_{DS1}(\text{sat}) + V_{GS1}(50\mu\text{A})$

$$i_D = \frac{\beta}{2}(V_{GS1} - V_{T1})^2 \rightarrow \qquad V_{GS1} = \sqrt{\frac{2i_D}{\beta}} + V_{T1} = V_{DS1}(\text{sat}) + V_{T1}$$

$$\therefore \quad V_{icm}^+(\max) = V_{DD} - V_{SD3}(\text{sat}) + V_{T1} = V_{DD} - \sqrt{\frac{2I_{D3}}{\beta_3}} + V_{T1}$$

$$V_{icm}^+(\max) = V_{DD} - 0.3015 - 0.5 = \underline{\underline{V_{DD} - 0.8015}}$$

(b.) $V_{icm}^-(\min) = V_{DS5}(\text{sat}) + V_{GS1}(50\mu\text{A}) = V_{DS5}(\text{sat}) + V_{DS1}(\text{sat}) + V_{T1}$

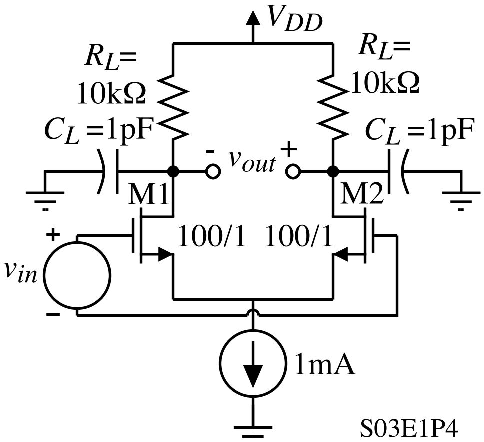
$$V_{icm}^-(\min) = \sqrt{\frac{2I_{D5}}{\beta_5}} + \sqrt{\frac{2I_{D1}}{\beta_1}} + V_{T1} = 0.1348 + 0.0953 - 0.5 = \underline{\underline{-0.2698\text{V}}}$$

(c.) $ICMR = V_{icm}^+(\max) - V_{icm}^-(\min) = V_{DD} - 0.8015 + 0.2698 = V_{DD} - 0.5317$

$\therefore \quad V_{DD} - 0.5317 = 0.5V_{DD} \qquad \rightarrow \qquad V_{DD} = 2(0.5317) = \underline{\underline{1.063\text{V}}}$

Problem 2 - (036412E1P3)

Find the numerical values of all roots and the midband gain of the transfer function v_{out}/v_{in} of the differential amplifier shown. Assume that $K_N' = 110\mu A/V^2$, $V_{TN} = 0.7V$, and $\lambda_N = 0.04V^{-1}$. The values of $C_{gs} = 0.2pF$ and $C_{gd} = 20fF$.



S03E1P4

Solution

A small-signal model appropriate for this circuit is shown.

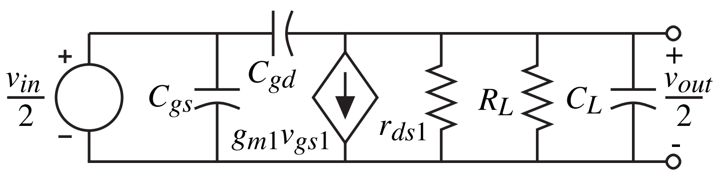


Fig. S03E1S4

Summing the currents at the output nodes gives,

$$g_{m1}v_{gs1} + sC_{gd}(v_{out}-v_{in}) + (g_{ds1} + G_L)v_{out} + sC_L\, v_{out} = 0$$

(Note: we are ignoring the fact that v_{out} and v_{in} should be divided by two since it makes no difference in the results and is easier to write.) Replacing v_{gs1} by v_{in} gives

$$-(g_{m1} - sC_{gd})v_{in} = [(g_{ds1} + G_L) + sC_L + sC_{gd}]\, v_{out}$$

$$\frac{v_{out}}{v_{in}} = \frac{-(g_{m1} - sC_{gd})}{s(C_L + C_{gd}) + (g_{ds1} + G_L)} = \left(\frac{-g_{m1}}{g_{ds1} + G_L}\right)\left(\frac{1 - \frac{sC_{gd}}{g_m}}{1 + s\frac{C_L + C_{gd}}{g_{ds1} + G_L}}\right)$$

$\therefore$ MGB $= -\, g_{m1}(r_{ds}||R_L)$, Zero $= \dfrac{g_m}{C_{gd}}$ and Pole $= -\dfrac{g_{ds} + G_L}{C_{gd} + C_L}$

$$g_m = \sqrt{2\cdot 110\cdot 100\cdot 500} = 3316.7\mu S \quad \text{and} \quad r_{ds} = \frac{1}{\lambda I_D} = \frac{25}{500\mu A} = 50\ k\Omega$$

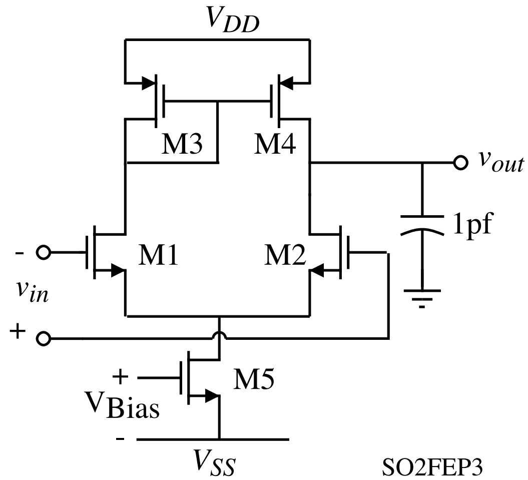
$\therefore$ MGB $= -3.3167mS\cdot(10k\Omega||50k\Omega) =$ <u>-27.64 V/V</u>

$$\text{Zero} = \frac{3.3167\text{x}10^{-3}}{20\text{x}10^{-15}} = \underline{1.658\text{x}10^{11}\ \text{radians/sec.}}$$

$$\text{Pole} = \frac{-1}{1.02\text{x}10^{-12}(10k\Omega||50k\Omega)} = \underline{-1.1176\text{x}10^{8}\ \text{radians/sec.}}$$

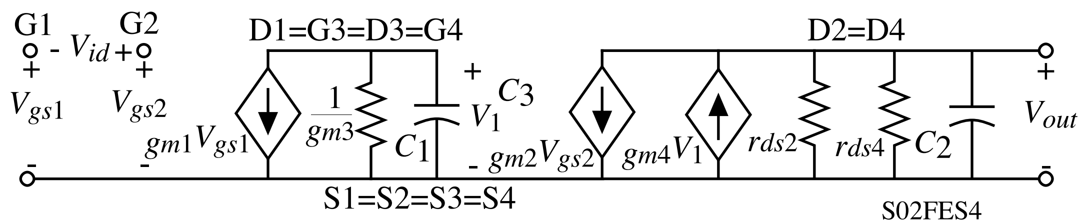
Problem 3 - (026412FE3)

A current mirror load, CMOS differential amplifier is shown. The current in M5 is 100μA. Assume the parameters of the NMOS transistors are K_N' =110V/μA^2, V_{TN} = 0.7V, λ_N =0.04V^{-1} and for the PMOS transistors are K_P' =110V/μA^2, V_{TP} = 0.7V, λ_P =0.04V^{-1}. (a.) Find the small-signal output resistance and voltage gain if the W/L ratio of M1 and M2 is 100μm/1μm. (b.) If the W/L ratio of M3 and M4 is 50μm/1μm and C_{ox} = 24.7x10^{-4}F/m^2, and the effective output capacitance is 1pF, find all roots of this amplifier (ignore the influence of C_{gd4}). (c.) What is the –3dB frequency in Hertz?



Solution

The small-signal model suitable for this problem is shown below.



C_1 = 2(0.667)(50x10^{-12}m^2)(24.7x10^{-4}F/m^2) = 0.1647pF $\quad g_{m3} = \sqrt{2\cdot 50\cdot 50\cdot 50}$ = 500μS

$$V_{out} = (g_{m4}V_1 - g_{m2}V_{gs2})Z_{out} = \left(\frac{g_{m4}g_{m1}V_{gs1}}{g_{m3} + sC_1} - g_{m2}V_{gs2}\right)Z_{out}$$

$$= \left[\left(\frac{1}{s\frac{C_1}{g_{m3}} + 1}\right)\left(\frac{-g_{m1}V_{in}}{2}\right) - \frac{g_{m2}V_{in}}{2}\right]\left(\frac{1}{sC_L + g_{ds2} + g_{ds4}}\right)$$

$$= -g_{md}\left(\frac{s\frac{C_1}{g_{m3}} + 2}{s\frac{C_1}{g_{m3}} + 1}\right)\left(\frac{1}{sC_2 + g_{ds2} + g_{ds4}}\right)\frac{V_{in}}{2} = -g_{md}\left(\frac{s\frac{C_1}{2g_{m3}} + 1}{s\frac{C_1}{g_{m3}} + 1}\right)\left(\frac{1}{sC_2 + g_{ds2} + g_{ds4}}\right)V_{in}$$

The small-signal ourput resistance and voltage gain is,

$$R_{out} = \frac{1}{g_{ds2}+g_{ds4}} = \frac{10^6}{50\ (0.05+0.04)} = \underline{\underline{222\text{k}\Omega}} A_{vd} = -g_{m1}R_{out}$$

$g_{m1} = g_{m1} = \sqrt{2\cdot 110\cdot 100\cdot 50}$ = 1.049mS $\Rightarrow A_{vd} = -g_{m1}R_{out}$ = (1.049)(222) = $\underline{\underline{-233\text{V/V}}}$

The roots are, $p_1 = -\dfrac{g_{m3}}{C_1} = -\dfrac{500\mu\text{S}}{0.1647\text{pF}}$ = $\underline{\underline{-3.036\text{x}10^9\text{rps}}}$, $z_1 = 2p_1$ = $\underline{\underline{-6.072\text{x}10^9\text{rps}}}$,

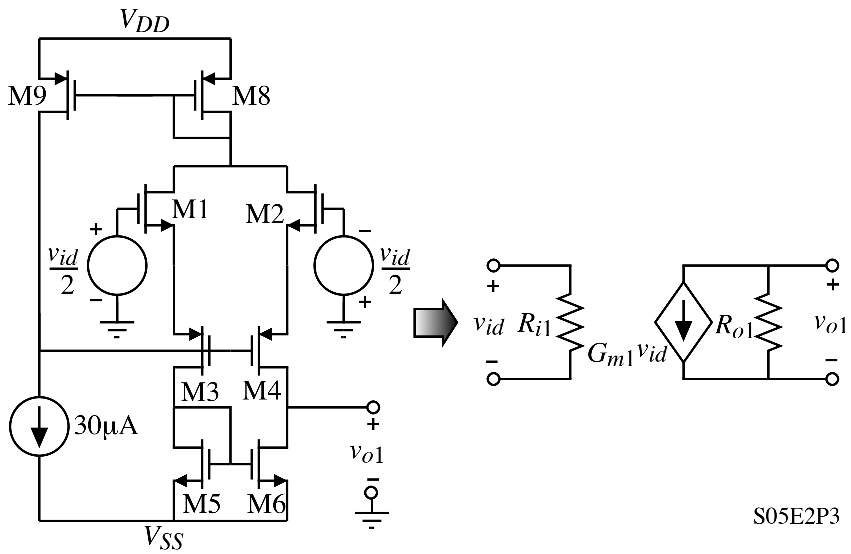
and $p_2 = -\dfrac{g_{ds2}+g_{ds4}}{C_2} = -\dfrac{1}{222\text{k}\Omega\cdot 1\text{pF}}$ = $\underline{\underline{-4.504\text{x}10^6\text{ rps}}}$ $\Rightarrow f_{-3\text{dB}} = \dfrac{4.504\text{x}10^6}{2\pi}$ = $\underline{\underline{717\text{kHz}}}$

Problem 4 - (056412E2P2)

The CMOS equivalent of a 741 op amp input stage is shown. If the transistor model parameters are $K_N' = 300\mu\text{A/V}^2$, $V_{TN} = 0.5\text{V}$, $\lambda_N = 0.02\text{V}^{-1}$ and $K_P' = 70\mu\text{A/V}^2$, $V_{TP} = -0.5\text{V}$, $\lambda_P = 0.04\text{V}^{-1}$ find the numerical values of R_{i1}, G_{m1}, and R_{o1} for this input stage if all W/L's of every transistor are 10.

Solution

The small-signal model for this problem is shown. First find the small-signal model parameters:



S05E2P3

$g_{m1} = g_{m2} = \sqrt{2\cdot 300\cdot 10\cdot 15}$
$=300\mu\text{S}$

$g_{m3} = g_{m4} = \sqrt{2\cdot 70\cdot 10\cdot 15} = 145\mu\text{S}$

$r_{ds1} = r_{ds2} = r_{ds5} = r_{ds6} = 50/15\mu\text{A} = 3.33\text{M}\Omega$ and $r_{ds3} = r_{ds4} = 25/15\mu\text{A} = 1.67\text{M}\Omega$

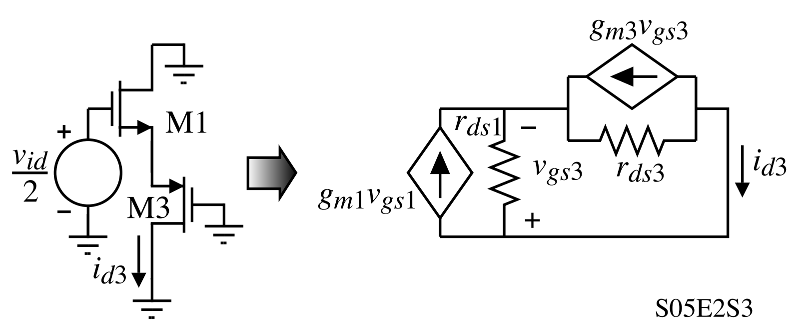
Summing currents:

$$g_{m1}v_{gs1}+\frac{v_{gs3}}{r_{ds1}}+\frac{v_{gs3}}{r_{ds3}}+g_{m3}v_{gs3} =$$

$$300v_{gs1}+0.3v_{gs1}+0.6v_{gs3}+145v_{gs3} = 0$$

$$300.3v_{gs1}+145.6v_{gs3} = 0 \quad \rightarrow$$

$$v_{gs1} = -0.485v_{gs3}$$



S05E2S3

Voltage loop through M1 and M3:

$$0.5g_{m1}v_{id} = v_{gs1} - v_{gs3} = -1.485v_{gs3}$$

$$\rightarrow \quad v_{gs3} = -0.337v_{id}$$

$$i_{d3} \approx -g_{m3}v_{gs3} = 0.337\cdot 145\mu\text{S}v_{id} = 48.82\mu\text{S } v_{id}$$

$$G_{m1}v_{id} = (i_{d3}+ i_{d4}) = 97.65\mu\text{S } v_{id} \qquad \therefore\ G_{m1} = \underline{\underline{97.65\mu\text{S}}} \qquad R_{i1} = \underline{\underline{\infty}}$$

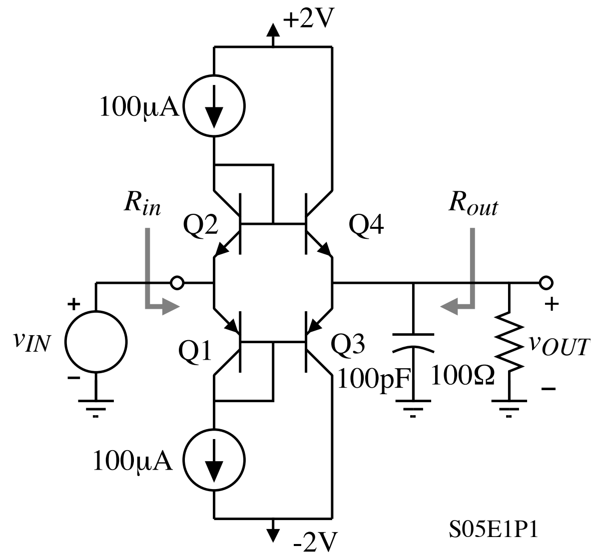
Ouput resistance:

$$R_{o1} = r_{ds6}||[(1/g_{m2})g_{m4}r_{ds4}] = 3.33\text{M}\Omega||0.807\text{M}\Omega = \underline{\underline{0.650\text{M}\Omega}}$$

OUTPUT AMPLIFIERS

Problem 1 (056412E1P1)

An emitter follower, push-pull output stage is shown. Assume that $\beta_N = \beta_P = 100$, $V_t = 25\text{mV}$, and $I_s = 10\text{fA}$.



a.) If the emitter areas of Q1 and Q2 are $10\mu\text{m}^2$, find the emitter area of Q3 and Q4 so that the collector current in Q3 and Q4 is 1mA when $v_{IN} = v_{OUT} = 0$.

b.) What is the ±peak output voltage of this amplifier? Assume the 100μA sources can have a minimum voltage across them of 0.2V.

c.) What is the ±slew rate of this amplifier in V/μs?

d.) What is the small-signal input and output resistance of this amplifier when $v_{IN} = v_{OUT} = 0$? (Do not include the load resistance in the output resistance.)

Solution

a.) $V_{EB1}+V_{BE2} = V_{BE4}+V_{EB3} \rightarrow \dfrac{I_{C1}{}^2}{I_{s1}I_{s2}} = \dfrac{I_{C3}{}^2}{I_{s3}I_{s4}} \rightarrow I_{s3} = I_{s4} = \dfrac{I_{C3}I_{s1}}{I_{C1}} = 10I_{s1}$

$\therefore A_{E3} = A_{E4} = 10A_{E1} = \underline{\underline{100\mu\text{m}^2}}$

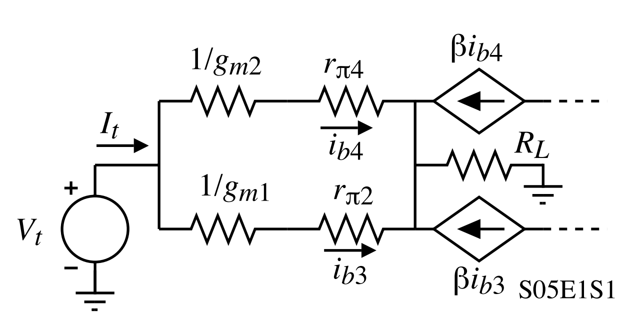
b.) $V_{peak} = \pm(100\mu\text{A})(1+\beta_o)R_L = \pm 100\mu\text{A}\cdot 101\cdot 100\Omega = \pm 1.01\text{V}$

Check to make sure this answer is okay. $V_{BE4} = V_t \ln\left(\dfrac{10.1\text{mA}}{10\text{fA}}\right) = 0.691\text{V}$

$\therefore$ Maximum swing is 2-0.691-0.2 = 1.109V so $V_{peak} = \underline{\underline{\pm 1.01\text{V}}}$

c.) $\pm SR = \left(\dfrac{10.1\text{mA}}{100\text{pF}}\right) = \underline{\underline{101\text{V}/\mu\text{s}}}$

d.) Small signal model:



$$V_t = \frac{I_t}{2}\left(\frac{1}{g_{m2}}+r_{\pi 4}\right) + R_L I_t(1+\beta_o)$$

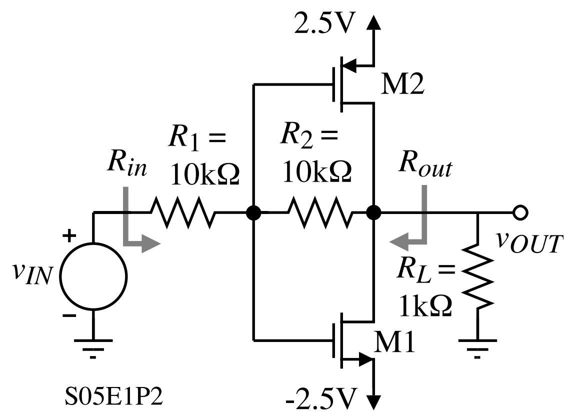
$$g_{m2} = \frac{100\mu\text{A}}{25\text{mV}} = \frac{1}{250\Omega}$$

$$g_{m4} = \frac{1\text{mA}}{25\text{mV}} = \frac{1}{25\Omega} \qquad R_{in} = 0.5[250+25(101)] + 101(100) = \underline{\underline{11.487\text{k}\Omega}}$$

$$R_{out} = 0.5\left[\frac{1}{g_{m4}} + \frac{1/g_{m2}}{1+\beta_o}\right] = 0.5[25 + (250/101)] = \underline{\underline{13.37\Omega}}$$

Problem 2 (056412E1P2)

Find the value for the small-signal output resistance R_{out} ignoring R_L and the value of the small-signal input resistance for the amplifier shown. Let the dc currents through M1 and M2 be 500μA, W_1/L_1 = 100μm/1μm and W_2/L_2 = 200μm/1μm. Assume the parameters of the NMOS transistors are K_N'=110V/μA^2, V_{TN} = 0.7V, and for the PMOS transistors are K_P'=50V/μA^2, V_{TP} = -0.7V. Ignore r_{ds1} and r_{ds2}.



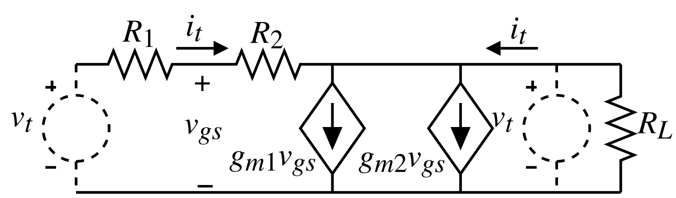
S05E1P2

Solution

Calculating the small-signal parameters gives,

$$g_{m1} = \sqrt{2 \cdot 110 \cdot 500 \cdot 100} = 3.316\text{mS},\ g_{m2} = \sqrt{2 \cdot 50 \cdot 500 \cdot 200} = 3.162\text{mS}$$

The small-signal model is given as,



S05E1S2

For R_{out}, sum the currents at the output (with the LH v_t =0) to get,

$$i_t = v_t\left[\frac{1}{R_1+R_2} + \frac{g_{m1}+g_{m2}}{2}\right] \quad \rightarrow \quad R_{out} = \frac{v_t}{i_t} = \left[\frac{1}{R_1+R_2} + \frac{g_{m1}+g_{m2}}{2}\right]^{-1} = \underline{\underline{308\Omega}}$$

For R_{in}, remove the RH v_t and write a loop equation at the input to get,

$$v_t = i_t(R_1 + R_2) + (i_t - g_{m1}v_{gs} - g_{m2}v_{gs})R_L = i_t(R_1 + R_2 + R_L) - (g_{m1} + g_{m2})v_{gs}$$

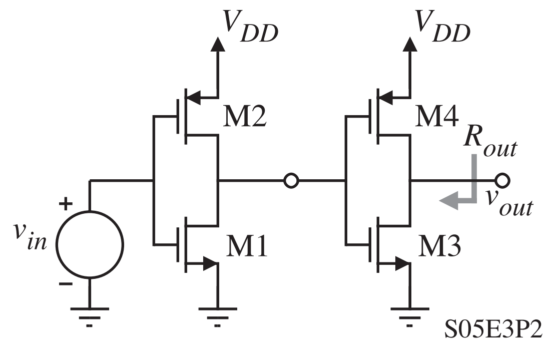
But $v_{gs} = v_t - i_t R_1$ which gives,

$$R_{in} = \frac{v_t}{i_t} = \frac{R_1+R_2+R_L+(g_{m1}+g_{m2})R_LR_1}{1+(g_{m1}+g_{m2})R_L} = \frac{201\text{k}\Omega+(3.316+3.162)(1)(100\text{k}\Omega)}{1+(3.316+3.162)(1)}$$

$$R_{in} = \underline{\underline{113.5\text{k}\Omega}}$$

Problem 3 – (056412E3P1)

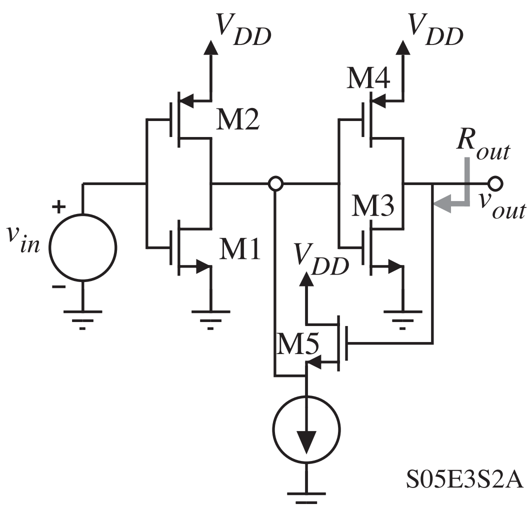
A simple amplifier consisting of two cascaded CMOS inverters is shown. By using one transistor (either NMOS or PMOS) and ideal current sources and batteries as necessary, show how you would reduce the output resistance to as small as possible. Estimate the output resistance of your circuit assuming that all transistors (those in the amplifier and the one you use) have the same value of g_m and r_{ds}. Further assume, that the CMOS inverters are operating in class AB.



S05E3P2

Solution

There are two possibilities which will be examined below.

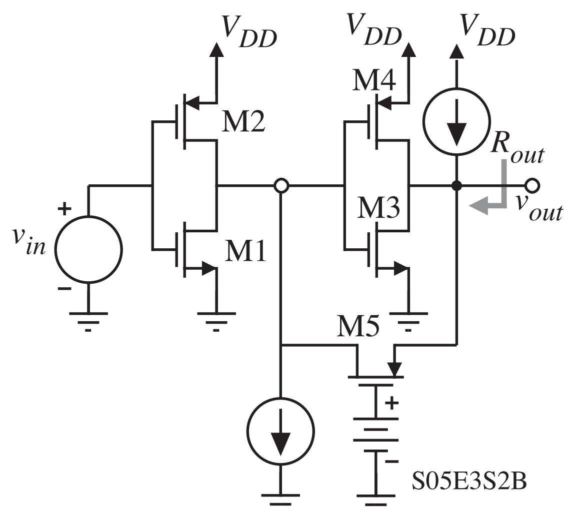


S05E3S2A

$R_{out}(\text{no fb.}) = 0.5r_{ds}$

Loop gain $\approx 1\cdot g_m r_{ds}$

$$R_{out}(\text{fb.}) \approx \frac{0.5r_{ds}}{g_m r_{ds}} = \frac{1}{2g_m}$$



S05E3S2B

$R_{out}(\text{no fb.}) \approx 1/g_m$

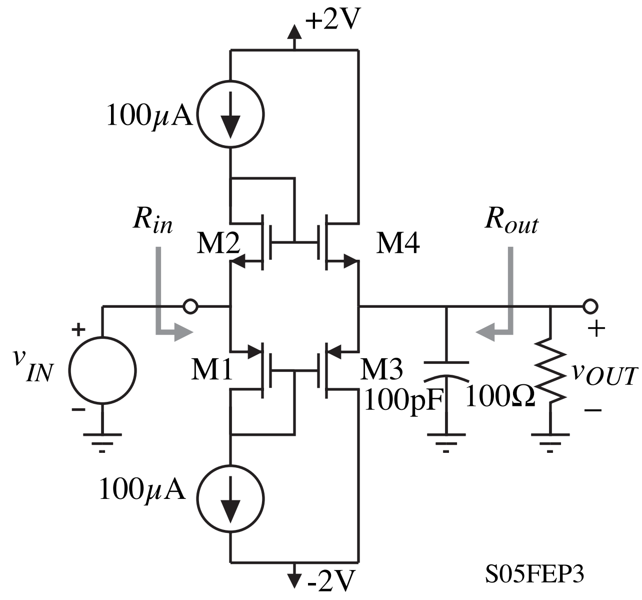
Loop gain $\approx 2\, g_m(r_{ds}/3) = 0.667\, g_m r_{ds}$

$$R_{out}(\text{fb.}) \approx \frac{1/g_m}{0.667 g_m r_{ds}} = \frac{3}{2g_m{}^2 r_{ds}}$$

Therefore, the solution on the right has a low resistance by the amount of $3/g_m r_{ds}$.

Problem 4 – (056412FE3)

A source follower, push-pull output stage is shown. Assume the parameters of the NMOS transistors are K_N'=110V/μA^2, V_{TN} = 0.7V, λ_N=0.04V^{-1} and for the PMOS transistors are K_P'=50V/μA^2, V_{TP} = -0.7V, λ_P=0.05V^{-1}.



a.) If W_1/L_1 = W_2/L_2 = 10, find the W_3/L_3 and W_4/L_4 so that the drain current in M3 and M4 is 1mA when $v_{IN} = v_{OUT} = 0$.

b.) What is the ±peak output voltage of this amplifier? Assume the 100μA sources can have a minimum voltage across them of 0.2V.

c.) What is the ±slew rate of this amplifier in V/μs?

d.) What is the small-signal input and output resistance of this amplifier when $v_{IN} = v_{OUT} = 0$? (Do not include the load resistance in the output resistance.)

Solution

a.) With $v_{IN} = v_{OUT} = 0$, the W/L ratios of M3 and M4 are given by the current ratios. Thus, $W_3/L_3 = W_4/L_4 = \underline{\underline{100}}$.

b.) The current limit due to 1mA is ±1V. Check to see if voltage limit is less.

$$V_{GS4}(1\text{mA}) = \sqrt{\frac{2\cdot 1\text{mA}}{110\cdot 100}} + 0.7 = 0.426 + 0.7 = 1.126\text{V}$$

$$V_{out}(\max) = 2 - 0.2 - 1.126 = \underline{\underline{0.674\text{V}}}$$

$$V_{GS3}(1\text{mA}) = \sqrt{\frac{2\cdot 1\text{mA}}{50\cdot 100}} + 0.7 = 0.632 + 0.7 = 1.332\text{V}$$

$$V_{out}(\min) = 2 - 0.2 - 1.332 = \underline{\underline{0.467\text{V}}}$$

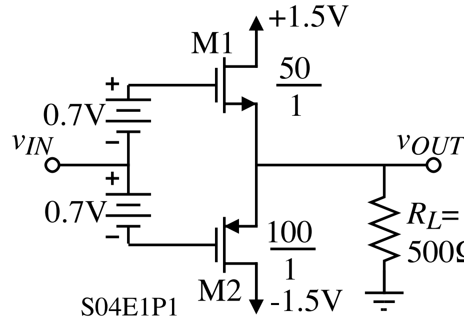
c.) The slew rate is

$$\pm SR = \frac{1\text{mA}}{100\text{pF}} = \underline{\underline{10\text{V}/\mu\text{s}}}$$

d.) $R_{in} = \infty$. $\quad R_{out} = \dfrac{1}{g_{m3} + g_{m4}} \quad g_{m4} = \sqrt{2\cdot 110\cdot 1000\cdot 100}\ \mu\text{S} = 4.69\text{mS}$

$$g_{m3} = \sqrt{2\cdot 50\cdot 1000\cdot 100}\ \mu\text{S} = 3.162\text{mS} \qquad R_{out} = \frac{1000}{3.162 + 4.69} = \underline{\underline{127\Omega}}$$

Problem 5 - (046412E1P1)

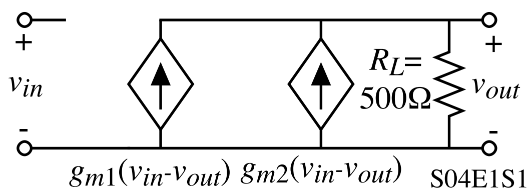


A push-pull follower is shown with a 500Ω load. Assume that the MOSFETs have the following model parameters: . $K_N' = 100\mu A/V^2$, $V_{TN} = 0.5V$, and $K_P' = 50\mu A/V^2$, $V_{TP} = -0.5V$. Ignore the bulk effects and assume $\lambda = 0$.

a.) Find the small signal voltage gain and the output resistance (not including R_L) for the conditions of part a.) if the dc current in M1 and M2 is $100\mu A$.

b.) What is the output voltage when $v_{IN} = 0.5V$?

Solution



a.) The small-signal model is given as shown

where $g_{m1} = \sqrt{2K_N'(W_1/L_1)I_{D1}} = \sqrt{2\cdot 100\cdot 50\cdot 100}$

$$g_{m1} = 1\text{mS},\ g_{m2} = \sqrt{2\cdot 50\cdot 100\cdot 100} = 1\text{mS}$$

Summing currents at the output node gives,

$$g_{m1}(v_{in} - v_{out}) + g_{m2}(v_{in} - v_{out}) = G_L v_{out}$$

$$\therefore \quad \frac{v_{out}}{v_{in}} = \frac{g_{m1} + g_{m2}}{g_{m1} + g_{m2} + G_L} = \frac{1+1}{1+1+2} \underline{\underline{= 0.5V/V}} \quad \text{and} \quad R_{out} = \frac{1}{g_{m1}+g_{m2}} = \frac{1}{2\text{mS}} = \underline{\underline{500\Omega}}$$

b.) Under the condition of $v_{IN} = 0.5V$, the gate voltages are

$$V_{G1} = 0.5V+0.7V = 1.2V \qquad \text{and} \qquad V_{G1} = 0.5V-0.7V = -0.2V$$

We know that the output voltage can be expressed as $V_{OUT} = (I_1\text{-}I_2)0.5k\Omega$ where I_1andI_2 are the dc currents in M1 and M2.

Next we need to make an assumption about the operating region of the two transistors. Let us assume that M1 is saturated and M2 is cutoff. Therefore, $I_2 = 0$ and

$$I_1 = 0.5(100)(50)[1.2\text{-}V_{OUT} - 0.5)]^2\ (\mu A) = 2.5(0.7\text{-}V_{OUT})^2\ (mA)$$

$$\therefore \quad V_{OUT} = (I_1)0.5k\Omega = 1.25(0.7\text{-}V_{OUT})^2 \rightarrow 0.8V_{OUT} = 0.49 - 1.4V_{OUT} + V_{OUT}^2$$

The resulting quadratic, $V_{OUT}^2 - 2.2V_{OUT} + 0.49 = 0$ gives

$$V_{OUT} = 1.19\pm 0.5\sqrt{2.2^2\text{-}4(0.49)} = 1.1 \pm 0.5(2.880) = 1.1\pm 0.845 = \underline{\underline{0.252V}}$$

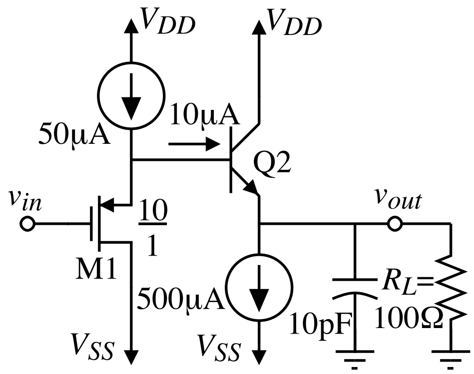
Check the regions of M1 and M2.

M1: $V_{DS1} = 1.5\text{-}0.252 = 1.25V > V_{GS1}\text{-}V_{TN} = 1.2\text{-}0.5 = 0.7$ $\therefore$ M1 is saturated.

M2: $V_{SG2} = 0.252 - (-0.2) = 0.452 < |V_{TP}| = 0.5$ $\therefore$ M2 is cutoff

Problem 6 - (046412FE1)

An output stage is shown. Assume the parameters of the NMOS transistors are K_N'=110μA^2/V, V_{TN} = 0.7V, λ_N=0.04V^{-1}, the PMOS transistors are K_P'=50V/μA^2, V_{TP} = -0.7V, λ_P=0.05V^{-1} and the lateral npn BJT has a current gain of β_F = 50 and V_t = 25mV. Find the small-signal output resistance (not including R_L), the small-signal voltage gain (ignore the bulk effect on M1), and the large signal slew rate (plus and minus) if a 10pF capacitor is connected to the output.



F04FES1A

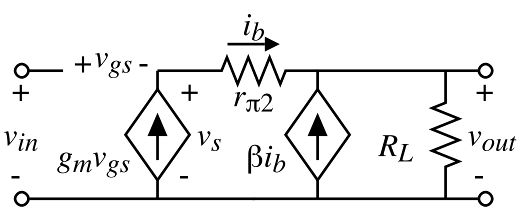
Solution

Model parameters:

M1: $g_{m1} = \sqrt{2\cdot 40\cdot 10\cdot 50} = 0.2\text{mS}$

Q2: $g_{m2} = \dfrac{500\mu\text{A}}{25\text{mV}} = 20\text{mS}$ and $r_{\pi 2} = \dfrac{51}{20\text{mS}} = 2.55\text{k}\Omega$

Small-signal model:



S04FES1

$$R_{out} = \frac{r_{\pi 2}+(1/g_{m1})}{1+\beta} = \frac{2.55\text{K}+5\text{K}}{51} = \underline{\underline{148\Omega}}$$

$$\frac{v_{out}}{v_{in}} = \left(\frac{v_{out}}{i_b}\right)\left(\frac{i_b}{v_{gs}}\right)\left(\frac{v_{gs}}{v_{in}}\right)$$

$$= [(1+\beta)R_L](g_{m1})\left(\frac{1}{1+g_{m1}[r_{\pi 2}+(1+\beta)R_L]}\right)$$

$$\frac{v_{out}}{v_{in}} = \left(\frac{g_{m1}[(1+\beta)R_L]}{1+g_{m1}[r_{\pi 2}+(1+\beta)R_L]}\right) = \frac{0.2\text{mS}\cdot 101\cdot 100\Omega}{1+0.2\text{mS}(2.55\text{k}\Omega+5.1\text{k}\Omega)} = \frac{1.20}{2.53} = \underline{\underline{0.403\text{V/V}}}$$

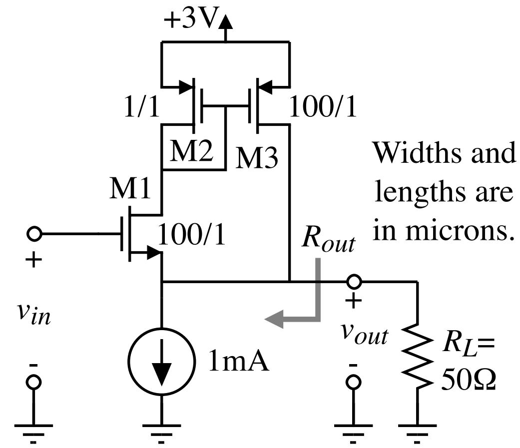
Slew rates:

$$SR^+ = \frac{50\mu\text{A}(51) - 50\mu\text{A}}{10\text{pF}} = \underline{\underline{205\ \text{V}/\mu\text{s}}}$$

$$SR^- = \frac{500\mu\text{A}}{10\text{pF}} = \underline{\underline{-50\ \text{V}/\mu\text{s}}}$$

Problem 7 - (036412E1P1)

Find an algebraic expression for the voltage gain, v_{out}/v_{in}, and the output resistance, R_{out}, of the source follower shown in terms of the small-signal model parameters, g_m and R_L (ignore r_{ds}). If the bias current is 1mA find the numerical value of the voltage gain and the output resistance. Assume that $K_N' = 110\mu A/V^2$, $V_{TN} = 0.7V$, and $K_P' = 50\mu A/V^2$, $V_{TP} = -0.7V$.



S03E1P1

Solution

A small-signal model for this circuit is shown below neglecting r_{ds} of the transistors.

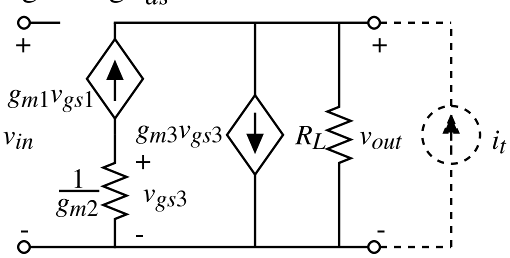


Fig. S03E1S1

Summing currents at the output node gives,

$$g_{m1}v_{gs1} = g_{m3}v_{gs3} + G_Lv_{out}$$

Also, $v_{gs3} = -\, g_{m1}v_{gs1}(1/g_{m2})$

$$\therefore \quad g_{m1}v_{gs1} = g_{m3}\left(-\frac{g_{m1}}{g_{m2}}\right)v_{gs1} + G_Lv_{out}$$

$$g_{m1}v_{gs1}\left(1+\frac{g_{m3}}{g_{m2}}\right) = G_Lv_{out} \quad \rightarrow \quad g_{m1}(v_{in}-v_{out})\left(1+\frac{g_{m3}}{g_{m2}}\right) = G_Lv_{out}$$

$$\therefore \quad \boxed{\frac{v_{out}}{v_{in}} = \frac{g_{m1}\left(1+\frac{g_{m3}}{g_{m2}}\right)}{g_{m1}\left(1+\frac{g_{m3}}{g_{m2}}\right)+G_L}}$$

Setting $v_{in} = 0$ and applying i_t and solving for v_{out} and ignoring R_L gives,

$$i_t = g_{m3}v_{gs3} + g_{m1}v_{out} = g_{m3}\left(\frac{g_{m1}}{g_{m2}}\right)v_{out} + g_{m1}v_{out}$$

$$\therefore \quad \frac{v_{out}}{i_t} = \boxed{R_{out} = \frac{1}{g_{m1}\left(1+\frac{g_{m3}}{g_{m2}}\right)}}$$

Note that the 1mA splits between M1(M2) and M3 in a ratio of 1 to 100. Therefore, $I_{D1} = I_{D2} = 9.9\mu A$ and $I_{D3} = 990.1\mu A$.

$\therefore \; g_{m1} = \sqrt{2\cdot 110\cdot 100\cdot 9.9} = 466.71\mu S$, $g_{m2} = \sqrt{2\cdot 50\cdot 1\cdot 9.9} = 31.47\mu S$

and $g_{m3} = \sqrt{2\cdot 110\cdot 100\cdot 990.1} = 3146.7\mu S$

$$\frac{v_{out}}{v_{in}} = \frac{466.71\cdot 101}{466.71\cdot 101 + 1/50} = \frac{47.137}{47.137+20} = \underline{\underline{0.702\ V/V}}$$

$$R_{out} = \frac{1000}{47.137} = \underline{\underline{21.2\Omega}}$$

Problem 8 - (036412E1P3)

a) For the emitter follower output stage shown below, find the value of R_1 for maximum efficiency and find the value of that efficiency. $V_{CC}=-V_{EE}=2.5\text{V}$, $V_{CE}(sat)=0.2\text{V}$, $R_L=10\text{k}\Omega$, $V_{BE}(on)=0.7\text{V}$.

b) A load capacitor of 100pF is attached to the output voltage. If the input voltage suddenly drops from 2.5V to -2.5V, explain what happens at the output and accurately sketch the output voltage as a function of time, specifying its initial and final values and times.

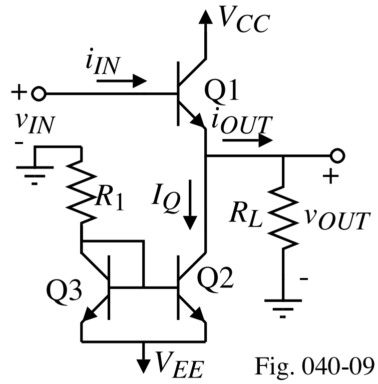


Fig. 040-09

Solution

The I_Q for maximum efficiency is found as,

$$I_Q=\left(\frac{V_{CC}-V_{CE}(sat)}{R_L}\right)=230\mu\text{A}$$

$$R_1=\left(\frac{-V_{EE}-V_{BE}}{I_Q}\right)=7.826\text{k}\Omega$$

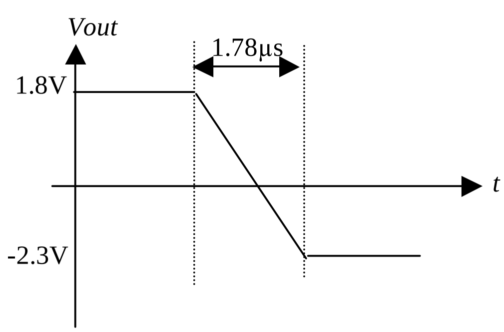
$$P_L(\max)=\left(\frac{V_{CC}-V_{CE}(sat)}{\sqrt{2}}\right)\left(\frac{I_Q}{\sqrt{2}}\right)=0.5(2.3\text{V})(0.23\text{mA})=0.2645\text{mW}$$

$$P_{supply}=2V_{CC}I_Q=2(2.5)(0.23\text{mA})=1.15\text{mW}$$

$$\eta=\frac{P_{L(\max)}}{P_{supply}}=\frac{1}{4}\left(1-\frac{V_{CE(sat)}}{V_{CC}}\right)=23\%$$

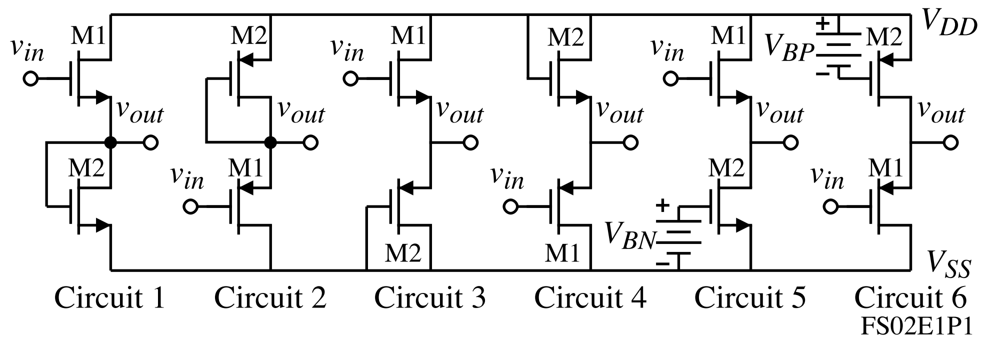
b) The output would slew under such condition. The current will be limited by the bias current:

Slew rate=0.23mA/100pF=2.3V/μs



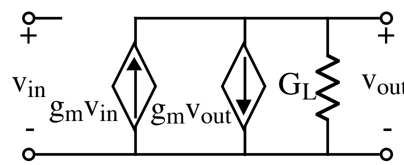
Problem 9 - (026412E1P1)

Six versions of a source follower are shown below. Assume that $K'_N = 2K'_P$, $\lambda_P = 2\lambda_N$, all W/L ratios of all devices are equal, and that all bias currents in each device are equal. Neglect bulk effects in this problem and assume no external load resistor. Identify which circuit or circuits have the following characteristics: (a.) highest small-signal voltage gain, (b.) lowest small-signal voltage gain, (c.) the highest output resistance, (d.) the lowest output resistance, (e.) the highest v_{out}(max) and (f.) the lowest v_{out}(max).



Solution

(a.) and (b.) - Voltage gain. Small signal model:



The voltage gain is found as: $\frac{v_{out}}{v_{in}} = \frac{g_m}{g_m+G_L}$

where G_L is the load conductance. Therefore we get:

Circuit	1	2	3	4	5	6
$\frac{v_{out}}{v_{in}}$	$\frac{g_{mN}}{g_{mN}+g_{mN}}$	$\frac{g_{mP}}{g_{mP}+g_{mP}}$	$\frac{g_{mN}}{g_{mN}+g_{mP}}$	$\frac{g_{mP}}{g_{mP}+g_{mN}}$	$\frac{g_{mN}}{g_{mN}+g_{dsN}+g_{dsP}}$	$\frac{g_{mP}}{g_{mP}+g_{dsN}+g_{dsP}}$

But $g_{mN} = \sqrt{2}\, g_{mP}$ and $g_{dsN} = 0.5g_{dsP}$, therefore

Circuit	1	2	3	4	5	6
$\frac{v_{out}}{v_{in}}$	$\frac{1}{2}$	$\frac{1}{2}$	0.5858	0.4142	$\frac{g_{mP}}{g_{mP}+(g_{dsP}+g_{dsN})/\sqrt{2}}$	$\frac{g_{mP}}{g_{mP}+g_{dsP}+g_{dsN}}$

Thus circuit 5 has the highest gain and circuit 4 the lowest gain

(c.) and (d.) - Output resistance.

The denominators of the first table show the following:

Circuit 6 has the highest output resistance and circuit 1 the lowest output resistance.

(e.) Assuming no current has to be provided by the output, circuits 2, 4, and 6 can pull the output to V_{DD}. ∴ Circuits 2 and 4 and 6 have the highest output swing.

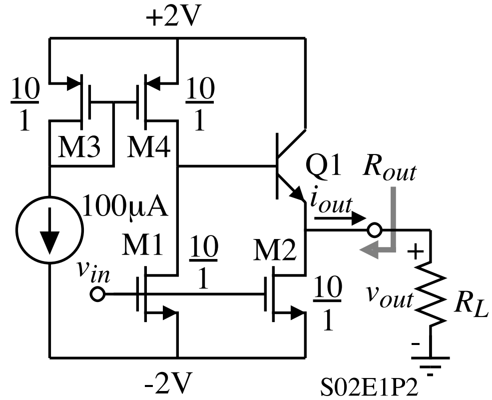
(f.) Assuming no current has to be provided by the output, circuits 1, 3, and 5 can pull the output to ground. ∴ Circuits 1 and 3 and 5 have lowest output swing.

Summary

(a.) Ckt. 5 has the highest voltage gain
(b.) Ckt. 4 has the lowest voltage gain
(c.) Ckt. 6 has the highest output resistance
(d.) Ckt. 1 has the lowest output resistance
(e.) Ckts. 2,4 and 6 have the highest output
(f.) Ckts. 1,3 and 5 have the lowest output

Problem 10 - (026412E1P2)

An output stage using both MOSFETs and a BJT is shown. Assume the transistor parameters are $K_N' = 110\mu A/V^2$, $V_T = 0.7V$, and $\lambda_N = 0.04V^{-1}$ for the NMOS; $K_P' = 50\mu A/V^2$, $V_T = -0.7V$, and $\lambda_P = 0.05V^{-1}$ for the PMOS and $\beta_F = 100$, $V_t = 0.025V$, and $I_s = 10fA$ for the NPN BJT. (a.) If v_{in} can vary between ±2V, what is the maximum positive and negative value of i_{out} when $R_L = 0\Omega$? (b.) If v_{in} can vary between ±2V, what is the maximum and minimum output voltage when $R_L = 100\Omega$?



Solution

(a.) The maximum i_{out} occurs when v_{in} = -2V. All of the 100μA through M4 is base current giving a maximum $i_{out} = (1+\beta)100\mu A = 10.1mA$ → $i_{out}(\max) = \underline{\underline{10.1mA}}$

The maximum $-i_{out}$ occurs when v_{in} = +3V. Since V_{DS} = 2V and $V_{GS} - V_T$ = 3.3V, M2 is in the triode region. Under these conditions, we assume M1 absorbs all of the 100μA of M4 and therefore the BJT is off and maximum $-i_{out}$ is,

$$-i_{out}(\max) = \frac{K_N'W}{L}[(V_{GS2}-V_T)v_{DS} - 0.5v_{DS}^2] = 110\cdot 10[3.3\cdot 2 - 0.5(2)^2] = 5.06mA \;\therefore$$
$$-i_{out}(\max) = \underline{\underline{-5.06mA}}$$

(b.) There are 2 possible answers for the maximum v_{out}. The current limited max. v_{out} is

$$\text{Max. } v_{out} = i_{out}(\max)R_L = 10.1mA\cdot 0.1k\Omega = 1.01V$$

The voltage limited $v_{out}(\max)$ is,

$$\text{Max. } v_{out} = 2V - V_{SD4}(\text{sat}) - V_{BE1}(10.1mA) = 2-\sqrt{\frac{2\cdot 100}{50\cdot 10}} - 0.025\ln\left(\frac{10mA}{10fA}\right)$$

$$= 2-0.6325-0.6908 = 0.6768V \qquad \therefore \text{ Max. } v_{out} = \underline{\underline{0.6768V}}$$

For the maximum $-v_{out}$ we see that the V_{GS2} = 4V which strongly suggests that M2 will be in the triode region. Equating the current in the 100Ω resistor with that in M2 gives,

$$\frac{2-v_{DS}}{100} = \frac{K_N'W}{L}[(V_{GS2}-V_T)v_{DS} - 0.5v_{DS}^2]$$

$$0.02-0.01v_{DS} = 1.1\text{x}10^{-3}[3.3v_{DS} - 0.5v_{DS}^2] \rightarrow v_{DS}^2 - 24.782v_{DS} + 36.36 = 0$$

$\therefore \quad v_{DS} = +12.391 \pm 10.8247 \rightarrow v_{DS} = 1.5662V$

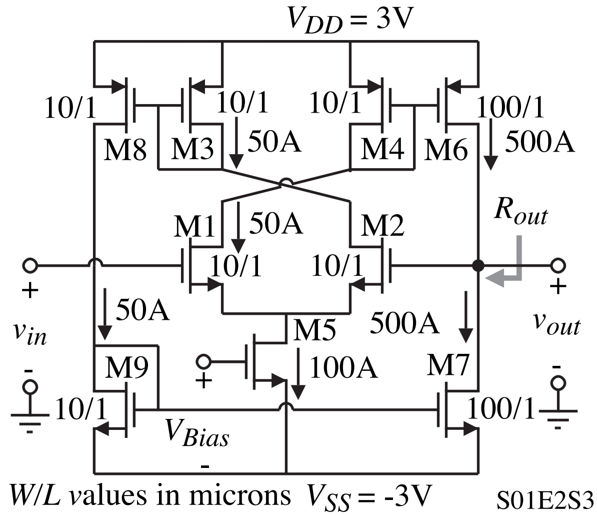
$\therefore \quad \text{Max. } -v_{out} = -2V + 1.5662V = \underline{\underline{-0.4338V}}$

The current through M2 under this condition is $\frac{110\cdot 10}{2\cdot 1}(1.5662V)^2 = 1.349mA$

It can be shown that if M2 remains saturated that Max. $-v_{out} = I\cdot 100\Omega = -0.1815V$
So our assumption that M2 was in the triode region is valid.

Problem 10 - (016412E2P3)

A CMOS circuit used as an output buffer for an OTA is shown. Find the value of the small signal output resistance, R_{out}, and from this value estimate the -3dB bandwidth if a 50pF capacitor is attached to the output. What is the maximum and minimum output voltage if a 1kΩ resistor is attached to the output? What is the quiescent power dissipation of this circuit? Use the following model parameters: K_N'=110μA/V^2, K_P' = 50μA/V^2, V_{TN} = -V_{TP} = 0.7V, λ_N = 0.04V^{-1} and λ_P = 0.05V^{-1}.



Solution

Use feedback concepts to calculate the output resistance, R_{out}.

$$R_{out} = \frac{R_o}{1-LG}$$

where R_o is the output resistance with the feedback open and LG is the loop gain.

$$R_o = \frac{1}{g_{ds6}+g_{ds7}} = \frac{1}{(\lambda_N+\lambda_P)I_6} = \frac{10^6}{0.09\cdot 500} = 22.22\text{k}\Omega$$

The loop gain is,

$$LG = \frac{v_{out}'}{v_{out}} = -\frac{1}{2}\left[\frac{g_{m2}g_{m6}}{g_{m4}} + \frac{g_{m1}g_{m9}}{g_{m7}}\right] R_o$$

$g_{m1} = g_{m2} = \sqrt{2\cdot 110\cdot 50\cdot 10} = 331.67\mu\text{S}$, $g_{m3} = g_{m4} = \sqrt{2\cdot 50\cdot 50\cdot 10} = 223.6\mu\text{S}$,

$g_{m6} = \sqrt{2\cdot 50\cdot 100\cdot 500} = 2236\mu\text{S}$ and $g_{m7} = \sqrt{2\cdot 110\cdot 500\cdot 100} = 3316.7\mu\text{S}$

$$\therefore \quad LG = \frac{v_{out}'}{v_{out}} = -\frac{1}{2}\left[\frac{-331.67\cdot 2236}{223.6} + \frac{-331.67\cdot 3316.7}{331.67}\right] = -73.68\text{V/V}$$

$$R_{out} = \frac{R_o}{1-LG} = \frac{22.22\text{k}\Omega}{1+73.68} = \underline{\underline{294.5\Omega}}$$

$$f_{-3\text{dB}} = \frac{1}{2\pi\cdot R_{out}\cdot 50\text{pF}} = \frac{1}{2\pi\cdot 294.5\cdot 50\text{pF}} = \underline{\underline{10.81\text{MHz}}}$$

To get the maximum swing, we must check two limits. First, the saturation voltages of M6 and M7.

$$V_{ds6}(\text{sat}) = \sqrt{\frac{2\cdot 1000}{50\cdot 100}} = 0.6325\text{V} \quad \text{and} \quad V_{ds7}(\text{sat}) = \sqrt{\frac{2\cdot 1000}{110\cdot 100}} = 0.4264\text{V}$$

Second, the maximum current available to the 1kΩ resistor is ±1mA which means that the output swing can only be ±1V. Therefore, <u>maximum/minimum output = ±1V</u>.

P_{diss} = 6V(650μA) = $\underline{\underline{3.9\text{mW}}}$

Problem 11 - (016412FEP1)

An output amplifier is shown. Assume that v_{IN} can vary from -2.5V to +2.5V. Let $K_P' = 50\mu A/V^2$, $V_{TP} = -0.7V$, and $\lambda_P = 0.05V^{-1}$. Ignore bulk effects.

a.) Find the maximum value of v_{OUT}, $v_{OUT}(\max)$.

b.) Find the minimum value of v_{OUT}, $v_{OUT}(\min)$.

c.) Find the positive slew rate, SR^+ when v_{OUT} = 0V in volts/microseconds.

d.) Find the negative slew rate, SR^- when v_{OUT} = 0V in volts/microseconds.

e.) Find the small signal output resistance (excluding the 10kΩ resistor) when v_{OUT} = 0V.

Solution

a.) When v_{IN} = +2.5V, the transistor is shut off and $\underline{\underline{v_{OUT}(\max) = 200\mu A\cdot 10k\Omega = +2V}}$

b.) When v_{IN} = -2.5V, the transistor is in saturation (drain = gate) and the minimum output voltage under steady-state is,

$$v_{OUT} = -10k\Omega(I_D - 200\mu A) = -10k\Omega\left[\frac{50\cdot 300}{2}(v_{OUT}+2.5-0.7)^2 - 200\mu A\right]$$

$$v_{OUT} = -75(v_{OUT}+1.8)^2 + 2 \quad \rightarrow \quad v_{OUT}^2 + 3.6133v_{OUT} + 3.21333 = 0$$

$$\therefore \quad v_{OUT} = -\frac{3.61333}{2} \pm \frac{\sqrt{(3.61333)^2 - 4\cdot 3.21333}}{2} = -1.80667 \pm 0.22519$$

It can be shown that the correct choice is $\underline{\underline{v_{OUT}(\min) = -1.80667 + 0.22519 = -1.5815V}}$

c.) The positive slew rate is $SR^+ = \dfrac{200\mu A}{50pF} = +4V/\mu s \quad \rightarrow \quad \underline{\underline{SR^+ = +4V/\mu s}}$

d.) The negative slew rate is found as follows. With v_{OUT} = 0V, the drain current is

$$I_D = 7.5mA/V^2(2.5-0.7)^2 = 24.3mA$$

Therefore, the sourcing current is 24.3mA-0.2mA = 24.1mA which gives a negative slew rate of

$$SR^- = \frac{24.1mA}{50pF} = -482V/\mu s \quad \rightarrow \quad \underline{\underline{SR^- = -482V/\mu s}}$$

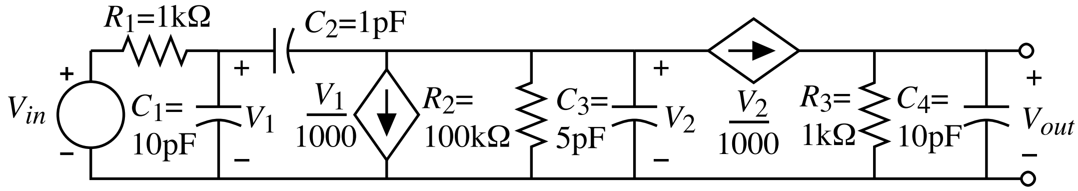
e.) The output resistance, R_{out}, is approximately equal to $1/g_m$. Therefore,

$$R_{out} \approx \frac{1}{g_m} = \sqrt{\frac{L}{2K_P I_D W}} = \frac{1}{\sqrt{2\cdot 50\cdot 200\cdot 300}} = 408.2\Omega \quad \rightarrow \quad \underline{\underline{R_{out} \approx 408\Omega}}$$

SMALL SIGNAL FREQUENCY RESPONSE

Problem 1 (056412E1P3)

Find the midband voltage gain and the –3dB frequency in Hertz for the circuit shown.



S05E1P3

Solution

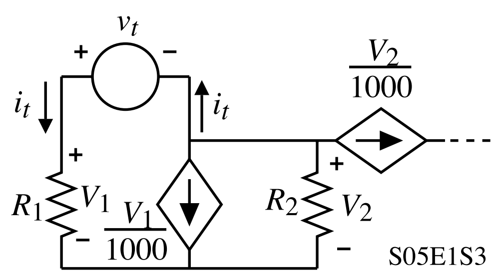
The midband voltage gain can be expressed as,

$$\frac{V_{out}}{V_{in}} = \frac{V_{out}}{V_2}\frac{V_2}{V_1}\frac{V_1}{V_{in}} = (1)\left(\frac{-R_2}{R_2+1000}\right)(1) = \underline{\underline{-0.99\text{V/V}}}$$

Finding the open-circuit, time constants:

R_{C1O}: $\quad R_{C1O} = R_1 = 1\text{k}\Omega \quad\rightarrow\quad R_{C1O}C_1 = 10\text{ns}$

R_{C2O}:



S05E1S3

$$v_t = R_1 i_t + R_2\left[i_t + \frac{V_1}{1000} + \frac{V_2}{1000}\right]$$

But $v_t = V_1 - V_2$ and $V_1 = R_1 i_t$,

$$\therefore \quad v_t = R_1 i_t + R_2 i_t + \frac{2R_1R_2 i_t}{1000} - \frac{R_2 v_t}{1000}$$

$$R_{C2O} = \frac{v_t}{i_t} = \frac{R_1+R_2 + 0.002R_1R_2}{1+0.001R_2}$$

$$= \frac{1\text{k}\Omega+100\text{k}\Omega+200\text{k}\Omega}{1+100} = 2.98\text{k}\Omega \quad\rightarrow\quad R_{C2O}C_2 = 2.98\text{ns}$$

R_{C3O}: $\quad R_{C3O} = R_2 \| 1\text{k}\Omega = 0.99\text{k}\Omega \quad\rightarrow\quad R_{C3O}C_3 = 4.95\text{ns}$

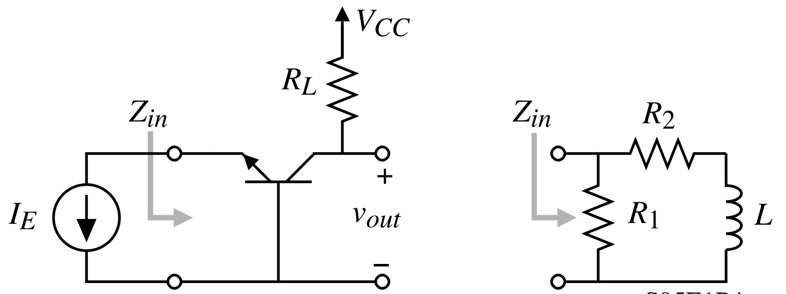
R_{C4O}: $\quad R_{C4O} = R_3 = 1\text{k}\Omega \quad\rightarrow\quad R_{C4O}C_4 = 10\text{ns}$

$$\Sigma T_{oc} = (10+2.98+4.95+10)\text{ns} = 27.93\text{ns}$$

$$\omega_{\text{-3dB}} \approx \frac{1}{\Sigma T_{oc}} = 35.8\text{x}10^6 \quad\rightarrow\quad f_{\text{-3dB}} = \underline{\underline{5.698\text{ MHz}}}$$

Problem 2 - (056412E1P4)

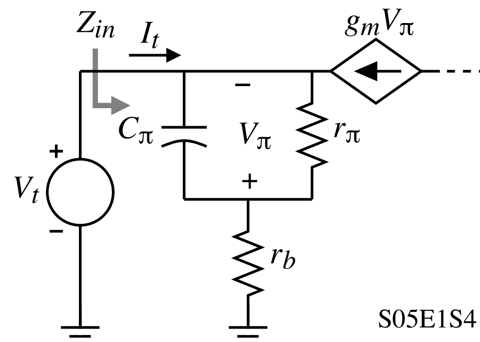
On page 514 of the text, the statement is made that "the common base input impedance is low at low frequencies and becomes inductive at high frequencies"... Find the small-signal input impedance to the common base amplifier and express the values of the equivalent circuit, R_1, R_2, and L in terms of the parameters of the BJT small signal model (r_b, r_π, C_π, and β_o). Ignore r_o and assume that $R_1 > R_2$.



S05E1P4

Solution

Use the following small signal model for this problem.



S05E1S4

$$I_t + \frac{V_\pi}{Z_\pi} + g_m V_\pi = 0 \;\rightarrow\; I_t = -V_\pi\left(g_m + \frac{1}{Z_\pi}\right)$$

and

$$V_t = -V_\pi - \frac{V_\pi}{Z_\pi} r_b \;\rightarrow\; V_t = -V_\pi\left(1 + \frac{r_b}{Z_\pi}\right)$$

$$\therefore\quad Z_{in} = \frac{V_t}{I_t} = \left(\frac{Z_\pi + r_b}{1 + g_m Z_\pi}\right) \quad \text{where} \quad Z_\pi = \frac{r_\pi}{sC_\pi r_\pi + 1}$$

Now,

$$Z_{in} = \frac{r_b + \dfrac{r_\pi}{sC_\pi r_\pi + 1}}{1 + \dfrac{g_m r_\pi}{sC_\pi r_\pi + 1}} = \frac{r_b(1 + sC_\pi r_\pi) + r_\pi}{1 + g_m r_\pi + sC_\pi r_\pi} = \frac{(r_b + r_\pi) + sC_\pi r_\pi r_b}{1 + \beta_o + sC_\pi r_\pi}$$

$$= \frac{\dfrac{(r_b + r_\pi)}{\beta_o} + \dfrac{sC_\pi r_\pi r_b}{\beta_o}}{1 + \dfrac{1}{\beta_o} + \dfrac{sC_\pi r_\pi}{\beta_o}} = \frac{\left(\dfrac{(r_b + r_\pi)}{\beta_o} + \dfrac{sC_\pi r_\pi r_b}{\beta_o}\right) r_b}{r_b + \dfrac{r_b}{\beta_o} + \dfrac{sC_\pi r_\pi r_b}{\beta_o}} \approx \frac{\left(\dfrac{(r_b + r_\pi)}{\beta_o} + \dfrac{sC_\pi r_\pi r_b}{\beta_o}\right) r_b}{r_b + \dfrac{sC_\pi r_\pi r_b}{\beta_o}}$$

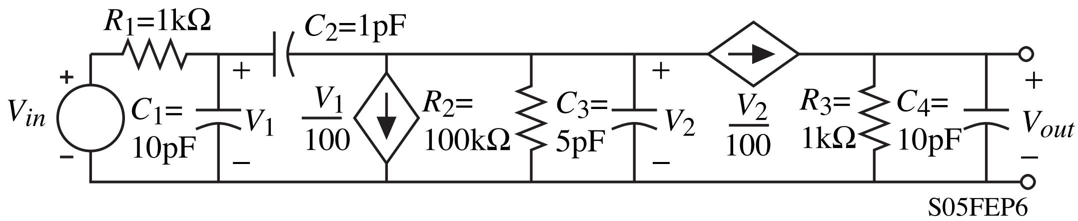
$$Z_{in} = \frac{R_1(R_2 + sL)}{R_1 + R_2 + sL} \approx \frac{R_1(R_2 + sL)}{R_1 + sL} \quad \text{if } R_1 > R_2$$

Equating the two expressions for Z_{in} gives,

$$\boxed{R_1 = r_b,\; R_2 = \frac{(r_b + r_\pi)}{\beta_o},\; \text{and } L = \frac{C_\pi r_\pi r_b}{\beta_o}}$$

Problem 3 - (056412FE6)

Find the midband voltage gain and the –3dB frequency in Hertz for the circuit shown.



Solution

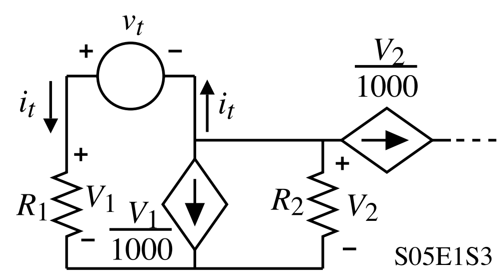
The midband voltage gain can be expressed as,

$$\frac{V_{out}}{V_{in}} = \frac{V_{out}}{V_2}\frac{V_2}{V_1}\frac{V_1}{V_{in}} = (10)\left(\frac{-R_2}{R_2+1000}\right)(1) = \underline{\underline{-9.9\text{V/V}}}$$

Finding the open-circuit, time constants:

R_{C1O}: $R_{C1O} = R_1 = 1\text{k}\Omega$ → $R_{C1O}C_1 = 10\text{ns}$

R_{C2O}:



$$v_t = R_1 i_t + R_2\left[i_t + \frac{V_1}{100} + \frac{V_2}{100}\right]$$

But $v_t = V_1 - V_2$ and $V_1 = R_1 i_t$,

$$\therefore \quad v_t = R_1 i_t + R_2 i_t + \frac{2R_1R_2i_t}{100} - \frac{R_2v_t}{100}$$

$$R_{C2O} = \frac{v_t}{i_t} = \frac{R_1+R_2 + 0.02R_1R_2}{1+0.01R_2}$$

$$= \frac{1\text{k}\Omega+100\text{k}\Omega+2000\text{k}\Omega}{1+1000} = 2.099\text{k}\Omega \quad \rightarrow \quad R_{C2O}C_2 = 2.1\text{ns}$$

R_{C3O}: $R_{C3O} = R_2 \,||\, 100\Omega = 99.9\Omega$ → $R_{C3O}C_3 = 0.5\text{ns}$

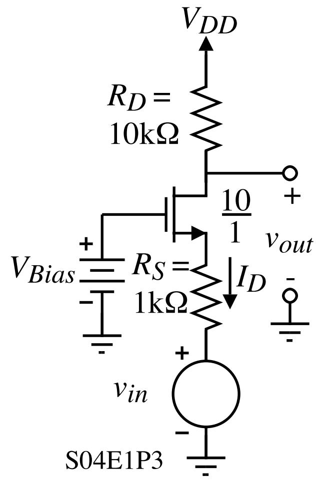
R_{C4O}: $R_{C4O} = R_3 = 1\text{k}\Omega$ → $R_{C4O}C_4 = 10\text{ns}$

$\Sigma T_{oc} = (10+2.1+0.5+10)\text{ns} = 22.6\text{ns}$

$$\omega_{-3\text{dB}} \approx \frac{1}{\Sigma T_{oc}} = 44.25\text{x}10^6 \quad \rightarrow \quad f_{-3\text{dB}} = \underline{\underline{7.04\text{ MHz}}}$$

Problem 4 - (046412E1P3)

Find the voltage transfer function of the common-gate amplifier shown. Identify the numerical values of the small-signal voltage gain, v_{out}/v_{in}, and the poles and zeros. Assume that I_D = 500μA, K_N' = 100μA/V^2, V_{TN} = 0.5V, and K_P' = 50μA/V^2, V_{TP} = -0.5V, $\lambda \approx 0V^{-1}$, C_{gs} = 0.5pF and C_{gd} = 0.1pF.



S04E1P3

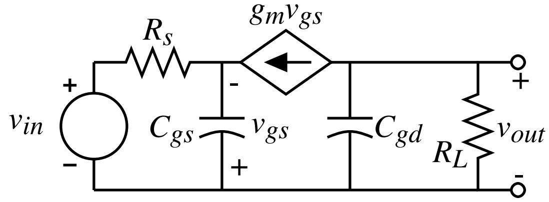
Solution

The small signal transconductance is,

$$g_m = \sqrt{2\cdot K_N'(W/L)I_D} = \sqrt{2\cdot 100\cdot 10\cdot 500} = 1\text{mS}$$

$$r_{ds} = \infty$$

The small signal model is,



S04E1S3

The voltage gain can be expressed as follows,

$$\frac{V_{out}}{V_{in}} = \left(\frac{V_{out}}{V_{gs}}\right)\left(\frac{V_{gs}}{V_{in}}\right), \qquad \frac{V_{out}}{V_{gs}} = -g_m\left(\frac{R_L(1/sC_{gd})}{R_L+(1/sC_{gd})}\right)$$

Sum currents at the source to get,

$$\frac{V_{in} + V_{gs}}{R_s} + g_m V_{gs} + sC_{gs}V_{gs} = 0 \qquad \rightarrow \qquad \frac{V_{gs}}{V_{in}} = \frac{-G_s}{G_s + g_m + sC_{gs}}$$

$$\therefore \quad \frac{V_{out}}{V_{in}} = \left(\frac{g_m R_L}{1+ g_m R_L}\right)\left(\frac{1}{sC_{gd}R_L+1}\right)\left(\frac{1}{\frac{sC_{gs}}{g_m+G_s}+1}\right)$$

The various values are,

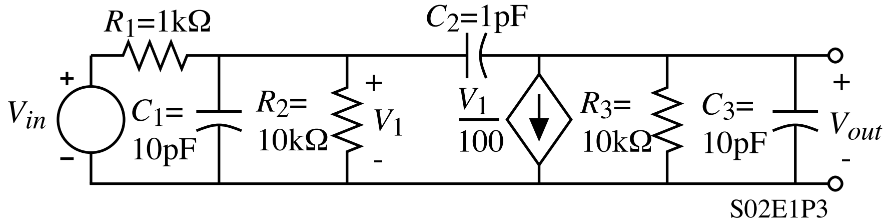
$$\text{Voltage gain} = \frac{g_m R_L}{1+ g_m R_L} = \frac{1\cdot 10}{1+1} = \underline{\underline{5\text{V/V}}}$$

$$p_1 = \frac{-1}{C_{gd}R_L} = \frac{-1}{10^{-13}\cdot 10^4} = \underline{\underline{-10^9 \text{ radians/sec.}}}$$

$$p_2 = \frac{-(g_m+G_s)}{C_{gs}} = \frac{-10^{-3}+10^{-3}}{0.5\text{x}10^{-12}} = \underline{\underline{-4\text{x}10^9 \text{ radians/sec.}}}$$

Problem 5 - (026412E1P3)

Find the midband voltage gain and the –3dB frequency in Hertz for the circuit shown.



Solution

The midband gain is given as,

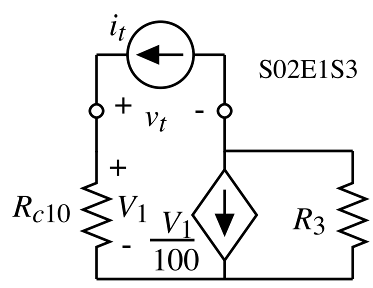
$$\frac{V_{out}}{V_{in}} = -\left(\frac{10\text{k}\Omega}{100}\right)\left(\frac{10\text{k}\Omega}{11\text{k}\Omega}\right) = \underline{\underline{-90.91\text{V/V}}}$$

To find the –3dB frequency requires finding the 3 open-circuit time constants.

R_{C10}:

$$R_{C10} = 1\text{k}\Omega||10\text{k}\Omega = 0.9091\text{k}\Omega \quad \rightarrow \quad R_{C10}C_1 = 0.9091\cdot 10\text{ns} = 9.09\text{ns}$$

R_{C20}:



$$v_t = i_t R_{C10} + R_3(i_t + 0.01V_1)$$

$$= i_t(R_{C10} + R_3 + 0.01R_{C10}R_3)$$

$$\therefore R_{C20} = R_{C10} + R_3 + 0.01R_{C10}R_3$$

$$= 0.9091 + 10(1+0.01\cdot 909.1)\text{k}\Omega = 101.82\text{k}\Omega$$

$$R_{C20}C_2 = 101.82\cdot 1\text{ns} = 101.82\text{ns}$$

R_{C30}:

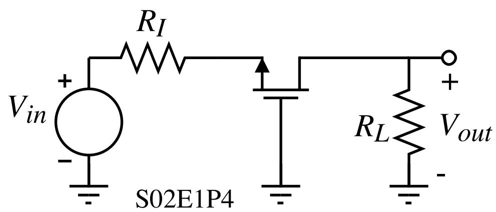
$$R_{C30} = 10\text{k}\Omega \quad \rightarrow \quad R_{C30}C_3 = 10\cdot 10\text{ns} = 100\text{ns}$$

$$\Sigma T_0 = (9.091 + 101.82 + 100)\text{ns} = 210.91\text{ns} \rightarrow \omega_{-3\text{dB}} = \frac{1}{\Sigma T_0} = 4.74\text{x}10^6 \text{ rad/s}$$

$$f_{-3\text{dB}} = \frac{4.74\text{x}10^6}{2\pi} = \underline{\underline{754.6\text{kHz}}}$$

Problem 6 - (026412E1P4)

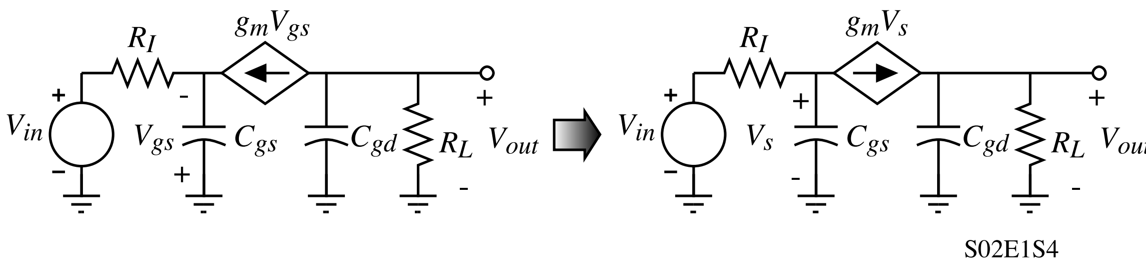
Find the midband voltage gain and the exact value of the two poles of the voltage transfer function for the circuit shown. Assume that R_I = 1kΩ, R_L = 10KΩ, g_m = 1mS, C_{gs} = 5pF and C_{gd} = 1pF. Ignore r_{ds}.



Solution

The best approach to this problem is a direct analysis.

Small-signal model:



$$V_{out} = g_m Z_L V_s \qquad \text{where} \qquad Z_L = \frac{1}{sR_LC_{gd}+1} \qquad \text{and} \qquad \frac{V_{in}-V_s}{R_I} = g_mV_s + sC_{gs}V_s$$

Solving for V_s from the second equation gives,

$$V_s = \frac{V_{in}}{1+g_mR_I+sC_{gs}R_I}$$

Substituting V_s in the first equation gives,

$$V_{out} = g_mZ_L\frac{V_{in}}{1+g_mR_I+sC_{gs}R_I} \quad \rightarrow \quad \frac{V_{out}}{V_{in}} = g_m\left(\frac{1}{sR_LC_{gd}+1}\right)\left(\frac{1}{1+g_mR_I+sC_{gs}R_I}\right)$$

$$= \left(\frac{g_mR_L}{1+g_mR_I}\right)\left(\frac{1}{sR_LC_{gd}+1}\right)\left(\frac{1}{\frac{sC_{gd}R_I}{1+g_mR_I}+1}\right) = \text{MBG}\left(\frac{1}{1-\frac{s}{p_1}}\right)\left(\frac{1}{1-\frac{s}{p_2}}\right)$$

$$\therefore \ \text{MBG} = \left(\frac{g_mR_L}{1+g_mR_I}\right) = \left(\frac{1\cdot10}{1+1\cdot1}\right) = \underline{\underline{5\text{V/V}}}$$

$$p_1 = -\frac{1}{R_LC_{gd}} = -\frac{1}{10\cdot1\text{ns}} = \underline{\underline{-10^8 \text{ rad/s}}} \quad \text{and} \quad p_2 = -\frac{1+g_mR_I}{R_IC_{gs}} = -\frac{1+1}{1\cdot5\text{ns}} = \underline{\underline{-4\text{x}10^8 \text{ rad/s}}}$$

COMPENSATION OF OP AMPS

Problem 1 - (056412E2P2)

If a two-stage, Miller compensated CMOS op amp has a RHP zero at $5GB$, a dominant pole due to the Miller compensation, and a second pole at $-p_2$, find the value of the first stage transconductance (g_{mI}), the second stage transconductance (g_{mII}), and the value of the Miller capacitor, C_c, if GB = 10MHz, the load capacitor is 10pF, and the phase margin is to be 50°. Assume that the unity gain magnitude frequency is GB.

Solution

1.) The phase margin gives p_2 which will give g_{mII}.

$$180° - 90° - \tan^{-1}\left(\frac{GB}{|p_2|}\right) - \tan^{-1}(0.2) = 50° \qquad \rightarrow \tan^{-1}\left(\frac{GB}{|p_2|}\right) = 28.69°$$

$$\therefore \quad |p_2| = \frac{GB}{0.544} = \frac{20\pi\text{MHz}}{0.544} = 115.5\text{x}10^6 \text{ rads/sec.}$$

We know that,

$$|p_2| = \frac{g_{mII}}{C_L} \qquad \rightarrow \qquad g_{mII} = |p_2|C_L = (115.5\text{x}10^6 \text{ rads/sec.})(10\text{pF}) = \underline{\underline{1.155\text{mS}}}$$

2.) The Miller capacitor is found from the RHP zero location.

$$\frac{g_{mII}}{C_c} = z_1 \qquad \rightarrow \qquad C_c = \frac{g_{mII}}{z_1} = \frac{1.115\text{mS}}{5\cdot GB} = \frac{1.115\text{mS}}{10\pi\text{x}10^7} = \underline{\underline{3.55\text{pF}}}$$

3.) Finally, the input stage transconductance is given by,

$$GB = \frac{g_{mI}}{C_c} \qquad \rightarrow \qquad g_{mI} = GB\cdot C_c = (2\pi\text{x}10^7)(3.55\text{pF}) = \underline{\underline{223\mu\text{S}}}$$

Problem 2 - (046412E2P1)

A self-compensated op amp has three higher order poles grouped closely around $-1\text{x}10^9$ radians/sec. What should be the *GB* of this op amp in Hz to achieve a 60° phase margin? If the low frequency gain of the op amp is 80dB, where is the location of the dominant pole, p_1? If the output resistance of this amplifier is 10MΩ, what is the value of C_L that will give this location for p_1? (Ignore any other capacitance at the output for this part of the problem).

Solution

The key to this problem is to assume that the three closely grouped poles around $-1\text{x}10^9$ radians/sec. can be approximated as three poles at $-1\text{x}10^9$ radians/sec. Therefore,

$$\text{Phase margin} = \text{PM} = 180° - \tan^{-1}\left(\frac{GB}{|p_1|}\right) - 3\tan^{-1}\left(\frac{GB}{|p_H|}\right) = 60°$$

where p_H is a pole at $-1\text{x}10^9$ radians/sec. Assuming that $GB/|p_1|$ is large then, we can write the above as,

$$180° - 90° - 3\tan^{-1}\left(\frac{GB}{|p_H|}\right) = 60° \rightarrow 30° = -3\tan^{-1}\left(\frac{GB}{|p_H|}\right) \rightarrow \frac{GB}{|p_H|} = \tan(10°) = 0.1763$$

$\therefore$ $GB = 0.1763|p_H| = 176.3$ Mradians/sec. $\rightarrow$ $\underline{\underline{GB = 28.06\text{MHz}}}$

80dB $\rightarrow$ 10,000 which gives

$$|p_1| = \frac{GB}{A_v} = \frac{176.3\text{x}10^6}{10^4} = \underline{\underline{17{,}630 \text{ radians/sec.}}} \rightarrow |p_1| = 2.806\text{kHz}$$

The expression for p_1 is

$$|p_1| = \frac{1}{R_{out}C_L} \rightarrow C_L = \frac{1}{R_{out}|p_1|} = \frac{1}{1.763\text{x}10^4 \cdot 10^7} = \underline{\underline{5.672\text{pF}}}$$

Problem 3 - (036412E2P2)

A two-stage, Miller compensated op amp has the following values: g_{mI} = 100μS, g_{mII} = 1000μS, C_c = 2pF, and C_L = 10pF.

a.) What value of nulling resistor, R_z, will cancel the output pole?

b.) If the output capacitance of the first stage is C_I = 1pF, what is the phase margin in part a.) if R_z is 5kΩ.

c.) If C_L is increased to 20pF and R_z = 5kΩ, what is the new phase margin?

Solution

a.) The zero is given as $z = \dfrac{1}{C_c\left(\dfrac{1}{g_{mII}} - R_z\right)}$ and the output pole is $p_2 = -\dfrac{g_{mII}}{C_c}$. Equating these two roots gives,

$$R_z = \frac{1}{g_{mII}}\left(\frac{C_L+C_c}{C_c}\right) = \frac{1}{1000\mu\text{S}}\left(\frac{12}{2}\right) = \underline{\underline{6\text{k}\Omega}}$$

b.) The pole due to R_z is

$$p_4 = -\frac{1}{R_zC_I} = -\frac{1}{5\text{k}\Omega\cdot 1\text{pF}} = -2\text{x}10^8 \text{ rads/sec.}$$

Also, the GB is

$$GB = \frac{g_{mI}}{C_c} = \frac{100\mu\text{S}}{2\text{pF}} = 50\text{x}10^6 \text{ rads/sec.}$$

The phase margin is,

$$PM = 180° - 90° - \tan^{-1}\left(\frac{GB}{|p_4|}\right) = 90° - \tan^{-1}\left(\frac{50}{200}\right) = 90° - 14° = \underline{\underline{76°}}$$

(You should assume that z_1 still cancels p_2. If you do assume this, the answer is 71.2°.)

c.) The new phase margin is,

$$PM = 180° - 90° + \tan^{-1}\left(\frac{GB}{|p_2|}\right) - \tan^{-1}\left(\frac{2GB}{|p_2|}\right) - \tan^{-1}\left(\frac{GB}{|p_4|}\right)$$

$$z_1 = -\frac{g_{mII}}{C_L} = -\frac{1000\mu\text{S}}{10\text{pF}} = -100\text{x}10^6 \text{ rads/sec.}$$

$$p_2 = -\frac{g_{mII}}{C_L} = -\frac{1000\mu\text{S}}{20\text{pF}} = -50\text{x}10^6 \text{ rads/sec.}$$

$$\therefore \quad PM = 90° + \tan^{-1}\left(\frac{50}{50}\right) - \tan^{-1}\left(\frac{100}{50}\right) - \tan^{-1}\left(\frac{50}{200}\right) = 90° + 43° - 63.43° - 14° = \underline{\underline{57.52°}}$$

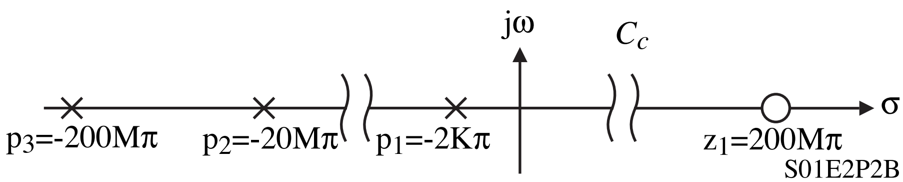
Problem 4 - (016412E2P2)

The poles and zeros of a Miller compensated, two-stage op amp are shown below.

(a.) If the influence of p_3 and z_1 are ignored, what is the GB in MHz of this op amp for 60° phase margin?

(b.) What is the value of $A_v(0)$? What is the value of C_c if g_{m1}=g_{m2}=500µS?

(c.) If p_2 is moved to p_3, what is the new GB in MHz for 60° phase margin? What is the new C_c if the input transconductances are the same as in (b.)?



Solution

(a.) The phase margin, PM, can be written as

$$\text{PM} = 180 - \tan^{-1}\left(\frac{GB}{|p_2|}\right) - \tan^{-1}\left(\frac{GB}{|p_3|}\right) - \tan^{-1}\left(\frac{GB}{z_1}\right) \approx 90° - \tan^{-1}\left(\frac{GB}{|p_2|}\right) = 60°$$

$$\therefore \quad \tan^{-1}\left(\frac{GB}{|p_2|}\right) = 30° \quad \rightarrow \quad GB = 0.5774 \cdot |p_2| = \underline{\underline{5.774\text{MHz}}}$$

(b.)
$$A_v(0) = \frac{GB}{|p_1|} = \frac{5.774\text{MHz}}{1\text{kHz}} = \underline{\underline{5{,}774\text{V/V}}}$$

$$\frac{g_{m1}}{C_c} = GB \quad \rightarrow \quad C_c = \frac{g_{m1}}{GB} = \frac{500\mu\text{S}}{2\pi \cdot 5.774\text{x}10^6} = \underline{\underline{13.78\text{pF}}}$$

(c.) The phase margin, PM, can be written as

$$\text{PM} = 180 - \tan^{-1}\left(\frac{GB}{|p_2|}\right) - \tan^{-1}\left(\frac{GB}{|p_3|}\right) - \tan^{-1}\left(\frac{GB}{z_1}\right) \approx 90° - 3 \cdot \tan^{-1}\left(\frac{GB}{|p_2|}\right) = 60°$$

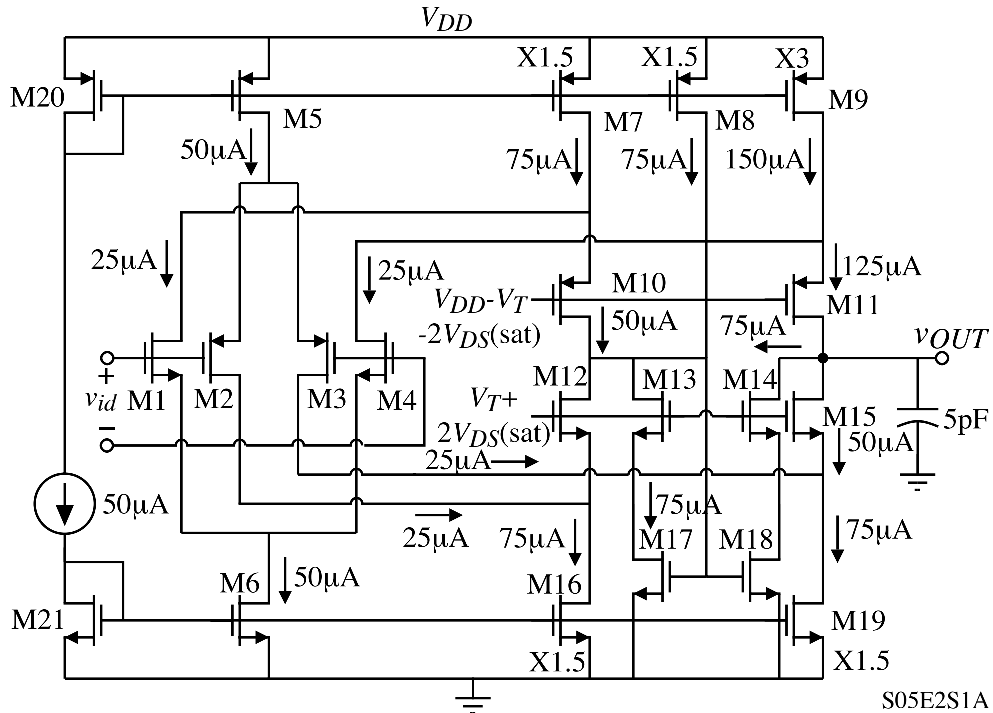
$$\therefore \quad \tan^{-1}\left(\frac{GB}{|p_2|}\right) = 10° \quad \rightarrow \quad GB = 0.1763 \cdot |p_2| = 0.01763 \cdot 100\text{MHz} = \underline{\underline{17.63\text{MHz}}}$$

$$C_c = \frac{g_{m1}}{GB} = \frac{500\mu\text{S}}{2\pi \cdot 17.63\text{x}10^6} = \underline{\underline{4.514\text{pF}}}$$

OP AMPS

Problem 1 - (056412E2P1)

The CMOS op amp shown uses a complementary differential input stages to achieve a wider input voltage common mode range. Assume that all transistors are scaled from a X1 NMOS and PMOS that have been designed to have a small-signal transconductance of 100μS and a channel conductance of 1μS at 25μA of current. Give your best estimate of the slew rate (V/μs), output resistance, R_{out}, small-signal voltage gain (v_{out}/v_{id}), and the gainbandwidth, GB, in MHz.



Solution

The dc currents for v_{id} = 0 are shown above. One can show that the maximum amount of current available to the output capacitor is twice the 50μA current sink/source or 100μA. Therefore, the slew rate is <u>SR = 100μA/5pF = 20V/μs</u>.

The small-signal voltage gain can be written by inspection as (note the M13-M14-M17-M18 combination is used to recover the full differential output of both complementary input stages),

$$\frac{v_{out}}{v_{id}} = (g_{m1}+g_{m2})R_{out} \text{ where } g_{m1} = g_{m2} = 100\mu\text{S}$$

$$R_{out} \approx [(r_{ds9}||r_{ds4})g_{m11}r_{ds11}]||(r_{ds18}g_{m14}r_{ds14})|| [(r_{ds3}||r_{ds19})g_{m15}r_{ds15}]$$

Scaling r_{ds} for the currents gives,

$$r_{ds9} = 1000\text{k}\Omega/6 = 166.7\text{k}\Omega,\ r_{ds11} = 1000\text{k}\Omega/5 = 200\text{k}\Omega,$$

$$r_{ds18} = r_{ds14} = r_{ds19} = 1000\text{k}\Omega/3 = 333.3\text{k}\Omega,\ r_{ds15} = 1000\text{k}\Omega/2 = 500\text{k}\Omega$$

Problem 1 (056412E2P1)– Continued

Scaling g_m for the currents gives,

$$g_{m11} = \sqrt{5}\ 100\mu\text{S} = 223.6\mu\text{S},\ g_{m14} = \sqrt{3}\ 100\mu\text{S} = 173\mu\text{S},\ g_{m15} = \sqrt{2}\ 100\mu\text{S} = 141\mu\text{S}$$

$\therefore\ R_{out} \approx$

$$[(167||1000)(0.224)(200\text{k}\Omega)]||[(333)(0.173)(333.3\text{k}\Omega)]||[(333||1000)(0.173)(500\text{k}\Omega)]$$

$$R_{out} = 6.390\text{M}\Omega||19.18\text{M}\Omega||17.62\text{M}\Omega = \underline{\underline{3.768\text{M}\Omega}}$$

Now,

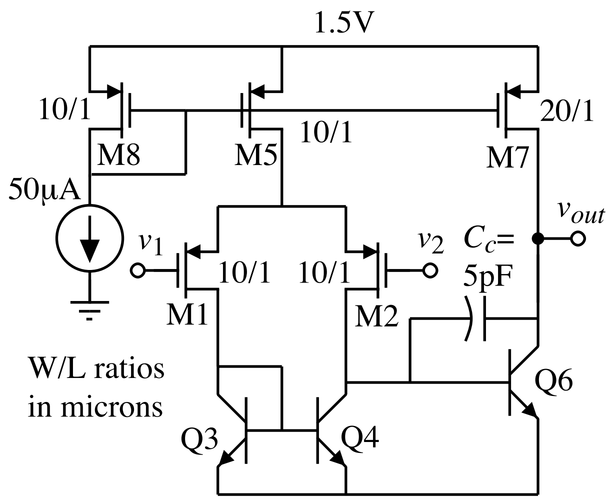
$$\frac{v_{out}}{v_{id}} = 200\mu\text{S}(3.768\text{M}\Omega) = \underline{\underline{769\text{ V/V}}}$$

The gainbandwidth is,

$$GB = \frac{g_{m1}+g_{m2}}{C_L} = \frac{200\mu\text{S}}{5\text{pF}} = 40\text{x}10^6 \text{ rads/sec or } \underline{\underline{6.28\text{MHz}}}$$

Problem 2 - (056412FE5)

A two-stage, BiCMOS op amp is shown. For the PMOS transistors, the model parameters are K_P'=50μA/V^2, V_{TP} = -0.7V and λ_P = 0.05V^{-1}. For the NPN BJTs, the model parameters are β_F = 100, V_{CE}(sat) = 0.2V, V_A = 25V, V_t = 26mV, I_s = 10fA and n=1. (a.) Identify which input is positive and which input is negative. (b.) Find the numerical values of differential voltage gain, $A_v(0)$, GB (in Hertz), the slew rate, SR, and the location of the RHP zero. (c.) Find the numerical value of the maximum and minimum input common mode voltages.



S01E2P1

Solution

(a.) The plus and minus signs on the schematic show which input is positive and negative.

(b.) The differential voltage gain, $A_v(0)$, is given as

$$A_v(0) = \frac{g_{m1}}{g_{ds2}+g_{o4}+g_{\pi 6}} \cdot \frac{g_{m6}}{g_{ds7}+g_{o6}} \qquad g_{m1} = g_{m2} = \sqrt{2\cdot 50\cdot 25\cdot 10} = 158.1\mu\text{S}$$

$$r_{ds2} = \frac{1}{\lambda_P I_D} = \frac{20}{25\mu\text{A}} = 0.8\text{M}\Omega,\ r_{o4} = \frac{V_A}{I_C} = \frac{25\text{V}}{25\mu\text{A}} = 1\text{M}\Omega,\ g_{m6} = \frac{I_C}{V_t} = \frac{100\mu\text{A}}{26\text{mV}} = 3846\mu\text{S}$$

$$r_{\pi 6} = \frac{\beta_F}{g_{m6}} = 26\text{k}\Omega, \quad r_{ds7} = \frac{1}{\lambda_P I_D} = \frac{20}{100\mu\text{A}} = 0.2\text{M}\Omega \text{ and } r_{o6} = \frac{V_A}{I_C} = \frac{25\text{V}}{100\mu\text{A}} = 0.25\text{M}\Omega$$

$\therefore \quad |A_v(0)|$ = [158.1(0.8||1||0.026)][3846(0.2||0.25)]= 3.888·427.36 = 1,659.6V/V

$$GB = \frac{g_{m1}}{C_c} = \frac{158.1\mu\text{S}}{5\text{pF}} = 31.62\text{x}10^6 \text{ rads/sec} \rightarrow GB = 5.0325\text{MHz}$$

$$SR = \frac{50\mu\text{A}}{5\text{pF}} = 10\text{V}/\mu\text{s}$$

$$\text{RHP zero} = \frac{g_{m6}}{C_c} = \frac{3.846\text{mS}}{5\text{pF}} = 769.24\text{x}10^6 \text{ rads/sec. (122MHz)}$$

(c.) The maximum input common mode voltage is given as

$$v_{icm}+ = V_{CC}-V_{DS5}(\text{sat}) - V_{SG1} = 1.5 - \sqrt{\frac{2\cdot 50}{50\cdot 10}} - 0.7 - \sqrt{\frac{2\cdot 25}{50\cdot 10}} = 0.8 - 0.447 - 0.316 =$$

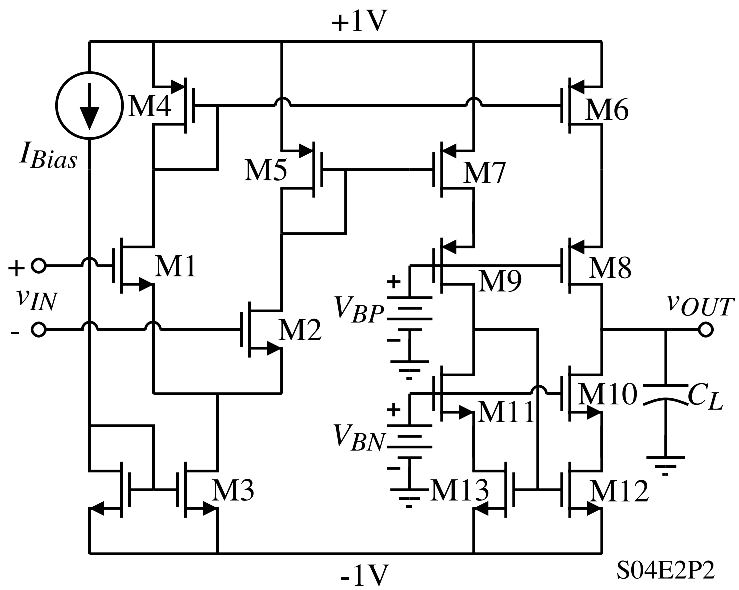
$\therefore \quad v_{icm}+$ = 0.0367V

$$v_{icm}- = -1.5 + V_{BE3} - V_{T1} = -1.5 + V_t \ln\left(\frac{25\mu\text{A}}{10\text{fA}}\right) - 0.7 = -2.2 + 0.5626 = -1.6374\text{V}$$

Problem 3 - (046412E2P2)

Design the values of W for each of the transistors of the op amp shown assuming that the channel lengths of all transistors are 1μm. Also design the values of the bias voltages V_{BN} and V_{BP}. The transistor model parameters are $K_N' = 300\mu A/V^2$, $V_{TN} = 0.5V$, and $K_P' = 70\mu A/V^2$, $V_{TP} = -0.5V$. Ignore the bulk effects. Use the following constraints among the transistor widths:

$W_1 = W_2$, $W_4 = W_5$, $W_6 = 10W_4$, $W_7 = 10W_5$, $W_8 = W_9$, and $W_{10} = W_{11} = W_{12} = W_{13}$



Round the values of the transistor widths to the nearest integer that meets or exceeds the specifications. Do not use safety factors or worst case in your design. The op amp specifications assuming a load capacitance of 5pF are:

$V_{icm}^+ = 0.75V$, $V_{icm}^- = -0.25V$, $GB = 200MHz$, $V_{out}^+ = 0.5V$, $V_{out}^- = -0.5V$, $SR = 100V/\mu s$

Solution

1.) $SR = 100V/\mu s \rightarrow I_{out} = C_L \cdot SR = 5\text{x}10^{-12} \cdot 10^8 = 500\mu A \rightarrow I_3 = 50\mu A$

2.) $V_{icm}^+ = 0.75V \rightarrow V_{SG4} = V_{DD} - V_{icm}^+ + V_{TN} = 1.0 - 0.75 + 0.5 = 0.75V$

$$V_{ON3} = 0.75 - 0.5 = 0.25V \quad \rightarrow \frac{W_4}{L_4} = \frac{2I_4}{K_N(V_{ON4})^2} = \frac{50}{70(0.25)^2} = 11.43 = 12$$

$\therefore \underline{\underline{W_4 = W_5 = 12\mu m}} \rightarrow \underline{\underline{W_6 = W_7 = 120\mu m}}$

3.) $GB = 200MHz$ or $GB = 400\pi\text{x}10^6$ rads/sec.

$$GB = \frac{g_{m1}}{C_L} 10 \quad \rightarrow \quad g_{m1} = \frac{GB \cdot C_L}{10} = \frac{400\pi\text{x}10^6 \cdot 5\text{x}10^{-12}}{10} = 628\mu S$$

$$\frac{W_1}{L_1} = \frac{g_{m1}^2}{2K_N I_1} = \frac{628^2}{50 \cdot 300} = 26.32 = 27 \quad \therefore \quad \underline{\underline{W_1 = W_2 = 27\mu m}}$$

4.) $V_{icm}^- = -0.25V \rightarrow V_{DS3} = V_{icm}^- V_{GS1} - V_{SS}$

$$V_{GS1} = \sqrt{\frac{2 \cdot 25}{300 \cdot 27}} + 0.5 = 0.5786V \quad \rightarrow V_{DS3} = -0.25 - 0.5786 + 1 = 0.1714V$$

$$\therefore \frac{W_3}{L_3} = \frac{2I_3}{K_N(V_{ON3})^2} = \frac{2 \cdot 50}{300(0.1714)^2} = 11.34 = 12 \quad \therefore \underline{\underline{W_3 = 12\mu m}}$$

Problem 3 - (046412E2P2) – Continued

5.) V_{out}^{+}=0.5V

$$V_{SD6} = \sqrt{\frac{2 \cdot I_6}{K_N (W_6/L_6)}} = \sqrt{\frac{2 \cdot 250}{70 \cdot 120}} = 0.243\text{V} \quad \rightarrow V_{SD8} = 0.256\text{V}$$

$$\therefore \quad \frac{W_8}{L_8} = \frac{2I_8}{K_P(V_{ON8})^2} = \frac{2 \cdot 250}{70(0.256)^2} = 108.99 = 109 \; \therefore \; \underline{\underline{W_8 = W_9 = 109\mu\text{m}}}$$

6.) V_{out}^{-}= -0.5V Let $V_{DS10} = V_{DS12}$ = 0.25V

$$\frac{W_{12}}{L_{12}} = \frac{2I_{12}}{K_N(V_{ON12})^2} = \frac{2 \cdot 250}{300(0.25)^2} = 26.67 = 27$$

$$\therefore \quad \underline{\underline{W_{10} = W_{11} = W_{12} = W_{13} = 27\mu\text{m}}}$$

6.) $V_{BN} = V_{ON10} + V_{ON12} + V_{TN} + V_{SS}$ = 0.25V+0.25V+0.5V-1V = 0V

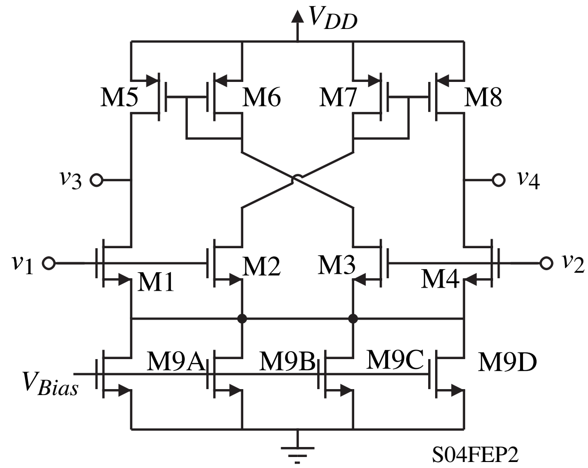
$\therefore \; \underline{\underline{V_{BN} = 0\text{V}}}$

$V_{BP} = V_{DD} - V_{ON6} - V_{ON8} + |V_{TP}|$ = 1V – 0.25V – 0.25V – 0.5V = 0V

$\therefore \; \underline{\underline{V_{BP} = 0\text{V}}}$

Problem 4 - (046412FE2)

A differential-in, differential-out amplifier is shown that eliminates the need for matching sinks and sources. Assume that all W/L values are equal and that each transistor has approximately the same current flowing through it. If all transistors are in the saturation region, find an algebraic expression for the voltage gain, v_{out}/v_{in}, and the differential output resistance, R_{out}, where $v_{out} = v_3 - v_4$ and $v_{in} = v_1 - v_2$. R_{out} is the resistance seen between the output terminals.



Solution

Using the schematic approach to small signal analysis, we apply $v_{in}/2$ positively to M1 (M2) and negatively to M4 (M3). The resulting ac currents are shown on the schematic. At node, v_3, these currents flow out of a resistance whose value is $r_{ds1}||r_{ds5}$ to give v_3 as

$$v_3 = -\left(\frac{g_{m1}+g_{m3}}{2(g_{ds1}+g_{ds5})}\right) v_{in} = \frac{-g_{m1}v_{in}}{g_{ds1}+g_{ds5}}$$

Similarly for v_4, we get

$$v_4 = \left(\frac{g_{m2}+g_{m4}}{2(g_{ds2}+g_{ds8})}\right) v_{in} = \frac{g_{m2}v_{in}}{g_{ds2}+g_{ds8}} \Rightarrow \boxed{\frac{v_{out}}{v_{in}} = -\frac{g_{m1}+g_{m2}}{g_{ds1}+g_{ds5}} = -\frac{g_{m1}+g_{m2}}{g_{ds4}+g_{ds8}}}$$

The output resistance seen differentially is the sum of the resistances seen to ground which is

$$\boxed{R_{out} = \frac{1}{g_{ds1}+g_{ds5}} + \frac{1}{g_{ds4}+g_{ds8}} = r_{ds1}||r_{ds5} + r_{ds4}||r_{ds8}}$$

Problem 5 - (036412E2P1)

A CMOS op amp is shown. All W/L values of all transistors are 10μm/1μm. Assume that $K_N' = 110\mu A/V^2$, $K_P' = 50\mu A/V^2$, $V_{TN} = 0.7V$, $V_{TP} = -0.7V$, $\lambda_N = 0.04V^{-1}$, and $\lambda_P = 0.05V^{-1}$. Find the low frequency differential voltage gain, v_{out}/v_{in}, the gainbandwidth, *GB*, the slew rate, *SR*, and the power dissipation, P_{diss} if $V_{DD} = 2V$.

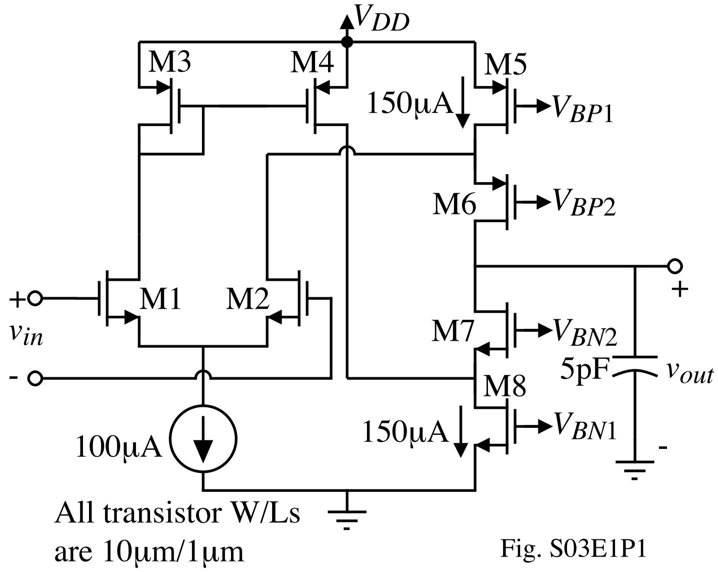


Fig. S03E1P1

Solution

The small-signal voltage gain can be expressed as,

$$\frac{v_{out}}{v_{in}} = g_{m1}R_{out} = g_{m2}R_{out}{}^*$$

where $R_{out} \approx [g_{m7}r_{ds7}(r_{ds4} || r_{ds8})] || [g_{m6}r_{ds6}(r_{ds2} || r_{ds5})]$

Evaluating the small signal parameters,

$$g_{m1} = g_{m2} = \sqrt{2\cdot110\cdot10\cdot50} = 331.7\mu S,\ r_{ds1} = r_{ds2} = (25/50)M\Omega = 0.5M\Omega$$

$$g_{m6} = \sqrt{2\cdot50\cdot10\cdot100} = 316.2\mu S,\ r_{ds6} = (20/100)M\Omega = 0.2M\Omega$$

$$r_{ds5} = (20/150)M\Omega = 0.133M\Omega,\ \ r_{ds4} = (20/50)M\Omega = 0.4M\Omega$$

$$g_{m7} = \sqrt{2\cdot110\cdot10\cdot100} = 469\mu S,\ r_{ds7} = (25/100)M\Omega = 0.25M\Omega$$

$$r_{ds8} = (25/150)M\Omega = 0.167M\Omega$$

$$\therefore \quad R_{out} \approx [469\cdot0.25(0.4||0.167)]||[316.2\cdot0.2(0.5||0.133)]M\Omega$$

$$= (13.796||6.644)M\Omega = 4.484M\Omega$$

$$\frac{v_{out}}{v_{in}} = 331.7\cdot4.484 = \underline{\underline{1487\ V/V}}$$

$$GB = \frac{g_{m1}}{C_L} = \frac{331.7\text{x}10^{-6}}{5\text{x}10^{-12}} = 66.33\text{x}10^{+6} \rightarrow \underline{\underline{10.56MHz}}$$

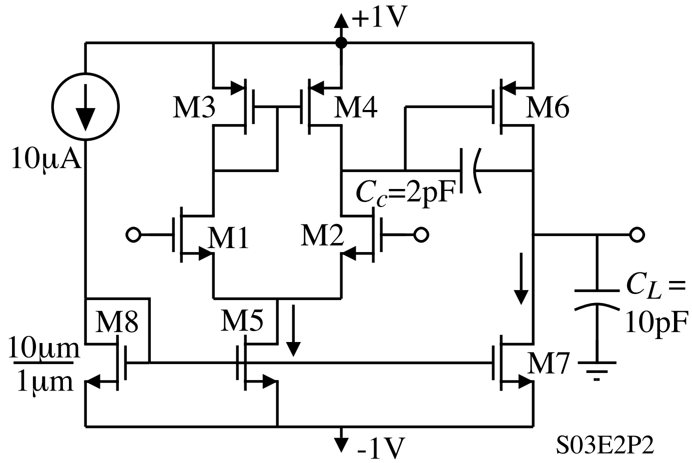
$$SR = \frac{100\mu A}{C_L} = \frac{100\text{x}10^{-6}}{5\text{x}10^{-12}} = \underline{\underline{20V/\mu s}}$$

$$P_{diss} = 2(50\mu A+50\mu A+150\mu A) = \underline{\underline{500\mu W}}$$

* This expression ignores the fact that about half the signal is lost due to the input resistances at the sources of M6 and M7 are at an r_{ds} level.

Problem 6 - (036412E2P3)

For the CMOS op amp shown, assume the model parameters for the transistors are $K_N' = 110\mu A/V^2$, $K_P' = 50\mu A/V^2$, $V_{TN} = 0.7V$, $V_{TP} = -0.7V$, $\lambda_N = 0.04V^{-1}$, and $\lambda_P = 0.05V^{-1}$. Let all transistor lengths be $1\mu m$ and design the widths of every transistor and the dc currents I_5 and I_7 to satisfy the following specifications:



Slew rate = 10V/μs

+ICMR = 0.8V

-ICMR = 0V

GB = 10MHz

Phase margin = 60° ($g_{mII} = 10g_{mI}$ and $V_{SG4}=V_{SG6}$)

Solution

Slew rate → $I_5 = SR\cdot C_L = 10V\mu s\cdot 10pF = \underline{20\mu A}$ → $W_5 = 20\mu m$ (check *-ICMR* later)

+ICMR → $0.8 = 1 - V_{SG3} + 0.7$ → $V_{SG3} = 0.9$ → $V_{SD3}(\text{sat}) = 0.2V$

$$\frac{W_3}{L_3} = \frac{W_4}{L_4} = \frac{2I_3}{K_P(V_{SD3}(\text{sat}))^2} = \frac{2\cdot 10}{50(0.2)^2} = 10 \ \rightarrow\ W_3 = W_4 = \underline{10\mu m}$$

$$GB \rightarrow \frac{g_{m1}}{C_c} = GB \rightarrow g_{m1} = GB\cdot C_c = 20\pi x10^6\cdot 2x10^{-12} = 40\pi\ \mu S$$

$$g_{m1} = \sqrt{2K_N\frac{W_1}{L_1}I_1} \rightarrow g_{m1}{}^2 = 2K_N\frac{W_1}{L_1}I_1 \rightarrow \frac{W_1}{L_1} = \frac{g_{m1}{}^2}{2K_NI_1} = \frac{(40\pi)^2}{2\cdot 110\cdot 10} = 7.17$$

$W_1 = W_2 = \underline{7.17\mu m}$

$$\text{-ICMR} \rightarrow 0 = V_{GS1} + V_{DS5}(\text{sat}) - 1 \rightarrow V_{DS5}(\text{sat}) = 1 - V_{GS1} = 1 - \sqrt{\frac{2I_1}{K_N(W_1/L_1)}} - V_{TN}$$

$$V_{DS5}(\text{sat}) = 1 - \sqrt{\frac{20}{110\cdot 7.17}} + 0.7 = 1 - 0.859 = 0.141V$$

$$\frac{W_5}{L_5} = \frac{2I_5}{K_N(V_{DS5}(\text{sat}))^2} = \frac{2\cdot 10}{110(0.141)^2} = 18.29 \ \rightarrow\ W_5 = 18.29\mu m \rightarrow W_5 = \underline{20\mu m}$$

60° phase margin → $g_{m6} = 10\ g_{m1} = 400\pi\ \mu S$

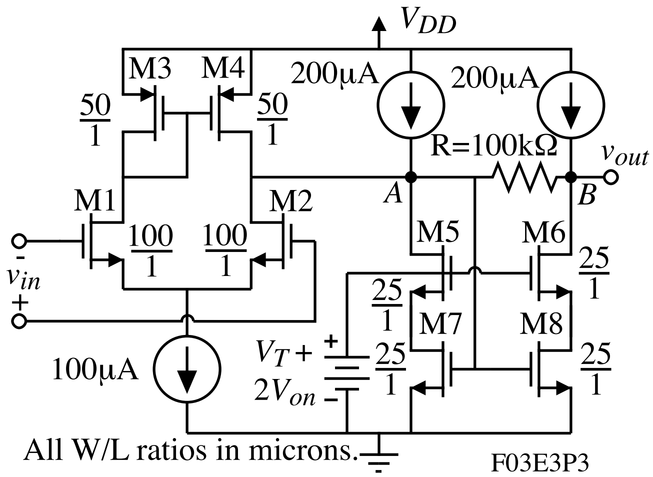
Also, $g_{m4} = \sqrt{2\cdot 50\cdot 10\cdot 10} = 100\mu S$ → $W_6 = \frac{400\pi}{100}10 = 40\pi = \underline{125.66\ \mu m}$

$$I_6 = \frac{g_{m6}{}^2}{2K_P(W_6/L_6)} = \frac{(400\pi)^2}{100\cdot 125.66} = \underline{125.66\mu A}$$

$$W_7 = W_5\frac{I_6}{I_5} = 20\frac{125.66}{20} = \underline{125.66\mu m}$$

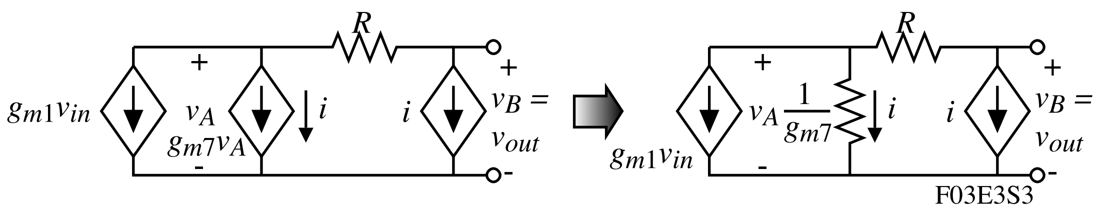
Problem 7 - (036412E3P3)

A low-gain, high-bandwidth voltage amplifier is shown. Find the low frequency voltage gain, v_{out}/v_{in}, and the unity-gainbandwidth, GB, if the sum of the capacitance connected to nodes A and B is 0.5pF each. Assume that the independent current sources used have infinite resistance. The transistor model parameters are K_N' =110μA/V^2, V_{TN} = 0.7V, λ_N=0, K_P' =50μA/V^2, V_{TP}= -0.7V, λ_P=0.



Solution

The low frequency voltage gain can be found by inspection as $0.5g_{m1}R$. For those of you not into "found by inspection" the following small-signal model is useful.



$$v_{out} = i\left(-R + \frac{1}{g_{m7}}\right) = -\frac{g_{m1}}{2}\left(-R + \frac{1}{g_{m7}}\right)v_{in} \quad g_{m1} = \sqrt{2\cdot110\cdot100\cdot50} = 1.048\text{mS}$$

$$g_{m7} = \sqrt{2\cdot110\cdot25\cdot200} = 1.048\text{mS} \qquad \therefore \quad \frac{v_{out}}{v_{in}} = -\frac{1.048}{2}\left(-100 + \frac{1}{1.048}\right) = \underline{\underline{51.9\text{ V/V}}}$$

The approach to the second part of the problem will be to find the poles at A and B. The resistance to ground at node A is effectively $R_A \approx 1/g_{m7}$ = 1/1.048mS and at node B to ground is $R_B = R$ = 100kΩ. However, because of the shunt feedback at node B (and A) with a loop gain of 1, the output resistance is really 50kΩ. Therefore,

$$p_A = \frac{2g_{m7}}{R_A} = \frac{2\cdot1.048\text{mS}}{0.5\text{pF}} = 4.192\text{x}10^9 \text{ rads/sec.}$$

and

$$p_B = \frac{2}{R_BC_B} = \frac{2}{100\text{k}\Omega\cdot0.5\text{pF}} = 40\text{x}10^6 \text{ rads/sec.}$$

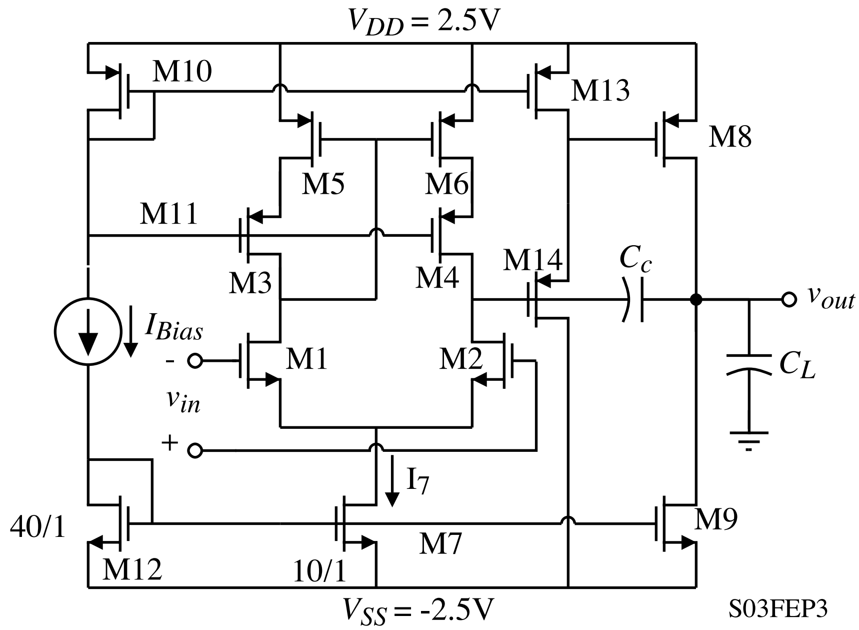
$\therefore$ $GB = 51.9\cdot40\text{x}10^6 = 2076\text{x}10^6$ rads/sec → $\underline{\underline{GB = 330.4 \text{ MHz}}}$

The gainbandwidth can also be calculated using the principle that $GB = g_m/C$ where g_m is the transconductance that converts the input voltage to current (g_{m1}) and C is the capacitance that causes the dominant pole (0.5pF). Thus,

$GB = 1.048\text{mS}/0.5\text{pF} = 2096\text{x}10^6$ rads/sec → $GB = 333.6$ MHz

Problem 8 - (035412FE3)

An internally-compensated, cascode op amp is shown. (a) Derive an expression for the common-mode input range. (b) Find W_1/L_1, W_2/L_2, W_5/L_5, and W_6/L_6 when I_{BIAS} is 80 μA and the input CMR is -1.25 V to +2 V. Use $K'_N = 110\ \mu A/V^2$, $K'_p = 50\ \mu A/V^2$ and $|V_T| = 0.6$ to 0.8V. (c.) Develop an expression for the small-signal differential-voltage gain and output resistance of the cascode op amp.



Solution

(a.) $V_{icm}(\min) = V_{SS} + V_{DS7}(\text{sat}) + V_{DS1}(\text{sat}) + V_{T1}(\max)$

and

$V_{icm}(\max) = V_{DD} - V_{SD5}(\text{sat}) - V_{T5}(\max) + V_{T1}(\min)$ (we will ignore that M8 and M14 cause a more severe upper ICM limit)

$\therefore \quad ICMR = V_{icm}(\max) - V_{icm}(\min)$

$$ICMR = (V_{DD}-V_{SS})+[V_{DS7}(\text{sat})+V_{DS1}(\text{sat})+V_{T1}(\max)]-[V_{SD5}(\text{sat})+V_{T5}(\max)-V_{T1}(\min)]$$

(b.) $I_7 = \frac{1}{4} I_{BIAS} = 20\mu A$ Using $V_{DS}(\text{sat}) = \sqrt{\frac{2I}{K'(W/L)}}$ and $\frac{W}{L} = \frac{2I}{K'[V_{DS}(\text{sat})]^2}$ gives,

$V_{DS7}(\text{sat}) = 0.191\text{V} \rightarrow V_{icm}(\min) = -2.5\text{V}+0.191\text{V}+V_{DS1}(\text{sat})+0.8\text{V} \rightarrow V_{DS1}(\text{sat}) = 0.259\text{V}$

$$\therefore \quad \frac{W_1}{L_1} = \frac{W_2}{L_2} = \frac{20\mu A}{110 \cdot 0.259^2} = \underline{\underline{2.70}}$$

$V_{icm}(\max) = 2.0\text{V} = 2.5\text{V} - V_{SD5}(\text{sat}) - 0.6\text{V} + 0.8\text{V} \rightarrow V_{SD5}(\text{sat}) = 0.3\text{V}$

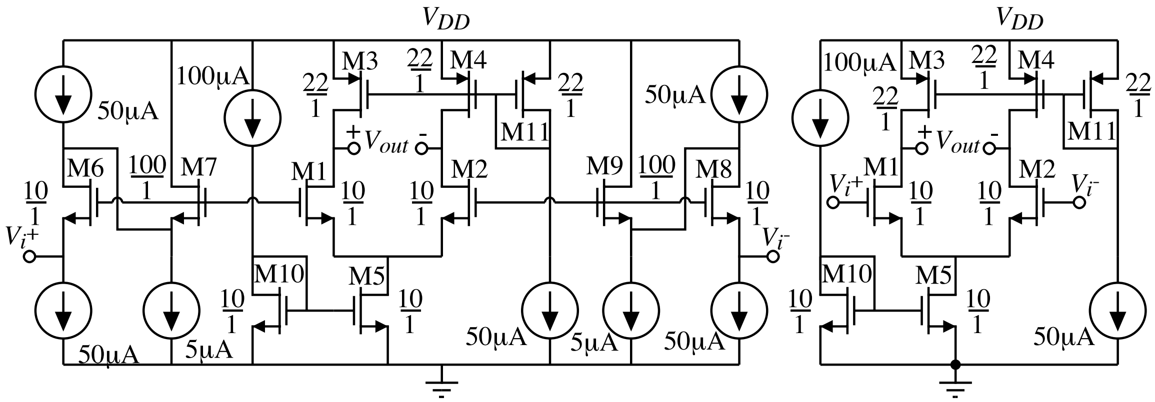
$$\therefore \quad \frac{W_5}{L_5} = \frac{W_6}{L_6} = \frac{20\mu A}{50 \cdot 0.3^2} = \underline{\underline{4.44}}$$

(c.) By inspection, we can write:

$$A_v = (-g_{m1} r_{ds2})\left(\frac{g_{m14}}{g_{m14}+g_{ds13}+g_{ds14}}\right)\left(\frac{-g_{m8}}{g_{ds8}+g_{ds9}}\right)$$

Problem 9 – (036412FE4)

George P. Burdell has submitted the following input stage as a wide range ICMR stage. Assuming that the transistor model parameters are K_N' =110μA/V^2, V_{TN} = 0.7V, λ_N=0.04V^{-1}, K_P' =50μA/V^2, V_{TP}= -0.7V, λ_P=0.05V^{-1}, your job is to check this op amp out. In particular, what is the upper and lower input common mode voltages, what is the minimum power supply that gives zero input common mode range, what is the small-signal voltage gain, and compare this input stage with the classical differential input stage (list advantages and disadvantages).



The George P. Burdell Approach Classical Approach

Solution

GPB Differential Input Stage:

$$V_{icm}^+ = V_{DD} - V_{SD3}(\text{sat}) + V_{T1} - V_{GS6}(50\mu\text{A}) = V_{DD} - V_{SD3}(\text{sat}) + V_{T1} - V_{GS6}(\text{sat}) - V_{T6}$$

$$V_{icm}^+ = V_{DD} - V_{SD3}(\text{sat}) - V_{GS6}(\text{sat})$$

$$V_{icm}^- = V_{DS5}(\text{sat}) + V_{GS1}(50\mu\text{A}) - V_{GS6}(50\mu\text{A}) = V_{DS5}(\text{sat}) + V_{DS1}(\text{sat}) - V_{DS6}(\text{sat})$$

$$V_{DS1}(\text{sat}) = V_{DS6}(\text{sat}) = \sqrt{\frac{2\cdot 50}{110\cdot 10}} = 0.301\text{V}, \quad V_{DS5}(\text{sat}) = \sqrt{\frac{2\cdot 100}{110\cdot 10}} = 0.426\text{V},$$

and $V_{SD3}(\text{sat}) = \sqrt{\frac{2\cdot 50}{50\cdot 22}} = 0.301\text{V}$

∴ $V_{icm}^+ = \underline{\underline{V_{DD} - 0.602\text{V}}}$ and $V_{icm}^- = 0.426 + 0.301 - 0.301 = \underline{\underline{0.426\text{V}}}$

Note that $V_{DS6} = V_{GS6}-V_{GS7}$ = 1.001-0.73 = 0.271 < V_{DS6}(sat) so that M6 is slightly in the active region but this is not a problem.

The minimum V_{DD} is found by letting $V_{icm}^+ = V_{icm}^-$ which gives $V_{DD}(\text{min})$ = $\underline{\underline{1.028\text{V}}}$

The small-signal voltage gain is $A_{vd} = \dfrac{V_{out}}{V_i^+ - V_i^-} = \dfrac{-g_{m1}}{g_{ds1} + g_{ds3}} = \dfrac{-g_{m2}}{g_{ds2} + g_{ds4}}$

Problem 9 – (036412FE4) Continued

Classical Differential Input Stage:

$V_{icm}^{+} = V_{DD} - V_{SD3}(\text{sat}) + V_{T1} = V_{DD} - 0.301 + 0.7 = \underline{\underline{V_{DD} + 0.4\text{V}}}$

$V_{icm}^{-} = V_{DS5}(\text{sat}) + V_{GS1}(50\mu\text{A}) = \underline{\underline{1.427\text{V}}}$

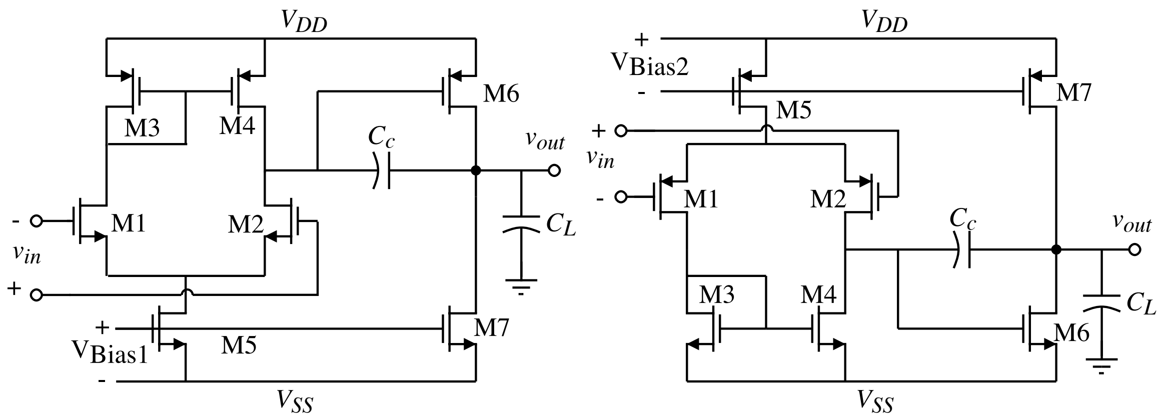
$V_{DD}(\text{min}) = \underline{\underline{1.027\text{V}}}$ and the small-signal voltage gain is the same.

Comparison between the two approaches:

Characteristic	GBP Differential Amplifier	Classical Differential Amplifier
V_{icm}^{+}	V_{DD} – 0.602V	V_{DD} + 0.4V
V_{icm}^{-}	0.426V	1.427V
V_{DD}(min)	1.028V	1.027V
P_{diss}	V_{DD}(360µA)	V_{DD}(250µA)
Noise	Higher	Lower
Input Offset Voltage	Larger	Smaller
Small-signal gain	Same	Same
Useable ICMR	Within power supply	Outside of power supply

Problem 10 - (026412E2P1)

The two op amps shown have identical voltages and currents for each transistor. The W/L values are identical for the transistors with the same number. Assume that $K_N' = 110\mu A/V^2$, $K_P' = 50\mu A/V^2$, $V_{TN} = 0.7V$, $V_{TP} = -0.7V$, $\lambda_N = 0.04V^{-1}$, and $\lambda_P = 0.05V^{-1}$. Fill in the blanks in the table with the entries chosen from the categories of "same", "lower", or "higher".



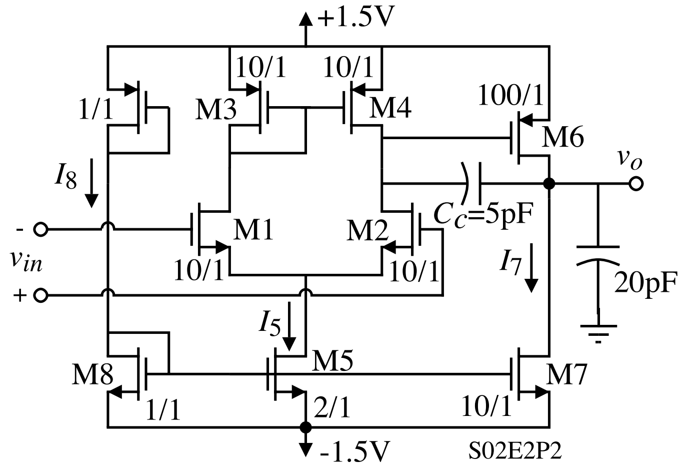
N-channel input Op Amp P-channel input Op Amp Fig. S02E2P1

Characteristic	N-Channel Input Op Amp	P-Channel Input Op Amp
Small-signal voltage gain	$\sqrt{4K_NS_1I_1K_PS_6I_6}$ (same)	$\sqrt{4K_PS_1I_1K_NS_6I_6}$ (same)
Small-signal output resistance	$(g_{dsN}+g_{dsP})^{-1}$ (same)	$(g_{dsN}+g_{dsP})^{-1}$ (same)
Gain-bandwidth	$\sqrt{2K_NS_1I_1}/C_c$ (higher)	$\sqrt{2K_PS_1I_1}/C_c$ (lower)
Upper input common mode voltage	$V_{DD}-V_{SGP}+V_{TN}$ (hi)	$V_{DD}-V_{SDP}(sat)-V_{SGP}$ (lo)
Lower input common mode voltage	$V_{SS}-V_{DSN}(sat)-V_{GSN}$ (lo)	$V_{SS}-V_{GSN}+V_{TP}$ (hi)
Maximum positive output voltage*	Lower ($I_6 \neq 0$)	Higher (I_7=0 if I_6=0)
Maximum negative output voltage*	Higher (I_7=0 if I_6=0)	Lower ($I_6 \neq 0$)
Phase Margin – 90°	$-\tan^{-1}\left(\frac{g_{mN}}{g_{mP}}\cdot\frac{C_L}{C_c}\right)-\tan^{-1}\left(\frac{g_{mN}}{g_{mP}}\right)$ (Lower)	$-\tan^{-1}\left(\frac{g_{mP}}{g_{mN}}\cdot\frac{C_L}{C_c}\right)-\tan^{-1}\left(\frac{g_{mP}}{g_{mN}}\right)$ (Higher)
Slew Rate (Assume due to C_c)	I_5/C_c (same)	I_5/C_c (same)
Power dissipation	$(V_{DD}-V_{SS})(I_5+I_7)$ (same)	$(V_{DD}-V_{SS})(I_5+I_7)$ (same)
Positive (V_{DD}) PSRR	Lower	Higher
Negative (V_{SS}) PSRR	Higher	Lower

* The transistors are not necessarily saturated for this characteristic.

Problem 11 - (026412E2P2)

For the op amp shown, assume all transistors are operating in the saturation region and find (a.) the dc value of I_5, I_7 and I_8, (b.) the low frequency differential voltage gain, $A_{vd}(0)$, (c.) the GB in Hz, (d.) the negative slew rates, (e.) the power dissipation, and (f.) the phase margin assuming that the open-loop unity gain is 1MHz. Assume the transistor parameters are $K_N' = 110\mu A/V^2$, $V_T = 0.7V$, and $\lambda_N = 0.04V^{-1}$ for the NMOS; $K_P' = 50\mu A/V^2$, $V_T = -0.7V$, and $\lambda_P = 0.05V^{-1}$ for the PMOS.



Solution

(a.) $3V = \sqrt{\frac{2\cdot I_8}{K_P\cdot 1}} + 0.7 + \sqrt{\frac{2\cdot I_8}{K_N\cdot 1}} + 0.7 \Rightarrow 1.6 = \sqrt{I_8}\left(\frac{1}{\sqrt{25}} + \frac{1}{\sqrt{55}}\right) \Rightarrow I_8 = 22.8\mu A$

$\therefore$ $I_8 = 22.8\mu A \quad I_5 = 2I_8 = 45.7\mu A$ and $I_7 = 10I_8 = 228\mu A$

(b.) $A_v(0) = g_{m1}(r_{ds2}||r_{ds4})g_{m6}(r_{ds6}||r_{ds7})$

$g_{m1} = \sqrt{2\cdot K_N\cdot 10\cdot I_8} = 224\mu S$, $g_{m6} = \sqrt{2\cdot K_P\cdot 100\cdot I_7} = 1510\mu S$, $r_{ds2} = \frac{25}{22.8} = 1.096M\Omega$,

$r_{ds4} = \frac{20}{22.8} = 0.877M\Omega$, $r_{ds6} = \frac{20}{228} = 0.088M\Omega$, and $r_{ds7} = \frac{25}{228} = 0.1096M\Omega$.

$\therefore$ $A_v(0) = (224\mu S)(0.4872M\Omega)(1510\mu S)(0.0488M\Omega) = 8042$ V/V

(c.) $GB = \frac{g_{m1}}{C_c} = \frac{224\mu S}{5pF} = 44.8$Mradians/sec = 7.13MHz

(d.) Due to C_c: $|SR| = \frac{I_5}{C_c} = \frac{45.7\mu A}{5pF} = 9.14$ V/μs

Due to C_L: $|SR| = \frac{I_7 - I_5}{C_L} = \frac{228\mu A - 45.7\mu A}{20pF} = 9.12V/\mu s$ $\quad\therefore$ $|SR| = 9.12V/\mu s$

(e.) Power Dissipation = $3(I_8+I_5+I_7) = 3(296.4\mu A) = 0.889mW$

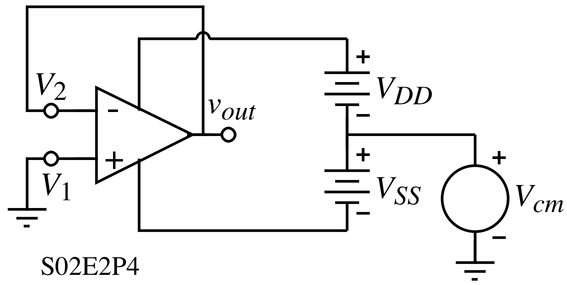
(f.) Phase margin = $180° - \tan^{-1}\left(\frac{GB}{GB/A_v(0)}\right) - \tan^{-1}\left(\frac{GB}{p_2}\right) - \tan^{-1}\left(\frac{GB}{z}\right)$

$p_2 = \frac{g_{m6}}{C_L} = 75.5\times10^6$ rads/sec and $z = \frac{g_{m6}}{C_c} = 302\times10^6$ rads/sec

$\therefore$ Phase margin = $90° - \tan^{-1}\left(\frac{6.28}{75.5}\right) - \tan^{-1}\left(\frac{6.28}{302}\right) = 84°$

Problem 12 - (026412E2P4)

A possible scheme for simulating the *CMRR* of an op amp is shown. Find the value of V_{out}/V_{cm} and show that it is approximately equal to 1/*CMRR*. What problems might result in the actual implementation of this circuit to measure *CMRR*?



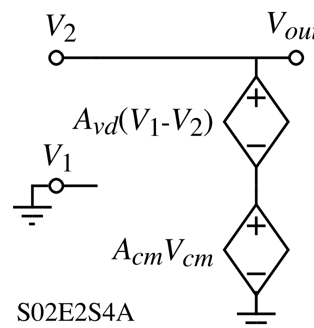
S02E2P4

Solution

The model for this circuit is shown. We can write that

$$V_{out} = A_{vd}(V_1\text{-}V_2) + A_{cm}V_{cm}$$

$$= -A_{vd}V_{out} + A_{cm}V_{cm}$$



S02E2S4A

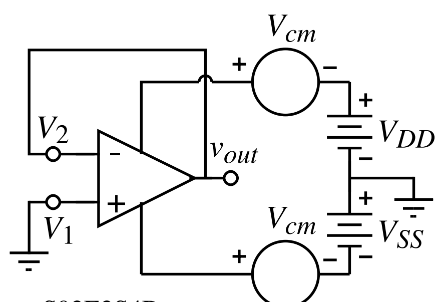
Thus,

$$V_{out}(1+A_{vd}) = A_{cm}V_{cm}$$

or

$$\frac{V_{out}}{V_{cm}} = \frac{A_{cm}}{1+A_{vd}} \approx \frac{A_{cm}}{A_{vd}} = \frac{1}{CMRR}$$

The potential problem with this method is that $PSRR^+$ is not equal to $PSRR^-$. This can be seen by moving the V_{cm} through the power supplies so it appears as power supply ripple as shown below. This method depends on the fact that the positive and negative power supply ripple will cancel each other.



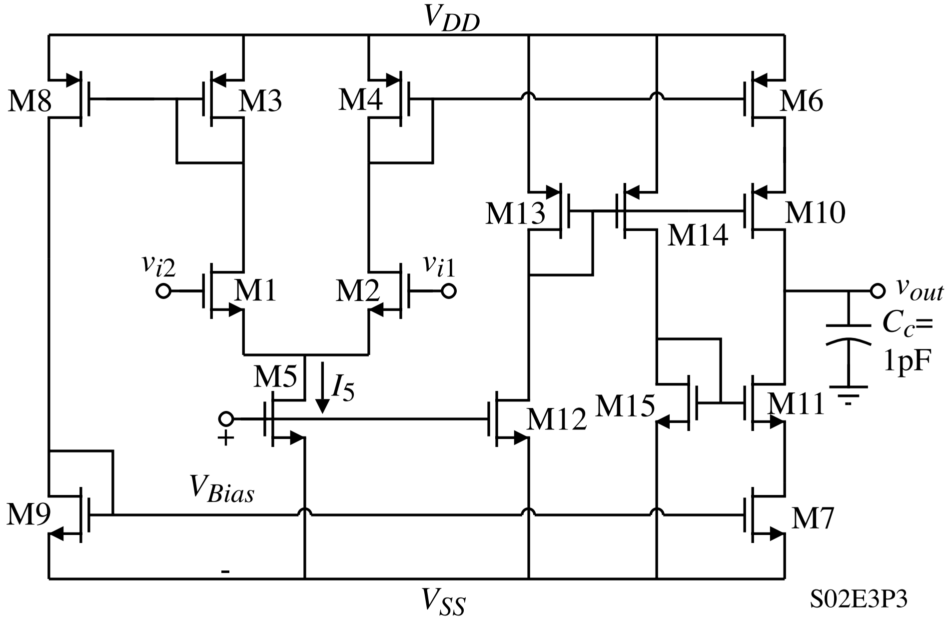
S02E2S4B

Problem 13 - (026412E3P3)

Calculate the small-signal voltage gain, the *SR* (C_L = 1pF), and the P_{diss} for the op amp shown where I_5 = 100nA and all transistors M1-M11 have a *W*/*L* of 10μm/1μm and $V_{DD} = -V_{SS}$ = 1.5V. If the minimum voltage across the drain-source of M6 and M7 are to be 0.1V, design the *W*/*L* ratios of M12-M15 that give the maximum plus and minus output voltage swing assuming that transistors M12 and M15 have a current of 50nA. The transistors are working in weak inversion and are modeled by the large signal model of

$$i_D = \frac{W}{L} I_{DO} \exp\left(\frac{v_{GS}}{nV_t}\right)$$

where I_{DO} = 2nA for PMOS and NMOS and n_P = 2.5 and n_N = 1.5. Assume V_t = 26mV and λ_N=0.4V^{-1} and λ_P=0.5V^{-1}.



Solution

The small-signal voltage gain, A_v, is $g_{m1}R_{out}$ (see end of solution) where,

$$R_{out} = (r_{ds6}g_{m10}r_{ds10})||(r_{ds7}g_{m11}r_{ds11})$$

With the currents and *W*/*L* ratios of transistors M1 through M11 known, we get

$$g_{m1} = g_{m11} = \frac{50\text{nA}}{1.5\cdot 26\text{mV}} = 1.282\mu\text{S} \quad \text{and} \quad r_{ds7} = r_{ds11} = \frac{10^9}{0.04\cdot 50} = 0.5\text{x}10^9\Omega$$

$$g_{m10} = \frac{50\text{nA}}{2.5\cdot 26\text{mV}} = 0.769\mu\text{S} \quad \text{and} \quad r_{ds6} = r_{ds10} = \frac{10^9}{0.05\cdot 50} = 0.4\text{x}10^9\Omega$$

$$R_{out} = (0.4\text{x}10^9\cdot 1.282\text{x}10^{-6}\cdot 0.4\text{x}10^9)||(0.5\text{x}10^9\cdot 0.769\text{x}10^{-6}\cdot 0.5\text{x}10^9) = 9.924\text{x}10^{10}\Omega$$

$$\therefore \quad A_v = 1.282\text{x}10^{-6}\cdot 9.924\text{x}10^{10} = \underline{127{,}726 \text{ V/V}}$$

$$SR = \frac{100\text{nA}}{1\text{pF}} = \underline{0.1\text{V}/\mu\text{s}}$$

$$P_{diss} = 3\text{V}(50\text{nA}\cdot 6) = \underline{0.9\mu\text{W}}$$

Problem 13 - (026412E3P3) - Continued

Design of the *W*/*L*'s of M12 through M15:

To get 50nA in M12 means the $W_{12}/L_{12} = 0.5(W_5/L_5) = \underline{\underline{5\mu\text{m}/1\mu\text{m}}}$

M15:

$$V_{GS11} = n_N V_t \ln\left(\frac{I_D}{I_{DO}(W/L)}\right) = 1.5\cdot 0.026 \ln\left(\frac{50}{2\cdot 10}\right) = 0.0357\text{V}$$

$$\therefore \quad V_{GS15} = 0.1 + 0.0357 = 0.1357\text{V} \;\rightarrow\; \frac{W_{15}}{L_{15}} = \frac{50\text{nA}}{2\text{nA}\cdot\exp\left(\frac{135.7}{1.5\cdot 26}\right)} = \underline{\underline{0.77\mu\text{m}/1\mu\text{m}}}$$

M13 and M14:

$$V_{SG10} = n_P V_t \ln\left(\frac{I_D}{I_{DO}(W/L)}\right) = 2.5\cdot 0.026 \ln\left(\frac{50}{2\cdot 10}\right) = 0.0596\text{V}$$

$$\therefore \quad V_{GS13} = 0.1 + 0.0596 = 0.1596\text{V} \;\rightarrow\; \frac{W_{13}}{L_{13}} = \frac{50\text{nA}}{2\text{nA}\cdot\exp\left(\frac{159.6}{1.5\cdot 26}\right)} = 2.146\mu\text{m}/1\mu\text{m}$$

Thus

$$\frac{W_{13}}{L_{13}} = \frac{W_{14}}{L_{14}} = \underline{\underline{2.146\mu\text{m}/1\mu\text{m}}}$$

Comments on the small-signal gain:

It is much easier to use the expression $g_{m1}R_{out}$ for the small-signal voltage gain. However, some prefer the following expression,

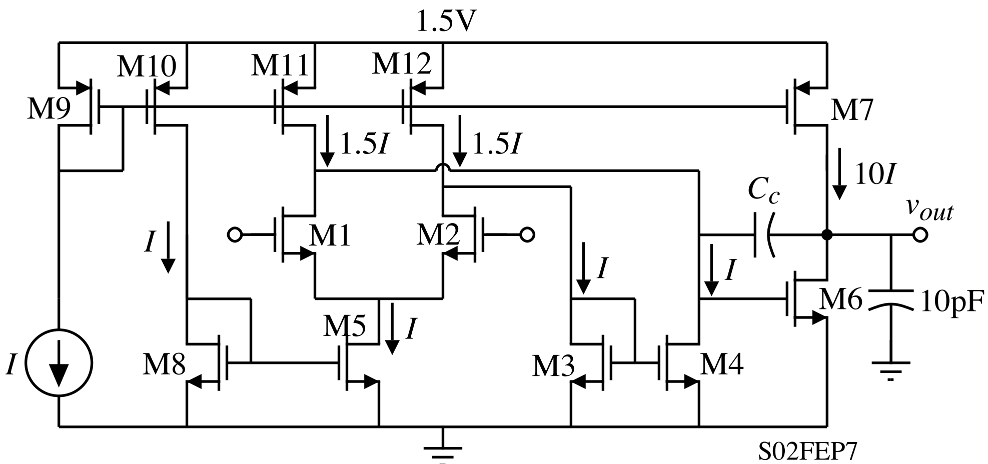
$$v_{out} = \left(\frac{g_{m1}\cdot g_{m8}\cdot g_{m7}}{2g_{m3}\cdot g_{m9}} + \frac{g_{m2}\cdot g_{m6}}{2g_{m4}}\right) R_{out}$$

which is equivalent since g_{m3}=g_{m8}, g_{m7}=g_{m9}, g_{m4}=g_{m6}, and g_{m1}=g_{m2}.

Problem 14 – (026412FE7)

A CMOS op amp capable of operating from 1.5V power supply is shown. All device lengths are 1μm and are to operate in the saturation region. Design all of the W values of every transistor of this op amp to meet the following specifications.

Slew rate = ±10V/μs	V_{out}(max) = 1.25V	V_{out}(min) = 0.75V
V_{ic}(min) = 1V	V_{ic}(max) = 2V	GB = 10MHz
Phase margin = 60° when the output pole = 2GB and the RHP zero = 10GB. Keep the mirror pole ≥ 10GB (C_{ox} = 0.5fF/μm^2).		



Your design should meet or exceed these specifications. Ignore bulk effects in this problem and summarize your W values to the nearest micron, the value of C_c(pF), and I(μA) in the following table. Use the following model parameters: K_N'=24μA/V^2, K_P' = 8μA/V^2, V_{TN} = - V_{TP} = 0.75V, λ_N = 0.01V^{-1} and λ_P = 0.02V^{-1}.

Solution

1.) p_2=2GB ⇒ $g_{m6}/C_L=2g_{m1}/C_c$ and z=10GB ⇒ $g_{m6}=10g_{m1}$. ∴ $\boxed{C_c = C_L/5 = 2\text{pF}}$

2.) $I = C_c \cdot SR = (2\text{x}10^{-12}) \cdot 10^7 = 20\mu\text{A}$ ∴ $\boxed{I = 20\mu\text{A}}$

3.) $GB = g_{m1}/C_c \Rightarrow g_{m1} = 20\pi\text{x}10^6 \cdot 2\text{x}10^{-12} = 40\pi\text{x}10^{-6} = 125.67\mu\text{S}$

$$\frac{W_1}{L_1} = \frac{W_2}{L_2} = \frac{g_{m1}^2}{2K_N(I/2)} = \frac{(125.67\text{x}10^{-6})^2}{2 \cdot 24\text{x}10^{-6} \cdot 10\text{x}10^{-6}} = 32.9 \Rightarrow \boxed{W1 = W_2 = 33\mu\text{m}}$$

4.) $V_{ic}(\min) = V_{DS5}(\text{sat.}) + V_{GS1}(10\mu\text{A}) = 1\text{V} \rightarrow V_{DS5}(\text{sat.}) = 1 - \sqrt{\frac{2 \cdot 10}{24 \cdot 33}} - 0.75 = 0.0908$

$$V_{DS5}(\text{sat}) = 0.0908 = \sqrt{\frac{2 \cdot I}{K_N S_5}} \rightarrow W_5 = \frac{2 \cdot 20}{24 \cdot (0.0908)^2} = 201.9\mu\text{m} \quad \boxed{W_5 = 202\mu\text{m}}$$

5.) $V_{ic}(\max) = V_{DD} - V_{SD11}(\text{sat}) + V_{TN} = 1.5 - V_{SD11}(\text{sat}) + 0.75 = 2\text{V} \rightarrow V_{SD11}(\text{sat}) = 0.25\text{V}$

$$V_{SD11}(\text{sat}) \le \sqrt{\frac{2 \cdot 1.5I}{K_P \cdot S_{11}}} \rightarrow S_{11} = W_{11} \ge \frac{2 \cdot 30}{(0.25)^2 \cdot 8} = 120 \rightarrow \underline{\underline{W_{11} = W_{12} \ge 120\mu\text{m}}}$$

Problem 14 – (026412FE7) - Continued

6.) Choose $S_3(S_4)$ by satisfying $V_{ic}(max)$ specification then check mirror pole.

$$V_{ic}(max) \geq V_{GS3}(20\mu A) + V_{TN} \rightarrow V_{GS3}(20\mu A) = 1.25V \geq \sqrt{\frac{2\cdot I}{K_N\cdot S_3}} + 0.75V$$

$$S_3 = S_4 = \frac{2\cdot 20}{(0.5)^2\cdot 24} = 6.67 \Rightarrow \boxed{W_3 = W_4 = 7\mu m}$$

7.) Check mirror pole ($p_3 = g_{m3}/C_{Mirror}$).

$$p_3 = \frac{g_{m3}}{C_{Mirror}} = \frac{g_{m3}}{2\cdot 0.667\cdot W_3\cdot L_3\cdot C_{ox}} = \frac{\sqrt{2\cdot 24\cdot 6.67\cdot 20}\text{x}10^{-6}}{2\cdot 0.667\cdot 6.67\cdot 0.5\text{x}10^{-15}} = 17.98\text{x}10^9$$ which is much greater than 10GB ($0.0628\text{x}10^9$). Therefore, W_3 and W_4 are OK.

8.) $g_{m6} = 10g_{m1} = 1256.7\mu S$

a.) $g_{m6} = \sqrt{2K_NS_6 10I} \Rightarrow W_6 = 164.5\mu m$

b.) $V_{out}(min) = 0.5 \Rightarrow V_{DS6}(sat) = 0.5 = \sqrt{\frac{2\cdot 10I}{K_NS_6}} \Rightarrow W_6 = 66.67\mu m$

Therefore, use $\boxed{W_6 = 165\mu m}$

Note: For proper mirroring, $S_4 = \frac{I_4}{I_6} S_6 = 8.25\mu m$ which is close enough to $7\mu m$.

9.) Use the $V_{out}(max)$ specification to design W_7.

$$V_{out}(max) = 0.25V \geq V_{DS7}(sat) = \sqrt{\frac{2\cdot 200\mu A}{8\text{x}10^{-6}\cdot S_7}}$$

$$\therefore\ S_7 \geq \frac{400\mu A}{8\text{x}10^{-6}(0.25)^2} \Rightarrow \boxed{W_7 = 800\mu m}$$

10.) Now to achieve the proper currents from the current source I gives,

$$S_9 = S_{10} = \frac{S_7}{10} = 80 \rightarrow \boxed{W_9 = W_{10} = 80\mu m}$$

and

$$S_{11} = S_{12} = \frac{1.5\cdot S_7}{10} = 120 \rightarrow W_{11} = W_{12} = 120\mu m.$$ We saw in step 5 that W_{11} and W_{12} had to be greater than $120\mu m$ to satisfy $V_{ic}(max)$. $\therefore$ $\boxed{W_{11}=W_{12}=120\mu m}$

11.) $P_{diss} = 15I\cdot 1.5V = 300\mu A\cdot 1.5V = 450\mu W$

C_c	I	W_1=W_2	W_3=W_4	W_5=W_8	W_6	W_7	W_9=W_{10}	W_{11}=W_{12}	P_{diss}
2pF	20μA	33μm	7μm	202μm	165μm	800μm	80μm	120μm	450μW

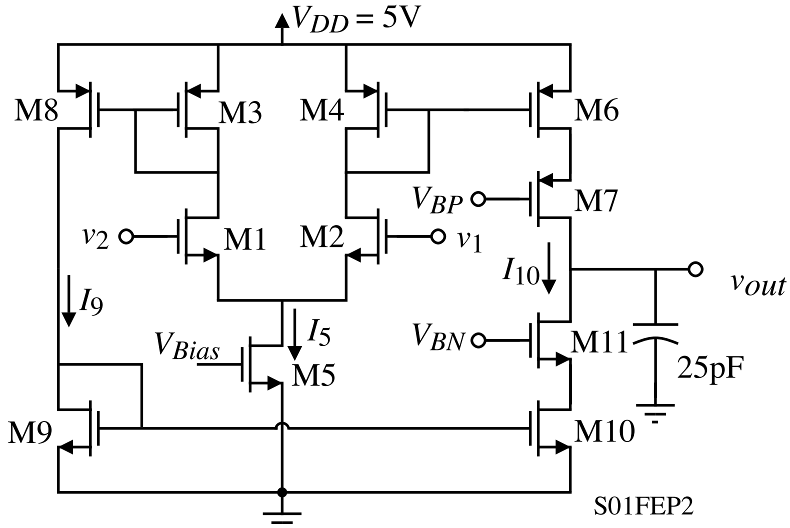
Problem 15 - (016412FE2)

A CMOS op amp that uses a 5V power supply is shown. All transistor lengths are 1μm and operate in the saturation region. Design all of the W values of every transistor of this op amp to meet the following specifications. Use the following model parameters: K_N'=110μA/V^2, K_P'=50μA/V^2, V_{TN}=0.7V, V_{TP}=-0.7V, λ_N=0.04V^{-1} and λ_P=0.05V^{-1}.

Slew rate = ±10V/μs	V_{out}(max) = 4V	V_{out}(min) = 1V
V_{ic}(min) = 1.5V	V_{ic}(max) = 4V	GB = 10MHz

Your design should meet or exceed these specifications. Ignore bulk effects and summarize your W values to the nearest micron, the bias current, I_5(μA), the power dissipation, the differential voltage gain, A_{vd}, and V_{BP} and V_{BN} in the following table. Assume that V_{bias} is whatever value necessary to give I_5.

W1=W2	W3=W4=W6 =W7=W8	W9=W10 =W11	W5	I_5(μA)	A_{vd}	V_{BP}	V_{BN}	P_{diss}
89.75	40	18.2	13.75	250μA	17,338V/V	3.3V	1.7V	2.5mW



Solution

Since $W3 = W4 = W6 = W7 = W8$ and $W9 = W10 = W11$, then I_5 is the current available to charge the 25pF load capacitor. Therefore,

$$I_5 = C\frac{dv_{OUT}}{dt} = 25\text{pF}(10\text{V}/\mu\text{s}) = \underline{\underline{250\mu\text{A}}}$$

Note that normally, $I_{10} = I_9$ = 125µA. However, for the following calculations we will use I_6 or I_{10} equal to 250µA for the following v_{OUT}(max/min) calculations.

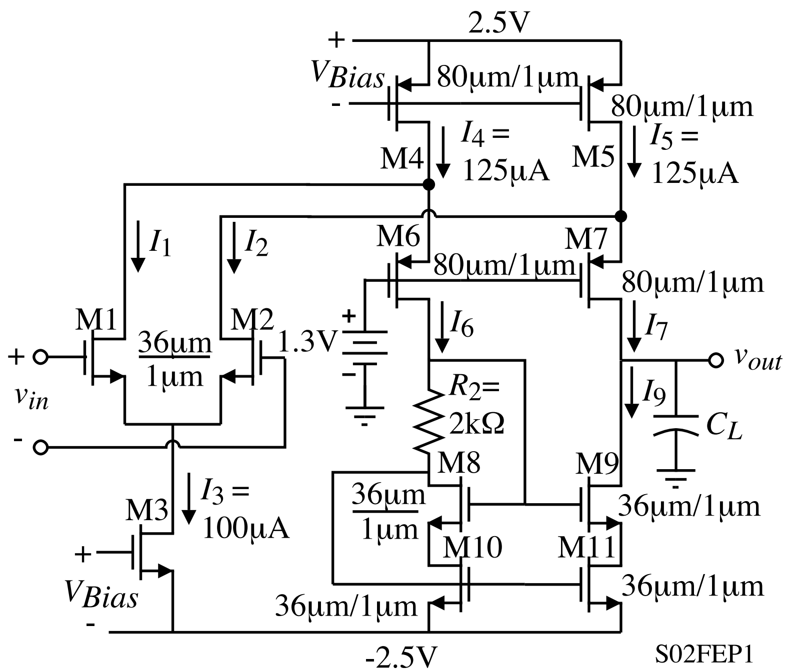
$$v_{OUT}(\text{max}) = 4\text{V} \quad \Rightarrow \quad 0.5 = \sqrt{\frac{2I_5}{K_P'(W6/L6)}} = \sqrt{\frac{2I_5}{K_P'(W6/L6)}}$$

$\therefore$ $\underline{W6 = W7 = 40 = W3 = W4 = W8}$

OPEN LOOP COMPARATORS

Problem 1 - (056412FE2)

If the folded-cascode op amp shown having a small-signal voltage gain of 7464V/V is used as a comparator, find the dominant pole if C_L = 5pF. If the input step is 10mV, determine whether the response is linear or slewing and find the propagation delay time. Assume the parameters of the NMOS transistors are K_N'=110V/μA^2, V_{TN} = 0.7V, λ_N=0.04V^{-1} and for the PMOS transistors are K_P'=50V/μA^2, V_{TP} = -0.7V, λ_P=0.05V^{-1}.



Solution

V_{OH} and V_{OL} can be found from many approaches. The easiest is simply to assume that V_{OH} and V_{OL} are 2.5V and –2.5V, respectively. However, no matter what the input, the values of V_{OH} and V_{OL} will be in the following range,

$$(V_{DD}\text{-}2V_{ON}) < V_{OH} < V_{DD} \quad \text{and} \quad V_{DD} < V_{OH} < (V_{SS}+2V_{ON})$$

The reasoning is as follows, suppose V_{in} >0. This gives I_1>I_2 which gives I_6<I_7 which gives I_9<I_7. V_{out} will increase until I_7 equals I_9. The only way this can happen is for M5 and M7 to leave saturation. The same reasoning holds for V_{in} <0.

Therefore assuming that V_{OH} and V_{OL} are 2.5V and –2.5V, respectively, we get

$$V_{in}(\text{min}) = \frac{5\text{V}}{7464} = 0.67\text{mV} \quad \rightarrow \quad k = \frac{10\text{mV}}{0.67\text{mV}} = 14.93$$

Problem 2 - (036412FE1)

An open-loop comparator has a gain of 10^4, a dominant pole of 10^5 radians/sec., a slew rate of 5V/μs and an output swing of 1V. (a.) If V_{in} = 1mV find the propagation delay time of this comparator (the time for the output to go halfway from one state to the other). (b.) Repeat part (a.) if V_{in} = 10mV. (c.) Repeat part (a.) if V_{in} = 100mV.

Solution

a.) We know that the linear output voltage of a single-pole comparator can be written as,

$$v_{out}(t) = A(1-e^{-tp_1})V_{in}$$

which can be solved for the propagation delay time as

$$t_p = \tau_1 ln\left(\frac{2k}{2k-1}\right) \quad \text{where } k = \frac{V_{in}}{V_{in}(\text{min})} \text{ and } V_{in}(\text{min}) = \frac{(V_{OH}-V_{OL})}{A} = \frac{1\text{V}}{10^4} = 0.1\text{mV}$$

We must first determine if the comparator is linear or slewing. The maximum slope occurs at t = 0 and is given as

$$\frac{dv_{out}(t)}{dt} = A\cdot p_1\cdot V_{in}\, e^{-tp_1} \rightarrow \frac{dv_{out}(0)}{dt} = A\cdot p_1\cdot V_{in} = 10^4\cdot 10^5\cdot 10^{-6} = 10^6 = 1\text{V}/\mu\text{s}$$

∴ The comparator is not slewing and t_p is given as

$$t_p = \tau_1 ln\left(\frac{2k}{2k-1}\right) = 10^{-5} ln\left(\frac{20}{20-1}\right) = \underline{\underline{0.513\mu\text{s}}}$$

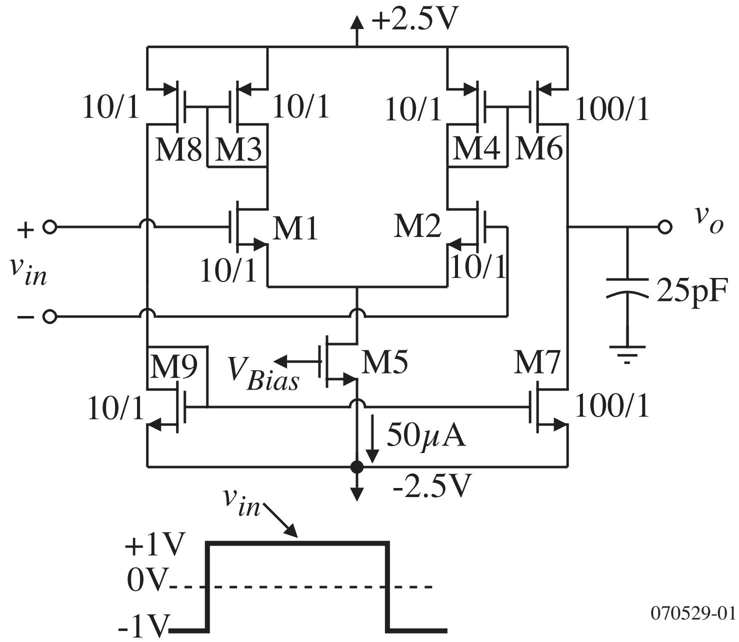
b.) We see the maximum slope for the linear response is 10V/μs which means that the comparator is slewing. Slewing at a rate of 5V/μs requires 0.1μs to go 0.5V. Therefore,

$$t_p = \underline{\underline{0.100\mu\text{s}}}$$

c.) The answer is the same as b.) namely $t_p = \underline{\underline{0.100\mu\text{s}}}$

Problem 3 - (016412FE3)

The comparator shown has an input applied as shown. Assuming the pulse width is wide enough, calculate the propagation delay time for this comparator. Assume that the trip point of the output is at 0V.



Solution

When v_{in} = -1V, $i_{D1} < i_{D2}$, which gives $i_{D6} > i_{D7}$. Therefore $v_o(0^-)$ = +2.5V. When v_{in} switches from –1V to +1V all of the 50μA flows through M1 and is mirrored via M3-M8 and M9-M7 and multiplied by 10 to give i_7 = 500μA. Thus, the falling propagation delay time is found as,

$$t_p^- = \frac{C \cdot \Delta V}{i_7} = \frac{25\text{pF}\cdot 2.5\text{V}}{500\mu\text{A}} = 125\text{ns}$$

Similarly, when v_{in} = +1V, v_o is at –2.5V. When v_{in} switches back to –1V, all of the 50μA of M5 flows through M2 giving i_6 = 500μA and i_7 =0. The rising propagation delay time is

$$t_p^+ = \frac{C \cdot \Delta V}{i_6} = \frac{25\text{pF}\cdot 2.5\text{V}}{500\mu\text{A}} = 125\text{ns}$$

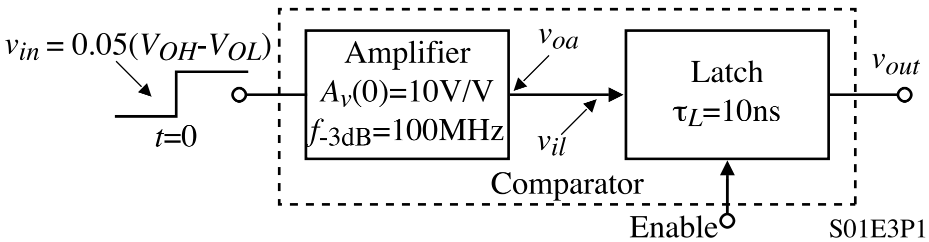
Consequently, the propagation delay time for this comparator is

$$\underline{\underline{t_p = 0.5(t_p^- + t_p^+) = 125\text{ns}}}$$

LATCHED COMPARATORS

Problem 1 - (056412FE1)

A comparator consists of an amplifier cascaded with a latch as shown below. The amplifier has a voltage gain of 10V/V and f_{-3dB} = 100MHz and the latch has a time constant of 10ns. The maximum and minimum voltage swings of the amplifier and latch are V_{OH} and V_{OL}. When should the latch be enabled after the application of a step input to the amplifier of $0.05(V_{OH}-V_{OL})$ to get minimum overall propagation time delay? What is the value of the minimum propagation time delay? It may useful to recall that the propagation time delay of the latch is given as $t_p = \tau_L \ln\left(\frac{V_{OH}-V_{OL}}{2v_{il}}\right)$ where v_{il} is the latch input (ΔV_i of the text).



Solution

The solution is based on the figure shown.

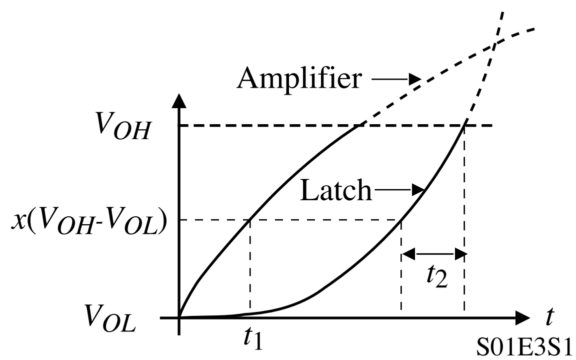
We note that,

$$v_{oa}(t) = 10[1-e^{-\omega_{-3dB}t}]0.05(V_{OH}-V_{OL}).$$

If we define the input voltage to the latch as,

$$v_{il} = x\cdot(V_{OH}-V_{OL})$$

then we can solve for t_1 and t_2 as follows:



$$x\cdot(V_{OH}-V_{OL}) = 10[1-e^{-\omega_{-3dB}t_1}]0.05(V_{OH}-V_{OL})$$

$\rightarrow$ $x = 0.5[1-e^{-\omega_{-3dB}t_1}]$

This gives,

$$t_1 = \frac{1}{\omega_{-3dB}} \ln\left(\frac{1}{1-2x}\right)$$

From the propagation time delay of the latch we get,

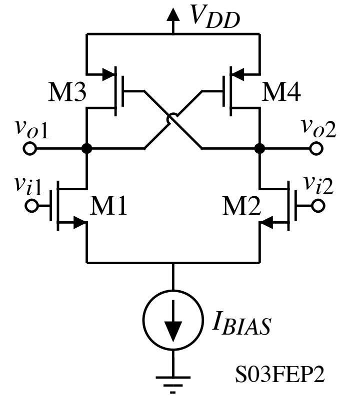
$$t_2 = \tau_L \ln\left(\frac{V_{OH}-V_{OL}}{2v_{il}}\right) = \tau_L \ln\left(\frac{1}{2x}\right)$$

$$\therefore \quad t_p = t_1 + t_2 = \frac{1}{\omega_{-3dB}} \ln\left(\frac{1}{1-2x}\right) + \tau_L \ln\left(\frac{1}{2x}\right) \quad \rightarrow \quad \frac{dt_p}{dx} = 0 \text{ gives } x = \frac{\pi}{1+2\pi} = 0.4313$$

$$t_1 = \frac{10\text{ns}}{2\pi} \ln(1+2\pi) = 1.592\text{ns}\cdot 1.9856 = \underline{\underline{3.16\text{ns}}} \quad \text{and} \quad t_2 = 10\text{ns} \ln\left(\frac{1+2\pi}{2\pi}\right) = 1.477\text{ns}$$

$$\therefore \quad t_p = t_1 + t_2 = 3.16\text{ns}+1.477\text{ns} = \underline{\underline{4.637\text{ns}}}$$

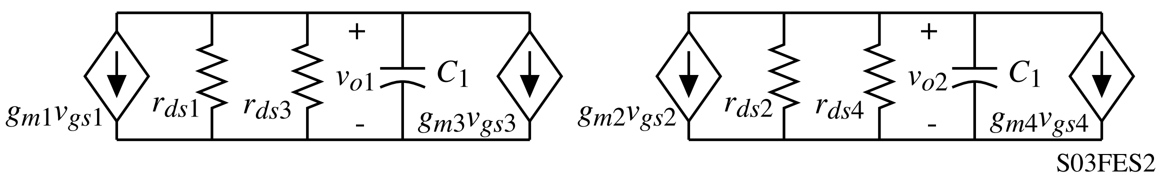
Problem 2 - (036412FE2)



Assume the capacitors connected to the drains of M1 and M2 (C_1 and C_2) are initially discharged. Express $\Delta V_{out} = v_{o2} - v_{o1}$ as a function of the applied input, $\Delta V_{in} = v_{i1}$-v_{i2}, in the time domain assuming ΔV_{in} is a step input. If $g_{m1} = g_{m2}$ = 1mS, $g_{m3} = g_{m4}$ = 100μS, and $C_1 = C_2$ = 1pF, what is the propagation delay time ($\Delta V_{out} = |0.5(V_{OH} - V_{OL})|$) for a step input of $\Delta V_{in} = 0.01(V_{OH} - V_{OL})$?

Solution

Small-signal model:



The nodal equations corresponding two these two circuits are:

$$g_{m1}v_{gs1} + g_{ds1}v_{o1} + g_{d3}v_{o1} + sC_1v_{o1} + g_{m3}v_{gs3} = 0$$

and

$$g_{m2}v_{gs2} + g_{ds2}v_{o2} + g_{d4}v_{o2} + sC_2v_{o2} + g_{m4}v_{gs4} = 0$$

We can write that,

$$(g_{ds1}+ g_{ds3}+ sC_1)\, v_{o1} = -\, g_{m1}v_{gs1} - g_{m3}v_{gs3}$$

and

$$(g_{ds2}+ g_{ds4}+ sC_2)\, v_{o2} = -\, g_{m1}v_{gs2} - g_{m4}v_{gs4}$$

Assuming matching, we get

$$(v_{o2} - v_{o1})(g_{ds1}+ g_{ds3}+ sC_1) = g_{m1}(v_{gs1}\text{-}\ v_{gs2}) + g_{m3}(v_{gs3}\text{-}\ v_{gs4})$$

or

$$(v_{o2} - v_{o1})(g_{ds1}+ g_{ds3}+ sC_1) = g_{m1}(v_{i1}\text{-}\ v_{i2}) + g_{m3}(v_{o2} - v_{o1})$$

$$(v_{o2} - v_{o1})(g_{ds1}+ g_{ds3}+ sC_1\text{-}\ g_{m3}) \approx (v_{o2} - v_{o1})(\ sC_1\text{-}\ g_{m3}) = g_{m1}(v_{i1}\text{-}\ v_{i2})$$

$$\therefore \quad (v_{o2} - v_{o1}) = \Delta V_{out}(s) = \frac{g_{m1}}{sC_1\text{-}\ g_{m3}}\,\Delta V_{in}(s) = \frac{g_{m1}}{g_{m3}}\left(\frac{g_{m3}/C_1}{s\text{ - }(g_{m3}/C_1)}\right)\frac{\Delta v_{in}}{s}$$

$$\Delta V_{out}(s) = \frac{g_{m1}}{C_1}\Delta v_{in}\left[\frac{k_1}{s} + \frac{k_2}{s\text{- }(g_{m3}/C_1)}\right] = \frac{g_{m1}}{g_{m3}}\left(\frac{g_{m3}/C_1}{s\text{ - }(g_{m3}/C_1)}\right)\frac{\Delta v_{in}}{s}$$

Solving for k_1 and k_2 gives $k_1 = -(C_1/g_{m3})$ and $k_2 = (C_1/g_{m3})$. Thus,

$$\Delta V_{out}(s) = \frac{g_{m1}}{g_{m3}}\left(\frac{1}{s\text{ - }(g_{m3}/C_1)} - \frac{1}{s}\right)\Delta_{in} \rightarrow \boxed{\Delta v_{out}(t) = \frac{g_{m1}}{g_{m3}}\Delta V_{in}[e^{(g_{m3}/C_1)t} - 1]}$$

If $\Delta V_{in} = 0.01(V_{OH} - V_{OL})$, then

$$0.5(V_{OH} - V_{OL}) = 0.1(V_{OH} - V_{OL})[e^{10^8 t_p}\text{-}1] \;\rightarrow\; 5 = e^{10^8 t_p}\text{-}1$$

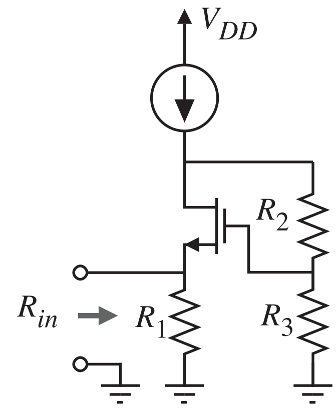
or

$$e^{10^8 t_p} = 6 \;\rightarrow\; t_p = \frac{1}{10^8}\,ln(6) = \frac{1.792}{10^8} = \underline{\underline{19.92\text{ ns}}}$$

FEEDBACK (THESE PROBLEMS DO NOT CORRESPOND WITH THE TEXT)

Problem 1 - (056412E3P3)

Use Blackmnn's formula to calculate the small-signal input resistance, R_{in}, of the circuit shown. Your answer should be in terms of the resistances R_1, R_2, R_3, g_m, and r_{ds}. Simplify your answer if $g_m r_{ds}$ >>1. Blackman's formula is,

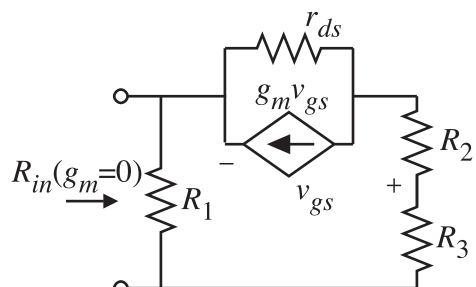


$$R_{in} = R_{in}(g_m{=}0)\left[\frac{1 + RR(\text{port shorted})}{1 + RR(\text{port opened})}\right]$$

Solution

$R_{in}(g_m{=}0)$:

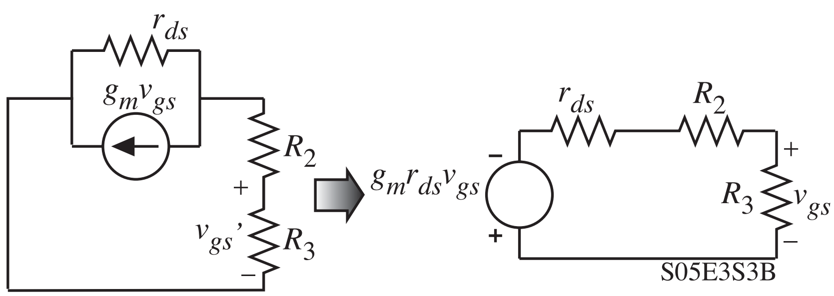
$$R_{in}(g_m{=}0) = R_1 || (r_{ds} + R_2 + R_3)$$



S05E3S3A

RR(port shorted):

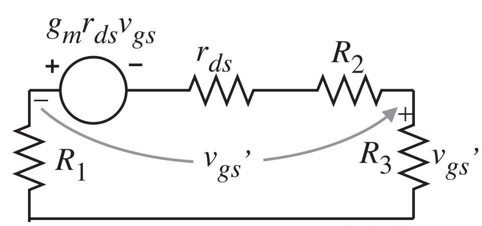
$$RR(0) = \frac{-g_m r_{ds} R_3}{r_{ds} + R_2 + R_3}$$



S05E3S3B

RR(port opened):

$$RR(\infty) = \frac{-g_m r_{ds}(R_1 + R_3)}{r_{ds} + R_1 + R_2 + R_3}$$



S05E3S3C

Therfore,

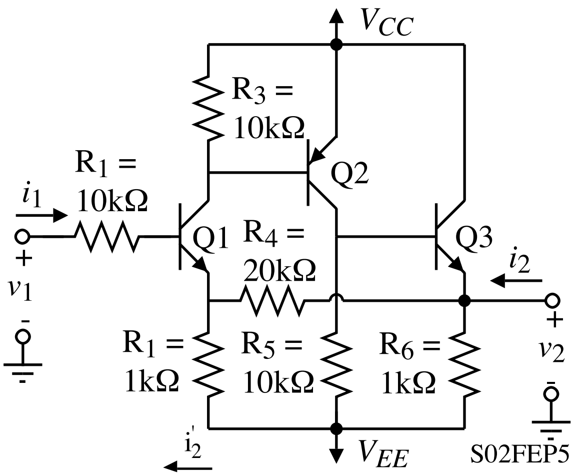
$$R_{in} = \frac{R_1(r_{ds} + R_1 + R_3)}{r_{ds} + R_1 + R_2 + R_3}\left[\frac{1 + \dfrac{g_m r_{ds} R_3}{r_{ds} + R_2 + R_3}}{1 + \dfrac{g_m r_{ds}(R_1 + R_3)}{r_{ds} + R_1 + R_2 + R_3}}\right]$$

$$= R_1\left[\frac{r_{ds} + R_2 + R_3 + g_m r_{ds} R_3}{r_{ds} + R_1 + R_2 + R_3 + g_m r_{ds}(R_1 + R_3)}\right] = R_1\left[\frac{r_{ds} + R_2 + R_3(1 + g_m r_{ds})}{r_{ds} + R_1 + (R_2 + R_3)(1 + g_m r_{ds})}\right]$$

$$R_{in} \approx \frac{R_1 R_3}{R_1 + R_3} \text{ if } g_m r_{ds} >> 1.$$

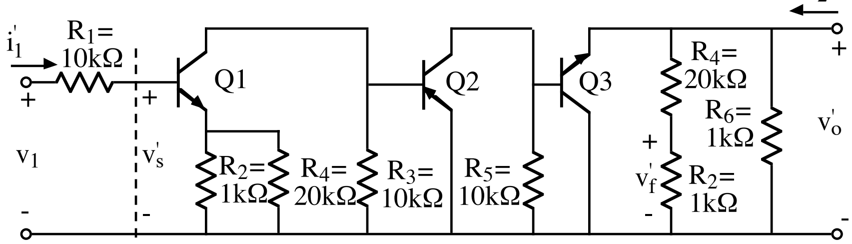
Problem 2 - (056412FE4)

The simplified schematic of a feedback amplifier is shown. Use the method of feedback analysis to find v_2/v_1, $R_{in} = v_1/i_1$, and $R_{out} = v_2/i_2$. Assume that all transistors are matched and that $\beta = 100$, $r_\pi = 5\text{k}\Omega$ and $r_o = \infty$.

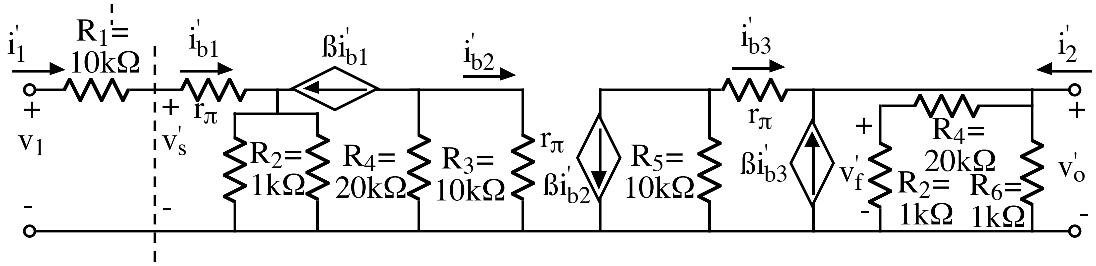


Solution

Open-loop, quasi-ac model:



Small-signal, open-loop model:



$$R_i = \frac{v_s'}{i_{b1}'} = r_\pi + (1+\beta)(R_2||R_4) = 5\text{k}\Omega + (101)(1\text{k}\Omega||20\text{k}\Omega) = 101.19\text{k}\Omega$$

$$a = \frac{v_o'}{v_s'} = \left(\frac{v_o'}{i_{b3}'}\right)\left(\frac{i_{b3}'}{i_{b2}'}\right)\left(\frac{i_{b2}'}{i_{b1}'}\right)\left(\frac{i_{b1}'}{v_s'}\right)$$

$$= (1+\beta)[R_6||(R_2+R_4)]\left(\frac{-\beta R_5}{R_5+r_\pi+(1+\beta)[R_6||(R_2+R_4)]}\right)\left(\frac{-\beta R_3}{R_3+r_\pi}\right)\left(\frac{1}{R_i}\right)$$

$$= [(101)(954.55)](-8.976)(-66.67)(1/101.19\text{k}\Omega) = 570.16 \text{ V/V}$$

$$f = \frac{R_2}{R_2+R_4} = \frac{1}{21} = 0.0476 \quad \text{and } R_o = \frac{v_o'}{i_2'} = R_6||(R_2+R_4)||\left(\frac{r_\pi+R_5}{1+\beta}\right) = 128.5\Omega$$

Closed-loop quantities are:

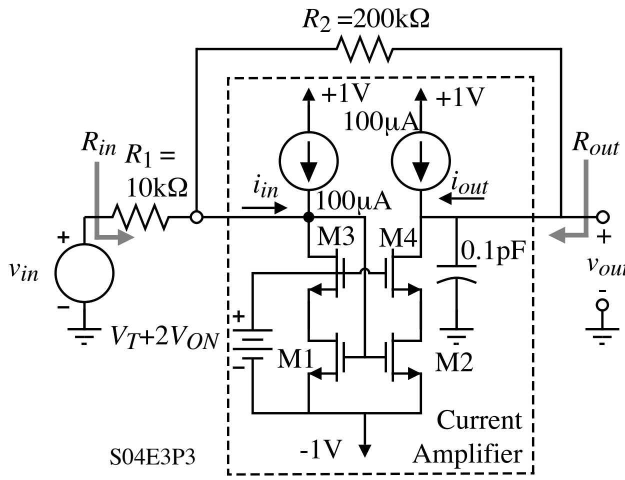
$$A_{vf} = \frac{v_o}{v_s} = \frac{a}{1+af} = \frac{570.16}{1+27.15} = 20.25,\ R_{if} = (1+af)R_i = 2.848\text{M}\Omega$$

$$\therefore \quad \boxed{R_{out} = R_{of} = \frac{R_o}{1+A_v\beta_f} = \frac{128.5\Omega}{28.15} = 4.565\Omega}$$

$$\boxed{R_{in} = R_1+R_{if} = 2.858\text{M}\Omega} \quad \text{and} \quad \boxed{\frac{v_2}{v_1} = A_{vf}\frac{R_{if}}{R_1+R_{if}} = 20.18 \text{ V/V}}$$

Problem 3 - (046412E3P3)

A voltage amplifier using feedback around a current amplifier is shown. In this problem assume all of the NMOS transistors are identical. Assume that R_1 is greater than the transistor transconductance and find the input resistance, R_{in}, the output resistance, R_{out}, the voltage gain, v_{out}/v_{in}, and the gainbandwidth (GB) in Hz. Assume that the output resistance connected to this voltage amplifier is large.



Solution

$R_{in} \approx R_1 = \underline{\underline{10k\Omega}}$

$$R_{out} = \frac{v_t}{i_t},\ i_t = 2\frac{v_{out}}{R_2} = 2\frac{v_t}{R_2} \rightarrow R_{out} = \frac{v_t}{i_t} = \frac{200k\Omega}{2} = \underline{\underline{100k\Omega}}$$

$$i_{in} \approx \frac{v_{in}}{R_1} + \frac{v_{out}}{R_2} \quad \text{and } i_{out} \approx -\frac{v_{out}}{R_2}$$

Since $i_{in} = i_{out}$, we get

$$\frac{v_{in}}{R_1} + \frac{v_{out}}{R_2} = -\frac{v_{out}}{R_2} \quad \rightarrow \quad \frac{v_{in}}{R_1} = -2\frac{v_{out}}{R_2} \quad \rightarrow \quad \frac{v_{out}}{v_{in}} = -\frac{R_2}{2R_1} = \underline{\underline{-10\text{V/V}}}$$

The dominant pole is found as,

$$p_{dominant} = \frac{1}{R_{out}C_{out}} = \frac{1}{100k\Omega\cdot 0.1pF} = 100\text{x}10^6 \text{ rads/sec.}$$

$\therefore \quad GB = 10\cdot 100\text{x}10^6$ rads/sec. $= 1000\text{x}10^6$ rads/sec. $\rightarrow \quad GB = \underline{\underline{159.15\text{MHz}}}$

Note: This problem can be worked as a feedback problem (which it is) so the results would be achieved from a shunt-shunt feedback network as follows.

The feedback factor would be $f = -1/R_2$ and the amplifier gain would be

$$a = \frac{v_{out}}{i_{in}} = -R_2 \quad \text{(loop gain is 1)}$$

Therefore the closed loop gain would be

$$\frac{v_{out}}{i_{in}} = \frac{a}{1+af} = \frac{-R_2}{2}$$

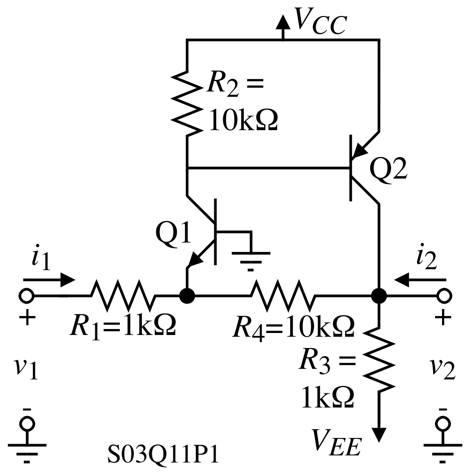
The desired voltage gain would be

$$\frac{v_{out}}{v_{in}} = \frac{v_{out}}{i_{in}}\frac{1}{R_{in}} = -\frac{R_2}{2R_1} = \underline{\underline{-10\text{V/V}}}$$

The input resistance of the current amplifier is approximately zero, so feedback would give the correct input and output resistances calculated above.

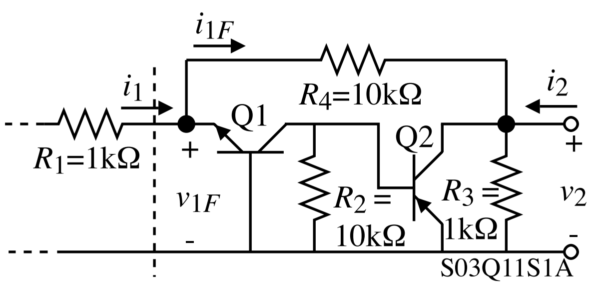
Problem 4 - (036412E3P2)

A shunt-shunt feedback amplifier is shown. Use the methods of feedback analysis to find the numerical values of v_2/v_1, v_1/i_1, and v_2/i_2. Assume that all transistors are matched and that V_t= 25mV, β (of the BJT) = 100, $I_{C1} = I_{C2}$ = 100µA, and $r_o = \infty$.



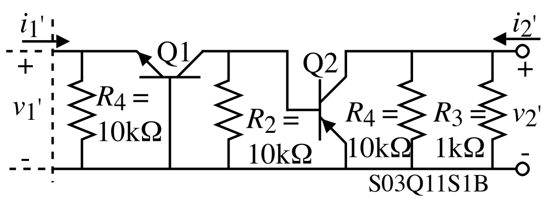
Solution

A simplified ac schematic for $\beta \neq 0$ is given as,

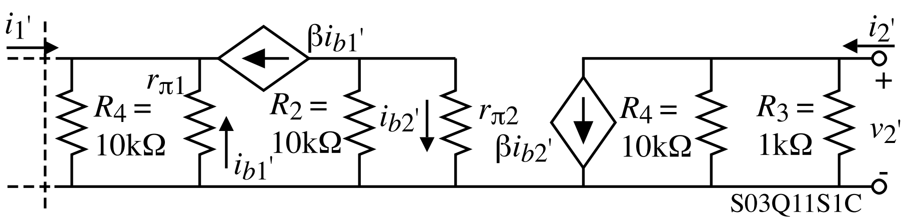


$$\beta = g_{12F} = \frac{i_{1F}}{v_2}\bigg|_{v_{1F}=0} = \frac{-1}{R_4} = \frac{-1}{10\text{k}\Omega}$$

The open-loop (β =0) simplified ac schematic is given as,



The small-signal model for (β = 0) is,



$$\frac{v_2'}{i_1'} = \left(\frac{v_2'}{i_{b2}'}\right)\left(\frac{i_{b2}'}{i_{b1}'}\right)\left(\frac{i_{b1}'}{i_1'}\right) = [-\beta(R_3||R_4)]\left(\frac{-\beta R_2}{r_{\pi 2}+R_2}\right)\left(\frac{-R_4}{R_4 + 1/g_{m1}}\frac{1}{1+\beta}\right)$$

$$= (-100\cdot 1\text{K}||10\text{K})\left(\frac{-100\cdot 10\text{K}}{35\text{K}}\right)\left(\frac{-10\text{K}}{10\text{K}+0.25\text{K}}\frac{1}{101}\right) = (-90.9)(-28.571)(-0.00966)$$

$$R_T = \frac{v_2'}{i_1'} = -25.087\text{k}\Omega \Rightarrow \qquad \frac{v_2}{i_1} = \frac{R_T}{1+\beta R_T} = \frac{-25.087\text{K}\Omega}{1+2.5087} = -7.15\text{k}\Omega$$

$$R_{in} = R_4||(1/g_{m1}) = 10000||250 = 244\Omega, \quad R_{inF} = \frac{R_{in}}{1+\beta R_T} = \frac{244\Omega}{3.509} = 69.5\Omega$$

$$\therefore \quad \frac{v_1}{i_1} = R_1 + R_{inF} = 1000 + 70 = \underline{\underline{1070\Omega}} \qquad \frac{v_2}{v_1} = \frac{v_2}{i_1}\frac{i_1}{v_1} = \frac{-7.51\text{K}}{1070} = \underline{\underline{-7.02\text{V/V}}}$$

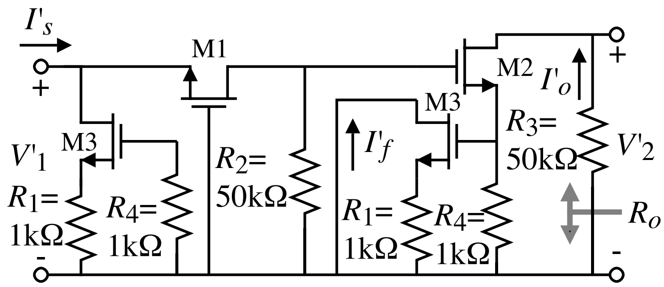
$$R_{out} = R_3||R_4 = 909\Omega \qquad \rightarrow \qquad \frac{v_2}{i_2} = \frac{R_{out}}{1+\beta R_T} = \frac{909\Omega}{3.509} = \underline{\underline{259\Omega}}$$

Problem 5 - (026412E3P1)

The simplified schematic of a feedback amplifier is shown. Use the method of feedback analysis to find V_2/V_1, $R_{in} = V_1/I_1$, and $R_{out} = V_2/I_2$. Assume that all transistors are matched and that g_m = 1mA/V and $r_{ds} = \infty$.

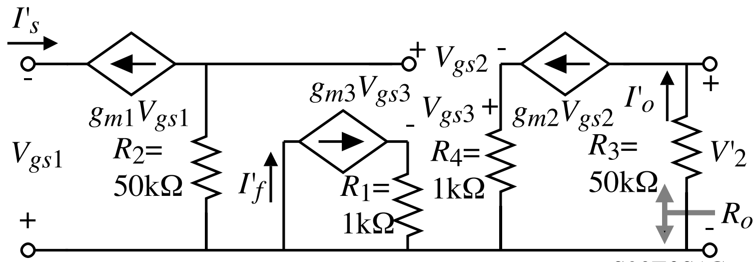
Solution

This feedback circuit is shunt-series. We begin with the open-loop, quasi-ac model shown to the right.



S02E3S1B

The small-signal, open-loop model is:



S02E3S1C

$$\frac{I'_o}{I'_s} = \left(\frac{I'_o}{V_{gs2}}\right)\left(\frac{V_{gs2}}{V_{gs1}}\right)\left(\frac{V_{gs1}}{I'_s}\right)$$

$$V_{gs2} = -g_{m1}V_{gs1}R_2 - g_{m2}V_{gs2}R_4$$

or

$$\frac{V_{gs2}}{V_{gs1}} = \frac{-g_{m1}R_2}{1 + g_{m2}R_4} = -\frac{50}{2} = -25 \qquad \therefore \quad a = \frac{I'_o}{I'_s} = (g_{m2})(-25)\left(\frac{-1}{g_{m1}}\right) = 25\text{A/A}$$

$$f = \frac{I'_f}{I'_o} = \left(\frac{I'_f}{V_{gs3}}\right)\left(\frac{V_{gs3}}{I'_o}\right) = (g_{m3})\left(\frac{R_4}{1 + g_{m3}R_1}\right) = (1\text{mA/V})(0.5\text{k}\Omega) = 0.5$$

$\therefore \; af = 25{\cdot}0.5 = 12.5$

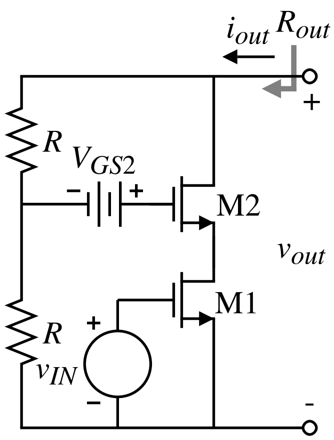
$$R_i = \frac{v'_1}{I'_s} = \frac{1}{g_{m1}} = 1\text{k}\Omega \;\rightarrow\; \boxed{R_{in} = R_{if} = \frac{R_i}{1 + af} = \frac{1000}{13.5} = 74.07\Omega}$$

$$\boxed{R_{out} = 50\text{k}\Omega \;\; (R_3 \text{ is outside the feedback loop})}$$

$$\frac{I_o}{I_s} = \frac{a}{1+af} = \frac{25}{1+12.5} = 1.852 \text{ A/A} \;\rightarrow\; \boxed{\frac{v_2}{v_1} = \frac{I_o(-50\text{k}\Omega)}{I_s(74.07\Omega)} = -1240.1 \text{ V/V}}$$

Problem 6 - (026412E2P2)

Use the Blackman's formula (see below) to calculate the small-signal output resistance of the stacked MOSFET configuration having identical drain-source drops for both transistors. Express your answer in terms of all the pertinent small-signal parameters and then simplify your answer if $g_m > g_{ds} > (1/R)$. Assume the MOSFETs are identical.



S02E3P2

$$R_{out} = R_{out}\,(g_m{=}0)\left[\frac{1 + RR(\text{output port shorted})}{1 + RR(\text{output port open})}\right]$$

(You may use small-signal analysis if you wish but this circuit seems to be one of the rare cases where feedback analysis is more efficient.)

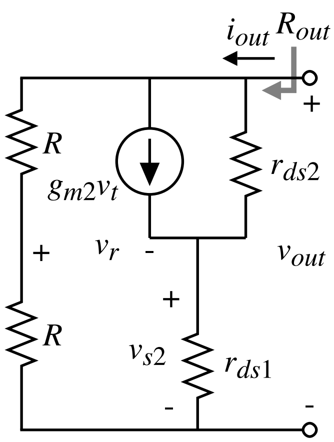
Solution

$$R_{out}\,(g_{m2}{=}0) = 2R\|(r_{ds1} + r_{ds2}) = \frac{2R(r_{ds1}+r_{ds2})}{2R+r_{ds1}+r_{ds2}}$$

RR(port shorted) = ?

$$v_r = 0 - v_{s2} = -\,g_{m2}v_t\left(\frac{r_{ds1}r_{ds2}}{r_{ds1}+r_{ds2}}\right)$$

$$\Rightarrow \quad RR(\text{port shorted}) = \frac{g_{m2}r_{ds1}r_{ds2}}{r_{ds1}+r_{ds2}}$$



S02E3S2

RR(port open) = ?

$$v_r = -\,g_{m2}v_t\left(\frac{r_{ds2}(r_{ds1}+R)}{r_{ds1}+r_{ds2}+2R}\right)$$

$$\Rightarrow \quad RR(\text{port open}) = \frac{g_{m2}r_{ds2}(r_{ds1}+R)}{r_{ds1}+r_{ds2}+2R}$$

$$\therefore \quad R_{out} = \frac{2R(r_{ds1}+r_{ds2})}{2R+r_{ds1}+r_{ds2}}\left[\frac{1+\dfrac{g_{m2}r_{ds1}r_{ds2}}{r_{ds1}+r_{ds2}}}{1+\dfrac{g_{m2}r_{ds2}(r_{ds1}+R)}{r_{ds1}+r_{ds2}+2R}}\right] = 2R\left(\frac{r_{ds1}+r_{ds2}+g_{m2}r_{ds1}r_{ds2}}{r_{ds1}+r_{ds2}+2R+g_{m2}r_{ds2}(r_{ds1}+R)}\right)$$

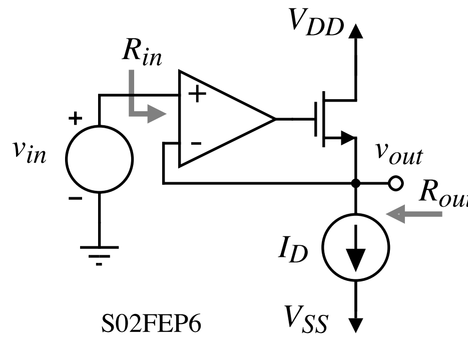
Using the assumptions of $g_m > g_{ds} > (1/R)$ we can simplify R_{out} as

$$R_{out} \approx 2R\left(\frac{g_{m2}r_{ds1}r_{ds2}}{g_{m2}r_{ds2}R}\right) = \underline{\underline{2r_{ds1}}}$$

What is the insight? Well there are two feedback loops, one a series (the normal cascode) and one a shunt. Apparently they are working against each other and the effective output resistance is pretty much what it would be if there were two transistors in series without any feedback.

Problem 7 - (026412FE6)

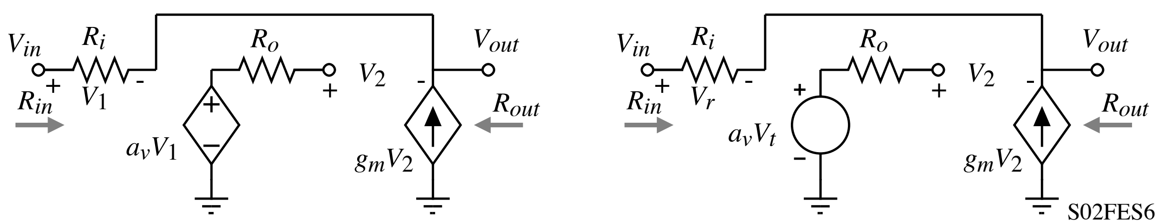
A voltage follower feedback circuit is shown. For the MOS transistor, I_D = 0.5mA, K' = 180μA/V^2, r_{ds} = ∞, and W/L = 100. Although, the bulk effect, g_{mbs}, should be considered, for simplicity ignore the bulk effects in this problem. For the op amp, assume that R_i = 1MΩ, R_o = 10kΩ, and a_v = 1000. Calculate the input resistance and output resistance using Blackman's formula given below.



$$R_{out} = R_{out}\text{ (Controlled Source Gain=0)}\left[\frac{1 + RR\text{(output port shorted)}}{1 + RR\text{(output port open)}}\right]$$

Solution

Circuit for calculating the return ratios.



Input Port:

$R_{in}(a_v\text{=}0) = R_i + (1/g_m)$, $\quad g_m = \sqrt{2\cdot 500\cdot 100\cdot 180} = 4.243\text{mS}$

$R_{in}(a_v\text{=}0) = 1\text{M}\Omega + 236\Omega \approx 1\text{M}\Omega$

RR(input port shorted):

$$V_r = -g_mR_i\,V_2 \text{ and } V_2 = a_vV_t - g_mR_i\,V_2 \quad\to V_r = \frac{-a_v\,g_mR_i}{1+g_mR_i}V_t$$

$$RR\text{(input port shorted)} = -\frac{V_r}{V_t} = \frac{-a_v\,g_mR_i}{1+g_mR_i} = -\frac{1000\cdot 4.243\text{mS}\cdot 1\text{M}\Omega}{1+4.243\text{mS}\cdot 1\text{M}\Omega} = -999.8$$

RR(input port open):

RR(input port open) = 0 because $V_r = 0$

$$\therefore \quad R_{in} = R_{in}\,(a_v\text{=}0)\left[\frac{1 + RR\text{(output port shorted)}}{1 + RR\text{(output port open)}}\right] = 1\text{M}\Omega(1+999.8) = \underline{\underline{1000.8\text{M}\Omega}}$$

Output Port:

$R_{out}(a_v\text{=}0) = R_i\,||(1/g_m) \approx 236\Omega$

RR(output port shorted):

RR(output port shorted) = 0 because $V_r = 0$

RR(output port open):

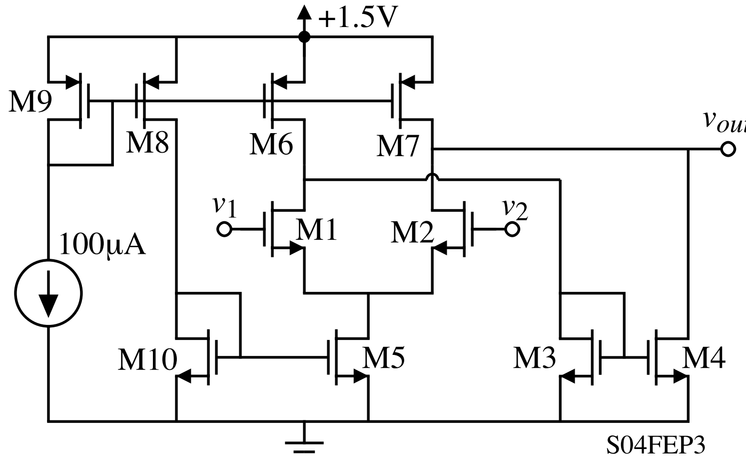
Same as the RR for the input port shorted.

$$\therefore \quad R_{out} = R_{out}\,(a_v\text{=}0)\left[\frac{1 + RR\text{(output port shorted)}}{1 + RR\text{(output port open)}}\right] = 236\Omega\left(\frac{1+0}{1+999.8}\right) = \underline{\underline{0.236\Omega}}$$

NOISE ANALYSIS

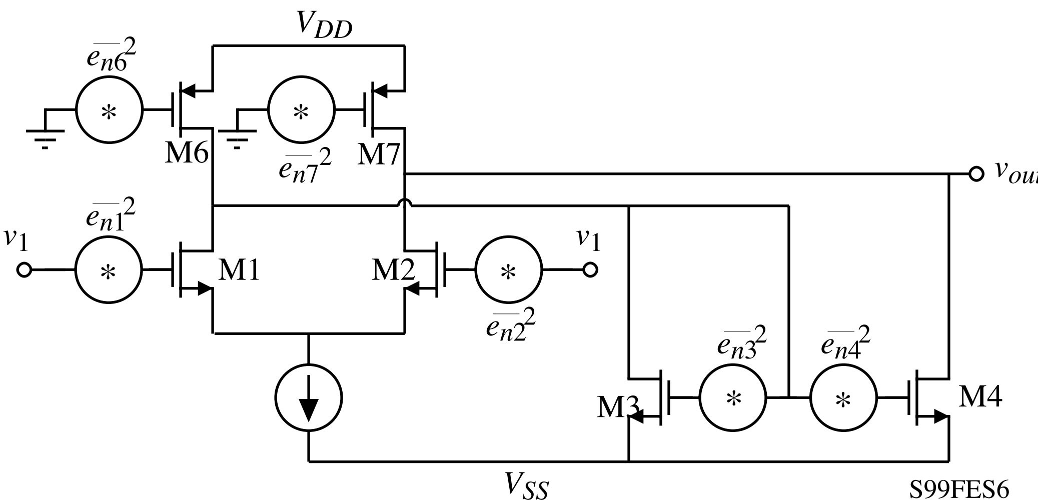
Problem 1 – (056412FE7)

Find an expression for the equivalent input noise voltage of the circuit in the previous problem, $\overline{e_{eq}^2}$, in terms of the small signal model parameters and the individual equivalent input noise voltages, $\overline{e_{ni}^2}$, of each of the transistors (i = 1 through 7). Assume M1 and M2, M3 and M4, and M6 and M7 are matched.



Solution

Equivalent noise circuit:



$$\overline{e_{out}^2} = (g_{m1}{}^2\overline{e_{n1}^2} + g_{m2}{}^2\overline{e_{n2}^2} + g_{m3}{}^2\overline{e_{n3}^2} + g_{m4}{}^2\overline{e_{n4}^2} + g_{m6}{}^2\overline{e_{n6}^2} + g_{m7}{}^2\overline{e_{n7}^2})R_{out}{}^2$$

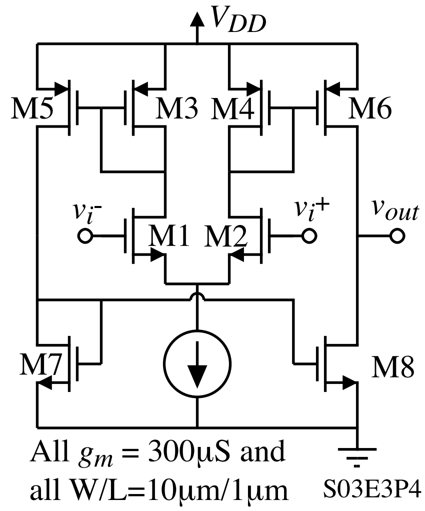
$$\overline{e_{eq}^2} = \frac{\overline{e_{out}^2}}{(g_{m1}R_{out})^2} = \overline{e_{n1}^2} + \overline{e_{n2}^2} + \left(\frac{g_{m3}}{g_{m1}}\right)^2(\overline{e_{n3}^2} + \overline{e_{n4}^2}) + \left(\frac{g_{m6}}{g_{m1}}\right)^2(\overline{e_{n6}^2} + \overline{e_{n7}^2})$$

If M1 through M2 are matched then $g_{m1} = g_{m2}$ and we get

$$\overline{e_{eq}^2} = 2\overline{e_{n1}^2} + 2\left(\frac{g_{m3}}{g_{m3}}\right)^2\overline{e_{n3}^2} + 2\left(\frac{g_{m6}}{g_{m1}}\right)^2\overline{e_{n6}^2}$$

Problem 2 - (036412E3P4)

For the amplifier shown assume that all transconductances are equal. Find (a.) the equivalent input noise voltage in units of V^2/Hz for thermal noise (k = 1.38x10^{-23} J/K), (b.) the equivalent input noise voltage in units of V^2/Hz for 1/f noise (B_N = 8x10^{-22} (V-m)^2 and B_P = 2x10^{-22} (V-m)^2), and (c.) the noise corner frequency in Hz. Using $\int_a^b \frac{1}{f}df$ = ln(b) – ln(a), find the rms noise voltage in a bandwidth of 1Hz to 100kHz in V(rms).



Solution

The short-circuit noise current as a function of all 8 of the noise sources in series with the gates can be written as,

$$i_{to}^2 = g_{m1}^2e_{n1}^2 + g_{m2}^2e_{n2}^2 + g_{m5}^2(e_{n3}^2 + e_{n5}^2) + g_{m6}^2(e_{n4}^2 + e_{n6}^2) + g_{m8}^2(e_{n7}^2 + e_{n8}^2)$$

The above can be written as,

$$i_{to}^2 = g_m^2[4\,e_{nN}^2 + 4\,e_{nP}^2]$$

Dividing by g_m^2 gives the equivalent input noise voltage as,

$$e_{eq}^2 = 4\,e_{nN}^2 + 4\,e_{nP}^2 = 4\,e_{nN}^2\left(1+\frac{e_{nP}^2}{e_{nN}^2}\right)$$

(a.) For thermal noise, $e_{nN}^2 = e_{nP}^2$ so that

$$e_{eq}^2 = 8\,e_{nN}^2 = 8\frac{8kT}{3g_{mN}} = 64\,\frac{1.38\text{x}10^{-23}\cdot 300}{3\cdot 300\text{x}10^{-6}} = \underline{\underline{2.944\text{x}10^{-16}\ \text{V}^2/\text{Hz}}}$$

(b.) For 1/f noise,

$$e_{nN}^2 = \frac{B_N}{fWL} = \frac{8\text{x}10^{-22}}{f10\text{x}10^{-12}} = \frac{8\text{x}10^{-11}}{f} \qquad \text{and} \qquad e_{nP}^2 = \frac{B_P}{fWL} = \frac{2\text{x}10^{-22}}{f10\text{x}10^{-12}} = \frac{2\text{x}10^{-11}}{f}$$

$$\therefore \quad e_{eq}^2 = 4\,e_{nN}^2\left(1+\frac{e_{nP}^2}{e_{nN}^2}\right) = \frac{32\text{x}10^{-11}}{f}\left(1+\frac{2}{8}\right) = \frac{40\text{x}10^{-11}}{f} \qquad \boxed{e_{eq}^2 = \frac{40\text{x}10^{-11}}{f}\ \text{V}^2/\text{Hz}}$$

(c.) Equating the above results gives,

$$\frac{40\text{x}10^{-11}}{f} = 2.944\text{x}10^{-16} \;\rightarrow\; f_c = \frac{40\text{x}10^{-11}}{2.944\text{x}10^{-16}} = \underline{\underline{1.359\text{MHz}}}$$

Finally, we can find the rms noise by integrating just the 1/f noise from 1Hz to 100kHz.

$$V_{eq}^2(\text{rms}) = \int_1^{10^5}\frac{40\text{x}10^{-11}}{f}\,\text{df} = 40\text{x}10^{-11}[\ln(10^5)-\ln(1)]$$

$$= 40\text{x}10^{-11}(11.513) = 4.605\text{x}10^{9}\ \text{V}^2(\text{rms}) \rightarrow \quad V_{eq}(\text{rms}) = \underline{\underline{68\mu\text{V (rms)}}}$$