Mismatch effects in Analog CMOS IC design

Matching is a key idea in analog IC design

- Absolute tolerances in device parameters are relatively large
- Identically sized devices on the same Silicon die:
  - Have (nearly) the same parameters
  - Operate at (nearly) the same temperature

Application examples studied so far:

- Distribution of bias currents using current mirrors
- Differential amplifiers
- Cancellation of temperature dependences

Next topic: effects of (small, random) mismatches in device parameters

- Input offset voltage in a differential amplifier with active load
- Current mirror mismatches

Random mismatches

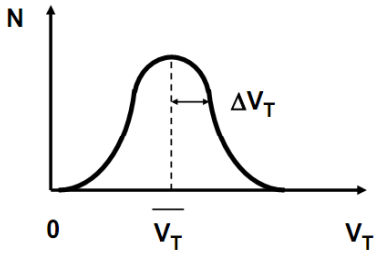
Sources of random mismatch include:

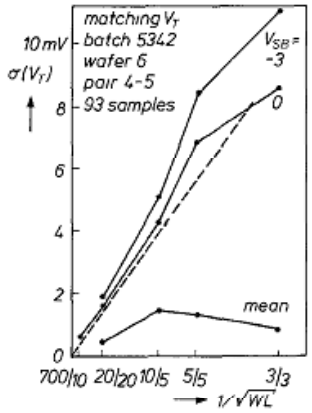
- Edge effects (rough edges)
- Material imperfections
- Variations in mobility

Device mismatch parameters:

- MOSFET
  Threshold voltage V_t,
  Conductance parameter $K = (\mu C_{ox}/2)(W/L) = \beta/2$
  Body effect parameter γ
- Resistors
  ρ (resistivity)
- Capacitors
  Oxide thickness variation

Threshold Voltage Mismatch



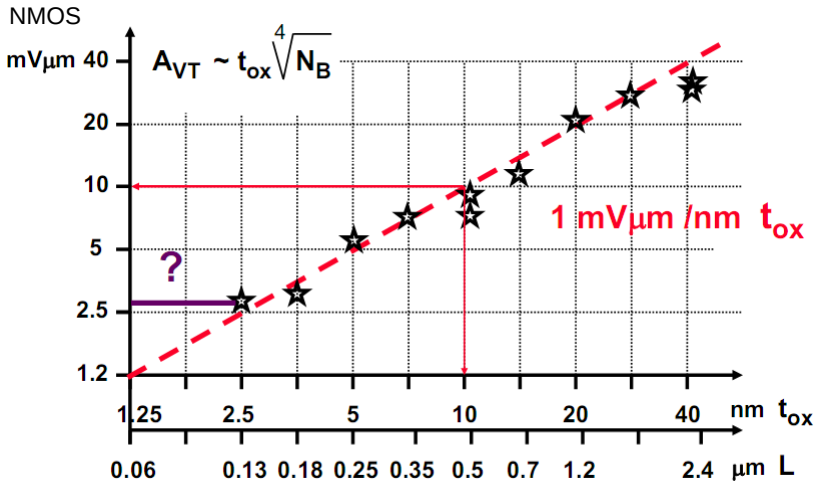


The threshold voltages among a group of transistors has a Gaussian profile about a mean. Experimentally, it has been shown that the difference in threshold voltages between 2 identically sized transistors behaves as:

$$\sigma_{\Delta V_t} = \frac{A_{V_t}}{\sqrt{WL}}$$ Note that to reduce the mismatch by ½ takes 4 times the area…

A fab will create test structures and measure ΔV_t multiple times per wafer for various sizes of transistors and collect ongoing statistics to monitor the process over time

Threshold Voltage Mismatch



The mismatch constant, A_{VT}, varies roughly linearly with process size. For p substrates, the PMOS has A_{VT} ~ 1.5*A_{VT} NMOS.

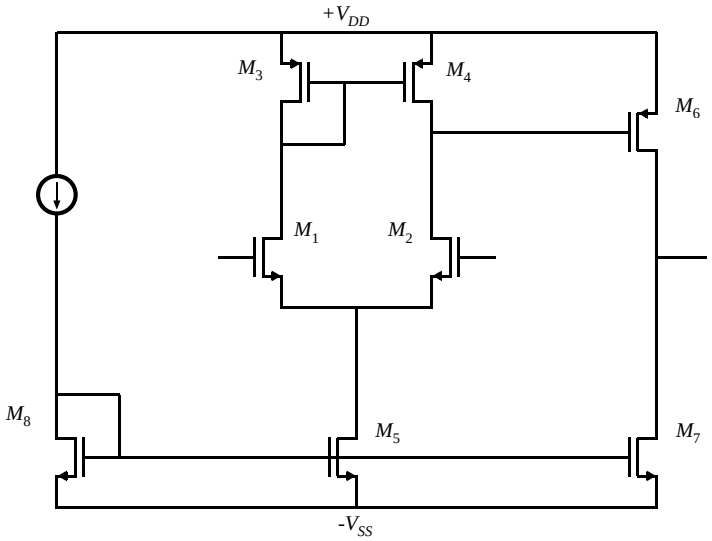
Conductance Parameter Mismatch

$$\frac{\sigma(\Delta\beta)}{\beta} = \frac{A_\beta}{\sqrt{WL}}$$

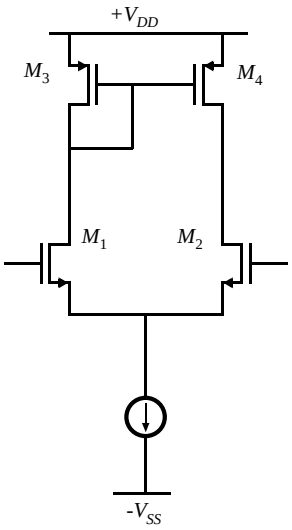
Typical A_β = 2%μm

Reference: Marcel J. M. Pelgrom, Matching properties of MOS transistors, IEEE JSSC, Oct. 1989

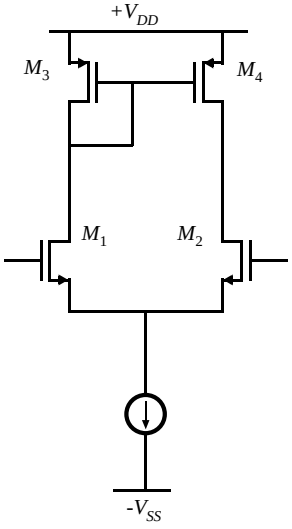
Application Example: Input Offset Voltage in a 2-stage CMOS op-amp



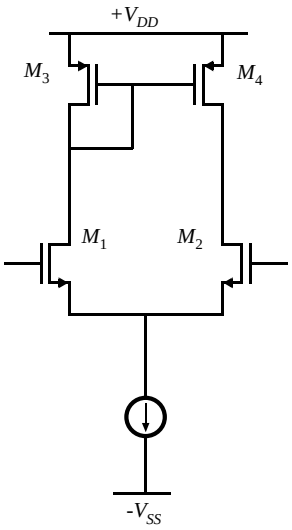
Input Offset Voltage in Differential Amplifier with Active (Current-Mirror) Load



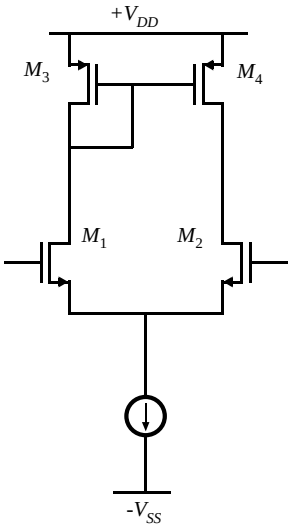
Input Offset Voltage in Differential Amplifier with Active (Current-Mirror) Load



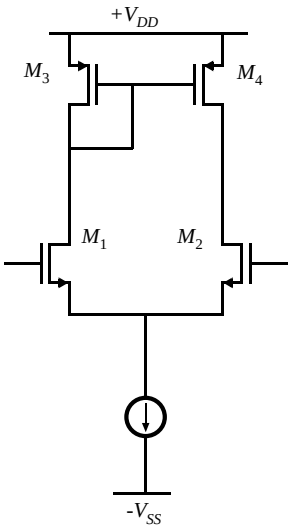
Current-Mirror Mismatch



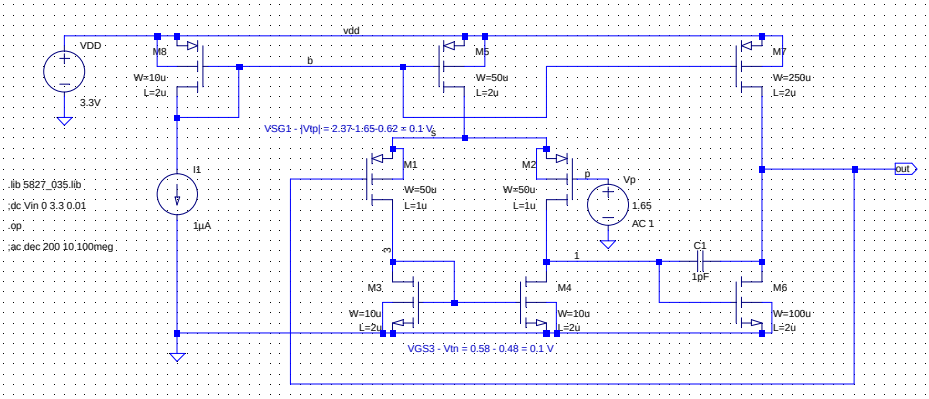
Current-Mirror Mismatch



Input Offset Voltage in Differential Amplifier with Active (Current-Mirror) Load



V_{OS} calculation example

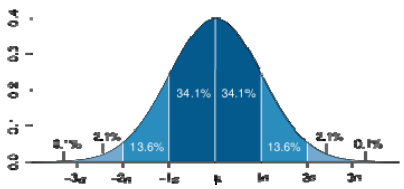


Process parameters: A_{Vtn} = 8 mVµm, A_{Vtp} = 12 mVµm, $A_\beta = A_K$ = 2%µm

$$\sigma_{\Delta V_t} = \frac{A_{V_t}}{\sqrt{WL}} \qquad \frac{\sigma(\Delta K)}{K} = \frac{\sigma(\Delta\beta)}{\beta} = \frac{A_\beta}{\sqrt{WL}}$$

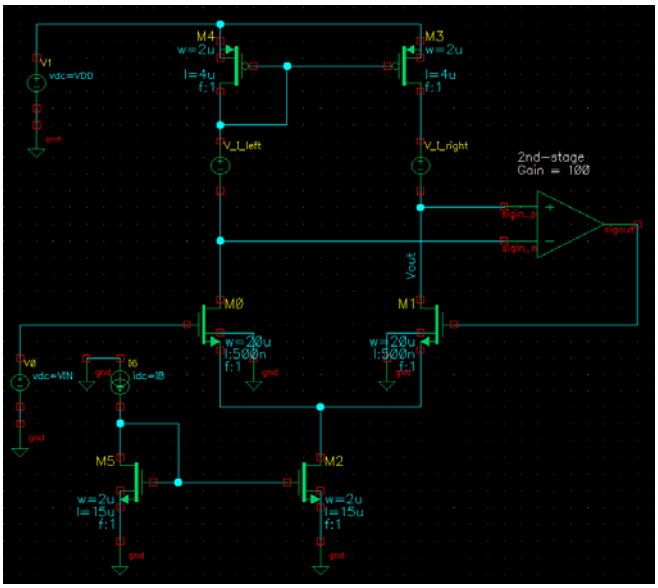
V_{OS} calculation example

pdf



Normal distribution

Input offset voltage analysis, example 2*



Analysis

1. Calculate ΔV_{gs} of input pair

2. Calculate $\Delta I_d/I_d$ of current mirror and reflect to input using g_m of input pair

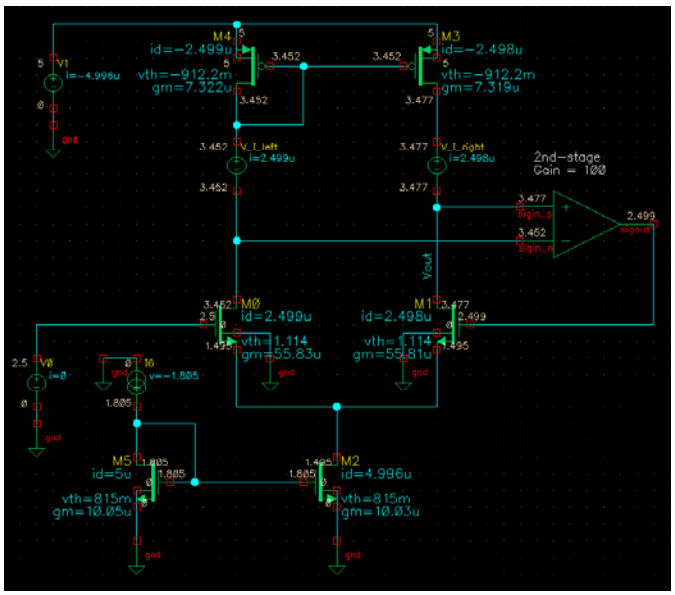
3. Combine to find standard deviation of V_{OS}

Check using Spice Monte Carlo analysis

CAD tools: Cadence

*This example in 0.5μ CMOS process was prepared by Art Zirger, National Semiconductor

DC operating point



Offset analysis: ΔV_{GS} of the NMOS diff pair

W/L = 20u/.5u, A_{Vt} = 16mVμm

$g_{m\_M0/M1}$ = 55.8μA/V, I_d = 2.5μA, A_β ~ 2%μm

$$\sigma(\Delta V_{gs}) = \sqrt{\left(\frac{\sigma(\Delta\beta)}{\beta}\frac{I_D}{g_m}\right)^2 + (\sigma(\Delta V_T))^2}$$

$$\sigma_{\Delta V_t} = \frac{A_{V_t}}{\sqrt{WL}} = \frac{16mV\mu m}{\sqrt{20\mu m * 0.5\mu m}} = 5.06mV$$

$$\frac{\sigma(\Delta\beta)}{\beta}\frac{I_D}{g_m} = \frac{.02\mu m}{\sqrt{20\mu m * 0.5\mu m}} * \frac{2.5\mu A}{55.8\,\mu A/V} = .28mV$$

$$\sigma(\Delta V_{gs}) = \sqrt{(.28mV)^2 + (5.06mV)^2} = 5.07mV$$

Offset analysis: ΔI_D of the PMOS mirror

$$\frac{\sigma(\Delta I_D)}{I_D} = \sqrt{\left(\frac{\sigma(\Delta\beta)}{\beta}\right)^2 + \left(\frac{g_m}{I_D}\sigma(\Delta V_T)\right)^2} = \sqrt{\left(\frac{.02\mu m}{\sqrt{2\mu m * 4\mu m}}\right)^2 + \left(\frac{7.32\,\mu A/V}{2.5\mu A}\frac{23mV\mu m}{\sqrt{2\mu m * 4\mu m}}\right)^2} = .025$$

Effects on the input offset voltage:

$$\sigma_{\Delta Vgs} = \left(\frac{\sigma(\Delta I_D)}{I_D}\right) * I_D / g_{mN} = .025 * 2.5\mu A / 55.8\,\mu A/V = 1.12mV$$

Input offset voltage

$$\sigma_{\Delta Vgs\_total} = \sqrt{\underbrace{(5.07mV)^2}_{\text{input pair}} + \underbrace{(1.12mV)^2}_{\text{current mirror}}} = 5.19mV$$

Given a choice to add area to current mirrors or input pair, in this example, more to be gained by using the area for the input pair.

CAD Tools for Checking Effects of Tolerances or Mismatches

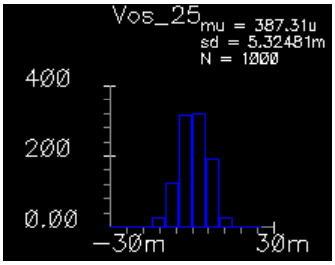
Spice "Monte Carlo" (.mc) analysis*

- Device models must include statistical parameters (distribution, mean, standard deviation)
- In Monte Carlo simulation, parameters of individual elements are selected randomly based on the statistical distribution specified in the device model
- It is necessary to perform a large number of simulations (100's) to develop good statistics

in LTSpice, Monte Carlo simulations can be done using mc(x,y) function, which generates a random number between x(1+y) and x*(1-y) with uniform distribution

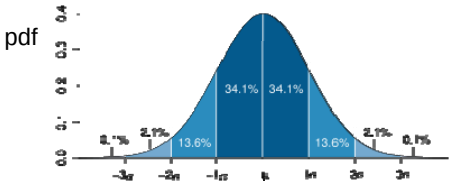
Models available for the 0.35u process do not include statistical parameters

Example: Monte Carlo analysis of the input offset voltage



1000 simulation runs

Result is a histogram of V_{OS} values, together with mean and standard deviation



Normal distribution