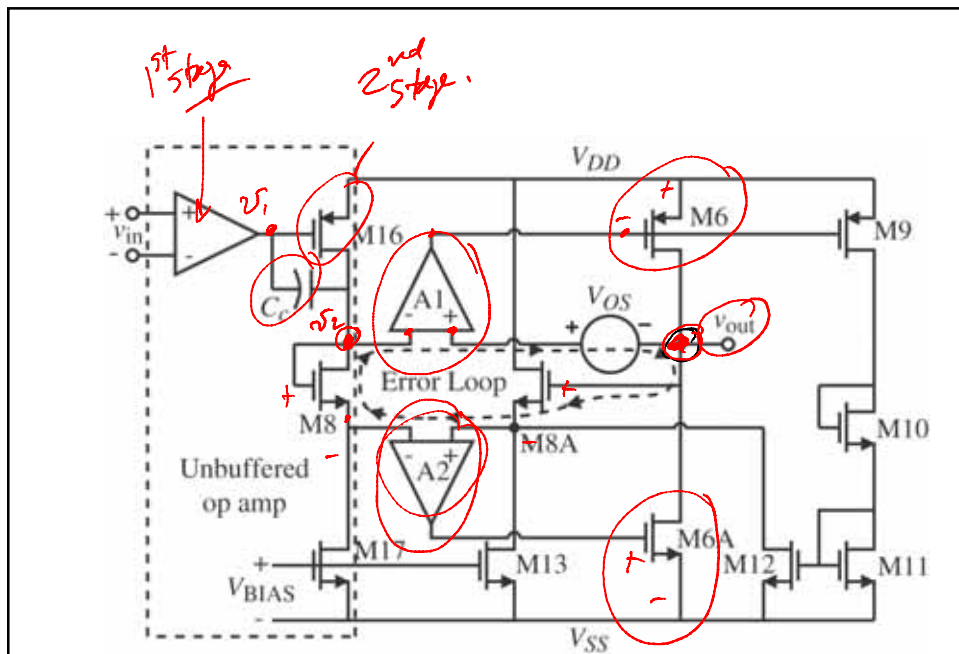


Lecture #17

- HW #5 Due Today
- HW #6 Due Next Friday
- Today
 - CG Cascode amplifiers
 - 0.35u CMOS process, LTSpice simulation models



Allen/Holberg Text Figure 7.1-6

Allen/Holberg Text figure 7.1-8

ECEN4827/5827 Analog IC Design 3

Review CS, CD, CG amplifiers

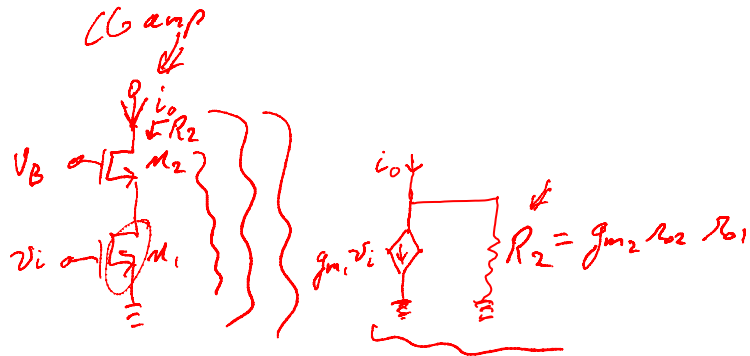
	D	S
Inputs	<ul style="list-style-type: none"> CS amp volt amp high gain inverting 	<ul style="list-style-type: none"> CD amp volt. buffer (unity gain) source follower (non-inverting) high gain, low Rout
	<ul style="list-style-type: none"> CG amp unity gain current buffer Cascode stage 	

non-inverting

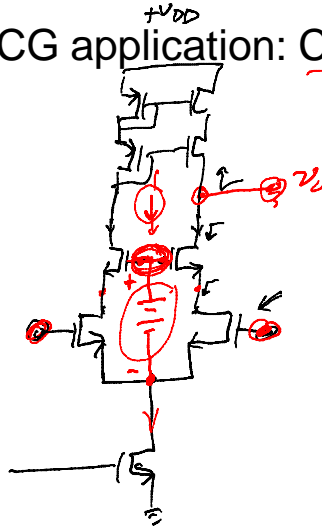
one inv.

ECEN4827/5827 Analog IC Design 4

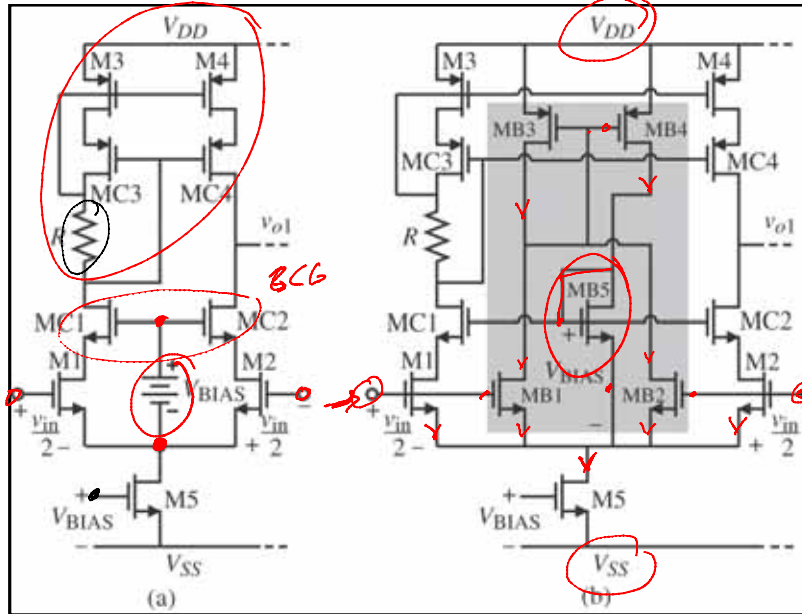
Review CS, CD, CG amplifiers



CG application: Cascode input stage

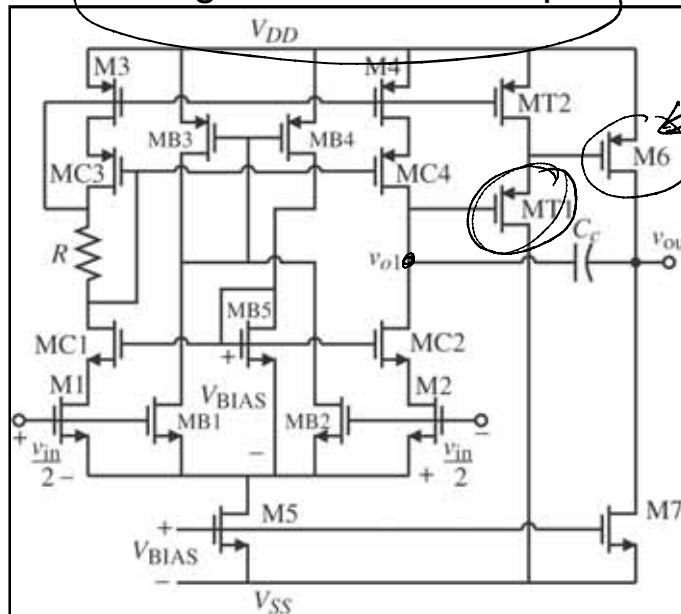


Cascode input: Example



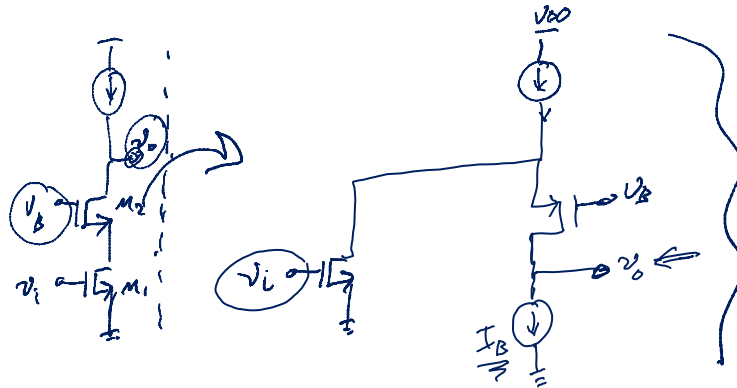
Allen/Holberg text Figure 6.5-1

2-Stage with cascode input

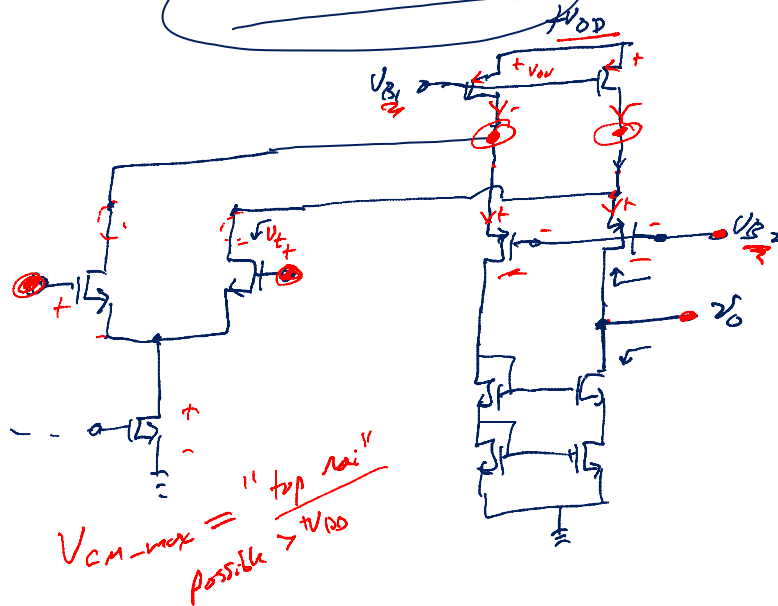


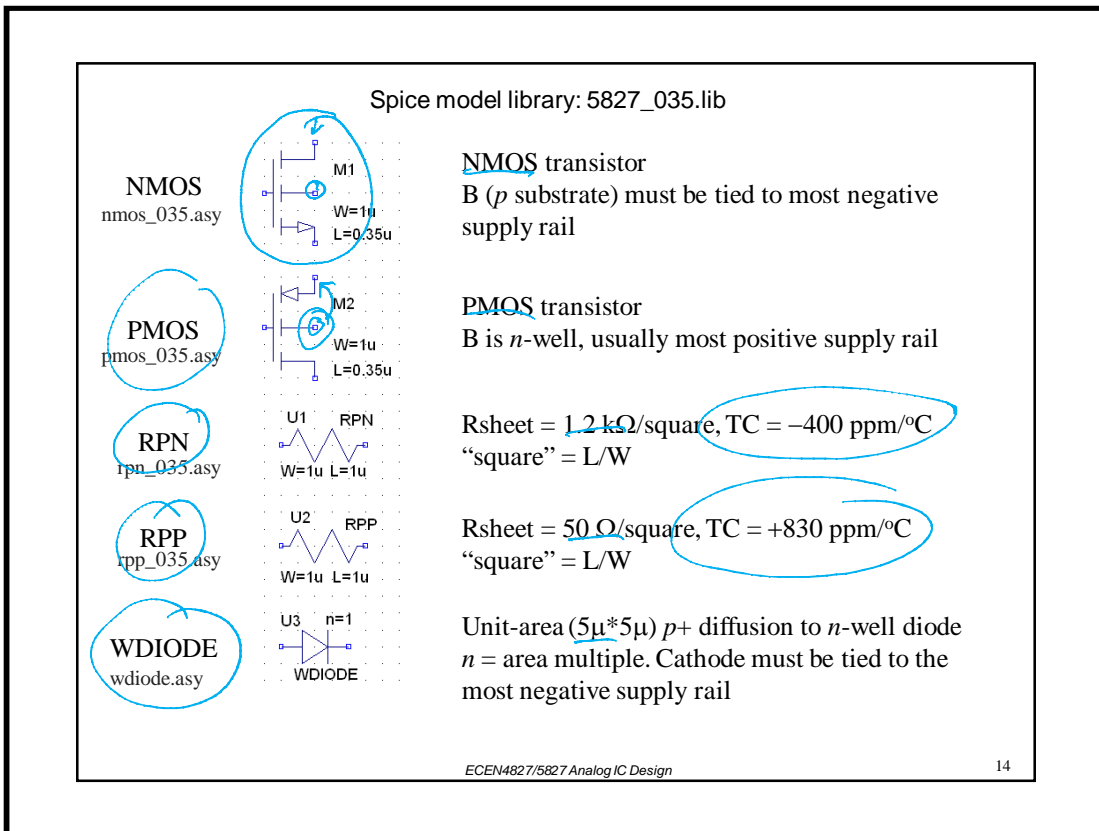
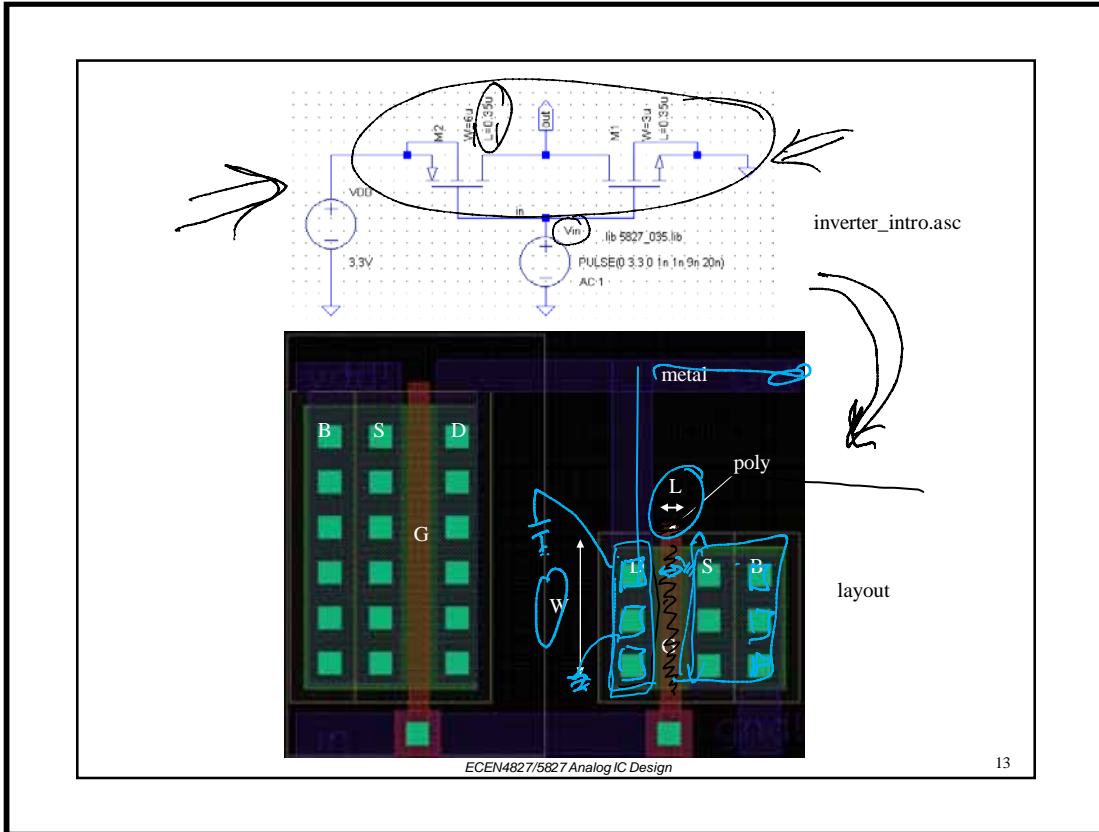
Allen/Holberg text Figure 6.5-2

Folded cascode



Folded cascode





Example: NMOS model

```

.subckt NM D G S B
+params: W=1u L=1u
M1 D G S B NM L={L} W={W} AS={2u*W} PS={2*(2u+W)} DS={2u*W} PD={2*(2u+W)}
.ends

* NMOS transistor model
.MODEL NM NMOS LEVEL=8

***** SIMULATION PARAMETERS *****
*
* format : LTspice
* model  : MOS BSIM3v3

TYPICAL MEAN CONDITION

*** Flags ***
+MOSMOD =1.000e+00 CAPMOD =2.000e+00
+NOIHMOS =3.000e+00
*
*** Threshold voltage related model parameters ***
+K1 =5.0296e-01
+K2 =3.3985e-02 K3 =-1.136e+00 K3B =-4.399e-01
+KCH =2.611e+17 UTH0 =4.979e-01
+UOFF =-1.925e-02 DUT0 =5.000e+01 DUT1 =1.039e+00
+DUT2 =-1.375e-03 KETA =2.032e-02
+PSCRF1 =1.518e+08 PSRFR2 =7.401e-05
... more (BSIM3 model is very detailed and complicated)...
        
```

- W, L are circuit design parameters, minimum 0.35μ, minimum increment 0.1μ
- NMOS Spice model can be used as a subcircuit, which allows automatic adjustments of AS (source area), PS (source perimeter), DS (drain area) and PD (drain perimeter) as functions of W, or as a native MOS device (user must then manually specify AS, PS, DS, PD)
- Very detailed BSIM3 model (industry standard)

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Approximate models for hand calculations

NMOS
nmos_035.asy

PMOS
pmos_035.asy

$V_m \approx 0.48 \text{ V}$
 $\mu_n C_{ox} \approx 90 \mu\text{A/V}^2$
 $\lambda_n \approx 0.035 \text{ 1/V (L=1}\mu\text{)}$
 $0.025 \text{ 1/V (L=2}\mu\text{)}$
 $< 0.015 \text{ 1/V (L>4}\mu\text{)}$

$V_{tp} \approx -0.62 \text{ V}$
 $\mu_p C_{ox} \approx 36 \mu\text{A/V}^2$
 $\lambda_p \approx 0.046 \text{ 1/V (L=1}\mu\text{)}$
 $0.019 \text{ 1/V (L=2}\mu\text{)}$
 $< 0.01 \text{ 1/V (L>4}\mu\text{)}$

Beware: do not expect very accurate results using hand calculations, especially for short channel lengths ($L < 2 \mu$)

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Setting up 0.35u CMOS symbols and model library for LTspice

Option 1: local (does not require administrative privileges)

- Place all symbol files (*.asy files) and model library (5827_035.lib) in a working folder, together with schematics

Option 2: make symbols and model library globally available

- Place all symbols (*.asy files) in a new folder (e.g. 5827) in

C:\Program Files\LTC\SwCADIII\lib\sym

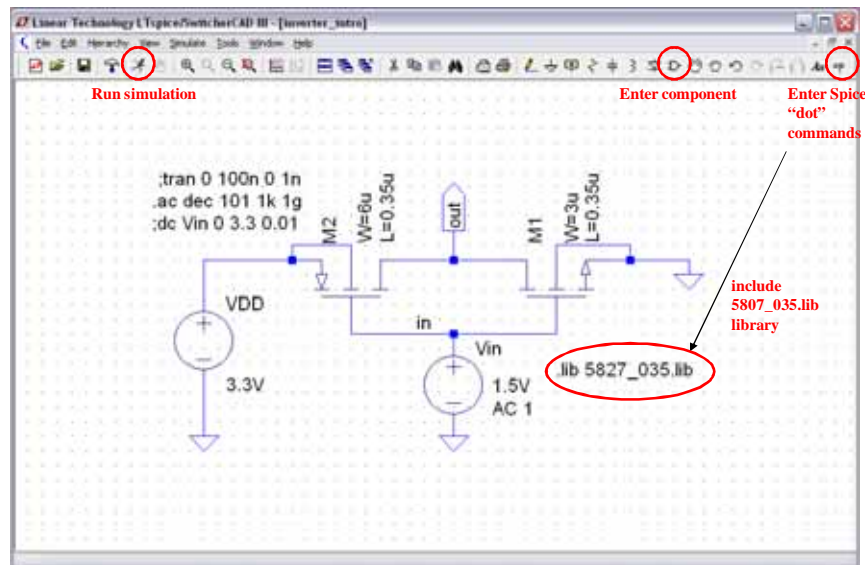
- Add model library 5827_035.lib to

C:\Program Files\LTC\SwCADIII\lib\sub

In any case, an LTspice schematic must include:

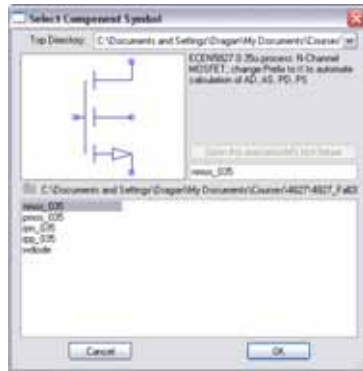
.lib 5827_035.lib

LTspice schematic entry



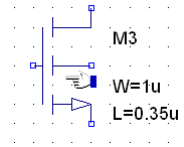
Use of NMOS symbol in LTspice

(1) place **nmos_035** symbol

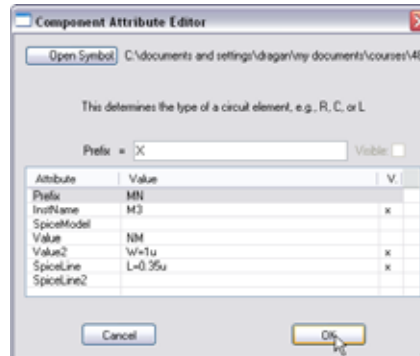


The same applies to **pmos_035**

(2) **CTRL-right click** to open Attribute Editor



(3) **Change Prefix to X** to use subcircuit model with automatic adjustments of AS, PS, AD, PD



Basic Spice simulations

Bias Point (.op)

- View DC operating point voltages and currents, and device small-signal model parameters in (text)

DC Sweep (.dc)

- Plot DC (or temperature) characteristics

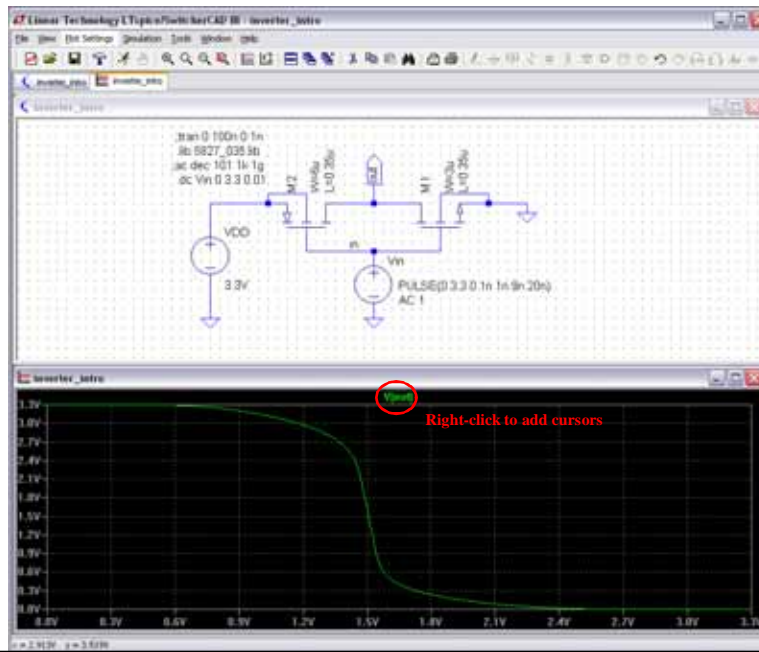
AC Sweep (.ac)

- Plot small-signal frequency responses

Transient (.tran)

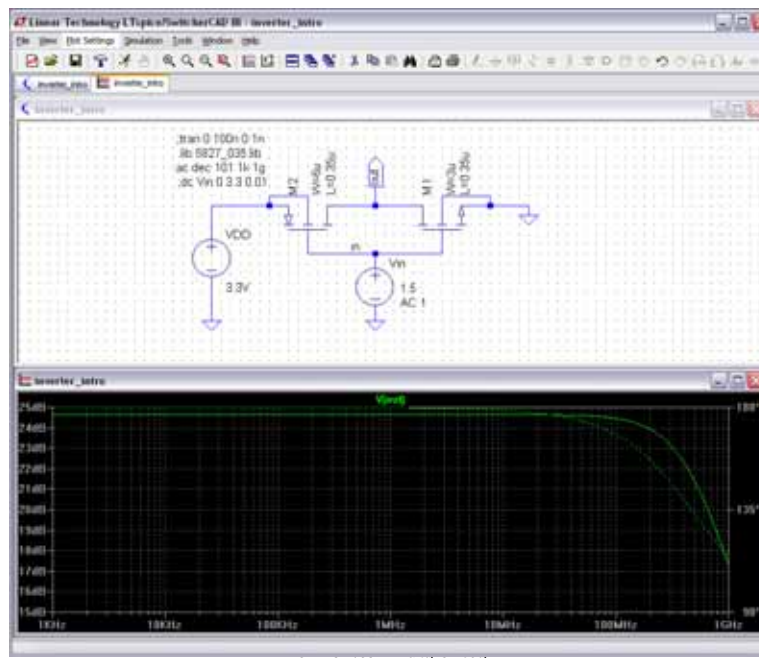
- Plot large-signal (total) waveforms

DC sweep example: inverter V_{OUT} versus V_{IN}



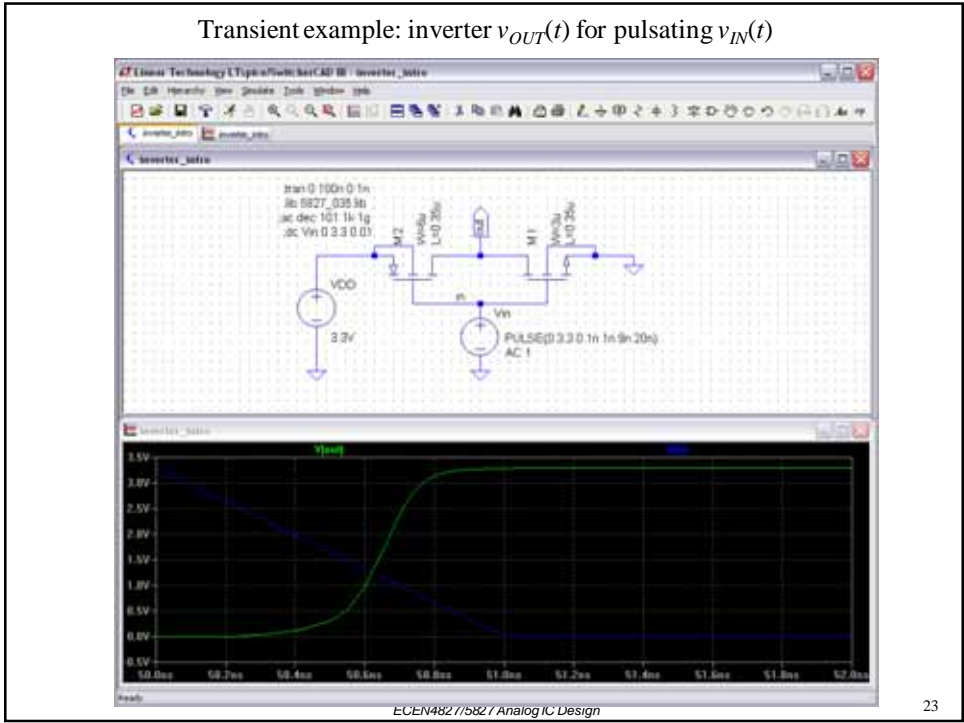
21

AC sweep example: inverter as an amplifier, magnitude response $\|v_{out}/v_{in}\|$ [dB]



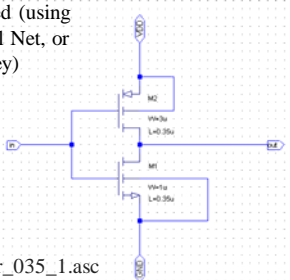
22

Transient example: inverter $v_{OUT}(t)$ for pulsating $v_{IN}(t)$

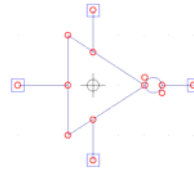


Hierarchical schematic entry

Inverter circuit with ports labeled (using Edit, Label Net, or F4 key)



Symbol representing the inverter circuit

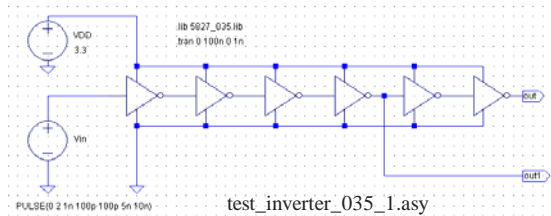


names must match

↑

↑

Symbols used to enter larger circuits



HW Problem S8

