Low Power Op-amp Design for Temperature Independent Voltage Reference

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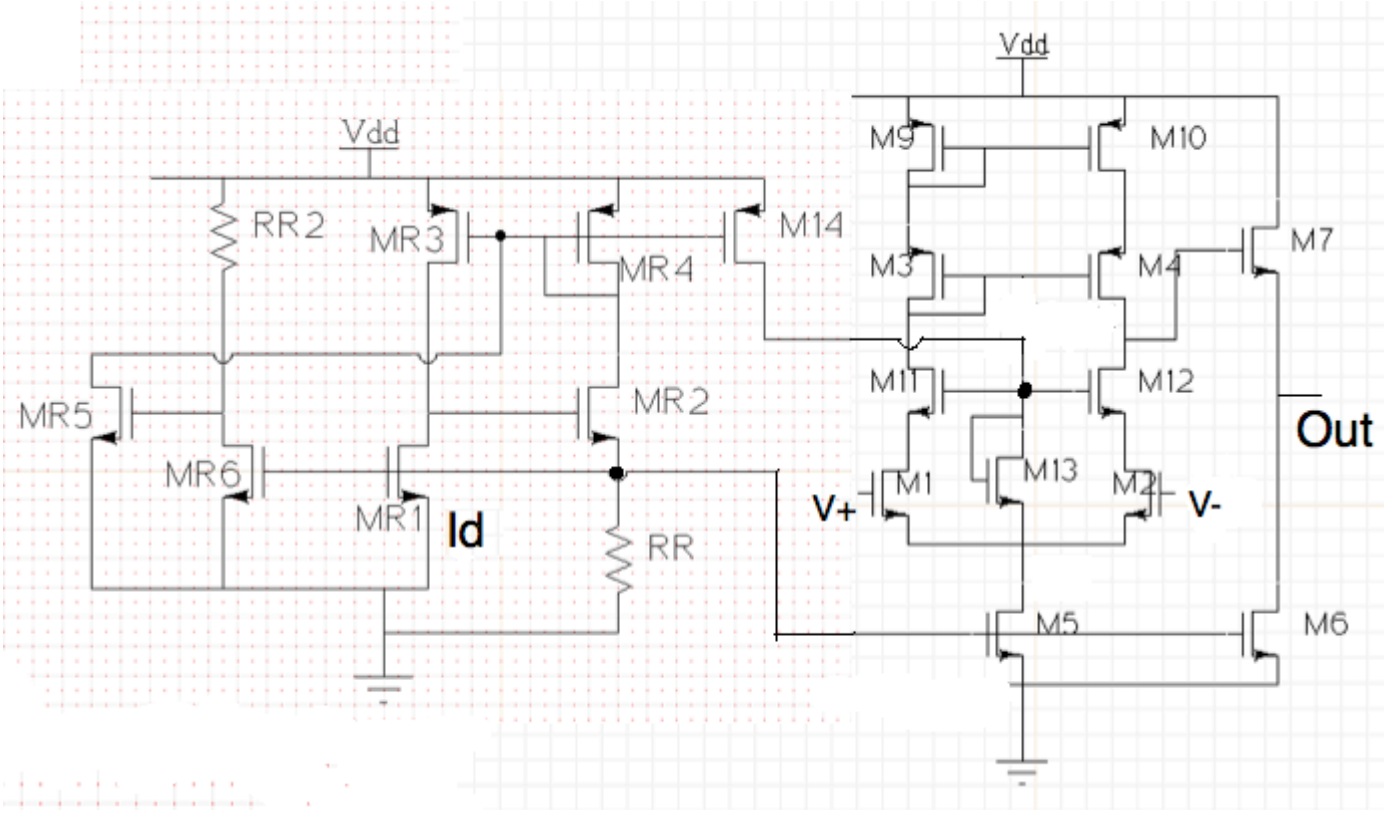

Figure 1: Supply Independent Current Mirror and Op-Amp

***Abstract*— In this project, we design a low power op-amp as part of a temperature independent voltage reference. Our op-amp is able to achieve a gain of 3120 while consuming only 0.1mW of power (without the output stage).**

I. Introduction

Fig. 1 shows our op-amp together with its supply-independent current mirrors. To achieve high gain, we use a cascode configuration for the first amplifier stage, which is based on a different pair (M1, M2). To ensure low output impedance, we use a source follower for the second stage (M7, M6). M13 is added to bias M11 and M12 for maximum swing. The current through each branch of the different pair is Id while the drain current through M13 is Id/2.

II. Supply Independent Current Design

For low power, Id is chosen to be as low as possible. Since $I_D = 2k'(W/L)(Vov)^2$ and Vov≥ 200mV for strong inversion, we want $(W/L)_N$ to be minimum = 1 for nmos $MR_{1\text{-}2}$ and Vov to be about 200mV. Thus $I_D = 2k'(W/L)(Vov)^2 \approx 5\mu A$. For pmos $MR_{3\text{-}4}$, choose $(W/L)_P = 2$ to obtain the same Vov and Id.

Since Id = Vgs1/RR, we choose resistor RR = (Vov+Vth)/Id ≈ 80kΩ. MR6 and MR5 together compose the start-up circuit. To turn off M5 after start-up, we want RR2 to be very large = 10MΩ. A large RR2 also helps to put M6 into triode mode and reduce the quiescent current drawn.

Since the channel length modulation effect will reduce power-supply rejection, we choose the length for the transistors MR1-4 be 10 times the minimum length to reduce λ. Thus $L_{MR1\text{-}4} = 10\mu m$, $W_{MR1\text{-}2} = 10\mu m$, $W_{MR3\text{-}4} = 20\mu m$. For convenience, MR6 and MR5 are chosen to have the same dimensions as the other nmos transistors. Simulation shows that when Vdd is increased from 5V to 6V, Id increases from 4.6μA to 4.8μA, a 4% increase. Fig. 2 shows the variation in Id (Ibias) against the supply voltage Vdd. Around 5V, Id is relatively insensitive to changes in Vdd.

To supply a current of Id/2 through M13, we want pmos M14 to have $W/L = 1/2(W/L)_P$ or W = 10 μm and L = 10 μm. To supply a current of Id into each of the branch of the differential pair, the total current through M5 should be 2.5×Id. Therefore, the dimensions of M5 are W = 25 μm and L = 10 μm.

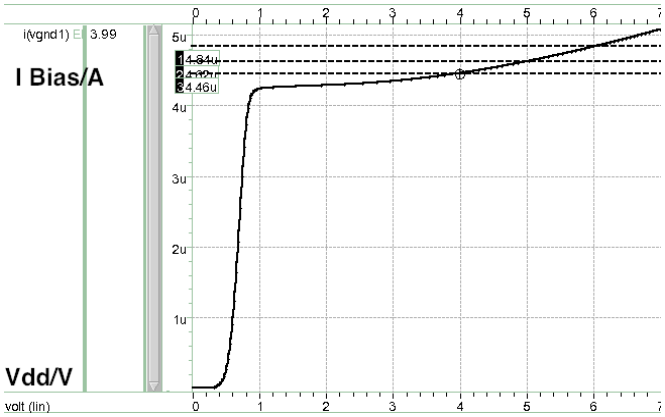

Figure 2. IBIAS vs Vdd between 0 and 7V

III. Amplifier Stages

As discussed previously, with I_D = 5μA, (W/L) = 1 gives Vov to be about 200mV for NMOS. Thus for the transistors in the first stage of the amplifier, i.e. the cascaded differential pair, we choose (W/L) = 1 for nmos MR1,2,11,12 and (W/L) = 2 for pmos MR3,4,9,10 (with L = 1 μm). For M13, since its drain current is about half of that of M1 and its overdrive voltage is about twice, its dimensions should be W/L = 1/8 or W = 1 μm and L = 8 μm.

A. Gain:

The gain of the amplifier is roughly equal to the gain of the first stage = $G_m \times R_o = g_{m1} \times (g_{m12} \times r_{012} \times r_{02} \parallel g_{m4} \times r_{04} \times r_{010})$ which is proportional to $g_m^2 \times r_o^2$. We note that although our current is low which translates to a low g_m , a low drain current will also means a high resistance for r_o . In fact, since g_m is proportional to the I_D/(Vgs-Vt) and r_0 is inversely proportional to I_D, $g_m \times r_o$ is inversely proportional to (Vgs-Vt) and we expect that with our choice of a low overdrive voltage (Vgs-Vt), a high gain should be achieved. This is confirmed in Fig. 3.

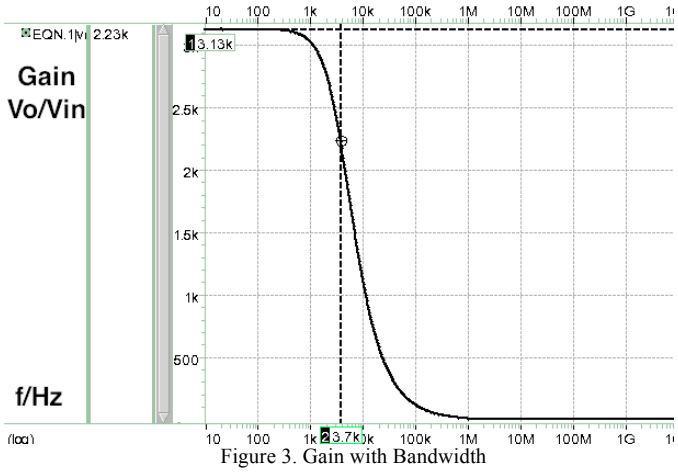

Figure 3. Gain with Bandwidth

Fig. 3 shows that our DC gain is 3120 and our 3dB cutoff frequency is 3.7kHz.

B. Output Impedance:

To achieve a low output impedance, the second stage is a source follower consisting of M7 and its biasing mirror transistor M6. The output impedance is approximately $1/g_{m7} = 1/(2I_{D7}k'W_7/L_7)^{1/2}$. Since we want the circuit to be low power, I_{D7} cannot be too high. Thus to ensure low output impedance, W_7/L_7 should be very large. However, since $1/g_{m7} = V_{ov7}/(2I_{D7})$, if we want $V_{ov7,min}$ = 200mV, for a maximum output resistance of 50Ω, at a minimum, I_{D7} has to be 2mA. A reasonable compromise is to aim for $V_{ov7,min}$ = 100mV and I_{D7} = 1mA which is realized with W_7= 1000 μm / L_7= 1 μm and W_6= 200 μm / L_7= 1 μm. Our measured output resistance is 51.7Ω ≈ 50Ω.

C. Stability:

Fig. 4 shows that our phase at unity gain is -95.8^0, which corresponds to a phase margin of 84.2^0. Thus our amplifier is stable and a compensation capacitor is not necessary. A compensation capacitor, if required, should be placed between the source and gate of M7 to move the zero to the left.

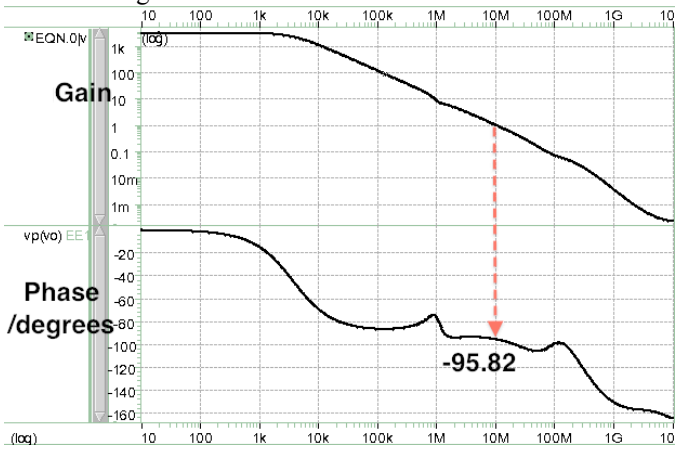

Figure 4. Gain and Phase of Vout/Vin vs Frequnecy.

D. Power Supply Rejection:

Fig. 5 shows a plot of A^+ = Vout/vdd versus frequency where vdd is a small signal applied to the power supply.

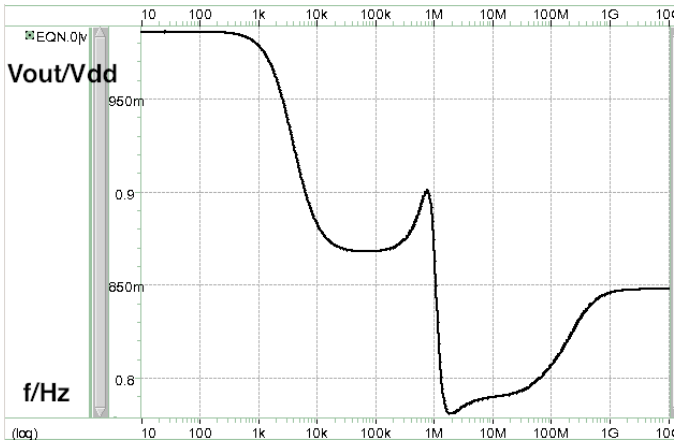

Fig. 5 Power Supply Gain A^+ versus frequency

We note that our power supply gain is quite low < 1 which implies a high Power Supply Rejection Ratio. The PSRR = A_{dm}/A^{+} is plotted in Fig. 6. As noted on the graph, our PSRR at DC is 3180, which deteriorates at higher frequency.

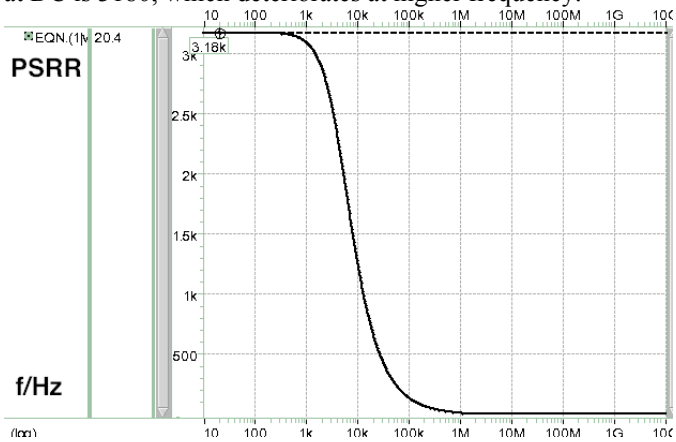

Fig. 6 Power Supply Rejection Ratio versus frequency

E. Temperature variation:

Our op-amp is tested in the band-gap voltage reference circuit configuration shown in Fig. 7 where it has been determined earlier that the optimum value for the resistors are R1=R3=1kΩ and R2=8.44kΩ.

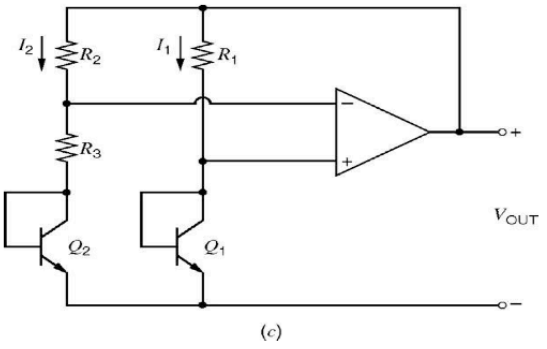

Fig. 7 Band-gap Voltage reference circuit

Figure 8 shows the variation of Vout against temperature (a) when no offset is applied and (b) when there is an offset voltage of 10mV.

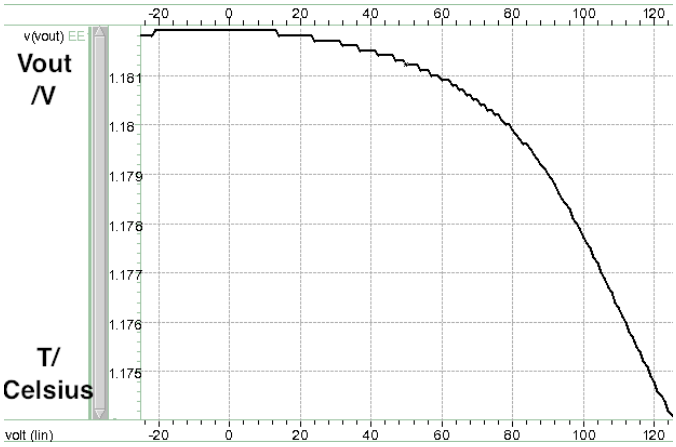

Fig. 8(a) Variation of Vout with temperature when Voffset = 0

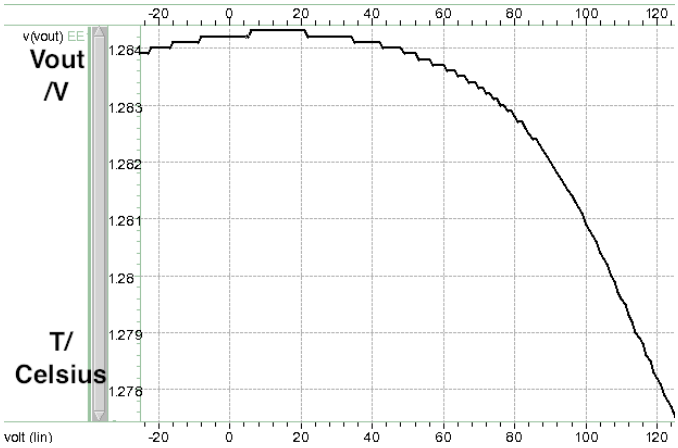

Fig. 8(b) Variation of Vout with temperature when Voffset = 10mV

In both cases, Vout only varies for about 8mV for the entire 150K temperature range, giving a temperature sensitivity of about 0.05mV/K.

F. Discussion of Power Consumption:

Due to the choice of a low biasing current $I_D \approx 5\mu A$, the current drawn by the op-amp not including the output stage is only 20.9μA, which corresponds to a low power consumption of 0.1mW. However, the output stage (source follower) draws a significantly larger current of 1.033mA (5.165mW) due to the requirement of a low output resistance. Our total power consumption is 5.265mW, 98% of which is due to the output stage.

For future work, alternate methods such as Class A and Class AB output stages should be explored for lower power consumption. The use of an internal feedback loop to reduce output impedance with a low quiescence current could also be explored.

G. Table of Component Sizing and Specifications:

TABLE I
COMPONENTS SIZES

M1, M2, M11, M12,	*W= 1u, L=1u*
M3, M4, M9, M10	*W= 2u, L=1u*
M6	*W = 200u, L=1u*
M7	*W=1000u, L=1u*
MR1, MR2, MR5, MR6, M14	*W=10u, L=10u*
MR3, MR4	*W=20u, L=10u*
M13	*W=1u, L=8u*
RR	*80kΩ*
RR2	*10MΩ*

TABLE II
SPECIFICATIONS AND PERFORMANCE

	Specification	*Actual Performance*
Gain	*>1000*	*3120*
Phase margin	*$>60^0$*	*84.2^0*
Output resistance	*50Ohm*	*~50Ohm*
PSRR	*>1000*	*3180*
Temperature dependence	*<1mV/K*	*0.05mV/K*
Bias Current Power-supply Sensitivity	*<10% per extra 1V VDD*	*4%*

IV. CONCLUSIONS

In this project, we have designed a low power op-amp for voltage reference application. For future work, a better ouput stage should be designed to minimize the quiescent current drawn while maintaining the low output impedance.

ACKNOWLEDGMENT

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REFERENCES

[1] P. R. Gray, P. J. Hurst, S. H. Lewis and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*, 5th ed., 2010.