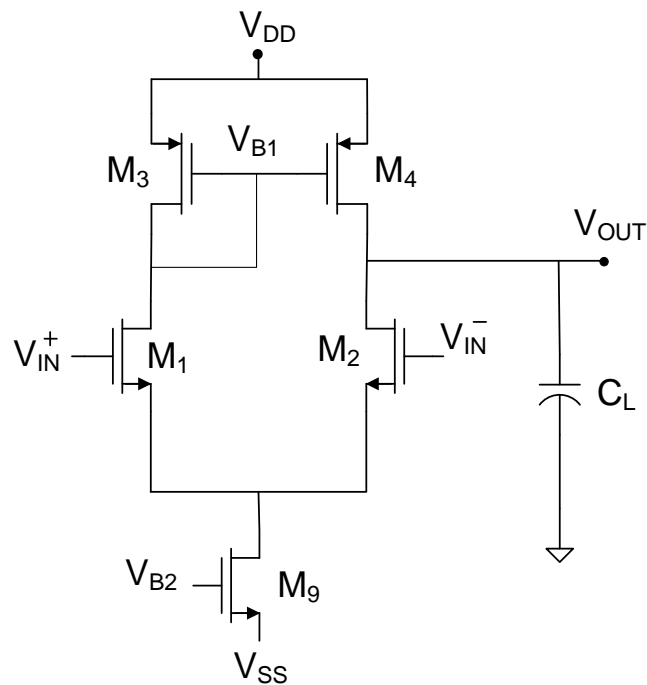


EE 435
 Homework 4
 Spring 2009

In the following problems, if reference to a semiconductor process is needed, assume processes with the following characteristics: CMOS Process -- $\mu_n C_{OX} = 100 \mu\text{A}/\text{V}^2$, $\mu_p C_{OX} = \mu_n C_{OX}/3$, $V_{TNO} = 0.5\text{V}$, $V_{TPO} = -0.5\text{V}$, $C_{OX} = 2\text{fF}/\mu^2$, $\lambda_n = \lambda_p = 0.01\text{V}^{-1}$, and $\gamma = 0.4\text{V}^{-1/2}$, Bipolar Process -- $J_S = 10^{-15}\text{A}/\mu^2$, $\beta = 100$ and $V_{AF} = 150\text{V}$. If more extensive parasitic capacitance parameters, use the model parameters in the attachment for the AMI 0.5u CMOS process.

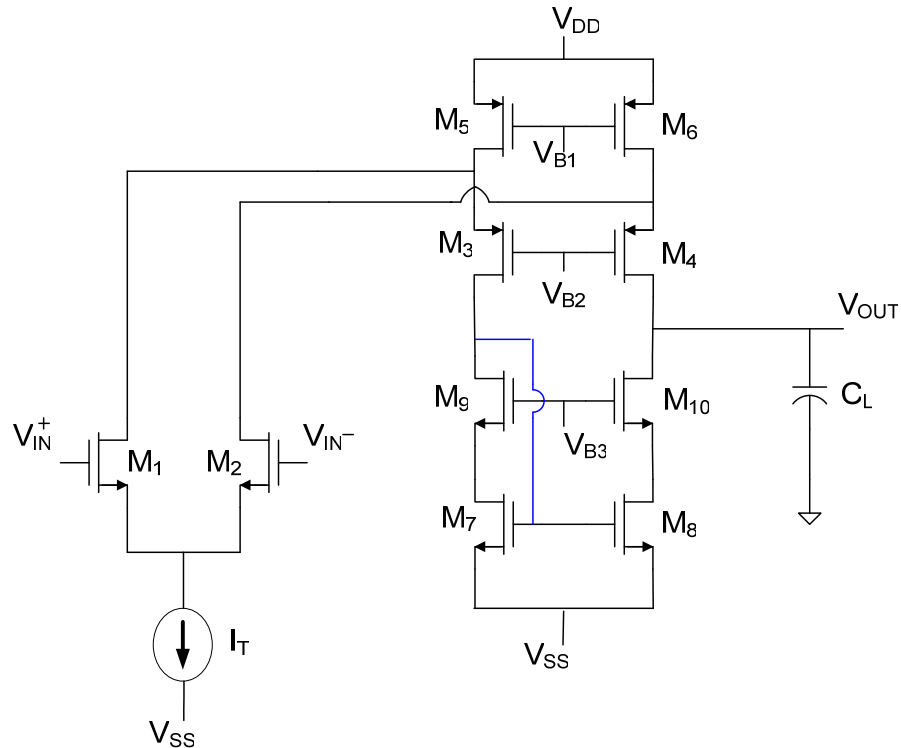
Problem 1 A reference op amp was designed with $V_{EB1} = V_{EB3} = 500\text{mV}$. If the supply voltages were $V_{DD} = 2.5\text{V}$, $V_{SS} = -2.5\text{V}$, determine

- The systematic output offset voltage
- The systematic input-referred offset voltage
 (assume $V_{IC} = 0\text{V}$ and the desired output voltage is 0V)



Problem 2 Assume that a folded-cascode op amp with n-channel inputs, tail-current input bias, and current-mirror n-channel biasing was designed so that all transistors had $V_{EB}=0.25V$. If $V_{DD} = 2.5V$, $V_{SS} = -2.5V$, $V_{B2}=1.4V$, $V_{B3} = -1.4V$, and the bias current in transistors $\{M_1, M_2, M_3, M_4, M_7, M_8, M_9, \text{ and } M_{10}\}$ are all the same,

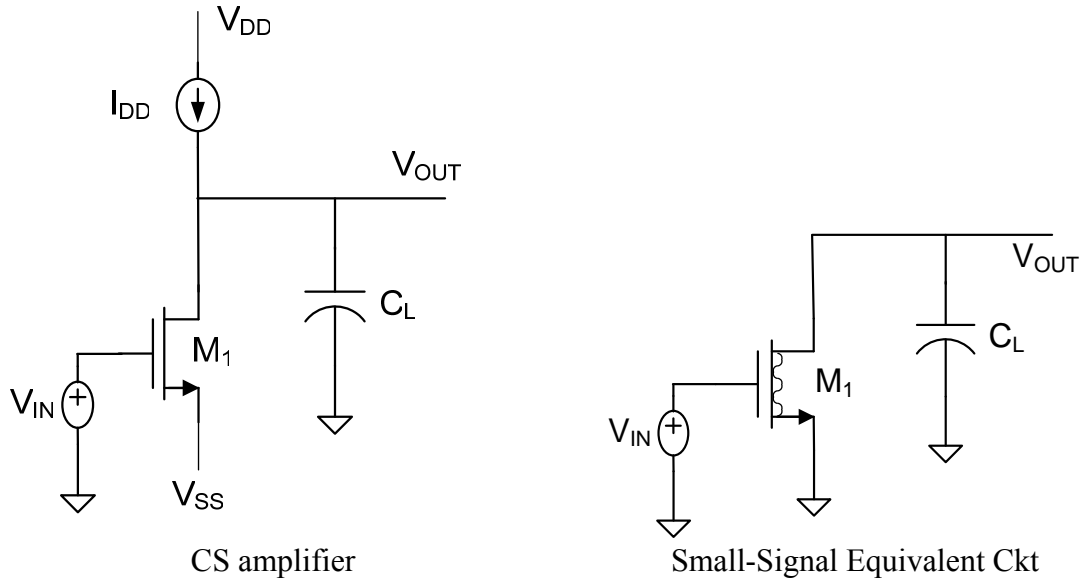
- Determine the devices sizes if $P=2mW$
- Determine the SR if the load capacitance is $2pF$
- What is the output signal swing?
- What is the dc gain of the amplifier?



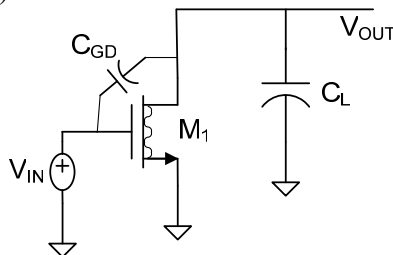
Problem 3 Analytically compare the power dissipation and the gain for the folded cascode amplifier discussed in Problem 2 with that of the reference op amp with the same excess biases and the same GB?

Problem 4 Analytically compare the power dissipation and the gain for the folded cascode amplifier discussed in Problem 2 with that of the telescopic cascode op amp with the same excess biases and the same GB?

Problem 5 The GB of the CS amplifier was shown to be g_m/C_L . In this derivation, C_L is the total load capacitance on the output node and the high-frequency coupling capacitance, C_C , from Gate to Drain was neglected.



- What is the GB of this amplifier if V_{SS} is chosen so that $V_{EB}=0.2V$ and $P=100\mu W$ (assume $V_{DD}=2.5V$)?
- What is the W/L ratio required for $V_{EB}=0.2V$ and $P=100\mu W$
- With the W/L ratio obtained in part b) and a length of $L=2\mu$, determine the parasitic drain-substrate capacitance, C_{DSUB} .
- If the load capacitance of $500fF$ is entirely an external load, how much will the dc gain and the GB change if the parasitic capacitance C_{DSUB} is present?
- What effect will the parasitic capacitance C_{GD} that has been neglected up to this point have on the GB of the amplifier? (Analytically derive GB if C_{GD} effects are included)



- Estimate the value of C_{GD} if the MOS device is fabricated in a 0.5μ AMI process assuming the same biasing as in part a)

TRANSISTOR PARAMETERS

| | W/L | N-CHANNEL | P-CHANNEL | UNITS |
|--------------------|----------|-----------|-----------|----------------------|
| MINIMUM | 3.0/0.6 | | | |
| Vth | | 0.78 | -0.93 | volts |
| SHORT | 20.0/0.6 | | | |
| Idss | | 439 | -238 | uA/um |
| Vth | | 0.69 | -0.90 | volts |
| Vpt | | 10.0 | -10.0 | volts |
| WIDE | 20.0/0.6 | | | |
| Ids0 | | < 2.5 | < 2.5 | pA/um |
| LARGE | 50/50 | | | |
| Vth | | 0.70 | -0.95 | volts |
| Vjtkd | | 11.4 | -11.7 | volts |
| Ijtk | | <50.0 | <50.0 | pA |
| Gamma | | 0.50 | 0.58 | V ^{0.5} |
| K' (Uo*Cox/2) | | 56.9 | -18.4 | uA/V ² |
| Low-field Mobility | | 474.57 | 153.46 | cm ² /V*s |

COMMENTS: XL_AMI_C5F

| FOX TRANSISTORS | GATE | N+ACTIVE | P+ACTIVE | UNITS |
|-----------------|------|----------|----------|-------|
| Vth | Poly | >15.0 | <-15.0 | volts |

| PROCESS PARAMETERS | N+ACTV | P+ACTV | POLY | PLY2_HR | POLY2 | MTL1 | MTL2 | UNITS |
|----------------------|--------|--------|------|---------|-------|------|------|----------|
| Sheet Resistance | 82.7 | 103.2 | 21.7 | 984 | 39.7 | 0.09 | 0.09 | ohms/sq |
| Contact Resistance | 56.2 | 118.4 | 14.6 | | 24.0 | | 0.78 | ohms |
| Gate Oxide Thickness | | 144 | | | | | | angstrom |

| PROCESS PARAMETERS | MTL3 | N\PLY | N_WELL | UNITS |
|--------------------|------|-------|--------|---------|
| Sheet Resistance | 0.05 | 824 | 815 | ohms/sq |
| Contact Resistance | 0.78 | | | ohms |

COMMENTS: N\POLY is N-well under polysilicon.

| CAPACITANCE PARAMETERS | N+ACTV | P+ACTV | POLY | POLY2 | M1 | M2 | M3 | N_WELL | UNITS |
|------------------------|--------|--------|------|-------|----|----|----|--------|--------------------|
| Area (substrate) | 429 | 721 | 82 | | 32 | 17 | 10 | 40 | aF/um ² |
| Area (N+active) | | | 2401 | | 36 | 16 | 12 | | aF/um ² |
| Area (P+active) | | | 2308 | | | | | | aF/um ² |
| Area (poly) | | | | 864 | 61 | 17 | 9 | | aF/um ² |
| Area (poly2) | | | | | 53 | | | | aF/um ² |
| Area (metal1) | | | | | | 34 | 13 | | aF/um ² |
| Area (metal2) | | | | | | | 32 | | aF/um ² |
| Fringe (substrate) | 311 | 256 | | | 74 | 58 | 39 | | aF/um |
| Fringe (poly) | | | | | 53 | 40 | 28 | | aF/um |
| Fringe (metal1) | | | | | | 55 | 32 | | aF/um |
| Fringe (metal2) | | | | | | | 48 | | aF/um |
| Overlap (N+active) | | | 206 | | | | | | aF/um |
| Overlap (P+active) | | | 278 | | | | | | aF/um |