Polytech'Montpellier
ERII 4

Design of Analog IC's

Chapitre IV
Advanced Analog Design Techniques

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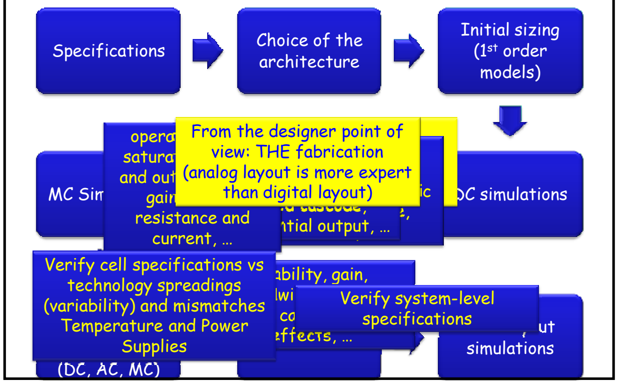
Outline

- Analog IC Design Flow
- Advanced specifications
- Advanced design techniques

Analog IC Design Flow



opera… satura… and out… gain… resistance and current, …

From the designer point of view: THE fabrication (analog layout is more expert than digital layout)

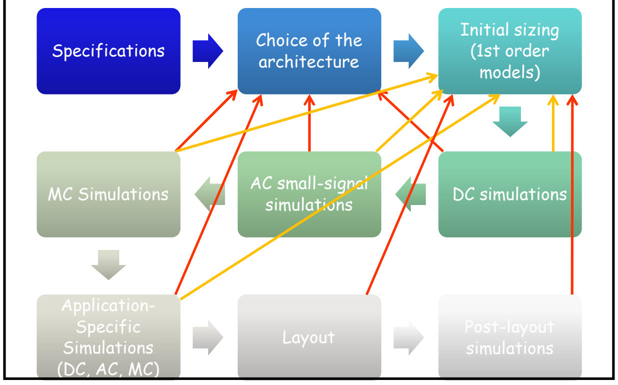
…tial output, …

Verify cell specifications vs technology spreadings (variability) and mismatches Temperature and Power Supplies

…ability, gain, …wi… co… effects, …

Verify system-level specifications

Analog IC Design Flow



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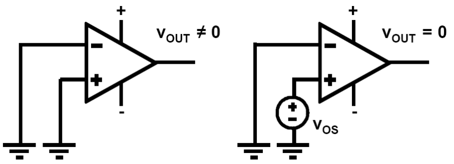
- Analog IC Design Flow
- Advanced specifications
  - Offset considerations
  - Common Mode Rejection Ratio
  - Design for low mismatches
  - Noise fundamentals
  - Characterization
- Advanced design techniques

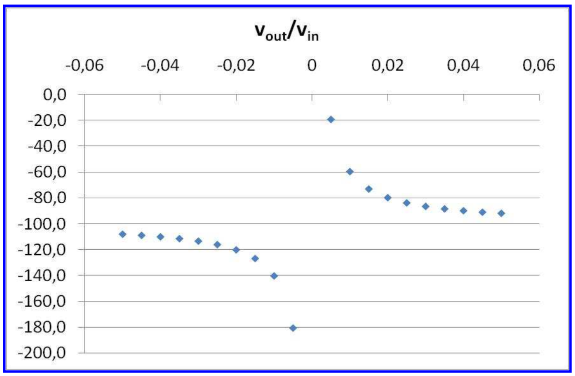
Offset considerations

- Definition: "input offset" of a differential amplifier is the differential input voltage that leads to a zero output voltage



SYMMETRICAL POWER SUPPLIES !!!

Offset considerations



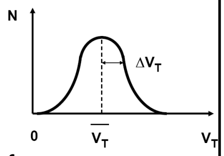
Offset considerations

- Offset is a random phenomenon due to:
  - Technology spreading → low "frequency" variations (die to die ; wafer to wafer ; run to run)
  - Mismatches → high "frequency" variations (device to device)
  - Variability → hot topic covering both previous origins
    - affecting technology parameters and dimensions
    - generally following a Gaussian distribution.
- Propagation to circuit behavior
  - Example: incertitude on saturation current
  - μC_{ox}, W/L and V_t are affected

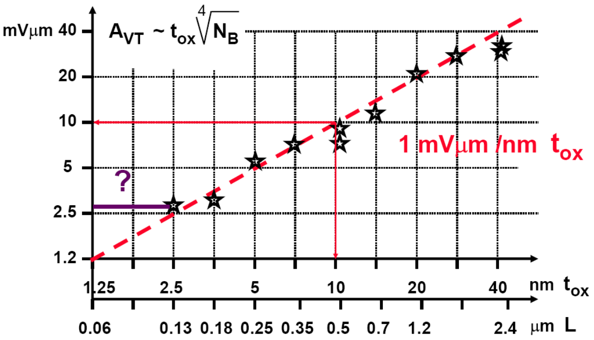
$$\boxed{I_{dsat} = \frac{\mu C_{ox}}{2}\frac{W}{L}\left(V_{gs} - V_t\right)^2}$$

Offset considerations

- *Gaussian distribution basics*
  - For a large number of identical devices the distribution of actual V_t (μC_{ox}, W/L) follows a Gaussian distribution
  - 0.5% of the values are more than ±3σ away from the average value
  - 6σ designs are then the standard in industry
    → 99.5% of yield in absence of defects
  - Run to run σ (technology spreading) is much higher than device to device σ (mismatches)
    → MC simulations



Offset considerations



Offset considerations

- μC_{ox} mismatches
  - Similar expressions than for V_t

$$\frac{\sigma_{\mu C_{ox}}}{\mu C_{ox}} = \frac{A_{\mu C_{ox}}}{\sqrt{WL}}$$

$$A_{\mu C_{ox}} \approx 0{,}0056\ \mu m$$

- W/L mismatches
- Example: 100μm/1μm NMOS in a 0,6 μm tech.

$$\frac{\sigma_{W/L}}{W/L} = A_{W/L}\sqrt{\frac{1}{W^2} + \frac{1}{L^2}}$$

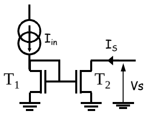
$$A_{W/L} \approx 0{,}02\mu m$$

$$\frac{\sigma_{V_t}}{V_t} = \frac{1{,}2mV}{600mV} = 0{,}2\% \qquad \frac{\sigma_{\mu C_{ox}}}{\mu C_{ox}} = 0{,}00056 = 0{,}056\% \qquad \frac{\sigma_{W/L}}{W/L} = 2\%$$

- 50% more for a PMOS
- 10 times less for MOST on the same die (mismatches)

Offset considerations

- Random offset in a current mirror

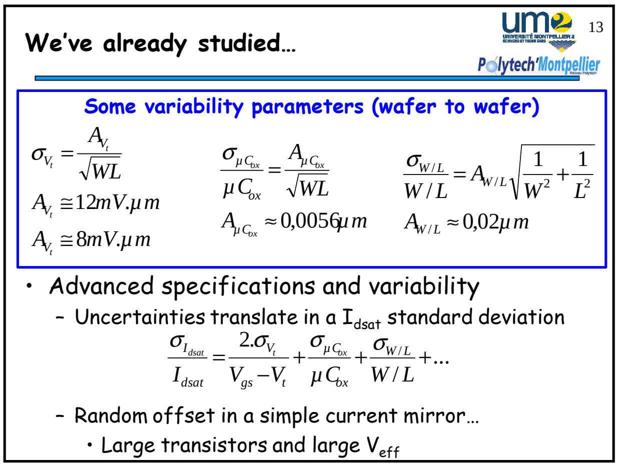


$$I_S = I_{dsat} = \frac{\mu C_{ox}}{2}\frac{W}{L}\left(V_{gs} - V_t\right)^2$$

$$\frac{\sigma_{I_S}}{I_S} = \frac{2.\sigma_{V_t}}{V_{gs} - V_t} + \frac{\sigma_{\mu C_{ox}}}{\mu C_{ox}} + \frac{\sigma_{W/L}}{W/L}$$

- Design tips
  → Large area and V_{eff}, long

• W=100μm ; L=1μm ; V_{eff}=0,1V	0,24%	56*ppm*	0,2%
• W=10μm ; L=10μm ; V_{eff}=1V	0,024%	56*ppm*	0,028%



We've already studied…

Some variability parameters (wafer to wafer)

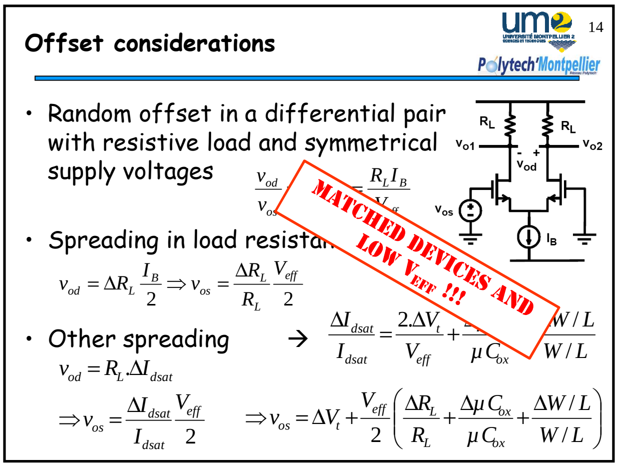
$$\sigma_{V_t} = \frac{A_{V_t}}{\sqrt{WL}} \qquad \frac{\sigma_{\mu C_{ox}}}{\mu C_{ox}} = \frac{A_{\mu C_{ox}}}{\sqrt{WL}} \qquad \frac{\sigma_{W/L}}{W/L} = A_{W/L}\sqrt{\frac{1}{W^2} + \frac{1}{L^2}}$$

$$A_{V_t} \cong 12mV.\mu m \qquad A_{\mu C_{ox}} \approx 0{,}0056\mu m \qquad A_{W/L} \approx 0{,}02\mu m$$

$$A_{V_t} \cong 8mV.\mu m$$

- Advanced specifications and variability
  - Uncertainties translate in a I_{dsat} standard deviation

    $$\frac{\sigma_{I_{dsat}}}{I_{dsat}} = \frac{2.\sigma_{V_t}}{V_{gs} - V_t} + \frac{\sigma_{\mu C_{ox}}}{\mu C_{ox}} + \frac{\sigma_{W/L}}{W/L} + \ldots$$
  - Random offset in a simple current mirror…
    - Large transistors and large V_{eff}



Offset considerations

- Random offset in a differential pair with resistive load and symmetrical supply voltages

$$\frac{v_{od}}{v_{os}} = \frac{R_L I_B}{V_{eff}}$$

MATCHED DEVICES AND LOW V_{EFF} !!!

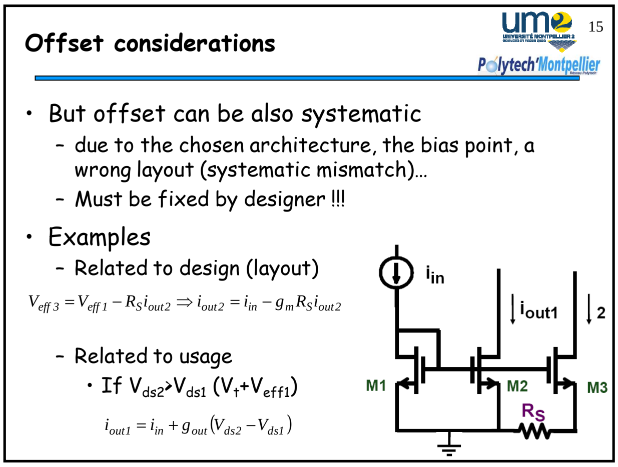
- Spreading in load resista

$$v_{od} = \Delta R_L \frac{I_B}{2} \Rightarrow v_{os} = \frac{\Delta R_L}{R_L}\frac{V_{eff}}{2}$$

- Other spreading → $\frac{\Delta I_{dsat}}{I_{dsat}} = \frac{2.\Delta V_t}{V_{eff}} + \frac{}{\mu C_{ox}} \quad \frac{W/L}{W/L}$

$$v_{od} = R_L.\Delta I_{dsat}$$

$$\Rightarrow v_{os} = \frac{\Delta I_{dsat}}{I_{dsat}}\frac{V_{eff}}{2} \qquad \Rightarrow v_{os} = \Delta V_t + \frac{V_{eff}}{2}\left(\frac{\Delta R_L}{R_L} + \frac{\Delta\mu C_{ox}}{\mu C_{ox}} + \frac{\Delta W/L}{W/L}\right)$$



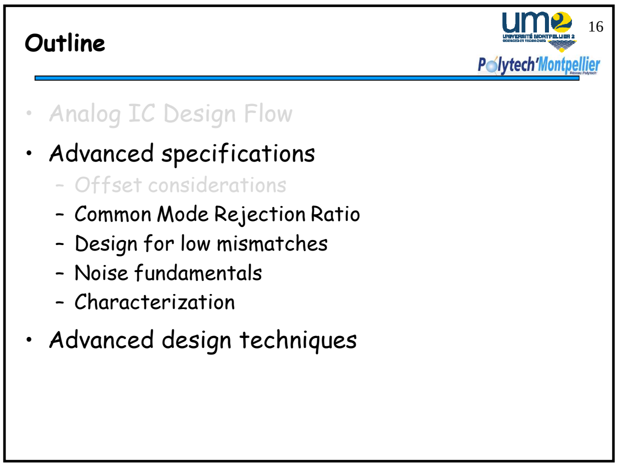
Offset considerations

- But offset can be also systematic
  - due to the chosen architecture, the bias point, a wrong layout (systematic mismatch)…
  - Must be fixed by designer !!!
- Examples
  - Related to design (layout)

$$V_{eff\,3} = V_{eff\,1} - R_S i_{out2} \Rightarrow i_{out2} = i_{in} - g_m R_S i_{out2}$$

  - Related to usage
    - If V_{ds2}>V_{ds1} (V_t+V_{eff1})

$$i_{out1} = i_{in} + g_{out}(V_{ds2} - V_{ds1})$$



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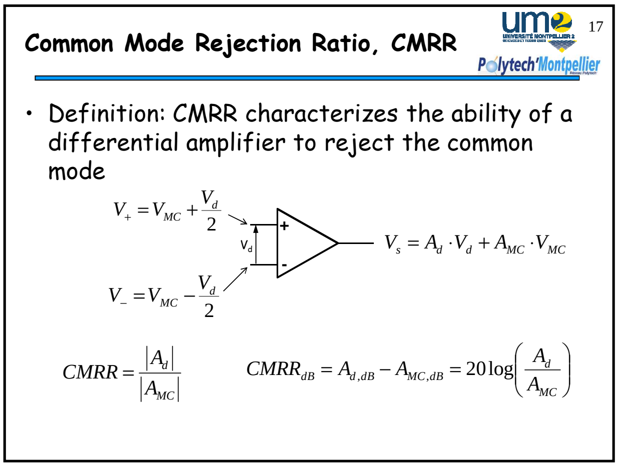


Common Mode Rejection Ratio, CMRR

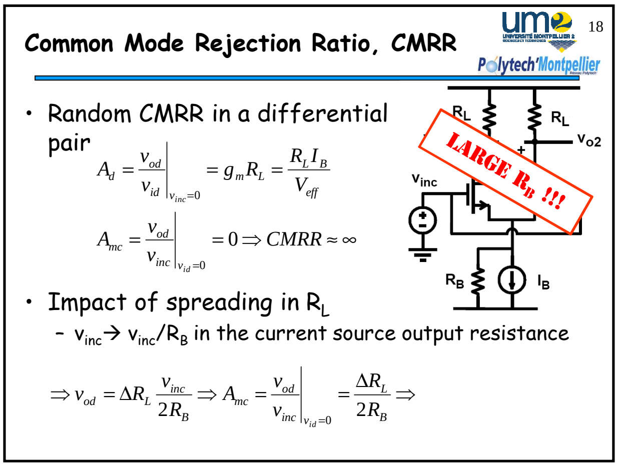
- Definition: CMRR characterizes the ability of a differential amplifier to reject the common mode

$$V_+ = V_{MC} + \frac{V_d}{2}$$

$$V_s = A_d \cdot V_d + A_{MC} \cdot V_{MC}$$

$$V_- = V_{MC} - \frac{V_d}{2}$$

$$CMRR = \frac{|A_d|}{|A_{MC}|} \qquad CMRR_{dB} = A_{d,dB} - A_{MC,dB} = 20\log\left(\frac{A_d}{A_{MC}}\right)$$



Common Mode Rejection Ratio, CMRR

- Random CMRR in a differential pair

$$A_d = \left.\frac{v_{od}}{v_{id}}\right|_{v_{inc}=0} = g_m R_L = \frac{R_L I_B}{V_{eff}}$$

$$A_{mc} = \left.\frac{v_{od}}{v_{inc}}\right|_{v_{id}=0} = 0 \Rightarrow CMRR \approx \infty$$

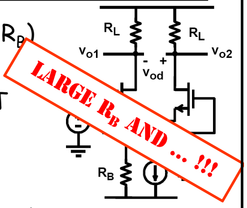
LARGE R_B !!!

- Impact of spreading in R_L
  - v_{inc}→ v_{inc}/R_B in the current source output resistance

$$\Rightarrow v_{od} = \Delta R_L \frac{v_{inc}}{2R_B} \Rightarrow A_{mc} = \left.\frac{v_{od}}{v_{inc}}\right|_{v_{id}=0} = \frac{\Delta R_L}{2R_B} \Rightarrow$$

Common Mode Rejection Ratio, CMRR

- Without R_L spreading, $v_{inc}/(2.R_B)$ in each load resistance
- Impact of spreading in MOST



$$v_{od} = R_L \Delta I(R_L) = R_L \frac{v_{inc}}{2R_B}\frac{\Delta I_{dsat}}{I_{dsat}}$$

$$\Rightarrow A_{mc} = \frac{v_{od}}{v_{inc}} = \frac{R_L}{2R_B}\left(\frac{2.\Delta V_t}{V_{eff}} + \frac{\Delta \mu C_{ox}}{\mu C_{ox}} + \frac{\Delta W/L}{W/L}\right)$$

Random CMRR and offset trade-off

- Design of low offset and high CMRR differential pair

$$v_{os} = \Delta V_t + \frac{V_{eff}}{2}\left(\frac{\Delta R_L}{R_L} + \frac{\Delta \mu C_{ox}}{\mu C_{ox}} + \frac{\Delta W/L}{W/L}\right) \quad CMRR = \frac{2 g_m R_B}{\frac{\Delta R_L}{R_L} + \frac{2.\Delta V_t}{V_{eff}} + \frac{\Delta \mu C_{ox}}{\mu C_{ox}} + \frac{\Delta W/L}{W/L}}$$

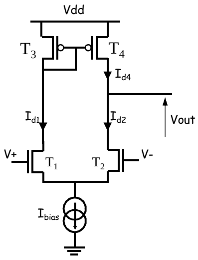
$$v_{os} \cdot CMRR = g_m V_{eff} R_B = I_B R_B$$

- The lower the offset, the higher the CMRR

1. Optimize for low offset
   - Low V_{eff} (0,1V), large transistors, matched resistors → reduce V_t spreading and current mismatch
2. Optimize for large CMRR → High $g_m(I_B)$ & R_B

Systematic CMRR

- Current source output resistance: R_B
- Common Mode V_{inc} → change bias current V_{inc}/R_B
- V_{inc}/R_B equally shares between T_1 and T_2
- Small-signal analysis to calculate induced output voltage



$$CMRR = 2 g_{m2} g_{m3} r_{ds1} R_B$$

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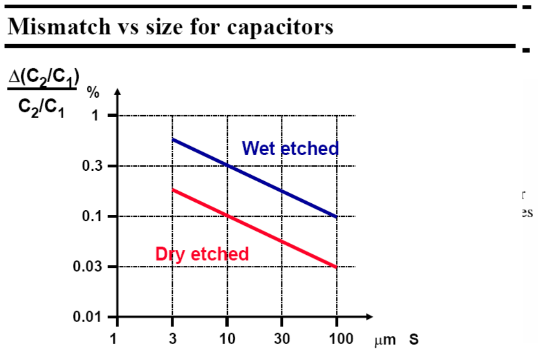
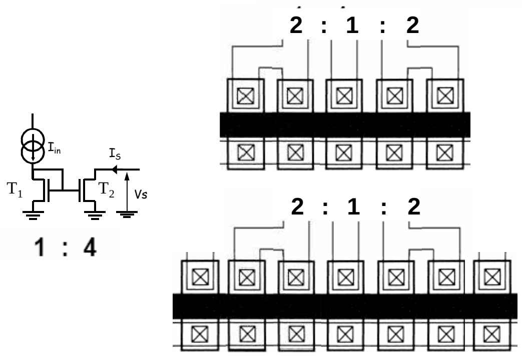
Design for low mismatches


Mismatch vs size for capacitors

Design for low mismatches



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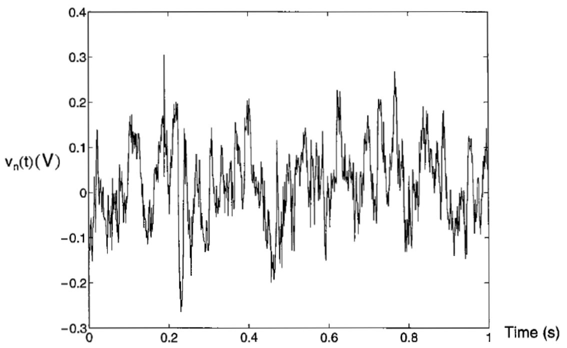
Noise considerations

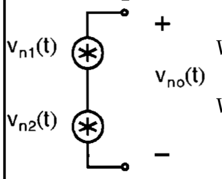
- Noise is any unwanted signal that interferes with a desired signal.
  - It can be deterministic or random.
  - It can be inherent to the circuit itself or coming from interferences with the outside world.
- Interference noise is caused by an identifiable external source. It can be deterministic or random.
  - e.g.: 50Hz hum in a loudspeaker, cellular phone interfering with a TV set, …
  - It can usually be eliminated by proper methods of grounding, shielding, etc (electromagnetic compatibility, EMC)
- Inherent noise is generated by the circuit itself. It is always random.
  - e.g.: resistance and transistors are noisy
  - Different shape of random noises are thermal, shot and flicker
  - It can not be eliminated (inherent) but its effects can be reduced by changing the circuit structure or the power consumption.

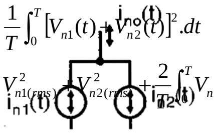
Random noise basics



Random noise basics

- Noise combination
  - Different noise sources combine as voltages in series and current in parallel





$$V^2_{no(rms)} = \frac{1}{T}\int_0^T [V_{n1}(t)+V_{n2}(t)]^2.dt$$

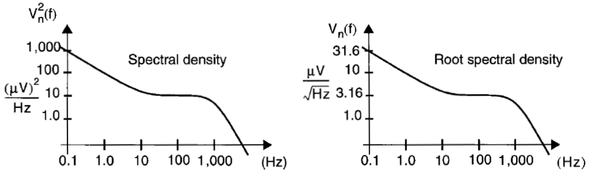
$$V^2_{no(rms)} = V^2_{n1(rms)} + V^2_{n2(rms)} + \frac{2}{T}\int_0^T V_{n1}(t).V_{n2}(t).dt$$

  - Assuming uncorrelated noise sources

$$\boxed{V^2_{no(rms)} = V^2_{n1(rms)} + V^2_{n2(rms)}}$$

Random noise basics

- Frequency-domain analysis
  - Noise spectral density



  - Noise is considered only in the bandwidth of the system → filtered out elsewhere
  - Noise rms value @ 100Hz for a 90Hz bandwidth? A 0.1 Hz bandwidth?

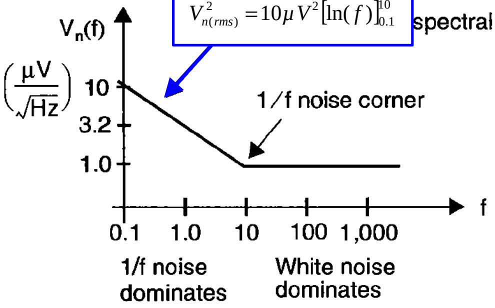
Random noise basics

- Noise Spectr… …ain shapes

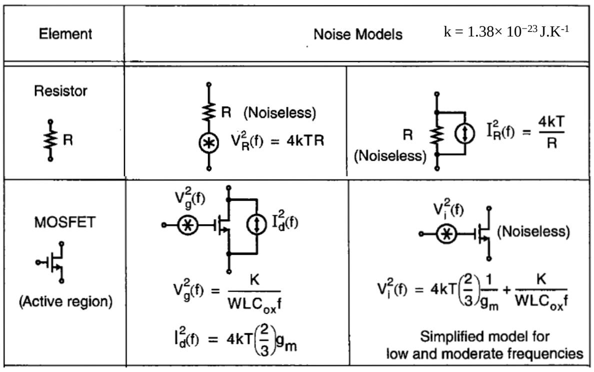
$$V^2_{n(rms)} = \int_{0.1}^{10} \frac{10\mu V^2}{f}.df$$

$$V^2_{n(rms)} = 10\mu V^2 [\ln(f)]_{0.1}^{10}$$

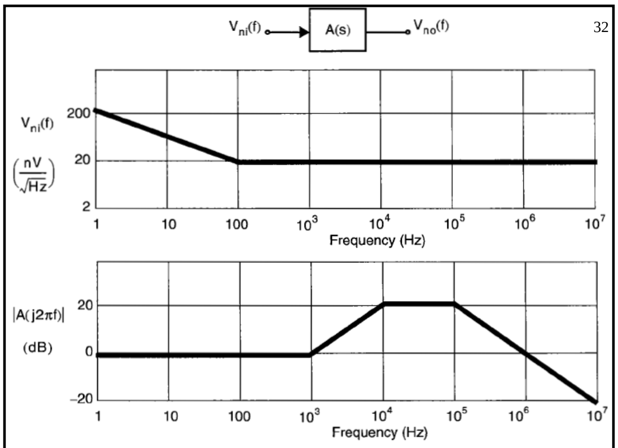
…spectral density

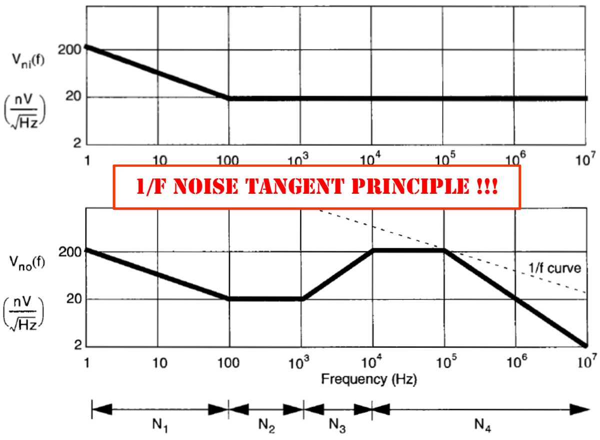


Inherent noise models



Element	Noise Models	$k = 1.38\times 10^{-23}$ J.K^{-1}
Resistor R	R (Noiseless) $V_R^2(f) = 4kTR$	R (Noiseless) $I_R^2(f) = \frac{4kT}{R}$
MOSFET (Active region)	$V_g^2(f)$ $I_d^2(f)$ $V_g^2(f) = \frac{K}{WLC_{ox}f}$ $I_d^2(f) = 4kT\left(\frac{2}{3}\right)g_m$	$V_i^2(f)$ (Noiseless) $V_i^2(f) = 4kT\left(\frac{2}{3}\right)\frac{1}{g_m} + \frac{K}{WLC_{ox}f}$ Simplified model for low and moderate frequencies





1/F NOISE TANGENT PRINCIPLE !!!

$$N_1^2 = \int_1^{100} \frac{200^2}{f}\,df = 200^2 \ln(f)\Big|_1^{100} = 1.84\times 10^5 (\mathrm{nV})^2$$

$$N_2^2 = \int_{100}^{10^3} 20^2\,df = 20^2 f\Big|_{100}^{10^3} = 3.6\times 10^5 (\mathrm{nV})^2$$

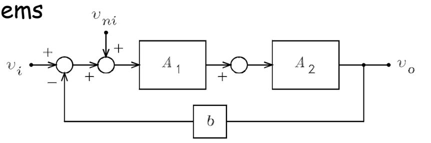
$$N_3^2 = \int_{10^3}^{10^4} \frac{20^2 f^2}{(10^3)^2}\,df = \left(\frac{20}{10^3}\right)^2\left[\frac{1}{3}f^3\Big|_{10^3}^{10^4}\right] = 1.33\times 10^8 (\mathrm{nV})^2$$

$$N_4^2 = \int_{10^4}^{\infty} \frac{200^2}{1+\left(\frac{f}{10^5}\right)^2}\,df = \int_0^{\infty} \frac{200^2}{1+\left(\frac{f}{10^5}\right)^2}\,df - \int_0^{10^4} 200^2\,df$$

$$= 200^2\left(\frac{\pi}{2}\right)10^5 - (200^2)(10^4) = 5.88\times 10^9 (\mathrm{nV})^2$$

Noise considerations

- Basic considerations regarding noise in feedback systems



  - V_{n1} represents the input noise in v_i, the equivalent input noise of A_1 and the output noise of b,
  - V_{ni2} represents the equivalent input noise of A_2

$$v_o = A_2\left[v_{ni2} + A_1\left(v_{ni1} + v_i - bv_o\right)\right] \qquad v_o = \frac{A_1A_2}{1+bA_1A_2}\left(v_i + v_{ni1} + \frac{v_{ni2}}{A_1}\right)$$

$$\boxed{v_{ni} = v_{ni1} + \frac{v_{ni2}}{A_1}}$$

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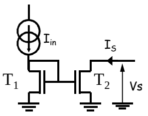
Characterization

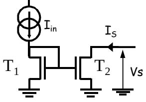


- Makes use of MC simulations
- Define a DOE
- Example : error in a current mirror
  - Set 1 : 100 runs, T_1=T_2
    - Studied influences : V_{eff} (I_{in}), WL, W/L, L
    - Initial design : V_{eff}=0,2V ; W/L=10 ; L=1µm ; V_s =2V

$$I_{in} = I_{dsat1} = \frac{\mu_n C_{ox}}{2}\frac{W}{L}{V_{eff}}^2 = 28\mu A$$

    - MC process : $\sigma(I_{dsat2}) = ?\quad ;\quad mean(I_{dsat2}) = ?$
    - MC process & mismatch : $\sigma(I_{dsat2}) = ?\quad ;\quad mean(I_{dsat2}) = ?$

Characterization



- Effect of V_{eff} → .1V < V_{eff} < 2V

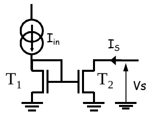
$$I_{in} = \frac{\mu_n C_{ox}}{2}\frac{W}{L}{V_{eff}}^2 > 7\mu A;\ I_{in} = \frac{\mu_n C_{ox}}{2}\frac{W}{L}{V_{eff}}^2 < 2.8mA$$

  - I_{in} = [10µA ; 50µA ; 100µA ; 200µA ; 500µA ; 1mA ; 2mA]
  - MC Process & mismatch : $\sigma(I_{dsat2}) = ?\quad ;\quad mean(I_{dsat2}) = ?$
- Effect of W/L : keep WL and V_{eff} constant

$$WL = 10\mu m^2 \Rightarrow W = \sqrt{\frac{W}{L}.10\mu m^2}\ ;\ \mathrm{L} = \sqrt{\frac{L}{W}.10\mu m^2}\ ;\ \mathrm{I_{in}} = \frac{28\mu A}{10}\frac{W}{L}$$

  - W/L = [.1 ; .2 ; .5 ; 1 ; 2 ; 5 ; 10]

Characterization



- Effect of L : keep WL and V_{eff} constant

$$WL = 10\mu m^2 \Rightarrow W = \frac{10\mu m^2}{L}\ ;\ \mathrm{I_{in}} = \frac{28\mu A}{10}\frac{10\mu m^2}{L^2}$$

  - L = [1 ; 2 ; 5 ; 10 ; 20] → $\sigma(I_{dsat2}) = ?\quad ;\quad mean(I_{dsat2}) = ?$
- Effect of WL : keep W/L and V_{eff} constant

$$W/L = 10 \Rightarrow W = \sqrt{10WL}\ ;\ L = \sqrt{\frac{WL}{10}}\ ;\ \mathrm{I_{in}} = 28\mu A$$

  - WL (µm²) = [7 ; 20 ; 50 ; 100 ; 200 ; 500 ; 1000 ; 2000]

→ $\sigma(I_{dsat2}) = ?\quad ;\quad mean(I_{dsat2}) = ?$

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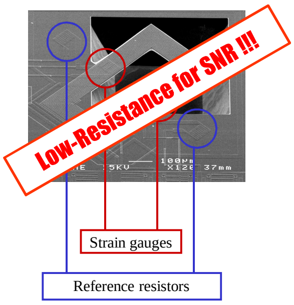
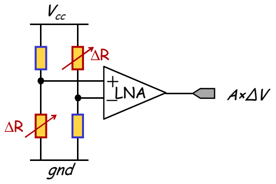
Case study: magnetometer signal conditioning



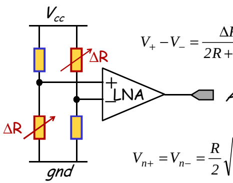


$$I_{TOT} = \frac{V_{CC}}{R} + I_{LNA} > 1mA$$

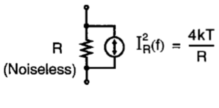
High power consumption

Targeted power consumption : *100µA (for mobile applications) – less for autonomous systems*

Wheatstone bridge SNR



$$V_+ - V_- = \frac{\Delta R}{2R + \Delta R}V_{CC} = \frac{\Delta R}{R}\frac{V_{CC}}{2}\left(\frac{1}{1 + \frac{\Delta R}{2R}}\right) = \frac{\Delta R}{R}\frac{V_{CC}}{2}\left(1 - \frac{\Delta R}{2R}\right) \cong \frac{\Delta R}{R}\frac{V_{CC}}{2}$$



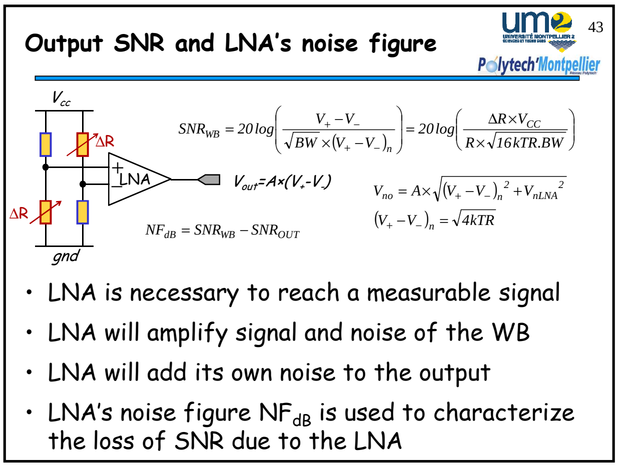
$$I_R^2(f) = \frac{4kT}{R}$$

$$V_{n+} = V_{n-} = \frac{R}{2}\sqrt{2\times\frac{4kT}{R}} = \sqrt{2kTR}$$

$$(V_+ - V_-)_n = \sqrt{{V_{n+}}^2 + {V_{n-}}^2} = \sqrt{4kTR}$$

$$SNR_{WB} = 20\log\left(\frac{V_+ - V_-}{\sqrt{BW}\times(V_+ - V_-)_n}\right) = 20\log\left(\frac{\Delta R\times V_{CC}}{R\times\sqrt{16kTR.BW}}\right)$$

- For a given signal (ΔR/R), SNR_{WB} increases with V_{cc} and reduces with R and BW



Output SNR and LNA’s noise figure

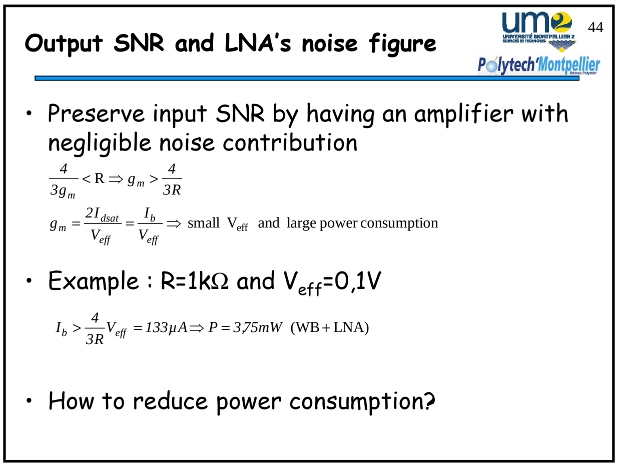
$$SNR_{WB} = 20\log\left(\frac{V_+ - V_-}{\sqrt{BW}\times(V_+ - V_-)_n}\right) = 20\log\left(\frac{\Delta R\times V_{CC}}{R\times\sqrt{16kTR.BW}}\right)$$

$$V_{no} = A\times\sqrt{(V_+ - V_-)_n^{\ 2} + V_{nLNA}^{\ 2}}$$

$$(V_+ - V_-)_n = \sqrt{4kTR}$$

$$NF_{dB} = SNR_{WB} - SNR_{OUT}$$

- LNA is necessary to reach a measurable signal
- LNA will amplify signal and noise of the WB
- LNA will add its own noise to the output
- LNA’s noise figure NF_{dB} is used to characterize the loss of SNR due to the LNA



Output SNR and LNA’s noise figure

- Preserve input SNR by having an amplifier with negligible noise contribution

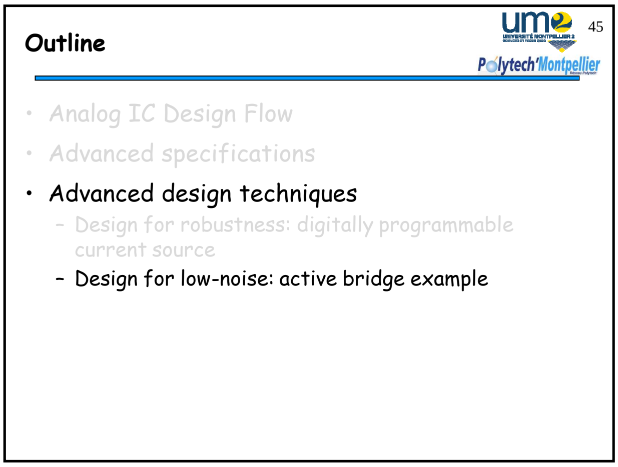
$$\frac{4}{3g_m} < \mathrm{R} \Rightarrow g_m > \frac{4}{3R}$$

$$g_m = \frac{2I_{dsat}}{V_{eff}} = \frac{I_b}{V_{eff}} \Rightarrow \text{small } \mathrm{V_{eff}} \text{ and large power consumption}$$

- Example : R=1kΩ and V_{eff}=0,1V

$$I_b > \frac{4}{3R}V_{eff} = 133\mu A \Rightarrow P = 3{,}75mW \ \ (\mathrm{WB+LNA})$$

- How to reduce power consumption?



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