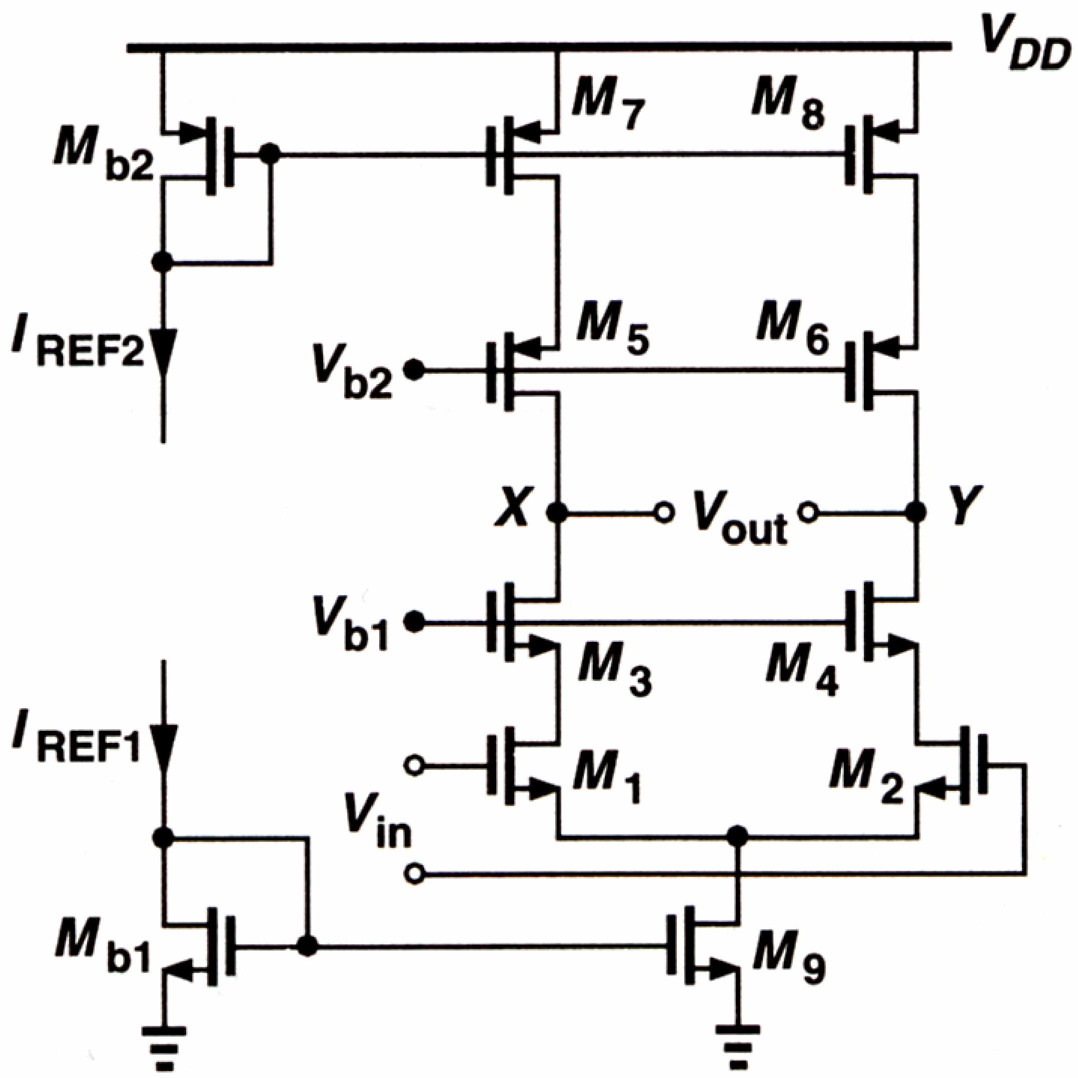
# 4. Design examples

# Design example of telescopic OP amp (1/5)






Spec:

VDD=3V, power=10mW,

Diff output swing=3V,

Voltage gain=2000,

L(eff)=0.5um

$\mu_n C_{ox} = 60\ \mu A/V^2$

$\mu_p C_{ox} = 30\ \mu A/V^2$

$\lambda_n = 0.1\ V^{-1}$

$\lambda_p = 0.2\ V^{-1}$ $\gamma = 0$

$V_{THN} = |V_{THP}| = 0.7\ V.$



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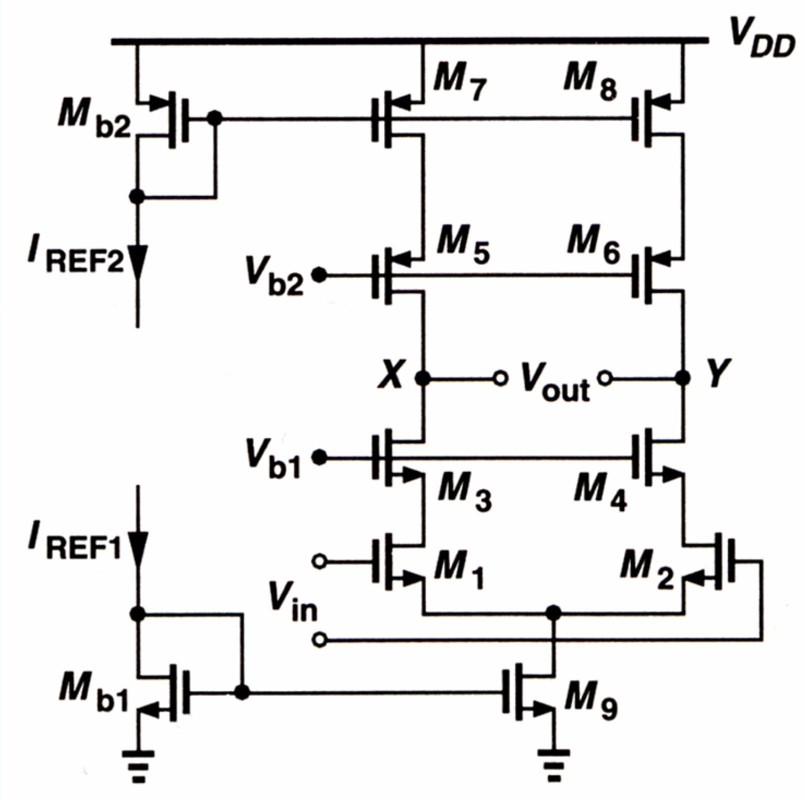
# Design example of telescopic OP amp (2/5)






From
VDD=3V, power=10mW,
➔ I(M9)=3mA
➔ Iref1=Iref2=330uA

From Output swing = 1.5V

$$|V_{OD7}| + |V_{OD5}| + V_{OD3} + V_{OD1} + V_{OD9} = 1.5\ \text{V}.$$

$$V_{OD9} \approx 0.5\ \text{V},\quad V_{OD7} = V_{OD5} = 300mV \quad V_{OD1} = V_{OD3} = 200\ \text{mV}.$$



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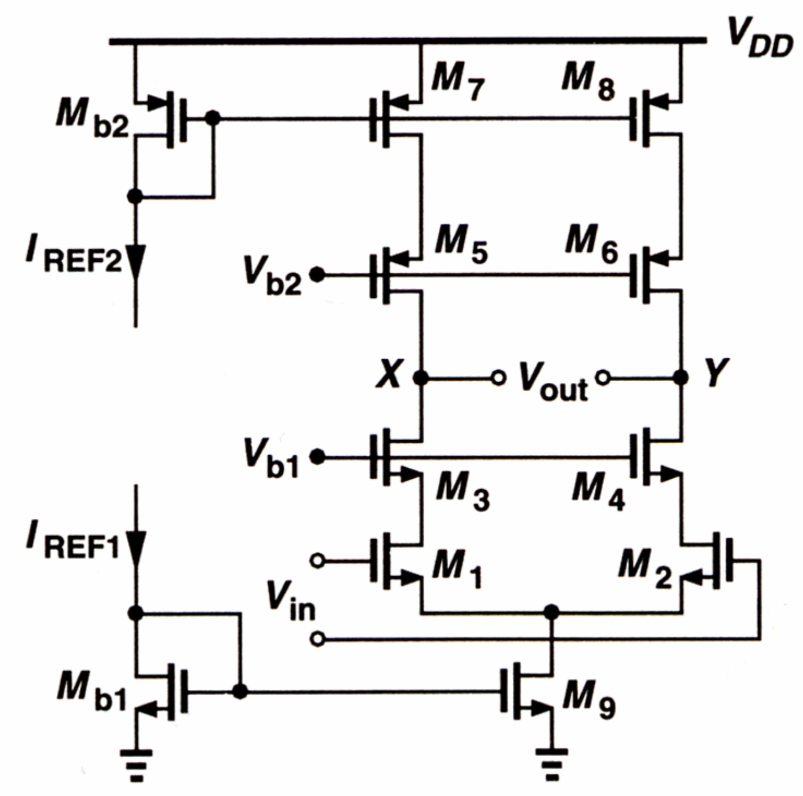
# Design example of telescopic OP amp (3/5)






From
I(M1−M8)=1.5mA
I(M9)=3mA
Iref1=Iref2=330uA

$$I_D = (1/2)\mu C_{ox}(W/L)(V_{GS} - V_{TH})^2$$

$$(W/L)_{1-4} = 1250, (W/L)_{5-8} = 1111, (W/L)_9 = 400.$$

$$A_v \approx g_{m1}[(g_{m3}r_{O3}r_{O1})\|(g_{m5}r_{O5}r_{O7})]$$

$$A_v = 1416,$$



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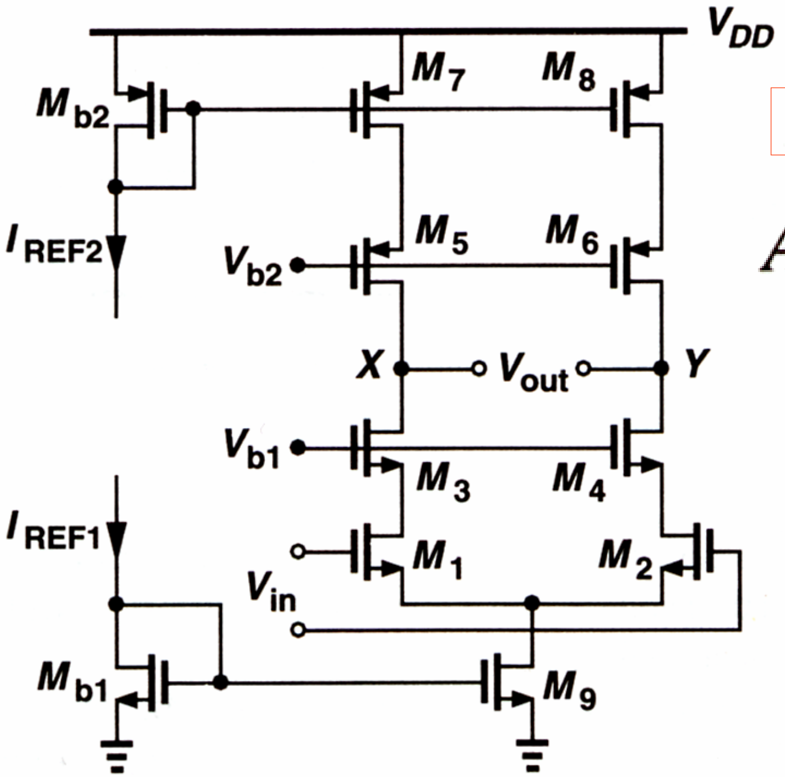
# Design example of telescopic OP amp (4/5)






$(W/L)_{1-4} = 1250, (W/L)_{5-8} = 1111, (W/L)_9 = 400.$

$$A_v \approx g_{m1}[(g_{m3}r_{O3}r_{O1})\|(g_{m5}r_{O5}r_{O7})]$$

$A_v = 1416,$ < 2000 (spec)

$$g_m r_O = \sqrt{2\mu C_{ox}(W/L)I_D}/(\lambda I_D).$$

$\lambda \propto 1/L$ $\quad g_m r_O \propto \sqrt{WL/I_D}.$

M1–M4: signal path ➔ keep min W, L for min cap

$(W/L)_{5-8} = 1111\,\mu m/1.0\,\mu m$ $\quad \lambda_p = 0.1\ V^{-1}$ $\quad A_v \approx 4000$

Vb1 = $V_{GS3} + V_{OD1} + V_{OD9} = 1.6$

Vb2 = $V_{DD} - (|V_{GS5}| + |V_{OD7}|) =$ 1.7V



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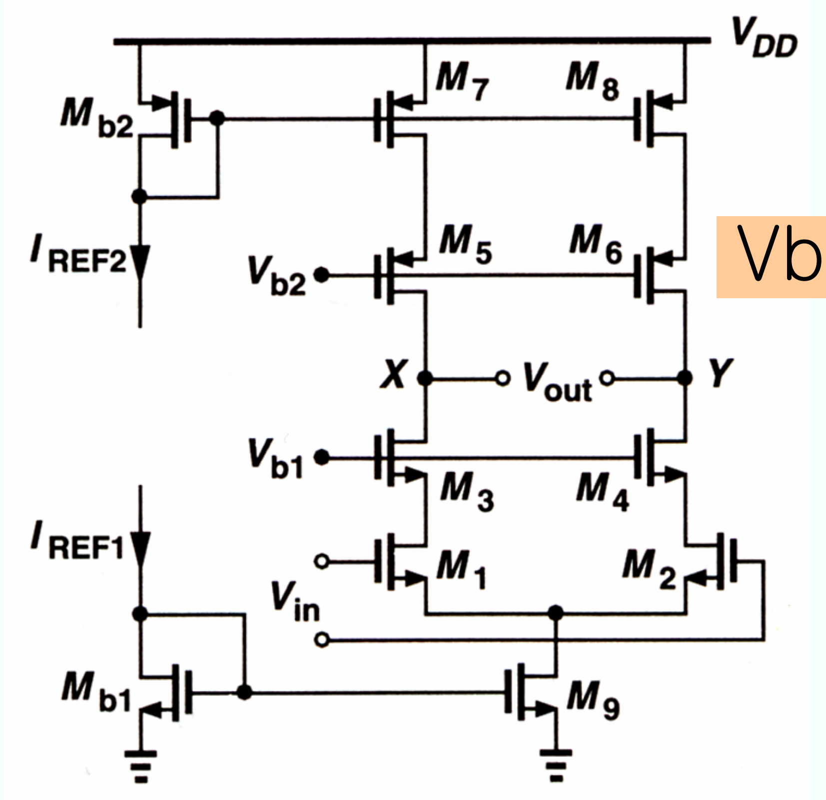
# Design example of telescopic OP amp (5/5)






Vb1 = $V_{GS3} + V_{OD1} + V_{OD9} = 1.6$

Vb2 = $V_{DD} - (|V_{GS5}| + |V_{OD7}|) =$ 1.7V

VX, VY : min=Vb1−VTHn = 0.9V

VX, VY : max=Vb2+|VTHp| = 2.4V

Differential output swing = 2 x (2.4−0.9) = 3V

ICMR limited to a point of 1.4V ➔ not practical



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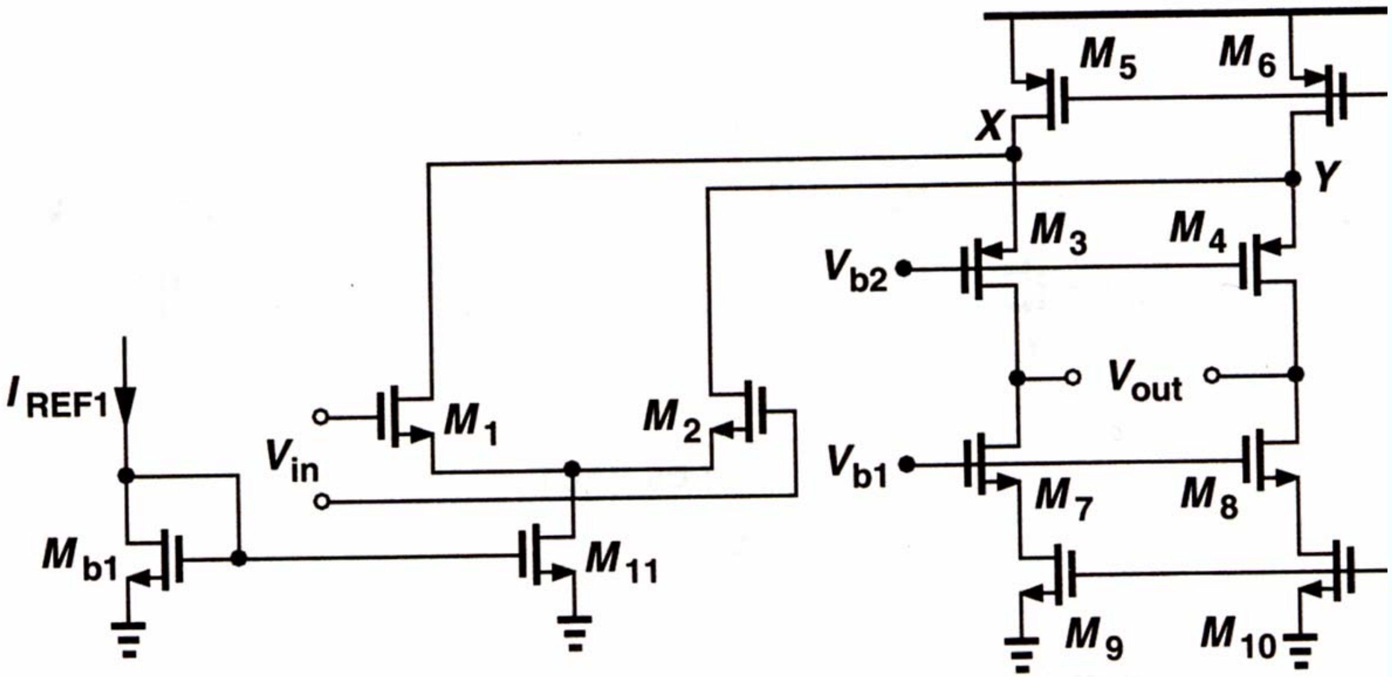
# Design example of folded cascode OP amp (1/5)






Spec:

VDD=3V, power=10mW,

Diff output swing=3V,

Voltage gain=2000,

L(eff)=0.5um

$$\mu_n C_{ox} = 60\ \mu A/V^2$$

$$\mu_p C_{ox} = 30\ \mu A/V^2$$

$$\lambda_n = 0.1\ V^{-1}$$

$$\lambda_p = 0.2\ V^{-1} \qquad \gamma = 0$$

$$V_{THN} = |V_{THP}| = 0.7\ V.$$



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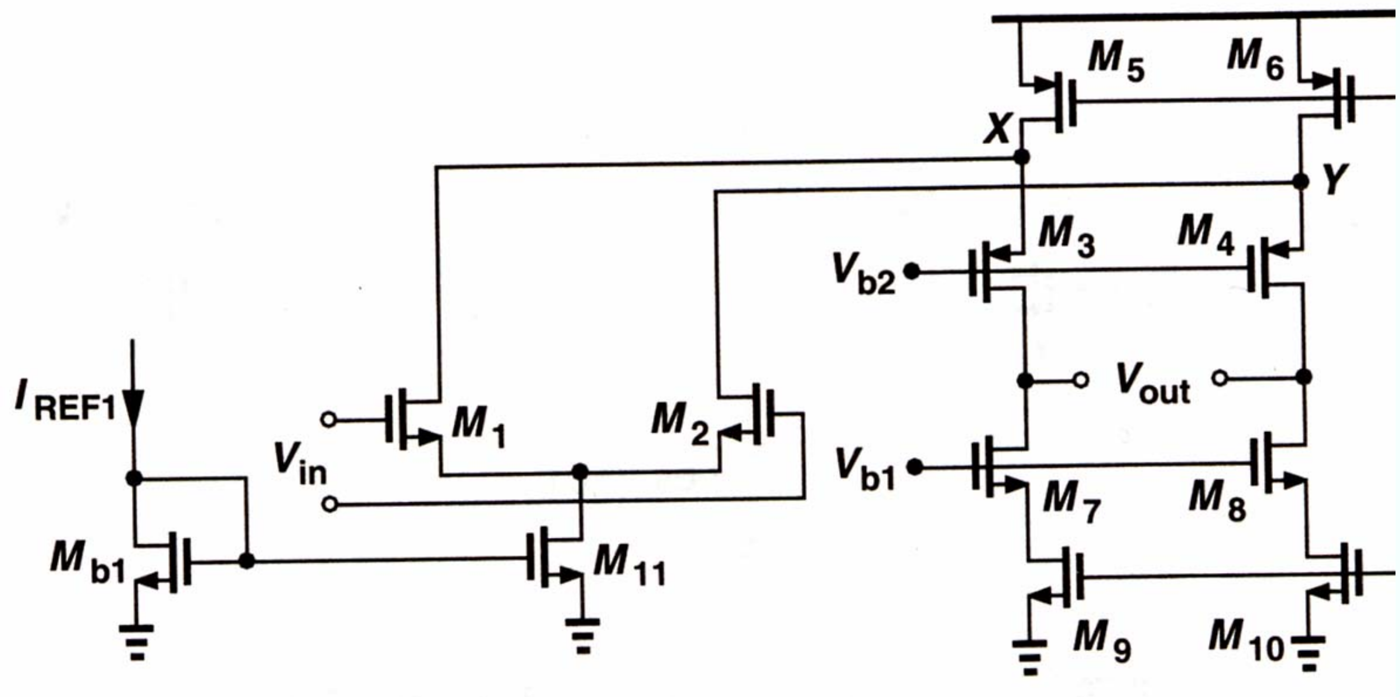
# Design example of folded cascode OP amp (2/5)






Allocate 1.5mA for input diff pair

Allocate 1.5mA for cascode branch

Allocate 0.33mA for current mirrors



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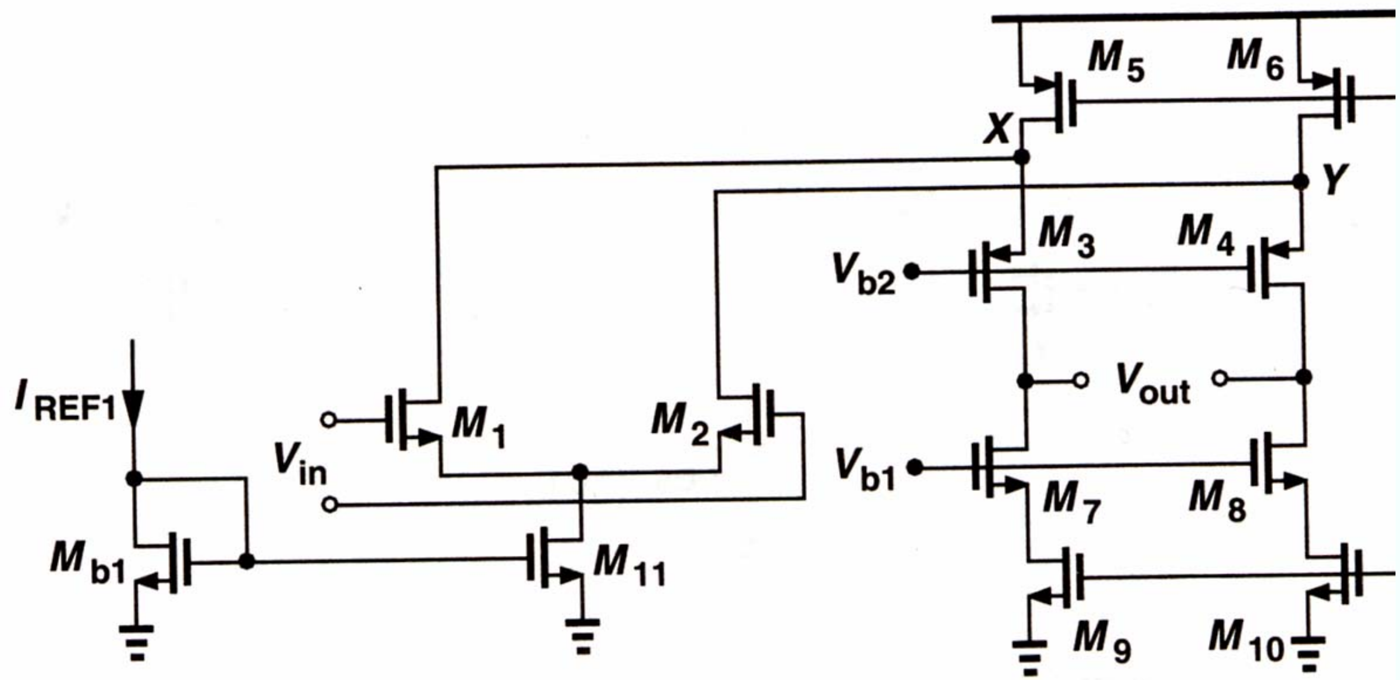
# Design example of folded cascode OP amp (3/5)






VDSAT (M5, M6) = 0.5V

VDSAT (M3, M4) = 0.4V

VDSAT (M7, M8, M9, M10) = 0.3V

➔ VOUT: min0.6V max 2.1V ➔ Diff output swing = 3V

$$(W/L)_{5,6} = 400, (W/L)_{3,4} = 313, (W/L)_{7-10} = 278$$



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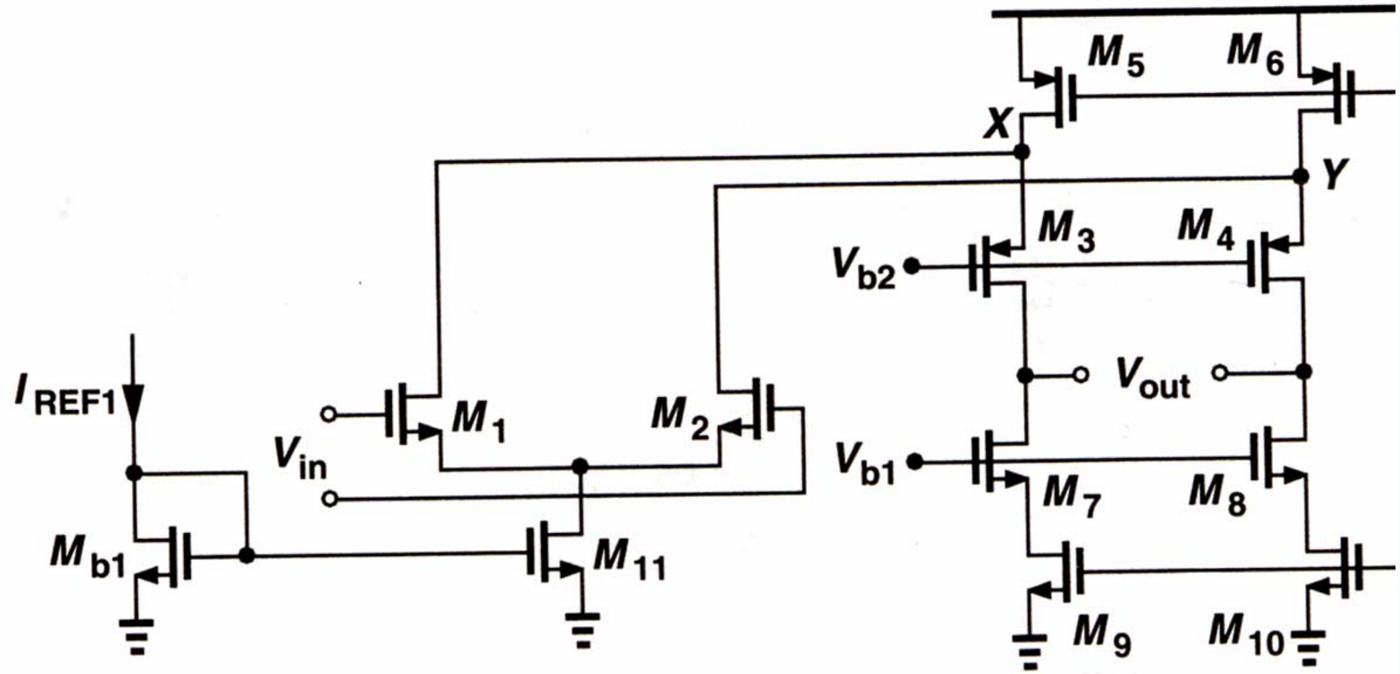
## Design example of folded cascode OP amp (4/5)






VOUT: min 0.6V max 2.1V

➔ Optimum output common mode level =1.35V

minimum dimensions of $M_1$-$M_2$

$$V_{GS2} + V_{OD11} = 1.35\ \text{V}. \quad V_{OD11} = 0.4\ \text{V}$$

$$V_{OD1,2} = 0.95 - 0.7 = 0.25\ \text{V} \quad (W/L)_{1,2} = 400$$



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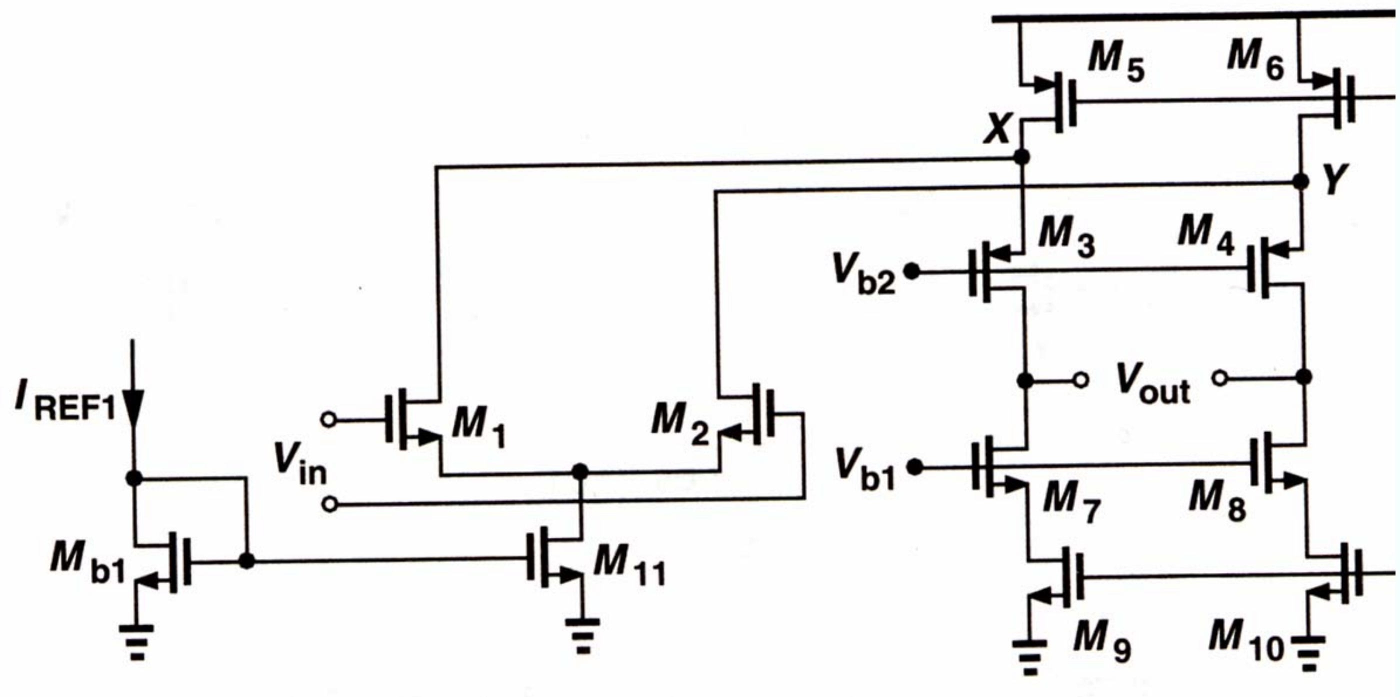
# Design example of folded cascode OP amp (5/5)






Gain = 400

To increase gain

(1) Increase W and L of M5, M6 (not in the signal path)

(2) increase both W and L of M3, M4

(3) Increase W of M1, M2



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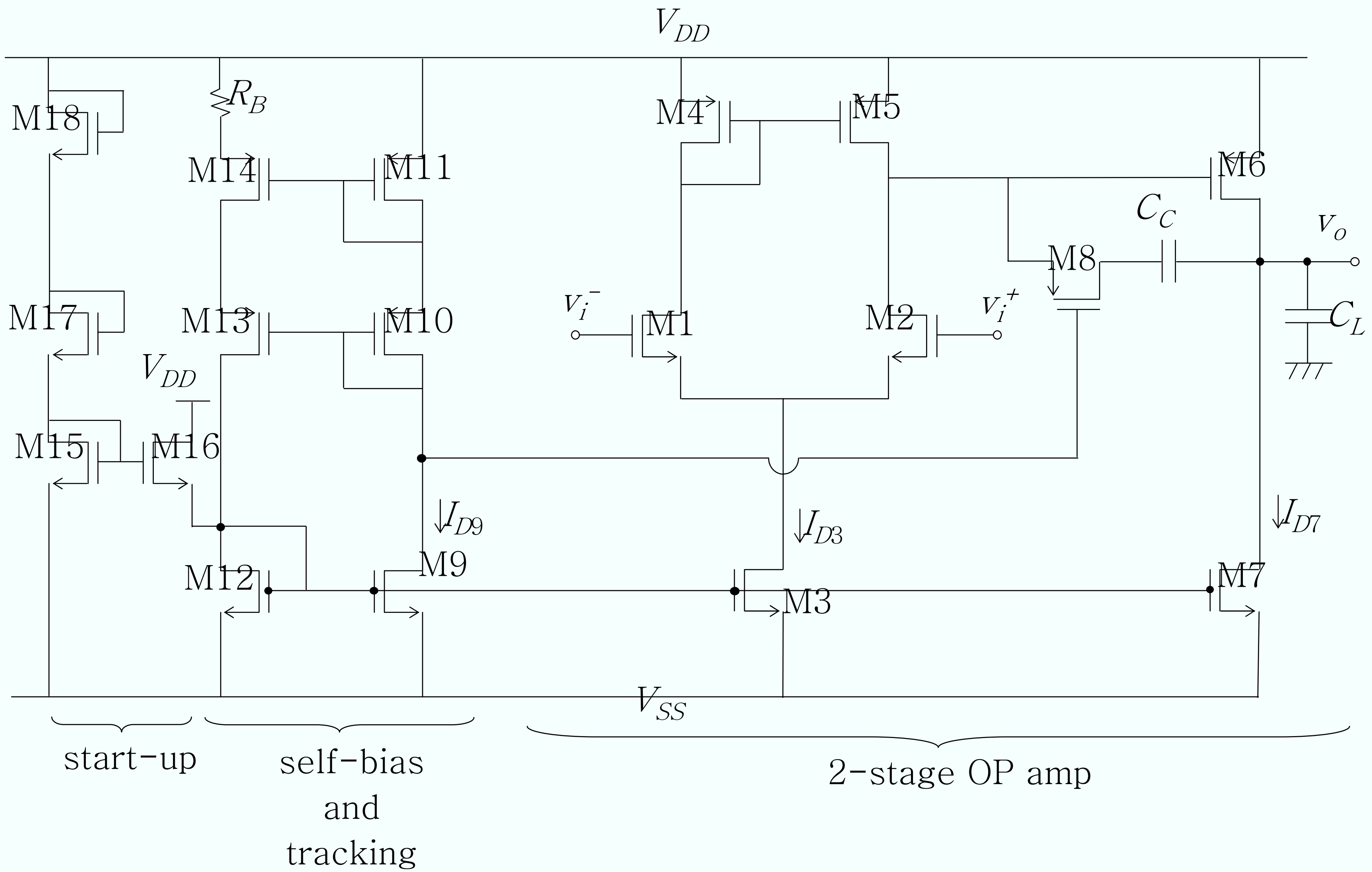
# 2-stage OP amp (design example)






**Tracking compensation ➔ bias independent Rz**

# 2-stage OP amp (Spec)



| Items | Specification |
|---|---|
| Supply voltage | $V_{DD} = 2.5V$ $V_{SS} = -2.5V$ |
| DC small signal voltage gain | > 3000 |
| Power consumption | $2mW$ |
| Load capacitance | $20pF$ |
| slew rate *SR* | $80\,V/\mu s$ |
| active input common mode voltage range (*CMR*) | $CMR_{min}$: $-1.2V$<br>$CMR_{max}$: $2.0V$ |
| gain-bandwidth product $\omega_T$ | $100MHz$ |
| Linear output voltage range (*OVR*) | $OVR_{min}$: $-2.0V$<br>$OVR_{max}$: $+2.0V$ |
| Low freq input equ. thermal noise voltage spectrum $v_{ieqn,th}$ | $10nV/\sqrt{Hz}$ |

## Some useful equations

**Target** $p_2 = z_1$ ➔ $R_z = \frac{1}{g_{m6}} \cdot \left(1 + \frac{C_L}{C_C}\right)$ ➔ **2-pole amp (p1,p3)**

**Target : phase margin > 60 deg** $PM = 180 - 90 - \tan^{-1}(\frac{\omega_T}{p_3})$

$$|p_3| > \frac{\omega_T}{\tan(30^\circ)} = \sqrt{3} \cdot \omega_T \qquad \frac{g_{m4}}{C_4} > \sqrt{3} \cdot \omega_T \qquad \omega_T = \frac{g_{m1}}{C_c}$$

$$P_D = (I_{D3} + I_{D7}) \cdot (V_{DD} - V_{SS})$$

$$A_{dv}(0) = g_{m1} \cdot (r_{o2} \| r_{o5}) \cdot g_{m6} \cdot (r_{o6} \| r_{o7})$$

$$A_{dv}(0) = 2 \cdot \sqrt{2} \cdot \sqrt{\mu_n \mu_p} \cdot C_{ox} \cdot \frac{1}{(\lambda_n + \lambda_p)^2} \cdot \sqrt{\frac{\left(\frac{W}{L}\right)_1 \cdot \left(\frac{W}{L}\right)_6}{I_{D3} \cdot I_{D7}}}$$

## Design steps

$$I_{D3} = I_{D7} = 0.5 \times \frac{2mW}{5} = 200\mu A$$

**Default channel length > min channel length**

**Input CMRmin, CMRmax → VDSAT3+VDSAT1 <= 0.5V, VDSAT4 <= 0.5V**

**OVRmin, OVRmax → VDSA6 <= 0.5V, VDSAT7 <= 0.5V**

**Decide all VDSATs → all W, L's**

**Calculate gain → adjust W, L's to meet gain spec.**

**Iterations to meet SR, $\omega_T$, PM spec.**

# Term project 1



(1) Choose an OP amp circuit

(2) Design by hand analysis with iterations

(3) Use SPICE to satisfy the target

(4) Fill in the spec Table

(5) Design a self bias circuit (using R)

(6) Due Nov 21st, submit by e-mail hjpark@postech.edu

(7) Use model parameters of HW1, VDD=3.3V CL=10pF

(8) Target

DC voltage gain >= 1000, OVR >= 1V,

GBW >= 100MHz, PM > $60^o$ with unity gain FB.

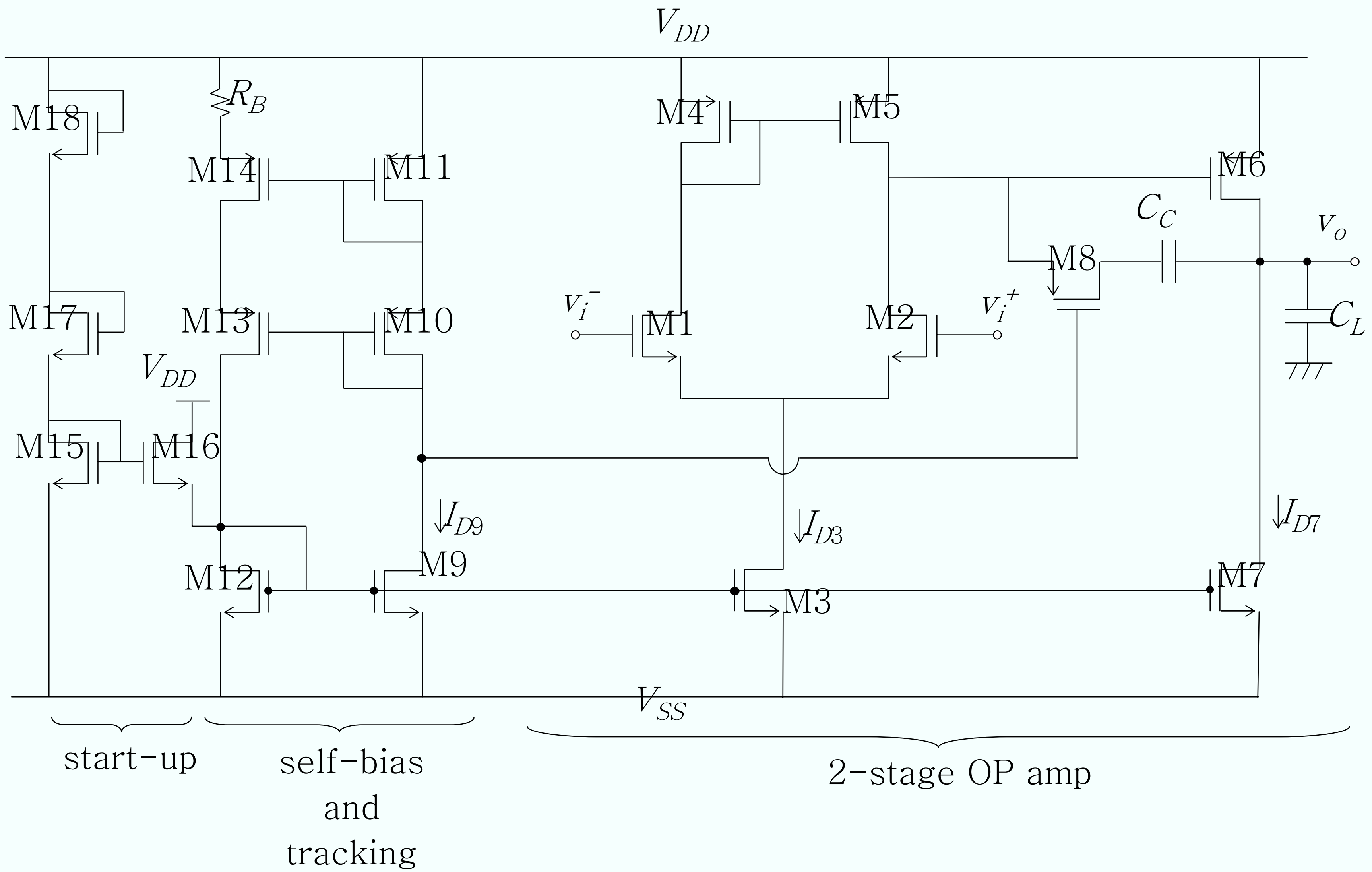
# Spec Table



| Items | Specification |
|---|---|
| Sum (Wi x Li) | |
| DC small signal voltage gain | |
| Power consumption (including bias circuit) | OP amp:<br>Bias circuit: |
| slew rate *SR* | |
| 0.1% settling time with unity gain feedback( 0.1V step) | |
| active input common mode voltage range (*ICMR*) | |
| gain-bandwidth product | |
| Linear output voltage range (*OVR*) | |
| Low freq input equ. thermal noise voltage spectrum | |

# Example OP amp circuit for Term Project 1: An

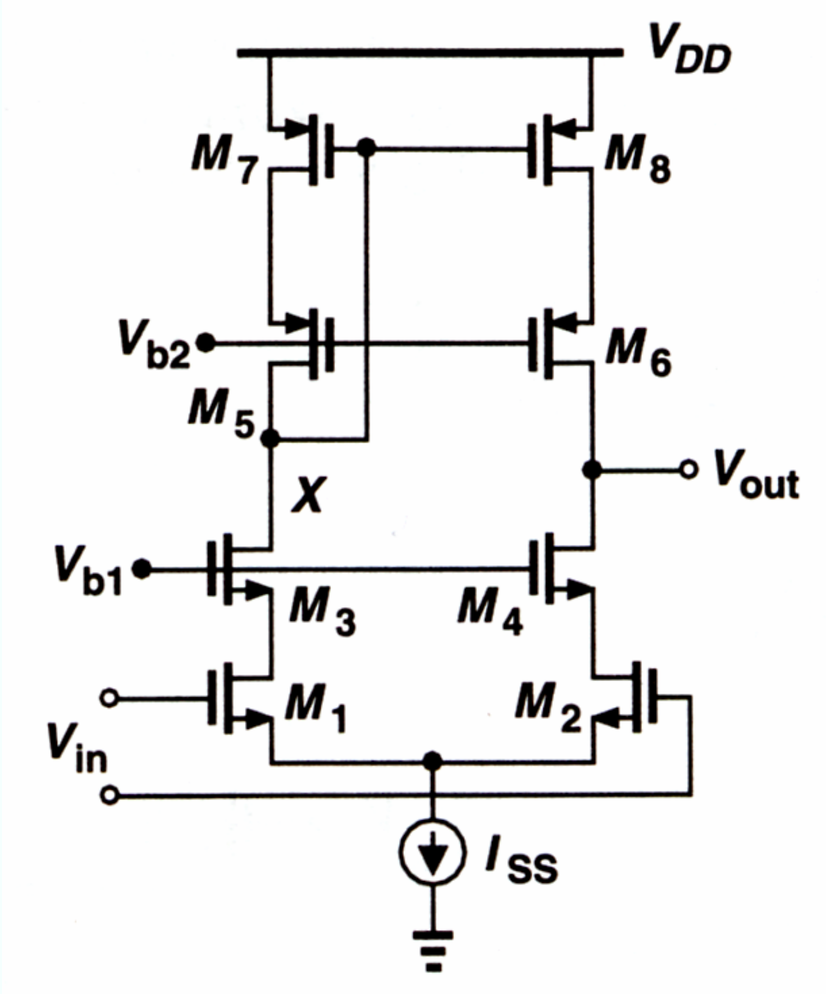





**Ap : PMOS input version of this circuit**

# Example OP amp circuit for Term Project 1: Bn

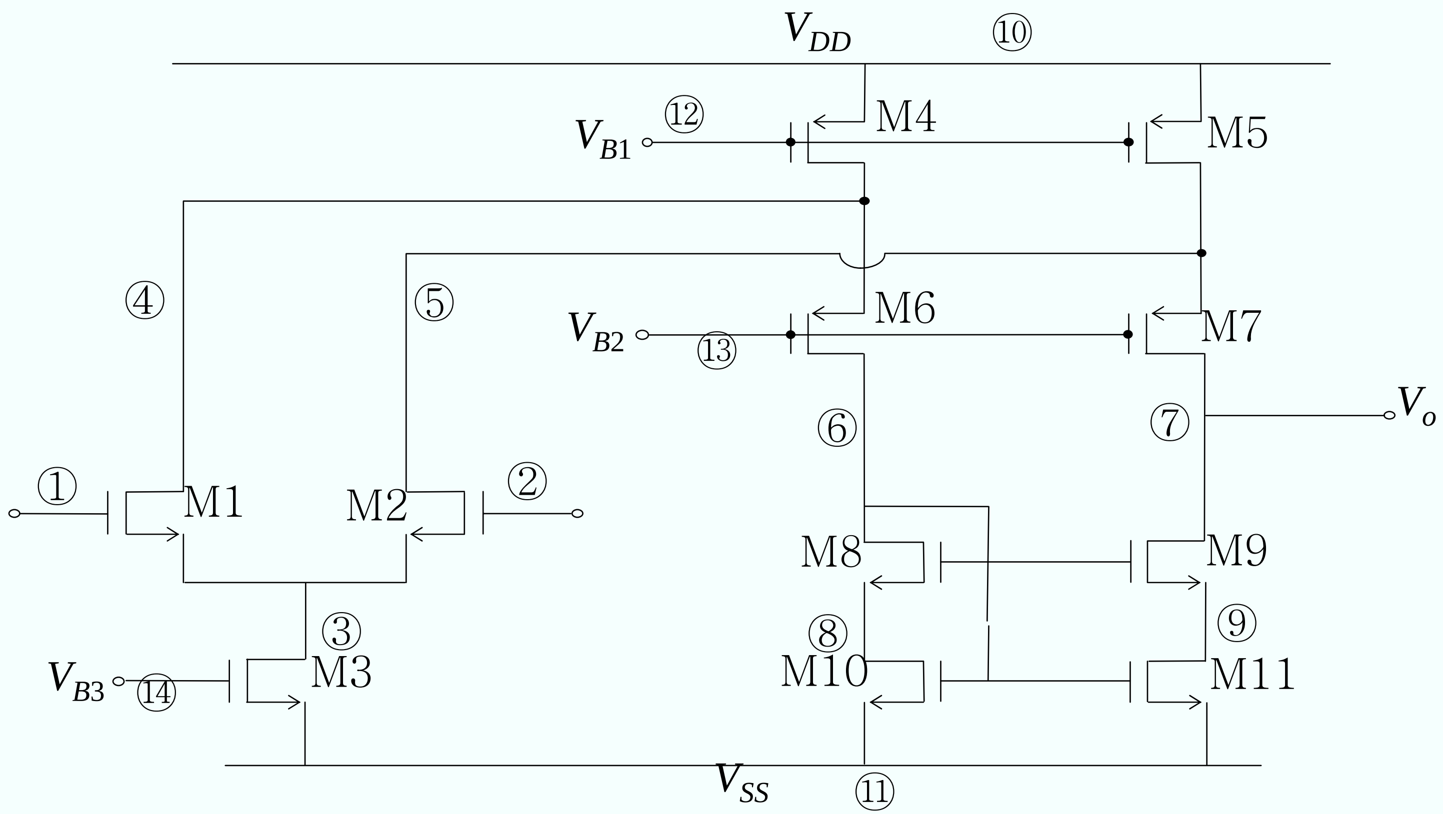





**Bp : PMOS input version of this circuit**

# Example OP amp circuit for Term Project 1: Cn

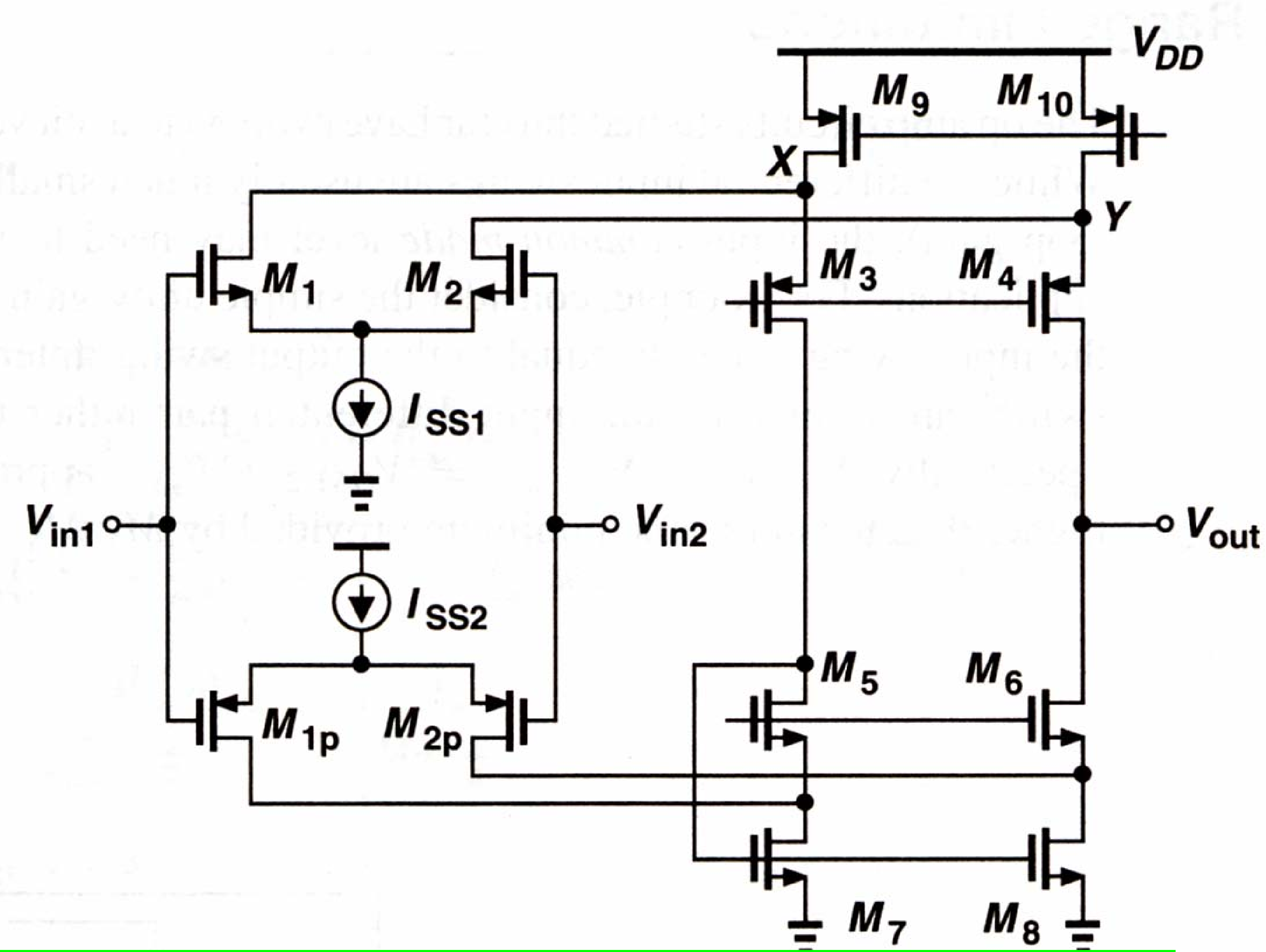





**Cp : PMOS input version of this circuit**

# Example OP amp circuit for Term Project1:Dn

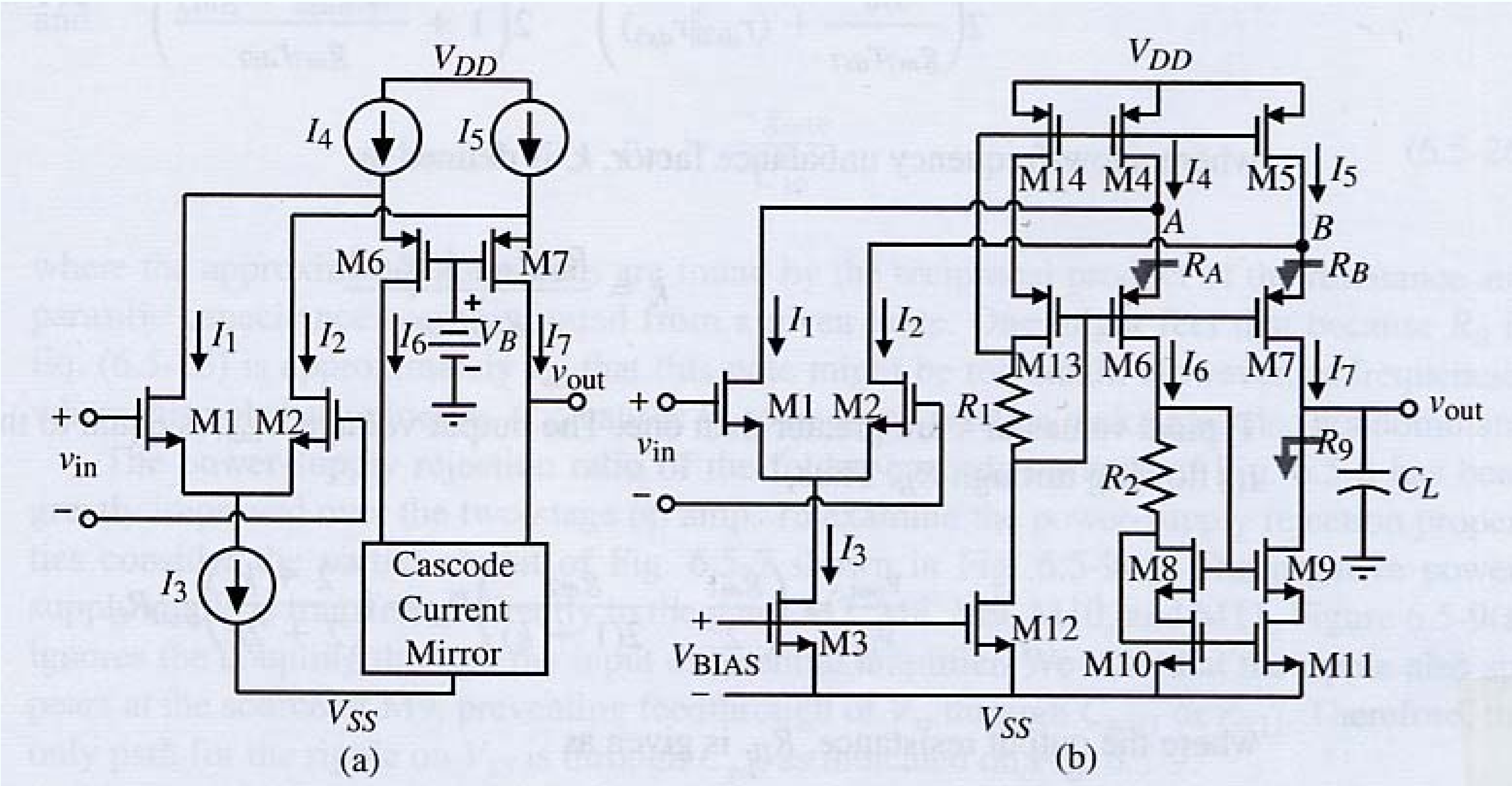





**Dp : PMOS side high-swing cascode version of this circuit**

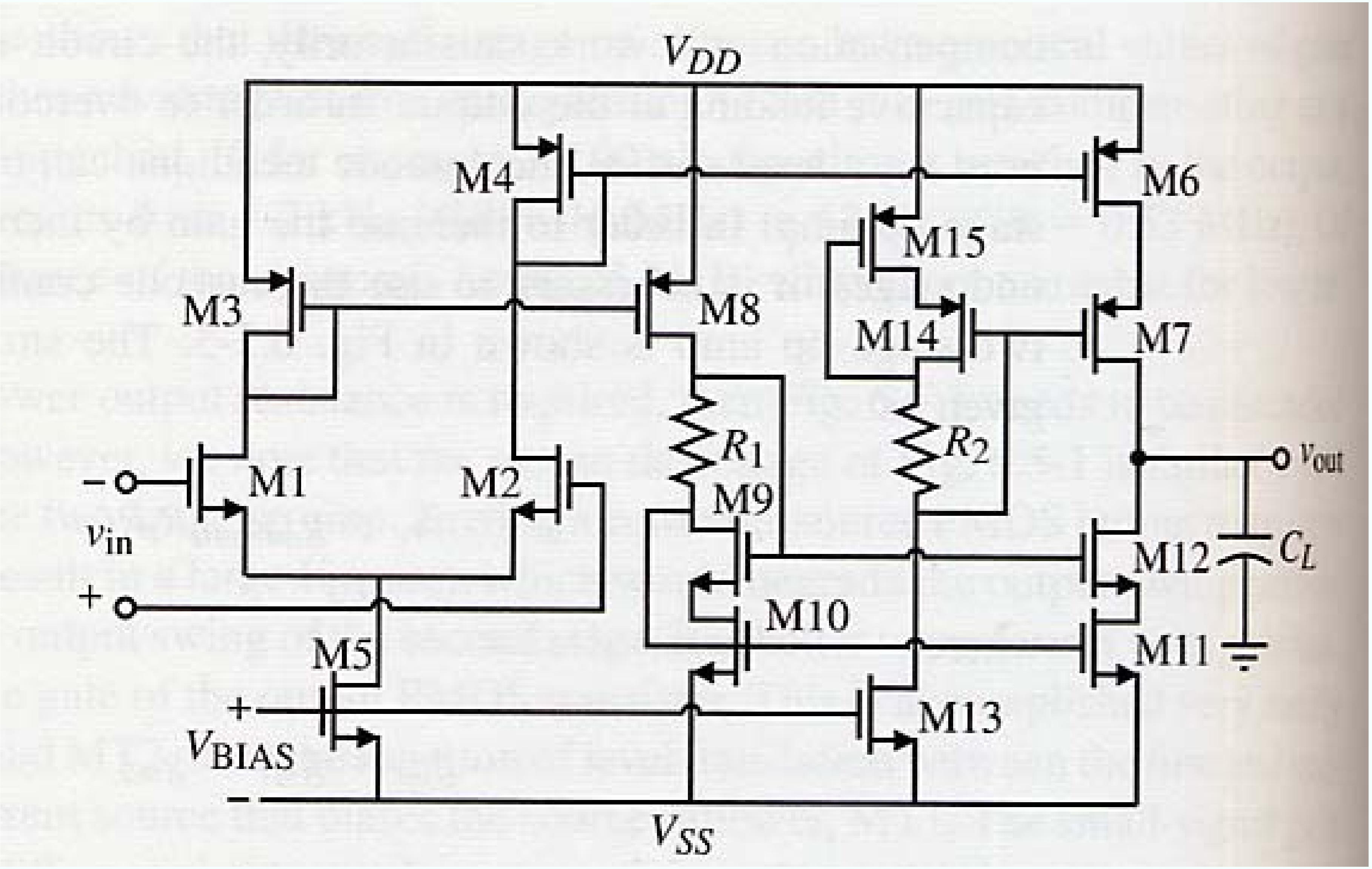
# Example OP amp circuit for Term Project1:Fn





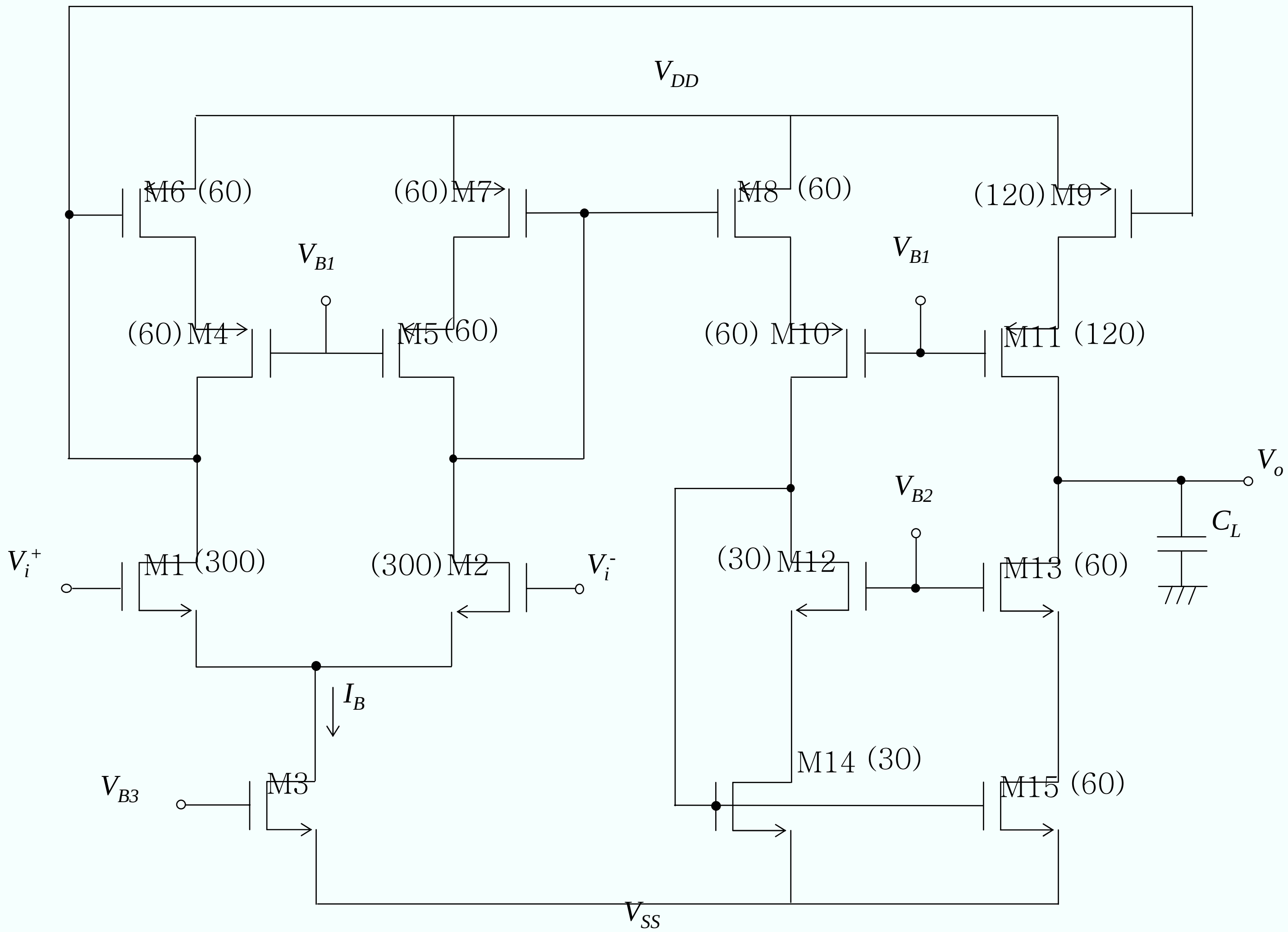
# Example OP amp circuit for Term Project1:Gn





# Example OP amp circuit for Term Project1:Hn

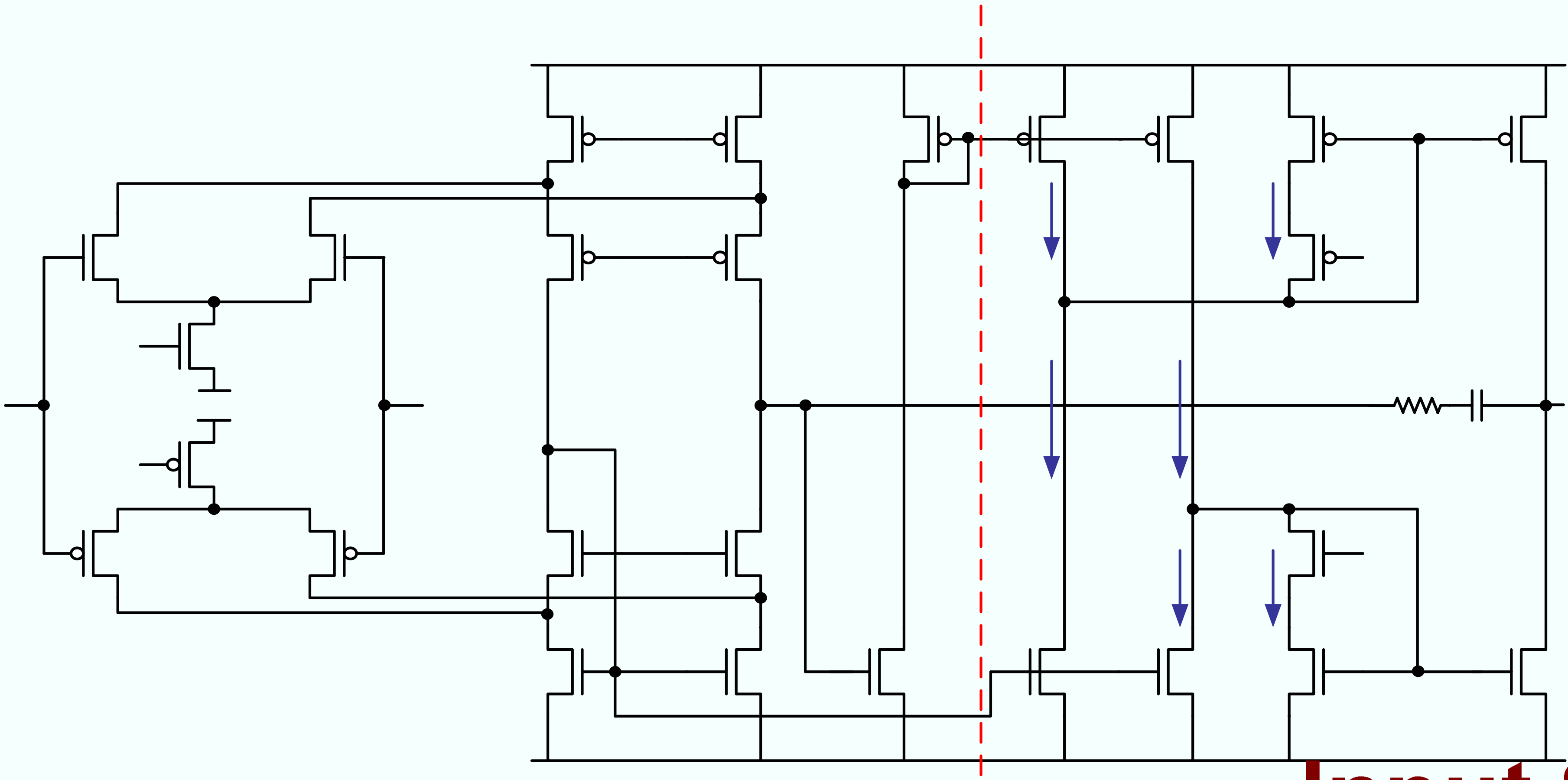





## Hp : PMOS input version of this circuit

# Example OP amp circuit for Term Project 1: I

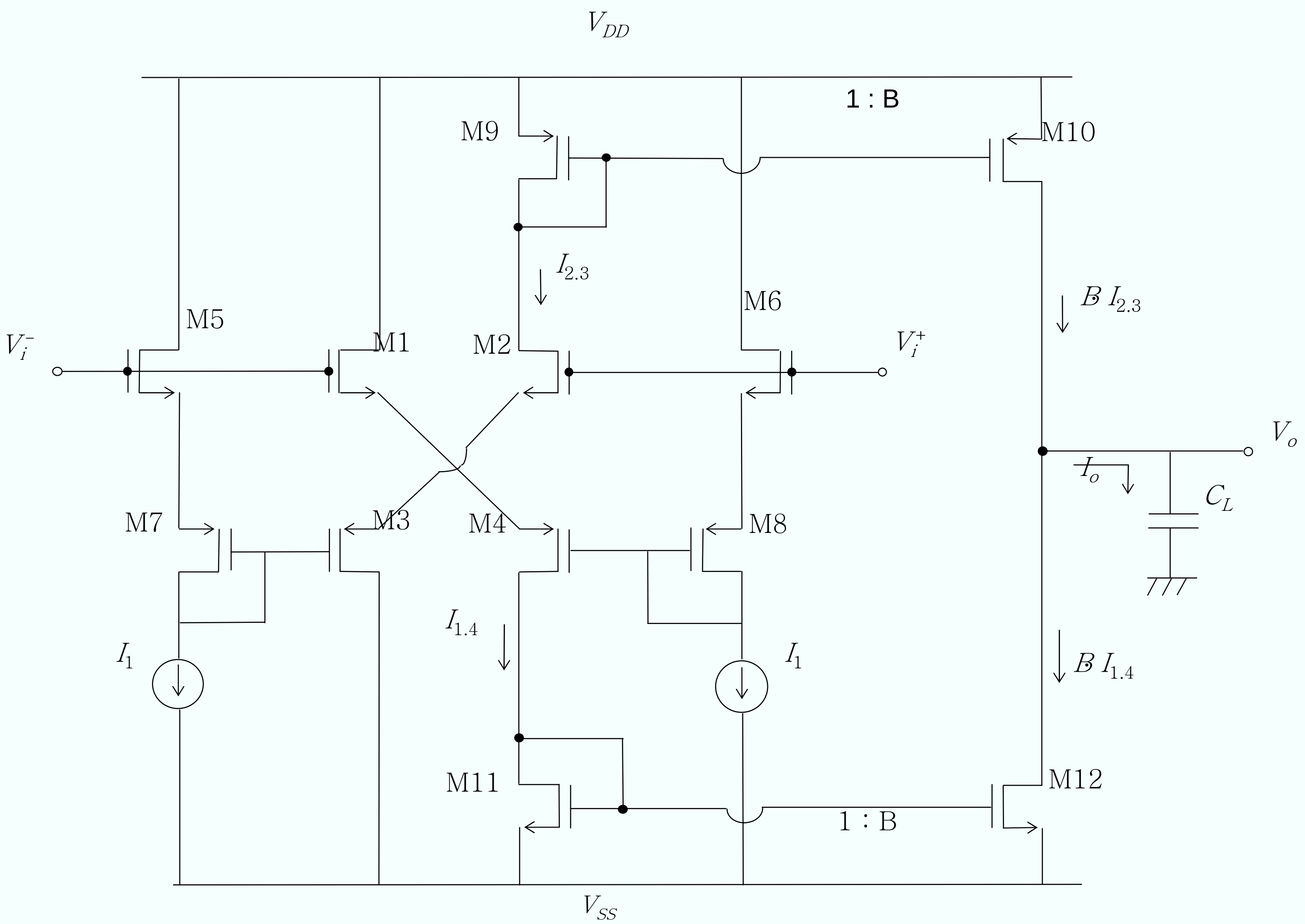




**Input Stag**

# Example OP amp circuit for Term Project 1: J

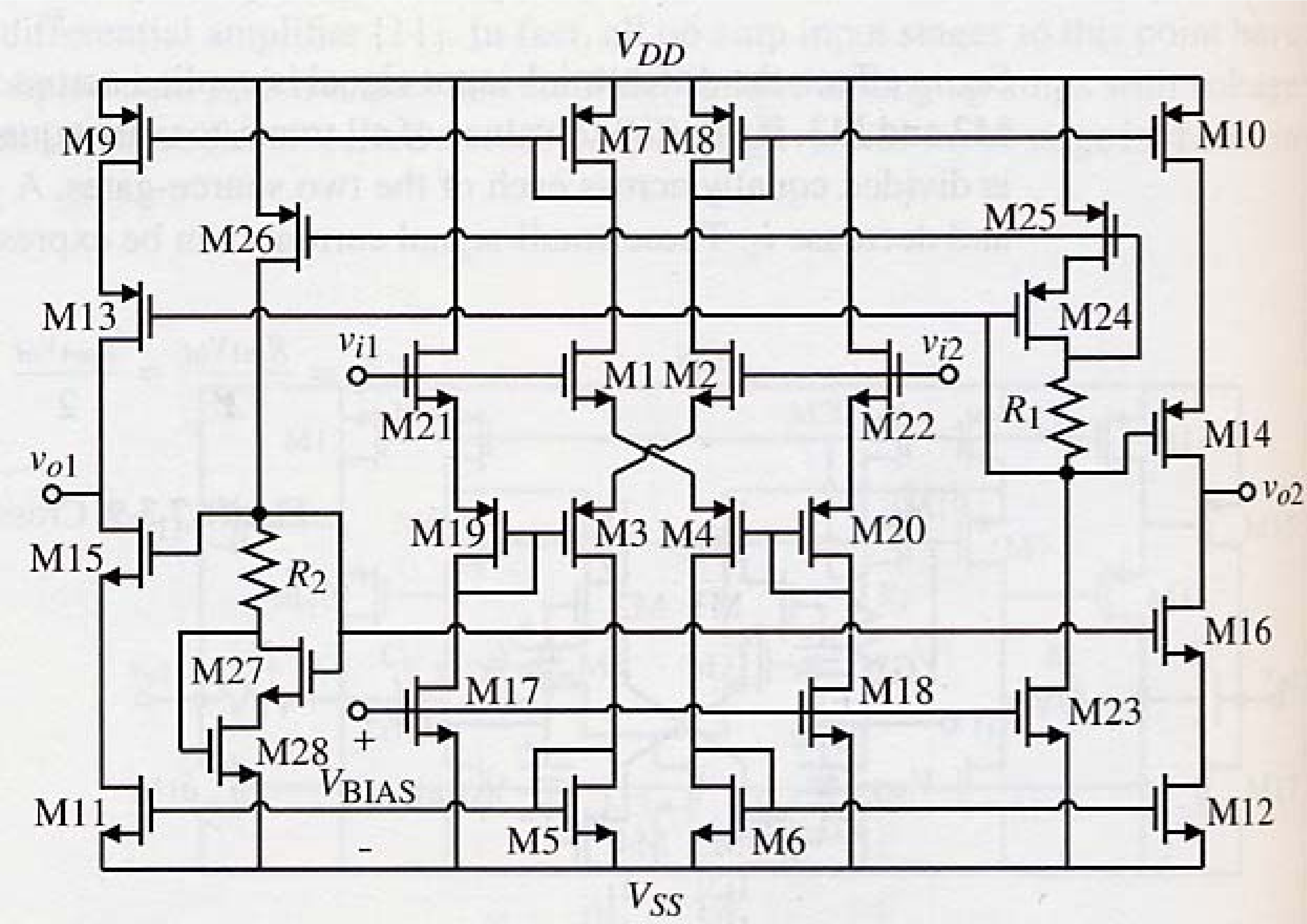





**Replace M10 & M12 by cascode output stages**

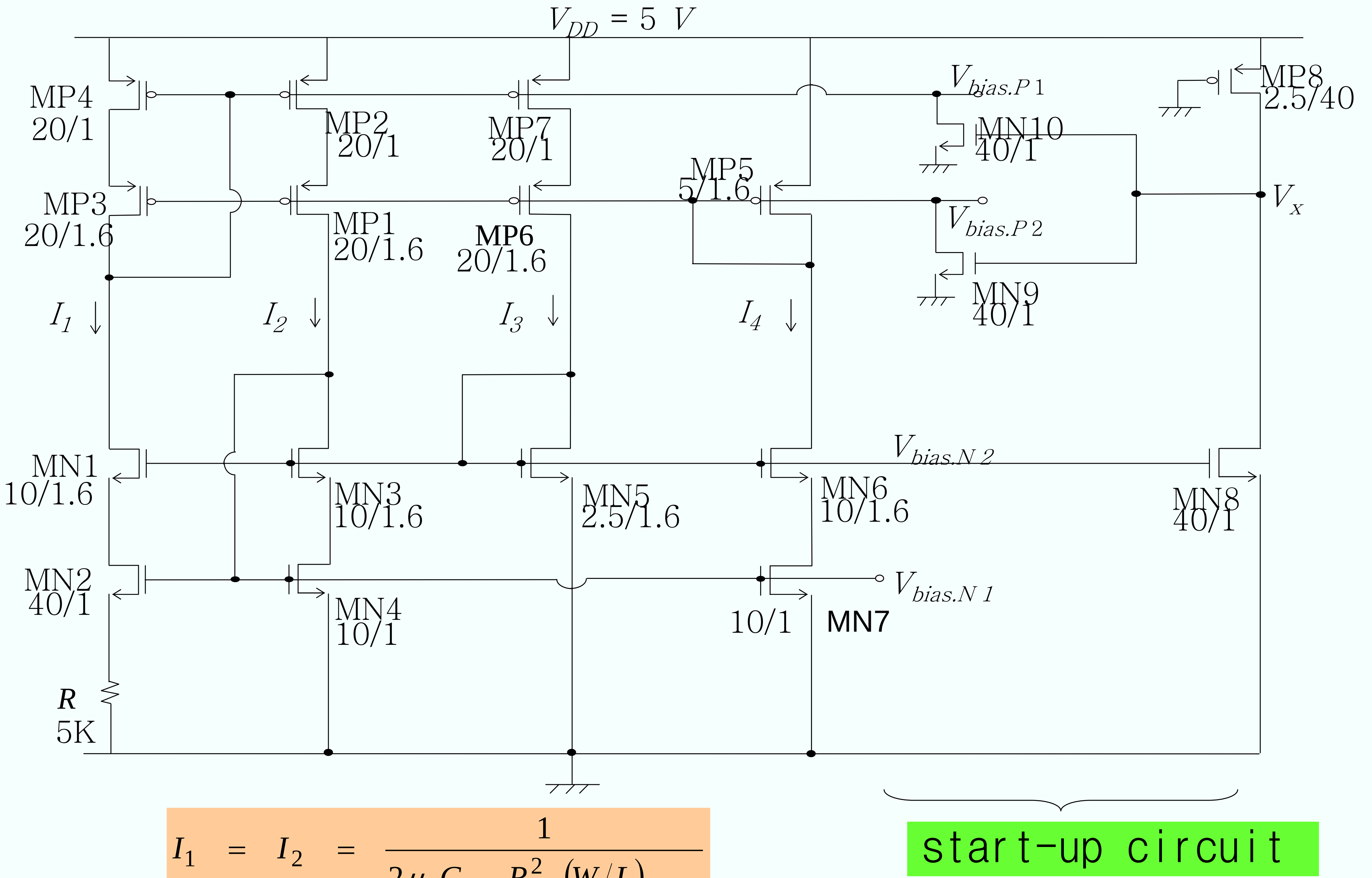
# Example OP amp circuit for Term Project1:En





# Example bias circuit for Term Project 1






$$I_1 = I_2 = \frac{1}{2\mu_n C_{ox} \cdot R^2 \cdot (W/L)_{MN4}}$$