POWER MANAGEMENT INTEGRATED CIRCUITS
DESIGN, FUNCTIONALITY ANALYSIS
AND APPLICATIONS

by

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ABSTRACT

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AND APPLICATIONS

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Power management is playing a significant role in modern electronics. Good power management is especially important for portable devices that rely on batteries. By smartly managing how the power is directed to different components of a system, e.g., reducing power to components that are not being used, the efficiency as well as the battery lifetime can be doubled or tripled.

There exists a large family of integrated circuits (IC) that are used for power management, e.g., linear regulators, switching regulators, power controllers, hot swap controllers, etc. The voltage reference is one of the key components in this family.

For high precision, the drift of a reference voltage needs to be minimized. This is especially true for the drift caused by temperature variation. This drift can be reduced by means of compensation. High performance of compensation is achieved through curvature correction. A novel approach for curvature compensation is proposed in this work. It is suitable for extra-low-voltage operation with micro power dissipation.

The overall performance of reference circuits are characterized by current efficiency, line regulation, load regulation, power supply rejection ratio, and noise in addition to temperature drift. To take into consideration all of these in a functionality analysis, a strategy is developed based on the General Systems Performance Theory. In this strategy, each aspect of performance is evaluated based on the fact how well this aspect of performance satisfies the predetermined task demands. Then all these individual evaluation results are combined to represent the overall performance.

The line regulations performance in the designed reference circuits are improved by introducing a linear voltage regulator. The error amplifier is one of the critical elements in the linear regulator. It needs to have high current driving capability as well as high efficiency. Thus error amplifiers are designed with class AB output stages. Finally the noisy raw supply voltages go through the designed linear regulator before being fed to the reference circuits, and the line regulation performance is enhanced dramatically. Also the linear regulator is applied to a variable gain amplifier to reduce the dependence of gain on power supply voltage.

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CHAPTER 1

INTRODUCTION

Power supplies are the most fundamental and indispensable component found in any integrated circuits. They need to be stable, constant and accurate to ensure the proper operation of analog, digital or mixed-signal circuits. Such voltages are converted by the power management circuits from raw supplies like batteries, generators, and other AC or DC sources, which are typically noisy and fluctuating. Power management circuits convert, regulate and control the power.

Nowadays the rapid development of mobile technology allows people to work anywhere at anytime. The portable devices, such as the cellular phone, laptop, PDA, free people from the desk. Most of these devices are powered by batteries. To maximally extend the lifetime of batteries, low-voltage power-efficient power management circuits are in high demand. Among the power management circuits, the reference circuit is one of the most critical components. For example, a voltage reference plays a significant part in the linear regulator to define the regulated output voltage. In fact, reference circuits have much in common with regulators. Functionally the latter can be described as reference circuits, but with greater current (or power) output capability. Thus these two types of circuits have almost the same specifications, like the line regulation, load regulation, efficiency, etc. Nevertheless the performance of

reference circuits is generally tighter with regard to the accuracy and drift. The drift may be caused by the temperature and aging effect. Sometimes it is even a bigger problem than the accuracy, since the initial error can always be trimmed, but compensating for the drift is difficult. For this reason, the development of compensation strategies for reference circuits suitable for low-voltage applications is the primary concentration of this work. This chapter will first discuss the fundamentals of temperature compensation for reference circuits.

1.1 Temperature Dependence

1.1.1 Temperature Coefficient

One of the most critical aspects of the performance of reference circuits is their temperature dependence. The temperature drift can be expressed in terms of the fractional change in output per degree centigrade of temperature variation, which is defined as fractional temperature coefficient TC_F [1]:

$$TC_F = \frac{1}{Y_{OUT}} \frac{\partial Y_{OUT}}{\partial T} \tag{1.1}$$

where Y_{OUT} may represent either output current or output voltage.

A key parameter of interest in the reference circuits is the variation of the output that occurs over a certain temperature range. Since the fractional temperature coefficient depicts the temperature sensitivity only at single temperature point, the effective temperature coefficient is generally used to characterize the behavior of the circuit over a broad range of temperature:

$$TC_{F(EFF)} = \frac{1}{Y_{NOM}} \left(\frac{Y_{MAX} - Y_{MIN}}{T_{MAX} - T_{MIN}} \right) \tag{1.2}$$

where Y_{MAX} and Y_{MIN} are the largest and smallest outputs observed over the temperature range of interest, $T_{MAX} - T_{MIN}$ is the temperature excursion, and Y_{NOM} is the nominal or mean output.

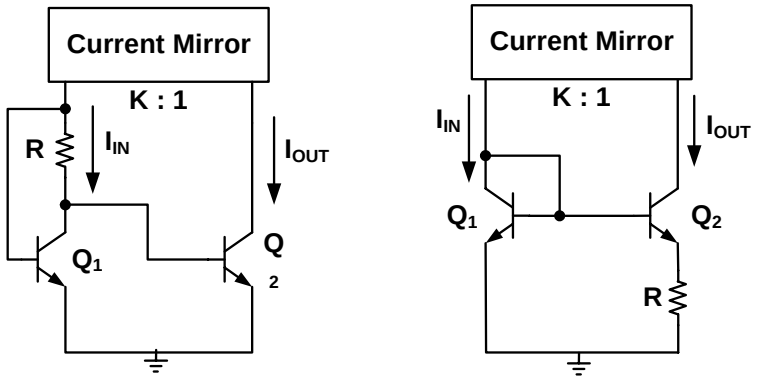
Nevertheless the definition of $TC_{F(EFF)}$ has limitations, especially when it describes the nonlinear variation common in a compensated reference circuit. In that case, one circuit may exhibit different $TC_{F(EFF)}$ if a different temperature range is of interest [1]. Thus the $TC_{F(EFF)}$ cannot uniquely determine the temperature characteristics of a compensated circuit if the temperature range is not fixed. And it is not justifiable to compare the $TC_{F(EFF)}$ of several circuits obtained in different temperature range. For this reason, the temperature range must be fixed to compare the temperature characteristics, typically from -55°*C* to 125°*C*. This range is used for all the simulations in this work.

1.1.2 PTAT And I-PTAT

Basically all the circuits can be classified into proportional-to-absolute-temperature (PTAT) and inversely-proportional-to-absolute-temperature (I-PTAT) in terms of the temperature coefficients of their outputs. I-PTAT is also referred as conversely-proportional-to-absolute-temperature (CTAT). The output of PTAT circuits has $TC_F > 0$, i.e., the output current or voltage increases monotonically with the increase of temperature. On the contrary, the output of I-PTAT circuits has $TC_F < 0$,

i.e., the output current or voltage decreases monotonically with the increase of temperature.

Usually the temperature compensation is accomplished through appropriate combinations of the outputs of PTAT and I-PTAT circuit cells. Next four PTAT and I-PTAT circuit cells, which are seen frequently in most reference circuits, will be summarized. The temperature dependence will be characterized by their output current.



(a) (b)

Figure 1.1 PTAT circuits (a) peaking current source, (b) Widlar current source.

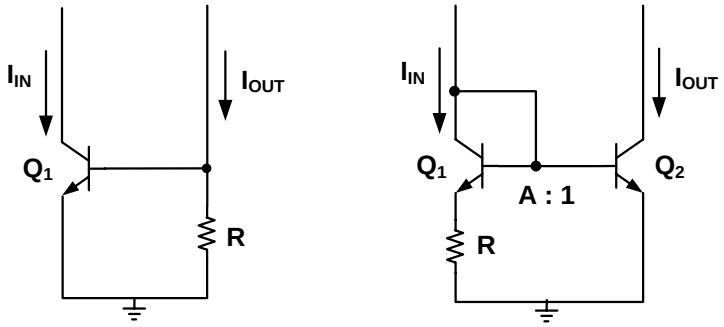
The PTAT output is typically designed to vary linearly with the thermal voltage, V_T. The circuits for such an implementation are shown in Fig. 1.1 [1]. Fig. 1.1(a) is called the peaking currents source, and Fig. 1.1(b) is called the Widlar current source. These current sources are usually loaded with a current mirror in order to realize linear variation of output current with the thermal voltage. For the peaking current source,

$$I_{OUT} = \frac{\ln(K)}{K \cdot R} V_T \tag{1.3}$$

For the Widlar current source,

$$I_{OUT} = \frac{\ln(K)}{R} V_T \tag{1.4}$$

where $K = I_{IN} / I_{OUT}$ denotes the gain of the current mirror in both figures. Alternatively, the area ratio of Q_2 to Q_1 may be set to a value greater than unity for similar results.



(a) (b)

Figure 1.2 I-PTAT circuits (a) V_{BE} biased current source, (b) inverse Widlar current source.

The I-PTAT output is most frequently implemented using the base-emitter voltage, V_{BE}, as shown in Fig. 1.2(a) [1]. The output current is given by

$$I_{OUT} = \frac{V_{BE}}{R} \tag{1.5}$$

Another approach is to use the inverse Widlar current source as depicted in Fig. 1.2(b) with the output current [34]

$$I_{OUT} = \frac{I_{IN}}{A} \exp\left(\frac{I_{IN} R}{V_T}\right) \tag{1.6}$$

where A is the area ratio of Q_1 to Q_2. The I-PTAT property can by observed from its TC_F which changes proportional to $-1/T^2$.

1.2 Strategies of Reference Circuits Design

1.2.1 Voltage Mode vs. Current Mode

Reference circuits include the voltage reference and the current reference. In the past decade, a lot of research efforts have been made to improve their temperature characteristics [1]-[16]. Those proposed techniques could be generally classified into voltage mode and current mode [2].

Voltage mode means a temperature independent voltage is obtained through appropriate combinations of temperature dependent voltages, e.g., addition of PTAT voltages and I-PTAT voltages [1], [8]-[11], or subtraction of two PTAT voltages or two I-PTAT voltages. For the voltage reference circuit, this temperature independent voltage is the final output reference voltage. For the current reference circuit, this temperature independent voltage is applied to a resistor to attain the final output reference current.

There are 3 major voltage mode designs – band-gap reference, buried Zener diode reference and XFET^{TM} reference [3]. The basic operation principle of voltage mode band-gap reference is to sum V_{BE} and V_T with appropriate weighting factors. As their opposite temperature dependences are cancelled, a reference voltage of around $1.205V$ will be achieved. A basic band-gap reference cell is shown in Fig. 1.3. The compensated reference voltage is equal to

$$V_R = V_{BE} + \frac{R_2}{R_3} \cdot \Delta V_{BE} = V_{BE} + V_T \frac{R_2}{R_3} \ln\left(\frac{I_{C2}}{I_{C1}} \cdot \frac{I_{S1}}{I_{S2}} \right) \approx 1.205\,V \qquad (1.7)$$

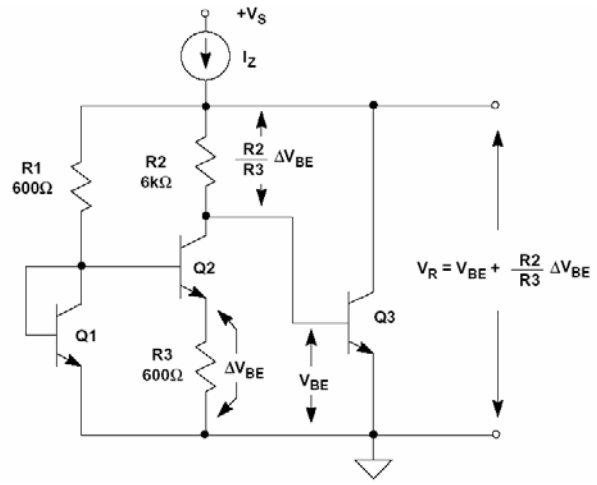


Figure 1.3 Widlar band-gap reference circuit [1] [3].

Another approach to achieve a reference voltage is to adopt the breakdown voltage of a Zener diode. When operating in the reverse breakdown region, a Zener diode exhibits negligible voltage change with current. Typically the breakdown voltage is in the range of 5*V* to 8*V* with a positive temperature drift of around +1.5*mV*/°*C* to +5*mV*/°*C* [2]. To improve the temperature performance, a forward-biased diode with a drift of roughly –2*mV*/°*C* can be cascaded as illustrated in Fig. 1.4. Surface operated diode junction breakdown is prone to crystal imperfections and other contamination. Thus Zener diodes formed at the surface are more noisy and less stable than are the buried (or sub-surface) ones.

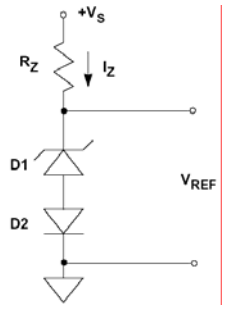


Figure 1.4 Zener diode reference circuit [2] [3].

The third approach is somewhat analogous to the band-gap reference for bipolar transistors. The JFET based reference operates a pair of JFET transistors with different pinchoff voltages, and amplifies the differential output to produce a stable reference voltage. One of the two JFETs uses an extra ion implantation. The basic topology is shown in Fig. 1.5.

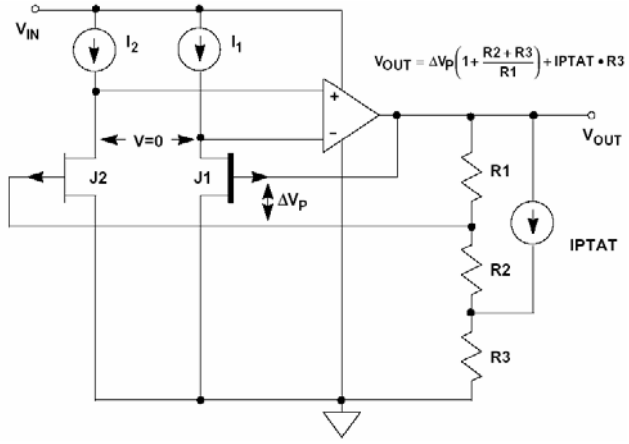


Figure 1.5 XFET^{TM} reference circuit topology [3].

The output reference voltage is given as

$$V_{OUT} = \Delta V_P \left(1 + \frac{R_2 + R_3}{R_1} \right) + I_{PTAT} \cdot R_3 \tag{1.8}$$

where ΔV_P is the difference of the pinchoff voltage of JFETs J_1 and J_2.

Table 1.1 summarizes the pro and con properties of the three major voltage mode reference architectures.

Table 1.1 Properties of voltage mode reference architectures [3].

Band-gap	Buried Zener	XFET™
< 5V supplies	> 5V supplies	< 5V supplies
High noise @ high power	Low noise @ high power	Low noise @ low power
Fair drift of < 50 *ppm*/°*C* (1st-order compensation)	Good drift of 1-2 *ppm*/°*C*	Good drift of 3-8 *ppm*/°*C*
long term stability	long term stability	long term stability
Fair hysteresis	Fair hysteresis	Low hysteresis

Current mode means a temperature independent current is obtained through appropriate combinations of temperature dependent currents. In comparison of voltage mode, current-mode compensation can be achieved by more combinations of currents including addition, subtraction, multiplication, and division, although current division can only be realized in theory. For the current reference circuit, this compensated current is just the final output reference current. For the voltage reference circuit, the final output reference voltage will be obtained as this current flows through one or more

resistors [2]. So basically an arbitrary voltage can be generated with appropriate resistor values. Due to these benefits, the designs conducted in this work will base on the current mode.

1.2.2 Technology Independent Mode vs. Technology Dependent Mode

Reference circuits can also be classified in terms of the employed temperature compensation techniques. In both voltage mode and current mode, those techniques can be divided into two categories, that is, technology dependent and technology independent.

The intrinsic device properties are determined by the fabrication technology, i.e., device parameters may present different values for different technologies. By taking advantage of such a difference properly, it is feasible to realize the temperature compensation. Since the performance of compensation is highly determined by the involved technologies, this type of compensation is considered technology dependent. Typically the temperature dependence differences in the threshold voltage of different MOS transistors and in different resistor materials are most frequently utilized for technology dependent compensation.

The threshold voltage difference can be gained by means of selective channel implant [43] [44], flat-band voltage difference with different gate materials [45], or work function difference with opposite gate doping [46]. However these solutions need additional fabrication steps. To be applicable in the standard low-cost CMOS technologies, the threshold voltage difference between NMOS and PMOS transistors is a nice choice [47].

Most processes offer a variety of resistor materials for the designer to choose from depending on the value of the resistor, precision requirements and temperature variation requirements. The selection of resistor materials can have tremendous impact on the circuit performance. Table 1.2 lists typical linear or first-order temperature coefficients for several common integrated resistance materials [48]. With careful manipulation of these resistors, their various temperature dependences can also effect high-order temperature compensation [15] [16] [23].

Table 1.2 Typical linear temperature coefficients of selected resistor materials at 25°*C*.

Material	TC_1 (*ppm*/°*C*)	Material	TC_1 (*ppm*/°*C*)
Aluminum, bulk	+3800	5*k*Ω/□, Base pinch diffusion	+2500
Copper, bulk	+4000	2*k*Ω/□, HSR implant (P-type)	+3000
Gold, bulk	+3700	500Ω/□, Polysilicon (4*k* Å N-type)	-1000
160Ω/□, Base diffusion	+1500	25Ω/□, Polysilicon (4*k* Å N-type)	+1000
7Ω/□, Emitter diffusion	+600	10*k*Ω/□, N-well	+6000

A drawback of technology dependent techniques is that compensation results are significantly degraded by processing variations, e.g., the drift of threshold voltage and resistor value. Moreover, availability of the mandated technology may restrict the wide application of these techniques. Therefore technology independent techniques, which

are relatively tolerant of processing variations, are highly preferred. This type of technique achieves the compensation through manipulation of circuit elements, not individual device parameter (at least not directly). The technology independent techniques consist of the mainstream in design of reference circuits. Thereby they will be discussed in detail with example implementations in Chapter II.

1.3 Low-Voltage Design

The intrinsic operating voltage limit of bipolar IC is somewhat greater than the base-emitter voltage of the transistors. With careful design, the "somewhat greater" aspect comes down to a collector-emitter saturation voltage ($V_{CE,SAT}$), possibly some resistive degeneration for matching improvement, and some additional safety margin to accommodate processing variation. So the low voltage constraint of conventional bipolar process requires the operating supply voltage

$$V_{SUP} > V_{BE} + V_{CE,SAT} \tag{1.9}$$

Clearly the V_{BE} and $V_{CE,SAT}$ of the bipolar transistor, and their likely variations, become quite important as the supply voltage is reduced. This constraint assumes that all parts of the circuitry have been fully optimized in terms of low operating headroom. Circuit structures like Darlington pairs, Wilson and β-helper current mirrors, and cascade configurations are all definitely out of the question as this constraint is complied. In this work, the core part of reference circuits will be developed for applications in such low-voltage environment.

1.4 Summary

This chapter gave some fundamental knowledge for the design of reference circuits. The importance of reference circuits in the power management integrated circuit family was briefly described. The prevalent PTAT and I-PTAT circuit cells, which are the basic building blocks of reference circuits, were summarized. Then the reference circuit design techniques were classified into voltage mode and current mode, or technology independent mode and technology dependent mode with their advantages and disadvantages addressed. Lastly constraints in the low-voltage design are identified. In a word, this chapter establishes a background for the analysis and design of reference circuits, which are to be completed in the following chapters.

CHAPTER 2

TEMPERATURE COMPENSATION IN BAND-GAP REFERENCES

Band-gap references have always been the most attractive technique in integrated circuit design for several reasons including relative simplicity, low voltage operation and technology independent. They are suitable for implementations in either voltage mode or current mode. The basic principle of the band-gap technique is to cancel the opposite temperature coefficients of V_{BE} and V_T as illustrated in Fig. 1.3. However V_{BE} and V_T have distinct temperature characteristics, i.e., V_T varies linearly with respect to temperature, while V_{BE} presents nonlinear variation. As a result, V_T is only capable of eliminating the linear temperature dependence of V_{BE}. And the first-order compensation is obtained. The temperature drift after first-order compensation is still too large to meet the high-precision requirement of reference circuits. To ameliorate the performance, a third compensation component needs to be added to eliminate the nonlinear temperature dependence of V_{BE}. This is known as the *curvature compensation* [1]. The curvature compensated output will exhibit much better temperature independence.

Since V_{BE} plays a significant role for the compensation in the band-gap technique, it is of great importance to investigate the temperature characteristics of V_{BE}. This may give some insight into the design of band-gap reference.

2.1 Nonlinear Temperature Characteristics of Base-Emitter Voltage

The conventional temperature compensation for a reference circuit is achieved by summing a V_{BE} dependent term and a V_T dependent term as given by

$$Y = f_1(V_{BE}) + f_2(V_T) \tag{2.1}$$

where Y is the final output of the reference circuit, f_1 is the term proportional to V_{BE} and f_2 is the term proportional to V_T. All of them represent voltage in the case of a voltage reference, and current in the case of a current reference. Because the temperature characteristics of f_1 and f_2 are intrinsically determined by V_{BE} and V_T respectively, the temperature characteristics of V_{BE} and V_T will be discussed.

The V_T increases linearly with temperature at $0.085 mV/°C$ [1]. In comparison, the temperature variation of V_{BE} is quite complicated [4]

$$V_{BE}(T) = \underbrace{(T/T_r)\cdot\left[V_{BE}(T_r) - V_G(T_r)\right]}_{1} + \underbrace{V_G(T)}_{2} - \underbrace{\eta V_T \ln(T/T_r)}_{3} + \underbrace{V_T \ln\left[I_C(T)/I_C(T_r)\right]}_{4} \tag{2.2}$$

where T_r is the nominal reference temperature (This temperature is often denoted as T_0. The subscript "0" is used to denote the quantity at $0K$. Since T_0 is not associated with $0K$, T_r is used to avoid any possible confusion), and $\eta = 4 - n$. n comes from the temperature equation of "effective" mobility, $\overline{\mu}$, and is given by [1] [4]

$$\overline{\mu}(T) = CT^{-n} \tag{2.3}$$

where C is a temperature independent constant, and the value of n depends on the technology.

The band-gap voltage, V_G, is also a temperature dependent quantity. And it differs with semiconductor materials. For silicon, to the author's knowledge, there are four methods to model the temperature variation of V_G. According to [5], an expression is given as

$$V_G(T) = V_{G0} - \frac{\alpha \cdot T^2}{T + \beta} \tag{2.4}$$

where $\alpha = 7.021 \cdot 10^{-4}$ *V/K*, $\beta = 1108$ *K* and $V_{G0} = 1.1557$ *V*. This equation and parameter values are adopted in HSpice (Level 0, 1, 3), Spectre and ADS (Level 0, 1, 3 until ADS2003A) to calculate the temperature variation of V_G.

The second method is based on the same equation, but takes into account the dissociation energy of the excitation. In [6], it was suggested that the constants in Equ. (2.4) should have the values $\alpha = 4.73 \cdot 10^{-4}$ *V/K*, $\beta = 636\,K$ and $V_{G0} = 1.170\,V$. These parameter values are adopted in Hspice (Level 2) and ADS (Level 2 until ADS2003A). An empirical modeling of V_G has been reported in [7], and is given by

$$V_G(T) = \begin{cases} 1.1785 - 9.025 \cdot 10^{-5} T - 3.05 \cdot 10^{-7} T^2 & 150K < T < 300K \\ 1.20595 - 2.7325 \cdot 10^{-4} T & 300K \le T < 400K \end{cases} \tag{2.5}$$

It can match to the measured data within $\pm 0.2mV$.

In [8] another equation was proposed as

$$V_G(T) = K_3 + K_2 T + K_1 T \ln T \tag{2.6}$$

By least-square fitting of Equ. (2.6) to Equ. (2.5), the values of K_1, K_2 and K_3 are found to be $K_1 = -8.459 \cdot 10^{-5}$ *V/K*, $K_2 = 3.042 \cdot 10^{-4}$ *V/K* and $K_3 = 1.1774$ *V*. The

discrepancy between Equ. (2.5) and Equ. (2.6) is less than $\pm 0.3mV$ over the temperature range of $0°C$ to $70°C$.

Therefore the nonlinearity of V_{BE} results from the combined effects of V_G, $\overline{\mu}$ and I_C as indicated by the second, third and fourth term in Equ. (2.2). To gain more insight, Equ. (2.2) can be expanded into Taylor series at $T = T_r$ as

$$V_{BE}(T) = V_{BE}(T_r)\left(1 + TC_1 \cdot \Delta T + TC_2 \cdot \Delta T^2 + \cdots\right) \tag{2.7}$$

where $\Delta T = T - T_r$, and

$$TC_1 = \left[\frac{I_C^{'}(T_r)}{I_C(T_r)} - \frac{I_S^{'}(T_r)}{I_S(T_r)}\right] \cdot \ln^{-1}\left[\frac{I_C(T_r)}{I_S(T_r)}\right] + \frac{1}{T_r} \tag{2.8}$$

$$\begin{aligned} TC_2 = \Bigg\{ & \frac{1}{T_r}\left[\frac{I_C^{'}(T_r)}{I_C(T_r)} - \frac{I_S^{'}(T_r)}{I_S(T_r)}\right] - \frac{1}{2}\left[\frac{I_C^{'}(T_r)}{I_C(T_r)}\right]^2 + \frac{1}{2}\left[\frac{I_S^{'}(T_r)}{I_S(T_r)}\right]^2 \\ & + \frac{1}{2}\left[\frac{I_C^{''}(T_r)}{I_C(T_r)} - \frac{I_S^{''}(T_r)}{I_S(T_r)}\right]\Bigg\} \cdot \ln^{-1}\left[\frac{I_C(T_r)}{I_S(T_r)}\right] \end{aligned} \tag{2.9}$$

where $I_C^{'}(T_r) = \left.\frac{dI_C}{dT}\right|_{T=Tr}$, $I_S^{'}(T_r) = \left.\frac{dI_S}{dT}\right|_{T=Tr}$, $I_C^{''}(T_r) = \left.\frac{d^2 I_C}{dT^2}\right|_{T=Tr}$ and $I_S^{''}(T_r) = \left.\frac{d^2 I_S}{dT^2}\right|_{T=Tr}$.

There must be non-zero higher-order terms, primarily the second-order term [4]. And these higher-order terms cannot be eliminated by V_T. Thus the conventional temperature compensation, as shown in Fig. 1.3, is considered as the first-order compensation. Improved performance can be achieved by removing the higher-order terms in V_{BE}, which demands the inclusion of a third compensation term during the compensation. However generation of such a term usually complicates the design of the

whole circuit. As a consequence, the total power consumption is increased and more chip area is occupied. Therefore a technique that requires no or less extra circuits for the curvature compensation will be highly preferred. Typically compensated to the first-order, the reference output is skewed-parabola shaped; to the second-order, 'N' shaped; to the third-order, 'M' shaped [23] as shown in Fig. 2.1. While the temperature coefficient drops from less than 50 *ppm*/°*C*, to less than 10 *ppm*/°*C*, and to less than 1 *ppm*/°*C* correspondingly.

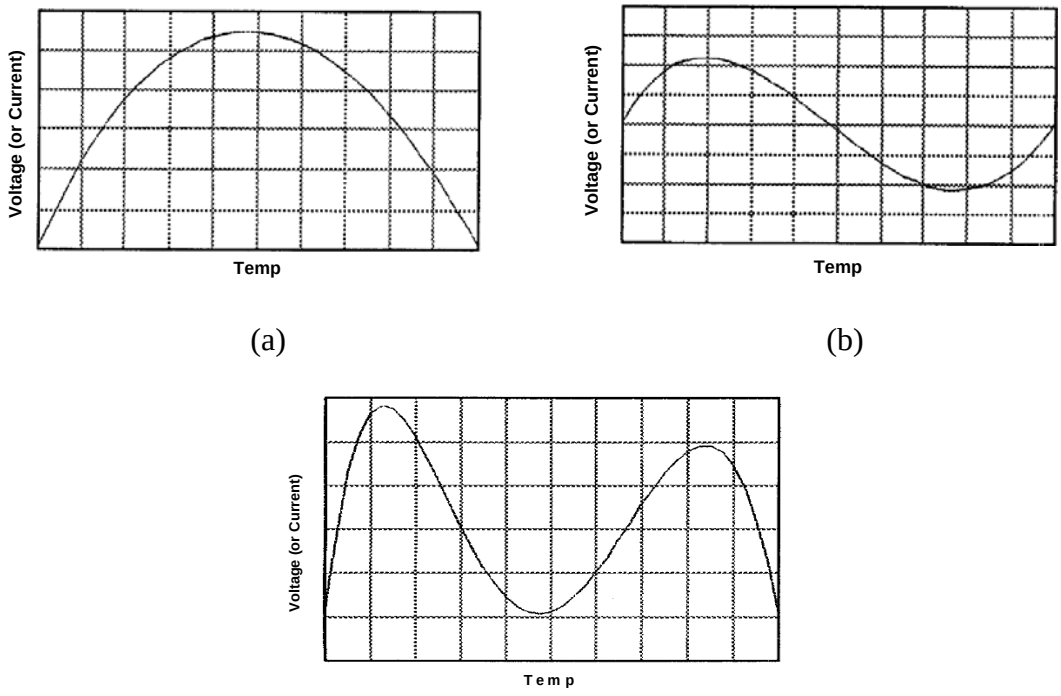


Figure 2.1 Temperature characteristics of band-gap references after (a) first-order compensation, (b) second-order compensation, (c) third-order compensation [23].

2.2 Voltage-Mode Temperature Compensation

There have been a number of effective techniques to realize the voltage mode compensation. All of them are intended for voltage reference design. A brief review of them is provided next.

2.2.1 Reference Circuit A

A curvature compensated band-gap voltage reference is shown in Fig. 2.2 [9]. The gain G of the gain block is determined by a capacitor ratio C_2/C_1. Since the temperature dependence of current can be described as [1] [4]

$$I = M \cdot T^a \tag{2.10}$$

where M is a temperature independent number. For the temperature independent current, I_I, $a = 0$. For the PTAT current, I_{PTAT}, $a = 1$.

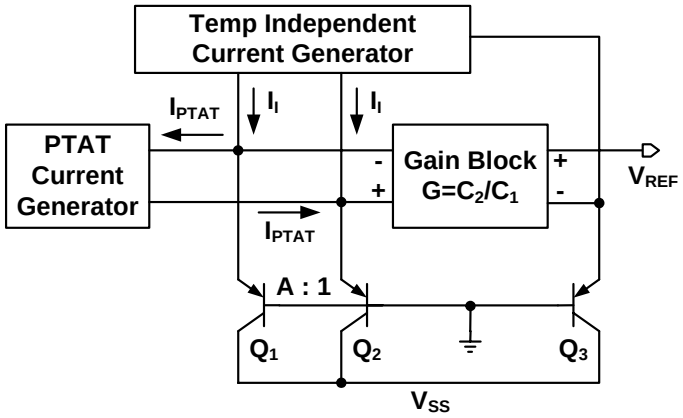


Figure 2.2 Schematic diagram of band-gap reference A [9].

The reference voltage is equal to

$$V_{REF} = V_{BE3} + G \cdot \Delta V_{BE} \tag{2.11}$$

where

$$\Delta V_{BE} = V_{BE2} - V_{BE1} = V_T \ln\left(A\frac{I_I + I_{PTAT}}{I_I - I_{PTAT}} \right) = V_T \ln A + 2\frac{I_{PTAT}}{I_I} V_T + \cdots \qquad (2.12)$$

So ΔV_{BE} contains a term proportional to T^2, which can cancel out the quadratic term in V_{BE}. The final reference output will have only higher-order temperature variations which are quite small. The measurement result shows this design is capable of exhibiting a temperature drift of 25.6 *ppm*/°*C* in the temperature range of -55°*C* to +125°*C*.

2.2.2 Reference Circuit B

Based on the similar idea, a design is developed as shown in Fig. 2.3 [8]. In the design of Fig. 2.2, ΔV_{BE} is generated using transistors Q_1 and Q_2 with bias current $I_I - I_{PTAT}$ and $I_I + I_{PTAT}$ respectively. In the design of Fig. 2.3, ΔV_{BE} is generated using transistors Q_2 and Q_3 with bias current I_{PTAT} and I_I. Adopting Equ. (2.2) for V_{BE2} and V_{BE3}, and Equ. (2.6) for V_G, ΔV_{BE} can be calculated as

$$\Delta V_{BE} = \frac{T}{T_r}\left[V_{BE2}(T_r) - V_{BE3}(T_r)\right] + V_T \ln\frac{T}{T_r} \qquad (2.13)$$

Then

$$V_{C1} = \left(1 + \frac{R_3}{R_2}\right)\Delta V_{BE} = \left(1 + \frac{R_3}{R_2}\right)\left[V_{BE2}(T_r) - V_{BE3}(T_r)\right]\frac{T}{T_r} + \left(1 + \frac{R_3}{R_2}\right)V_T \ln\frac{T}{T_r} \qquad (2.14)$$

If R_2, R_3 and R_5 are adjusted such that

$$1 + \frac{R_3}{R_2} = \eta - K_1\frac{q}{k} - 1 \qquad (2.15)$$

and

$$V_{C2} = I_{PTAT} R_5 = \left\{ K_3 - V_{BE4}(T_r) - \left(1 + \frac{R_3}{R_2}\right)\left[V_{BE2}(T_r) - V_{BE3}(T_r)\right] \right\} \frac{T}{T_r} \tag{2.16}$$

The reference voltage will be equal to

$$V_{REF} = -\left[V_{C1}(T) + V_{BE4}(T) + V_{C2}(T)\right] = -K_3 \tag{2.17}$$

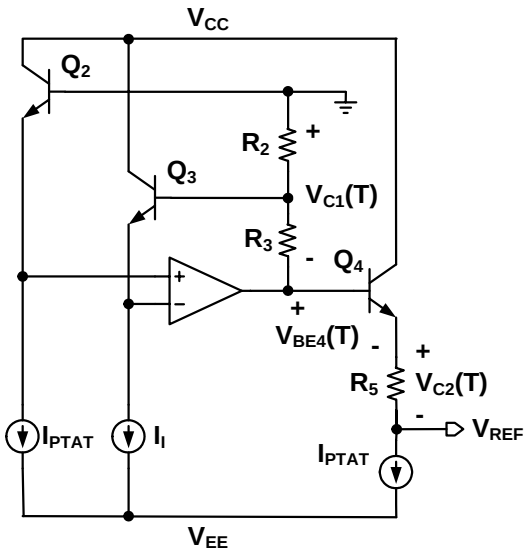


Figure 2.3 Schematic diagram of band-gap reference B [8].

The linear and nonlinear terms in V_{REF} are removed completely. Experimentally the mean value of the temperature drift is 15.1 *ppm*/°*C* over the range of 0°*C* to +70°*C*.

2.2.3 Reference Circuit C

Instead of introducing a nonlinearity term for correction, the nonlinearity in V_{BE} can be removed directly. Because the nonlinearity in V_{BE} is dependent on the bias collector current. For a transistor with PTAT current, the nonlinearity is about 25% less

than that of a transistor with constant current. If four lower-nonlinearity V_{BE} is subtracted by three higher-nonlinearity V_{BE}, there will result a voltage with linear temperature variation. Based on this principle, an implementation is shown in Fig. 2.4[10].

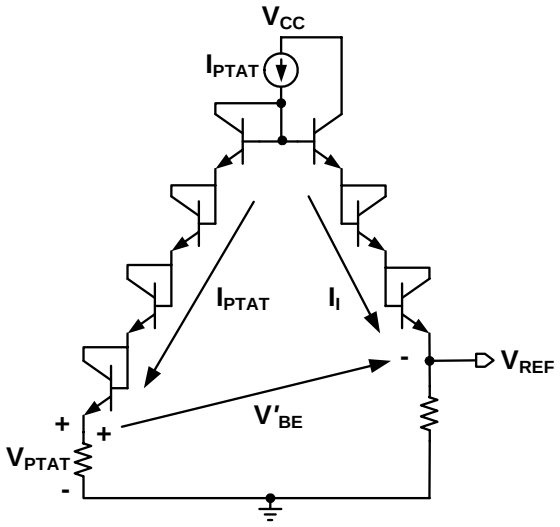


Figure 2.4 Schematic diagram of band-gap reference C [10].

The reference voltage is equal to

$$V_{REF} = V_{PTAT} + V_{BE}^{'} \tag{2.18}$$

If V_G is assumed to have linear temperature variation, $V_{BE}^{'}$ is given as

$$V_{BE}^{'} = 4V_{BE}(I_{PTAT}) - 3V_{BE}(I_I) = V_{G0} - \frac{V_{G0} - V_{BE}(T_r)}{T_r}T - (\eta - 4)V_T \ln\frac{T}{T_r} \tag{2.19}$$

Since $\eta - 4$ is approximately equal to zero, Equ. (2.19) can be further simplified to obtain a theoretical linear relationship with respect to temperature,

$$V_{BE}^{'} = V_{G0} - \frac{V_{G0} - V_{BE}(T_r)}{T_r} T \tag{2.20}$$

This design achieved a temperature drift of 5 *ppm*/°*C* over the temperature range of -25°*C* to +85°*C*.

2.2.4 Reference Circuit D

An exponentially compensated voltage reference is proposed in [11]. This design makes use of the exponential temperature properties of the current gain β to compensate the nonlinearity in V_{BE}. The concept circuit is shown in Fig. 2.5.

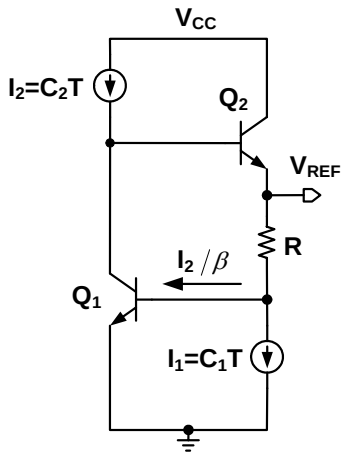


Figure 2.5 Concept schematic of band-gap reference D [11].

The reference voltage is given as

$$V_{REF} = V_{BE1}(T) + C_1 RT + C_2 RT / \beta_F \tag{2.21}$$

where

$$\beta_F = \beta_\infty \exp\left(-\frac{\Delta E_G}{kT}\right) \tag{2.22}$$

This technique is capable of achieving temperature stability superior to the second-order compensation technique. Fig. 2.5 implements a positive reference. A negative reference is simply the complement of the architecture. Experimental measurements show that the mean temperature drift is 8.94 *ppm*/°*C* and 6.65 *ppm*/°*C* for positive and negative design respectively over the temperature range of -55°*C* to +125°*C*.

2.3 Current-Mode Temperature Compensation

For voltage mode, the compensation is generally achieved through addition of temperature dependent voltages. For current mode, these techniques can be applied in a similar way. Additionally subtraction, multiplication and division of temperature dependent currents are also able to achieve the required compensation, although the division technique only works mathematically. In this section, current mode temperature compensation techniques will be discussed in terms of the current addition, current subtraction, current multiplication and current division.

2.3.1 Current Addition

The fundamental principle of current addition is to add two currents, an I-PTAT and a PTAT current, and cancel the temperature dependence in the final sum. Usually addition of such two current components is only able to achieve the first-order temperature compensation. To improve the temperature compensation performance, it is necessary to add a third current component, I_{NL}, that presents nonlinear temperature

variation. Such a current component is generated by additional circuitry, which typically increases the complexity as well as the power dissipation of the whole circuit [2] [12]. A method that does not require complicated circuitry is to utilize the base current of a BJT transistor [11].

The curvature corrected current mode reference proposed in [12] is depicted in Fig. 2.6. The principle is a current proportional to V_{BE}, $2I_{VBE}$, and a nonlinear correction current, $2I_{NL}$, are generated. When the nonlinear correction is performed appropriately, $2(I_{VBE}+I_{NL})$ should consist of a constant component, and a PTAT component which is to be compensated by using a PTAT current source.

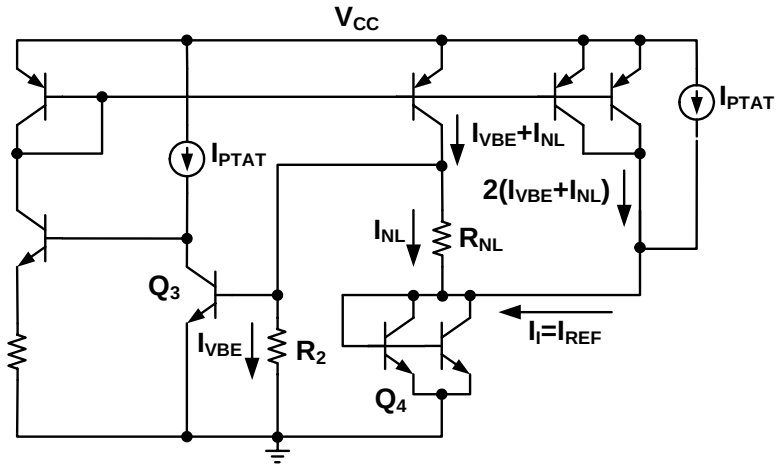


Figure 2.6 Schematic of current addition reference with curvature correction [12].

The I_{NL} is defined as the ΔV_{BE} of transistor Q_3 and Q_4 and resistor R_{NL} as

$$I_{NL}=\frac{V_T}{R_{NL}}\ln\left(\frac{I_{C3}}{I_{C4}}\frac{I_{S4}}{I_{S3}}\right)=\frac{V_T}{R_{NL}}\ln\left(\frac{I_{S4}}{I_{S3}}\frac{I_{PTAT}}{I_I+I_{NL}}\right) \tag{2.23}$$

The value of R_{NL} is chosen in such a way that the temperature dependent parts of current $2(I_{VBE}+I_{NL})$ and I_{PTAT} are able to compensate each other and obtain a temperature independent current I_I equal to

$$I_I = 2(I_{VBE}+I_{NL})+I_{PTAT} = 2V_{G0}/R_2 \tag{2.24}$$

By applying this constant current to a resistor, a reference voltage is obtained with ±3 *ppm*/°*C* temperature drift experimentally.

2.3.2 Current Subtraction

In [2], a voltage reference is developed also based on the current addition technique. However the current subtraction technique is employed to generate the nonlinear current component I_{NL} as illustrated in Fig. 2.7.

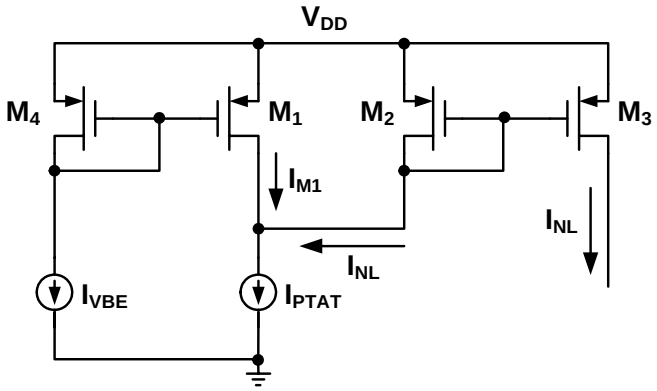


Figure 2.7 Schematic of current subtraction for nonlinear current generation [2].

At the lower half of the temperature range, I_{PTAT} is less than I_{VBE}. As a result, M_2 is off and M_1 is non-saturated with drain current limited to I_{PTAT}. At the upper half

of the temperature range, I_{PTAT} becomes greater than I_{VBE}. Then M_1 is saturated with current equal to I_{VBE}, while M_2 sources the current difference of I_{VBE} and I_{PTAT}. The resulting current in M_3 is nonlinear, and can be described as

$$I_{NL} = \begin{cases} 0 & I_{VBE} \geq I_{PTAT} \\ I_{PTAT} - I_{VBE} & I_{VBE} < I_{PTAT} \end{cases} \tag{2.25}$$

A curvature corrected reference voltage is obtained as

$$V_{REF} = I_{VBE}\left(R_1 + R_2 + R_3\right) + I_{PTAT}\left(R_1 + R_2\right) + I_{NL}R_1 \tag{2.26}$$

Generally there are two ways to interpret the purpose of the subtraction of two varying quantities – to find the difference between them or to cancel anything they have in common. It is seen the current subtraction technique implemented in [2] is aimed at the current difference, which is to be used for the temperature compensation. However, if this technique is realized for the second purpose, the compensation can be directly achieved in the subtraction operation. This theory is illustrated in Fig. 2.8.

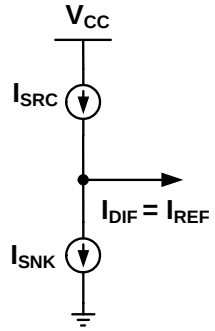


Figure 2.8 Schematic of current subtraction scheme for direct compensation.

Suppose there are two currents. One is the source current, I_{SRC}, and the other one is the sink current, I_{SNK}. They have different amplitudes at the nominal temperature, but with same polarity and amount of temperature variation. In other words, I_{SRC} and I_{SNK}, can be both PTAT or I-PTAT currents as long as they exhibit identical variation characteristics in the temperature range of interest. When they are subtracted from one another, their temperature dependence will tend to be cancelled, and a difference current, I_I, can be resulted with small or even zero variation.

2.3.3 Current Multiplication

The current multiplication scheme is actually implemented using a square-root cell as shown in Fig. 2.9. The square-root cell can be found in the output stage of *uA*741 Op-Amp composed of Q_{18}, Q_{19}, Q_{14} and Q_{20} [1]. The compensation principle stems from the fact that the multiplication is able to significantly reduce the temperature variation, and then the square-root operation will make it even smaller [13].

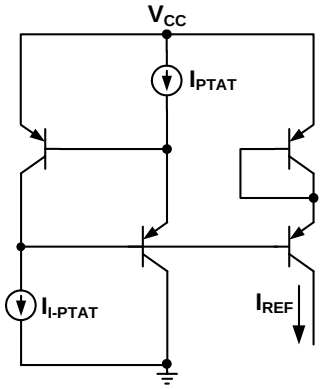


Figure 2.9 Square-root cell for implementation of current multiplication scheme [1] [13].

To provide more insight into the operating principle, the compensation behavior can be analyzed mathematically. Assume PTAT and I-PTAT currents have temperature dependence up to the second-order

$$I_{PTAT} = I_{PTAT}(T_r)\left(1 + TC_{11}\Delta T + TC_{21}\Delta T^2\right) \tag{2.27}$$

$$I_{I-PTAT} = I_{I-PTAT}(T_r)\left(1 + TC_{12}\Delta T + TC_{22}\Delta T^2\right) \tag{2.28}$$

where the first-order temperature coefficient TC_{11} is positive, while TC_{12} is negative. The sign of second-order temperature coefficients TC_{21} and TC_{22} is unknown.

The output current is given as

$$I_{REF} = \sqrt{I_{PTAT} I_{I-PTAT}} \tag{2.29}$$

Replace I_{PTAT} and I_{I-PTAT} in Equ. (2.29) with Equ. (2.27) and (2.28) respectively, and then expand it into Taylor series to the second order

$$\begin{aligned} I_{REF} = \sqrt{I_{PTAT}(T_r) I_{I-PTAT}(T_r)}\{1 + 0.5(TC_{11} + TC_{12})\Delta T \\ + [0.5(TC_{11}TC_{12} + TC_{21} + TC_{22}) - 0.125(TC_{11} + TC_{12})^2]\Delta T^2\} \end{aligned} \tag{2.30}$$

It is obvious that first-order compensation requires $TC_{11} = -TC_{12}$. When this condition is satisfied, curvature compensation can be obtained if

$$TC_{11}TC_{12} + TC_{21} + TC_{22} = 0 \tag{2.31}$$

So curvature compensation needs precise manipulation of the first- and second-order temperature coefficients.

2.3.4 Current Division

Suppose there are four currents which are labeled as I_1, I_2, I_3 and I_{REF}. The current I_{REF} is obtained by dividing the product of current I_1 and I_2 by the current I_3 as given by Equ. (2.32).

$$I_{REF} = (I_1 I_2)/I_3 \tag{2.32}$$

Current components I_1, I_2 and I_3 are approximated in the same way as in Equ. (2.27) and (2.28), and are given by

$$I_1 = I_1(T_r)(1 + TC_{11}\Delta T + TC_{21}\Delta T^2) \tag{2.33}$$

$$I_2 = I_2(T_r)(1 + TC_{12}\Delta T + TC_{22}\Delta T^2) \tag{2.34}$$

$$I_3 = I_3(T_r)(1 + TC_{13}\Delta T + TC_{23}\Delta T^2) \tag{2.35}$$

Then I_{REF} can be written as

$$\begin{aligned} I_{REF} = {} & I_1(T_r) I_2(T_r)/I_3(T_r)\{1 + (TC_{11} + TC_{12} - TC_{13})\Delta T \\ & + [TC_{11}TC_{12} - (TC_{11} + TC_{12} + TC_{13})TC_{13} + TC_{21} + TC_{22} - TC_{23}]\Delta T^2\} \end{aligned} \tag{2.36}$$

First-order and second-order compensations for the quotient current are achievable if it is satisfied that

$$TC_{11} + TC_{12} = TC_{13} \tag{2.37}$$

$$TC_{11}TC_{12} - (TC_{11} + TC_{12} + TC_{13})TC_{13} + TC_{21} + TC_{22} - TC_{23} = 0 \tag{2.38}$$

Even though the current division compensation is feasible theoretically as demonstrated above, no circuit is found to generate I_1, I_2 and I_3 with the required temperature coefficients so far.

2.4 Nonlinear Temperature Compensation Current

In both voltage mode and current mode, it is often necessary to generate a nonlinear current component to eliminate the nonlinearity of V_{BE} for higher-order compensation, such as I_2/β_F in Fig. 2.5, I_{NL} in Fig. 2.6 and Fig. 2.7. Usually these nonlinear current components aim at the cancellation of the second-order term in V_{BE}. With such second-order compensations, a typical temperature coefficient of less than 10 *ppm*/°*C* can be achieved. If higher precision is required, the third-, even the fourth-order terms need to be removed. A classical approach to provide such high-order terms is to adopt the translinear cell [21] [22].

Fig. 2.10 depicts the circuit suitable for both the third- and fourth-order term generation.

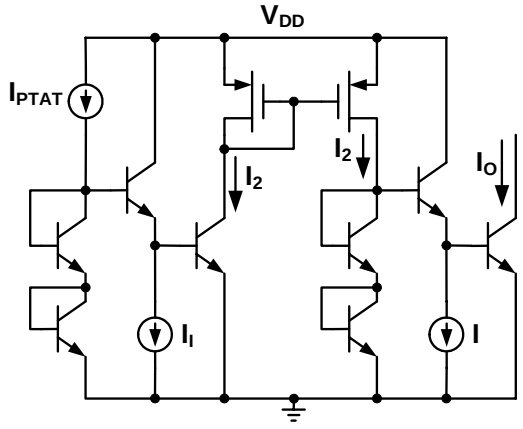


Figure 2.10 Translinear circuit generating T^3 or T^4 currents [21].

The I_2 to the left is given by

$$I_2 = I_{PTAT}^2 / I_I \tag{2.39}$$

i.e., I_2 is proportional to the T^2. With such an I_2 mirrored to the right, I_O can be found as

$$I_O = I_2^2 / I = I_{PTAT}^4 / (I_I \cdot I) \tag{2.40}$$

It is seen that I_O will be proportional to T^3 if I is PTAT, and I_O will be proportional to T^4 if I is temperature independent.

The advantage of this approach is each higher-order term can be adjusted independently since they are generated separately. Theoretically this approach is capable of reducing the temperature coefficient down to 0.2 *ppm*/°*C* [21].

2.5 Summary

The nonlinear temperature characteristics of V_{BE} are analyzed in this chapter first. Then the design of reference circuits is briefly reviewed with focus on the design of technology independent band-gap references. Through the analysis of the temperature dependence of band-gap voltage and base-emitter voltage, it is known that curvature compensation is critical for high performance reference circuits. Then some of the successful designs are illustrated in terms of the voltage mode and the current mode respectively. For the current mode, the circuits are further classified into addition, subtraction, multiplication and division.

CHAPTER 3

CURRENT-MODE BAND-GAP REFERENCES DESIGN

The reference voltage realized in the band-gap voltage mode is fixed at about $1.2V$, which corresponds to the band-gap voltage at $0K$. In comparison, the current mode approach offers the flexibility in the output voltage. Also the current addition, subtraction, multiplication and division schemes give greater maneuverability in the temperature compensation, nevertheless the division scheme is merely possible in theory so far. Therefore the current mode approach will be the choice of our design. In this chapter, the addition, subtraction and multiplication compensation schemes will be employed respectively to develop band-gap reference circuits in the current mode. The temperature dependence of the output reference current will be measured for all the designs. It is straightforward to transform the temperature independent reference current to the reference voltage if necessary.

3.1 Base-Collector-Voltage-Dependent Current

To achieve better temperature independence, higher-order terms, at least to the second-order, need to be removed in the compensation. This mandates the inclusion of a nonlinear component. To generate such a component, it is suggested not to use any additional circuitry, because the complexity as well as the power consumption of the entire circuit will increase correspondingly. A novel approach requiring no extra

circuitry is to bias the BJT transistor in the saturation region. By exploiting the operation behavior of a BJT transistor in this region, it is found there exist nonlinear current components suitable for higher-order compensation.

The basic Ebers-Moll model for a NPN transistor is depicted in Fig. 3.1 [17].

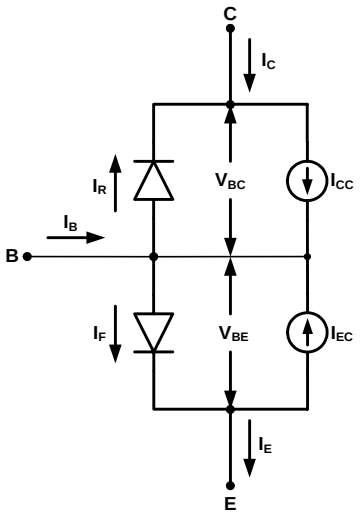


Figure 3.1 Basic Ebers-Moll model for a NPN transistor.

The currents of collector, base and emitter are given by

$$I_C = I_{CC} - I_R \tag{3.1}$$

$$I_B = (I_R - I_{EC}) - (I_{CC} - I_F) = I_{CC}/\beta_F + I_{EC}/\beta_R \tag{3.2}$$

$$I_E = I_F - I_{EC} \tag{3.3}$$

In the above equations,

$$I_{CC} = \alpha_F \cdot I_F = I_S \cdot [\exp(V_{BE}/V_T) - 1] \tag{3.4}$$

$$I_{EC} = \alpha_R \cdot I_R = I_S \cdot [\exp(V_{BC}/V_T) - 1] \tag{3.5}$$

$$\alpha_F = \beta_F / (1 + \beta_F) \tag{3.6}$$

$$\alpha_R = \beta_R / (1 + \beta_R) \tag{3.7}$$

The current I_F is the reference forward current, and I_R is the reference reverse-diode current. It is seen that all the current components depend on either V_{BE} or V_{BC}. In a general situation, the transistor operates in the forward active region with the base-emitter junction forward biased and base-collector junction reverse biased, i.e., $V_{BE} > 0$ and $V_{BC} < 0$ for a NPN transistor. In this case, V_{BC}-dependent currents, I_R and I_{EC}, are negligible since they are much less than V_{BE}-dependent counterparts, I_F and I_{CC}. However if the transistor operates in the saturation region with $V_{BC} > 0$, the effect of V_{BC}-dependent currents needs to be taken into account. With appropriate adjustments, these current components can be used for the nonlinear compensation. However saturation is out of the safe operating area of a BJT transistor. The effects of saturation will be discussed first.

3.1.1 Saturation in BJT Transistors

A BJT transistor enters saturation when both its base-emitter and base-collector junctions simultaneously are forward-biased. Unfortunately, problems can result from the saturation, which might cause circuit malfunctions [1] [48].

For discrete transistors, the saturation prolongs its turnoff time, or also called its reverse recovery time. Because forward bias of the base-collector junction results in substantial accumulation of excess minority carriers on both sides of the junction. The incurred charge cannot be withdrawn immediately.

For an integrated BJT transistor, saturation not only increases its reverse recovery time, but also has other deleterious effects.

The junction isolation, composed of P substrate and P+ isolation, is usually reversed-biased to isolate the transistor from the remainder of the circuit. If the base-collector junction is forward-biased, many of the holes injected across the base-collector junction will diffuse to the collector-substrate junction. The electric field across this reverse-biased junction draws these holes into the substrate. This process can be thought of as a PNP transistor parasitized in a NPN transistor. The base, collector and substrate of the vertical NPN transistor form the emitter, base and collector of the parasitic PNP transistor respectively. When the NPN transistor has its base-collector junctions forward-biased, the PNP transistor turns on and diverts excess base drive into the substrate. This unexpected source of substrate current can potentially lead to *substrate debiasing*. Sufficient debiasing may cause the isolation junctions to forward-bias and inject minority carriers into active circuitry. Substrate debiasing can be averted by adding guard rings to prevent holes in the collector from reaching the substrate.

Saturation also causes *current hogging*. Under the condition of saturation, some of the transistor's base current flows through the base-collector junction rather than the base-emitter junction. This diversion of current reduces the base-emitter voltage. If the base-emitter junctions of several transistors are connected in parallel, they will experience the same voltage drop when one of them saturates. As a consequence, less base drive is needed in those non-saturated transistors. In other words, the base current of the saturated transistor increases at the expense of the other transistors. This disturbs

the balance of the circuit and might lead to serious malfunctions. The current hogging can be cured by inclusion of matched ballasting resistors at the base or clamping diode across the base-collector junction.

3.1.2 Temperature Dependence of V_{BC} -Dependent Current

Next the temperature dependence of V_{BC} -dependent currents will be derived. Since the V_{BC} -dependent current may be scaled before it is able to achieve the required compensation, their temperature dependence is derived from the following approximation

$$I_{VBC} \approx B \cdot I_S \cdot \exp\left(V_{BC}/V_T\right) \tag{3.8}$$

where I_{VBC} denotes all the V_{BC} -dependent currents. (Typically, I_{VBE} and I_{VT} are used to represent the current proportional to V_{BE} and V_T respectively, i.e., $I_{VBE} = V_{BE}/R$ and $I_{VT} = V_T/R$. But I_{VBC} represents the current which is an exponential function of V_{BC} for the NPN transistor. For the PNP transistor, this current will depend on V_{CB}. Nonetheless it is still named I_{VBC}.) Also $\exp\left(V_{BC}/V_T\right) >> 1$ is assumed.

Expand Equ. (3.8) into a Taylor series at $T = T_r$

$$I_{VBC}(T) = I_{VBC}(T_r) \cdot \left(1 + TC_1 \cdot \Delta T + TC_2 \cdot \Delta T^2 + \cdots\right) \tag{3.9}$$

The first-order and second-order temperature coefficient are given by

$$TC_1 = \frac{I_S'(T_r)}{I_S(T_r)} + \frac{B'(T_r)}{B(T_r)} + \frac{V_{BC}'(T_r)}{V_{Tr}} - \frac{V_{BC}(T_r)}{T_r \cdot V_{Tr}} \tag{3.10}$$

$$TC_2 = \left[\frac{I_S^{'}(T_r)}{I_S(T_r)} + \frac{B^{'}(T_r)}{B(T_r)} - \frac{1}{T_r} + \frac{1}{2}\frac{V_{BC}^{'}(T_r)}{V_{Tr}} - \frac{1}{2}\frac{V_{BC}(T_r)}{T_r \cdot V_{Tr}}\right] \cdot \left[\frac{V_{BC}^{'}(T_r)}{V_{Tr}} - \frac{V_{BC}(T_r)}{T_r \cdot V_{Tr}}\right] + \frac{B^{'}(T_r)}{B(T_r)}\frac{I_S^{'}(T_r)}{I_S(T_r)} + \frac{1}{2}\frac{I_S^{''}(T_r)}{I_S(T_r)} + \frac{1}{2}\frac{B^{''}(T_r)}{B(T_r)} + \frac{1}{2}\frac{V_{BC}^{''}(T_r)}{V_{Tr}} \quad (3.11)$$

where $I_S^{'}(T_r) = \frac{dI_S}{dT}\Big|_{T=Tr}$, $I_S^{''}(T_r) = \frac{d^2 I_S}{dT^2}\Big|_{T=Tr}$, $B^{'}(T_r) = \frac{dB}{dT}\Big|_{T=Tr}$, $B^{''}(T_r) = \frac{d^2 B}{dT^2}\Big|_{T=Tr}$,

$V_{BC}^{'}(T_r) = \frac{dV_{BC}}{dT}\Big|_{T=Tr}$ and $V_{BC}^{''}(T_r) = \frac{d^2 V_{BC}}{dT^2}\Big|_{T=Tr}$.

The temperature dependent expression of I_S is given as

$$I_S(T) = I_S(T_r)\left(\frac{T}{T_r}\right)^{\eta} \exp\left[\frac{V_G(T_r)}{V_{Tr}} - \frac{V_G(T)}{V_T}\right] \quad (3.12)$$

Appendix A provides the derivation of above equation. Then $I_S^{'}(T_r)/I_S(T_r)$ and $I_S^{''}(T_r)/I_S(T_r)$ are equal to

$$\frac{I_S^{'}(T_r)}{I_S(T_r)} = \frac{\eta}{T_r} - \frac{V_G^{'}(T_r)}{V_{Tr}} + \frac{V_G(T_r)}{T_r \cdot V_{Tr}} \quad (3.13)$$

$$\frac{I_S^{''}(T_r)}{I_S(T_r)} = -\frac{\eta}{T_r^2} + \left[\frac{\eta}{T_r} + \frac{V_G(T_r)}{T_r \cdot V_{Tr}} - \frac{V_G^{'}(T_r)}{V_{Tr}}\right]^2 - \frac{2}{T_r \cdot V_{Tr}}\left[\frac{V_G(T_r)}{T_r} - V_G^{'}(T_r)\right] - \frac{V_G^{''}(T_r)}{V_{Tr}} \quad (3.14)$$

where $V_G^{'}(T_r) = \frac{dV_G}{dT}\Big|_{T=Tr}$ and $V_G^{''}(T_r) = \frac{d^2 V_G}{dT^2}\Big|_{T=Tr}$.

The parameter η correspond to " *XTI* " in the Spice Gummel-Poon (SGP) model. It is a technology dependent parameter. Typically η is around 4. If it is assumed $\eta = 4$ and $T_r = 25\,°C$, $I_S^{'}(T_r)/I_S(T_r)$ is calculated to be $0.17\,K^{-1}$, and $I_S^{''}(T_r)/I_S(T_r)$ is

$0.028\,K^{-2}$. For ±25% variation of η around 4, $I_S^{'}(T_r)/I_S(T_r)$ changes within ±2%, and $I_S^{''}(T_r)/I_S(T_r)$ changes within ±4%.

The temperature dependences of V_{BC} and scaling factor B are determined by the design of the reference circuit. In the next two sections, four designs will be proposed. Two of them are based on the current addition scheme. The other two are based on the current subtraction scheme. In these four designs, the saturation transistor is biased with various topologies, resulting V_{BC} or B to differ from each other. As shown next this difference will lead to distinct I_{VBC}, thereby distinct compensation effects.

3.2 Current-Addition Reference Designs

Two current-mode band-gap reference circuits are proposed by taking the advantage of the nonlinear temperature characteristics of V_{BC}-dependent currents. Hence they are named I_{VBC}-compensated band-gap references. These two designs both generate a positive reference voltage from ground. With slight modifications, they can be easily transformed to their complementary topology for the negative reference voltage generation.

3.2.1 I_{VBC}-Compensated Band-gap Reference A

The prototype circuit of the first I_{VBC}-compensated band-gap reference is depicted in Fig. 3.2.

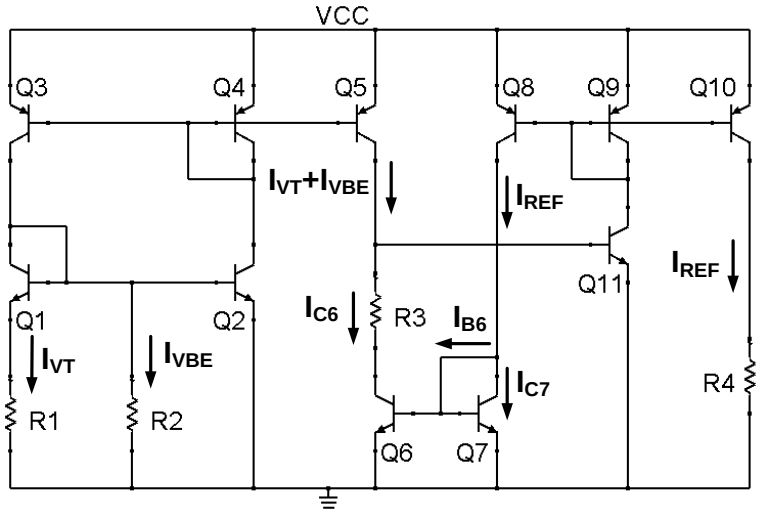


Figure 3.2 Prototype circuit of I_{VBC} -compensated band-gap reference A.

The operation principle is explained below. Q_1 ~ Q_4, R_1 and R_2 constitute a combination of a V_T -biased current source and a V_{BE} -biased current source [1] [33], and generate a current equal to $I_{VT} + I_{VBE}$ which are given by

$$I_{VT} = \frac{V_T}{R_1} \ln\left[\left(1 + \frac{I_{VBE}}{I_{VT}}\right)\frac{I_{S1}}{I_{S2}}\right] = \frac{V_T}{R_1}\left[\ln\left(1 + \frac{I_{VBE}}{I_{VT}}\right) + \ln\left(\frac{I_{S1}}{I_{S2}}\right)\right] \tag{3.15}$$

$$I_{VBE} = \frac{V_{BE2}}{R_2} \tag{3.16}$$

During the addition operation, I_{VT} and I_{VBE} will compensate each other to the first-order. Then this first-order compensated current $I_{VT} + I_{VBE}$ is mirrored by Q_5 before being fed into Q_6. Q_6 is intentionally biased in the saturation region. If the base currents of those transistors in the active region are neglected, from Equ. (3.1) the collector current of Q_6 is obtained as

$$I_{C6} = I_{VT} + I_{VBE} = I_{CC6} - I_{R6} \tag{3.17}$$

After rearrangements, I_{CC6} is given as

$$I_{CC6} = I_{VT} + I_{VBE} + I_{R6} = I_{VT} + I_{VBE} + I_{EC6}/\alpha_R \tag{3.18}$$

For Q_7, the diode-connection results $I_{EC7} = 0$. Then the collector current only depends on the V_{BE}, and $I_{C7} = I_{CC7}$ can be obtained from Equ. (3.1). Because Q_6 and Q_7 have the same base-emitter voltage and area factor, it is true that $I_{CC7} = I_{CC6}$. By taking into account the significant base current of Q_6 as given by Equ. (3.2), the reference current is derived as

$$I_{REF} = I_{C7} + I_{B6} = I_{CC6} + \frac{I_{CC6}}{\beta_F} + \frac{I_{EC6}}{\beta_R} = \frac{I_{CC6}}{\alpha_F} + \frac{I_{EC6}}{\beta_R} \tag{3.19}$$

Replacing I_{CC6} with Equ. (3.18), after rearrangement I_{REF} can be rewritten as

$$I_{REF} = \frac{1}{\alpha_F}\left(I_{VT} + I_{VBE}\right) + \left(\frac{1}{\alpha_F \alpha_R} + \frac{1}{\beta_R}\right) I_{EC6} \tag{3.20}$$

If it is assumed α_F is always equal to 1, the above equation can be simplified to

$$I_{REF} \approx \left(I_{VT} + I_{VBE}\right) + \left(\frac{1}{\alpha_R} + \frac{1}{\beta_R}\right) I_{EC6} = \left(I_{VT} + I_{VBE}\right) + \left(\frac{2 + \beta_R}{\beta_R}\right) I_{EC6} \tag{3.21}$$

Then

$$I_{VBC} = \left[\left(2 + \beta_R\right)/\beta_R\right] I_{EC6} \tag{3.22}$$

with

$$B = \left(2 + \beta_R\right)/\beta_R \tag{3.23}$$

Since this I_{VBC} is to compensate the nonlinearity of $I_{VT} + I_{VBE}$ to the second-order, the second-order temperature coefficients of I_{VT} , I_{VBE} and I_{VBC} will be investigated next.

Equ. (3.16) defines I_{VBE} . If the resistor is assumed temperature independent, the TC_2 of I_{VBE} is the same as that of V_{BE} which is given by Equ. (2.9). It has a negative value on the order of $10^{-6} K^{-2}$.

As shown in Equ. (3.15), I_{VT} is not linearly proportional to V_T in this design. (Actually due to the effects of base currents, the current generated by the conventional V_T -biased current source exhibits nonlinearity also. The simulation results show that it has a TC_2 of -3.75e-7 K^{-2} when the area ratio is set to 2. This value is less than that of I_{VBE} .) The nonlinearity is comparable to that of I_{VBE} , but can be reduced by increasing the area ratio of Q_1 to Q_2 such that $\ln(1 + I_{VBE}/I_{VT})$ is much less than $\ln(I_{S1}/I_{S2})$. The simulated TC_2 of I_{VT} and I_{VBE} for different area ratio of Q_1 to Q_2 are listed in Table 3.1.

Table 3.1 TC_2 of I_{VT} and I_{VBE} for different area ratio of Q_1 to Q_2.

Area ratio of Q_1 to Q_2	2	10	20
TC_2 of I_{VT} (K^{-2})	-2.87e-6	-7.6e-7	-4.5e-7
TC_2 of I_{VBE} (K^{-2})	-1.04e-6	-8.67e-7	-8.32e-7

For this reason, the structure adopted in Fig. 3.2 for $I_{VT} + I_{VBE}$ generation exhibits relatively high nonlinearity which will raise the difficulty for the follow-up higher-order compensation. The replacement structures will be presented in Chapter V.

It is observed that the current $I_{VT} + I_{VBE}$ generated by $Q_1 \sim Q_4$ has negative TC_2, mandating positive TC_2 of the nonlinear compensation current, I_{VBC}. To calculate the TC_2 of I_{VBC}, each term in Equ. (3.11) needs to be determined. I_S-associated terms are calculated in Equ. (3.13) and (3.14). Next the temperature dependence of the scaling factor B, as given in Equ. (3.23), will be obtained.

If the temperature dependence of β_R is assumed equal to $\beta_R(T) = \beta_R(T_r)(T/T_r)^m$ [18] [19], $B'(T_r)/B(T_r)$ and $B''(T_r)/B(T_r)$ are calculated to be

$$\frac{B'(T_r)}{B(T_r)} = \frac{-2m}{[2+\beta_R(T_r)]T_r} \tag{3.24}$$

$$\frac{B''(T_r)}{B(T_r)} = \frac{2m(m+1)}{[2+\beta_R(T_r)]T_r^2} \tag{3.25}$$

Technology dependent parameters m and β_R correspond to "*XTB*" and "*BR*" respectively in the SGP model. Typically m is less than 1, and β_R differs from less than 1 to 30. With m and β_R in these ranges, $B'(T_r)/B(T_r)$ is on the order of $10^{-3}K^{-1}$ or less, and $B''(T_r)/B(T_r)$ is on the order of $10^{-6}K^{-2}$ or less. Since $I_S'(T_r)/I_S(T_r)$ and $I_S''(T_r)/I_S(T_r)$ are on the order of $10^{-1}K^{-1}$ and $10^{-2}K^{-2}$ respectively, the temperature dependence caused by $(2+\beta_R)/\beta_R$ is negligible.

The temperature dependence of I_{VBC} is also affected by V_{BC}. The V_{BC} of Q_6 is determined from the loop formed by Q_6, Q_{11} and R_3, and given by

$$V_{BC6} = V_{BE6} - V_{BE11} + V_{R3} \tag{3.26}$$

V_{BE6} can be expressed by Equ. (2.2) as

$$\begin{aligned} V_{BE6}(T) = (T/T_r)\cdot[V_{BE6}(T_r) - V_G(T_r)] + V_G(T) \\ - \eta V_T \ln(T/T_r) + V_T \ln[I_{C6}(T)/I_{C6}(T_r)] \end{aligned} \tag{3.27}$$

I_{C6} can be expressed in the form of Equ. (2.10) with the temperature exponent equal to 2, because I_{C6} primarily exhibits only the second-order variation.

$$I_{C6}(T) = M \cdot T^2 \tag{3.28}$$

If I_{C6} is replaced by Equ. (3.28), Equ. (3.27) can be rewritten as

$$V_{BE6}(T) = (T/T_r)\cdot[V_{BE6}(T_r) - V_G(T_r)] + V_G(T) - (\eta - 2)\cdot V_T \ln(T/T_r) \tag{3.29}$$

By knowing that I_{C11} is temperature independent, V_{BE11} can be expressed in a similar way as

$$V_{BE11}(T) = (T/T_r)\cdot[V_{BE11}(T_r) - V_G(T_r)] + V_G(T) - \eta V_T \ln(T/T_r) \tag{3.30}$$

Substitute Equ. (3.29) and (3.30) into Equ. (3.26) for the corresponding terms, and rearrange

$$V_{BC6}(T) = (T/T_r)\cdot[V_{BE6}(T_r) - V_{BE11}(T_r)] + 2\cdot V_T \ln(T/T_r) + V_{R3} \tag{3.31}$$

Then $V_{BC}^{'}(T_r)$ and $V_{BC}^{''}(T_r)$ can be evaluated as

$$V_{BC6}^{'}(T_r) = \frac{V_{BE6}(T_r) - V_{BE11}(T_r) + 2V_{Tr}}{T_r} + V_{R3}^{'}(T_r) \tag{3.32}$$

$$V_{BC6}^{''}(T_r) = 2\frac{V_{Tr}}{T_r^2} + V_{R3}^{''}(T_r) \tag{3.33}$$

where $V_{R3}^{'}(T_r) = \frac{dV_{R3}}{dT}\big|_{T=Tr}$, $V_{R3}^{''}(T_r) = \frac{dV_{R3}}{dT}\big|_{T=Tr}$ and $V_{R3} = (I_{VT} + I_{VBE}) \cdot R_3$. If the resistor is assumed temperature independent, $V_{R3}^{'}$ is mainly determined by the first-order derivative of I_{VT} and I_{VBE}, which are denoted as $I_{VT}^{'} = \frac{dI_{VT}}{dT}$ and $I_{VBE}^{'} = \frac{dI_{VBE}}{dT}$ respectively. Because of the first-order compensation of I_{VT} and I_{VBE} , $I_{VT}^{'}(T_r) + I_{VBE}^{'}(T_r) = 0$, and $V_{R3}^{'}(T_r) = 0$ correspondingly. Thus $V_{BC6}^{'}(T_r)$ will be largely determined by the base-emitter voltage difference of Q_6 and Q_{11}.

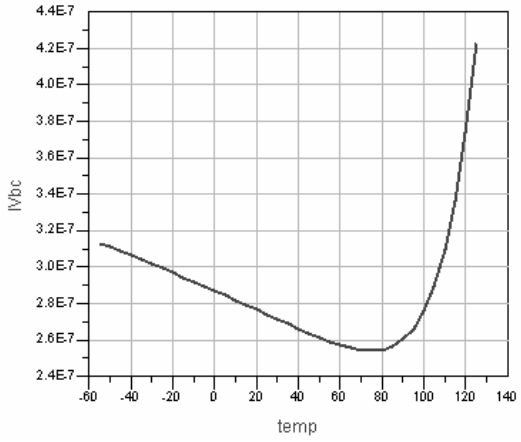
The negative second-order temperature drift of $I_{VT} + I_{VBE}$ makes $V_{R3}^{''}(T_r)$ negative also. This negative value is offset by the positive $2V_{Tr}/T_r^2$, which may lead to small $V_{BC6}^{''}(T_r)$.

So far every term necessary to compute the TC_1 and TC_2 of I_{VBC} has been determined. If Equ. (3.13), (3.14), (3.24), (3.25). (3.32) and (3.33) are substituted into Equ. (3.10) and (3.11) for the corresponding terms, the temperature coefficients can be expressed in terms of process-dependent terms and adjustable terms. Those terms associated with I_S and β_R are determined by the process, such as η, β_R and m. To acquire proper temperature coefficients, we can only adjust the temperature dependence of V_{BC6} through R_3, in that R_3 has large an impact on the first- and second-order derivative of V_{BC6}. The temperature drift of $I_{VBC}(T)$ depends on the product of $I_{VBC}(T_r)$

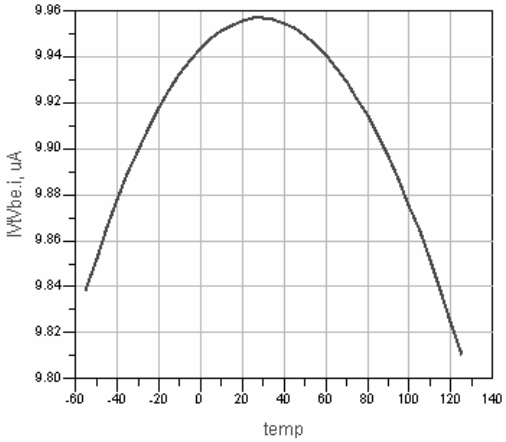
and temperature coefficients. Therefore the desired temperature drift can also be gained by means of changing $I_{VBC}(T_r)$, which is determined by R_3 and the area factor of Q_6. On the other hand, the temperature drift of $I_{VT} + I_{VBE}$ can be adjusted to facilitate the compensation of I_{VBC}. This can be achieved with appropriate values of R_1, R_2 and area ratio of Q_1 to Q_2.

The optimization of these parameter values is completed in ADS. During the optimization, R_1, R_2, R_3, area ratio of Q_1 to Q_2 and area factor of Q_6 are altered simultaneously for the least temperature variation of I_{REF} from -55°*C* to +125°*C*.

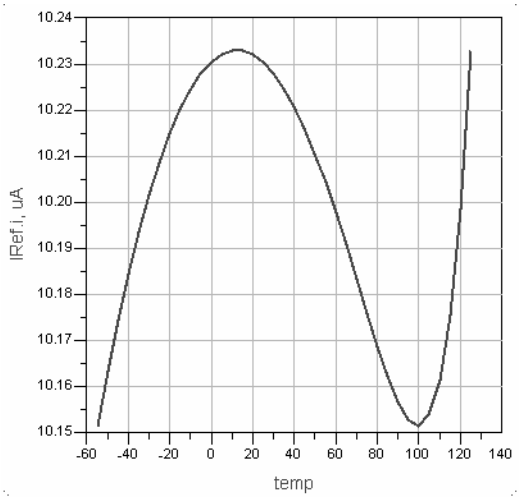
Fig. 3.3 depicts the simulation results after the optimization. Compensated to the second-order as depicted by Fig. 3.3(c), I_{REF} presents an average value of 10.2*uA* with a deviation of 44.4 *ppm*/°*C*. Although it is possible to reduce the deviation to 22 *ppm*/°*C*, this is achieved at the price of high branch currents if the same load resistor is used. This high current (i.e., more than 100*uA*) will bias Q_{10} in the saturation region. As explained in the next section, the saturation of Q_{10} may be unstable, since it depends on the power supply. Also higher currents cause more power consumptions, which is not suitable for the low-power design.



(a)



(b)



(c)

Figure 3.3 Temperature characteristics of I_{VBC} -compensated band-gap reference A (a) temperature variation of I_{VBC}, (b) temperature variation of $I_{VT} + I_{VBE}$, and (c) temperature variation of I_{REF}.

Although only Q_6 is intentionally biased in the saturation region, there are other transistors working in the saturation region accidentally during part of the temperature range. These transistors include Q_2, Q_3, Q_5, Q_8 and Q_{11}. This is an effect of low power supply voltage. For instance, for the transistor Q_2, its collector voltage is equal to the

supply voltage minus the emitter-base voltage of Q_4. This collector voltage may be less than its base voltage if the supply voltage is low. Then Q_2 is in saturation with the base-collector junction forward-biased. As the temperature increases, the temperature characteristics of base-emitter voltage cause the base voltage of Q_2 to decrease, while the collector voltage of Q_2 to increase. As a result, the base-collector junction will become reverse-biased. Q_2 begins to work in the active region. However, it should be noticed that Q_2, Q_3, Q_5, Q_8 and Q_{11} are unlike Q_6. They are not in hard saturation. Since the transistor behaviors in the soft saturation and in the active region do not deviate significantly, equations for the transistor in the active region are adopted for them in the entire temperature range.

3.2.2 I_{VBC}-Compensated Band-gap Reference B

The prototype circuit of second I_{VBC}-compensated band-gap reference is depicted in Fig. 3.4. In this design, $Q_1 \sim Q_4$ fulfill the same function as in the first design. The sum current $I_{VT} + I_{VBE}$ is fed into Q_6, which is the saturation transistor. However the saturation bias of Q_6 is realized in a different way.

The collector current of Q_6 is given by

$$I_{C6} = I_{CC6} - I_{R6} = I_{VT} + I_{VBE} - I_{B6} \tag{3.34}$$

The temperature independent reference current is to be developed in Q_7. Since Q_7 operates in the active region, $I_{C7} \approx I_{CC7}$. Still the same base-emitter voltage and area factor of Q_6 and Q_7 make $I_{CC7} = I_{CC6}$. Then from Equ. (3.34), I_{C7} can be obtained as

$$I_{C7} = I_{CC6} = I_{VT} + I_{VBE} + I_{R6} - I_{B6} \tag{3.35}$$

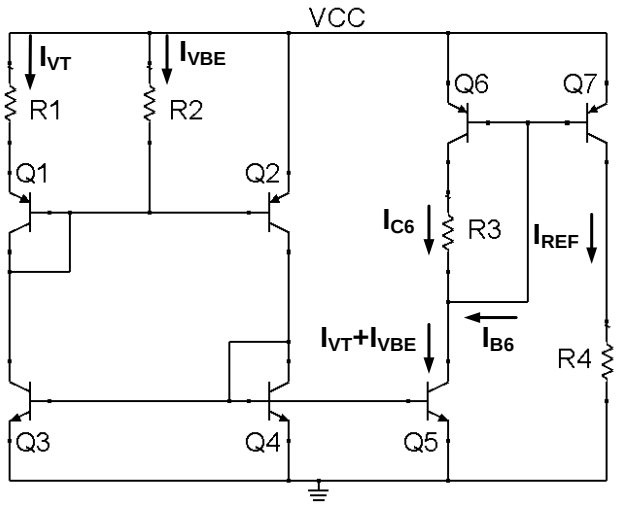


Figure 3.4 Prototype circuit of I_{VBC} -compensated band-gap reference B.

If Equ. (3.2), (3.5) and (3.7) are used, $I_{R6} - I_{B6}$ can be expressed in terms of I_{CC6} and I_{EC6} as

$$I_{R6} - I_{B6} = \frac{I_{EC6}}{\alpha_R} - \left(\frac{I_{EC6}}{\beta_R} + \frac{I_{CC6}}{\beta_F} \right) = \frac{I_{EC6}(1+\beta_R)}{\beta_R} - \frac{I_{EC6}}{\beta_R} - \frac{I_{CC6}}{\beta_F} = I_{EC6} - \frac{I_{CC6}}{\beta_F} \quad (3.36)$$

With Equ. (3.36), Equ. (3.35) can be rewritten as

$$I_{C7} = I_{VT} + I_{VBE} + I_{EC6} - I_{C7}/\beta_F \quad (3.37)$$

or

$$I_{REF} = I_{C7} = \frac{\beta_F}{\beta_F + 1}(I_{VT} + I_{VBE} + I_{EC6}) \approx I_{VT} + I_{VBE} + I_{EC6} \quad (3.38)$$

For this design, $I_{VBC} = I_{EC6}$ with $B = 1$.

The temperature dependences of I_{VT} and I_{VBE} are unchanged from the first design. For I_{VBC}, it is only necessary to investigate the temperature drift of V_{CB6}. (V_{CB} is used because Q_6 is a PNP transistor.) V_{CB6} is equal to the voltage drop of resistor R_3

$$V_{CB6} = V_{R3} = \left(I_{CC6} - I_{R6}\right)R_3 \tag{3.39}$$

Since I_{CC6} is intrinsically I_{REF}, it is assumed temperature independent. Thus the temperature dependence of V_{CB6} is totally defined by I_{R6}. The first- and second-order derivatives of V_{CB6} are given by

$$V_{CB6}^{'}(T_r) = \frac{-\dfrac{I_S^{'}(T_r)}{I_S(T_r)} + \dfrac{\alpha_R^{'}(T_r)}{\alpha_R(T_r)} + \dfrac{V_{CB6}(T_r)}{T_r \cdot V_{Tr}}}{\dfrac{1}{V_{Tr}} + \dfrac{1}{I_{R6}(T_r)\cdot R_3}} \tag{3.40}$$

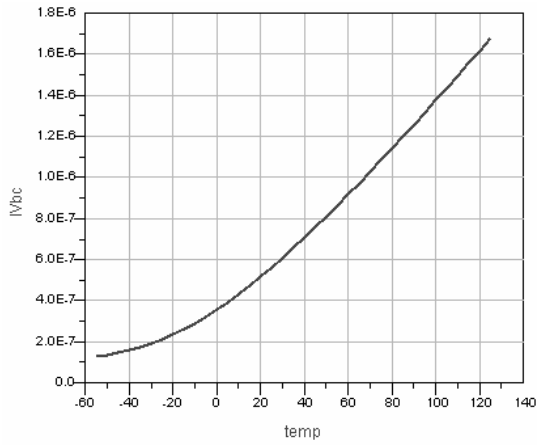
$$\begin{aligned} V_{CB6}^{''}(T_r) = \Bigg\{ & \left[\frac{2}{T_r} - 2\frac{I_S^{'}(T_r)}{I_S(T_r)} + 2\frac{\alpha_R^{'}(T_r)}{\alpha_R(T_r)} - \frac{V_{CB6}^{'}(T_r)}{V_{Tr}} + \frac{V_{CB6}(T_r)}{T_r \cdot V_{Tr}}\right] \\ & \cdot \left[\frac{V_{CB6}^{'}(T_r)}{V_{Tr}} - \frac{V_{CB6}(T_r)}{T_r \cdot V_{Tr}}\right] + 2\frac{\alpha_R^{'}(T_r)}{\alpha_R(T_r)}\left[\frac{I_S^{'}(T_r)}{I_S(T_r)} - \frac{\alpha_R^{'}(T_r)}{\alpha_R(T_r)}\right] \\ & - \frac{I_S^{''}(T_r)}{I_S(T_r)} + \frac{\alpha_R^{''}(T_r)}{\alpha_R(T_r)}\Bigg\} \frac{1}{1/V_{Tr} + 1/[I_{R6}(T_r)\cdot R_3]} \end{aligned} \tag{3.41}$$

where

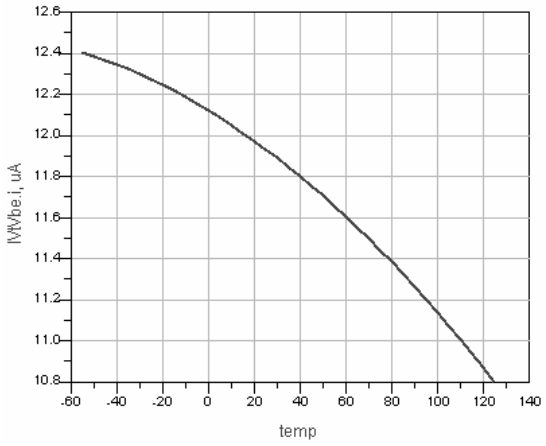
$$\frac{\alpha_R^{'}(T_r)}{\alpha_R(T_r)} = \left[1 - \alpha_R(T_r)\right]\frac{m}{T_r} \tag{3.42}$$

$$\frac{\alpha_R^{''}(T_r)}{\alpha_R(T_r)} = \left[m - 1 - 3m\alpha_R(T_r) + 2m\alpha_R^2(T_r) + \alpha_R(T_r)\right]\frac{m}{T_r^2} \tag{3.43}$$

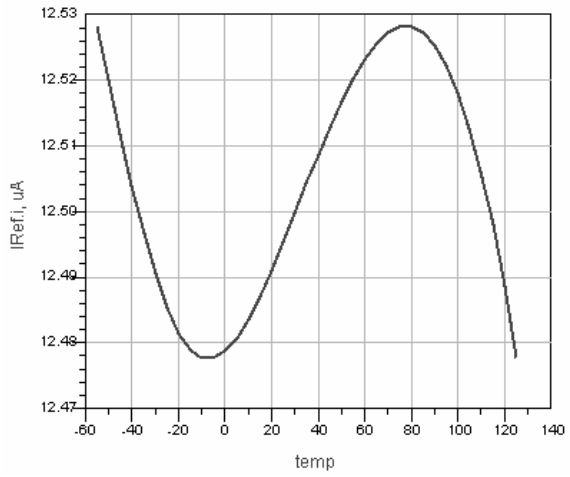
The same optimization strategy is adopted for this design. The simulated I_{REF} presents an average value of 12.5*uA* with a deviation as small as 22.4 *ppm*/°*C* as illustrated in Fig. 3.5(c).



(a)



(b)



(c)

Figure 3.5 Temperature characteristics of I_{VBC} -compensated band-gap reference B (a) temperature variation of I_{VBC}, (b) temperature variation of $I_{VT} + I_{VBE}$, and (c) temperature variation of I_{REF}.

During the course of optimization of the I_{VBC} -compensated band-gap reference A and B, it is found that usually the best compensation effects do not occur when the first-order temperature coefficient of I_{VBC} is zero as demonstrated by Fig. 3.3 (a) and 3.5(a). This feature intrigues us to make use of I_{VBC} intentionally as first-order temperature compensation currents as exemplified next.

3.3 Current-Subtraction Reference Designs

The reference circuit is to be designed using the current subtraction technique. As illustrated in Fig. 2.8, the compensation can be realized as one temperature dependent current is subtracted from the other one with the same temperature dependence.

To generate two currents with the same temperature dependence, the simplest way is to duplicate them from the same one current source. For example, assume a current proportional to V_{BE} is generated as

$$I_{VBE} = I_{VBE}(T_r)(1 - TC_1\Delta T) = I_{VBE}(T_r) - I_{VBE}(T_r)TC_1\Delta T \tag{3.44}$$

where $I_{VBE}(T_r)$ is the temperature invariant part and $I_{VBE}(T_r)TC_1\Delta T$ is the temperature variant part. Then this current is duplicated by two transistors with different area factors such that a difference current can be obtained. However the temperature variant and invariant parts are scaled at the same rate. The difference current will be still temperature dependent. Consequently it is necessary to adjust the temperature dependences of those two duplicated currents before the subtraction. More specifically,

either magnify the temperature dependence of the smaller current, or reduce the temperature dependence of the larger current.

This task can be accomplished again by V_{BC} -dependent currents. They are capable of the first-order compensation, nevertheless they are usually aimed at nonlinear temperature compensation. This capability can be utilized for direct first-order temperature compensation. As we know the conventional compensation currents I_{VT} and I_{VBE} have positive and negative first-order temperature coefficient respectively, what about I_{VBC} ? As indicated by Equ. (3.10), the TC_1 of I_{VBC} is adjustable, i.e., I_{VBC} can be either PTAT or I-PTAT current. However it is usually hard to make I_{VBC} an I-PTAT current. Because the TC_1 of I_{VBC} is primarily determined by $I_S^{'}(T_r)/I_S(T_r)$ and $[V_{BC}^{'}(T_r)-V_{BC}(T_r)/T_r]/V_{Tr}$. $I_S^{'}(T_r)/I_S(T_r)$ has a positive value of $0.17\,K^{-1}$. To make TC_1 negative, V_{BC} needs to at least decrease for approximately 0.5V from -25°C to +125°C, if $V_{BC}(T_r)$ is assumed to be 0.5V. Such a large amount of variation is hard to achieve. For this reason, basically I_{VBC} will function as a PTAT current if it is employed to compensate the first-order temperature dependence of certain current. The compensation accomplished in this approach will be illustrated with the following two designs.

3.3.1 I_{VBC} -Compensated Band-gap Reference C

The prototype circuit is depicted in Fig. 3.6. The I_{VBE} generated by Q_1, Q_3, Q_4 and R_1 is duplicated by Q_5 and Q_6. The area factor of Q_5 is larger than that of Q_6, say,

$2:1$, such that a difference current can flow through R_2. To make the difference current temperature independent, the temperature drift difference of I_{C5} and I_{C6} needs to be eliminated. This is achieved by taking advantage of the PTAT temperature characteristics of I_{VBC}.

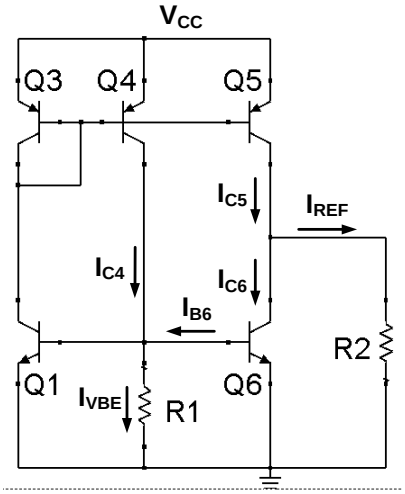


Figure 3.6 Prototype circuit of I_{VBC} -compensated band-gap reference C.

Since Q_6 is intentionally biased in saturation, the collector current of Q_4 is given by

$$I_{C4} = I_{VBE} + I_{B6} \tag{3.45}$$

This current is duplicated by Q_5 as

$$I_{C5} = 2I_{C4} = 2\left(I_{VBE} + I_{B6}\right) \tag{3.46}$$

Q_1 is fed by the collector current of Q_3, which is equal to the collector current of Q_4. Still $I_{C1} = I_{CC1}$ because Q_1 is in active region. Then I_{CC6} can be expressed as

$$I_{CC6} = I_{CC1} = I_{VBE} + I_{B6} \tag{3.47}$$

With the above equation for I_{CC6}, the collector current of Q_6 is given by

$$I_{C6} = I_{CC6} - I_{R6} = I_{VBE} + I_{B6} - I_{R6} \approx I_{VBE} - I_{EC6} \tag{3.48}$$

From Equ. (3.46) and (3.48), it is observed that the larger I-PTAT temperature drift of $2I_{VBE}$ is decreased by a PTAT component $2I_{B6}$, while the smaller I-PTAT temperature drift of I_{VBE} is increased by an I-PTAT component $-I_{EC6}$. Hence it is possible for I_{C5} and I_{C6} to exhibit identical temperature drift. By subtracting these two currents, the difference current is obtained as

$$I_{DIF} = I_{C5} - I_{C6} = I_{VBE} + I_{B6} + I_{R6} \tag{3.49}$$

With appropriate adjustments, the temperature drift can be completely removed, and the difference current becomes the temperature independent reference current as

$$I_{REF} = I_{VBE} + \left[\left(\beta_R + 2\right)/\beta_R\right] I_{EC6} \tag{3.50}$$

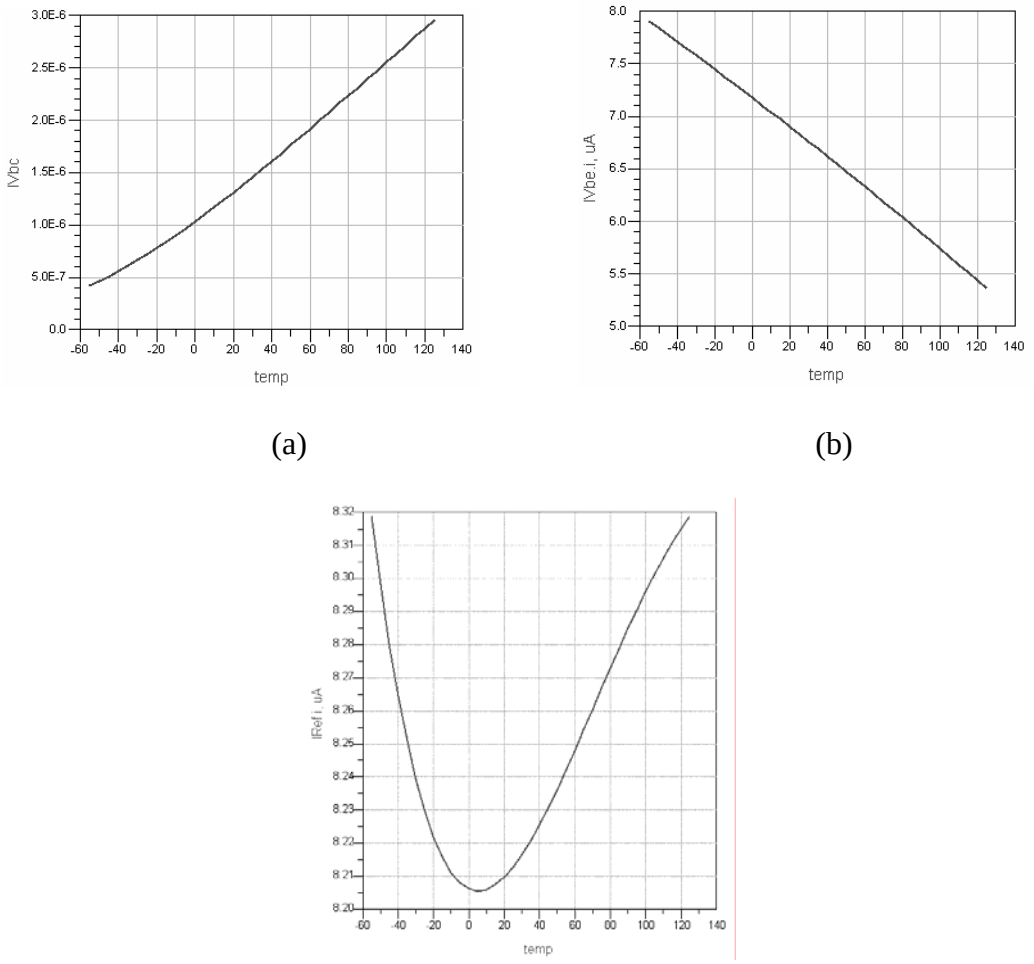
where $I_{VBC} = \left[\left(2 + \beta_R\right)/\beta_R\right] I_{EC6}$ with $B = \left(2 + \beta_R\right)/\beta_R$.

The scaling factor of this I_{VBC} is the same as the one in Equ. (3.23). Its temperature dependences are still given by Equ. (3.24) and (3.25). To find the temperature dependences of this I_{VBC}, only V_{BC} needs to be considered. V_{BC6} is given as

$$V_{BC6} = V_{BE6} - V_{CE6} = V_{BE6} - I_{REF} R_2 \tag{3.51}$$

It is seen basically the temperature dependence of V_{BC6} is completely determined by that of V_{BE6}, which are given in Equ. (2.8) and (2.9). The simulation

result of this design is depicted in Fig. 3.7. I_{REF} presents an average value of 8.253uA with 76.24 $ppm/°C$ deviation.



(a) (b)

(c)

Figure 3.7 Temperature characteristics of I_{VBC} -compensated band-gap reference C (a) temperature variation of I_{VBC} , (b) temperature variation of I_{VBE} , and (c) temperature variation of I_{REF} .

3.3.2 I_{VBC}-Compensated Band-gap Reference D

In the design of Fig. 3.6, those two currents involved in the subtraction are scaled duplicates of I_{VBE}. Instead of I_{VBE}, I_{VT} can be duplicated also. The prototype circuit is depicted in Fig. 3.8. Due to the PTAT characteristics of I_{VT}, Q_5 must be the saturation transistor. If Q_6 is in saturation, the collector currents of Q_5 and Q_6 are still given by Equ. (3.46) and Equ. (3.48) respectively except I_{VBE} is replaced by I_{VT}. Then the larger temperature drift of $2I_{VT}$ is further exaggerated, while the smaller temperature drift of I_{VT} is reduced. With such an enhanced temperature drift difference, subtraction of I_{C5} and I_{C6} cannot generate a temperature independent current.

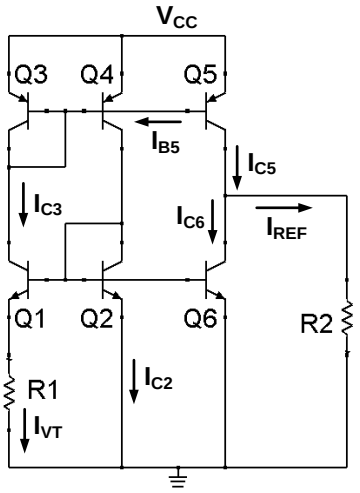


Figure 3.8 Prototype circuit of I_{VBC}-compensated band-gap reference D.

Since Q_5 is in saturation, the collector current of Q_3 is given by

$$I_{C3} = I_{VT} - I_{B5} \tag{3.52}$$

Also this is the collector current of Q_6

$$I_{C6} = I_{VT} - I_{B5} \tag{3.53}$$

and half of I_{CC5}

$$I_{CC5} = 2\left(I_{VT} - I_{B5}\right) \tag{3.54}$$

The collector current of Q_5 is

$$I_{C5} = I_{CC5} - I_{R5} = 2\left(I_{VT} - I_{B5}\right) - I_{R5} \tag{3.55}$$

The difference current as well as the reference current is obtained as

$$I_{REF} = I_{DIF} = I_{C5} - I_{C6} = I_{VT} - \left(I_{B5} + I_{R5}\right) = I_{VT} - \left[\left(\beta_R + 2\right)/\beta_R\right] I_{EC5} \tag{3.56}$$

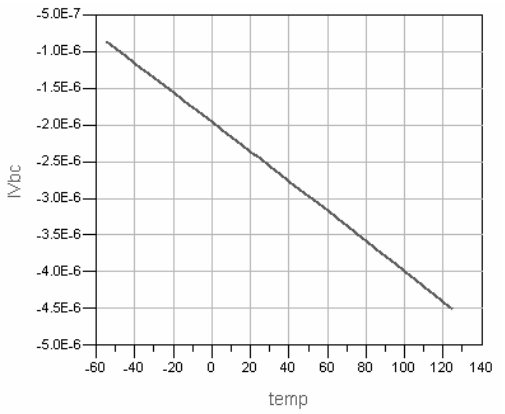
where $I_{VBC} = -\left[\left(2 + \beta_R\right)/\beta_R\right] I_{EC6}$ with $B = -\left(2 + \beta_R\right)/\beta_R$.

Similarly the temperature dependence of this I_{VBC} can be acquired as long as that of V_{BC} is determined. Since V_{CB5} is calculated to be

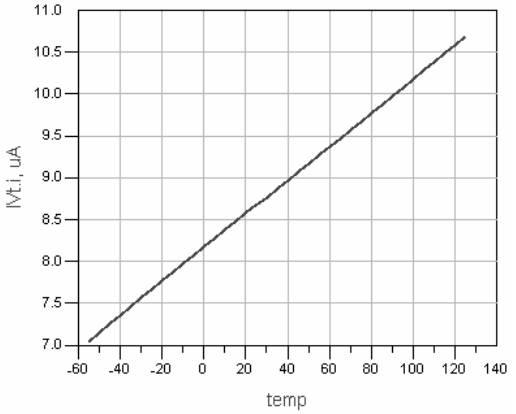
$$V_{CB5} = I_{REF} R_2 + V_{EB5} - V_{CC}\,, \tag{3.57}$$

the temperature dependence of V_{CB5} is same as that of V_{EB5}. The simulation result is depicted in Fig. 3.9. I_{REF} presents an average value of 6.198*uA* with a deviation of 25.24 *ppm*/°*C*.

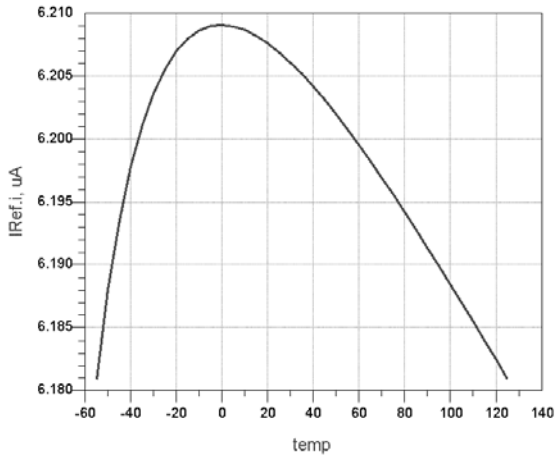
However a drawback exists in this design. For Q_5 being the saturation transistor, V_{CB5} is dependent on the supply voltage as given by Equ. (3.57). So the noise in the supply voltage will have a direct impact on the saturation level of Q_5, and thereby degrade the compensation performance.



(a)



(b)



(c)

Figure 3.9 Temperature characteristics of I_{VBC} -compensated band-gap reference D (a) temperature variation of I_{VBC} , (b) temperature variation of I_{VT} , and (c) temperature variation of I_{REF} .

3.4 Current-Multiplication Reference Designs

Current multiplication scheme is realized using the square-root cell shown in Fig. 2.9. By using the CMOS counterpart of this circuit, a temperature independent

current reference is developed [13]. The measurement results show that the output current has an average 227 *ppm*/°*C* variation for the temperature range of 0°*C* to +75°*C*.

Fig. 3.10 shows a current-multiplication reference design in BJT technology. The square-root cell is composed of Q_1 ~ Q_4. When a V_T -dependent current and a V_{BE} -dependent current undergo the square-root operation, their opposite temperature dependences tend to cancel each other. A temperature independent output reference current can be produced.

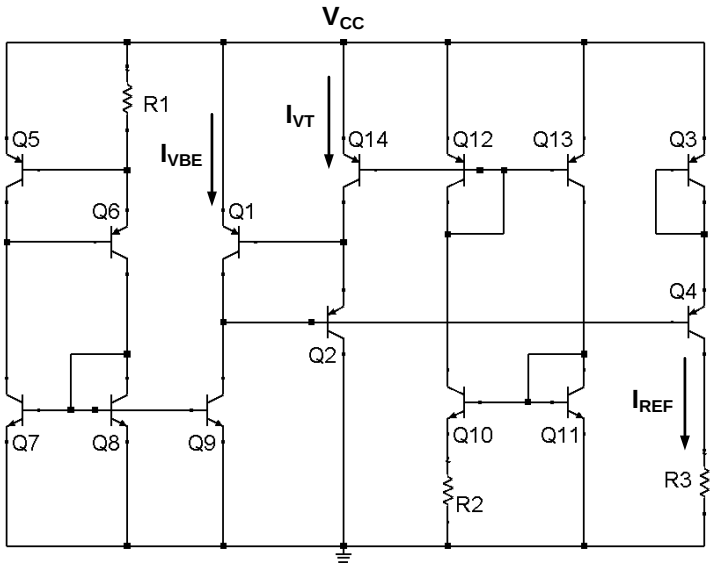


Figure 3.10 Prototype circuit of current-multiplication reference.

Fig. 3.11 shows the simulation result. I_{REF} presents an average value of 7.812*uA* with a deviation of 76.04 *ppm*/°*C*.

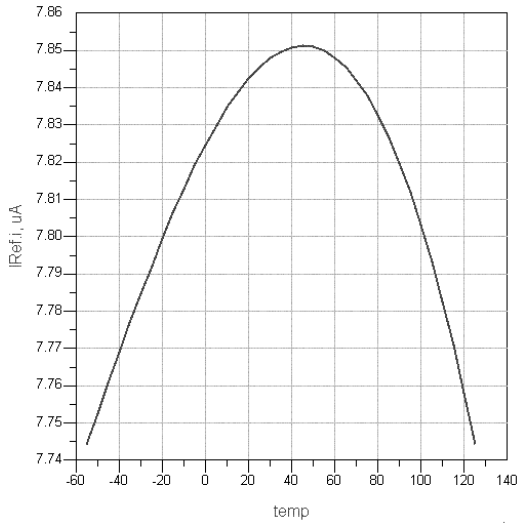


Figure 3.11 Temperature characteristics of I_{REF} of current-multiplication reference.

3.5 Summary

To eliminate higher-order terms and achieve better temperature compensation, nonlinear temperature compensation current is indispensable. In this chapter, an innovative approach is proposed to generate such a current component. The advantage of utilizing V_{BC} -dependent currents for compensation is that no extra circuitry is required. As the complexity of circuits is not increased, the chip area as well as power consumption will remain low. The compensation technique is realized in the I_{VBC} -compensated band-gap reference A, B, C and D. The references A and B are designed based on the current addition scheme, while C and D are based on the current subtraction scheme. All of these four designs have the minimum power supply requirement of $V_{BE} + V_{CE,SAT}$. Then the current multiplication scheme is realized using the core cell illustrated in Chapter II. This design requires the power supply greater than

$2V_{BE} + V_{CE,SAT}$, which leads to higher power dissipation. Table 3.2 summarizes some major aspects of performance considered in this chapter for the five designs. A thorough performance comparison for them will be carried out in chapter IV.

Table 3.2 Summary of band-gap reference circuits simulation results.

	Addition		Subtraction		Multiplication
	A	B	C	D	Square-root
Order of compensation	2nd	2nd	1st	1st	1st
Temperature drift ($ppm/°C$)	44.4	22.4	76.2	25.2	76.0
Mean reference current (uA)	10.2	12.5	8.25	6.20	7.81
Minimum supply voltage	$V_{BE} + V_{CE,SAT}$				$2V_{BE} + V_{CE,SAT}$
Supply voltage (V)	1.5				3
Power dissipation (uW)	91.2	73.0	45.8	44.6	359.5

CHAPTER 4

FUNCTIONALITY ANALYSIS OF REFERENCE CIRCUITS

To evaluate the performance of reference circuits, the temperature independency is a critical issue, which has been the primary concern in the reference circuit designs. Nonetheless there are other issues which are not negligible, such as line regulation, load regulation, power efficiency and noise performance. All these need to be taken into account in assess of the overall performance of a reference circuit, although each issue may have different importance for a specific application. In the case of evaluation of multiple aspects of performance, an obstacle is frequently encountered. Usually when there are several designs to choose from, each design is only good at a certain aspect of performance compared to the others. In other words, each one has different advantages and drawbacks. There is no design with superior performance in every aspect. If each aspect is assumed to have the same importance, which one has the best overall performance? Or equivalently, how should all the aspects be combined together into a single number reflective of the overall performance? In this chapter, a "multiple-to-one" method is developed to numerically characterize all aspects of performance under consideration with one single parameter. In terms of this parameter, the "figure-of-merit" comparison of different designs can be carried out. This method is developed based on the General Systems Performance Theory [24]. A brief introduction of this

theory will begin this chapter. A list of acronyms used in this chapter is given in Appendix D.

4.1 General Systems Performance Theory

The General Systems Performance Theory (GSPT) [24] is a systematic strategy for comprehensive analysis of system performance. It has been widely used in human performance measurement and analysis [25]-[28]. In GSPT, the performance is defined as how well a given structure (or system) executes a specified function. In the case of circuits, the (overall) performance refers to the ability (or quality) of circuit to fulfill the required specifications. The ability to fulfill one specification is one aspect of the overall performance.

The system performance has a multidimensional property, because it may consist of more than one aspect. In GSPT, the system performance is analyzed in the multidimensional performance space (MPS), in which each aspect of performances corresponds to one dimension (i.e., a Dimension of Performance, or DOP). The performance is measured by the value of DOP. For each DOP, a metric is defined so that

- The value is always greater than or equal to zero, and
- A larger value is always considered better performance in this specific aspect.

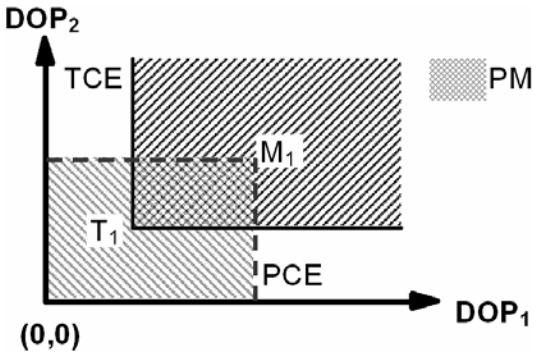
In GSPT, a system is always analyzed with respect to a task. The performance of a system is usually interpreted as the available "resource", and is expressed as R_A for each DOP. The task demand sets the performance goal, in other words, the required "resource" to complete the task, and is expressed as R_D for each DOP. If the system has

better performance than the task demands in each aspect, i.e., $R_A \geq R_D$ for each DOP, the system is able to complete the task. The system is deemed to be "successful" for the specific task. If the system falls short of the demands in any aspect, i.e., $R_A < R_D$ for any DOP, the system fails to complete the task.

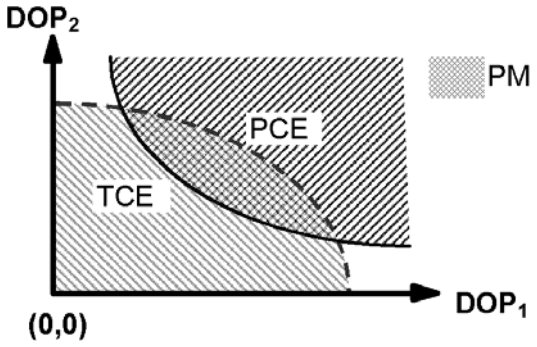
Generally the "success" of a system is determined using either the Performance Capacity Envelope (PCE) and/or the Task Capacity Envelope (TCE). Their definitions follow. Since the system performance in an aspect corresponds to a DOP value, the overall performances can be represented by a point in the MPS. Similarly the task demands in an aspect corresponds to a DOP value, the overall demands can be represented a point in the MPS as well. These two points are named system point and task point respectively.

For example, in the MPS of Fig. 4.1(a), assume "M_1" is a system point and "T_1" is a task point. The x-axis and y-axis values of "M_1" correspond to the system performance in the DOP_1 and DOP_2 respectively. The x-axis and y-axis values of "T_1" correspond to the task demands on the DOP_1 and DOP_2 respectively. There exists an envelope, inside which all the points have smaller values than the system point in each DOP, as shown in Fig. 4.1(a) by the dashed line. This envelope is named the PCE. Similarly the task point determines the TCE, inside which all the points have greater values than the task point in each DOP, as shown in Fig. 4.1(a) by the solid line. If system performances can vary in a certain range, multiple system points will be defined. The PCE formed by these system points may not be rectangular any more, but a curve as depicted in Fig. 4.1(b) by the dashed line. Similarly the task demands can also vary.

Then multiple task points are defined. The TCE formed by these task points may be a curve as depicted in Fig. 4.1(b) by the solid line. The performance and task relationship depicted in Fig. 4.1(a) is for an ideal system, while Fig. 4.1(b) is for a practical system.



(a)



(b)

Figure 4.1 Representation of "success" of a system in the 2-D multidimensional performance space for the (a) ideal case, and (b) practical case. (DOP - Dimension of Performance, TCE - Task Capacity Envelope, PCE - Performance Capacity Envelope, PM - Performance Margin.)

The lower limit of the PCE is always zero, because all DOPs must have positive values. The upper limit depends on the system point(s). The TCE merely has lower limits defined by the task point(s). There are no upper limits due to the-larger-the-better

property of DOP value. Then the "success" of a system can be determined by any of the following criteria:

- If the task point lies inside the PCE, the system is "successful", because the system performance in every aspect is better than what is demanded to accomplish the task. If the point is outside the PCE, that task cannot be accomplished by the system. Or,
- The system point must lie inside the TCE for the "success" of the system. Or,
- An overlap of the PCE and the TCE must exist for the "success" of the system.

Given this perspective, it can be seen readily that if a PCE encloses a larger volume, it can contain more task points, i.e., more tasks can be completed. Therefore this volume, defined as the Composite Performance Capacity (CPC), can be a metric to assess how good a system is. Moreover the quantity of CPC minus the overlap of PCE and TCE manifests how "hard" the system has to work to fulfill the task, or how much capacity the system has to use for the task. On the other hand, the overlap, shown as double-hatched in Fig. 4.1(a), can be regarded as the Performance Margin (PM). It exhibits the excess capacity of the system for the task. Accordingly a larger overlap is preferred.

4.2 GSPT Analysis of Varying Quantity

In order to apply GSPT to the functionality analysis of a system, the metric for DOP needs to be determined first for every aspect of performance under consideration. The performance can be constant or varying quantity. To analyze varying quantities, three methods are suggested in [24]. By considering an example in which the system

performance and task demands are both time-dependent, these three methods are introduced to determine the "success" of the system. In the first method, the condition $R_A(t) \geq R_D(t)$ needs to be satisfied for all time instants over which the task execution occurs. In the second, the worst-case analysis is employed. In a worst-case view of the system, the worst system performance over time, i.e. the minimum value of R_A, is required to be equal to or greater than the maximum task demands over time, that is, $R_A(t)_{\min} \geq R_D(t)_{\max}$. In the third, a statistical consideration is adopted. Such a method would yield predictions of success of the type "success will be achieved certain percent of the time" or "the probability of success is certain percent". Note that, the condition $R_A(t) \geq R_D(t)$ is not satisfied for all time instants in the third method.

In this work another method will be developed, which introduces the concept of Functionality Volume. Based on the Functionality Volume, a new approach to define DOP metric is proposed. With this definition of DOP metric, CPC value is easy to be determined which measures the overall performance the system.

4.2.1 Functionality Volume

Before the concept of Functionality Volume is brought in, it is necessary to define the environmental parameters. Environmental parameters determine the operating conditions, such as temperature, frequency, pressure and etc. All of them can change independently. However not every environmental parameter is concerned in a work. The operating point of a system will be determined by all the environmental parameters of concern. For example, if temperature and frequency are concerned

environmental parameters, an operating point will be determined by specifying a temperature and a frequency, say the system is operating at $25°C$ and $1kHz$.

Considering a hypothetical system, of which the performances vary with operating conditions. For simplicity, assume the operating condition is determined by one environmental parameter. This does not affect the generality of the theory. Then the system performance in any aspect can be described in a two-dimensional space as shown in Fig. 4.2. The x- and y-axis represent the operating condition and performance in the specific aspect respectively.

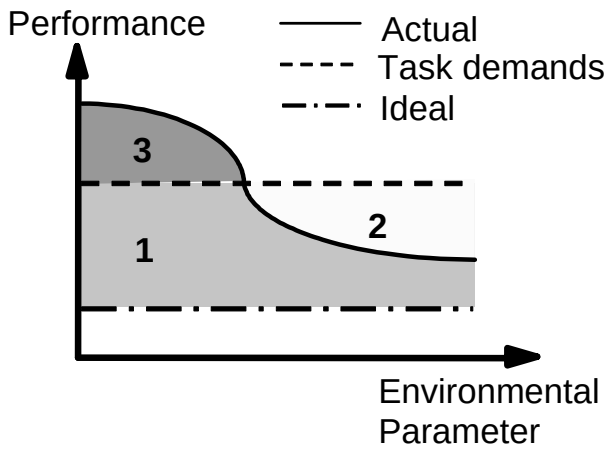


Figure 4.2 Representation of system performance and task demand in the 2-D performance vs. environment space when task demands are not met at all operating points.

Since this kind of space shows how one aspect of performance varies with environmental parameters, they are named performance vs. environment space (PES). In comparison to the MPS in which all the dimensions represent the performance, in the PES, at least one dimension is the environmental parameter. Each aspect of

performance can be represented in a PES, no matter it is varying or constant quantity. The constant quantity will be depicted by straight horizontal line. The varying quantity will be depicted by a curve.

In Fig. 4.2, the actual performance is illustrated by the solid line. The dash-dot line represents the ideal performance. Not surprisingly, the actual performance deviates from the ideal performance. Since the ideal-performance-line and actual-performance-line never converge, there always exists a non-zero area between them. And the larger the deviation from the ideal state, the larger the area. Hence it can be regarded as a "comprehensive" measure of the deviations of reality from ideality in the specific aspect. This area is named the Functionality Volume (FV). (Although it stands for the area in a 2-D PES, and only stands for the volume in a 3-D PES.) In the example of Fig. 4.2, the sum of the area in region 1 and 3 is considered the FV for the specific aspect of performance. For each aspect of performance, the FV can be determined in the corresponding PES. The general definition of FV is given below.

Definitions At every operating point of the system determined by all the concerned environmental parameters, there is a deviation between the actual response and ideal response in a certain aspect. Functionality Volume is defined as the definite integral of the deviations at all operating points. It represents the overall deviations of the system in that aspect. A smaller value of Functionality Volume represents smaller deviations from ideality. If the Functionality Volume is normalized by the concerned range of environmental parameters, it represents the average deviation.

In this definition of FV, what is concerned is merely the absolute value of deviations between actual and ideal performance. Whether the ideal value is greater than or less than the actual value at any operating point, the performance is always considered better as long as the actual performance approaches the ideal performance to reduce the deviations.

It should be noticed that the FV is defined so that a smaller value represents better performance. It does not possess the-larger-the-better property, which is one of the two requirements of DOP metric. Consequently, instead of the FV, its reciprocal value can be adopted as DOP. Nonetheless this choice has disadvantages. Since the system vs. task analysis is carried out in the MPS, only one value can be adopted for each DOP (reciprocal of FV, worst-case value, etc.). As a result, considerable useful information is lost, e.g., the worst-case value does not describe the overall variation of one DOP with respect to the concerned environmental parameters; the FV just stands for the average, and does not reveal the maximum or minimum variation. It will be advisable if the system vs. task analysis is performed before any information is lost. This can be achieved if some pre-analysis is done in the PES. When the task demands are incorporated in this space, another parameter can be developed as the DOP.

4.2.2 Incorporating Task Demands into the PES

The task demands set the required performance on each DOP. It can be depicted as a horizontal line in the 2-D PES, if there are the same task demands at every operating point. In Fig. 4.2, the dash line represents the hypothetical task demands. It is observed that there is also a deviation from the task-demands-line to ideal-performance-

line as represented by the area between them. Like the definition of FV, this area is defined as the Demand Volume (DV). In the example of Fig. 4.2, the sum of the area in region 1 and 2 is considered the Demand Volume for the specific aspect of performance. The Demand Volume specifies the allowed maximum deviation. In other words, a larger Demand Volume corresponds to lower requirements for the system. Then it is easier for the system to fulfill the requirements.

In the Fig. 4.2, the demands are not met at all operating points. The task-demands-line separates the total FV into two portions – Region 1 and Region 3. All the points in the Region 1 have deviations less than the allowed maximum value specified by the task demands. So FV in this region satisfies the demands, and is considered as useful FV. In the Region 3, the deviations of all the points are larger than the allowed maximum value. The FV in this region does not satisfy the demands, and is considered as useless FV.

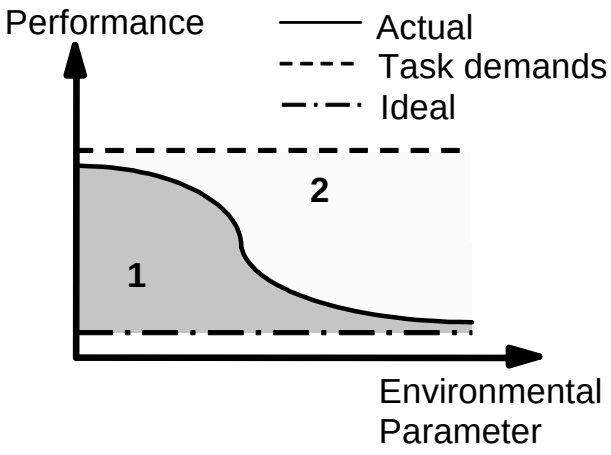


Figure 4.3 Representation of system performance and task demands in the 2-D performance vs. environment space when task demands are met at all operating points.

There is another situation in which the demands are met at all operating points as shown in Fig. 4.3. In this case, all of the FV meets the demands. The useful and total FVs are equal, i.e., the area in Region 1.

In the case when the system does not meet task demands in all operating points, how much the system is able to fulfill the task demands is of interest. While in the case when the system does meet task demands in all operating points, how much excess capacity the system possesses to fulfill the task demands is of interest. Due to this difference, there should be different methods to specify how well the system is able to accomplish the task in one aspect. In the first case, Fulfillment Degree of Demands (FDD) [29] is adopted. It is denoted by the ratio of useful to total FV. The FDD is always less than 1. In the second case, the excess capacity or redundancy is adopted, and is denoted by the ratio of Demand Volume to FV. This ratio is always greater than 1. In conclusion, the metric of DOP will be defined according to the relationship between system performances and task demands as

$$DOP = \begin{cases} FV_{useful} / FV_{total} & \text{task is not completed at all operating points} \\ DV / FV & \text{task is completed at all operating points} \end{cases} \tag{4.1}$$

The definition meets both requirements for DOP metric. It has a threshold value of 1. The value can be interpreted as:

$$DOP \begin{cases} < 1 & \text{the task demands are not satisfied,} \\ = 1 & \text{the task demands are satisfied exactly,} \\ > 1 & \text{the task demands are satisfied with excess.} \end{cases} \tag{4.2}$$

It is worthy of mentioning that this DOP metric may be discontinuous at the threshold value. Consider the example shown in the Fig. 4.2. As the task demands get less restrained (that is, the task-demands-line moves upward away from the ideal-performance-line), or the system performance is improved (that is, the actual-performance-line moves downward to the ideal-performance-line), the useless FV will approach 0, and FDD will approach 1. As soon as the useless FV reduces to 0, task demands begin to be completed in the whole operating range. In this situation, the definition as well as the calculation of DOP will change from FDD to excess capacity. If the excess capacity is greater than 0, the value of DOP will be immediately greater than 1, which implies a significantly improved system performance with respect to the task demands. Thus it can be concluded that the inherent discontinuity of DOP gives much credit to the system which is able to complete the task.

4.2.3 Mapping from PES to MPS

In the previous analysis, the DOP metric is determined. For any aspect, one number is found to represent how well the system functions to fulfill a certain task. Then in the MPS, these multiple numbers can be represented by a single point. The Composite Performance Capacity determined by this point is demonstrated to be a best choice to characterize the overall performance of the system. It is calculated as

$$CPC = \prod_{i=1}^{n} DOP_i \tag{4.3}$$

where $i = 1, 2, \ldots, n$ and n is the total aspects of performance under consideration.

Note that from Equ. (4.3) the CPC is equal to zero if one DOP is zero. Does a zero-valued CPC make any sense? The answer is yes. The reason is no task can be completed if one DOP is equal to zero. The zero-valued DOP is the limiting aspect of performance, which restricts the overall performance of a system.

4.3 System Tradeoff Analysis

The optimization is critical for achieving the best performance of the circuit. For most analog circuits, this process is complicated and difficult because of the multiple conflicting design objectives and performance restrains. For such a multiple-objective design, generally multiple competing objectives cannot be met concurrently. The fulfillment of one objective will cause the degradation of at least one of the other objectives. If there are tradeoffs between the required specifications for a specific type of circuit, the so-called Pareto (also called nondominant or noninferior) solution can be obtained [30] [31]. Typically the Pareto solution is not a unique solution, but a solution set with an infinite number of Pareto solutions. Tradeoffs between some or all of the objectives are involved among these solutions. Nevertheless a quantitative characterization of the tradeoff is nonexistent. The analysis presented next will be aimed at answering the question – how much the tradeoff is.

In the following discussion, characteristics of tradeoff will be analyzed based on a general system instead of any specific circuit. The simplest case will be assumed that the system has two aspects of performance under consideration. The system performances in these two aspects are measured with respect to certain task demands in the corresponding PES respectively. The DOP metric is determined using the method

developed in the last section so that the-larger-the-better criterion is complied. Then both aspects of performance can be represented in a 2-D MPS, in which the tradeoff between them will be analyzed.

4.3.1 Tradeoff Characteristics

If a system is optimized simultaneously for multiple aspects of performance, the relative importance of each aspect can be adjusted by changing its weighting factor [32]. The importance of one aspect of performance will be emphasized with a larger weighting factor, i.e., this aspect of performance will be improved while sacrificing the others. In the case of two aspects of performance, variation of one aspect with respect to the other one can be illustrated by a curve (e.g., the dash-dot line in Fig. 4.4.) in a 2-D MPS. It can be obtained by optimizing two aspects of performance at the same time with different weighting factors.

Let us name these two aspects of performance as Performance A and B. First the weighting factors of Performance A and B are set to 1 and 0 respectively, i.e., the weighting factor ratio of Performance A to B is infinity. Under this condition, Performance A achieves its best result as denoted by the DOP metric value of Max_A, while Performance B is at its worst value. Next the weighting factor ratio is gradually decreased from infinity to obtain the intermediate values, which causes Performance A to degrade from its best value and Performance B to improve from its worst value. When the weighting factors of Performance A and B are set to 0 and 1 respectively, the best Performance B, as denoted by Max_B, and worst Performance A are gained.

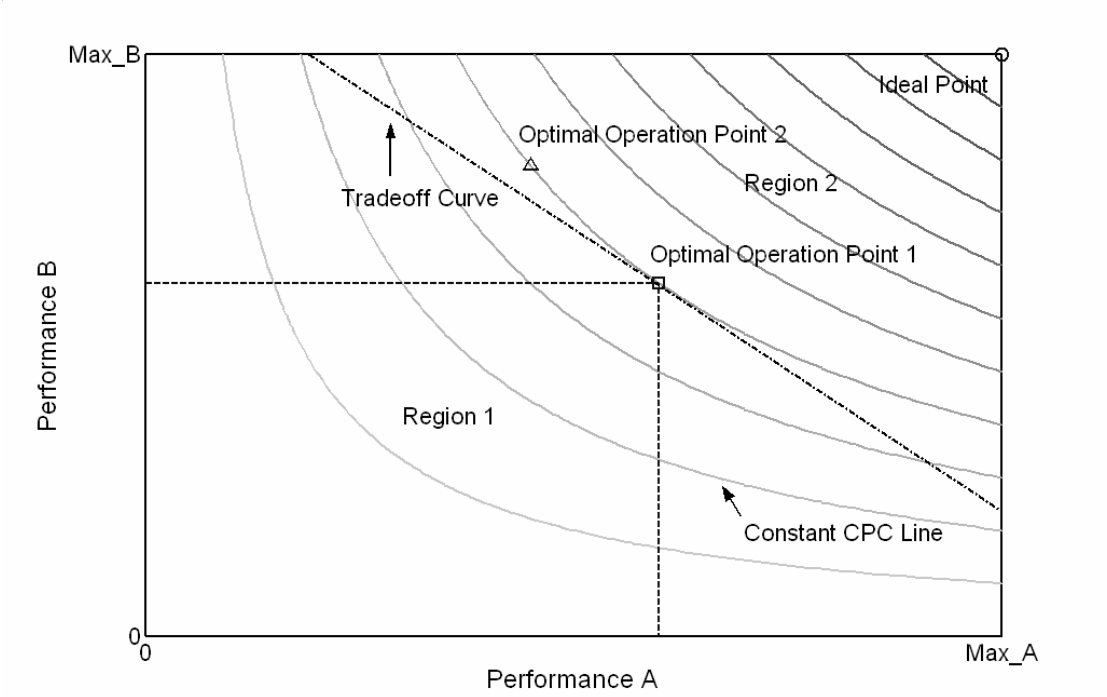


Figure 4.4 Tradeoff Degree determination for a general system in a 2-D multidimensional performance space.

By connecting all the points together a curve is formed as depicted by the dash-dot line in Fig 4.4. We call this curve the tradeoff curve. It shows how one aspect of performance decreases as the other one increases when there is a tradeoff. In the ideal situation no tradeoff exists between performances, i.e., the change of any one of them will not influence the others. The tradeoff curve will be of "rectangular" type, i.e., the ideal tradeoff curve coincides with the axis borderlines. The ideal solution (e.g., as indicated by the symbol "○" in Fig. 4.4.) occurs at the point where all the optimization goals acquire their maximum values concurrently. However there are always deviations between the ideal case and the actual case. As tradeoffs always exist, it needs to quantitatively characterize them for accurate analysis and comparison.

4.3.2 Tradeoff Degree

The tradeoff curve is obtained in the MPS. Each point on the curve corresponds to a certain performance in each aspect, and thereby represents a possible operating point of system. For every operating point, there is a CPC value associated with it. Since a larger CPC value represents better overall performance, the system is desired to work at a point with the largest CPC value, i.e., the system should operate at a point as close to the ideal point as possible. Such an operating point is defined as the optimal operating point. The CPC value associated with it is defined as optimal CPC value. The CPC value associated with ideal point is defined as ideal CPC value.

As the optimal operating point is getting closer to the ideal point, the optimal CPC value will approach the ideal CPC value, which is the theoretical maximum value. Then the tradeoff can be characterized by the Tradeoff Degree (TD), which is defined as the ratio of optimal CPC value to ideal CPC value

$$\mathrm{TD} = \frac{\text{optimal CPC value}}{\text{ideal CPC value}} \tag{4.4}$$

The tradeoff Degree denotes the smallest deviation of operating point from ideal point which a circuit is able to achieve. It is always less than 1. A larger value of Tradeoff Degree is considered better overall performance and less tradeoff.

A general example is illustrated in the Fig. 4.4, where a certain system has two aspects of performance, Performance A and B, with maximum value of Max_A and Max_B respectively. The ideal optimal solution occurs at the point where Max_A and Max_B can be obtained simultaneously as denoted by the symbol "○". Assume the circuit has an optimal operating point somewhere between the maximum values as

indicated with the symbol "□". This optimal operating point 1 defines a dash line, which separates the whole area into two portions – Region 1 and Region 2. The area of Region 1 corresponds to the optimal CPC value, and Region (1+2) corresponds to the ideal CPC value. Then the Tradeoff Degree of the system can be calculated as the area ratio of Region 1 to Region (1+2).

It is worthy of mentioning that this definition of Tradeoff Degree implies the area ratio of all the points on a constant-area line will be identical for a specific ideal point. Therefore, if several optimal solution points happen to be on the same constant CPC line, their tradeoffs will be considered the same. For example, in Fig. 4.4, the tradeoff determined by optimal operating point 1 and 2, as marked by the symbol "□" and "Δ" respectively, will be considered the same, since these two points occur on the same constant CPC line.

4.4 Important Aspects of Performance for Reference Circuits

Typically the band-gap reference is employed as a voltage reference. As a voltage reference, the major specifications can be classified into two categories:

- Static-state specifications include temperature dependence, accuracy, current efficiency, line regulation and load regulation;
- High-frequency specifications include power supply rejection ratio and noise.

4.4.1 Temperature Dependence

The temperature dependence is expressed in *ppm*/°*C* or *ppm*/*K*. Its value depends on the order of temperature compensation. When the temperature range of

interest is larger, the temperature dependence is higher. Ideally this value is equal to zero.

4.4.2 Accuracy

The accuracy is a measure of all the stochastic influences: matching errors of transistors and resistors and variation of process parameters. Usually it is better to select a reference with the required value and accuracy to avoid external trimming and scaling if possible. This allows the best temperature independency to be realized, as high accuracy and low temperature dependence generally go hand-in-hand. In this work, since no specific value is designated for the reference output, the accuracy will not be considered in the following performance analysis and comparison of reference circuits.

4.4.3 Line Regulation

Line regulation measures the ability of the circuit to ignore changes of input voltage. It is defined as the percentage change in output voltage for a specified change in input voltage

$$\text{Line Regulation} : \left(\Delta V_O / V_O\right) / \Delta V_I \tag{4.5}$$

Line regulation is usually specified in *ppm*/*V* of input voltage. It is a steady-state DC measurement. Ideally it is equal to zero.

4.4.4 Load Regulation

Load regulation is a measure of the circuit's ability to maintain the specified output voltage under varying load conditions. Similarly it is defined as the percentage change in V_O for a specified change in I_O

$$\text{Load Regulation} : \Delta V_O / \Delta I_O \tag{4.6}$$

Load regulation is usually specified in *uV*/*mA* or *m*Ω. It should be as small as possible, and ideally is equal to zero.

4.4.5 Current Efficiency

To ameliorate the temperature characteristics of a reference circuit, compensation circuits are added. This usually leads to an increase of the complexity of the reference circuit. And a large amount of current is drawn from the power supply by the compensation circuits. This amount of current is considered as the quiescent current, I_q, which is equal to the difference between supply current and output reference current. Thus the efficiency is limited by the quiescent as follows

$$\text{Current Efficiency}: I_O/\left(I_O + I_q\right) \tag{4.7}$$

The current efficiency is only specified at the nominal operating point. It is a fixed value for a circuit, once the nominal operating point is determined. The current efficiency is an extremely critical property of battery powered products. Battery life is restricted by the total battery current drain. Under the condition that output current is much greater than quiescent current, the operating lifetime of a battery is essentially determined by the output current. On the other hand, effects of quiescent current on battery life are most prevalent if the output current is low compared to the quiescent current, i.e., the current efficiency is low. Consequently current efficiency plays a significant role in designing battery-powered supplies. Ideal current efficiency is equal to 1.

4.4.6 Power Supply Rejection Ratio

Both line regulation and power supply rejection ratio (PSRR) are measures of the circuit's ability to reject the various forms of noise on the incoming supply voltage. But they target at different forms of noise. PSRR measures how well the circuit rejects an AC signal riding on a nominal input DC voltage. Mathematically

$$\text{PSRR}: \delta V_O / \delta V_I \tag{4.8}$$

where δ indicates AC values. PSRR is usually specified in *dB*. PSRR is at a maximum at low frequencies, and begins to fall as the frequency increases, depending upon the design of the circuit.

PSRR is an essential parameter particularly in RF circuitry. In RF communications, low dropout linear regulators (LDOs) are used to generate supply voltages for the RF circuitry. The voltage reference is a critical part in the LDO. The output voltage of the LDO must be especially clean when powering a synthesizer or a voltage-controlled oscillator (VCO). The power supply of the LDO and voltage reference often includes wideband AC ripple superimposed on the DC. It is expected that the ripple is rejected. If the rejection is thorough, an ideal value of PSRR is achieved at negative infinity.

4.4.7 Noise

Noise in reference circuits is quite disadvantageous for those circuits referring their bias quantities to the band-gap reference voltage. Low noise references are important in high-resolution systems to prevent loss of accuracy. Since white noise is statistical, a given noise density must be related to an equivalent peak-to-peak noise in

the relevant bandwidth. Strictly speaking, the peak-to-peak noise in a Gaussian system is infinite (but its probability is infinitesimal). Conventionally, the figure of 6.6×rms is used to define a practical peak value - statistically, this occurs less than 0.1% of the time. This peak-to-peak value should be less than ½ LSB in order to maintain required accuracy [3].

Reference noise is not always specified, and when it is, there is not total uniformity on how. For example, some devices are characterized for peak-to-peak noise in a 0.1 to 10*Hz* bandwidth, while others are specified in terms of wideband rms or peak-to-peak noise over a specified bandwidth. The most useful way to specify noise is a plot of noise voltage spectral density ($nV/\sqrt{Hz}$) versus frequency. Ideally the noise spectral density is zero. Most good IC references have the values around $100\,nV/\sqrt{Hz}$ [3].

4.5 Functionality Analysis of Reference Circuits

The five reference circuits proposed in Chapter III are investigated in terms of the static-state and high-frequency specifications except the accuracy. Their performances are summarized in Table 4.1, where each aspect of performance is still specified in the usual method discussed in Section 4.4. Next these performances are evaluated using GSPT, and described in terms of FV. Each DOP of reference circuit A will be measured first as an example.

First of all, GSPT is applied to characterize the drift of reference current with temperature. Such drift will be described by the relative drift of the reference current

$$\text{Relative drift} = \frac{|\Delta I|}{I_{MEAN}} = \frac{|I_{REF} - I_{MEAN}|}{I_{MEAN}}, \tag{4.9}$$

where I_{REF} is a function of temperature, and I_{MEAN} is the mean value of I_{REF}. In the calculation of effective temperature coefficient, as given by Equ. (1.2), the peak-to-peak variation is normalized by the nominal or mean output as well as the temperature range. In comparison, Equ. (4.9) calculates the relative drift at each temperature point, and is not normalized by the temperature range, since every circuit is simulated in the same range.

Table 4.1 Performance summary of reference circuits.

	Addition		Subtraction		Multiplication
	A	B	C	D	Square-root
Temperature drift ($ppm/°C$)	44.4	22.4	76.2	25.2	76.0
Current efficiency (%)	16.9	25.7	26.9	20.9	6.52
Line regulation (ppm/V)	6,577	9,778	11,802	154,049	19,670
PSRR@1kHz (dB)	-63.1	-58.2	-57.2	-0.368	-55.8
Noise@1kHz ($nV/\sqrt{Hz}$)	55.1	68.9	40.28	63.42	68.9
Load regulation	R_L				

Ideally I_{REF} remains constant at I_{MEAN}, that is, the relative drift is zero. Thus the ideal performance will be represented by a horizontal line as illustrated by the dash-dot line in Fig. 4.5. It overlaps the x-axis. The allowed relative drift, or the task demand, is

set to 0.0018 which corresponds to 10 *ppm*/°*C* in the temperature range from -55°*C* to +125°*C*. In Fig. 4.5, it is represented by the horizontal dash line. The solid curve describes the actual relative drift of reference circuit A. Basically it presents the same variation as the curve in Fig. 3.3(c), except that the negative part of the drift is flipped over the x-axis. The actual performance of the relative drift does not meet the task demands at all points. The total FV is separated into useful and useless FVs, which are labeled as 1 and 3 respectively. The DV equals the sum of the area with label of 1 and 2. In this case, the DOP indicates the FDD. From the first equation in Equ. (4.1), it is calculated to be 0.62.

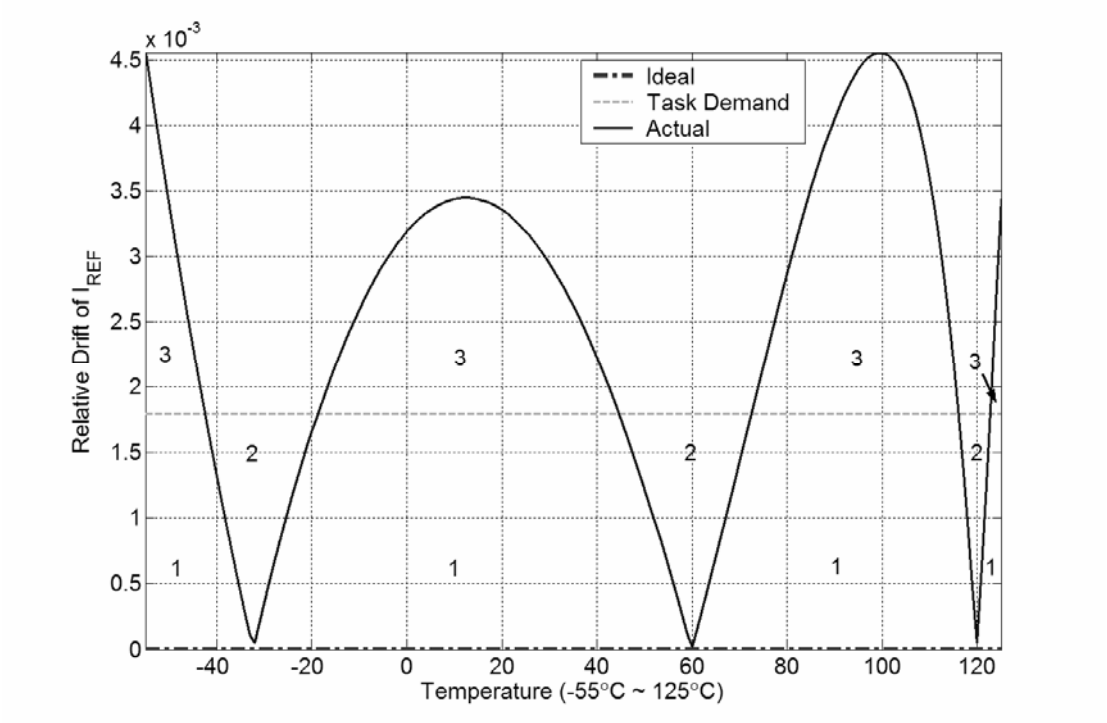


Figure 4.5 Ideal, allowed and actual relative drift of the current of reference circuit A with temperature.

The line regulation is similar to the temperature drift, except that it is the drift of reference current with respect to the supply voltage. So the relative drift of reference current with supply voltage can be calculated by Equ. (4.9) also. But I_{REF} and I_{MEAN} are now functions of supply voltage, instead of temperature. The ideal performance remains at zero relative drift. The task demands are set to 0.000875, which corresponds to 250 *ppm*/*V* for voltage range from 1.5*V* to 5*V*. The actual drift of reference circuit A as well as the ideal and allowed drifts are all shown in Fig. 4.6. Again the task demands are not satisfied at every point, and a FDD of merely 0.14 is obtained.

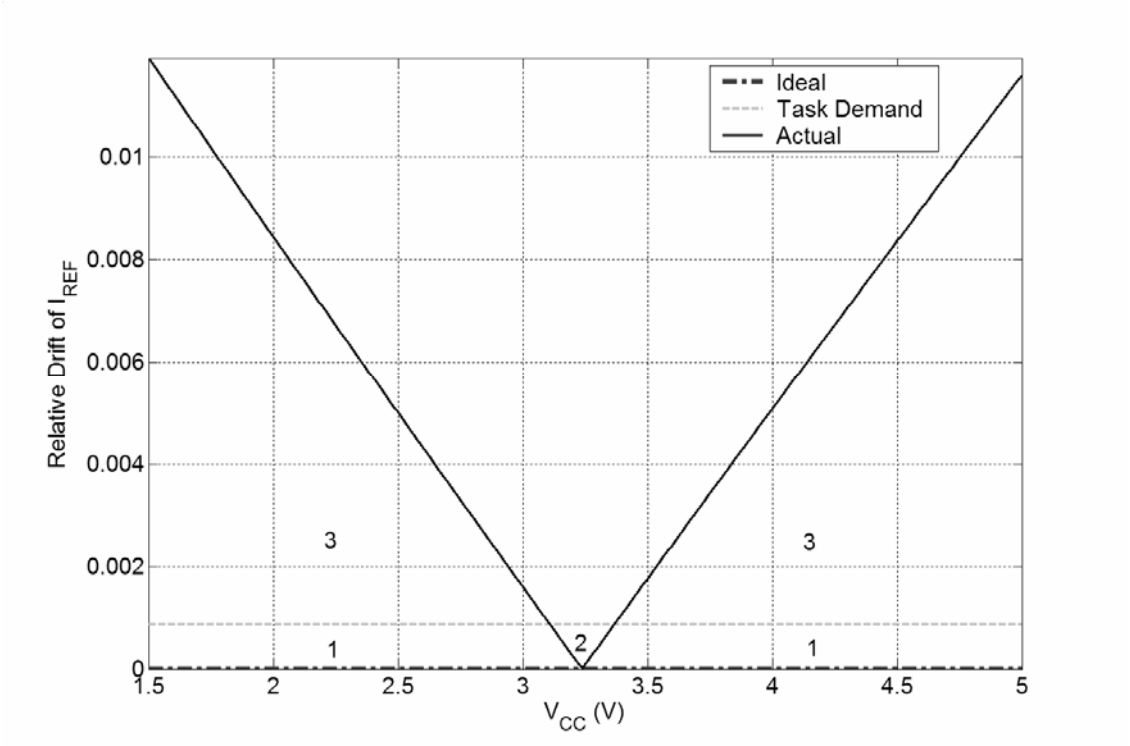


Figure 4.6 Ideal, allowed and actual relative drift of the current of reference circuit A with supply voltage.

The third aspect of performance is PSRR, which changes with frequency. Table 4.1 just lists the PSRRs at 1*kHz* for each circuit. In this analysis, PSRR remains to be calculated by Equ. (4.8). But it is not specified in *dB*. Then the ideal PSRR is zero at all frequencies. The task demands are set to 0.00316 or -50*dB* equivalently. The actual PSRR as a function of frequency for reference circuit A as well as the ideal and allowed PSRR are all shown in Fig. 4.7, and a FDD of 0.66 is acquired.

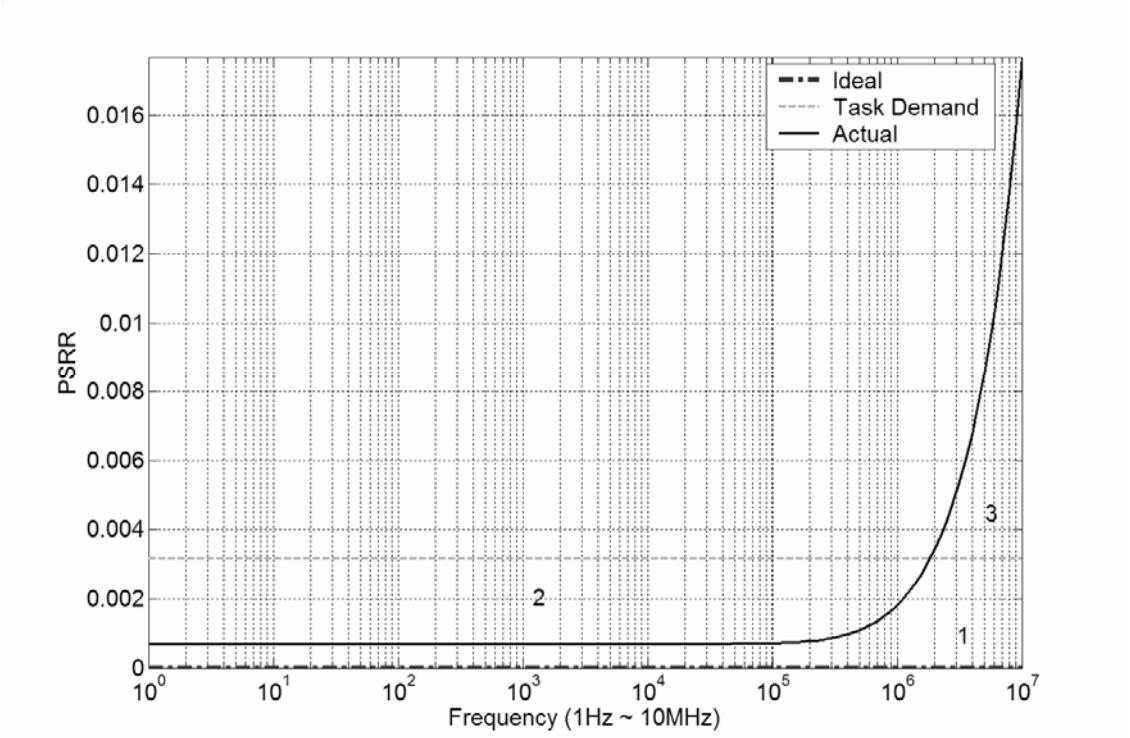


Figure 4.7 Ideal, allowed and actual PSRR of reference circuit A.

Noise spectrum also changes with frequency. Ideally there is no noise at any frequency. For $100\,nV/\sqrt{Hz}$ allowed noise, the FDD of reference circuit A is 0.91 as illustrated in Fig. 4.8.

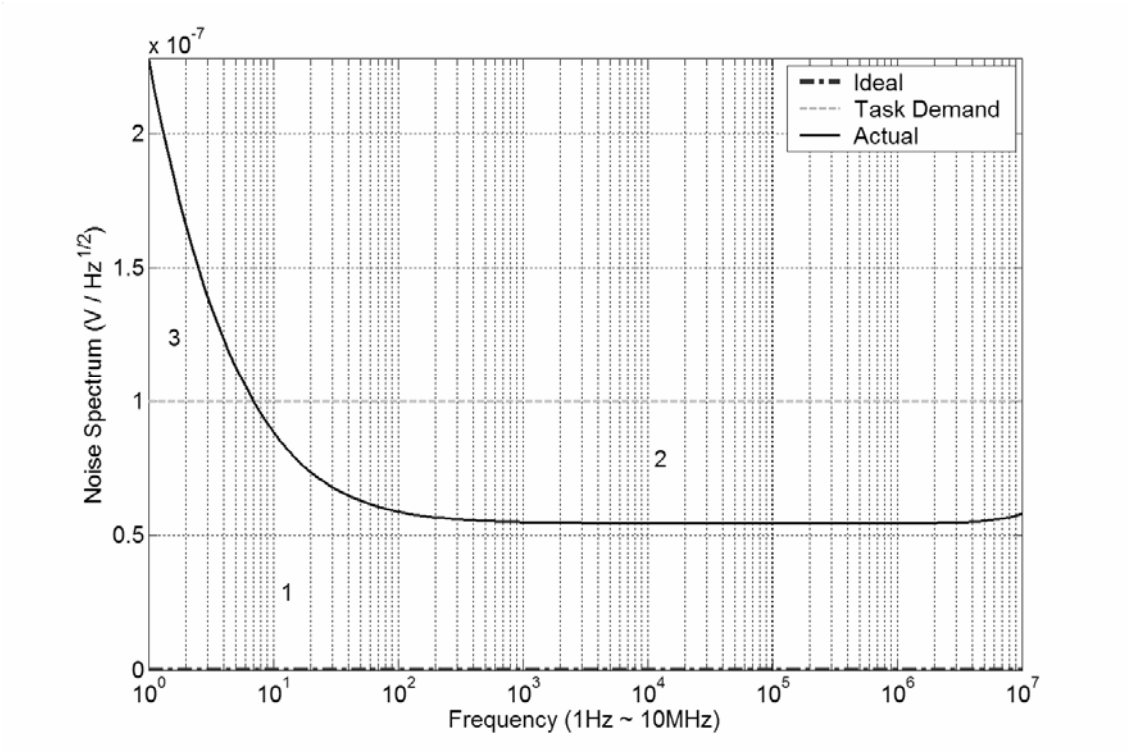


Figure 4.8 Ideal, allowed and actual noise spectrum of reference circuit A.

Unlike the drifts with temperature and supply voltage, PSRR and noise spectrum which are all varying quantities, current efficiency and load regulation have single values for a certain circuit. The evaluation of them is relatively simple. A single-value quantity can be considered as a multiple-value quantity whose values are constant in the concerned operating range. (Strictly speaking, current efficiency and load regulation

also change with operating points. But only the values at nominal conditions are of interest. So these values are assumed at any operating point.) Then the FV of single-value quantity is nothing but the difference between its value and the ideal value multiplied by the operating range. The DV of the task demands for single-value quantity can be calculated in the same way. When the DOP is calculated by either equation in Equ. (4.1), the same operating range existing in both nominator and denominator will be cancelled. Thus, in the case of single-value quantity, FV and DV in Equ. (4.1) can be calculated without multiplying the operating range, in other words, normalized FV and DV are adopted.

Let us see an example, where the current efficiency of reference circuit A is to be evaluated. The ideal current efficiency is unity. The total normalized FV of reference circuit A is the deviation from unity, that is, $1-0.169=0.831$. If the efficiency is required to be higher than 0.5, the normalized useful FV is $1-0.5=0.5$. So reference circuit A has a FDD of approximately 0.60 in the current efficiency. Load regulation, ideally is zero. If the load regulation is preferred being above $100\,\Omega$, reference circuit A will have a FDD of 0.01 for $R_L = 10k\Omega$.

Performances of all the other circuits are evaluated in the same way with the same task demands as those used for reference circuit A. The results are listed in Table 4.2. Since all the circuits have DOP less than unity in every aspect of performance, they are unable to fulfill the specified task demands at all operating points. Nevertheless they present different FDD in each aspect. For instance, reference circuit B has the best temperature drift, PSRR and noise performance; reference circuit C has the best current

efficiency; reference circuit A has the best line regulation. Since all circuits have their reference current applied to the same R_L, they exhibit the same load regulations.

Table 4.2 Functionality comparison of reference circuits.

		Addition		Subtraction		Multiplication
		A	B	C	D	Square-root
DOP	Temperature drift	0.622	0.967	0.414	0.934	0.445
	Current efficiency	0.602	0.673	0.684	0.632	0.535
	Line regulation	0.143	0.107	0.0893	0.00763	0.0868
	PSRR	0.663	0.696	0.624	0.00329	0.136
	Noise	0.910	0.992	0.576	0.967	0.975
	Load regulation	0.0100				
CPC		3.08e-4	4.81e-4	0.909e-4	1.43e-7	0.274e-4

For a circuit, a certain aspect of performance may be the best if measured in the usual way, but may not be if measured using GSPT. This can be observed by comparing the results in Table 4.1 and 4.2. For example, Table 4.1 shows reference circuit A has the best PSRR, but, Table 4.2 shows reference circuit B has the best PSRR. The reason is the PSRR is measured only at one frequency (i.e., 1kHz) in Table 4.1. A best value at one frequency cannot guarantee best values at all frequencies. The variation of PSRR over the whole frequency range needs to be considered to acquire a comprehensive evaluation. This is done using GSPT.

The overall performance is represented by CPC. Reference circuit B exhibits the largest CPC value, or equivalently the best overall performance among all the five circuits under evaluation.

4.6 Summary

This chapter gives an overall functionality analysis of those five reference circuits developed in Chapter III based on the General Systems Performance Theory. This analysis is carried out on reference circuits. But the idea of Functionality Volume and General Systems Performance Theory are developed for general systems, and not limited to a specific type of circuitry. Hence what is done in this chapter can be generalized to fit other types of circuits with slight modifications. What is most important is the appropriate definitions for each DOP, which should be able to contain as much information of the corresponding aspect of performance as possible. Then overall performances of a system can be easily evaluated by the CPC in the MPS. From the design point of view, a larger CPC is regarded as the objective of the design. Therefore the circuit optimization can be performed for maximum CPC.

CHAPTER 5

PERFORMANCE IMPROVEMENTS

Although the I_{VBC}-dependent current components are able to compensate the temperature variation to the second order, the best temperature drift is still above 20 *ppm*/°*C*. This is the result of the high nonlinearity existing in the sum current $I_{VT} + I_{VBE}$ (Fig. 3.4). If the nonlinearity of the first-order compensated sum current is reduced, the final temperature dependence can be further ameliorated. This requires the design of a new current source to generate the I_{VT} and I_{VBE} currents.

The self-biased circuit cells consist of the major parts in the reference circuits. However there is a probability that they do not work at the desired operating point since the operating point may not be stable. So the stability of self-biased circuits should be investigated. Also a startup circuitry is indispensable to ensure the proper operation of self-biased circuits.

5.1 Stability of Self-Biased Circuits

Typically the performance of a circuit should not vary with the power supply. To lower the supply-sensitivity, bias currents in the circuit need to depend on a voltage other than the supply voltage. The most convenient voltage standards by which the bias currents are produced include the base-emitter voltage of a BJT transistor (V_{BE}), the

threshold voltage of a MOS transistor (V_{TH}), the thermal voltage (V_T) and the breakdown voltage of a reverse-biased *pn* junction which is usually a Zener diode [1]. In BJT technology, V_{BE} and V_T references are most widely used. All the bias currents (the compensation currents not included) in the circuit proposed in Chapter III depend either on V_{BE}, V_T or a combination of them.

Typically self-biased circuits are formed by connecting a current mirror to the V_{BE} or V_T current source as illustrated in Fig. 5.1. Such a topology establishes a positive feedback loop, in that this loop responds to any change in the current by a further change of the current in a direction which reinforces the initial change.

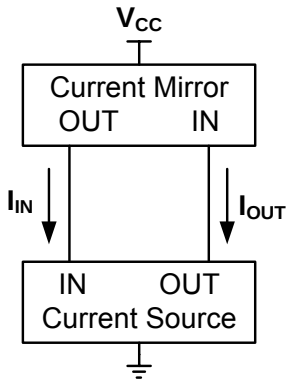


Figure 5.1 Block diagram of a self-biased reference [1].

It is also well known that this topology may effect two potential operating points [1]. One is the so-called “dead” operating point at which all the bias currents are almost zero. The other one is the normal operating point at which the circuit is desired to operate. Ordinarily both of these two operating points are stable. The stability can be

tested using the Nyquist criterion, which states that a circuit with positive feedback is stable if the loop gain is less than unity [1]. The loop gain of a self-biased circuit is basically determined by the gain of the current source, since the gain of the current mirror is usually unity. In other words, if the gain of the current source is less than unity, the whole self-biased circuit will be stable. Next the stability of self-biased circuits will be investigated by calculating the gain of each current source.

5.1.1 Self-Biasing V_{BE} Reference

The V_{BE}-biased current reference is shown in Fig. 5.2 [1].

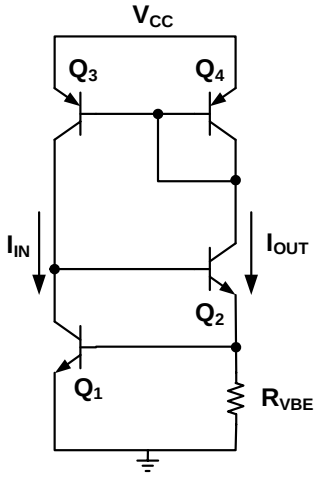


Figure 5.2 Self-biasing V_{BE} reference.

If the base currents are ignored, it is easy to find I_{OUT}

$$I_{OUT} = \frac{V_T}{R_{VBE}} \ln\left(\frac{I_{IN}}{I_S}\right) \tag{5.1}$$

By taking the derivative of I_{OUT} with respect to I_{IN}, the gain of the V_{BE}-biased current reference is found as

$$G_{VBE} = \frac{\Delta I_{OUT}}{\Delta I_{IN}} = \frac{dI_{OUT}}{dI_{IN}} = \frac{V_T}{I_{IN} R_{VBE}} \tag{5.2}$$

The positive feedback formed by the current mirror forces $I_{IN} = I_{OUT}$. So $I_{IN} R_{VBE}$ can be replaced by $I_{OUT} R_{VBE}$ which is equal to V_{BE1}. We can see that the gain is actually equal to the ratio of V_T to V_{BE1}. Since this ratio is definitely much less than unity, the V_{BE}-biased current reference is stable at the desired operating point.

Furthermore transistor Q_2 is capable of stabilizing the circuit operation. Q_2 and R_{VBE} form a structure of common emitter with emitter degeneration, where R_{VBE} is called the emitter degeneration or emitter ballasting resistor. If there is an increment of I_{OUT} for any reason, the voltage across resistor R_{VBE}, or equivalently the emitter voltage of Q_2, will increase. As a result, the base-emitter voltage of Q_2 is reduced, mandating lower current flowing through it. Therefore the initial change is counteracted. But a drawback of adding Q_2 is the minimum supply voltage is increased from $V_{BE} + V_{CE,SAT}$ to $2V_{BE} + V_{CE,SAT}$.

5.1.2 Self-Biasing V_T Reference

The classical V_T-biased current reference is shown in Fig. 5.3(a) [1].

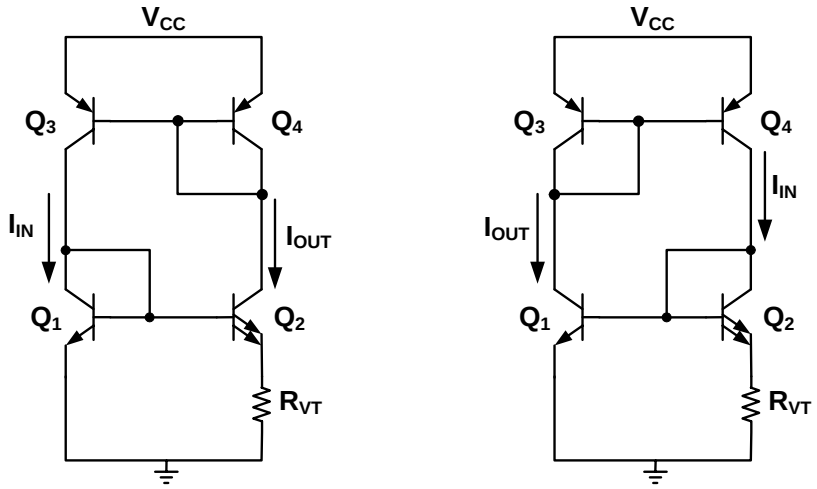
A simple analysis will show that the relationship between I_{IN} and I_{OUT} is given by

$$I_{OUT}R_{VT} = V_T \ln\left(\frac{I_{IN}}{I_{OUT}} \cdot \frac{I_{S2}}{I_{S1}}\right) \tag{5.3}$$

Similarly the gain is found by calculating derivative of I_{OUT} with respect to I_{IN}

$$G_{VT(a)} = \frac{dI_{OUT}}{dI_{IN}} = \frac{1}{\frac{R_{VT}}{V_T} I_{IN} + \frac{I_{IN}}{I_{OUT}}} \tag{5.4}$$

In the situation of $I_{IN} = I_{OUT}$, the gain is less than unity, which makes the V_T-biased current reference in Fig. 5.3(a) stable.



(a) (b)

Figure 5.3 Self-biasing V_T reference with (a) Widlar current source and (b) inverse Widlar current source.

In Fig. 5.3(a), the V_T-dependent current is generated by a Widlar current source. Actually the inverse Widlar current source is also able to generate such a current with

the help of current mirror. The implementation is illustrated in Fig. 5.3(b). It is found that I_{IN} and I_{OUT} are related as

$$I_{IN}R_{VT} = V_T \ln\left(\frac{I_{OUT}}{I_{IN}} \cdot \frac{I_{S2}}{I_{S1}}\right) \tag{5.5}$$

Notice that Equ. (5.3) and (5.5) are basically the same except that I_{IN} and I_{OUT} are switched, which implies that the derivative of I_{OUT} with respect to I_{IN} is the reciprocal of Equ. (5.4) with I_{IN} and I_{OUT} interchanged

$$G_{VT(b)} = \frac{1}{G_{VT(a)}} = \frac{R_{VT}}{V_T} I_{OUT} + \frac{I_{OUT}}{I_{IN}} \tag{5.6}$$

In the situation of $I_{IN} = I_{OUT}$, the gain is greater than unity, which means the V_T -biased current reference with inverse Widlar current source is unstable at the desired operating point.

More insight can be gained by comparing the transfer characteristics of Widlar and inverse Widlar current source. For both of them, the output current increases monotonically as the input reference current increases [34] as depicted qualitatively in Fig. 5.4. For a certain amount of change in the input current, however, the inverse Widlar current source presents more change in the output current than the Widlar current source. This is why the inverse Widlar current source is sometimes useful to bias stages at very high-gain currents.

The representative transfer characteristics of a current mirror with a resistive load (R_L) are also depicted in Fig. 5.4. For the current mirror, I_{OUT} is the input

reference current, while I_{IN} is the output current. When I_{OUT} is small, I_{IN} tracks I_{OUT} as expected. As I_{IN} continues to increase, the output transistor is driven into saturation. Then I_{IN} stops increasing with I_{OUT}, and remains almost constant at I_{SAT} which is approximately equal to $\left(V_{CC} - V_{CE,SAT}\right)/R_L$.

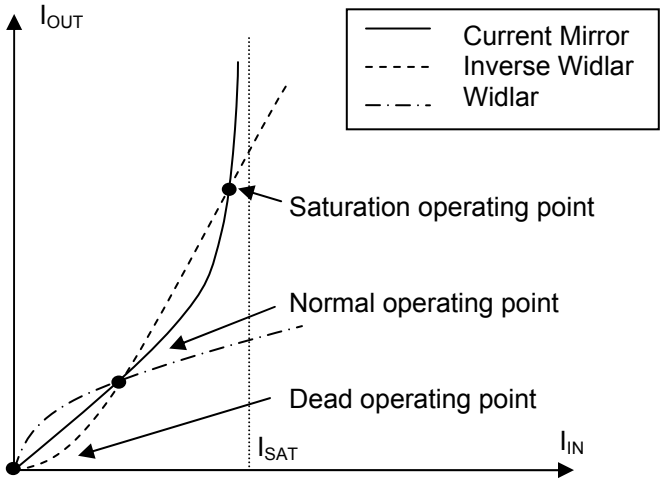


Figure 5.4 Determination of the operating points for the self-biasing V_T references.

By drawing all the transfer characteristics in one figure, the operating point can be determined. It is observed that there are two operating points for the V_T-biased current reference with Widlar current source, and three operating points for that with inverse Widlar current source. The analysis earlier in this subsection shows that the inverse-Widlar-based design is unstable at the desired operating point. It may drift to the third operating point. Fig. 5.4 shows that this point is reached when the output transistor of current mirror is in saturation. Simulation results show that actually the

output transistors of both current mirror and inverse Widlar current source are in saturation at the third operating point. Thereby this operating point is named the saturation operating point. Table 5.1 lists the all the potential operating points of both self-biasing V_T references when $R_{VT} = 5K$. Due to the intrinsic instability, use of the V_T-biased current reference with inverse Widlar current source should be avoided.

Table 5.1 Operating points of self-biasing V_T reference with Widlar and inverse Widlar current sources when $R_{VT} = 5K$.

Operating Point	Dead		Normal		Saturation
	Widlar	Inverse Widlar	Widlar	Inverse Widlar	Inverse Widlar
I_{IN}	≈ 0	≈ 0	$3.328uA$	$3.846uA$	$1.074mA$
I_{OUT}	≈ 0	≈ 0	$3.381uA$	$3.908uA$	$4.173mA$

5.1.3 Self-Biasing $V_T + V_{BE}$ Reference

In Chapter III, I_{VBC}-compensated band-gap reference A and B employ a current reference in which the bias current is the sum of V_T- and V_{BE}-dependent currents. The circuit is repeated in Fig. 5.5.

I_{VT} and I_{VBE} have been already given by Equ. (3.15) and (3.16) respectively. But they need to be rewritten in terms of I_{IN} and I_{OUT} to find the relationship between I_{IN} and I_{OUT}

$$I_{VT} = \frac{V_T}{R_{VT}} \ln\left(\frac{I_{OUT}}{I_{VT}} \cdot \frac{I_{S1}}{I_{S2}} \right) \tag{5.7}$$

$$I_{VBE} = \frac{V_T}{R_{VBE}} \ln\left(\frac{I_{OUT}}{I_{S2}}\right) \tag{5.8}$$

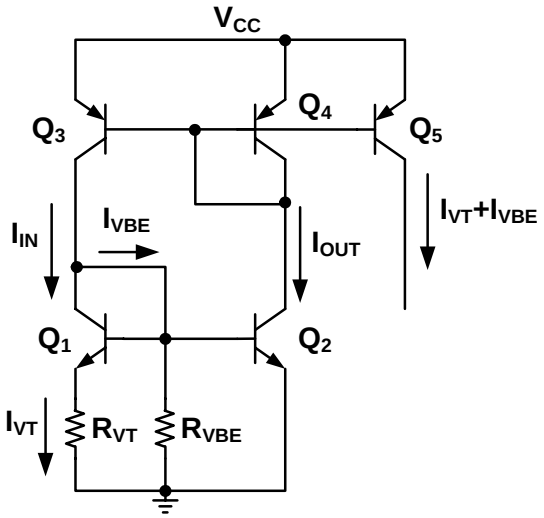


Figure 5.5 Self-biasing $V_T + V_{BE}$ reference A.

Since I_{IN} is approximately the sum of I_{VT} and I_{VBE}, I_{VT} can also be written as

$$I_{VT} = I_{IN} - I_{VBE} = I_{IN} - \frac{V_T}{R_{VBE}} \ln\left(\frac{I_{OUT}}{I_{S2}}\right) \tag{5.9}$$

Substitute Equ. (5.9) into Equ. (5.7) for I_{VT} to find the relationship between I_{IN} and I_{OUT}

$$I_{IN} - \frac{V_T}{R_{VBE}} \ln\left(\frac{I_{OUT}}{I_{S2}}\right) = \frac{V_T}{R_{VT}} \ln\left[\frac{I_{S1}}{I_{S2}} \cdot \frac{I_{OUT}}{I_{IN} - \frac{V_T}{R_{VBE}} \ln\left(\frac{I_{OUT}}{I_{S2}}\right)}\right] \tag{5.10}$$

Then the gain is ready to be calculated as

$$G_{VT+VBE} = \frac{dI_{OUT}}{dI_{IN}} = \frac{I_{OUT}}{\frac{V_T}{R_{VBE}} + \frac{I_{VT}}{1 + \frac{I_{VT} R_{VT}}{V_T}}} \tag{5.11}$$

It is obvious that $V_T / R_{VBE} < I_{VBE}$ and $I_{VT} / \left(1 + I_{VT} R_{VT} / V_T\right) < I_{VT}$. The denominator of Equ. (5.11) is less than $I_{VT} + I_{VBE}$, or equivalently I_{OUT}. Since this gain is greater than unity, the self-biasing $V_T + V_{BE}$ reference in Fig. 5.5 is unstable.

As alternatives to the design in Fig. 5.5, the two designs depicted in Fig. 5.6 and 5.7 can be adopted. The design in Fig. 5.6 is nothing but a direct combination of Fig. 5.2 and Fig. 5.3(a). The design in Fig. 5.7 still employs the Widlar configuration of Fig. 5.3(a) to generate the PTAT current, I_{VT}. This current is mirrored to Q_5. Then an I-PTAT current, I_{VBE}, is generated proportional to the base-emitter voltage of Q_5. I_{VT} and I_{VBE} are added together as they flow into Q_6, and finally Q_9. Both alternative designs are stable. Moreover they will not have any influence on the temperature analysis or equations accomplished in Chapter III.

However the design in Fig. 5.5, 5.6 and 5.7 differ dramatically in their second-order temperature drift. When each of them generates a first-order compensated 10*uA* current, Fig. 5.8 compares the second-order temperature drift of these three designs. The circuit in Fig. 5.7 presents the lowest drift of 11.40 *ppm*/°*C*, followed by 19.93 *ppm*/°*C* drift of Fig. 5.6 and 85.04 *ppm*/°*C* drift of Fig. 5.5. Since a smaller second-order temperature drift of $I_{VT} + I_{VBE}$ will ease the later second-order compensation, in the

final design, $I_{VT} + I_{VBE}$ will be implemented by Fig. 5.7 which presents the smallest second-order temperature drift among them.

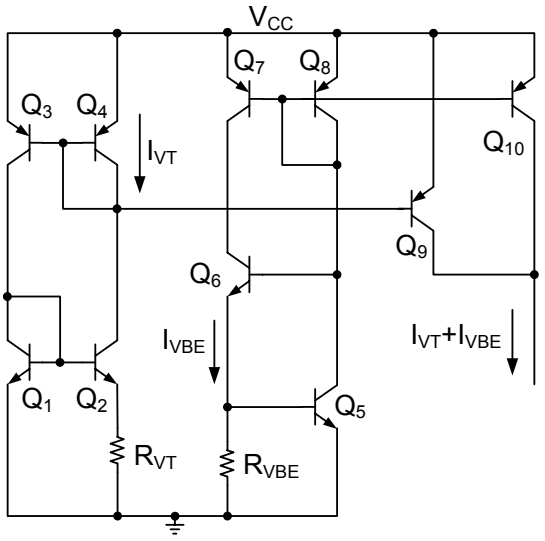


Figure 5.6 Self-biasing $V_T + V_{BE}$ reference B.

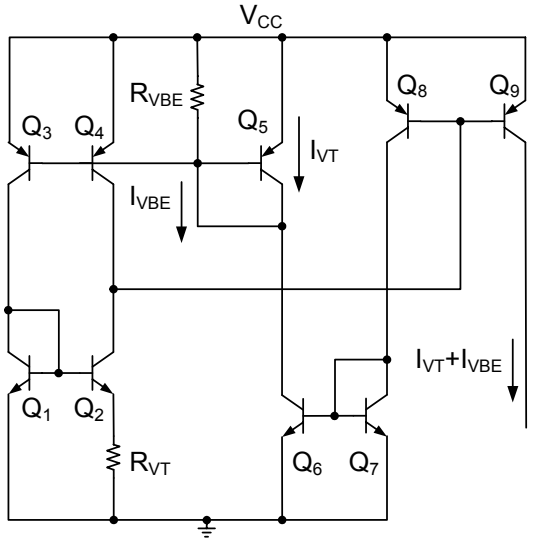


Figure 5.7 Self-biasing $V_T + V_{BE}$ reference C.

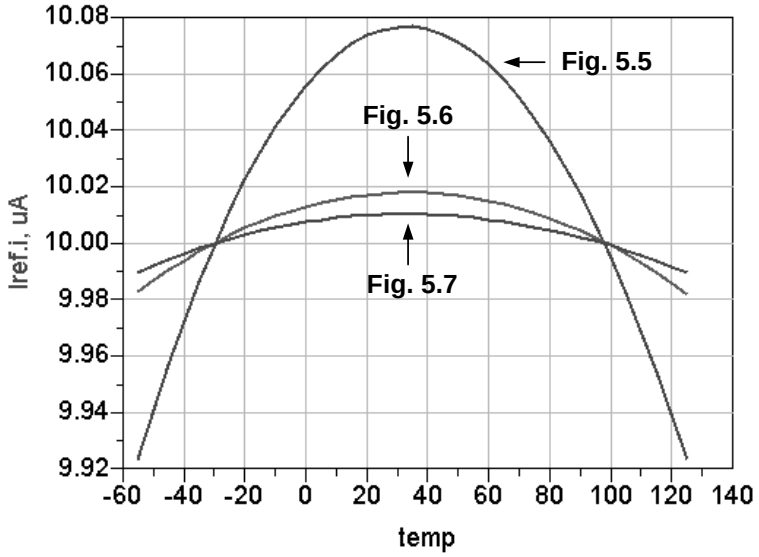


Figure 5.8 Comparison of second-order temperature drift of $I_{VT} + I_{VBE}$ designs.

5.2 Startup Circuitry

Startup circuitry plays a significant role in the reference circuitry. It brings out a reference circuit from the dead zone and ensures the reference circuit to operate at the normal operating point by injecting some current into the core circuit. Once the desired operating point is reached, it is disconnected so as not to interfere with the normal operation of the core circuit. In addition to these basic requirements, it is better if the startup circuit is able to inject a higher amount of current during startup and shut itself off completely after disconnection. Higher injection current is required for a fast startup of the reference circuit. If the startup circuit is not turned off completely and continues to consume constant current after initial startup, the total power consumption of the circuit will increase. This is critical in a battery-operated condition.

5.2.1 Design Principles

The startup circuit needs to be turned on once the power supply is turned on. To meet such a requirement, at least one transistor in the startup circuit needs to operate in the active region. Commonly this is guaranteed by means of putting one or more diode-connected BJT or MOS transistors in series with a resistor [1] [12] [35] [36] (In the case of MOS implementation, the resistor may not be necessary.). A second method involves biasing the gate of NMOS with the power supply [16] [37] or a voltage close to the power supply [38] [39]. A third method involves connecting the gate of a PMOS with ground [40] or a voltage close to ground [1] [41]. These three methods are illustrated in Fig. 5.9 respectively.

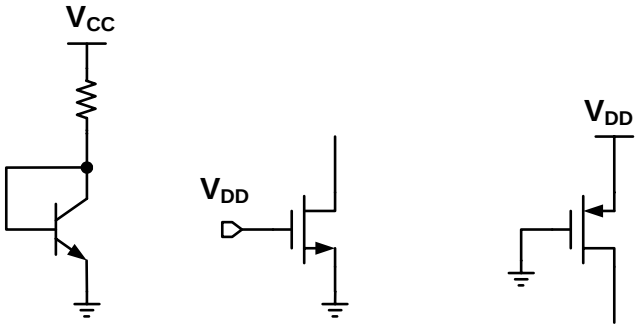
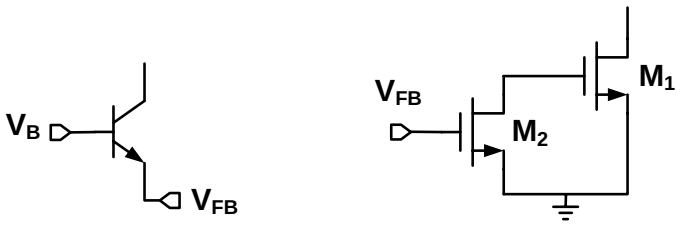


Figure 5.9 Circuit topologies with guaranteed startup (a) first method, (b) second method, and (c) third method.

When the reference circuit begins to operate normally, the startup circuit becomes useless. Then the reference circuit should feedback a voltage to disconnect itself with the startup circuit. In BJT technology, such a disconnection is accomplished

by decreasing the base-emitter voltage of the BJT transistor connecting both circuits [35]. For example, the feedback voltage (V_{FB}) can be applied to the emitter of the "bridge" transistor as shown in Fig. 5.10(a). Initially the feedback voltage is almost zero. As the feedback voltage rises to its normal value, the "bridge" transistor is turned off. Similarly in MOS technology, the gate-source voltage is reduced below the threshold voltage for disconnection. However this is achieved in a different way. Fig. 5.10(b) shows a popular approach adopted in most designs [1] [37] [38] [39] [40] [41]. Usually M_1 begins to conduct startup current as soon as the power supply is turned on. M_2 remains off due to the low feedback voltage. This voltage will increase as the reference circuit approaches its normal operating point. After it arrives at a value greater than the threshold voltage of M_2, M_2 is turned on. Since there is no current flowing through M_2, its drain-source voltage needs to be zero. This will pull down the gate voltage of M_1, and turn off M_1 finally.



(a) (b)

Figure 5.10 Circuit topologies to achieve disconnection (a) first method, and (b) second method.

An example of a BJT startup circuit is illustrated in Fig. 5.11. Its topology as well as startup process is similar to that of the inverter-based startup circuits in CMOS

technology [1], except that large degeneration resistors are inserted at the emitter of all the transistors in the startup circuit. Without these resistors, the core circuit will not be able to work at the desired point. Suppose Q_{S1} is not emitter-degenerated. After startup, Q_{S1} works in the saturation region with a large base current which will interfere with the normal operation of the core circuit. A large R_{S1} can limit the base-emitter voltage, thereby the base and collector current of Q_{S1}. Resistors R_{S2} and R_{S3} limit the base-emitter voltage of Q_{S2} and Q_{S3} respectively. Without R_{S3}, Q_{S3} cannot shut down and keeps injecting current into the core circuit in the post-startup period. The simulated startup process, obtained with all the degeneration resistors set to 200*k*, is depicted in Fig. 5.12.

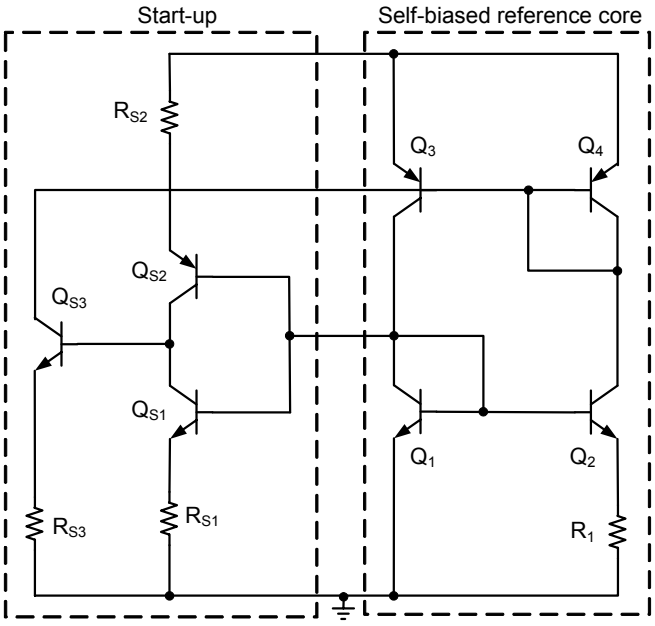


Figure 5.11 BJT implementation of inverter-based startup circuit.

Once disconnected, the startup circuit should not consume any current in the standpoint of low power design. This is especially a challenge for the design of a circuit with guaranteed startup. Notice that there is always quiescent current flowing in the design of Fig. 5.9(a) and Fig. 5.11. The quiescent current in Fig. 5.9(b) and 5.9(c) can be eliminated by forcing zero drain-source voltage after startup. An alternative solution is to design in a capacitive approach [42].

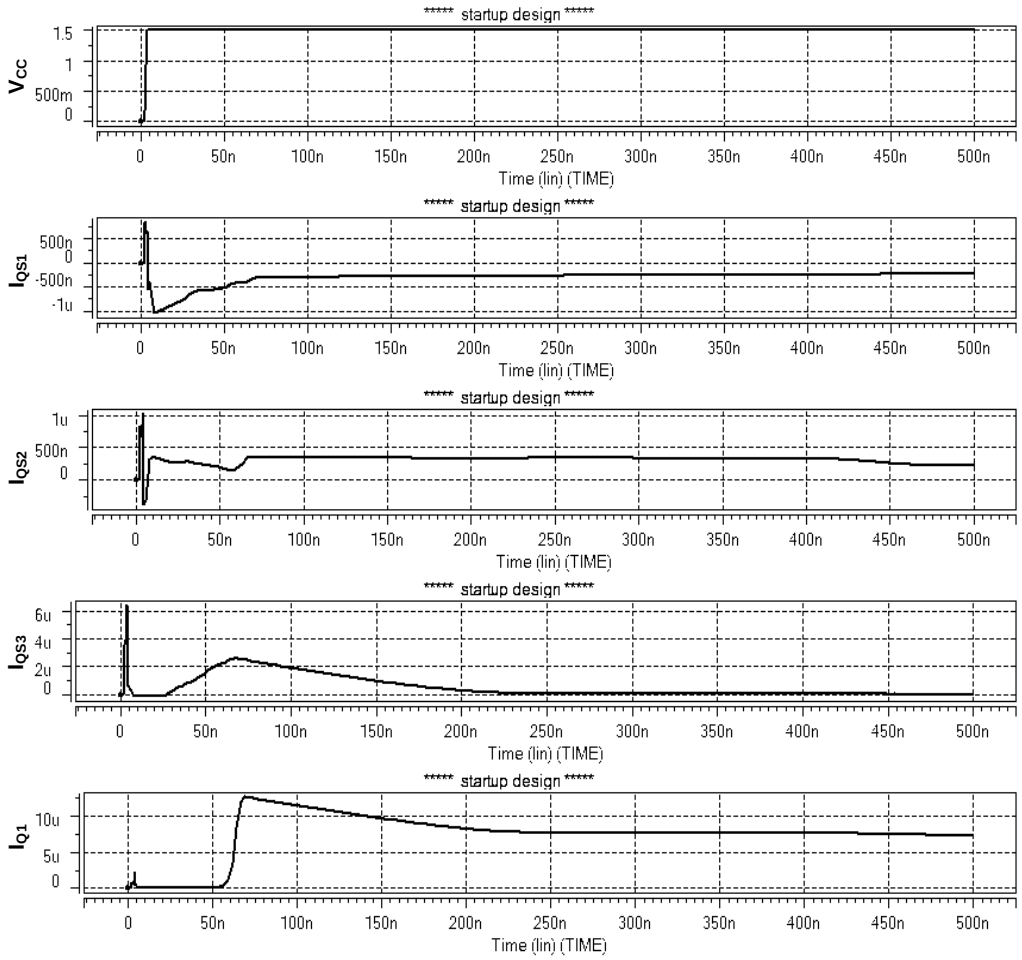


Figure 5.12 Startup process of BJT implementation of inverter-based startup circuit.

5.2.2 Capacitive-Approach Design

A capacitive startup circuit is shown in Fig. 5.13. The self-biasing V_T reference with Widlar current source has been taken as an example for simulation purpose. This will not affect the generalness of the design.

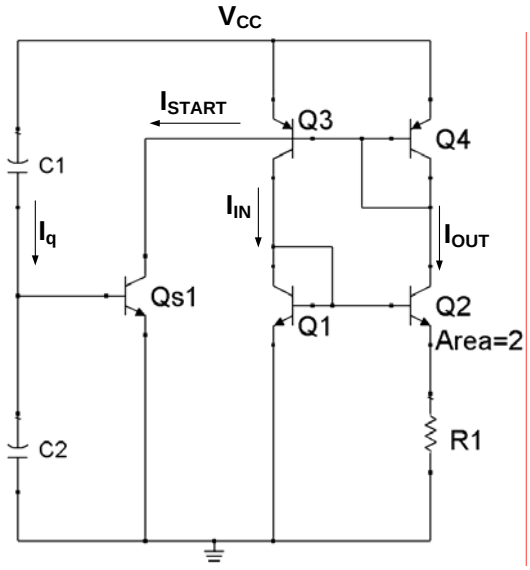


Figure 5.13 Capacitive startup circuit design.

Capacitors C_1 and C_2 form a voltage divider. When V_{CC} is ramping up from $0V$, the base voltage of Q_{S1} follows V_{CC} by $V_{CC}[C_1/(C_1+C_2)]$. The value of C_1 and C_2 is chosen in such a way that the divided voltage is high enough to turn on Q_{S1}. When Q_{S1} is turned on, a startup current, I_{START}, will begin discharging the base of Q_3 and Q_4 towards ground. Then the reference circuit is started. When V_{CC} remains constant, no current will flow into the base of Q_{S1}, mandating the startup current to drop to zero. The

startup circuit is disconnected, and consumes no more power. This entire process is illustrated in Fig. 5.14.

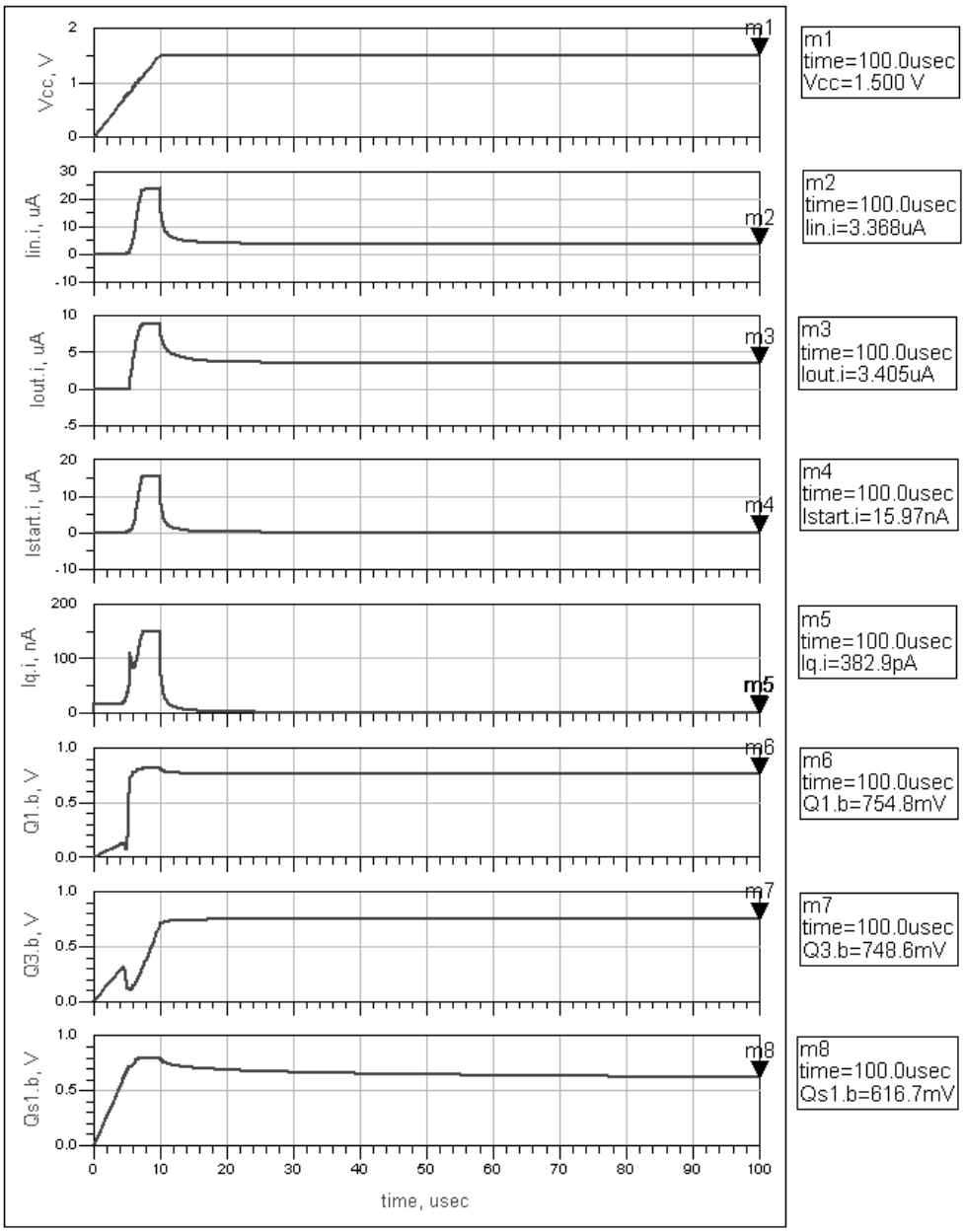


Figure 5.14 Startup waveforms of the capacitive startup circuit.

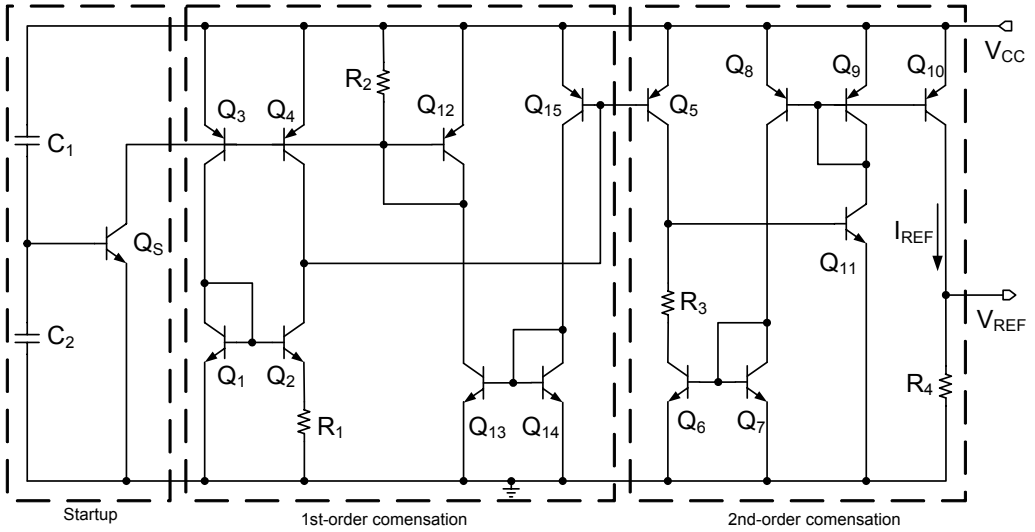
Because transistor Q_{S1} is turned off during the normal operation of the circuit, noise from the power supply will not be coupled to the core circuit through capacitances C_1 and C_2. This startup circuit will not deteriorate the noise performance.

One drawback of the design is the value of C_1 and C_2 is dependent on V_{CC}. The reason is for certain V_{CC}, the capacitors value is selected such that enough voltage can be applied at the base of Q_{S1}, e.g., at least $0.7V$. As V_{CC} decreases, the divided voltage may become lower than the required voltage, and unable to turn on Q_{S1}. Therefore, the ratio of C_2 to C_1 can only be chosen to ensure normal start-up for certain range of V_{CC}.

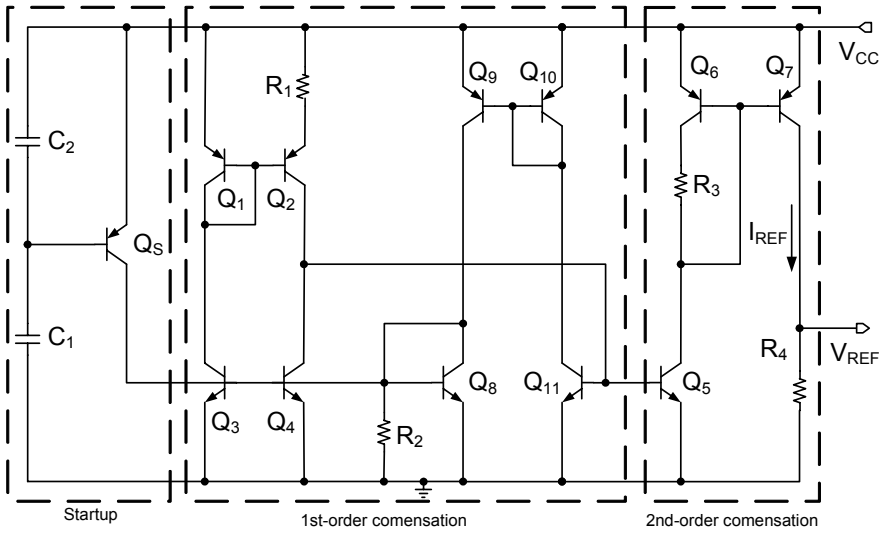
5.3 Improved Band-gap Reference Design

The complete schematics of improved second-order I_{VBC} -compensated band-gap reference A and B are illustrated in Fig. 5.15(a) and 5.15(b) respectively. They are denoted as band-gap reference A′ and B′ correspondingly. Both circuits are started up in the capacitive approach.

The temperature characteristics of band-gap reference A′ and B′ in Fig. 5.15 are obtained when a reference current of $10.0uA$ is generated. R_4 is set to $50k$ in both designs to generate $500mV$ reference voltage. Since temperature dependence of resistors is not taken into account in this work, the reference voltage will exhibit the same temperature dependence as the reference current. As shown in Fig. 5.16(a) and 5.16(b), in the temperature range from -55°C to 125°C, the temperature drift of reference A is improved from 44.4 $ppm/°C$ to 8.45 $ppm/°C$, and that of reference B is improved from 22.4 $ppm/°C$ to 1.74 $ppm/°C$.



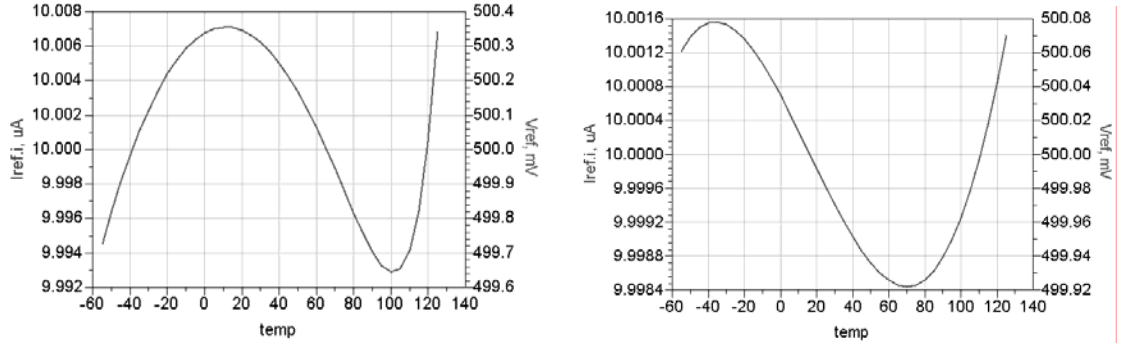
(a)



(b)

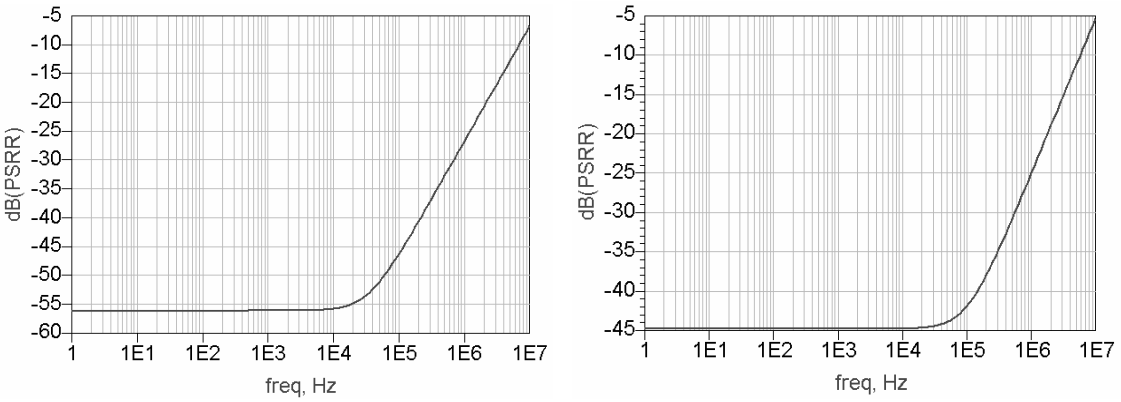
Figure 5.15 Schematic of improved second-order I_{VBC} -compensated band-gap reference (a) A′ and (b) B′.

These two circuits require a minimum supply voltage is $V_{BE}+V_{CE,SAT}$. Under $1.5V$ supply voltage, they consume $86.4uW$ and $45.7uW$ power respectively.



(a) (b)

Figure 5.16 Temperature drift of reference current and voltage of (a) band-gap reference A´ and (b) band-gap reference B´ with temperature independent resistors.



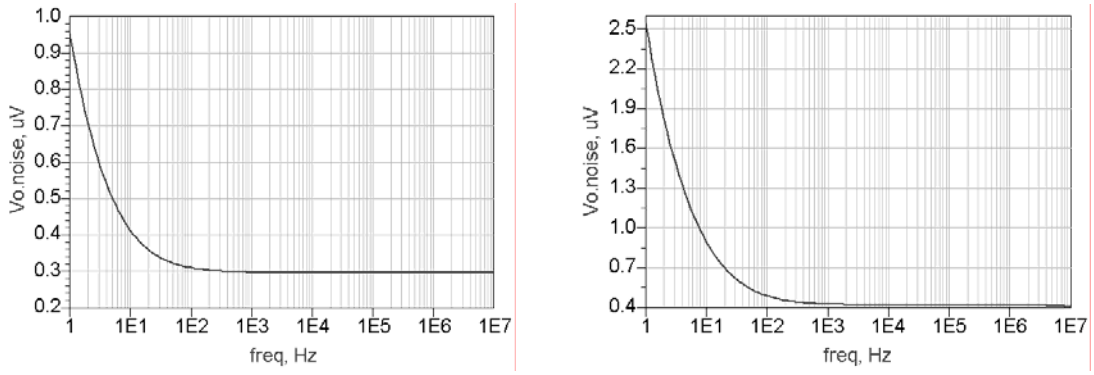
(a) (b)

Figure 5.17 PSRR of band-gap reference (a) A´ and (b) B´.

Fig. 5.17(a) and 5.17(b) illustrate the power supply rejection ratio (PSRR) of each design respectively. For both designs, the PSRR can be approximated by

$$PSRR = 20\log\left(\frac{\delta V_{REF}}{\delta V_{CC}}\right) \approx 20\log\left(\frac{R_4}{R_4 + r_O}\right) \tag{5.12}$$

where r_O represents the output resistance of Q_{10} for reference A and that of Q_7 for reference B. It is seen that the PSRR can be ameliorated if R_4 is reduced for a lower output voltage. In the situation of $R_4 = 50k$, the PSRR is equal to -56.1dB and -44.8dB respectively at 1kHz. If $R_4 = 10k$, the PSRR is -69.4dB and -58.8dB respectively at 1kHz as observed from Fig. 5.19(a) and 5.19(b).

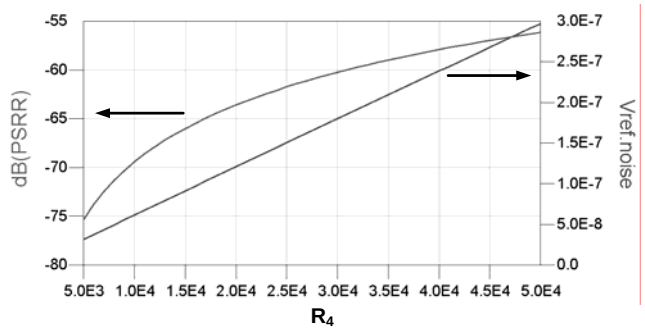


(a) (b)

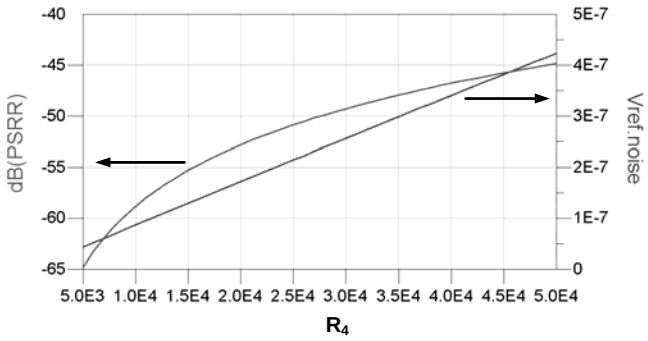
Figure 5.18 Noise spectrum of band-gap reference (a) A′ and (b) B′.

Fig. 5.18(a) and 5.18(b) depict the noise spectrum. When $R_4 = 50k$, the noise voltage spectral density is equal to 297nV and 423nV respectively at 1kHz. Also the noise will decrease as the output voltage decreases as shown in Fig. 5.19(a) and 5.19(b). When $R_4 = 10k$, the noise density is equal to 61.5nV and 87.0nV respectively at 1kHz.

Table 5.2 summarizes all these aspects of the performance considered so far for both designs when R_4 is set to 50k.



(a)



(b)

Figure 5.19 PSRR and noise spectrum at 1*kHz* vs. R_4 of band-gap reference (a) A´ and (b) B´.

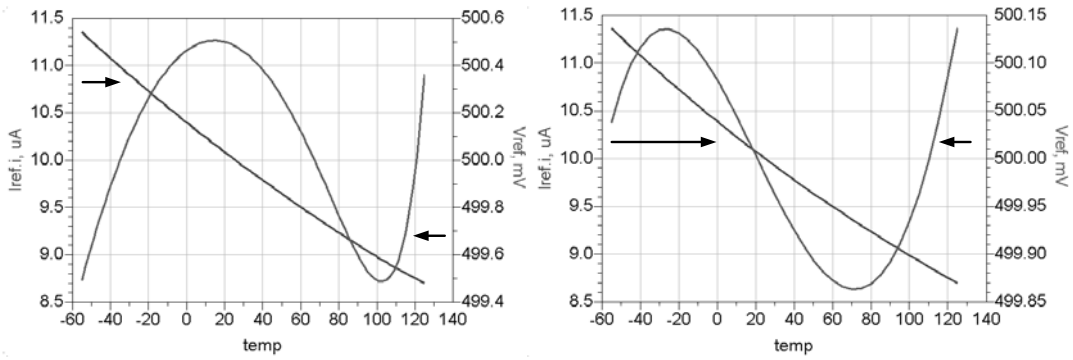
5.4 Temperature Dependence of Resistors

In both mathematical derivations and circuit simulations completed so far, all resistors are assumed temperature independent. In fact this is not true. For more accurate results, the temperature dependences of resistors must be taken into account. With temperature dependent resistors, the developments of voltage reference and current reference will be slightly different. For example, if a current reference is designed in the current mode, the reference current must be temperature independent. If a voltage reference is designed in the current mode, the reference current should present

certain temperature dependence to account for that of the load resistor. In this work, the temperature independent reference voltage will be the goal of the designs.

Table 5.2 Summary of simulation results for I_{VBC}-compensated band-gap reference A′ and B′ with $R_4 = 50k$.

	A′	B′
Mean reference current (uA)	10.0	10.0
Temp. dependence ($ppm/°C$)	8.45	1.74
Supply voltage (V)	1.5	1.5
Power dissipation (uW)	86.4	45.7
PSRR@1kHz (dB)	-56.1	-44.8
Noise@1kHz ($nV/\sqrt{Hz}$)	297	423



(a) (b)

Figure 5.20 Temperature drift of the reference current and voltage of band-gap reference (a) A′ and (b) B′ when resistors are assumed temperature dependent with linear temperature coefficient equal to +1500 $ppm/°C$.

With all the resistors assumed to have linear temperature coefficient of +1500 *ppm*/°*C* [1] [48], temperature drifts of the reference voltage of band-gap references A′ and B′ are depicted in Fig. 5.20. In the temperature range from -55°*C* to 125°*C*, the temperature drift of reference A′ and B′ is degraded to 11.3 *ppm*/°*C* and 3.04 *ppm*/°*C* respectively. Notice that reference currents present negative temperature variation to account for the positive temperature dependence of load resistors, and reference voltages are still curvature compensated.

5.5 Summary

The stability of the normal operating point of self-biased circuitry is analyzed. A stable self-biasing $V_T + V_{BE}$ reference circuit is proposed, which only presents 11.40 *ppm*/°*C* temperature drift in the temperature range from -55°*C* to 125°*C*. It eases the following second-order compensation. A simple startup circuit is developed in the capacitive approach. Finally the second-order I_{VBC} -compensated band-gap reference A and B, developed in Chapter III, are revised by employing the new $V_T + V_{BE}$ reference and the capacitive startup circuit. Some important aspects of performance are acquired, except the line regulation, which will be improved using the low-dropout regulator as discussed in Chapter VI.

CHAPTER 6

LINEAR REGULATOR

The self-biased circuits aim to eliminate the dependence of output characteristics on the power supply voltage. Actually they can only alleviate such dependence due to the finite output impedance of a transistor. Typically to enhance the line regulation performance, the raw noisy power supply voltage should be regulated by a linear low-dropout voltage regulator (LDO) before fed into the reference circuits.

6.1 Low Dropout Linear Voltage Regulator Structure

Due to the finite the output resistance of transistors, the output characteristics of self-biased reference circuits still vary with the supply voltage. This can be observed from the poor line regulation performances listed in Table 4.1. So the raw supply voltage usually needs to be regulated by a voltage regulator before it can be used. The voltage regulator eliminates any fluctuation in such a raw DC input voltage, and produces a constant, well-specified output voltage suitable to power up other circuitry.

A common type of voltage regulator is the *series* regulator. The name *series* comes from the fact that the output voltage is controlled by a power transistor in series with the output [1]. The circuit is composed of four blocks: the voltage reference, the pass element, the sampling resistors, and the error amplifier as depicted in Fig. 6.1.

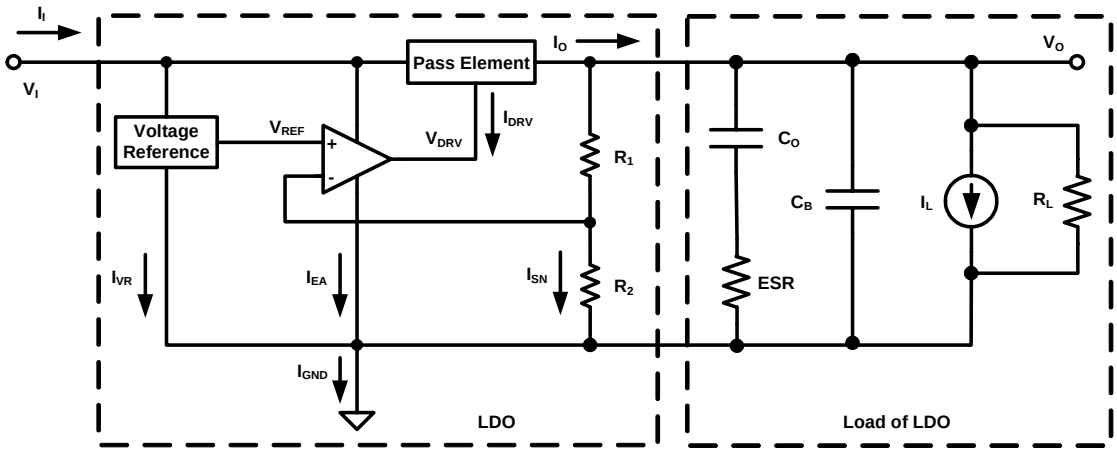


Figure 6.1 Typical topology and load of linear voltage regulator [2] [49].

Voltage reference – is the basis for the output voltage. The output voltage cannot be more accurate or stable over temperature than the reference voltage. Therefore it is usually implemented in the band-gap approach which is able to produce a high-precision low-drift reference voltage.

Pass element – boosts the output-current capabilities of the error amplifier to a higher level. This involves transferring large current from the input to the load under the control of the error amplifier. Note that the type of pass element determines which input of the error amplifier is connected to sampled output voltage. If P-type pass elements are utilized, e.g, PNP or PMOS, the sampled output voltage needs to be applied to the positive input of the error amplifier to form a negative feedback. For N-type pass elements, e.g, NPN or NMOS, the sampled signal is applied to the negative input.

Sampling resistors – scale the output to a value suitable for comparison against the reference voltage by the error amplifier. A desired output voltage can be acquired

with proper values of R_1 and R_2. Since resistors R_1 and R_2 are connected in a series-shunt feedback, a high input impedance is presented to the voltage reference, which is desirable to minimize the loading effects. Additionally quite low output impedance will result at the output, which is exactly the requirement for a good voltage source [1].

Error amplifier – takes a scaled-down version of the output, compares against the reference voltage, and adjusts the output to reduce the error. For large loop gain, the error is driven close to zero. Then the output voltage is regulated at

$$V_O = V_{REF} \frac{R_1 + R_2}{R_2} \tag{6.1}$$

Above relationship holds true only if the input voltage is sufficiently high to keep the error amplifier and the pass element from saturating. As the input voltage nears the output voltage, a critical point exists at which the voltage regulator begins to lose the loop control of the output. This point determines the dropout voltage of the regulator, which is equal to the minimum difference between the input and the output voltage

$$V_{DO} = V_{I,MIN} - V_O \tag{6.2}$$

The dropout voltage is an intrinsic factor in determining the efficiency of the regulator circuits regardless of the load condition. For high efficiency, which is of great importance particularly for the battery-operated devices, a low dropout voltage is mandatory. The low-dropout voltage regulators are advantageous in such applications, because they are capable of offering reliable solutions at the expense of fewer components, smaller size, and less wasted power. Thus the design of a low-dropout

voltage regulator becomes one of the most intriguing topics in nowadays power management circuits design. Since the band-gap reference has been discussed in detail in previous chapters, and the sampling resistors network is quite simple, attention will be focused on the error amplifier and pass element in this section.

6.2 Pass Element

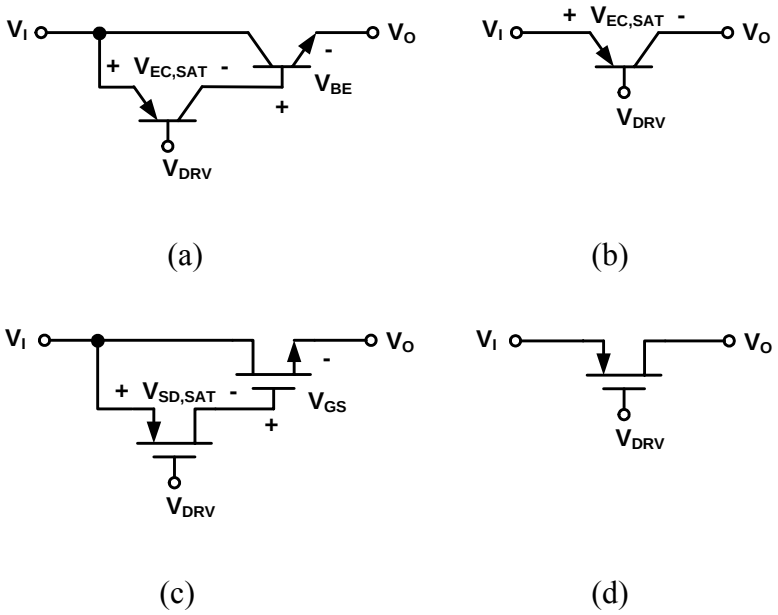


Figure 6.2 Pass element structures (a) NPN, (b) PNP, (c) NMOS and (d) PMOS.

The four basic implementations for the pass element are illustrated in Fig. 6.2 [2] [49]. A comparison of their strengths and limitations are summarized in Table 6.1 [2] [49]. Lowest dropout voltages are achieved by PMOS and PNP transistors, which is one source-drain saturation voltage, $V_{SD,SAT}$, and one emitter-collector saturation voltage, $V_{EC,SAT}$, respectively. In addition, N-type (NPN or NMOS) devices require a

positive drive signal with respect to the output, while P-type (PNP or PMOS) devices are driven from a negative signal with respect to the input. Generating a positive drive signal becomes difficult at low input voltages. As a result, the P-type pass elements are more prevalent.

Table 6.1 Comparison of pass element structures.

	NPN	PNP	NMOS	PMOS
$I_{O,MAX}$	High	High	Low	Low
I_{GND}	Medium	Large	Low	Low
V_{DO}	$V_{EC,SAT}+V_{BE}$	$V_{EC,SAT}$	$V_{SD,SAT}+V_{GS}$	$V_{SD,SAT}$
Speed	Fast	Slow	Medium	Medium

In low-voltage battery applications, PMOS implementations are even more attractive than PNP implementations, because a lower ground current and dropout voltage can be obtained. In the dropout situation, the PMOS pass element goes into the linear region, where the transistor acts as a fixed, low-value resistor. The resistance is referred to as the drain-to-source on resistance, $R_{SD,ON}$. It is seen that $R_{SD,ON}$ is determined by the physical design of the transistor and the available gate drive. The product of $R_{SD,ON}$ and the output current determines the source-drain saturation voltage, $V_{SD,SAT}$, which is also the dropout voltage of PMOS LDOs. For PNP LDOs, the dropout voltage is determined by the saturation emitter-collector voltage of the transistor,

$V_{EC,SAT}$. Typically $V_{EC,SAT} > V_{SD,SAT}$. Hence PMOS LDOs have a lower dropout voltage than that of PNP LDOs [50].

Ground current is the difference between the input and output currents

$$I_{GND} = I_I - I_O \tag{6.3}$$

It is returned to the input supply through the ground pin of the LDO. The ground current is actually the sum of all the internal bias currents of the LDO as indicated in Fig. 6.1, and is given by

$$I_{GND} = I_{VR} + I_{EA} + I_{SN} + I_{DRV} \tag{6.4}$$

where I_{VR}, I_{SN} and I_{EA} denote the currents through the voltage reference, sampling network and error amplifier respectively, I_{DRV} is the pass element drive current.

The efficiency of a LDO is calculated as

$$\eta = \frac{I_O V_O}{I_I V_I} \times 100\% \tag{6.5}$$

To enhance the efficiency, the difference between input and output voltage as well as the difference between input and output current should both be minimized. So the dropout voltage and ground current should be as low as possible.

Typically bipolar devices are good at delivering higher current as illustrated in Table 6.1. However this is achieved at the price of high base current due to the current-driven nature of bipolar devices. Such a high base current, correspondingly a high ground current, will degrade the efficiency. The drive current for a voltage-driven PMOS device is primarily the parasitic leakage of the device, which is much lower

compared to the base current of a PNP device. Thus PMOS devices are superior in minimizing the ground current.

In a PNP LDO, the ground current is also affected by the input voltage. As the input voltage approaches the output voltage, the voltage drop across the pass element will decrease. When the PNP transistor enters the dropout region, the current gain of transistor can drop to a value less than 1. When this happens, the output current can only be sustained with more base current, and more ground current in turn. By comparison, the leakage current of a PMOS device remains fairly constant as the LDO enters the dropout region [50].

The noise in a LDO may arise from the LDO itself and the raw input signal. To reduce the internally generated noise, developments of voltage reference and error amplifier are essential, since they have the most noise contribution. To reject the noise from the input, a high PSRR is required. The PSRR is determined by the output impedance of the pass element and the insensitivity of the error amplifier to input noise. PNP LDOs typically exhibit better PSRR characteristics than PMOS counterparts. The PSRR of a LDO can be improved by increasing the loop gain or the output impedance of pass element [50]. A comparison of the P-type pass element is illustrated in Table 6.2.

The pass element to be adopted in this work is shown in Fig. 6.3. In this structure, the error amplifier will not drive the PNP pass transistor Q_1 directly, but through a NPN transistor Q_2 [3]. The advantage is the current gain of the pass element as well as the loop gain (see Section 6.3) will be boosted by a factor of β_n. And the

current driving capability of the error amplifier will be alleviated. The capacitor C_{COMP} helps to shape the frequency response of the loop gain.

Table 6.2 Comparison of P-type pass elements.

	PNP	PMOS
Lower V_{DO}		√
Higher $I_{O,MAX}$	√	
Lower I_{GND}		√
Independence of I_{GND} on input and load conditions		√
Higher PSRR	√	

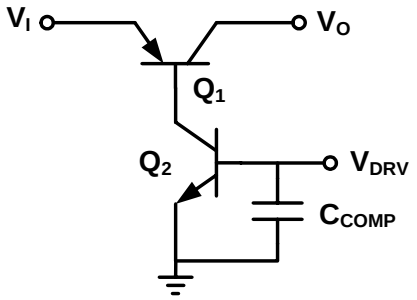


Figure 6.3 PNP pass element structure driven by NPN transistor.

6.3 Error Amplifier

The performances of a regulator circuit can be evaluated by the same criteria as discussed in Chapter IV, because the regulator circuit has much in common with the

reference circuit. Among those specification, line and load regulations are important for the output voltage accuracy. They are both inversely proportional to the loop gain [49]

$$\text{Line regulation: } \frac{\Delta V_O}{\Delta V_I} \approx \frac{R_L}{(r_O + R_L)L_0} \tag{6.6}$$

$$\text{Load regulation: } \frac{\Delta V_O}{\Delta I_O} \approx \frac{R_L}{L_0} \tag{6.7}$$

where $L_0 = R_L R_2 G_A \beta / (R_1 + R_2)$ is the DC loop gain; β is the current gain of the pass element; G_A is the transconductance of the error amplifier; r_O is the output resistance of the pass element; R_L is the load resistance of the LDO, and assumed much less than $R_1 + R_2$. So a large loop gain is required for a good line and load regulation performance. However the gain cannot be too high due to the tradeoff between the gain and the bandwidth. A large bandwidth, corresponding to a high slew rate, is essential for a minimal-overshoot fast-recovery transient response of the LDO. Thus the error amplifier needs to be developed with gain and bandwidth being optimized simultaneously.

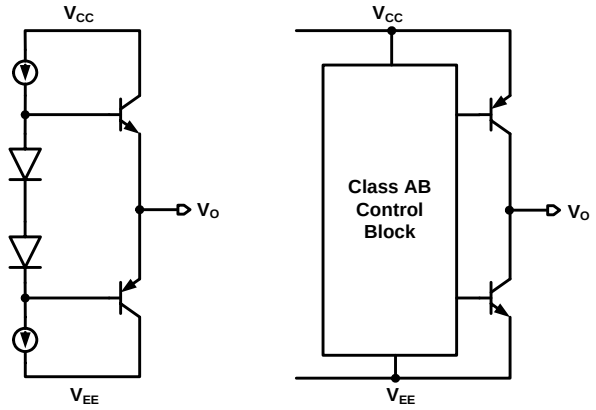
A major distinction between the reference circuit and the regulator circuit is the current drive capability. The latter one could be functionally regarded as a reference circuit, but with greater current output capability [3]. The regulator circuit may need to output a current as low as $50mA$ or as high as $5A$ [50]. If the pass element is implemented by the bipolar devices, the current-driven characteristics will demand a high drive current from the error amplifier under heavy load conditions. Furthermore, when the LDO operates in the dropout region, the significant drop of the current gain

may lead to a drive current comparable with the output current. To satisfy such a high-current drive requirement, a class AB output stage is indispensable for the amplifier.

For low voltage applications, the voltage reference typically produces a voltage less than $1V$, e.g., a $199.2mV$, $595mV$ and $603mV$ output voltage is generated in [12], [2] and [38] respectively. To handle such a low common-mode voltage, a PNP differential pair is clearly the choice of the amplifier input stage.

The foregoing implies the design of class AB output stages and power-efficient overall topologies for bandwidth and gain.

6.3.1 Class AB Output Stage



(a) (b)

Figure 6.4 Class AB output stages (a) conventional, (b) rail-to-rail.

The output stage of amplifier should provide a rail-to-rail output with minimal nonlinear distortions, low quiescent power dissipation, and high output current driving capability. A rail-to-rail output is important under low-voltage low-power applications

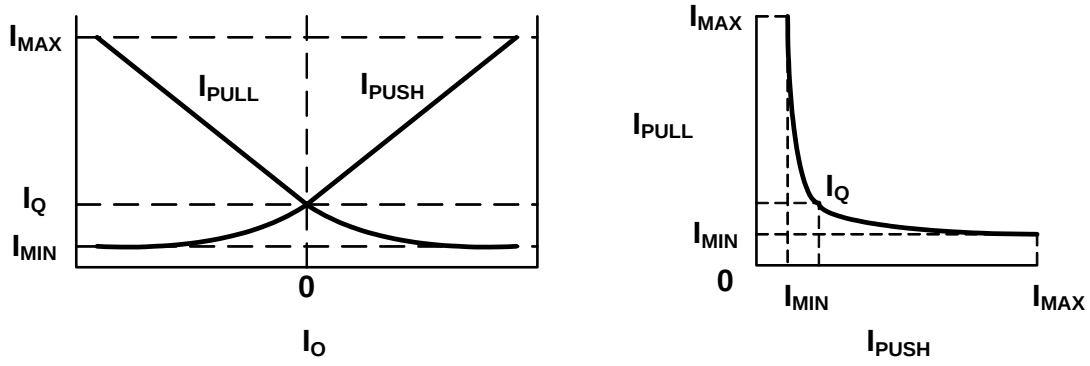
in order to efficiently use the supply voltage. So the conventional voltage-follower configuration, as depicted in Fig. 6.4(a), should be replaced by the common-emitter configuration (or common-source configuration in MOS technology) as depicted in Fig. 6.4(b). Good linearity is equivalent to the stable gain that is independent of the output voltage or current. Any deviation corresponds to a change in the amplifier open-loop gain that results in nonlinear distortion. At low-frequencies this distortion can be negligible due to the high open-loop gain and small absolute value of the deviations. But as the frequency increases close to the amplifier bandwidth, these nonlinearities become more critical.

The above requirements dictate the use of class AB output stage. An efficient class AB biasing must satisfy four requirements [51]:

- The ratio of maximum current (I_{MAX}) to quiescent current (I_Q) is high for both push (I_{PUSH}) and pull current (I_{PULL}) to achieve high efficiency.
- When the output stage is driven hard, a minimum current (I_{MIN}) not much smaller than the quiescent current is maintained, so that neither transistor is ever cut off. So the high-frequency distortion is obviated.
- A smooth AB transition is exhibited to avoid low-frequency distortion
- The output transistors must be directly driven by the preceding stages without delay from the class AB control circuit.

Fig. 6.5 shows the desired class AB output characteristics [51] [52]. To acquire such characteristics, the class AB control block should be able to maintain a low quiescent current for both push and pull transistors while the amplifier stands idle, and

keeps the push or pull current above a certain minimum value while the other one is high.

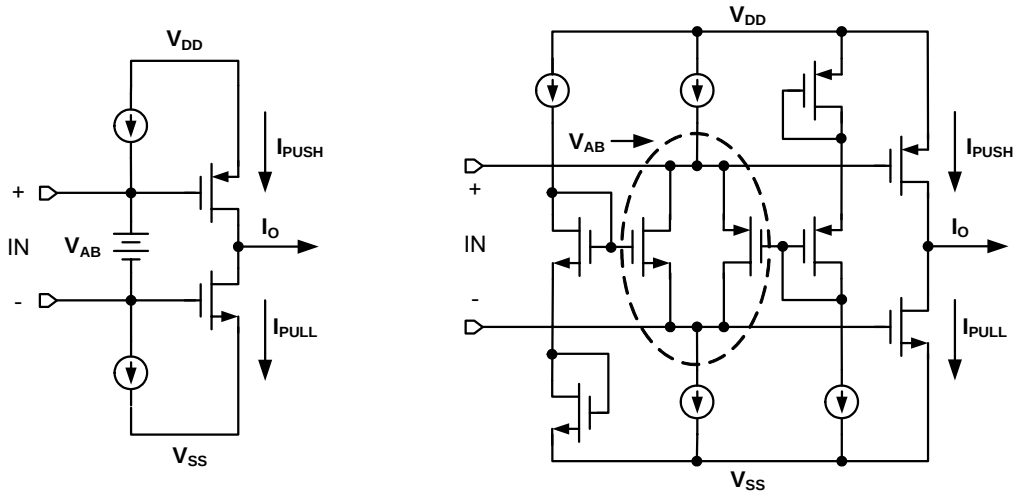


(a) (b)

Figure 6.5 Desired class AB characteristics (a) I_{PULL} and I_{PUSH} vs. I_O, (b) I_{PULL} vs. I_{PUSH}.

6.3.1.1 Review of Class AB Output Stage

The required class AB control can be implemented in several ways [51] – [54]. The conventional approach realizes the class AB control through a floating voltage source, V_{AB}, which can be implemented by complementary head-to-tail connected transistors together with biasing circuits as illustrated in Fig. 6.6 [51] [52]. The class AB control circuit couples the gates of the output transistors in the quiescent mode of operation by generating a low impedance. When one output transistor delivers a large output current, the other output transistor is regulated at a constant drain current and the gate of the output transistors are decoupling by generating large impedance. At the same, the class AB control circuit steers all the signals to the active output transistor [52].



(a) (b)

Figure 6.6 Class AB control realized by a floating voltage (a) concept design, (b) practical implementation where input can be voltage or current input.

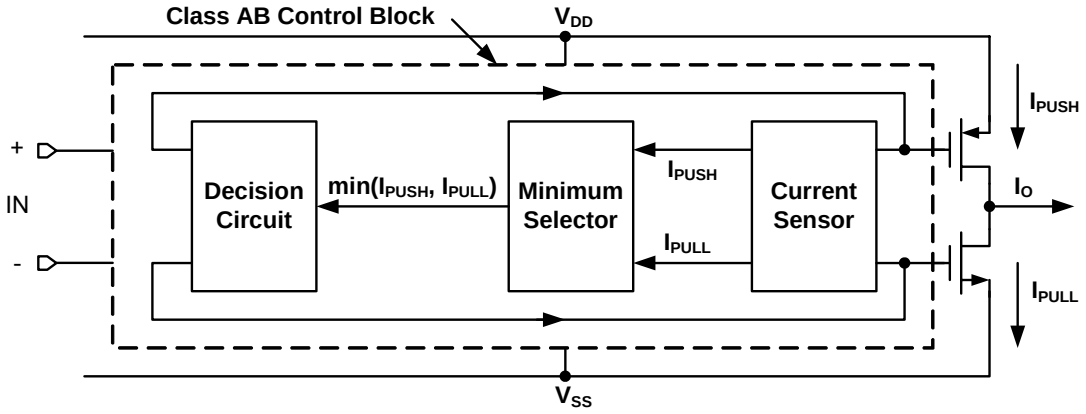


Figure 6.7 Block diagram of class AB control implemented by a feedback loop.

The quiescent and minimum currents can also be controlled by a feedback loop [51] – [53] as shown in Fig. 6.7. The current sensor is usually implemented by a current

mirror, which reproduces the push and pull current by sensing the gate-source voltage of output devices. The smaller one of these two currents will be selected by the minimum selector circuit, and then fed into the decision circuit. The decision circuit is basically a differential amplifier, which compares the input current with a certain reference current, and generates a control signal to adjust the gate-source voltage of output devices. Since the current sensor, minimum selector and decision circuit are connected in a feedback loop, the smaller one of the push and pull current will be always regulated at the predetermined reference current. For low-power applications, the push and pull current may be scaled down by the current sensor before fed into the minimum selector and decision circuit. Then the class AB control block only needs to handle the scaled-down version of the push and pull current. And the original push and pull current will be regulated at a scaled-up version of the reference current.

Another approach to obtain the desired class AB behavior is to realize the harmonic mean principle [52] [54]

$$I_{REF}\left(I_{PUSH}+I_{PULL}\right)=I_{PUSH}I_{PULL} \tag{6.8}$$

Frequently a scaled-down version of I_{PUSH} and I_{PULL} will be handled in the class AB control. The scaling factor, or the current gain, is represented by α, which is less than 1 typically [54]. If α is taken into account, the harmonic mean principle is scaled as

$$I_{REF}\left(\alpha\cdot I_{PUSH}+\alpha\cdot I_{PULL}\right)=\left(\alpha\cdot I_{PUSH}\right)\cdot\left(\alpha\cdot I_{PULL}\right) \tag{6.9}$$

In the quiescent state, there is no output current since I_{PUSH} and I_{PULL} are equal. From Equ. (6.9), the quiescent current is given by

$$I_Q = (2/\alpha) \cdot I_{REF} \tag{6.10}$$

If either I_{PUSH} and I_{PULL} is under heavy driving condition, the other one is regulated at the reference current

$$I_{MIN} = I_{REF} / \alpha \tag{6.11}$$

For example, if the output stage is sourcing high current, I_{PUSH} is much larger than I_{PULL}. When I_{PULL} is neglected in the left-hand side of Equ. (6.9), then

$$I_{REF}(\alpha \cdot I_{PUSH} + \alpha \cdot I_{PULL}) \approx \alpha \cdot I_{PUSH} I_{REF} = \alpha^2 \cdot I_{PUSH} I_{PULL} \tag{6.12}$$

Then I_{PULL} approaches its minimum value

$$I_{PULL} = I_{REF} / \alpha \tag{6.13}$$

A straightforward way to implement the harmonic mean principle is to employ a translinear loop with proper current flows in each transistor as depicted in Fig. 6.8 [54].

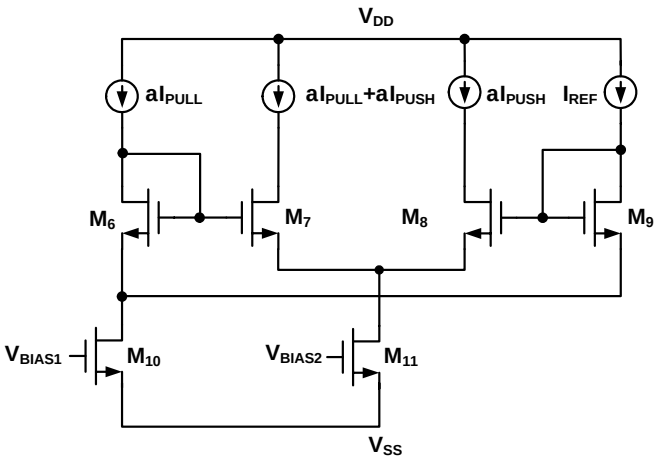


Figure 6.8 Class AB output stage based on straightforward implementation of harmonic mean principle.

However the output stage proposed in [54] does not truly realize the principle. In [54], the transistor M_{10} is biased to flow a scaled-down version of I_{PULL}. Then the current flow in M_6 is actually the scaled-down version of I_{PULL} minus I_{REF}. Thus the following principle is implemented

$$I_{REF}\left(\alpha \cdot I_{PUSH} + \alpha \cdot I_{PULL} - I_{REF}\right) = \alpha \cdot I_{PUSH}\left(\alpha \cdot I_{PULL} - I_{REF}\right) \tag{6.14}$$

where α is chosen to be $1/9$ in [54].

If the harmonic mean principle is implemented directly, it is hard to properly bias the tail transistors, e.g., M_{10} and M_{11} in Fig. 6.8. To circumvent this obstacle, the principle can be realized indirectly using the current subtraction technique.

6.3.1.2 Current-Subtraction Class AB Control

Equ. (6.9) can be rewritten as

$$\alpha \cdot I_{PUSH} I_{REF} = \alpha \cdot I_{PULL}\left(\alpha \cdot I_{PUSH} - I_{REF}\right) \tag{6.15.a}$$

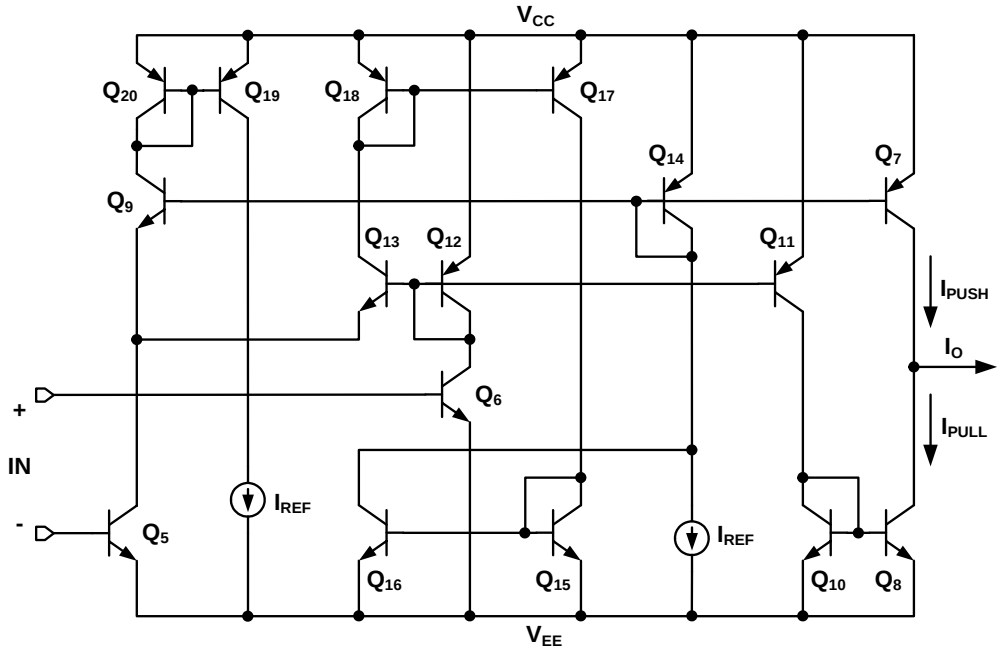
or

$$\alpha \cdot I_{PULL} I_{REF} = \alpha \cdot I_{PUSH}\left(\alpha \cdot I_{PULL} - I_{REF}\right) \tag{6.16.b}$$

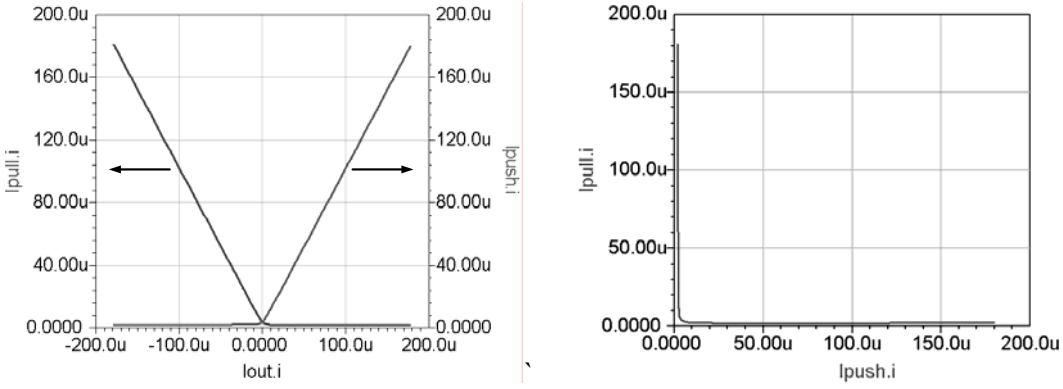
Since Equs. (6.15.a) and (6.15.b) are derived from Equ. (6.9), the circuit implementations of them should have the same I_Q and I_{MIN} as given in Equ. (6.10) and (6.11) respectively.

Fig. 6.9(a) depicts an implementation of Equ. (6.15.a). Transistor Q_{14} measures the I_{PUSH} in Q_7. This replicate of I_{PUSH} is subtracted by the I_{REF} before being fed into Q_{16}, and then Q_{13} through current mirrors composed of Q_{15}, Q_{16}, Q_{17} and Q_{18}. The I_{PULL} is reproduced in Q_{12}. The current in Q_9 is I_{REF}. Consequently the harmonic mean

principle of Equ. (6.15.a) is implemented by the translinear loop of Q_{12}, Q_{13}, Q_9 and Q_{14} (or Q_7 equivalently).



(a)



(b) (c)

Figure 6.9 Class AB output stage using asymmetrical current subtraction for current regulation. (a) circuit, (b) I_{PUSH} and I_{PULL} vs. I_{OUT}, (c) I_{PUSH} vs. I_{PULL}.

The I_{MIN} is demonstrated mathematically equal to I_{REF}/α in Equ. (6.11). Physically such a regulation is achieved by the current subtraction operation, which guarantees that at least I_{REF} will always flow in Q_{14}, and in turn I_{REF}/α in Q_7. Then the translinear loop regulates the I_{MIN} in Q_8 at I_{REF}/α. Since only I_{PUSH} is directly regulated by the current subtraction, this circuit is considered as an "asymmetrical" design.

For a certain I_{REF}, I_Q and I_{MIN} can be adjusted by α. Generally a value less than unity is used [54]. In this situation, the class AB control block only needs to handle a scaled-down version of I_{PUSH} and I_{PULL}. If I_{PUSH} and I_{PULL} are fixed, the power dissipation of the control block will be reduced, especially under the heavy-driven condition. On the other hand, if power dissipation of the control block is fixed, the output transistors pair will have higher driving capability. However the price that is paid is slightly increased power dissipation in the output transistors pair. Because I_{PUSH} and I_{PULL} will be regulated at an I_{MIN} equal to I_{REF}/α, and I_Q will be equal to $2I_{REF}/\alpha$. A high I_{MIN} is unnecessary to prevent either of the push and pull transistor from cutting off. It leads to more current wasted in the "idle" transistor when the other one is driving hard. But this waste current is generally negligible relative to the high driving current. Similarly, although a high I_Q increases the quiescent power dissipation in the output transistors pair by a factor equal to $1/\alpha$, this power dissipation is still small relative to that of the class AB control block when α is not much less than 1. In conclusion, $\alpha < 1$ lowers the power dissipation in the control block, while raising it in the output transistors pair. Hence, α should be chosen for the lowest total power dissipation, provided that the current driving requirement is satisfied.

Table 6.3 Class AB output characteristics summary for the output stage in Fig. 6.9(a).

α		1/2	1/4	1/8
I_{MIN} (uA)	I_{PUSH}	2.09	4.12	7.99
	I_{PULL}	2.11	5.87	11.1
I_{MAX} (uA)	I_{PUSH}	180.4	610.5	1223
	I_{PULL}	181.0	613.9	1224
I_Q (uA)		3.86	8.48	15.0
I_{SUP} (uA)		13.1	18.9	24.6
I_{MAX} / I_{SUP}		13.8	32.3	49.7

Fig. 6.9(b) and 6.9(c) show the class AB characteristics of the output stage proposed in Fig. 6.9(a). The I_{REF} is chosen to be $1uA$, and α is set to $1/2$. Theoretically I_{MIN} of both I_{PUSH} and I_{PULL} should be equal to $2uA$, and I_Q should be $4uA$. The simulation results show that I_{MIN} of I_{PUSH} and I_{PULL} is regulated at $2.09uA$ and $2.11uA$ respectively. The maximum output current (I_{MAX}) is above $180uA$. The output transistors pair has I_Q of $3.86uA$. The whole output stage consumes $13.06uA$ supply current (I_{SUP}) in the quiescent state. The ratio of I_{MAX} to I_{SUP} indicates the power efficiency of the circuit, and is equal to 13.8. For enhanced current output capability and efficiency, a smaller α is necessary. Table 6.3 shows that I_{MAX} increases from approximately $180uA$, $610uA$ to $1223uA$ as α is reduced from 1/2, 1/4 to 1/8. But I_{SUP} does not increase as much as I_{MAX}. So the ratio of I_{MAX} to I_{SUP} is improved from 13.8, 32.3 to 49.7. Note the

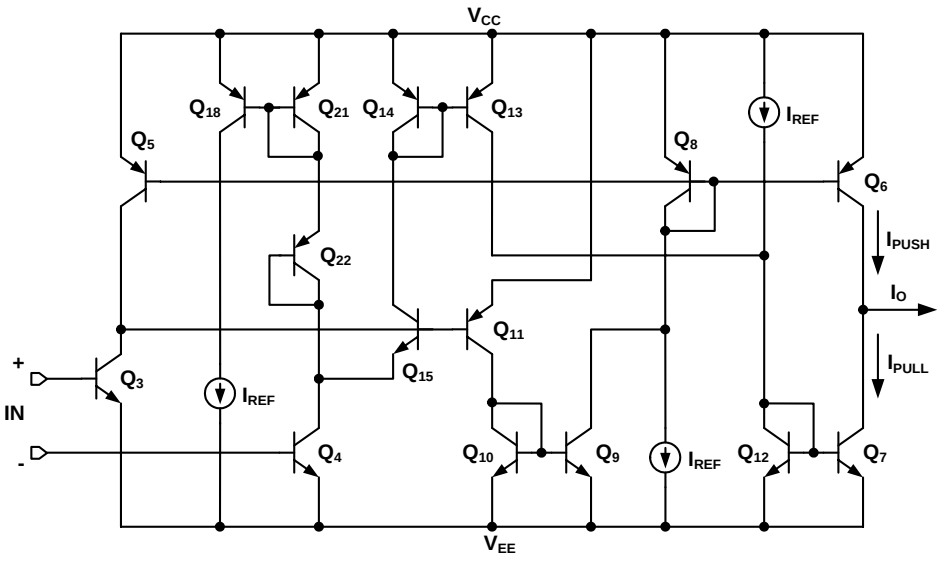
ratio is calculated using the smaller I_{MAX} for I_{PUSH} and I_{PULL} for each α. Another way to enhance the current output capability and efficiency is to employ larger transistors at the cost of larger chip area.

In the design of Fig. 6.9(a), the output transistors are not directly driven by the preceding stage to enhance the current driving capability. Because BJT transistors are current driven, the preceding stage needs to provide the base current of the output transistors if the output transistors are directly driven by the preceding stage. These base currents can be as high as the bias current of the preceding stage under heavy load condition. For a higher output current capability, the bias current must be increased, which leads to higher power consumption. This problem is avoided by breaking the direct connection of the output transistors pair and preceding stages. Then the base currents of the output transistors are provided by the replicates of their collector currents, e.g., the collector current of Q_{10} sources the base current of the pull transistor Q_8 and itself, the collector current of Q_{14} sinks the base current of push transistor Q_7 and itself. (More precisely, the base current of Q_9 also sinks a certain amount of the base currents of Q_7 and Q_{14}, and the collector current of Q_{14} sinks the rest. However the base current of Q_9 is so low that it is negligible.) A disadvantage is that additional phase shift can be caused by the control block. So the required Miller compensation capacitors are large, which will significantly reduce the slew rate.

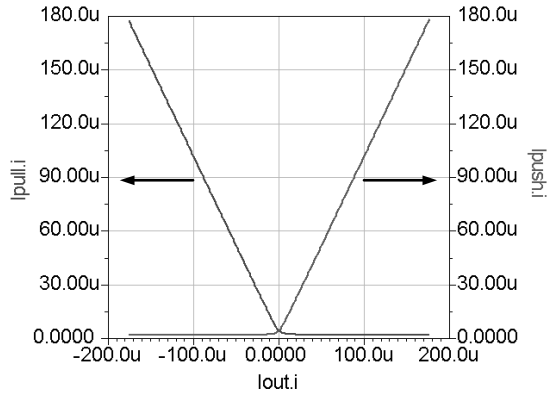
Still based on the current subtraction strategy, the harmonic mean principle can be realized in another topology as depicted in Fig. 6.10(a). The tranlinear loop consists of Q_{11}, Q_{15}, Q_{21} and Q_{22}. The difference currents of $\alpha \cdot I_{PUSH} - I_{REF}$ and $\alpha \cdot I_{PULL} - I_{REF}$

are fed into Q_{11} and Q_{15} respectively. The currents in Q_{21} and Q_{22} are the same, and equal to I_{REF}. Then the translinear loop implements the following equation

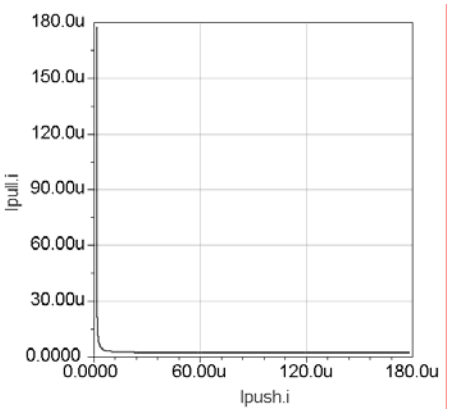
$$(\alpha \cdot I_{PUSH} - I_{REF}) \cdot (\alpha \cdot I_{PULL} - I_{REF}) = I_{REF}^2 \tag{6.17}$$



(a)



(b)



(c)

Figure 6.10 Class AB output stage using symmetrical current subtraction for current regulation. (a) circuit, (b) I_{PUSH} and I_{PULL} vs. I_{OUT}, (c) I_{PUSH} vs. I_{PULL}.

It can be easily simplified into the scaled form of the harmonic mean principle in Equ. (6.9). Since both I_{PUSH} and I_{PULL} are directly regulated by the current subtraction, the circuit in Fig. 6.10(a) is considered a "symmetrical" design. Its class AB characteristics, obtained under the circumstance of $\alpha = 1/2$, are illustrated in Fig. 6.10(b) and 6.10(c).

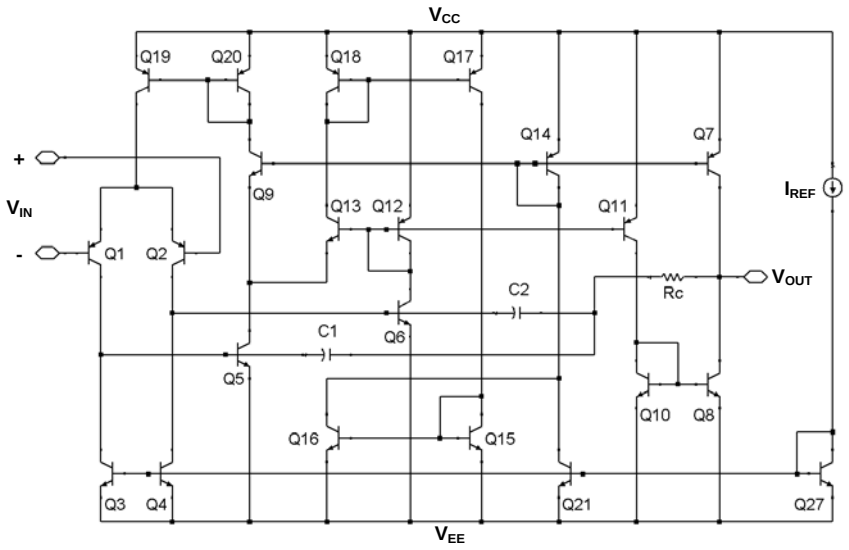
Table 6.4 summarizes how the performance changes with the change of α. It is observed that the "symmetrical" design has inferior current driving capability and power efficiency than the "asymmetrical" design as α is reduced.

Table 6.4 Class AB output characteristics summary for the output stage in Fig. 6.10(a).

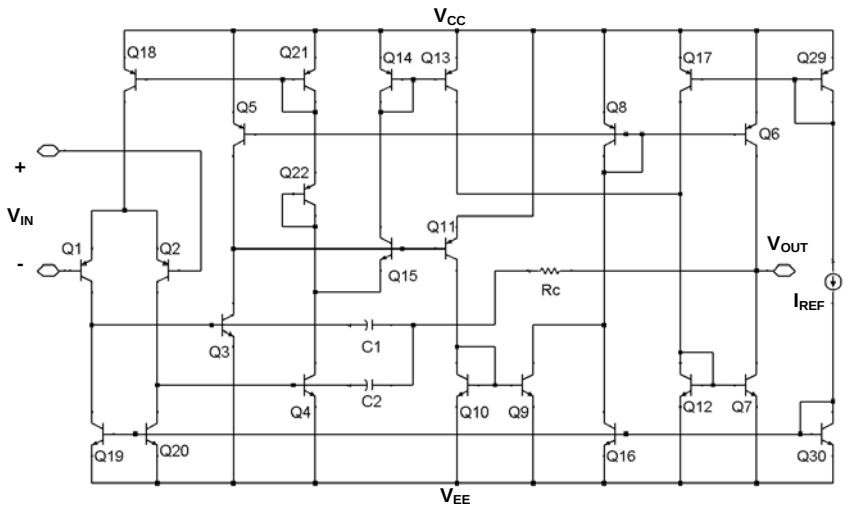
α		1/2	1/4	1/8
I_{MIN} (uA)	I_{PUSH}	1.79	3.49	6.82
	I_{PULL}	1.92	3.73	7.11
I_{MAX} (uA)	I_{PUSH}	178.5	347.2	653.6
	I_{PULL}	177.4	342.8	646.9
I_Q (uA)		4.41	7.83	16.1
I_{SUP} (uA)		10.5	12.9	21.8
I_{MAX} / I_{SUP}		16.9	26.6	29.7

6.3.2 Error Amplifier with the Class AB Output Stage

The two-stage error amplifiers with the proposed class AB output stages are depicted in Fig. 6.11.



(a)



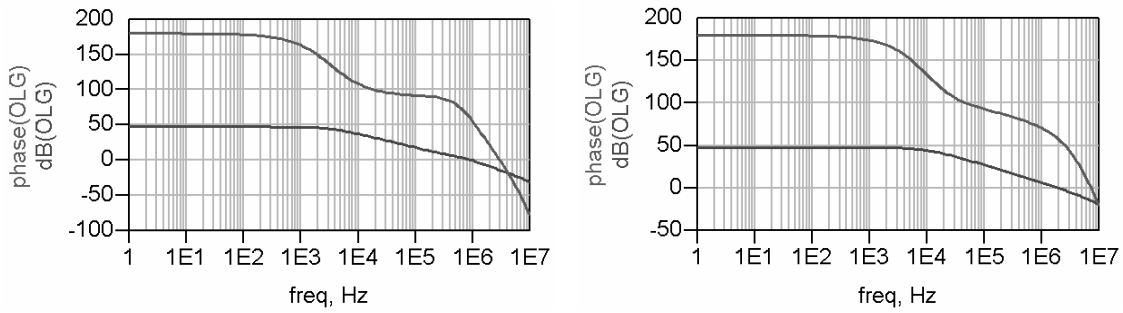
(b)

Figure 6.11 Two-stage operational amplifiers with current-subtraction class AB control. (a) asymmetrical, (b) symmetrical.

The PNP input differential pair is selected to account for the low V_{REF} which is to be applied at the noninverting input node. So the maximum common mode voltage

will be one base-emitter voltage plus one collector-emitter saturation voltage below the positive power supply voltage, i.e., the common mode input voltage range (CMIR) is from V_{EE} to $V_{CC} - V_{BE} - V_{CE,SAT}$.

The input offset voltage (V_{OS}) is the differential input voltage that must be applied to drive the output to zero. It results from the nonideal effects of bias mismatch as well as component mismatch. The offset voltage caused by the bias mismatch is systematic offset. Since no simulator offers the ability to predict component mismatch, only systematic offset can be simulated. The asymmetric and symmetric designs exhibit such an offset voltage of $86uV$ and $165uV$ respectively.



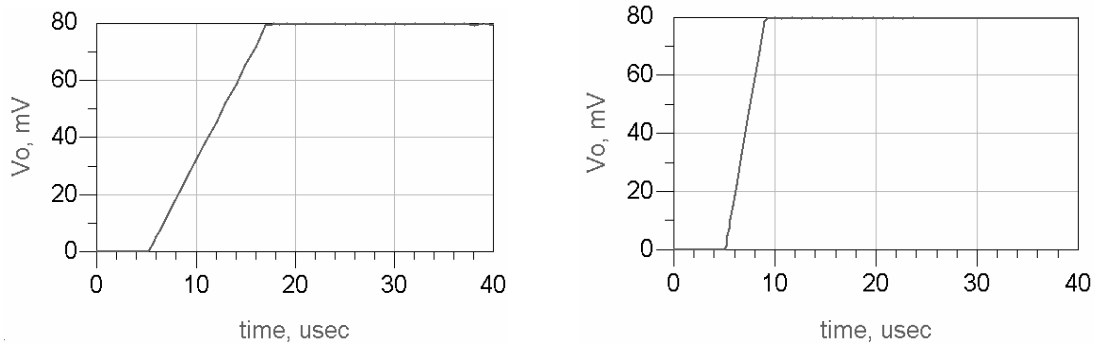
(a) (b)

Figure 6.12 Open loop frequency response of proposed two-stage operational amplifiers. (a) asymmetrical, (b) symmetrical.

Miller capacitors with a nulling resistor are utilized to compensate the frequency responses of the amplifiers, which are loaded with a $100pF$ capacitor in parallel with a $10k$ resistor. Fig. 6.12 presents the open-loop frequency responses of the proposed amplifiers in the case of $\alpha = 1/2$. For a 60° phase margin, the asymmetrical design

requires C_1 of $0.1pF$ and C_2 of $21.5pF$ with a unity-gain-frequency (UGF) of $0.891MHz$. While the symmetrical design merely requires C_1 of $0.1pF$ and C_2 of $7pF$ to achieve the 60° phase margin with a UGF of $1.78MHz$.

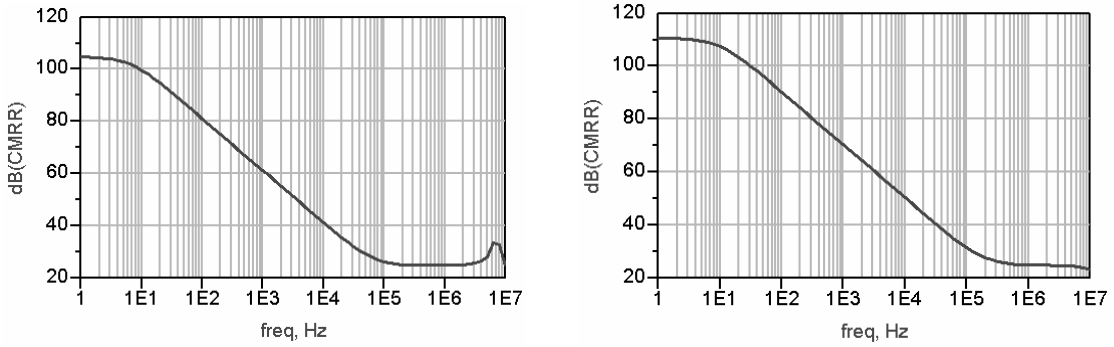
The transient responses to $80mV$ ideal step pulse are illustrated in Fig. 6.13. Not surprisingly, both asymmetric and symmetric designs are quite slow with a slew rate of $6.7mV/uS$ and $20mV/uS$ respectively, a 1% settling time of $12.5uS$ and $4.1uS$ respectively.



(a) (b)

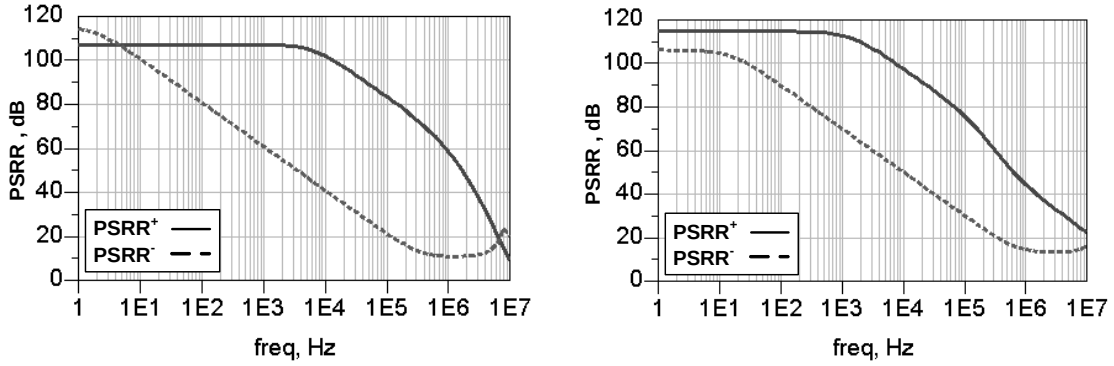
Figure 6.13 Step responses of proposed two-stage operational amplifiers. (a) asymmetrical, (b) symmetrical.

The differential amplifier aims at sensing the differential input while rejecting the common-mode input. This requires a high differential gain and small common-mode gain, in other words, a large common mode rejection ratio (CMRR) is necessary. Fig. 6.14 depicts the CMRR performance of the proposed amplifiers. For both designs, the CMRR degrades as the frequency increases. At $1kHz$, the asymmetrical and symmetrical design has a CMRR of $761.1dB$ and $70.3dB$ respectively.



(a) (b)

Figure 6.14 CMRR of proposed two-stage operational amplifiers. (a) asymmetrical, (b) symmetrical.



(a) (b)

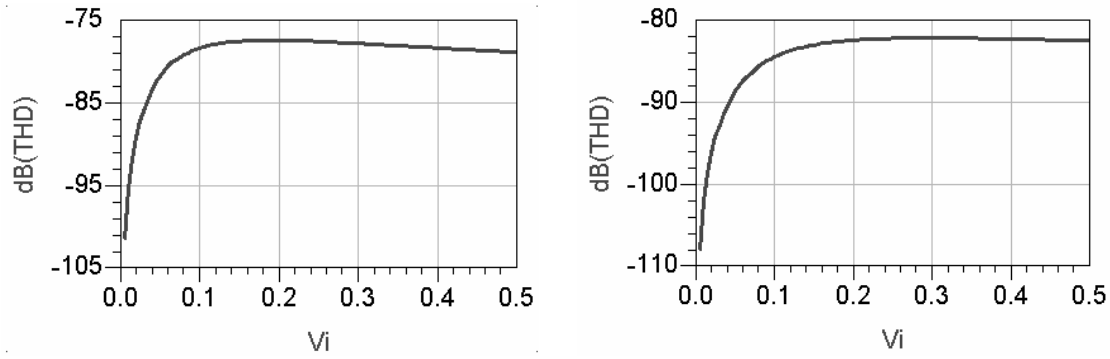
Figure 6.15 PSRR of proposed two-stage operational amplifiers. (a) asymmetrical, (b) symmetrical.

In practice, the variation in the power supply voltages also contributes to the amplifier output fluctuation. This effect can be represented by two voltage sources, $V_{CC} / PSRR^{+}$ and $V_{EE} / PSRR^{-}$, applied at the input of amplifier [1]. It is seen that the PSRR should be maximized to minimize such undesired contributions. Typically the

PSRR also deteriorates as the frequency increases. As shown in Fig. 6.15, at 1*kHz*, the proposed amplifiers exhibit $PSRR^+$ of 107*dB* and 113*dB* respectively, $PSRR^-$ of 78.8*dB* and 84.4*dB* respectively.

The total harmonic distortion (THD) is measured when the amplifier is connected in the unity feedback configuration. Fig. 6.16 shows the variations of THD at 1*kHz* as a function of the input voltage (or the output voltage equivalently). It is observed that the THD degrades dramatically for about 30*dB* as the input voltage increases from 0.01*V* to 0.2*V*, and then remains almost constant as the input voltage approaches 0.5*V*. At 0.5*V*, the amplifiers present THD of -78.8*dB* and -84.4*dB* respectively.

The performances of the proposed operational amplifiers are summarized in Table 6.5.



(a) (b)

Figure 6.16 THD @ 1*kHz* of proposed two-stage operational amplifiers. (a) asymmetrical, (b) symmetrical.

Table 6.5 Performance summary of proposed operational amplifiers.

Performance		asymmetrical	symmetrical
Supply voltage (*V*)		3	3
Supply current (*uA*)		28.56	29.95
Peak output current (*uA*)		>180	>180
Input offset voltage (*uV*)		86	165
CMIR (*V*)	max	$V_{CC} - V_{BE} - V_{CE,SAT}$	$V_{CC} - V_{BE} - V_{CE,SAT}$
	min	V_{EE}	V_{EE}
Output voltage swing (*V*)	max	$V_{CC} - V_{CE,SAT}$	$V_{CC} - V_{CE,SAT}$
	min	$V_{EE} + V_{CE,SAT}$	$V_{EE} + V_{CE,SAT}$
Unity gain frequency (*MHz*)		0.891	1.78
Phase margin (°)		60	60
Open loop gain (*dB*)		47.2	47.5
Slew rate (*mV*/*uS*)		6.7	20
Settling time @ 1% (*uS*)		12.5	4.1
CMRR @ 1*kHz* (*dB*)		61.1	70.3
PSRR @ 1*kHz* (*dB*)	$PSRR^+$	107	113
	$PSRR^-$	60.7	69.9
THD @ 1*kHz*, $V_I = 0.5V$ (*dB*)		-78.8	-84.4

6.4 Low Dropout Voltage Regulator

The LDO is constructed as shown in Fig. 6.1. Although the error amplifier can be replaced with either one of the operational amplifiers shown in Fig. 6.11, the symmetrical design is utilized since it presents better performances than the asymmetrical design in terms of UGF, PSRR, CMRR, THD, slew rate and settling time as listed in Table 6.5. Due to the restriction of the technology for fabrication, the pass element is implemented by a PNP transistor driven by a NPN transistor as depicted in Fig. 6.3. The voltage reference is implemented by a forward-biased diode.

Typically the load of a LDO, as depicted in Fig. 6.1, consists of an output load current (I_L) and associated output impedance (R_L), an output capacitor (C_O) and associated equivalent series resistance (ESR), and bypass capacitors (C_B). The open loop frequency response of such an architecture can be characterized by three poles and one zero, and is potentially unstable [2] [3]. (The detailed expressions of the poles and zero can be found in [2] [3].) The zero plays a significant role in stabilizing the frequency response. It needs to be located before the UGF such that the phase shift at the UGF is less than 180°, which will make the regulator stable. Usually the zero needs to be maintained in a range. If the zero is too low, the highest pole may become lower than the UGF. If the zero is too high, it can be higher than the UGF. These minimum and maximum values of zero determine the stable range of the ESR, which is called *tunnel of death*.

Fig. 6.17 shows the simulated loop gain response of the LDO when $I_L = 100mA$, ESR = 0.5Ω, $C_O = 4.7uF$, $C_B = 0.1uF$ and $C_{COMP} = 1nF$. It presents a DC loop gain of

60*dB* and a UGF of 455*kHz*. A high loop gain is required for high precision because it improves both the line regulation and load regulation. But the stability will be sacrificed. A wide bandwidth is critical for a good load transient response with minimum overshoot as well as undershoot, and fast recovery time.

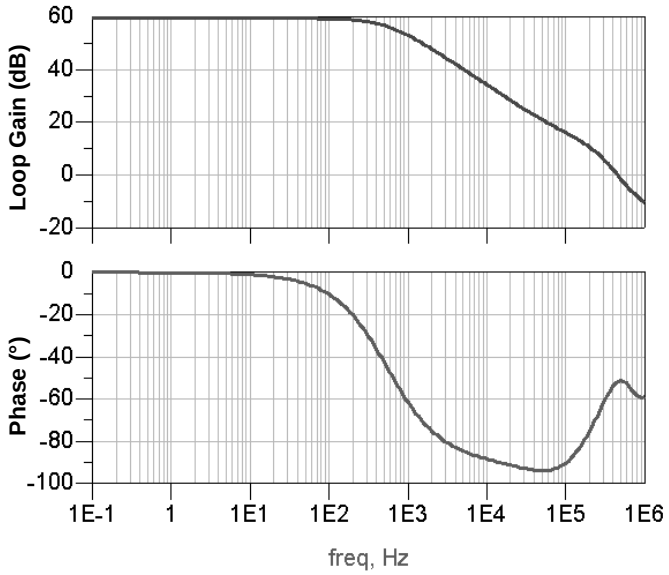
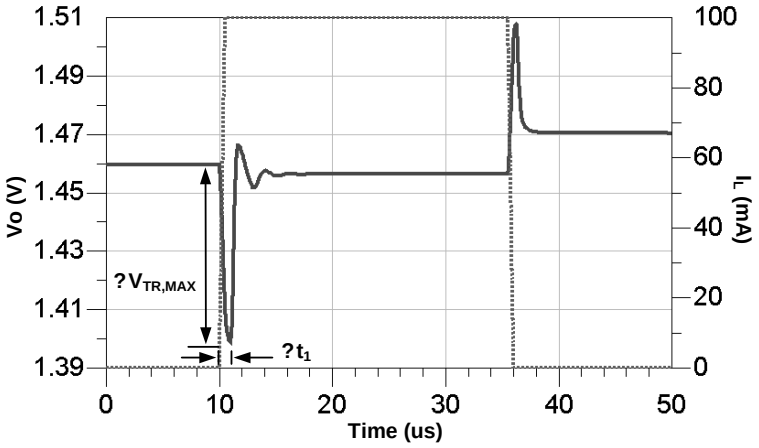


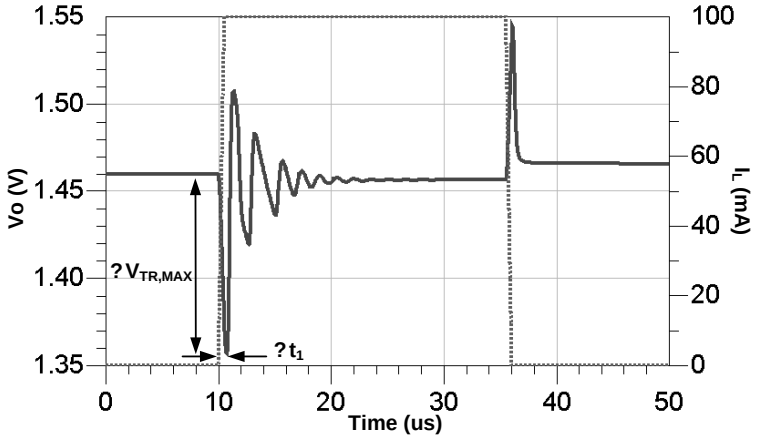
Figure 6.17 Loop gain of the LDO when I_L = 100*mA*, ESR = 0.5Ω, C_O = 4.7*uF*, C_B = 0.1*uF* and C_{COMP} = 1*nF*.

The transient response of the LDO on a step change of load current from 0 to 100*mA* and vice versa is illustrated in Fig. 6.18. The maximum output voltage variation ($\Delta V_{TR,MAX}$) is 61*mV* for ESR = 0.5Ω, and 103*mV* for ESR = 1Ω. It is the result of the voltage variation across the capacitors C_O and C_B, plus the voltage drop across the ESR. It is given by [2] [49]

$$\Delta V_{TR,MAX} = \frac{I_{L,MAX}}{C_O + C_B} \cdot \Delta t_1 + I_{L,MAX} \cdot ESR \tag{6.18}$$



(a)



(b)

Figure 6.18 Transient response of the LDO for a step load change from 0 to 100mA and vice versa when (a) ESR = 0.5Ω, and (b) ESR = 1Ω.

In the case of ESR = 0.5Ω, the first term causes a voltage variation of 14*mV*, while the second term causes 47*mV*. In the case of ESR = 1Ω, the first term results 9*mV*, and the second term goes as high as 94*mV*. It is seen that the second term is much

higher than the first term. The ESR value should be minimized in order to lower the maximum output voltage variation. However the tunnel of death limits the ESR values.

The line regulation, as illustrated in Fig.6.19, is tested under the condition of I_L = 0 and I_L = 60*mA* respectively. For I_L = 0, the output voltage varies from 1.460*V* to 1.523*V* for the input voltage changing from 2*V* to 5*V*, i.e., 21*mV*/*V* of line regulation. For I_L = 60*mA*, the output voltage presents a little bit more deviation. It varies from 1.458*V* to 1.523*V* for the input voltage changing from 2*V* to 5*V*, i.e., 22*mV*/*V* of line regulation. In both cases, the regulation is not maintained when the input voltage drops lower than 1.65*V*, where the output voltage is 1.44*V*, i.e., the dropout voltage is 210*mV*.

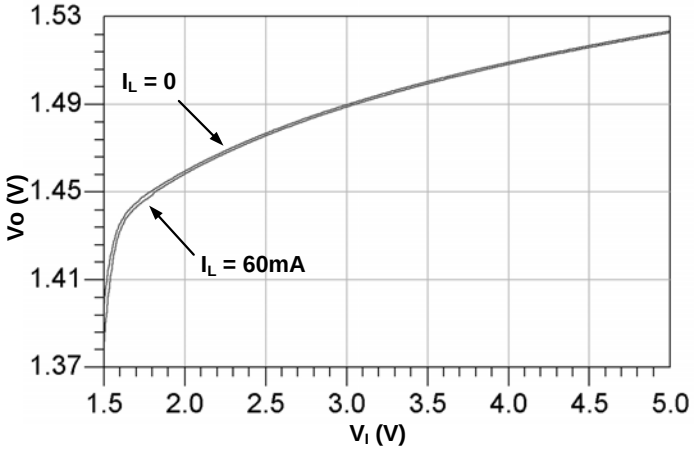


Figure 6.19 Line regulation performance of the LDO.

The LDO achieves the load regulation of 32*uV*/*mA* for V_I = 2*V* and 16*uV*/*mA* for V_I = 5*V* as depicted in Fig. 6.20.

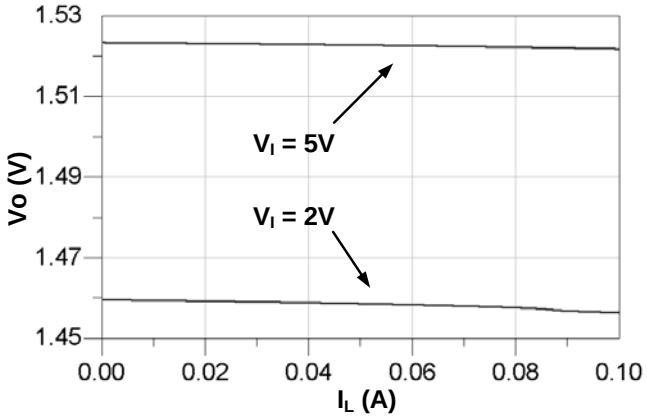


Figure 6.20 Load regulation performance of the LDO.

The noise is also important aspect of performances. Because the linear regulator is generally connected as a post-regulator of the switching regulator, it needs to suppress the noise generated by the switching regulator. The noise performances under the condition of $V_I = 2V$ and $I_L = 100mA$ is illustrated in Fig. 6.21. The LDO exhibits noise spectrum density of $3.14\,uV/\sqrt{Hz}$ at $10Hz$, and $112\,nV/\sqrt{Hz}$ at $100Hz$.

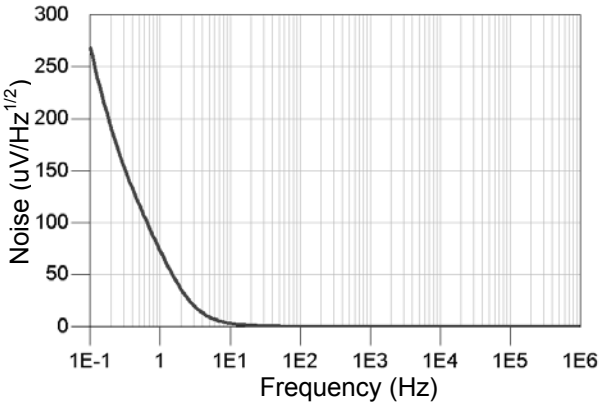


Figure 6.21 Noise spectrum density of the LDO.

The performances of the LDO are summarized in Table 6.6.

Table 6.6 Performance summary of proposed LDO.

Quiescent current (*uA*)	102
Maximum load current (*mA*)	>100
Dropout voltage (*mV*) @ I_L = 60*mA*	210
Line regulation (*mV*/*V*) @ I_L = 60*mA*	22
Load regulation (*uV*/*mA*) @ V_I = 2*V*	32
Maximum output voltage variation (*mV*)	103
Noise @ V_I = 3*V*, I_L = 100*mA*, 10*Hz* ($uV/\sqrt{Hz}$)	3.14
ESR range (Ω)	0 ~ 1

6.5 Summary

This chapter stressed the importance of line regulation performance of reference circuits. This aspect of performance was to be improved with the linear low-dropout voltage regulator. The key components in the prevailing LDO architecture were discussed. For high efficiency, P-type pass elements were preferred. For the same reason, the error amplifier was designed with the class AB output characteristics. Then the LDO was assembled with the proposed two-stage class AB operational amplifier, band-gap reference, PNP pass transistor, and sampling resistors. The LDO regulated the raw input voltage, suppressed the noise, and generated an output voltage suitable as the power supply of other circuits.

CHAPTER 7

APPLICATIONS OF LINEAR REGULATOR

The line regulation of circuits can be significantly enhanced if the raw power supply voltage is regulated by the linear regulator. In this chapter, the linear low-dropout voltage regulator will be applied to the band-gap references developed in Chapter V to improve their poor line regulation performances. Then the effect of the linear regulator is further stressed using a variable gain amplifier.

7.1 Band-gap Reference with Linear Regulator

The line regulations of band-gap references developed in Chapter V are measured by varying the input voltage from 2*V* to 5*V*. Without the linear regulator, band-gap reference A´ and B´ present line regulations of 3270*ppm*/*V* and 10051*ppm*/*V* respectively. With linear regulator, the supply voltage is regulated between 1.458*V* to 1.523*V* as the input voltage varies, which causes only 68.2*ppm*/*V* and 248.8*ppm*/*V* change of reference voltage of band-gap references A´ and B´ respectively. It is obvious that the regulator significantly enhances the line regulation performance.

7.2 Variable Gain Amplifier with Linear Regulator

The linear regulator generates a well-regulated low-noise output voltage, which will be used as the power supply for other circuits. Such a supply voltage is important

for the performance of circuits. In this section the effect of the linear regulator will be illustrated using a variable gain amplifier (VGA).

7.2.1 Introduction to Variable Gain Amplifier

The variable gain amplifier is the most critical component in the automatic gain control (AGC) circuits which play significant role in the transceiver architecture for wireless communication. A basic requirement of VGA is the gain should exhibit linear-in-dB variation with respect to the control voltage. And the gain range in which the linearity can be maintained should be wide, e.g., at least 80dB is required in the CDMA systems [56] [57].

The gain control can be realized in two approaches – digital and analog. Generally the digital control is obtained by switching on and off the resistor in a R-ladder [58] [59] or R-array [60] to discretely adjust the gain. Such discontinuity can be avoided in the analog control. For BJT technology, due to the inherent exponential relationship between the collector current and the base-emitter voltage, the continuous analog control can be obtained easily by varying the bias current [61] [62] or steering the current [56] [57]. In CMOS technology, the linear-in-dB characteristics can only be achieved with the exponential-function-approximation circuits [63] [64]. The gain range obtained in this way is typically small. For CMOS or Bi-CMOS technology, there is another option which is to use the emitter-degenerated differential pair as depicted in Fig. 7.1. The degeneration resistor is implemented using the channel resistance R_{DS} of a triode-region MOS transistor. However the gain cannot be varied exponentially due to the linear relationship between R_{DS} and V_{GS}. Hence it is desired to have a degeneration

"resistor" which can achieve the exponential gain control. This is realized by employing BJT transistors as emitter degeneration resistors in the differential pair.

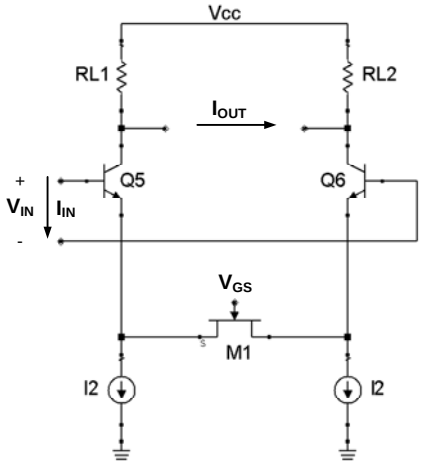


Figure 7.1 Emitter degenerated differential pair with MOS implementation of the degeneration resistor.

7.2.2 BJT Implementation of Degeneration Resistors

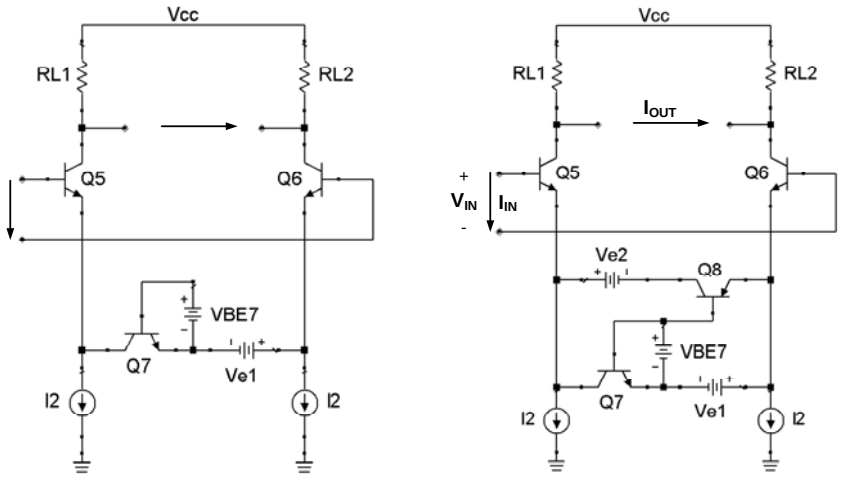
A design of the BJT implementation of emitter-degeneration resistor in the differential pair is shown in the Fig. 7.2 (a). The differential current gain is easy to be derived by knowing the fact that the differential output current is equal to twice the collector current of Q_7 if all the base currents are neglected, and is given by

$$A_I = \frac{I_{OUT}}{I_{IN}} = \frac{2 \cdot I_S}{I_{IN}} \cdot \exp\left(\frac{V_{BE7}}{V_T}\right) \tag{7.1}$$

It is seen that the gain can be varied exponentially by V_{BE7}. Compared to the MOS degeneration resistor, BJT implementation requires a voltage source, V_{e1}, to guarantee Q_7 to operate in the active region. The a voltage source V_{e1} lowers the emitter

voltage of Q_7 to a value such that the voltage drop across the collector-emitter junction of Q_7 is at least greater than the collector-emitter saturation voltage. The value of V_{e1} is calculated to be

$$V_{e1} = V_{BE1} - V_{BE2} + V_{CE7} - V_{IN} \tag{7.2}$$



(a) (b)

Figure 7.2 Emitter degenerated differential pair with BJT implementation of (a) "unidirectional", and (b) "bidirectional" degeneration resistor.

Since the base-emitter voltage will not change significantly with the collector current, the difference between V_{BE1} and V_{BE2} is usually negligible. Hence to guarantee V_{CE7} greater than the collector-emitter saturation voltage, which is assumed to be 0.2*V*, V_{e1} should be greater than

$$V_{e1} \geq 0.2 V_{IN} \tag{7.3}$$

In this design, V_{e1} is chosen to be 0.7*V*, which is greater than the minimum value of 0.2*V*, in order to reversely bias the base-collector junction of Q_7, and ensure Q_7 to operate in the forward-active region.

Unlike the MOS transistor of which the source and drain are physically interchangeable due to the symmetrical structure, the emitter and collector of a BJT transistor are not interchangeable. Consequently the design in Fig. 7.2 (a) is considered "unidirectional", i.e., V_{IN} must be positive. To make the design "bidirectional", a PNP transistor Q_8 is added in shunt with Q_7 as shown in Fig. 7.2 (b), where a voltage source V_{e2} has the same function as V_{e1} in Fig. 7.2 (a) and is also set to 0.7*V*. To realize the desired operation mode, Q_7 and Q_8 need to be turned on in a complementary fashion according to the differential input voltage, that is, when $V_{IN} > 0$, Q_7 is turned on and Q_8 is cut off; when $V_{IN} < 0$, Q_8 is turned on and Q_7 is cut off. This required complementary operation mode is achievable. By inspecting the loop formed by Q_7, Q_8 and V_{e1}, it is found that

$$V_{EB8} + V_{BE7} = V_{e1} \tag{7.4}$$

Since V_{e1} is chosen to be 0.7*V*, when either Q_7 or Q_8 is turned on, the forward bias voltage of approximately 0.7*V* in the base-emitter junction will force the base-emitter voltage of the other transistor equal to 0*V*. Hence when one of Q_7 and Q_8 operates in the active region, the other one must be cut off. Also when both V_{BE7} and V_{EB8} are less than 0.7*V*, both transistors are cut off, e.g., under the condition of $V_{IN} = 0$, $V_{BE7} = V_{EB8} = 0.35V$.

7.2.3 Gilbert-Cell-Based Variable Gain Amplifier

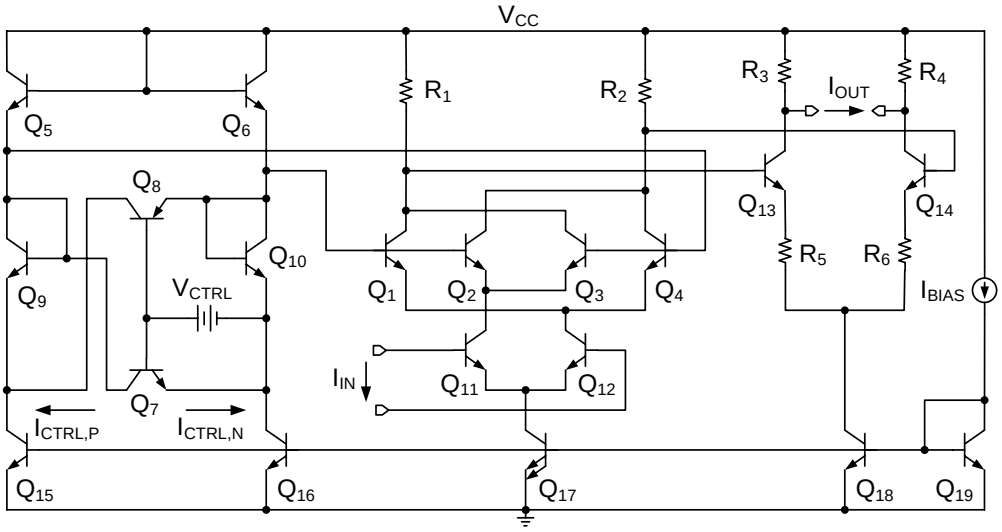


Figure 7.3 VGA concept circuit with the gain controlled by BJT degeneration resistor.

The BJT degeneration resistors can be applied to the VGA design. Such a circuit is shown in Fig. 7.3. The double-balanced Gilbert cell ($Q_1 \sim Q_4$) is employed as the core cell of the VGA. To compensate for the hyperbolic tangent transfer characteristics of the basic cell, Q_5 and Q_6 are added as the predistortion circuits [1]. The emitter-degeneration part consists of $Q_7 \sim Q_{10}$. Compared to the "bidirectional" design in Fig. 7.2 (b), voltage sources V_{e2} and V_{e1} are replaced by two diode-connected real transistors Q_9 and Q_{10}. Q_9 and Q_{10} are no longer placed in series with Q_7 and Q_8 respectively, but in series with Q_6 and Q_5 to generate approximately $0.7V$ voltage drop. This change will not affect the analysis completed earlier. The collector-emitter currents flowing through degeneration transistors Q_7 and Q_8, labeled as $I_{CTRL,N}$ and $I_{CTRL,P}$ respectively, are

deemed as the control current, I_{CTRL}. Then it can be found that the magnitude of current gain is given by

$$|A_I| = I_{CTRL} / I_2 \tag{7.5}$$

When Q_7 conducts, $I_{CTRL} = I_{CTRL,N}$, and (7.5) can be rewritten as

$$|A_I| = \frac{I_{S,N}}{I_2} \exp\left(\frac{V_{CTRL}}{V_T}\right) \tag{7.6}$$

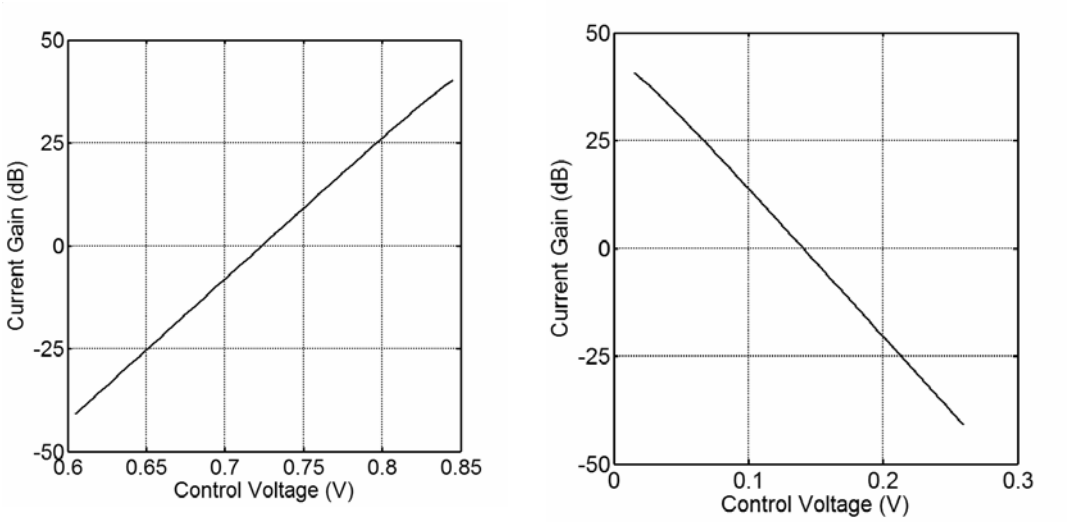
When Q_8 conducts, $I_{CTRL} = I_{CTRL,P}$, and (7.5) can be rewritten as

$$|A_I| = \frac{I_{S,P}}{I_2} \exp\left(\frac{V_{BE10} - V_{CTRL}}{V_T}\right) \tag{7.7}$$

7.2.4 Simulation Results

The VGA is simulated under 3*V* supply voltage. It consumes 4*mA* current. The current gain variations at 100*MHz* are shown in Fig. 7.4 (a) and (b) for the cases when Q_7 is "ON" and Q_8 is "ON" respectively. For the control signal, V_{CTRL}, changing from 0.605*V* to 0.845*V*, Q_7 conducts the control current. The gain is varied from -40.9*dB* to 40.3*dB* with error less than 1*dB*. High third-order input interception point (IIP_3) is required at low gain, while low noise figure (NF) is required at high gain. The IIP_3 is -13.3*dBm* at the minimum gain. The NF is 9.8*dB* at the maximum gain. Another mode of operation is to turn on Q_8, which is achieved when V_{CTRL} changes from 0.015*V* to 0.260*V*. The gain is varied from 40.8*dB* to -41.0*dB* with error less than 1.5*dB*. The IIP_3 is -11.6*dBm* at the minimum gain. The NF is 9.4*dB* at the maximum gain. In both cases, the gain error mainly occurs at high gain. And the dynamic range can be compromised

for enhanced IIP_3 and NF performances. The results confirm the feasibility of utilizing BJT degeneration resistors to obtain accurate linear-in-dB gain characteristics.



(a) (b)

Figure 7.4 Linear-in-dB variation of current gain w.r.t. the floating control voltage. (a) Q_7 is "ON", (b) Q_8 is "ON".

The influence of linear regulator can be seen by the gain deviation caused by the input voltage variation. Without the proposed linear regulator, the gain varies for 1.046*dB* maximally as the raw input voltage varies from 3*V* to 5*V*, i.e., 0.523*dB*/*V*. This is obtained when V_{CTRL} is set to 0.035*V*, 0.2*V*, 0.725*V* and 0.79*V*. With the regulator, the power supply voltage is regulated from 2.964*V* to 3.094*V* as the raw input voltage varies from 3.5*V* to 5*V*, which causes a maximum gain variation of 0.066*dB* or 0.044*dB*/*V* only.

7.3 Summary

Linear low-dropout voltage regulators aim at eliminating or alleviating the dependence of output characteristics of circuits on their power supply. With the application of the linear regulator, the band-gap references present much less line regulation. Also the linear regulator is applied to a VGA to reduce the dependence of gain on supply voltage.

CHAPTER 8

CONCLUSIONS AND FUTURE WORK

8.1 Conclusions

Temperature drift is the most critical issue in the design of band-gap reference circuits. This drift needs to be reduced by means of compensations, e.g., the weighted sum of PTAT and I-PTAT terms. However such compensation is only able to eliminate the term linearly dependent on temperature, i.e., the first-order compensation is achieved. The temperature drift after the first-order compensation can be less than 50 *ppm*/°*C*. Further reduction of the drift can be achieved with the curvature compensation, in which the nonlinearly temperature dependent terms, primarily the second-order term, is cancelled by an intentionally introduced nonlinear term. The curvature corrected drift can be less than 10 *ppm*/°*C*. However generation of such a nonlinear term is usually difficult, especially in the low-voltage design environment. This problem is solved in this work by forward biasing the base-collector junction of one BJT transistor, which will induce a current component exponentially proportional to V_{BC}. With proper adjustments of V_{BC}, this V_{BC}-dependent current is able to accomplish the required nonlinear compensation. Four current-mode reference circuits are developed based on this technique. Two of them implement the current-addition scheme, and present curvature corrected temperature drifts of 8.45 *ppm*/°*C* and 1.74 *ppm*/°*C* respectively in

their revised version. The other two implement the current-subtraction scheme, where the V_{BC}-dependent current functions for linear compensation only. And the first-order compensated drifts of 76.2 *ppm*/°*C* and 25.2 *ppm*/°*C* are obtained respectively. Another reference circuit implements the current-multiplication scheme using the square-root cell, and shows a first-order compensated drift of 76.0 *ppm*/°*C*.

In addition to temperature drift, reference circuits have other aspects of performance to be characterized, such as current efficiency, line regulation, load regulation, PSRR, and noise spectrum. Each of them has a role to play in the overall performance of reference circuits. To take into account all of them in the overall performance evaluation, the GSPT comes into play. Each aspect of performance, or each DOP, is described in terms of the FV, and evaluated with respect to predetermined task demands. For certain DOP, if task demands are satisfied at every operating point, the DOP will represent the excess capacity of the circuit for the specific task. If task demands are not satisfied at every operating point, the DOP will represent the FDD of the circuit for the specific task. In the first case, the DOP value is always greater than unity. The larger the DOP value, the larger the excess capacity. In the second case, the DOP value is always less than unity. As the circuit is able to fulfill the task demands at more operating points, the DOP value approaches unity. The closer the DOP value approaches unity, the larger the FDD. After each DOP is determined, the overall performance is ready to be evaluated by the CPC which is equal to the product of all the DOP values. For task demands of 10 *ppm*/°*C* in temperature drift, 250 *ppm*/*V* in line regulation, -50*dB* in PSRR, $100\,nV/\sqrt{Hz}$ in noise, 0.5 in current efficiency, and $100\,\Omega$

in load regulation, reference circuit B presents the largest CPC value, or equivalently the best overall performance among all the five circuits under consideration.

The functionality analysis shows that the line regulation is poor for every circuit. For improvement, the noisy raw supply voltages should go through a linear voltage regulator before being fed to the reference circuits. Typically the linear regulator consists of a voltage reference, an error amplifier, a pass element, and sampling resistors. The error amplifier largely determines most aspects of performance of the regulator, e.g., a large loop-gain is necessary for a high precision output voltage, a wide loop-gain bandwidth can effectively improve the PSRR, a high slew rate and wide loop-gain bandwidth can result in a good load transient response like fast recovery time, minimum overshoot and undershoot [55]. Moreover the error amplifier needs to have high current driving capability to provide the base current of the bipolar pass element. When the regulator operates in the dropout region, the current gain drops dramatically and causes the base current to go as high as the output current. Thus two class AB output stages, namely asymmetrical and symmetrical, are developed for the error amplifier. The class AB characteristics are acquired by implementing the current-subtraction technique in combination with harmonic mean principle. In asymmetrical design, the current subtraction operation is applied directly to regulate the minimum current of the push transistor. In symmetrical design, the current subtraction operation is applied directly to both pull and push transistors. The amplifier with symmetrical implementation of class AB control presents better performance in terms of unity-gain bandwidth, CMRR, PSRR and THD. It is selected as the error amplifier in the regulator.

With all the necessary components, the linear low-dropout voltage regulator is assembled and applied to the band-gap reference to significantly enhance its line regulation performance.

8.2 Future Work

The concept of current division compensation was demonstrated theoretically. The next step is to design the current component with required temperature coefficients.

In the design of capacitive startup circuitry, the value of C_1 and C_2 is dependent on V_{CC}. As V_{CC} decreases, the divided voltage may become lower than the required voltage, and unable to turn on Q_{S1}. Therefore, the ratio of C_2 to C_1 can only be chosen to ensure normal start-up for a certain range of V_{CC}. Such dependence on V_{CC} should be minimized in the future design.

In the class AB output stage, implementation of the harmonic mean principle necessitates a translinear loop, which demands a minimum supply voltage of $2V_{BE} + V_{CE,SAT}$ for proper operation. To approach the theoretical limits of $V_{BE} + 2V_{CE,SAT}$, the translinear loop cannot exist in the circuit. Thus a new principle is needed to combine with the current-subtraction technique for class AB control.

APPENDIX A

SATURATION CURRENT TEMPERATURE DEPENDENCE

The saturation current is given as [1] [17]

$$I_S(T) = \frac{qAn_i^2(T)\overline{D}(T)}{Q_B} \tag{A.1}$$

where $q = 1.6 \times 10^{-19}\, coulombs$ is the electron charge, A is the emitter area, and $Q_B = W_B N_B$ is termed as the Gummel number which is the number of doping atoms per unit area in the base region. N_B represents the impurity profile in the base region, and W_B is the effective base width.

The temperature dependent expression of the intrinsic carrier concentration n_i is given as

$$n_i(T) = \sqrt{N_C(T)N_V(T)\exp\left[-\frac{V_G(T)}{V_T}\right]} \tag{A.2}$$

where N_C and N_V are conduction band and valence band effective density of states respectively. They are both proportional to $T^{3/2}$. Equ. (A.2) can be written as

$$n_i^2(T) = B \cdot T^3 \exp\left[-\frac{V_G(T)}{V_T}\right] \tag{A.3}$$

The "effective" diffusion constant, $\overline{D}$, is associated with the "effective" minority carrier mobility, $\overline{\mu}$, by the Einstein relation

$$\overline{D}(T) = V_T\,\overline{\mu}(T) \tag{A.4}$$

where the temperature dependence of $\overline{\mu}$ is given by

$$\overline{\mu}(T) = C \cdot T^{-n} \tag{A.5}$$

Substituting $n_i^2(T)$ and $\overline{D}(T)$ with Equ. (A.3), (A.4) and (A.5), after rearrangement, the saturation current is obtained.

$$I_S(T) = \frac{kABC}{Q_B} \cdot T^{4-n} \exp\left[-\frac{V_G(T)}{V_T}\right] \tag{A.6}$$

At a certain reference temperature, T_r, I_S is equal to

$$I_S(T_r) = \frac{kABC}{Q_B} \cdot T_r^{4-n} \exp\left[-\frac{V_G(T_r)}{V_{Tr}}\right] \tag{A.7}$$

Dividing Equ. (A.6) by Equ. (A.7) gives

$$\frac{I_S(T)}{I_S(T_r)} = \left(\frac{T}{T_r}\right)^{\eta} \exp\left[\frac{V_G(T_r)}{V_{Tr}} - \frac{V_G(T)}{V_T}\right] \tag{A.8}$$

where $\eta = 4 - n$.

APPENDIX B

IMPORTANT SIMULATION SETUPS

The setup for simulating and measuring the CMRR of operational amplifier is shown in Fig. B.1 [66] [67]. And the CMRR is obtained as

$$CMRR \approx v_I / v_O \tag{B.1}$$

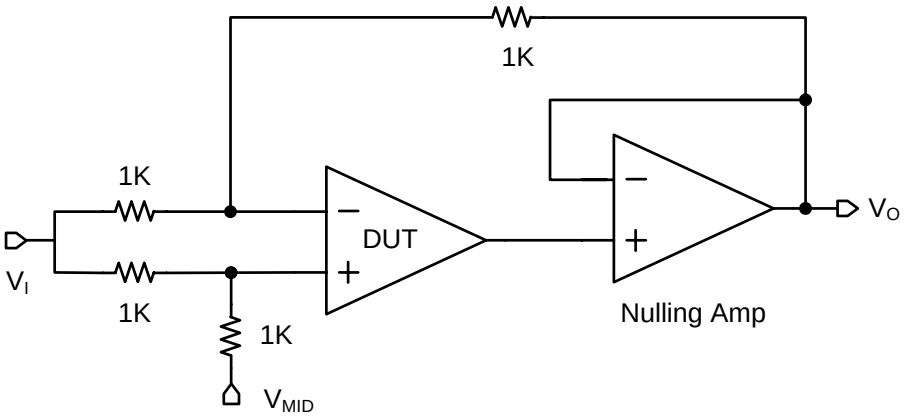


Figure B.1 CMRR simulation and measurement setup.

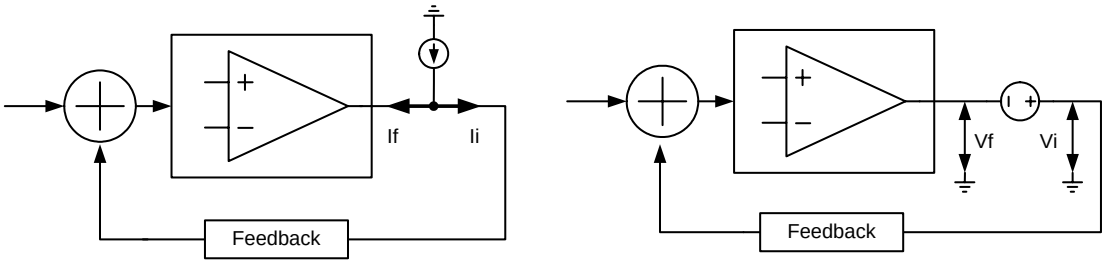


Figure B.2 Loop gain simulation setup.

The setup for simulating the loop gain of a feedback system is illustrated in Fig. B.2 [65], and the loop gain is given by

$$LG = \left(A_i \cdot A_v - 1\right) / \left(A_i + A_v + 2\right) \tag{B.1}$$

where

$$A_i = i_f / i_i \tag{B.2}$$

$$A_v = v_f / v_i \tag{B.3}$$

Fig. B.3 [68] depicts a universal test setup. Open loop gain can be measured by setting V_{ic} to zero and V_{id} to ±1V. CMRR can be measured by setting V_{id} to zero and V_{ic} to ±1V.

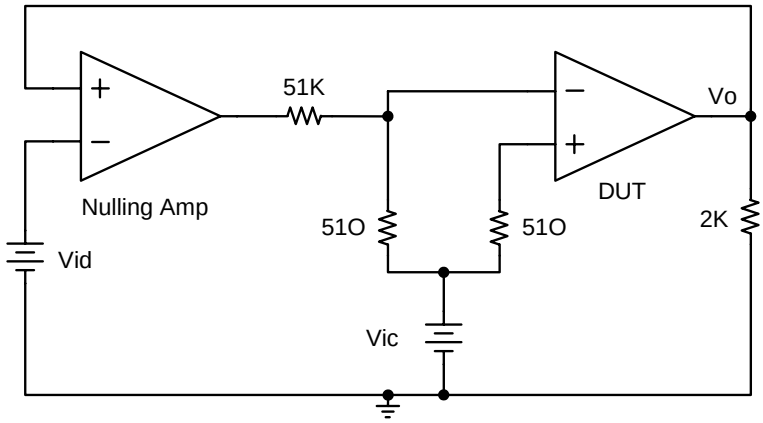


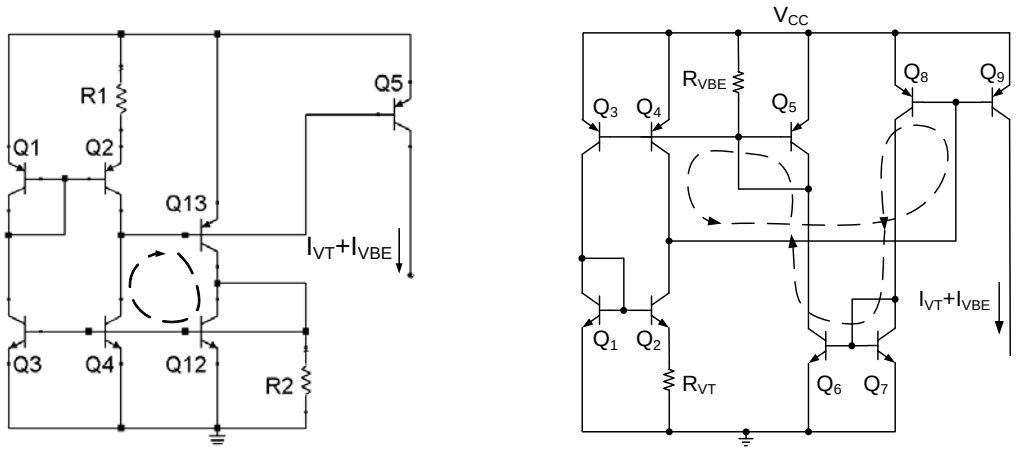
Figure B.3 Universal test circuit to measure CMRR and loop gain.

APPENDIX C

EAGLE 17 RUN MEASUREMENTS

In Eagle 17 run, two band-gap voltage references and one OpAmp were fabricated.

The final version of the band-gap references, shown in Fig. 5.15, adopts Fig. C.1(b) to generate the first-order compensated current. The circuit in Fig. C.1(a) achieves the first-order compensation in the same way. However, Fig. C.1(a) is not stable due to the positive feedback loop formed by Q_{13}, Q_{12} and Q_4 as indicated by the dashed line. The loop gain is equal to the transistor current gain, β, which is greater than unity. Compared to Fig. C.1(a), Fig. C.1(b) has negative feedback loop formed by Q_8, Q_7, Q_6, Q_5 and Q_4 as indicated by the dashed line. It also has loop gain of β.

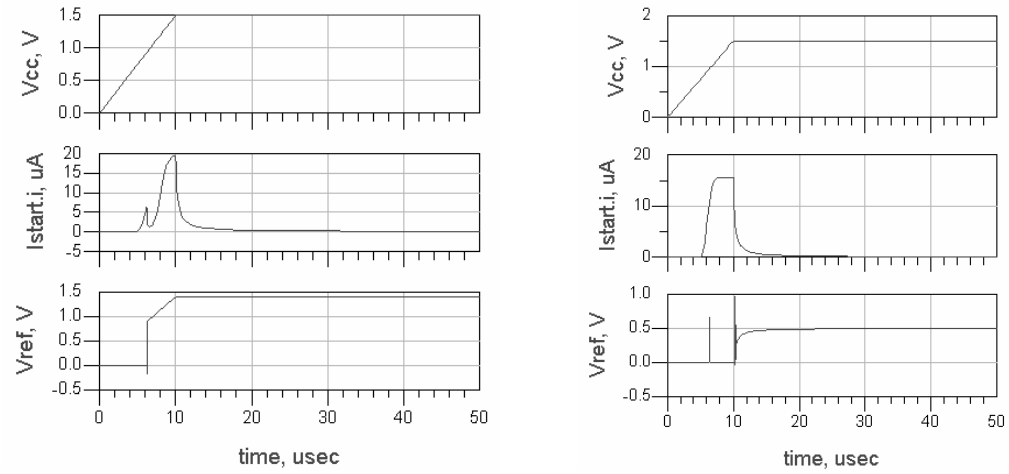


(a) (b)

Figure C.1 First-order compensation circuits (a) unstable (b) stable.

Whether the circuit is stable or not can be verified from the startup processes. Fig. C.2(a) and C.2(b) illustrate the startup process of I_{VBC}-compensated band-gap reference A using Fig. C.1(a) and C.1(b) as the first-order compensation circuit

respectively. The stability problem of Fig. C.1(a) causes transistors to go to saturation, and results in the output reference voltage to be always around 200*mV* below the power supply. This is seen from both simulation and measurement. With Fig. C.1(b), the whole reference circuit is stable, and able to generate the desired reference voltage of 500*mV*.



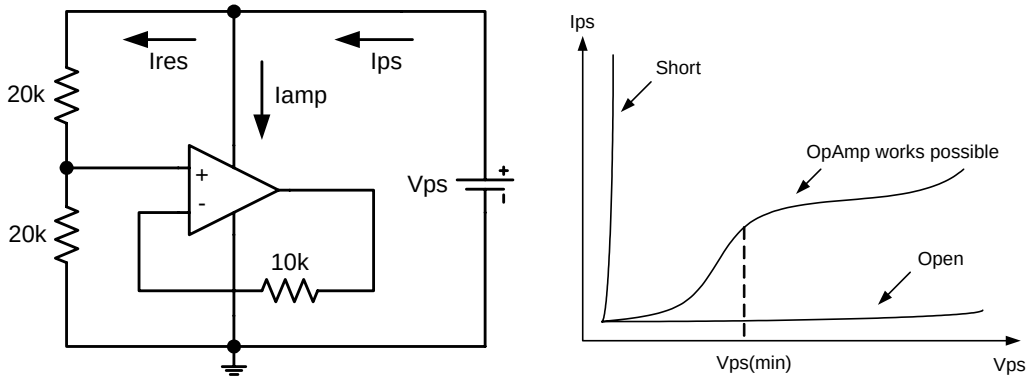
(a) (b)

Figure C.2 Startup process of I_{VBC}-compensated band-gap reference A with the first-order compensation circuit implemented using (a) Fig. C.1(a), and (b) Fig. C.1(b) where V_{cc} is the power supply voltage, I_{start} is the startup current, and V_{ref} is the output reference voltage.

Because the stability problem was found after the submission for fabrication, Fig. C.1(a) was the one fabricated in the Eagle 17 run. It was revised to Fig. C.1(b), which is the one included in the dissertation.

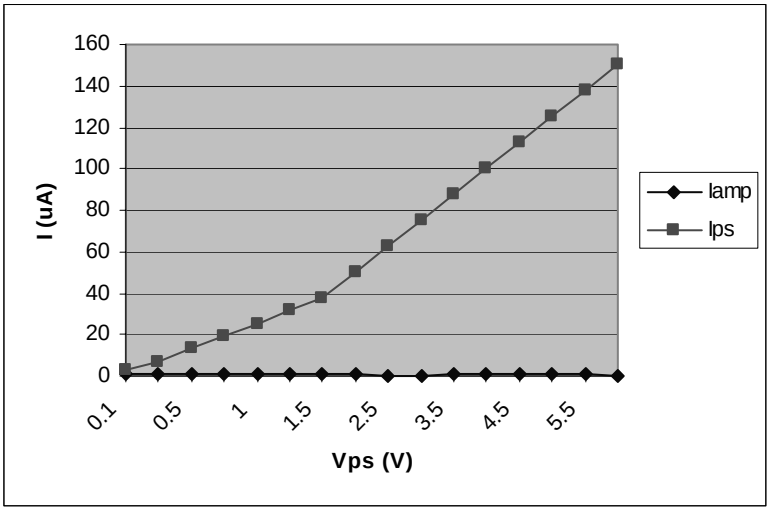
However the fact that transistors operate in the saturation region demonstrates that the startup circuitry works appropriately. It is able to drive the self-biased circuit out of the dead zone as desired.

For an operational amplifier (OpAmp), the first test is open/short circuit test using the circuit shown in Fig. C.3(a). By inspecting the characteristics of the current, as shown in Fig. C.3(b), the OpAmp can be determined if it is open circuit or short circuit. If either of these happened, no further test will be necessary [68]. The test result of the OpAmp fabricated in Eagle17 run is shown in Fig. C.4(a). It reveals that the OpAmp is open circuit. A 741 OpAmp is used for comparison. The test result of the 741 OpAmp is shown in Fig. C.4(b). That is the desired characteristics of the current as a function of the supply voltage.

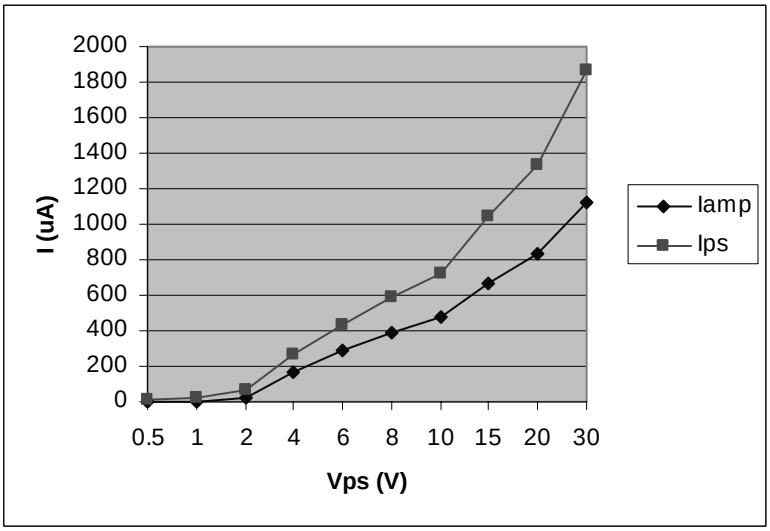


(a) (b)

Figure C.3 Open/short verification test circuit (a) configuration, (b) characteristics.



(a)



(b)

Figure C.4 Open/short circuit test results of (a) the OpAmp fabricated in Eagle 17 run (b) 741 OpAmp.

Since the OpAmp adopts Fig. C.1(a) to generate the bias current, the malfunction of the bias circuit results in the malfunction of the OpAmp. But it is not known whether the core of the OpAmp functions well or not. The OpAmp was tested in

the inverting and non-inverting configurations. It cannot generate the desired outputs in either case.

The unsuccessful test of the band-gap references and OpAmp is caused by the local positive feedback loop in the first-order temperature compensation circuit. This problem was not found before the submission of the design. Because of this problem, it is unable to test whether the proposed curvature compensation scheme for the band-gap reference and the developed Class AB control scheme for the OpAmp can function as desired. Therefore a circuit should be developed such that each feature can be tested individually, that is, the circuit should be a design-for-test (DFT) circuit. Each circuit should just have one new feature with the rest of the circuit implemented by any fail-safe circuit. For example, if the bias of the OpAmp were implemented by the basic circuits, e.g., a resistor in series with a diode-connected transistor, it would be possible to run the Class AB control test. The I_{VBC}-compensated band-gap reference A and B should employ the conventional first-order compensation circuits, e.g., the one in Fig. 5.6, such that the I_{VBC} curvature compensation method can be tested. When every feature is tested successfully, then it is ready to assemble all of them together, and run the final test.

APPENDIX D

ACRONYMS

AGC - automatic gain control

CMIR - common mode input range

CMRR - common mode rejection ratio

CPC - composite performance capacity

CTAT - conversely-proportional-to-absolute-temperature

DOP - dimension of performance

DV - demand volume

ESR - equivalent series resistance

FDD - fulfillment degree of demands

FV - functionality volume

GSPT - general systems performance theory

IIP_3 - third-order input interception point

I-PTAT - inversely-proportional-to-absolute-temperature

LDO - low dropout regulator

MPS - multidimensional performance space

NF - noise figure

PCE - performance capacity envelope

PES - performance vs. environment space

PM - performance margin

PSRR - power supply rejection ratio

PTAT - proportional-to-absolute-temperature

SGP - Spice Gummel-Poon

TCE - task capacity envelope

TD - tradeoff degree

THD - total harmonic distortion

UGF - unity gain frequency

VGA - variable gain amplifier

VCO - voltage-controlled oscillator

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