An Ultra-Low Power CMOS PTAT Current Source

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***Abstract*— A low-voltage, ultra-low-power sub-threshold proportional to absolute temperature (PTAT) current source is proposed. The new topology generates the PTAT current from the ratio between the drain currents of two transistors in subthreshold operation. Linearity is analyzed and a compensation strategy to improve it is developed. This is the first time such a design scheme is presented. Total current drain for the circuit is approximately 3.8 μA with a minimum supply voltage of 1 V and a PSRR greater than 50 dB at room temperature. The linear range is at least from -40 °C to 125 °C. The performance of the proposed reference is compared with several existing designs.**

I. Introduction

There are many contexts in which a small, low-power-consumption PTAT source is very valuable. Power, area, speed and temperature range factors are important constraints in modern VLSI design. As transistor dimensions decrease, it is possible to lower the operating voltage of circuits, and dynamic voltage scaling (DVS) has been successfully implemented in several commercial applications to reduce power consumption. Excessive temperature on a microchip due to increased power density is being addressed by DVS, considered an efficient dynamic thermal management (DTM) technique. DVS/DTM automation techniques require thermal sensors that operate over a range of supply voltages. Therefore, temperature sensor designs such as this one are needed to address these engineering challenges.

The design goals of this study are to implement a PTAT current source capable of maintaining stable output despite variation in power supply voltage and CMOS process parameters; to quantify linearity and to maintain that linearity at an acceptable level; to minimize power consumption; and to achieve a design that meets or exceeds these metrics as compared to other sensor designs. The basic principle to obtain the PTAT current presented in this work was inspired by the CMOS sensor introduced in Reference [1]. The source proposed here uses a different topology and compensation to improve linearity. A circuit to generate the independent-of-ambient-temperature (IOAT) reference current required by the PTAT reference is also presented in this work. All simulations reported here were performed using the TSMC 180 nm CMOS process parameters with the Spectre simulator. Results are reported for the temperature range valid for these parameters: -40 °C to 125 °C. The proposed source is linear in the entire range. Total current drain for the circuit is around 3.8 μA with a minimum supply voltage of 1 V and a PSRR greater than 50dB at room temperature.

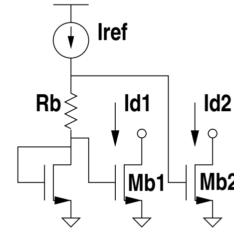

Fig. 1. I_{D1} and I_{D2} generator

The paper is organized as follows. The basic principle of operation of the PTAT is described first, followed by consideration of non-ideal effects and a compensation strategy. The IOAT source is described next. After that simulation results and a comparison of the main performance parameters of the proposed design with several existing designs are presented.

II. Principle of Operation and Design Description

A. PTAT Source

In this work, the drain current for transistors in the sub-threshold region operating as a current source (I_D) is modeled by (Eq. (1.252) in [3])

$$I_D = \frac{W}{L} I_t \exp\left(\frac{V_G - V_{TH}}{nV_T}\right) , \quad (1)$$

where W and L are the width and length of the channel, I_t is a current that is temperature-dependent, V_{TH} is the threshold voltage, V_G is the gate-source voltage, n is the subthreshold slope parameter and V_T is the thermal voltage, given by

$$V_T = \frac{kT}{q} , \quad (2)$$

where k is Boltzmann's constant, T is the absolute temperature, and q is the electron charge. Consider the circuit shown in Fig. 1. The IOAT reference current (I_{ref}) induces a voltage drop over resistor R_b. Transistors Mb1 and Mb2 have gate voltages separated by the small voltage over R_b. The Mb1 and Mb2 branches respectively generate two slightly different currents, I_{D1} and I_{D2}. If channel length modulation is neglected

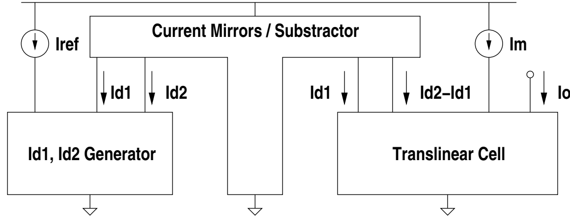

Fig. 2. Block diagram of PTAT generator

and transistor dimensions are matched, from Eq. (1), I_{D2}/I_{D1} is given by

$$\frac{I_{D2}}{I_{D1}} = \exp\left(\frac{I_{ref}R_b}{nV_T}\right) . \quad (3)$$

A first-order Taylor series expansion of Eq. (3) results in

$$\frac{I_{D2}}{I_{D1}} \approx 1 + \frac{I_{ref}R_b}{nV_T} . \quad (4)$$

A current proportional to V_T can be obtained as follows:

$$\frac{1}{\frac{I_{D2}}{I_{D1}} - 1} = \frac{I_{D1}}{I_{D2} - I_{D1}} \approx \frac{nV_T}{I_{ref}R_b} . \quad (5)$$

Equation (5) can be implemented using a translinear cell (analog multiplier) with 4 currents. In addition to I_{D1} and I_{D2}, the difference of these currents is generated and sent to the translinear cell as shown in Fig. 2. This is an improvement over a previously presented topology [1] that requires a multiplier with 6 currents plus the calculation of an additional current. The complete schematic for the PTAT reference is shown in Fig. 3. All transistors in this schematic operate in the weak inversion region. Current mirrors operate with a V_{DS} of at least 100 mV and are cascoded to reduce systematic error and increase rejection to variations in the supply voltage. All current mirrors use a system that is effectively dual-input and cascoded (Fig. 4.13 in [3]): the reference current generation circuit has a dual-input current mirror where the first current is used to generate the bias voltage for the common-gate transistor, and the second branch functions as the actual mirror. All common-gate transistors in current mirrors are biased using the same voltage (V_{bb} for PMOS or V_{bn} for NMOS); this is an approximation to dual-input operation and significantly decreases the required area and current for the design. The minimum voltage drop required by the cascode current sources is thus around 200 mV. All gate-source voltages are smaller than 400 mV. This scheme increases the power supply rejection ratio while allowing low-voltage operation.

Starting from the left side in Fig. 3, I_{D1} and I_{D2} are generated by transistors Mb1 and Mb2. These two currents generate the mirror biasing voltages V_{b1} and V_{b2}, respectively. I_{D1} is copied with a PMOS mirror and then again by an NMOS mirror to produce $I_{D2} - I_{D1}$. This was made in order to optimize the size of Mb1 and Mb2 for low n variation (short channel) as opposed to current mirror operation (long channel). The accuracy of $I_{D2} - I_{D1}$ is critical: this term is near an order of magnitude smaller than I_{D1} and this results in an amplification in the relative error of the final PTAT current.

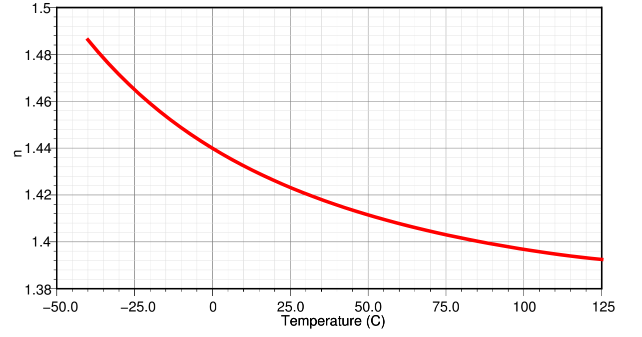

Fig. 4. Subthreshold slope (n) as a function of temperature

The multiplier is formed by transistors M1–M4, Mm1 and Mm2. Since the gate-source voltages of matched M1–M4 form a loop, from Eq. (1) it can be shown that the drain currents of these transistors satisfy

$$\frac{I_{D1}}{(\frac{W}{L})_1}\frac{I_M}{(\frac{W}{L})_3} = \frac{I_2}{(\frac{W}{L})_2}\frac{I_O}{(\frac{W}{L})_4} , \quad (6)$$

where I_O is the output current and I_M is the other current sent to the multiplier. For the moment, ignore the contribution to I_M by the Mp-Mq mirror. To allow operation of these transistors at similar current density (similar V_{GS}), I_2 is set to $2(I_{D2} - I_{D1})$ and

$$(W/L)_1 = (W/L)_3 = (W/L)_4 = 5(W/L)_2 .$$

Thus the resulting multiplier constant is 0.1, *i.e.*,

$$I_O = \frac{I_{D1}I_M}{10(I_{D2} - I_{D1})} . \quad (7)$$

Combining Eq. (5) and Eq. (7) we obtain

$$I_O = \frac{nI_M}{10I_{ref}R_b}V_T = \alpha V_T . \quad (8)$$

Thus, the output current is proportional to V_T provided the truncated Taylor expansion is accurate and α can be made constant with temperature. Fig. 4 shows the variation of n with temperature calculated using Eq.(3) from a simulation with $I_{ref} = 100$ nA, $R_b = 20$ kΩ, $W = 10$ μm and $L = 10$ μm. The corresponding value of $\partial I_O/\partial T$ (PTAT gain) numerically calculated from Eq. (3) is shown in Fig. 5. The gain is reduced for low temperatures due to the negative contribution in the slope of n. The biasing resistor (R_B) also varies with temperature but changes are much smaller, in the order of ±1% in the entire temperature range. The combined effect of the variations in n, R_b and the error due to the Taylor series truncation in the PTAT gain is shown in Fig. 6, with a constant $I_M = 120$ nA. Two curves are shown: the first is numerically obtained from Eq. (7) (ideal current substractor/multiplier) and the second is the actual circuit response (real current substractor/multiplier).

The compensation proposed here to linearize the gain is to make I_M to decrease with temperature. A small negative PTAT (NPTAT) component is added to I_M to achieve this (Transistors Mp and Mq in Fig 3). This is conceptually illustrated in Fig 7. Assume we set $I_M = I_{m0} - k_m(T - T_1)$, with $I_{m0} = 120$ nA and

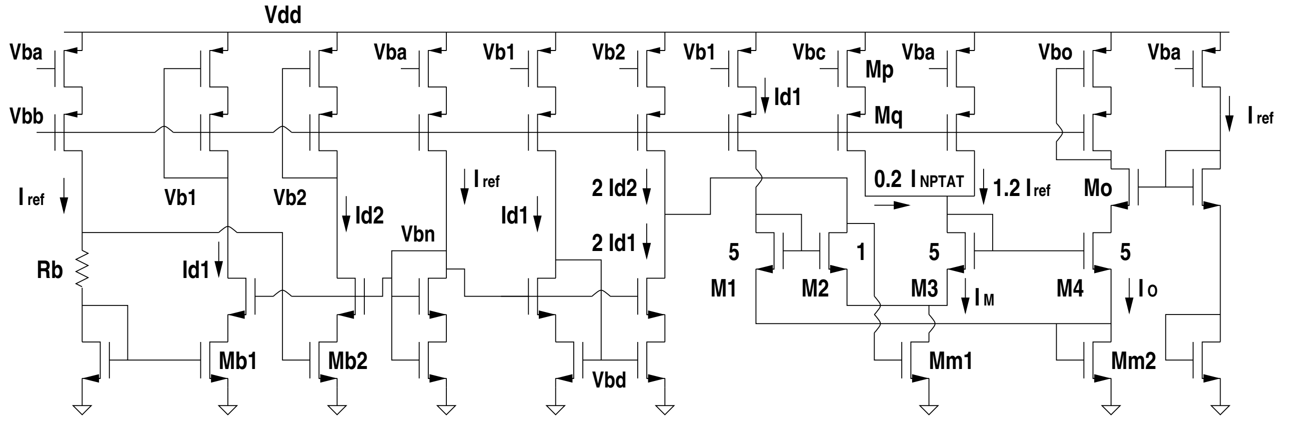

Fig. 3. Complete PTAT source schematic

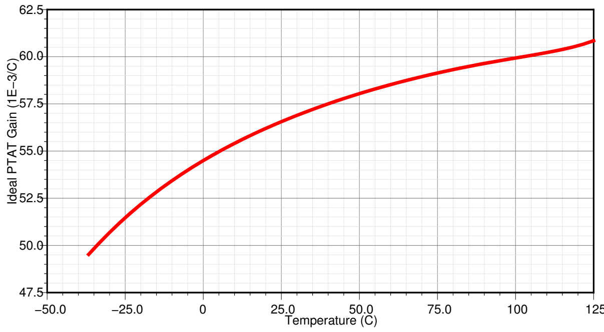

Fig. 5. PTAT gain as a function of temperature numerically calculated from Eq. (3)

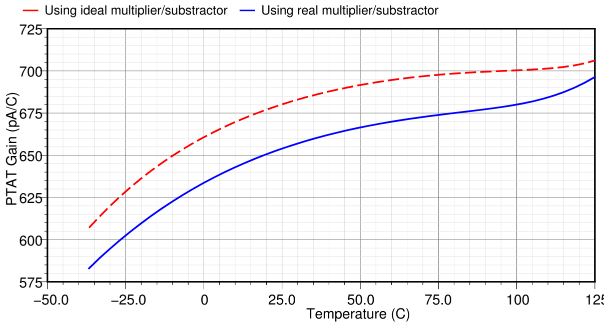

Fig. 6. PTAT gain as a function of temperature for a constant $I_M = 120$ nA

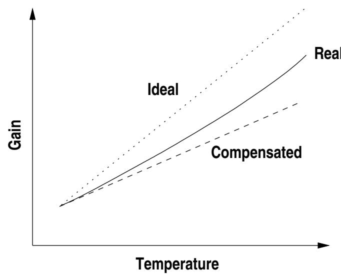

Fig. 7. Gain compensation concept

TABLE I
PARAMETERS FOR k_m DETERMINATION

T (K)	T (°C)	n	$\partial n/\partial T$ (1/K)
233	-40	1.49	-1.58×10^{-3}
398	125	1.39	-1.34×10^{-4}

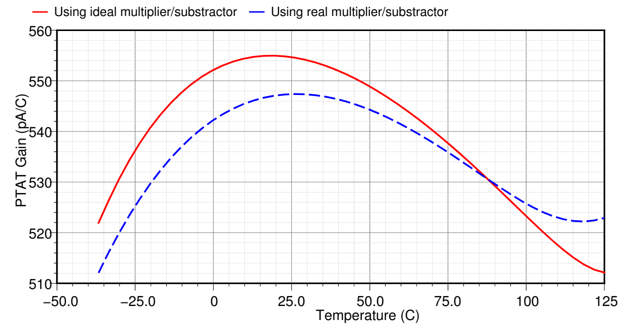

Fig. 8. PTAT output current as a function of temperature with $k_m = 59$ pA/°C

$T_1 = 233$ K (approximately -40 °C). We want to find a value of k_m that linearizes the gain. From Eq. (8), $\partial I_O/\partial T$ satisfies

$$\frac{10qI_{ref}R_b}{k}\frac{\partial I_O}{\partial T} = \left(\frac{\partial n}{\partial T}T + n\right)(I_{m0} - k_m(T - T_1)) - nk_mT\ . \quad (9)$$

The desired value of k_m is found by equating the right-hand sides of Eq. (9) at the two extreme temperatures of this design using the parameters shown in Table I. The resulting value of k_m is 59 pA/°C. The simulated PTAT gain with compensation set as calculated here is shown in Fig. 8. It can be observed that the PTAT gain variation is significantly lower. It was reduced from approximately 20.6 % in Fig. 6 to 6.8 % after compensation. As can be observed in Fig 7, after linearization the output current I_O has an IOAT component. In the current implementation this component is removed to produce a pure PTAT current (I_{PTAT}) using the circuit shown in Fig 9.

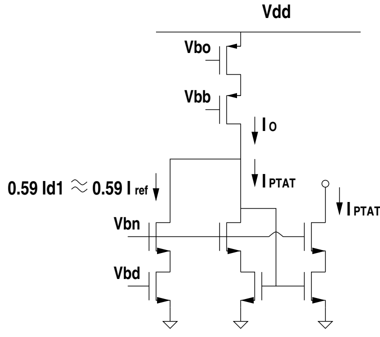

Fig. 9. PTAT current offset correction and mirroring circuit

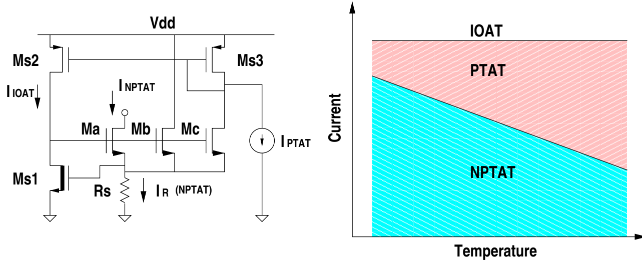

Fig. 10. Modified self-biasing V_{TH} reference circuit

B. IOAT and Negative PTAT Source

The reference current (I_{ref}) in Eq. (3) and I_M are generated using a self-biasing V_{TH} reference [3] modified to produce an IOAT current. A simplified schematic is shown in Fig. 10. Transistor M_{S1} is a 'native' (unimplanted) NMOS transistor with a slightly negative threshold voltage at room temperature. This results in a low voltage drop across R_S and thus it is possible to achieve small currents with reasonable resistor values. This transistor has a long channel and is operating in strong inversion with an IOAT drain current. The voltage across R_S and the I_R current are thus negatively proportional to temperature [3]. In this work $R_S = 80$ kΩ with a corresponding value of $I_R = 1.28$ μA at room temperature. This is the branch with the highest current in the design. Transistors M_a, M_b and M_c divide I_R as follows: M_a provides an NPTAT output current, M_c provides the NPTAT component that is mirrored by M_{S2}–M_{S3}, and the remaining current needed by R_S is provided by M_b. Transistor M_{S3} conducts a sum of a PTAT and an NPTAT currents which are adjusted to cancel each other as shown in Fig. 10. The PTAT gain in the final circuit is approximately 0.48 nA/C. I_R drops approximately 7.2 nA/C. The I_R fraction that is needed to produce I_{IOAT} is then 1/15. This current is thus

$$I_{IOAT} = 0.48 \times 300 + 1280/15 \approx 230 \text{ nA} = 2.3 I_{ref}$$

The complete schematic for the IOAT reference is shown in Fig. 11. As with the PTAT current generator, in this circuit the current mirrors have also been cascoded to improve PSRR. This source is self-biasing and requires a start-up circuit, not included in the figure.

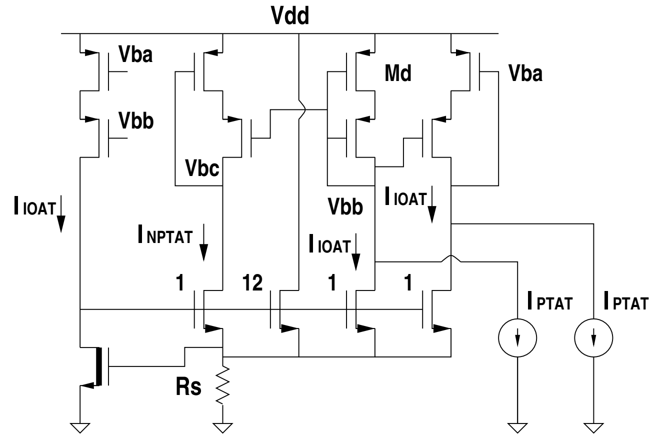

Fig. 11. Complete IOAT source schematic

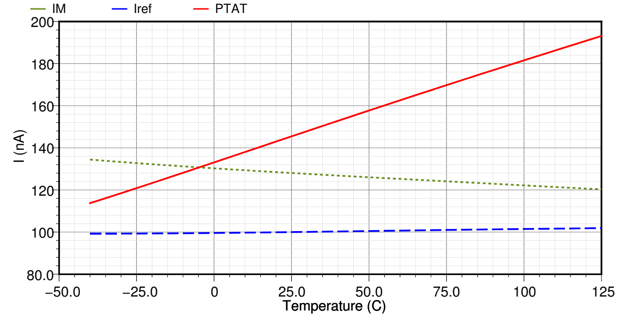

Fig. 12. PTAT output current, I_{ref} and I_M for nominal values

III. Simulation Results and Discussion

As mentioned before, all simulations reported here were performed using the TSMC 180 nm CMOS process parameters with the Spectre simulator. Unless otherwise specified, the supply voltage in all simulations (V_{DD}) is 1 V. The nominal PTAT output current (I_{PTAT}) as a function of temperature is shown in Fig. 12. In this figure I_{ref} and I_M are also plotted. The PTAT gain is shown in Fig. 13. This gain differs somewhat from the result in Fig. 8 because it includes the effects of self-biasing (*i.e.*, I_{ref} is not perfectly constant equal to 100 nA) and I_M has been tuned for optimum linearity under these conditions. Figure 14 shows how power supply rejection ratio

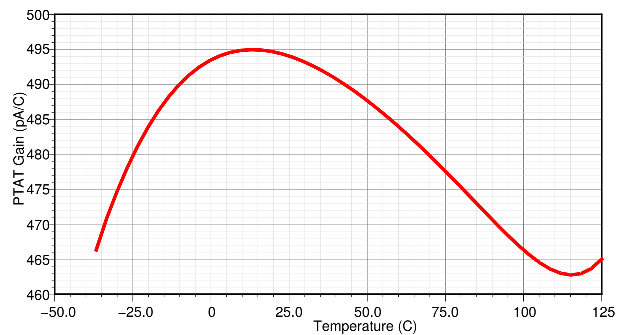

Fig. 13. PTAT output current as a function of temperature for nominal values

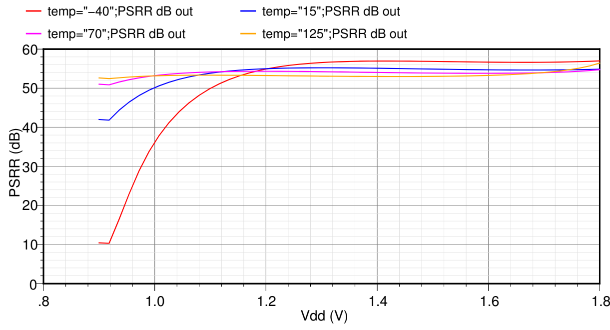

Fig. 14. PSRR of the PTAT current as a function of V_{DD} for different temperatures

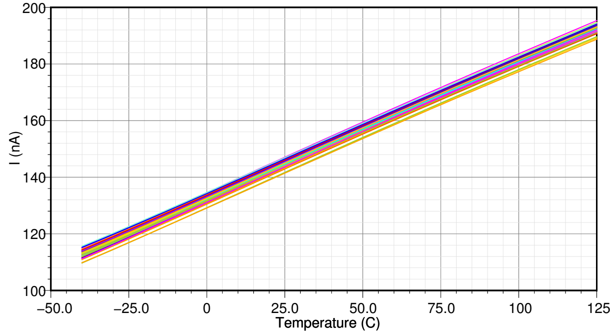

Fig. 15. Montecarlo analysis of I_{PTAT} not including resistor variations

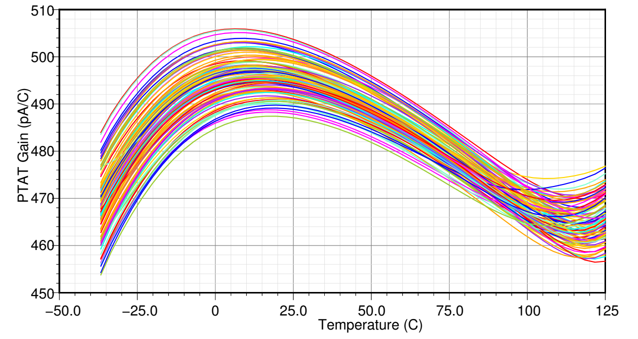

Fig. 16. Montecarlo analysis of the PTAT gain not including resistor variations

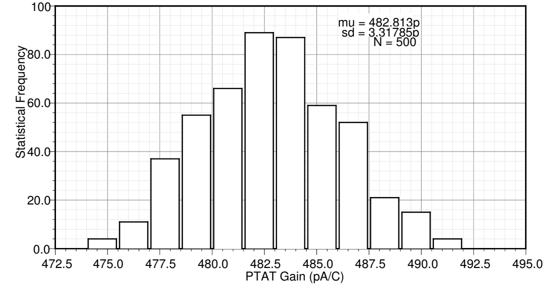

Fig. 17. PTAT gain histogram for 500 simulations not including resistor variations

and output current stabilize as supply voltage increases. The PSRR was calculated as follows:

$$\text{PSRR} = 20\log\left(\frac{\partial I_{PTAT}}{\partial V_{DD}}\frac{V_{DD}}{I_{PTAT}}\right)$$

The PSRR is greater than 50 dB for most operating conditions. The worst condition is at -40 °C due to the increased gate-source voltages required at this temperature. Sensitivity to process variations and PSRR are the main factors that prevent reducing currents or further shrinking the area of the design. Figures 15 and 16 show the result of a Montecarlo analysis with 100 simulations including process and mismatch variations in transistors only. It can be observed that the linearity in all cases remains similar and the variations in gain due to mismatch/process parameter are smaller than the nonlinearity. Fig. 17 shows the PTAT gain histogram for 500 simulations. The mean average gain is 482.3 pA/°C with a standard deviation of 3.3 pA/°C. The resistors in this design are implemented using a high-resistance P+ poly layer without silicide. The 6σ range for these resistors is approximately ±20 %. Figure 18 shows results of a Montecarlo analysis including resistor variations. It can be observed that linearity is not affected much but the spread is much greater. Fig. 19 shows the PTAT gain histogram including resistor variations for 500 simulations. The mean average gain does not change much at 487.5 pA/°C but the standard deviation is increased more than tenfold to 39.9 pA/°C. Variations in R_S produce variations in the reference current. However this is not the main cause of variation. It can be seen from Eq. (8) that if I_M/I_{ref} is kept constant the output current does not change. The observed variations in the PTAT current and gain are mainly due to variations in R_b.

Table II compares the main parameters of several temperature sensors found in the literature. The proposed circuit is quite competitive. The most significant advantage in this design is the combination of a highly linear output for a wide range of supply voltages, low power consumption and a relatively small area. The total gate plus resistor area in this design is 1026 μm^2. The PSRR is greater than 50 dB for V_{DD} greater than 1.13 V. This feature is especially important in DVS contexts where the sensor must exhibit consistent behaviour despite changes in the supply.

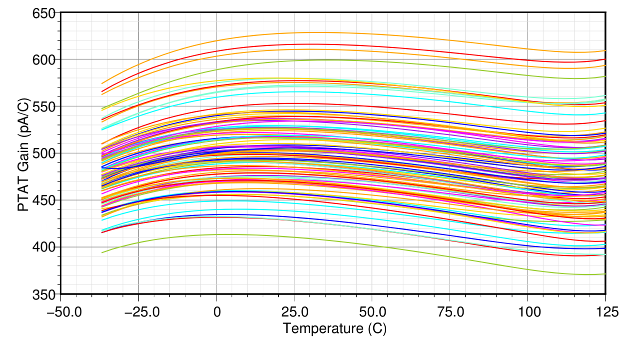

Fig. 18. Montecarlo analysis of the PTAT gain including resistor variations

TABLE II

COMPARISON OF MAIN PARAMETERS OF THE PROPOSED SENSOR AND OTHER PUBLISHED TEMPERATURE SENSORS

Reference	V_{DD}	Power	PSRR	T range	Sensitivity	Linearity	Area	Technology	Monte Carlo deviations
[1]	1.5V	$< 5.8\mu W$		$-20°C - 100°C$	$113pA/°C$, $21.4Hz/°C$	Good		350nm CMOS	
[2]				$10°C - 90°C$	$0.95 - 1.15$ $°C/bit$	Excellent		65nmCMOS	
[4]				$30°C - 150°C$	$\sim 1.8mV/°C$	Good		50nm CMOS predictive model	$\sim 10\%$
[5]		$28.53\mu W$		$-55°C - 170°C$	$264\mu V/°C$	Excellent	$1260\mu m^2$	130nm and 180nm CMOS	
[6]				$-23°C - 157°C$				500nm CMOS	
[7]		$> 16nW$		$25°C - 350°C$	$\sim 37\Omega/°C$	Acceptable	$> 1200\mu m^2$	Custom SOI	
[8]	3.3V	$< 50\mu W$	32.2dB	$0°C - 75°C$	$1.2V/°C$	Good	$1600\mu m^2$	180nm MOS	0.43% or 6.14%
[9]	$> 950mV$	$< 5\mu W$	$> 60dB$	$0°C - 50°C$	$220\mu V/°C$, $1.13nA/°C$	Good	$50000\mu m^2$	$1.2\mu m$ and 350nm CMOS	$<\sim 5\%$
[10]	1.3V	$80\mu W$	$> 100dB$	$-50°C - 130°C$				180nm CMOS	0.5%
[11]	$2.5V$ $(1.8V - 3.3V)$	$300\mu W$ $2.2mW$		$20°C - 60°C$			$< 10^6\mu m^2$	250nm CMOS	Calibrated
[12]	5V				$2.7V/°C$			$1.2\mu m$BiCMOS	
Proposed	1.0–1.8 V	$3.8\mu W$	$> 35dB$	$-40°C - 125°C$	$487pA/°C$	Excellent	$> 1000\mu m^2$	180nm CMOS	8%

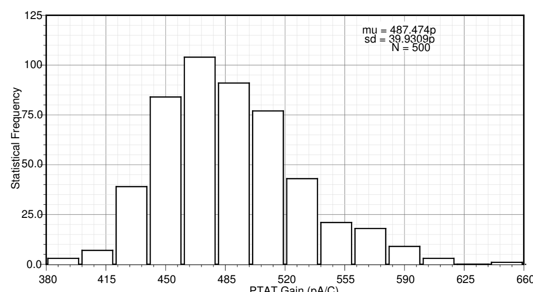

Fig. 19. PTAT gain histogram for 500 simulations including resistor variations

IV. CONCLUSIONS

A novel CMOS PTAT current source has been studied and designed. The design uses an original topology with improved linearity. The response is very linear in the valid range of the simulation parameters (−40°C–125°C) and it is likely to remain linear for an even greater range in practice. A good PSRR for supply voltages of 1 V or greater was achieved by using cascoded mirrors. Some weaknesses of this design are the variation in gain produced by variations in the resistor values and the use some non-standard process steps (unimplanted transistor). Further research will focus on replacing resistors with transistors as it has been done with other designs [5] and implementing the design using standard transistors only.

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