SHORT PAPER

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Low Power Temperature Compensated CMOS Current Reference

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***Abstract* — This paper describes a new circuit of a temperature-compensated CMOS current reference. The temperature dependency of the output current has been compensated by the addition of two currents which have exactly opposite temperature dependencies. Using a simple circuit, an appreciably low value of temperature drift of the output current has been obtained. The operation principle of the circuit has been described and the performance has been observed through computer simulations. The technology used is UMC 0.18µM with supply voltage of 1V. The current reference shows a temperature drift of 190ppm/^{0}C in the temperature range of -40^{0}C to +120^{0}C with a minimal power consumption of 80µW. This current reference can be used in some consumer systems like video & image processing, signal processing applications, RF circuits etc.**

I. INTRODUCTION

Present day high-performance analog, digital and power electronic systems require stable current references for proper operations. A reliable current reference should be independent of temperature, supply voltage and process variations. For this purpose, many designs to implement high-precision temperature-compensated current references have been proposed. At first the references were designed from BJTs but with the advent of CMOS technology, the scene has changed. It is a need to implement high performance current references using CMOS technology owing to their better performance over the BJT counterparts.
Power consumption is also an important aspect in the growing technology of portable devices. Low voltage and low power design of stable current references are some of the challenges faced while working in this area. This paper gives a new topology to implement a CMOS current reference. The design has been tested on UMC 180nm technology with a supply voltage of 1V.

II. PRINCIPLE OF CURRENT GENERATION

The variations of a current shown to the absolute temperature can be classified into two broad categories:

1. Proportional to absolute temperature (PTAT)
2. Inversely proportional to absolute temperature (ITAT)

The basic idea to have a first order temperature compensation is to add a PTAT current with an ITAT current. This way, the current which is obtained would show a much slower variation compared to the original PTAT or ITAT currents. [3]

The individual currents are generated by using a self-biased feedback loop. The circuit used in both the loops is the same but the two loops have been designed to give opposite temperature coefficients of current. After obtaining these PTAT and ITAT currents we add both these currents to obtain a fairly constant current with respect to temperature variations.
Fig.1 shows the idea of this first order temperature compensation.

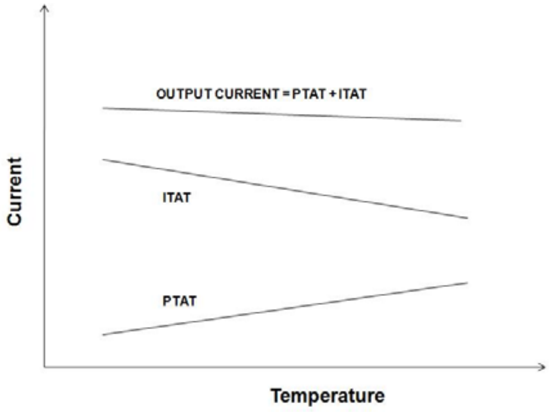

Fig.1 First order temperature compensation

As has been discussed the individual PTAT and ITAT currents have been generated using a feedback loop. Fig.2 shows this current generation circuit.
The circuit shown is made up of two cross-connected current mirrors: M1 & M2 and the Widlar current mirror M3-M4-R. In particular, the current mirror fixes the ratio between the currents flowing in the two branches, while the Widlar current mirror defines the value of the reference current. [4]

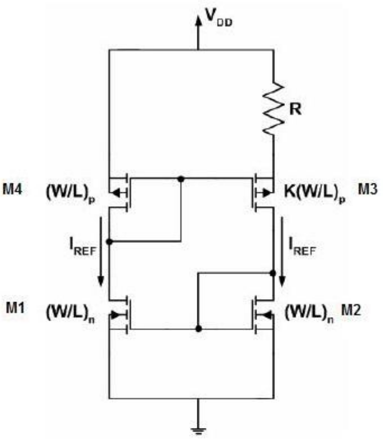

Fig.2 Basic Current Reference

The current generated by this circuit can be found out by mathematical analysis. Using the primitive MOS model the current expression is given as follows [4]:

$$Iref = \frac{2}{\mu p\ Cox\ \left(\frac{W}{L}\right)P} * \frac{1}{R^2} * \left(1 - \frac{1}{\sqrt{K}}\right)^2$$

III. SYSTEM ARCHITECTURE

Fig. 3 shows the complete schematic of the current reference. The transistors M0, M1, M2, M3 and R1 form one current generation loop while transistors M4, M5, M6, M7 and R2 form another current generation loop. The current generated by the first loop is a PTAT current while the other one is an ITAT current. The combined current flows through the transistor M10 which is a diode connected device.

The resistor values and their temperature coefficients can be designed to get an almost equal and opposite slope of the two currents with temperature. One of the resistors has a positive temp. coefficient (low resistive poly resistor) while the other has negative temp. coefficient (high resistive poly resistor). As a result the current in M10 is nearly constant with temperature.

The following table shows the design parameters used.

VDD = 1V, R0 = 7kΩ, R1 = 20kΩ

TRANSISTOR	WIDTH (µM)	LENGTH (µM)
M0 – NMOS	3 µ	1 µ
M1 – NMOS	3 µ	1 µ
M2 – PMOS	10 µ	1 µ
M3 – PMOS	20 µ	1 µ
M4 – NMOS	3 µ	1 µ
M5 – NMOS	3 µ	1 µ
M6 – PMOS	10 µ	1 µ
M7 – PMOS	20 µ	1 µ
M8 – NMOS	18 µ	1 µ
M9 – NMOS	18 µ	1 µ
M10 – PMOS	24 µ	1 µ

Table 1: Sizes of transistors used in the schematic

Technology used: UMC 0.18µM
MOS models: N_18_MM and P_18_MM

IV. EXPERIMENTAL RESULTS

Simulations done to calculate the variation of the output current with temperature showed that the output current is fairly constant with temperature at all corners.

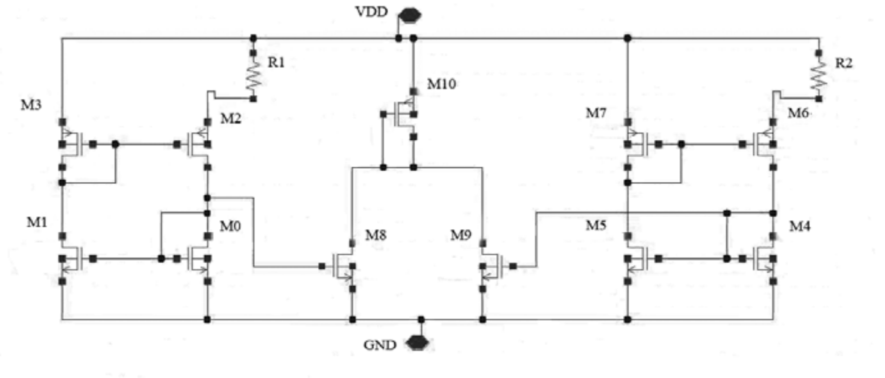

Fig.3 Schematic of the designed current reference

The output current obtained shows a variation of 190ppm /^{0}C in the temperature range of -40^{0}C to +120^{0}Cat TT corner. The circuit was also tested at all the other corners to obtain the dependencies of mobility and supply voltage variations on the output current. The values of the current and its variation obtained with temperature are given in the following table.

Table 2: Current Reference Performance

PROCESS CORNER	I (µA) at -40^{0}C	I (µA) at +30^{0}C	I (µA) at +120^{0}C	VARIATION OF CURRENT WITH TEMP. (ppm/^{0}C)
TT	58.57	58.08	58.39	190
FF	61.29	60.06	59.9	293
SS	48.71	50.21	52.2	427

Another important factor is the variation of output current due to any fluctuations in the supply voltage Vdd. To analyze this effect, the voltage gain from Vdd to the gate of M10 was observed at different temperatures. For the output current to be stable against these fluctuations, this voltage gain should be close to unity. In practice it comes out to be 802 mV/V (-1.8dB) at +30^{0}C and TT corner. This shows that the output current is appreciably stable to Vdd fluctuations.

Fig.4 shows the variation of the output current with temperature at TT corner.

V. CONCLUSION

In this paper, a new first-order temperature compensated CMOS current reference has been presented. With the help of the compact circuit, the temperature drift of the reference current obtained is approx. 190ppm/^{0}C which is an appreciable value. Even in the presence of process corners variations, the worst case temperature drift is about 427ppm/^{0}C. The circuit has a minimal power consumption of 80µW. The output current also shows a good rejection to the fluctuations in the supply voltage. The circuit has been designed using UMC 0.18µM technology and a supply voltage of 1V and the performance has been verified through computer simulations.

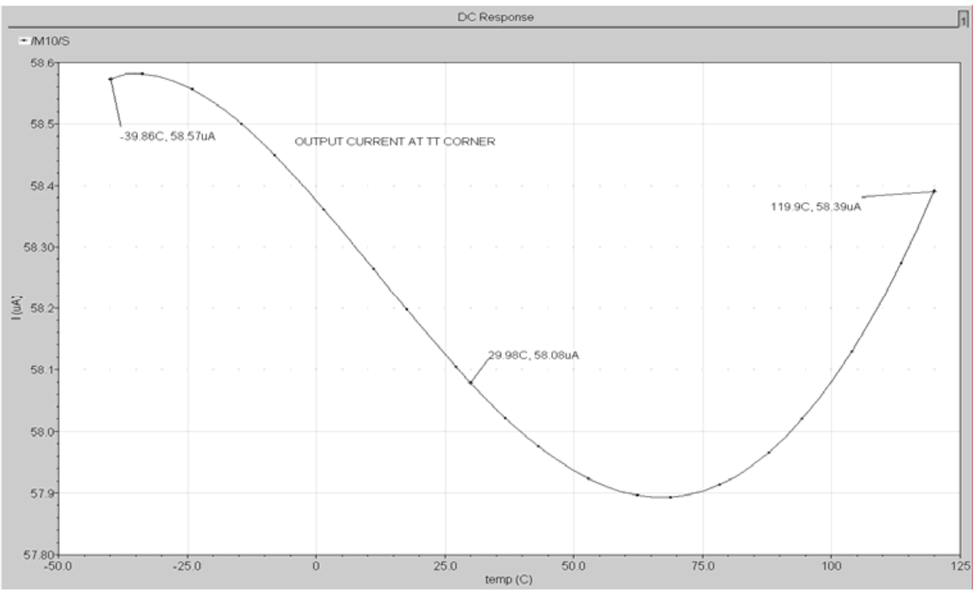

Fig.4 Variation of output current with temperature at TT corner

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