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Title

TSMC 0.18 UM CMOS MIXED SIGNAL MS GENERAL PURPOSE 1P6M SALICIDE ALCU_FSG 1.8&5V DESIGN RULE

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Contents : 97
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TSMC 0.18 UM CMOS MIXED SIGNAL MS GENERAL PURPOSE 1P6M SALICIDE ALCU_FSG 1.8&5V DESIGN RULE

Table of Contents:

1 Introduction

1.1 Overview

This document provides design rules and reference information for the design and layout of integrated circuits using TSMC 0.18 um CMOS Mixed Signal (MIM) 1P6M (single poly, 6 metal layers), 1.8V/5V, salicide, Al technology.

- For Logic part, please refer to CL018G 1.8/5V design rules in T-018-LO-DR-001.
- Logic 1.8V NTN and 1.8V PNP BJT are the same as CL018G 1.8/5V design rules in T-018-LO-DR-001.
- Mixed-signal DNW, HRI, 1.8V medium, UTM, 1.0fF MIM are the same as CM018 1.8/3.3V design rules in T-018-LO-DR-001.

The design rules (or layout rules) are defined as the dimension on wafer. The difference in feature size between the mask pattern and the wafer pattern are adjusted by CAD (Computer-Aided Design) bias.

1.2 Reference Documentation

This manual provides design rules specifically related to mixed signal design. Please always refer to the most updated version of the related documents.

Content	Reference Documentation	Document Number
Logic design rule	CL018G 1.8/5V design rule of "TSMC 0.18UM CMOS LOGIC/MS/RF AND 0.16UM CMOS LOGIC/MS DESIGN RULE (CL018G/LV/LP, CM018, CR018, CL016G, CM016)"	T-018-LO-DR-001
Wire bond and flip chip related rules	TSMC WIRE BOND, FLIP CHIP AND INTERCONNECTION DESIGN RULE	T-000-CL-DR-002
GDS layer usage	TSMC 0.18UM GDS LAYER USAGE DESCRIPTION FILE	T-018-LO-LE-003

1.3 USER GUIDE

1.3.1 Mixed Signal Design Recommendations

- It is recommended to use TSMC PDK cells to design your mixed signal circuit. These PDK cells have been well characterized with silicon. Please refer to the document (T-018-MM-SP-001-K1) for layout guideline.
- MIM only provide 1.0fF. 2.0fF MIM is not provided.
- Un-salicided poly/OD resistor and HRI poly resistor guidelines:
  - Dummy layers (DMN2V, DMP2V or RLPPDMY) are required for the tapeout to perform logic operation during mask making, and perform DRC on the poly resistor and HRI poly resistor (please refer to T-018-LO-MB-001 and T-018-MM-MB-001). Please refer to section 4.5.5 “HRI Poly Resistor Rule” and T-018-LO-DR-001 4.5.7 “Poly Resistor and OD Resistor Guidelines” .
  - Un-salicided poly resistor resistance is about 300 ohm/sq.
  - HRI poly resistor resistance is about 1000 ohm/sq.

1.4 Guidelines for CM016/CM0152 Technologies

- CM018 1.8/5V does NOT offer shrinkage technologies for CM016/CM0152.

1.5 TERMINOLOGY

The following definitions are used in the physical design rules:

N+ OD	:	OD covered with NP.
P+ OD	:	OD covered with PP.

2 Technology Overview

This chapter provides information about the following:

2.1 Semiconductor process features for Mixed Signal devices

The 0.18um MS process (CM018) is based on 0.18um logic 1P6M, 1.8V/5V, salicide process. The major mixed signal process features of the additional offering devices/process are:

1. Deep N-Well (DNW) is only applied to core device for isolating the noise from P-substrate.
2. Both 1.8 and 5V Medium Vt NMOS and medium Vt PMOS are offered in the 1.8/5V Mixed signal application. Four extra implant masks and the associated implant process are offered. Mask 118 and 117 are for 1.8V medium Vt N/PMOS. Mask 102 and 103 are for 5V medium Vt N/PMOS.
3. The P-type HRI (high resistance) poly resistor is offered.
4. The MIM capacitor is fabricated with two metals, which are separated by an insulator. TSMC provides 1fF/um^2 MIM capacitance. A CTM is used for capacitor top metal, where the bottom metal is the M_{top-1}. For example, M5 is used as the bottom metal for the 1P6M process. Figure 2.1.1 provides an example of an MIM capacitor cross section.
5. The ultra thick metal layer (UTM, 20KÅ or 40 KÅ thickness) is an optional layer for the inductor application. UTM is not allowed used simultaneously with Mn (8KÅ thickness) in the same chip.

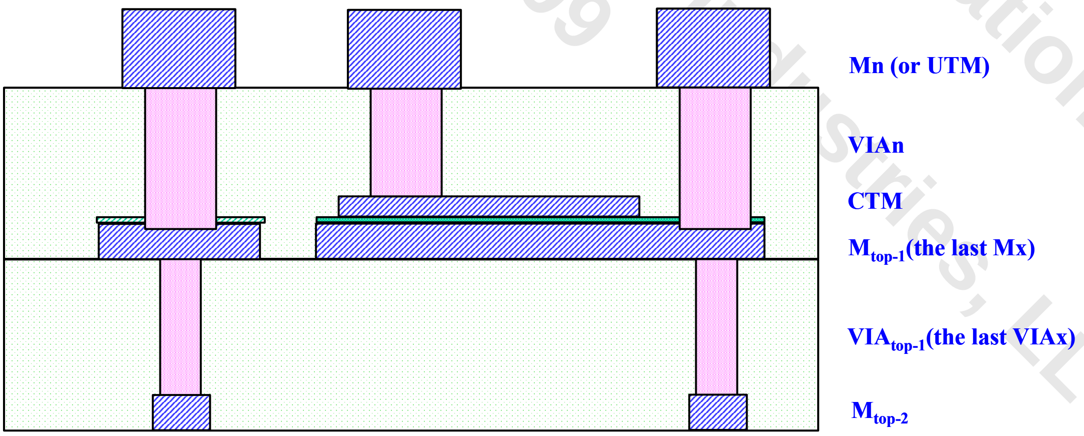


Figure 2.1.1 MIM capacitor cross section

2.2 Metallization Options

- Table 2.2.3 provides the metallization options for the 8KÅ top metal (Mn) with MIM.
- Table 2.2.4 and Table 2.2.5 provides the metallization options for the ultra thick top metal (UTM, 20KÅ or 40KÅ thickness) without and with MIM, respectively.
- “CTM” is the optional layer for capacitor top metal. And it is only allowed being placed at: (1) between M_{top-1} and Mn; or (2) between M_{top-1} and UTM.

Table 2.2.1 Naming for Different Metal Thicknesses

Metal type	Code
M1 (4KA thickness)	M1
Inter-layer Metal (4KA thickness)	Mx
Top Metal (8KA thickness)	Mn
Ultra thick Top Metal (20KÅ or 40KÅ thickness)	UTM *

* Please refer to T-018-LO-DR-001 Section 4.6.7 for the UTM deign rules.

Table 2.2.2 Naming for Different Via Types

Via type	Code	W/S(um)
Inter-layer Via	Vx (VIAx)	0.26/0.26
Top Via	Vn (VIAn)	0.36/0.35

Table 2.2.3 8KÅ Top Metal with MIM

Metal /Via	Total Number of Metal Layers			
	3	**4**	**5**	**6**
M1	M1	M1	M1	M1
VIA1	Vx	Vx	Vx	Vx
M2	Mx + CTM	Mx	Mx	Mx
VIA2	**Vn**	Vx	Vx	Vx
M3	**Mn**	Mx + CTM	Mx	Mx
VIA3		**Vn**	Vx	Vx
M4		**Mn**	Mx + CTM	Mx
VIA4			**Vn**	Vx
M5			**Mn**	Mx + CTM
VIA5				**Vn**
M6				**Mn**

Note:

1. The mark in the above table stands for MIM layer.

Table 2.2.4 Ultra Thick Top Metal (20KÅ or 40KÅ thickness) without MIM

Metal /Via	Total Number of Metal Layers			
	3	**4**	**5**	**6**
M1	M1	M1	M1	M1
VIA1	Vx	Vx	Vx	Vx
M2	Mx	Mx	Mx	Mx
VIA2	**Vn**	Vx	Vx	Vx
M3	**UTM**	Mx	Mx	Mx
VIA3		**Vn**	Vx	Vx
M4		**UTM**	Mx	Mx
VIA4			**Vn**	Vx
M5			**UTM**	Mx
VIA5				**Vn**
M6				**UTM**

Table 2.2.5 Ultra Thick Top Metal (20KÅ or 40KÅ thickness) with MIM

Metal /Via	**Total Number of Metal Layers**			
	3	**4**	**5**	**6**
M1	M1	M1	M1	M1
VIA1	Vx	Vx	Vx	Vx
M2	Mx + CTM	Mx	Mx	Mx
VIA2	**Vn**	Vx	Vx	Vx
M3	**UTM**	Mx + CTM	Mx	Mx
VIA3		**Vn**	Vx	Vx
M4		**UTM**	Mx + CTM	Mx
VIA4			**Vn**	Vx
M5			**UTM**	Mx + CTM
VIA5				**Vn**
M6				**UTM**

Note:

1. The mark ▬▬▬ in the above table stands for MIM layer.

3 General Layout Information

This chapter provides the following general layout information:

3.1 Mask Information, Key Process Sequence, and CAD layers Information

3.2 Special layer summary

3.3 Device truth tables

3.4 Device List & Spec

3.1 Mask Information, Key Process Sequence, and CAD Layers Information

Key Process Sequence * = Optional Mask	Mask Name	Mask ID	Digitized Area (Dark or Clear)	CAD Layer	Reference Layer in Logical Operation	Description
1*	DNW	119	C	82	-	Deep N-Well.
2	OD	120	D	3,11,12	-	Thin oxide for device, and interconnection.
3	ODR(1)	121	C	Derived	OD	Trench.
4	PW(1)	191	D	Derived	OD2,NW, NT_N	P-Well.
5*	1.8V VTM_N(1)	118	C	24	OD2,NW, NT_N	1.8V NMOS Vt implantation.
6	PW5V	193	C	Derived	OD2,NW, NT_N	5V P-Well
7*	5V VTM_N(1)	102	C	24	OD2,NW, NT_N	5V NMOS Vt implantation.
8	NW	192	C	2	OD2	N-Well.
9*	1.8 V VTM_P(1)	117	C	23	OD2, NW,	1.8V PMOS Vt implantation.
10	NW5V	194	C	2	OD2	5V N-Well
11*	5V VTM_P(1)	103	C	23	OD2, NW,	5V PMOS Vt implantation.
12	OD2	132	D	4	-	3.3V thick oxide.
13	PO	130	D	13	-	Poly-Si.
14	N2V(1)	114	C	Derived	NW, OD2, NP, DMN2V, VARDMY	1.8V NLDD implantation.
15	P2V(1)	113	C	Derived	NW, OD2, PP, DMP2V, VARDMY, RLPPDMY	1.8V PLDD implantation.
16	P3V(1)	115	C	Derived	NW, OD2, PP, DMN2V, DMP2V, VARDMY, RLPPDMY	5V PLDD implantation.
17	N3V(1)	116	C	Derived	NW, OD2, NP, DMN2V, DMP2V, VARDMY	5V NLDD implantation.
18	NP(1)	198	C	8	OD, NP, PP	N+ S/D implantation.
19	PP(1)	197	C	7	OD, NP, PP, RLPPDMY	P+ S/D implantation.
20*	HRI	133	C	48	-	High Resistor Implant
21*	ESD(1)	110	C	30	-	ESD implantation.
22	RPO(1)	155	D	34	NW, OD, OD2, PO, NP, RPO, CO	Resist protection oxide.
23	CO	156	C	15	-	Contact hole between M1 and (OD or PO).

Key Process Sequence * = Optional Mask	Mask Name	Mask ID	Digitized Area (Dark or Clear)	CAD Layer	Reference Layer in Logical Operation	Description
24	M1	160	D	16	-	1st metal for interconnection.
25	VIA1	178	C	17	-	Via1 hole between M2 and M1.
26	M2	180	D	18	-	2nd metal for interconnection.
27	VIA2	179	C	27	-	Via2 hole between M3 and M2.
28	M3	181	D	28	-	3rd metal for interconnection.
29	VIA3	173	C	29	-	Via3 hole between M4 and M3.
30	M4	184	D	31	-	4th metal for interconnection.
31	VIA4	174	C	32	-	Via4 hole between M5 and M4.
32*	CTM	182	D	67	-	Capacitor top metal
33	M5	185	D	33	-	5th metal for interconnection.
34	VIA5	175	C	39	-	Via5 hole between M6 and M5.
BEOL option1 (Top metal, M6, 8KA thickness)						
35	M6	186	D	38	-	6th metal for interconnection.
36*	FW	108	C	235	-	Fuse window
37	CB	107	C	19	-	Passivation open for bond pad.
38*	PM	009	D	89	CB, FW	Polyimide opening window
BEOL option2 (Ultra Thick top metal, UTM, 20KA/40KA thickness)						
35	UTM	186	D	38	-	6th metal for interconnection.
36*	FW	108	C	235	-	Fuse window
37	CB	107	C	19	-	Passivation open for bond pad.
38*	PM	009	D	89	CB, FW	Polyimide opening window

Note:
(1) Please refer to document “T-018-CM-MB-018” for the detailed logical operation.
(2) More bond pad related offeringss and rules are available in the bond pad design rule document. (Doc. No.: T-000-CL-DR-002)

3.2 Special Layer Summary

Table 3.2.1 lists special layers for CL018 DRC recognition or Tapeout required purpose and Table 3.2.2 lists special layers for CM018 DRC recognition or MT from purpose. If you do not follow the TSMC default CAD layer number, make sure that you change the layer mapping in the relative deck, like DRC/LVS and so on. Some CAD layer designators include a GDS datatype according to the GDS layer; datatype format.

The column "Tapeout required layer" indicates that this layer must be noted on the mask tapeout form, to provide information for mask making.

Table 3.2.1 Special Layer Summary for CL018

Special Layer Name	TSMC Default CAD Layer	Description	Associated With	DRC	Tapeout required layer
SDI	58;0	Dummy layer to cover ESD devices.	For DRC only (ESD rule check).	V	
DMN2V	184	Dummy layer for N+ poly resistor (non-silicided N+ poly resistor)	For DRC and logical operation	V	V
DMP2V	149	Dummy layer for P+ poly resistor (non-silicided P+ poly resistor)	For DRC and logical operation	V	V
RWDMY	52	Dummy layer for NW resistor	For DRC only (ESD rule check).	V	
ESD1DMY	136	Dummy layer to cover IO ESD region.	For DRC only (ESD rule check).	V	
ESD2DMY	137	Dummy layer to cover IO ESD region.	For DRC only (ESD rule check).	V	
DIODMY	56	Dummy layer to cover diode devices.	For DRC	V	
BJTDMY	49	Dummy layer to cover BJT devices.	For DRC	V	
LOGO	178	LOGO, dummy layer for product label and logo.	LOGO rule	V	
LUPWDMY	255;1	DRC dummy layer to waive the latch up rule if the silicon is verified for latch up issue.	For DRC only (LU rule check).	V	

Table 3.2.2 Special Layer Summary for CM018

Special Layer Name	TSMC Default CAD Layer	Description	Associated With	DRC	Tapeout required layer
VTM_P	23	VTM_P blocking implant	VTM_P rule	V	V
VTM_N	24	VTM_N blocking implant	VTM_N rule	V	V
CTMDMY	131	Dummy layer for MiM capacitor	CTM rule	V	
CTMDMY (drawing2)	131;10	Dummy layer for MiM capacitance with 1.0fF capacitance per unit area. (For LVS purpose)	CTM rule		
CTMDMY (drawing1)	131;21	Dummy layer for three terminals MiM capacitor. (For LVS purpose)	CTM rule		
RLPPDMY	134	Dummy layer for HRI poly resistor (non-silicided P- poly resistor)	HRI rule, Poly resistor rule	V	V
VARDMY	138	Dummy layer for both MOS and junction type varactor		V	V
INDDMY	139	Dummy layer for UTM in inductor application	UTM rule	V	

- Dummy layer (VARDMY) is needed for logical operation and DRC when varactor devices are implemented in circuit.

3.3 Device Truth Tables

This section contains the device truth tables for:

- Table 3.3.1 CL018 Logic General Purpose (G) 1.8V/5V technology
- Table 3.3.2 CM018 mixed signal 1.8/5V technology
- Table 3.3.3 Inductor

The following provides a legend for the following five device truth tables.

0 Does not cover the structures
1 Covers or matches the structures
***** Don't care

3.3.1 CL018G 1.8V/5V

Table 3.3.1 CL018 Logic General Purpose (G) 1.8V/5V technology

Device	SPICE name	Design Levels								Special Layer					
		NW	NT_N	OD	OD2	PO	NP	PP	RPO	DMN2V	DMP2V	RWDMY	RPDMY	DIODMY	BJTDMY
NMOS (1.8V)	nch	0	0	1	0	1	1	0	0	0	0	0	0	0	0
PMOS (1.8V)	pch	1	0	1	0	1	0	1	0	0	0	0	0	0	0
NMOS (5V)	nch_5	0	0	1	1	1	1	0	0	0	0	0	0	0	0
PMOS (5V)	pch_5	1	0	1	1	1	0	1	0	0	0	0	0	0	0
1.8V P+/NW/PSUB vertical PNP bipolar	pnp2 (Emitter area = 2×2 μm^2)	1	0	1	0	0	1#	1	0	0	0	0	0	0	1
	pnp5 (Emitter area = 5×5 μm^2)	1	0	1	0	0	1#	1	0	0	0	0	0	0	1
	pnp10 (Emitter area = 10×10 μm^2)	1	0	1	0	0	1#	1	0	0	0	0	0	0	1
1.8V P+/Nwell Junction Diode	PDIO	1	0	1	0	0	1#	1	0	0	0	0	0	1	0
1.8V N+/Pwell Junction Diode	NDIO	0	0	1	0	0	1	1#	0	0	0	0	0	1	0
1.8V NW/Psub Junction Diode	NWDIO	1	0	1	0	0	1#	1#	0	0	0	0	0	1	0
5V P+/Nwell Junction Diode	PDIO_5	1	0	1	1	0	1#	1	0	0	0	0	0	1	0
5V N+/Pwell Junction Diode	NDIO_5	0	0	1	1	0	1	1#	0	0	0	0	0	1	0
5V NW/Psub Junction Diode	NWDIO_5	1	0	1	1	0	1#	1#	0	0	0	0	0	1	0
N+ OD w/i Silicide Resistor (6.82 Ohm/sq)	rnod	0	0	1	0	0	1	0	0	0	0	0	1	0	0
N+ OD w/i Silicide Resistor (6.82 Ohm/sq)	rnodw	0	0	1	0	0	1	0	0	0	0	0	1	0	0
P+ OD w/i Silicide Resistor (7.76 Ohm/sq)	rpod	0	0	1	0	0	0	1	0	0	0	0	1	0	0
P+ OD w/i Silicide Resistor (7.76 Ohm/sq)	rpodw	0	0	1	0	0	0	1	0	0	0	0	1	0	0
N+ OD w/o Silicide Resistor (59 Ohm/sq)	rnodrpo	0	0	1	0	0	1	0	1	1	0	0	1	0	0
P+ OD w/o Silicide Resistor (133 Ohm/sq)	rpodrpo	0	0	1	0	0	0	1	1	0	1	0	1	0	0
N-well. Under OD Resistor (440 Ohm/sq)	rnwod	1	0	1	0	0	1	0	1	0	0	1	0	0	0
N-well. Under STI Resistor (927 Ohm/sq)	rnwsti	1	0	1#	0	0	1	0	0	0	0	1	0	0	0
N+ Poly w/i Silicide Resistor (7.89 Ohm/sq)	rnpo1	0	0	0	0	1	1	0	0	0	0	0	1	0	0
N+ Poly w/i Silicide Resistor (7.89 Ohm/sq)	rnpo1w	0	0	0	0	1	1	0	0	0	0	0	1	0	0
P+ Poly w/i Silicide Resistor (7.9 Ohm/sq)	rppo1	0	0	0	0	1	0	1	0	0	0	0	1	0	0
P+ Poly w/i Silicide Resistor (7.9 Ohm/sq)	rppo1w	0	0	0	0	1	0	1	0	0	0	0	1	0	0
N+ Poly w/o Silicide Resistor (311 Ohm/sq)	rnpo1rpo	0	0	0	0	1	1	0	1	1	0	0	1	0	0
P+ Poly w/o Silicide Resistor (311 Ohm/sq)	rppo1rpo	0	0	0	0	1	0	1	1	0	1	0	1	0	0

For pick-up

Note: The resistor value listed in table is just Rpure value. Please get more detail information in the SPICE document.

3.3.2 CM018 1.8V/5V

Table 3.3.2 CM018 mixed signal 1.8/5V technology

Device	SPICE name	Design Levels													Special Layer						
		DNW	OD	NWELL	NT_N	OD2	VTM_N	VTM_P	POLY	N+	P+	HRI	RPO	CTM	RLPPDMY	CTMDMY	CTMDMY(131;10)	CTMDMY(131;21)	VARDMY	BJTDMY	DIODMY
1.8V Medium V_t NMOS	Mench	0	1	0	0	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0
1.8V Medium V_t PMOS	Mepch	0	1	1	0	0	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0
5V Medium V_t NMOS	mench5	0	1	0	0	1	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0
5V Medium V_t PMOS	mepch5	0	1	1	0	1	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0
1.8V Native NMOS	nanch	0	1	1	1	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0
5V Native NMOS	nanch5	0	1	0	1	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0
1.8V N+/PW/DNW vertical NPN bipolar	NPN2 (Emitter area = 2×2 μm^2)	1	1	1	0	0	0	0	0	1	1#	0	0	0	0	0	0	0	0	1	0
	NPN5 (Emitter area = 5×5 μm^2)	1	1	1	0	0	0	0	0	1	1#	0	0	0	0	0	0	0	0	1	0
	NPN10 (Emitter area = 10×10 μm^2)	1	1	1	0	0	0	0	0	1	1#	0	0	0	0	0	0	0	0	1	0
5V N+/PW/DNW vertical NPN bipolar	NPN2 (Emitter area = 2×2 μm^2)	1	1	1	0	1	0	0	0	1	1#	0	0	0	0	0	0	0	0	1	0
	NPN5 (Emitter area = 5×5 μm^2)	1	1	1	0	1	0	0	0	1	1#	0	0	0	0	0	0	0	0	1	0
	NPN10 (Emitter area = 10×10 μm^2)	1	1	1	0	1	0	0	0	1	1#	0	0	0	0	0	0	0	0	1	0
5V P+/NW/PSUB vertical PNP bipolar	PNP2 (Emitter area = 2×2 μm^2)	0	1	1	0	1	0	0	0	1#	1	0	0	0	0	0	0	0	0	1	0
	PNP5 (Emitter area = 5×5 μm^2)	0	1	1	0	1	0	0	0	1#	1	0	0	0	0	0	0	0	0	1	0
	PNP10 (Emitter area = 10×10 μm^2)	0	1	1	0	1	0	0	0	1#	1	0	0	0	0	0	0	0	0	1	0
1.8V Varactor (NMOS capacitor)	nmoscap	0	1	1	0	0	0	0	1	1	0	0	0	0	0	0	0	0	1	0	0
5V Varactor (NMOS capacitor)	nmoscap_5	0	1	1	0	1	0	0	1	1	0	0	0	0	0	0	0	0	1	0	0
1.8V Medium VT P+/Nwell Junction Diode	PDIO_M	0	1	1	0	0	0	1	0	1#	1	0	0	0	0	0	0	0	0	0	1
1.8V Medium VT N+/Pwell Junction Diode	NDIO_M	0	1	0	0	0	1	0	0	1	1#	0	0	0	0	0	0	0	0	0	1
DNW/Psub Junction Diode	DNWPSUB	1	1	1	0	0	0	0	0	1#	1#	0	0	0	0	0	0	0	0	0	1
1.8V PW/DNW Junction Diode	PWDNW	1	1	1	0	0	0	0	0	1#	1	0	0	0	0	0	0	0	0	0	1
5V PW/DNW Junction Diode	PWDNW_5	1	1	1	0	1	0	0	0	1#	1	0	0	0	0	0	0	0	0	0	1
HRI P-Poly w/o silicide W≥1um(1075 Ohm/sq)	rppolyhri	0	0	0	0	0	0	0	1	0	1#	1	1	0	1	0	0	0	0	0	0
CM018 (GP2) Base Band mimcap																					
MIM capacitor (1fF/um^2)	mimcap_1p0_sin	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0	0	0	0
MIM capacitor (1fF/um^2)	mimcap_1p0_sin_3t	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	0	0	0

For pick-up

Note: The resistor value listed in table is just Rpure value. Please get more detail information in the SPICE document.

Table 3.3.3 Inductor

Device	SPICE name	Design Levels																				Special Layer								
		NW	NT_N	OD	OD2	PO	NP	PP	RPO	CO	M1	Via 1	M2	Via 2	M3	Via 3	M4	Via 4	M5	Via 5	M6	DMN2V	DMP2V	RWDMY	RPDMY	DIODMY	BJTDMY	ESD3DMY	RFDUMMY	INDDMY
Inductor	Subckt spiral_s2_std	0	1	1	0	0	0	1	0	1	1	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	1	1
	Subckt spiral_s3_std	0	1	1	0	0	0	1	0	1	1	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	1	1
	Subckt spiral_s2_sym	0	1	1	0	0	0	1	0	1	1	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	1	1
	Subckt spiral_s3_sym	0	1	1	0	0	0	1	0	1	1	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	1	1
	Subckt spiral_s2_sym_ct	0	1	1	0	0	0	1	0	1	1	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0	1	1
	Subckt spiral_s3_sym_ct	0	1	1	0	0	0	1	0	1	1	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0	1	1
	Subckt spiral_std_40k	0	1	1	0	0	0	1	0	1	1	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	1	1
	Subckt spiral_sym_40k	0	1	1	0	0	0	1	0	1	1	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	1	1
	Subckt spiral_sym_ct_40k	0	1	1	0	0	0	1	0	1	1	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0	1	1

3.4 Device List & Spec

This section lists all available devices and the related specs. The numbers in the table specify the range of allowed typical operation voltage.

3.4.1 CL018G 1.8V/5V

Table 3.4.1 CL018G 1.8/5V Device Feature

	Device	SPICE Name	|Vgs|	|Vds|	|Vbs|	|Reverse bias|	|Vce|	|Delta V|
MOS	NMOS (1.8V)	nch	0~1.8	0~1.8	0~1.8	-	-	-
	PMOS (1.8V)	pch	0~1.8	0~1.8	0~1.8	-	-	-
	NMOS (5V)	nch_5	0~5	0~5	0~5	-	-	-
	PMOS (5V)	pch_5	0~5	0~5	0~5	-	-	-
BJT	1.8V P+/NW/PSUB vertical PNP bipolar	pnp2 (Emitter area = 2×2 μm^2)	-	-	-	-	0~1.8	-
		pnp5 (Emitter area = 5×5 μm^2)	-	-	-	-	0~1.8	-
		pnp10 (Emitter area = 10×10 μm^2)	-	-	-	-	0~1.8	-
Diode	1.8V P+/Nwell Junction Diode	PDIO	-	-	-	0~1.8	-	-
	1.8V N+/Pwell Junction Diode	NDIO	-	-	-	0~1.8	-	-
	1.8V NW/Psub Junction Diode	NWDIO	-	-	-	0~1.8	-	-
	5V P+/Nwell Junction Diode	PDIO_5	-	-	-	0~5	-	-
	5V N+/Pwell Junction Diode	NDIO_5	-	-	-	0~5	-	-
	5V NW/Psub Junction Diode	NWDIO_5	-	-	-	0~5	-	-
Resistor	N+ OD w/i Silicide Resistor (6.82 Ohm/sq)	rnod	-	-	-	-	-	0~5
	N+ OD w/i Silicide Resistor (6.82 Ohm/sq)	rnodw	-	-	-	-	-	0~5
	P+ OD w/i Silicide Resistor (7.76 Ohm/sq)	rpod	-	-	-	-	-	0~5
	P+ OD w/i Silicide Resistor (7.76 Ohm/sq)	rpodw	-	-	-	-	-	0~5
	N+ OD w/o Silicide Resistor (59 Ohm/sq)	rnodrpo	-	-	-	-	-	0~5
	P+ OD w/o Silicide Resistor (133 Ohm/sq)	rpodrpo	-	-	-	-	-	0~5
	N-well. Under OD Resistor (440 Ohm/sq)	rnwod	-	-	-	-	-	0~5
	N-well. Under STI Resistor (927 Ohm/sq)	rnwsti	-	-	-	-	-	0~5
	N+ Poly w/i Silicide Resistor (7.89 Ohm/sq)	rnpo1	-	-	-	-	-	0~5
	N+ Poly w/i Silicide Resistor (7.89 Ohm/sq)	rnpo1w	-	-	-	-	-	0~5
	P+ Poly w/i Silicide Resistor (7.9 Ohm/sq)	rppo1	-	-	-	-	-	0~5
	P+ Poly w/i Silicide Resistor (7.9 Ohm/sq)	rppo1w	-	-	-	-	-	0~5
	N+ Poly w/o Silicide Resistor (311 Ohm/sq)	rnpo1rpo	-	-	-	-	-	0~5
	P+ Poly w/o Silicide Resistor (311 Ohm/sq)	rppo1rpo	-	-	-	-	-	0~5

3.4.2 CM018 1.8V/5V

Table 3.4.2 CM018 1.8/5V Device Feature

	Device	SPICE Name	|Vgs|	|Vds|	|Vbs|	|Reverse bias|	|Vce|	|Delta V|
MOS	1.8V Medium V_t NMOS	Mench	0~1.8	0~1.8	0~1.8	-	-	-
	1.8V Medium V_t PMOS	Mepch	0~1.8	0~1.8	0~1.8	-	-	-
	5V Medium V_t NMOS	mench5	0~5	0~5	0~5	-	-	-
	5V Medium V_t PMOS	mepch5	0~5	0~5	0~5	-	-	-
	1.8V Native NMOS	nanch	0~1.8	0~1.8	0~1.8	-	-	-
	5V Native NMOS	nanch5	0~5	0~5	0~5	-	-	-
BJT	1.8V N+/PW/DNW vertical NPN bipolar	NPN2 (Emitter area = 2×2 μm^2)	-	-	-	-	0~1.8	-
		NPN5 (Emitter area = 5×5 μm^2)	-	-	-	-	0~1.8	-
		NPN10 (Emitter area = 10×10 μm^2)	-	-	-	-	0~1.8	-
BJT	5V N+/PW/DNW vertical NPN bipolar	NPN2 (Emitter area = 2×2 μm^2)	-	-	-	-	-2.5~4	-
		NPN5 (Emitter area = 5×5 μm^2)	-	-	-	-	-2.5~4	-
		NPN10 (Emitter area = 10×10 μm^2)	-	-	-	-	-2.5~4	-
BJT	5V P+/NW/PSUB vertical PNP bipolar	PNP2 (Emitter area = 2×2 μm^2)	-	-	-	-	0~5	-
		PNP5 (Emitter area = 5×5 μm^2)	-	-	-	-	0~5	-
		PNP10 (Emitter area = 10×10 μm^2)	-	-	-	-	0~5	-
DIODE	1.8V Medium VT P+/Nwell Junction Diode	PDIO_M	-	-	-	0~1.8	-	-
	1.8V Medium VT N+/Pwell Junction Diode	NDIO_M	-	-	-	0~1.8	-	-
	DNW/Psub Junction Diode	DNWPSUB	-	-	-	0~5	-	-
	1.8V PW/DNW Junction Diode	PWDNW	-	-	-	0~1.8	-	-
	5V PW/DNW Junction Diode	PWDNW_5	-	-	-	0~5	-	-
Resistor	HRI P-Poly w/o silicide W≥1um (1075 Ohm/sq)	rppolyhri	-	-	-	-	-	0~5
Capacitor	MIM capacitor (1fF/um^2)	mimcap	-	-	-	-	-	0~5

3.4.3 BJT Device List

Table 3.4.3 BJT Device Feature

BJT Device	SPICE Name	1.8/5V Logic	1.8/5V Mixed Signal
1.8V P+/NW/PSUB vertical PNP bipolar	NPN2 (Emitter area = 2×2 μm^2)	V	V
	NPN5 (Emitter area = 5×5 μm^2)	V	V
	NPN10 (Emitter area = 10×10 μm^2)	V	V
1.8V N+/PW/DNW vertical NPN bipolar	NPN2 (Emitter area = 2×2 μm^2)		V
	NPN5 (Emitter area = 5×5 μm^2)		V
	NPN10 (Emitter area = 10×10 μm^2)		V
5V N+/PW/DNW vertical NPN bipolar	NPN2 (Emitter area = 2×2 μm^2)		V
	NPN5 (Emitter area = 5×5 μm^2)		V
	NPN10 (Emitter area = 10×10 μm^2)		V
5V P+/NW/PSUB vertical PNP bipolar	NPN2 (Emitter area = 2×2 μm^2)		V
	NPN5 (Emitter area = 5×5 μm^2)		V
	NPN10 (Emitter area = 10×10 μm^2)		V

4 Layout Rules and Recommendations

This chapter provides the following general layout information:

4.1 Layout Rule Conventions

Layout rules follow these conventions:

- Unless otherwise specified, all rules are of minimum dimension.
- The basic unit of measure is um; the basic area is um^2.
- Process, product, and reliability yields are expected to be improved when designs are relaxed from minimum dimensions. Minimum dimensions showed only to be used to shrink the chip size or to improve the circuit performance.
- Design rules requiring exact dimensions (“=” in the rule tables) are not to be relaxed.
- Recommendations are designated by a registered symbol “®” after the rule number.
- A registered symbol “U“ is marked after the rule number as the rule is not checked by DRC.
- Guidelines are designed by registered symbol “g” after the rule number.
- Recommendation is used to improve device performance based on existing rule (better to have) and guideline is just a reference (nice to have) without related rule.
- Bracket usage is the rules should be noted carefully:
  - Parentheses ( ) are used for explanations.
  - Square brackets [ ] are used for certain conditions.
  - Curved brackets { } are used to indicate that an operation is performed.

4.2 Special Geometries Used in Physical Design Rules

The following definitions are used in physical design rules:

4.2.1 Derived Geometries

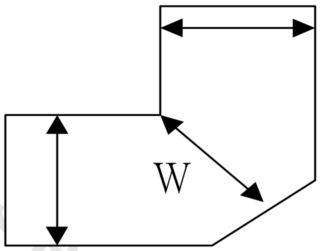
Term	Definition
N+OD	NP AND OD
P+OD	PP AND OD
GATE	PO AND OD
FIELD	NOT OD
PW	NOT NW
Dummy CTM	CTM NOT Interact VIAn

4.2.2 Special Definition

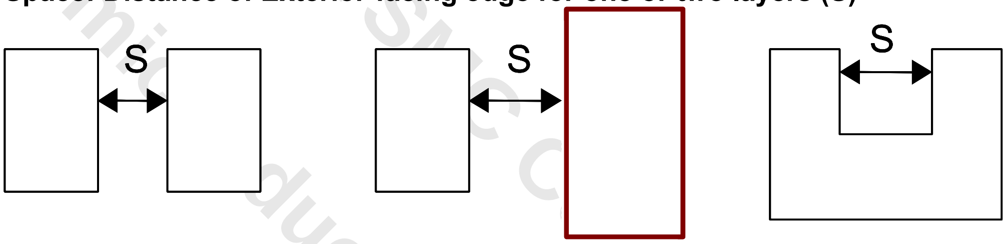
Term	Definition
NW	N-WELL
RW	PW inside DNW
M_{top}	The last metal layer (either Mn or UTM)
M_{top-1}	1st metal layer below M_{top}, that is, the last Mx layer
VIA_{top-1}	1st VIA hole below VIAn, that is, the last VIAx layer

4.3 Definition of Layout Geometrical Terminology

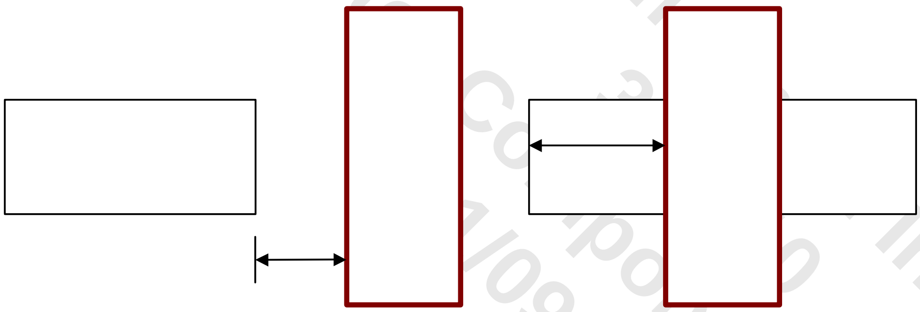
Width: Distance of interior-facing edge for a single layer (W)



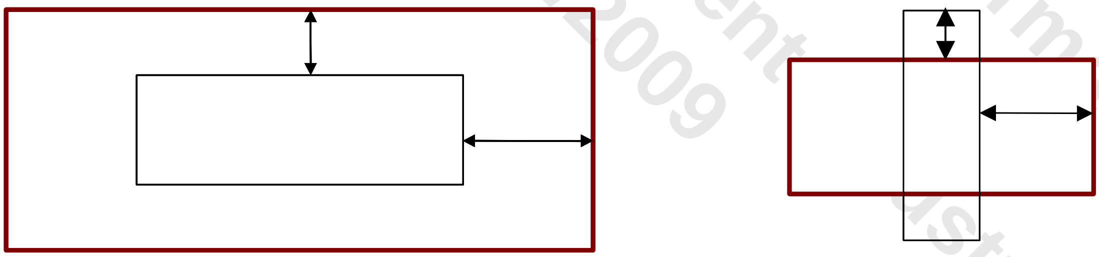
Space: Distance of Exterior-facing edge for one or two layers (S)



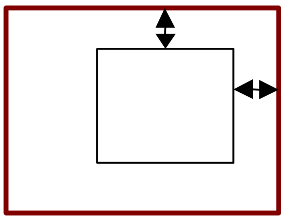
Clearance:



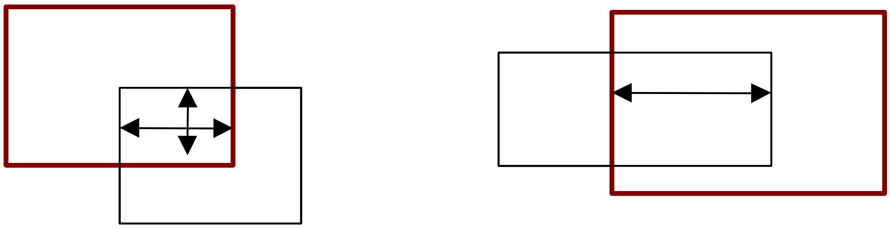
Extension: Distance of inside edge to outside edge (EX)



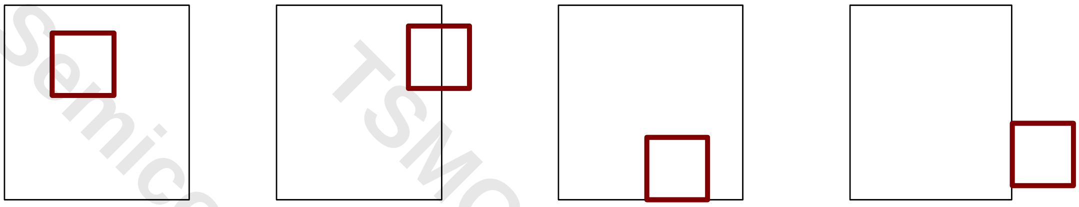
Enclosure: Distance of inside edge to outside edge (Fully inside) (EN)



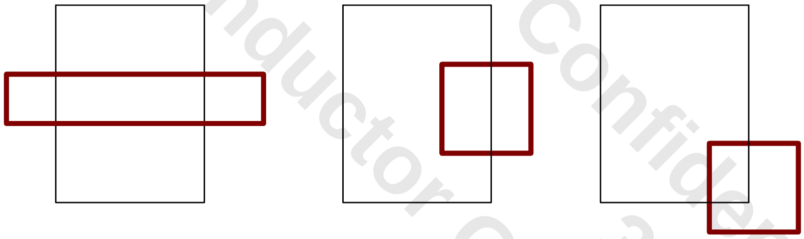
Overlap: Distance of interior-facing edge for two layers (O)



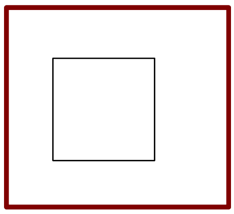
Interact



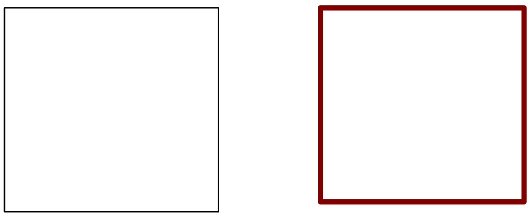
Cut



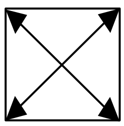
Inside



Outside



Area (A):



4.4 Minimum Pitches

DNW Pitch	8.00um (Width/Space: 3um / 5um)
CTM Pitch	5.20um (Width/Space: 4um / 1.2um)

4.5 Layout Rules and Guidelines

4.5.1 Deep N-Well (DNW) Layout Rules (Mask ID: 119)

Please refer to T-018-LO-DR-001 4.6.1 for DNW layout rule.

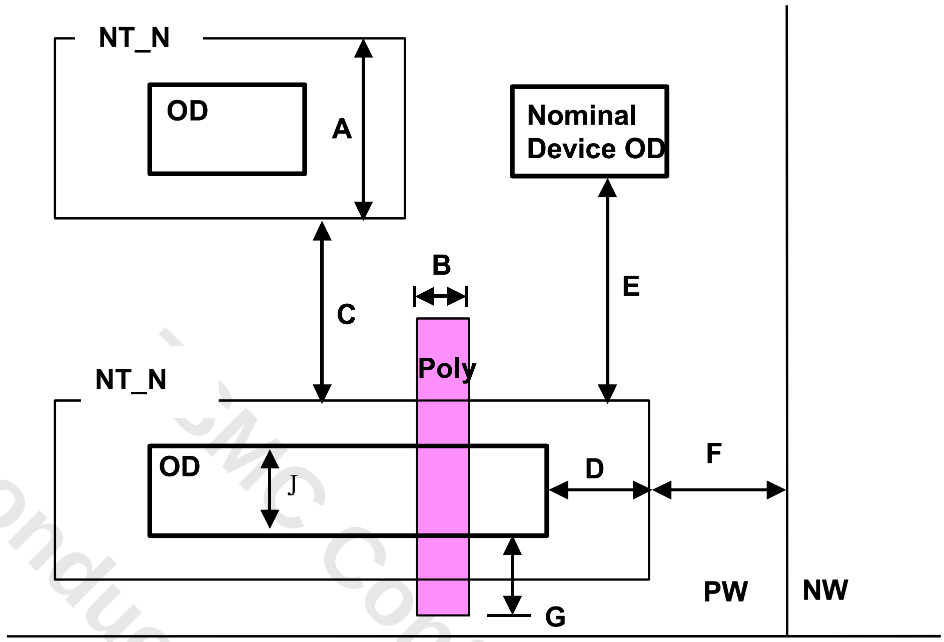
4.5.2 Native Device (NT_N) Layout Rules

NT_N, Native NMOS Blocked Implant Definition

- This layer is used for mask making rather than process requirements. If you use native NMOS devices in a circuit design, please use this drawn layer with NW to generate PW.

Rule No.	Description	Label		Layout Rule
Layer:	NT_N – Implant Definition to block PW, channel_N and VT_N implant for NMOS native device.			
NT_N.I.1	NT_N interact DNW is not allowed. (Butted is allowed)			
NT_N.I.2	Only one OD region allowed to be put in an NT_N region			
NT_N.I.3	A P+ Poly gate is not allowed to be put in an NT_N region			
NT_N.I.4	A bent Poly region is not allowed to be put in an NT_N region			
NT_N.W.1	Minimum dimension of a NT_N region.	A	≧	0.740
NT_N.W.2	Minimum Poly gate dimension of a 1.8V blocked NT_N device	B	≧	0.500
	Minimum Poly gate dimension of a 5V blocked native device.		≧	1.600
NT_N.W.3	Minimum OD dimension of a 5V blocked native device.	J	≧	1.200
NT_N.S.1	Minimum space between two NT_N regions.	C	≧	0.860
NT_N.E.1	Maximum and Minimum extension from a NT_N region beyond an NP OD region.	D	=	0.260
NT_N.C.1	Minimum clearance from a NT_N region to nominal OD region.	E	≧	0.520
NT_N.C.2	Minimum clearance from a NT_N region to an N-well edge.	F	≧	1.660
NT_N.PO.1	Minimum overlap of a PO region extended into field oxide (endcap)	G	≧	0.350

NT_N



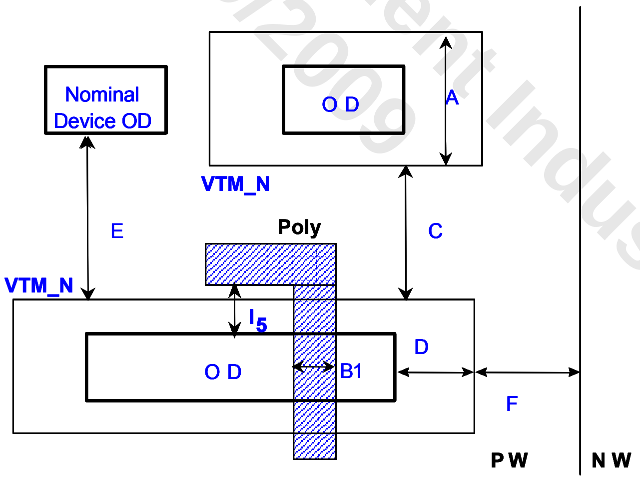
4.5.3 Medium Vt NMOS (VTM_N) Layout Rules (for 1.8V, Mask ID:118; for 5V, Mask ID:102)

VTM_N, Medium Vt NMOS Blocked Implant Definition

Thi layer is used to block 1.8V or 5V VTM_N implant. If you use medium VT NMOS device in a circuit design, TSMC will use this drawn layer with NW/OD2 to generate:

- 1.8V VTM_N mask*: Mask 118 is a reverse tone of (((OD2 OR NW) OR VTM_N) OR NT_N).*
- 5V VTM_N mask. *Mask 102 is generated by (((OD2 NOT NW) NOT VTM_N) NOT NT_N).*

Rule No.	Description	Label		Rule
VTM_N.W.1	Minimum dimension of a VTM_N region.	A	≧	0.74
VTM_N.W.2	Minimum PO gate dimension of a 1.8V medium Vt NMOS.	B_1	≧	0.30
VTM_N.W.4	Minimum PO gate dimension of a 5V medium Vt NMOS.	B_1	≧	0.80
VTM_N.S.1	Minimum space between two VTM_N regions. Merge if less than 0.44um.	C	≧	0.44
VTM_N.E.1	Minimum extension from a VTM_N region beyond an N+ OD region.	D	≧	0.26
VTM_N.C.1	Minimum clearance from a VTM_N region to an N+ OD region.	E	≧	0.70
VTM_N.C.2	Minimum clearance from a VTM_N region to an NW edge. (VTM_N interact NW is not allowed.)	F	≧	0.43
VTM_N.R.1	VTM_N interact DNW is not allowed. (Butted is allowed)			
VTM_N.R.2	VTM_N interact NT_N is not allowed. (Butted is allowed)			
VTM_N.R.3	A P+ GATE is not allowed in VTM_N region.			
VTM_N.R.4	A bent PO region is not allowed in VTM_N region.			
VTM_N.R.5	Minimum clearance from an OD region in VTM_N region to a PO on field oxide	I_5	≧	0.26



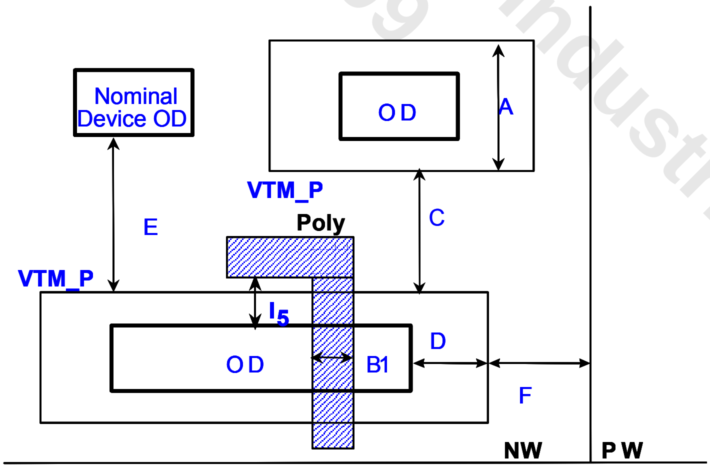
4.5.4 Medium Vt PMOS (VTM_P) Layout Rules (for 1.8V, Mask ID: 117; for 5V, Mask ID:103)

VTM_P, Medium Vt PMOS Blocked Implant Definition

This layer is used to block VTM_P implant. If you use medium VT PMOS device in a circuit design, TSMC will use this drawn layer with NW/OD2 to generate:

- 1.8V VTM_P mask. *Mask 117 is generated by ((NW NOT OD2) NOT VTM_P).*
- 5V VTM_P mask. *Mask 103 is generated by ((NW AND OD2) NOT VTM_P).*

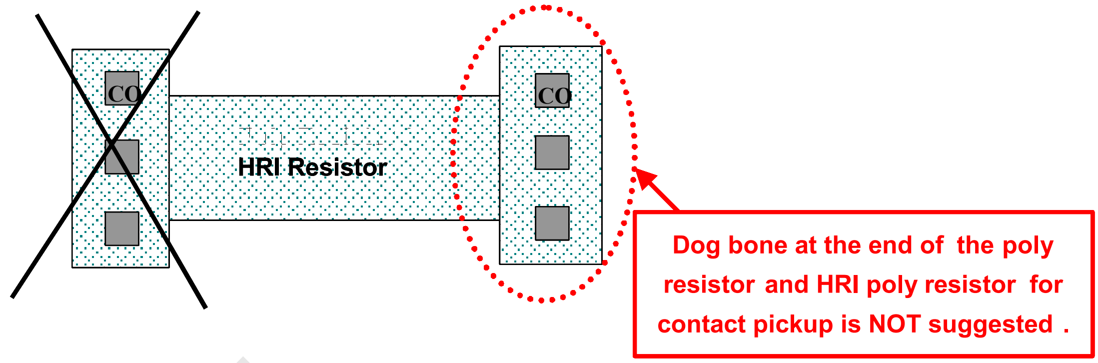
Rule No.	Description	Label		Rule
VTM_P.W.1	Minimum dimension of a VTM_P region.	A	≧	0.74
VTM_P.W.2	Minimum PO gate dimension of a 1.8V medium Vt PMOS.	B_1	≧	0.25
VTM_P.W.3	Minimum PO gate dimension of a 5V medium Vt PMOS.	B_1	≧	0.8
VTM_P.S.1	Minimum space between two VTM_P regions. Merge if less than 0.44um.	C	≧	0.44
VTM_P.E.1	Minimum extension from a VTM_P region beyond a P+ OD region.	D	≧	0.26
VTM_P.C.1	Minimum clearance from a VTM_P region to a P+ OD region.	E	≧	0.70
VTM_P.C.2	Minimum clearance from a VTM_P region to a PW edge. (VTM_P interact PW is not allowed.)	F	≧	0.43
VTM_P.R.1	VTM_P interact DNW is not allowed. (Butted is allowed)			
VTM_P.R.2	VTM_P interact NT_N is not allowed (Butted is allowed)			
VTM_P.R.4	A N+ GATE is not allowed in VTM_P region.			
VTM_P.R.5	A bent PO region is not allowed in a VTM_P region.			
VTM_P.R.6	Minimum clearance from an OD region in VTM_P region to a PO on field oxide	I_5	≧	0.26



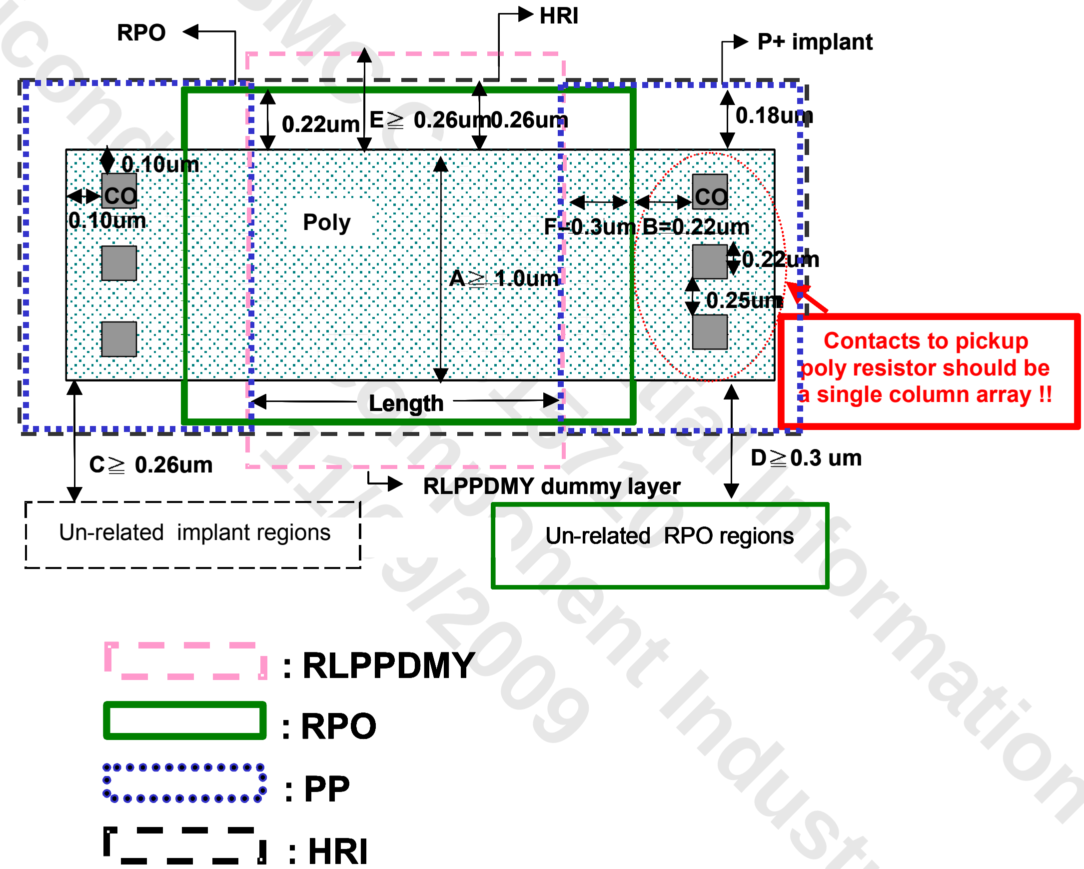
4.5.5 HRI Poly Resistor Rule

Dummy layers RLPPDMY is required for performing logic operation and DRC HRI poly resistor (please refer to T-018-MM-MB-001).

Rule No.	Description	Label		Rule
PO.W.1_HRI	Minimum width of a PO region for the high resistance poly resistor	A	≧	1.00
RPO.O.1_HRI	Minimum and maximum overlap of a PP for high poly resistor (HRI) end implant to a RPO region.	F	＝	0.30
RES.HRI.1®	It is strongly recommended that the HRI poly resistor width ≥ 1.0 um and resistor number of square $N_{sq} \geq 2$. (DRC will check the width and length 1um and 2um, respectively. Nsq is un-checkable)			
RES.HRI.2®	Recommend: the maximum and minimum clearance from a RPO to a contact on HRI poly resistor	B	＝	0.22
RES.HRI.3®	Recommend: the minimum clearance from HRI poly resistor to un-related implant regions	C	≧	0.26
RES.HRI.4®	Recommend: the minimum clearance from a un-related RPO to HRI poly resistor	D	≧	0.3
RES.HRI.5®	Recommend: Contact pickup of HRI poly resistor should be in a single column.			
RES.HRI.6®U	Recommend: Do not to use dog bone at the end of HRI poly resistor for contact pickup.			
RES.HRI.7®	Recommend: the minimum clearance from a RLPPDMY to the HRI poly resistor	E	≧	0.26



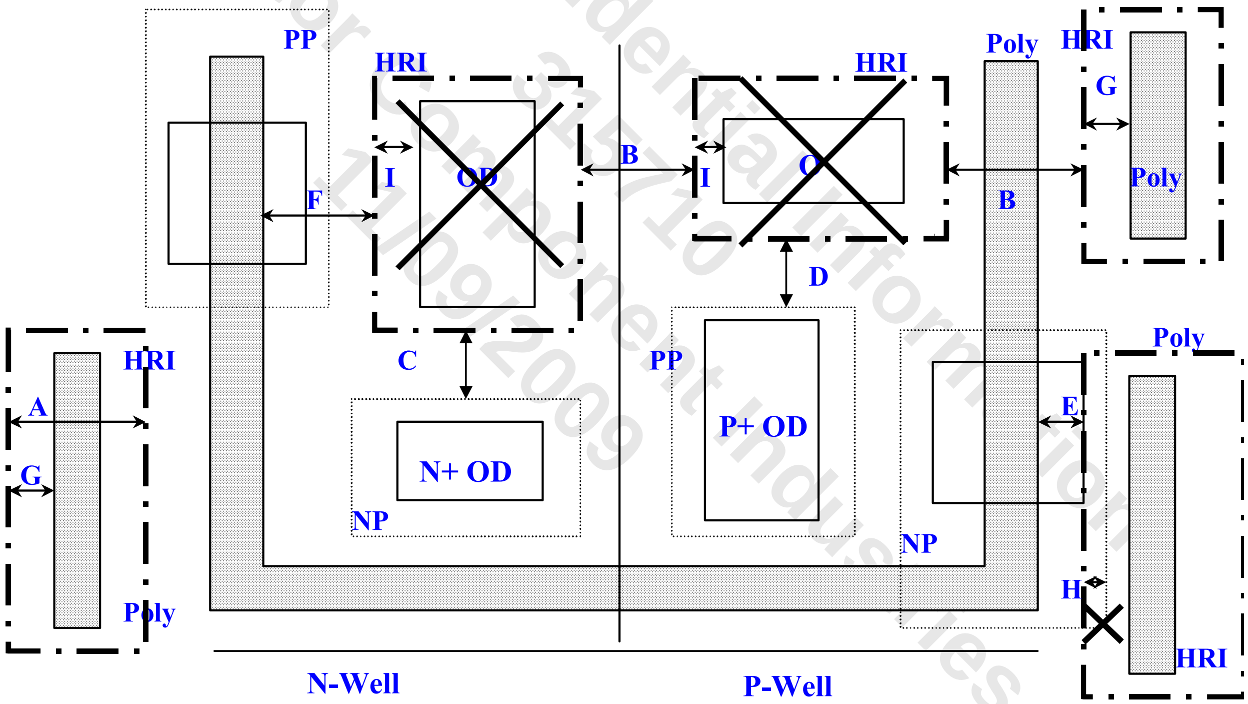
** High Poly Resistor (HRI) with RPO



4.5.6 High Resistor Implant (HRI) Layout Rules (Mask ID: 133)

RLPPDMY (CAD layer: 134) is a dummy layer for HRI poly resistance of DRC and logic operation.

Rule No.	Description	Label		Rule
HRI.W.1	Minimum width of a HRI region.	A	≧	0.44
HRI.S.1	Minimum space between two HRI regions. Merge if less than 0.44um.	B	≧	0.44
HRI.C.1	Minimum clearance from an HRI region to an NP region.	C	≧	0.26
HRI.C.2	Minimum clearance from an HRI region to a PP region.	D	≧	0.26
HRI.C.3	Minimum clearance from an HRI edge to an N-channel Poly gate.	E	≧	0.32
HRI.C.4	Minimum clearance from an HRI edge to a P-channel Poly gate.	F	≧	0.32
HRI.E.1	Minimum extension from an HRI region beyond a PO resistor region.	G	≧	0.26
HRI.R.1	Overlap of NP and HRI is not allowed.	H		
HRI.R.2	Overlap of OD and HRI is not allowed.	I		
HRI.A.1	Minimum area of a HRI region.	J	≧	0.3844



4.5.7 MIM Capacitor Layout Rules

- The MIM capacitors must be placed between the top two metal layers (M_{top} & M_{top-1}). The following layers are needed for MIM capacitor formation:
  (a) Top plate of the MIM capacitor: A drawn CAD layer CTM (CAD layer: 67) is required. CTM is not allowed for local interconnections.
  (b) Bottom plate of the MIM capacitor: the M_{top-1} (the last Mx) is required to form the MIM capacitors with CTM.
- VIAn is used for the connection between CTM and $M_{top.}$
- Three groups of layout rules are required for the MIM design:
  a) Mx rules for MIM capacitor bottom metal; (Section 4.5.7.1)
  b) CTM rules of the MIM capacitor top metal; (Section 4.5.7.2)
  c) VIA rules of the MIM capacitor; (Section 4.5.7.3)

4.5.7.1 Mx Layout Rules for Capacitor Bottom Metal

This section provides rules for the Mx (inter-metal layer) as the capacitor bottom metal. For 1P6M process, the inter-metal layer M5 is used as the MIM capacitor bottom metal.

Rule No.	Description	Label		Rule
MIM_Mx.W.1	Maximum dimension (both width and length) of Mx as MIM capacitor bottom metal		≦	35
MIM_Mx.S.1	Minimum space between two Mx regions as MIM capacitor bottom metal	B_3	≧	0.80
MIM_Mx.S.2	Minimum space between one Mx region as a dummy MIM capacitor bottom metal and the other Mx region as MIM capacitor bottom metal (Fig. 4.5.7.2)	B_2	≧	0.80
MIM_Mx.E.3	Minimum extension of an Mx region as MIM capacitor bottom metal beyond a CTM region and dummy CTM region.	E	≧	0.40

4.5.7.2 Capacitor Top Metal (CTM) Layout Rules (Mask ID: 182)

Rule No.	Description	Label		Rule
CTM.W.1	Minimum width of a CTM region.	A	≧	4.00
CTM.W.2	Minimum width of a dummy CTM region.	A_1	≧	0.40
CTM.S.1	Minimum space between two CTM regions.	B	≧	1.20
CTM.S.2	Minimum space between: a) a dummy CTM and a CTM region (Fig. 4.5.7.1) b) a dummy CTM and a dummy CTM	B_1	≧	0.80
CTM.R.2	Minimum density of all CTM (CTM+ dummy CTM) area 1. Density = total CTM layout area/chip area. 2. Dummy CTM is required for those with CTM density less than 3.0% for better matching behavior and process uniformity.		≧	3%
CTM.R.3	VIAn on dummy CTM is not allowed.			
CTM.W.4	Maximum dimension (one side) of a CTM region For example, 26um x 31um CTM is not allowed.		≦	30
CTM.A.1	Minimum area of CTM region (include dummy CTM)		≧	0.202
CTM.R.1	All CTM regions (include dummy CTM) cut Mx region as MIM capacitor bottom metal is not allowed.			
CTM.R.5	The MIM capacitor must be placed between the top two metal layers.			
CTM.R.4®[U]	Recommended: Designer needs to take care of the impact of the noise coupling if any circuit or routing is put under MIM.			

4.5.7.3 VIA Layout Rules for MIM Capacitor

In this section, VIAn is the top VIA (size 0.36um) which follows the VIA5 rules at T-018-LO-DR-001. VIA_{top-1} is the last inter VIA layer (size 0.26um) which follows the VIAx rules at T-018-LO-DR-001.

Rule No.	Description	Label		Rule
MIMVIA.S.1	Minimum space between two VIAn on the same CTM	I	≧	2.00
MIMVIA.S.2	Minimum space between two VIAn on the same MIM capacitor bottom metal	J	≧	4.00
MIMVIA.E.1	Minimum extension of a CTM region beyond a VIAn region.	C	≧	0.24
MIMVIA.E.2	Minimum extension of an Mx region as MIM capacitor bottom metal beyond a VIA_{top-1} or a VIAn region.	D	≧	0.12
MIMVIA.C.1	Minimum clearance of a VIA_{top-1} or a VIAn to a CTM region.	F	≧	0.40
MIMVIA.R.1	Minimum density of VIAn on CTM		≧	1 %
MIMVIA.R.3	VIA_{top-1} under CTM region is not allowed.			
MIMVIA.S.1®[U]	Recommended: Minimum and maximum space between two VIAn on CTM for SPICE simulation accuracy.	I	=	2.00
MIMVIA.S.2®[U]	Recommended: Minimum and maximum space between two VIAn on the MIM capacitor bottom metal for SPICE simulation accuracy.	J	=	4.00
MIMVIA.R.1®[U]	1. Please put the VIAn on the MIM capacitor bottom metal as many as possible for the purpose of high Q value in high frequency application. 2. Avoid using single VIAn to obtain lower parasitic resistance for more accurate SPICE simulation. 3. VCC < 60 ppm is only guaranteed for VIAn space = 4um (on MIM capacitor bottom metal) and VIAn space = 2um (on CTM).			
MIMVIA.R.2®[U]	Metal routing under MIM is allowed. Nonetheless, to place routing metal under MIM, it is strongly recommended to add a high frequency signal isolation metal layer under the MIM capacitor bottom metal. Customer should refer to TSMC PDK for better model accuracy.			

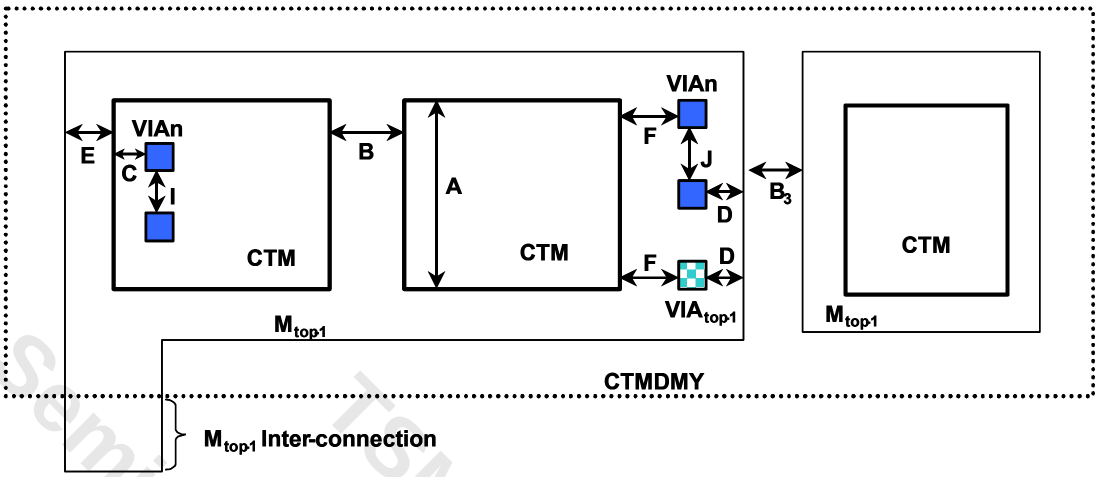


Fig. 4.5.7.1

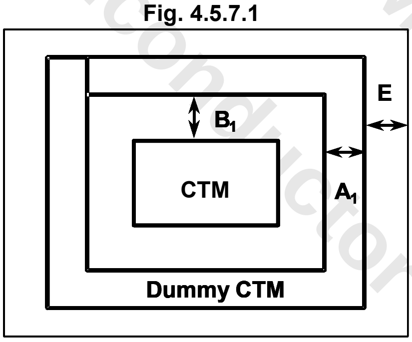
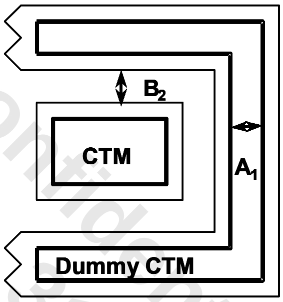
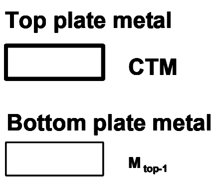
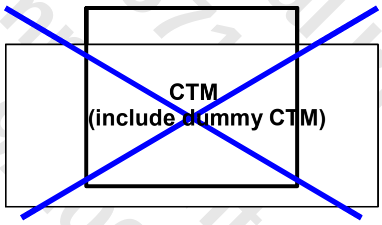


Fig. 4.5.7.2

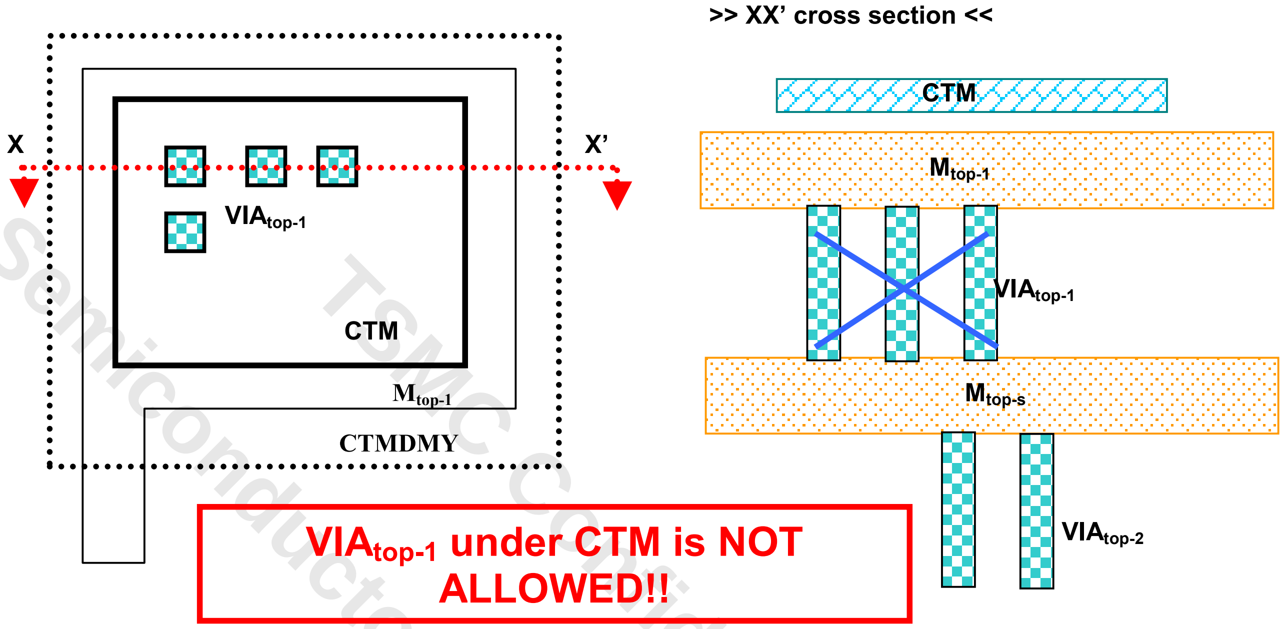




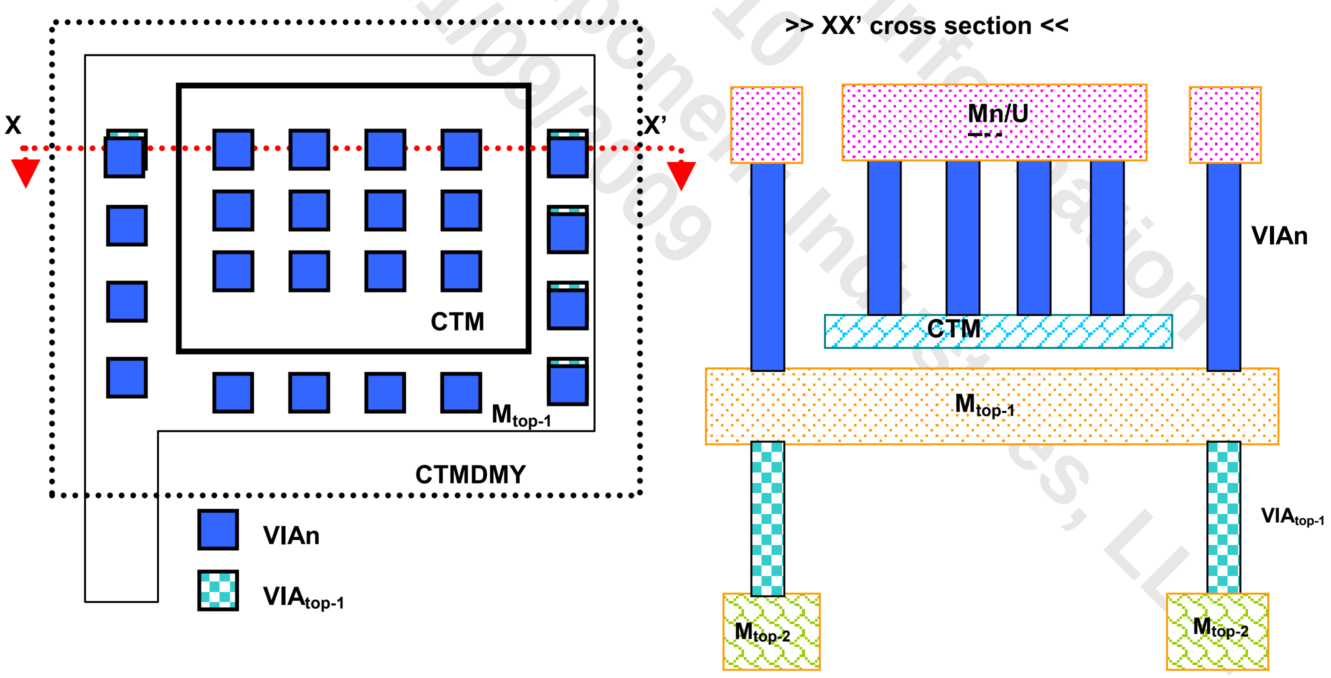
CTM.R.1



Layout Depiction of Rule MIMVIA.R.3



☐ **Layout Sample for MIM Capacitor (MIMVIA.S.1 & MIMVIA.S.2):**



4.5.8 Antenna Effect Prevention Layout Rules for MIM Capacitor

4.5.8.1 Overview

Antenna effect for MIM capacitor should be taken into consideration for your MIM capacitor design. The layout style of the MIM capacitor will impact its immunity to the antenna effect during process. Two major structures are defined:

(A) Floating MIM capacitor:

Floating MIM capacitor means both nodes of the MIM capacitor do not connect to the OD region. This structure offers high antenna ratio for both nodes. As illustrated in Fig.4.5.8.1, the MIM nodes can be either floating or tied to gate.

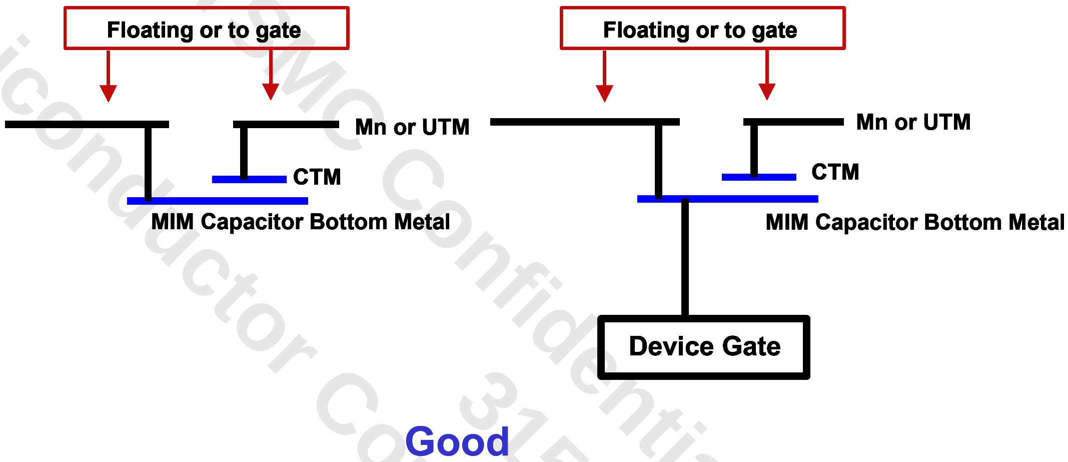


Fig.4.5.8.1 Schematic for floating MIM capacitor

(B) Single- node of the MIM capacitor is connected to the OD region:

The connection examples are illustrated in Fig.4.5.8.2. The plasma during top metal etching will stress MIM capacitor more severely, as in Fig.4.5.8.2(A) -- the MIM capacitor bottom metal is connected to the OD region through VIA_{top-1} and CTM is floating through VIAn.

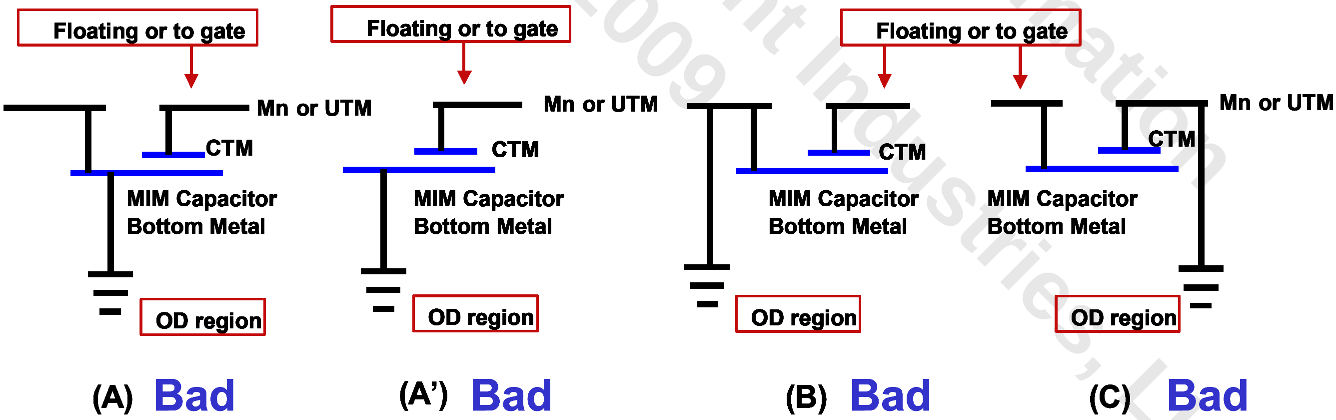


Fig. 4.5.8.2 Schematic for single-node of the MIM capacitor connected to the OD region

- To have better immunity for structure (B), it's suggested adding protection diodes on the associated terminal. In Fig.4.6.6.3, the protection diode is added on the CTM terminal and it can offer the other plasma discharge path and therefore, the MIM capacitor can be less affected by plasma damage.

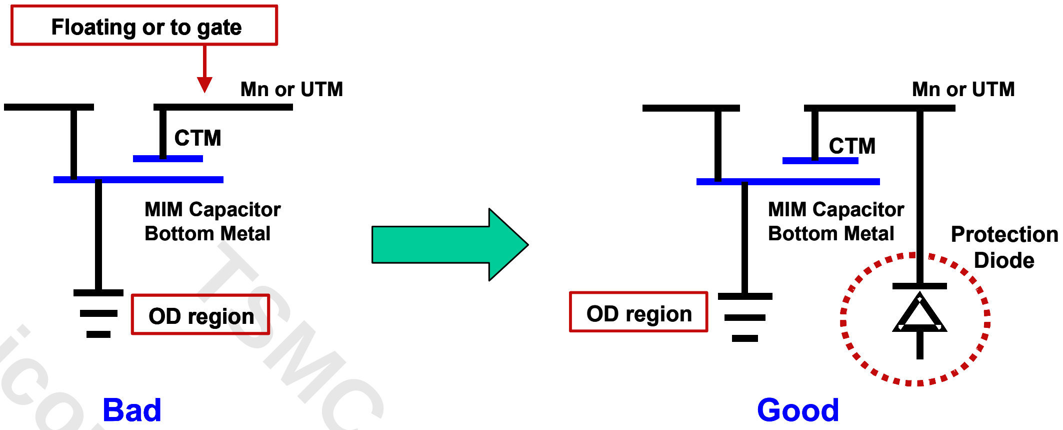


Fig. 4.5.8.3 Adding protection diode to improve the immunity to plasma damage

4.5.8.2 Antenna Effect Prevention Layout Rules

The following table provides antenna effect prevention rules. The rules are for the metal layers above the CTM. Take 1P4M process for example, only M4 should be checked.

Rule No.	Description		Antenna Ratio	
			CTM Node	Capacitor bottom metal node
A.R.MIM.1	Maximum ratio of Mn (or UTM) perimeter area to the MIM capacitor when neither CTM nor Mx as MIM capacitor bottom metal is connected to OD. (as structure (A))	≦	6000	6000
A.R.MIM.2	Maximum ratio of Mn (or UTM) perimeter area to the MIM capacitor when A) CTM is connected to OD; and B) Mx as MIM capacitor bottom metal is not connected to OD.	≦	NA	100
A.R.MIM.3	Maximum ratio of Mn (or UTM) perimeter area to the MIM capacitor when A) CTM is not connected to OD; and B) Mx as MIM capacitor bottom metal is connected to OD.	≦	100	NA
A.R.MIM.4	Maximum ratio of Mn (or UTM) perimeter area to the MIM capacitor when CTM and Mx as MIM capacitor bottom metal are both connected to OD or diode. For CTM node, the diode area is defined as: 1. The protection diode that is connected to CTM. 2. The diode area should be larger than, or equal to, 0.203 um^2. For Mx as MIM capacitor bottom metal, the diode area is defined as: 1. The protection diode that is connected to Mx as MIM capacitor bottom metal. 2. The diode area should be larger than, or equal to, 0.203 um^2.	≦	diode area * 400 + 2200	

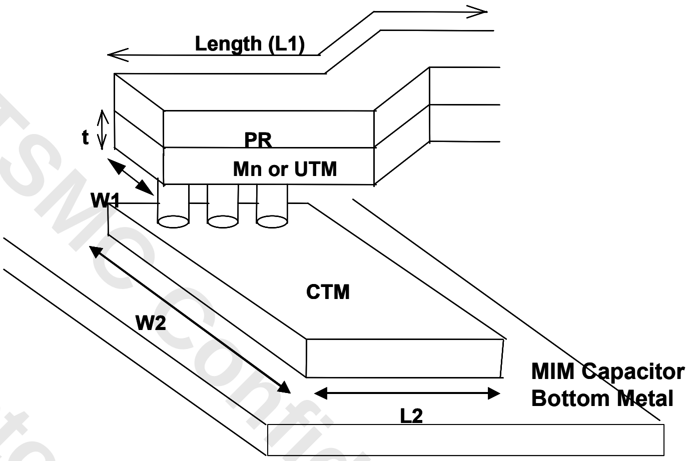
The thickness of M1-M5 is 5300Å.
The thickness of M6 is 9900Å.
The thickness of 20KÅ UTM is 23400Å.
The thickness of 40KÅ UTM is 46000Å.

- **The definition antenna ratio for each layer related to MIM capacitor:**

(A) CTM node Antenna Ratio

ratio ＝ 2 []L1 +)1)x t] / (W2 x L2)

L1 : metal length connected to CTM
W1 : metal width connected to CTM
t : metal thickness
W2 : connected CTM width
L2 : connected CTM length

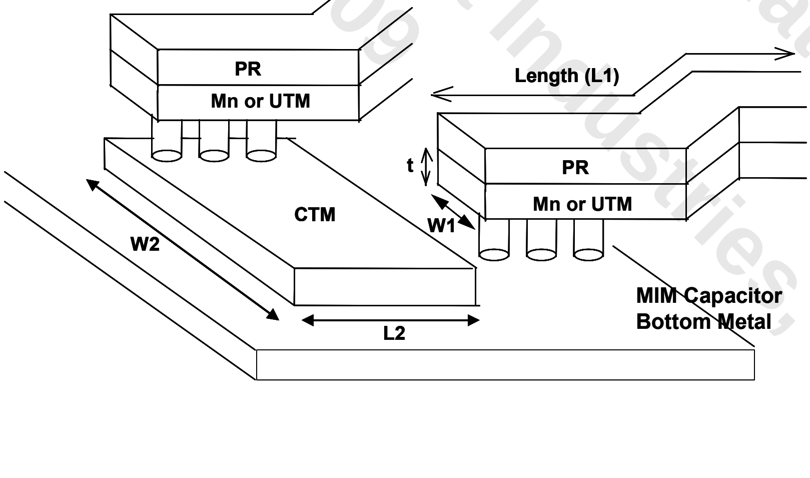


(B) The Antenna Ratio for Mx as MIM capacitor bottom metal

ratio ＝ 2 [(L1 +W1)x t] / (W2 x L2)

L1 : metal length connected to Mx as MIM capacitor bottom metal
W1 : metal width connected to Mx as MIM capacitor bottom metal
t : metal thickness
W2 : connected CTM width
L2 : connected CTM length

Note: For A.R.MIM.2 and A.R.MIM.4, only CTM connected to the OD will be calculated.



4.5.9 Ultra Thick Metal (UTM) Layout Rules (Mask ID: 186)

- UTM (20KÅ or 40KÅ thickness) is not allowed using with Mn (8KÅ thickness) in the same chip.
- UTM 20KÅ is not allowed using with UTM 40KÅ in the same chip.

4.5.9.1 20KÅ UTM design rule

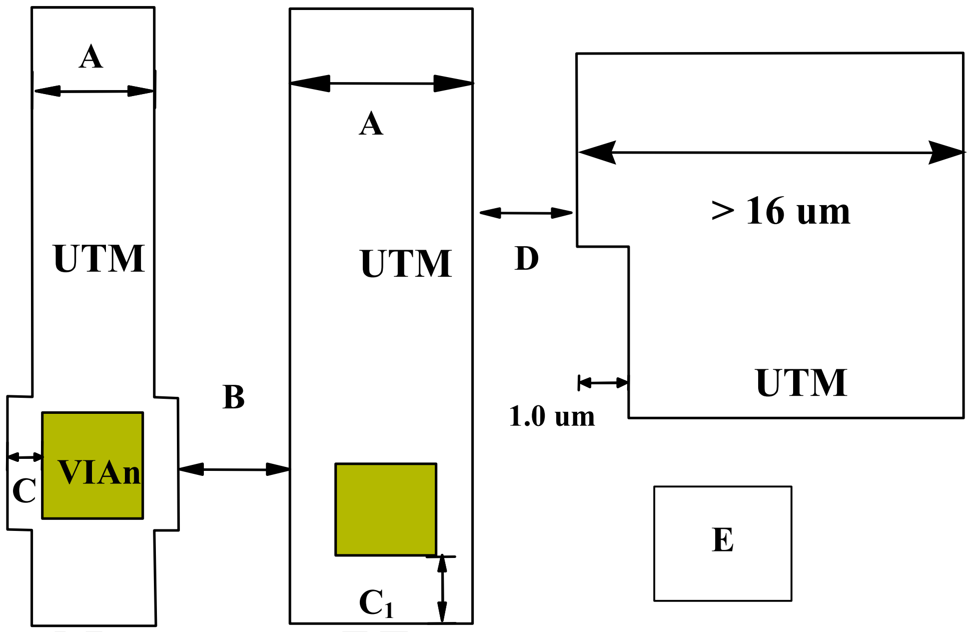
Rule No.	Description	Label		Rule
UTM20K.W.1	Minimum width of a UTM region	A	≧	1.50
UTM20K.S.1	Minimum space between two UTM regions	B	≧	1.50
UTM20K.E.1	Minimum extension of UTM region beyond VIAn	C	≧	0.30
UTM20K.E.2	Minimum extension of UTM region beyond VIAn at the end of UTM.	C_1	≧	0.45
UTM20K.S.2	Minimum space between UTM metal lines with one or both metal line width and length are greater than 16um; this also includes all UTM metals attached to these areas or extending out for a distance of ≤ 1.0um (exclude the application for inductor).	D	≧	3.00
UTM20K.A.1	Minimum area of a UTM region	E	≧	2.25
UTM20K.R.1	Minimum density of UTM area (exclude the application of inductor). 1. Density is calculated as: Total metal layout area/ chip area. 2. Dummy pattern is required for those with UTM density less than 30 %. A dummy metal example, which TSMC used in qual. vehicle, is 2.0 um x 5.0 um dummy lines with line spacing of 2.0 um.		≧	30.0%
UTM20K.C.1	Minimum clearance from one UTM used as inductor device to other UTM region. 1. INDDMY dummy layer is required to define the inductor device. 2. Three types of inductor layout are offered in TSMC PDK.	F	≧	50
UTM20K.E.3	Minimum extension of dummy“layer ”INDDMY" region beyond one UTM region which used as one inductor device.	G	≧	50
UTM20K.I.1	Via and metal layers inside INDDMY region are not allowed except underpass vias, metal interconnect and the substrate pick up node of the inductor.			
UTM20K.I.2	Both active and passive devices inside INDDMY region are not allowed.			

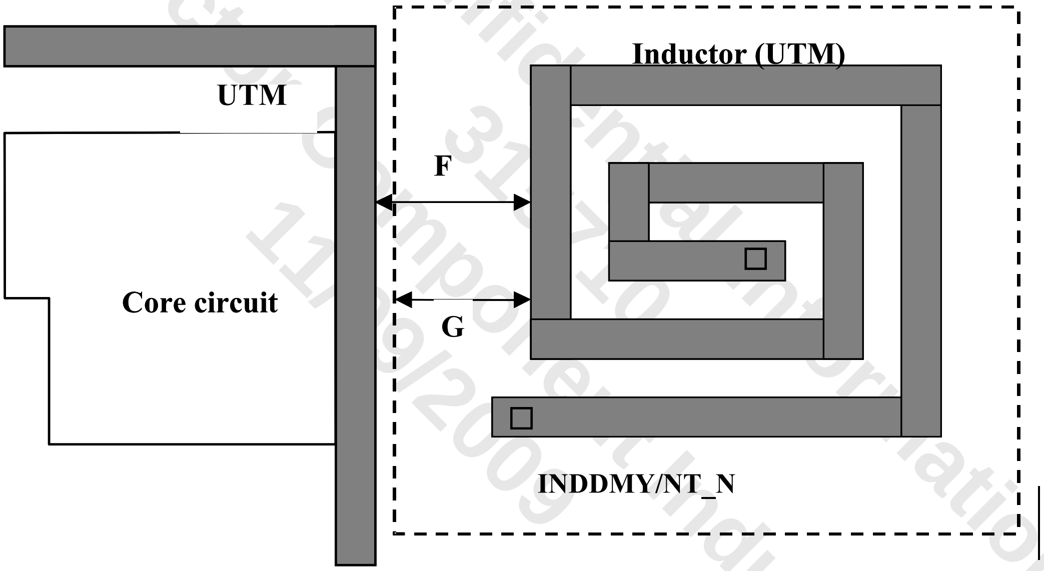
note: For inductor devices offered in TSMC's SPICE model, a native substrate region is adopted under the inductor coil to minimize eddy currents. This native substrate is specified by use of an NT_N (CAD#129) layer with the exact shape as the INDDMY layer. This NT_N drawn layer adds no process cost and no extra mask. And it is included in the TSMC PDK and its associated sample layout document. For those who prefer to draw inductors by themselves, designers have the option to draw a NT_N layer that exactly matches the INDDMY dummy marker layer geometry.

4.5.9.2 40KÅ UTM design rule

Rule No.	Description	Label		Rule
UTM40K.W.1	Minimum width of a UTM region	A	≧	2.60
UTM40K.S.1	Minimum space between two UTM regions	B	≧	2.50
UTM40K.E.1	Minimum extension of UTM region beyond VIAn	C	≧	0.40
UTM40K.E.2	Minimum extension of UTM region beyond VIAn at the end of UTM.	C_1	≧	0.45
UTM40K.S.2	Minimum space between UTM metal lines with one or both metal line width and length are greater than 16um; this also includes all UTM metals attached to these areas or extending out for a distance of ≤ 1.0um (exclude the application for inductor).	D	≧	4.00
UTM40K.A.1	Minimum area of a UTM region	E	≧	6.76
UTM40K.R.1	Minimum density of UTM area (exclude the application of inductor). 1. Density is calculated as: Total metal layout area/ chip area. 2. Dummy pattern is required for those with UTM density less than 30 %. A dummy metal example, which TSMC used in qual. vehicle, is 4.0 um x 4.0 um dummy lines with line spacing of 3.0 um.		≧	30.0%
UTM40K.C.1	Minimum clearance from one UTM used as inductor device to other UTM region. 1. INDDMY dummy layer is required to define the inductor device. 2. Three types of inductor layout are offered in TSMC PDK.	F	≧	50
UTM40K.E.3	Minimum extension of dummy“layer ”INDDMY" region beyond one UTM region which used as one inductor device. **Recommendations:** 1. Keep this enclosure as small and as close to 50 um as possible. 2. Keep INDDMY regions for separate inductors located as uniformly as possible over the whole chip area.	G	≧	50
UTM40K.I.1	Via and metal layers inside INDDMY region are not allowed except underpass vias, metal interconnect and the substrate pick up node of the inductor.			
UTM40K.I.2	Both active and passive devices inside INDDMY region are not allowed.			

note: For inductor devices offered in TSMC’s SPICE model, a native substrate region is adopted under the inductor coil to minimize eddy currents. This native substrate is specified by use of an NT_N (CAD#129) layer with the exact shape as the INDDMY layer. This NT_N drawn layer adds no process cost and no extra mask. And it is included in the TSMC PDK and its associated sample layout document. For those who prefer to draw inductors by themselves, designers have the option to draw a NT_N layer that exactly matches the INDDMY dummy marker layer geometry.





Dummy layer "INDDMY" is needed when UTM is implemented as inductor.

4.6 Reference Rule List

This document provides the related rules and reference information for the design and layout of integrated circuits using TSMC 0.18 um CMOS Mixed Signal (MIM) 1P6M (single poly, 6 metal layers), 1.8V/5V, salicide, Al technology. Some rules please refer to T-018-LO-DR-001 as list below:

T-018-LO-DR-001

4.5 LOGIC LAYOUT RULES AND GUIDELINES
4.5.1 N-Well (NW) Layout Rules (Mask ID: 192)
4.5.2 NW Resistor Layout Rules
4.5.4 Thin Oxide (OD) Layout Rules (Mask ID: 120)
4.5.5 Thick Oxide (OD2) Layout Rules (Mask ID: 132)
4.5.6 Poly (PO) Layout Rules (Mask ID: 130)
4.5.7 Poly Resistor and OD Resistor Guidelines
4.5.8 N+ S/D (NP) Layout Rules (Mask ID: 198)
4.5.9 P+ S/D (PP) Layout Rules (Mask ID: 197)
4.5.10 Resist Protection Oxide (RPO) Layout Rules (Mask ID: 155)
4.5.11 Contact (CO) Layout Rules (Mask ID: 156)
4.5.12 Metal-1 (M1) Layout Rules (Mask ID: 160)
4.5.13 VIA1 to VIA4 (VIAx) Layout Rules (Mask ID: 178, 179, 173, 174)
4.5.14 Metal-2 to Metal-5 (Mx) Layout Rules (Mask ID: 180, 181, 184, 185)
4.5.15 Top VIA (VIAn) Layout Rule (Mask ID: 175)
4.5.16 Top Metal (Mn) Layout Rule (Mask ID: 186)
4.5.17 Product Labels and Logo Layout Rules
4.5.18 Passivation (CB) & Polyimide (PM) Layout Rule (Mask ID: 107 & 009)
4.5.19 Metal Fuse Rule
4.5.20 Seal-Ring Rule
4.5.21 Antenna Effect Prevention (A) Layout Rules
4.5.22 Stress Release Rules
4.5.23 SRAM Guideline
4.5.24 Planar Capacitor EMB-SRAM Rules
4.6 MIXED SIGNAL & RF LAYOUT RULES AND GUIDELINES
4.6.1 Deep N-Well(DNW) Layout Rules(Mask ID:119)

5 Layout Guidelines for Latch-Up and I/O ESD

This chapter provides information about the following topics:

5.1 I/O ESD Protection Circuit Design and Layout Guideline

5.2 Layout Rule and Guideline for Latch-Up Prevention

If it is your first time to design ESD & Latch-Up circuit with TSMC design rules, it is strongly suggested treating below guidelines as rules for higher successful rate of new design. If your design has been verified by silicon, below content is guideline for your reference.

- **ESD rule numbers are the same as T-018-LO-DR-001, but update ESD.12g**
- **Latch up guidelines are the same as T-018-LO-DR-001, but update LUP.5.4g**

5.1 I/O ESD Protection Circuit Design and Layout Guideline

This Guideline is targeted to meet HBM>2KV and MM>200V ESD spec.

The ESD performance also depends on layout-style, which cannot be completely described in this guideline.

- **The ESD implant mask ID is 110 for 5V I/O designed by 5V NMOS. This layer is a drawing layer.**

5.1.1 General Guideline for ESD Protection

Rule No.	Description		Layout Rule
ESD.1g^{U}	Cannot use thick oxide transistor to protect thin oxide circuit; cannot use thin oxide transistor to protect thick oxide circuit.		
ESD.2g^{U}	NMOS and PMOS for ESD protection follow finger type structure with unique finger dimension and layout style.		
ESD.3g^{U}	Minimum N/PMOS total finger width for 5V and 1.8V I/O buffer.	≧	360
ESD.4g^{U}	Minimum total finger width for 5V and 1.8V power clamp device.	≧	360
ESD.5g^{U}	Minimum total finger width for 1.8V Power clamp device.	≧	720
ESD.6g	Unit finger width of NMOS and PMOS for I/O buffer (Fig.1)	≧	G 15 ~ 60
ESD.7g^{U}	ESD protection device should be surrounded by the appropriate base guard-ring. All other devices should be placed outside this guard-ring. It is illustrated in Fig.1.		
ESD.8g	Butting or inserted Substrate/Well pick-up's in the ESD N/PMOS are strictly prohibited. (see Fig.2)		
ESD.9g^{U}	OD area of edge side of ESD devices or I/O buffers should be Source or Bulk rather than Drain (see Fig.1), to avoid the unwanted parasitic bipolar effect or abnormal discharge path in ESD zapping.		
ESD.10g^{U}	Space between any two OD areas of the same type (N to N, or P to P) with one of the following connections should be larger than 2.4um, or a base guard ring (pickup ring) should be inserted in between them: One connects to a pad, and the other connects to another pad. One connects to a pad, and the other connects to VDD or VSS. One connects to VDD, and the other connects to VSS or another separated VDD.		
ESD.11g^{U}	Minimum resistance of I/O as R in Fig.3.	≧	200 Ω
ESD.12g^{U}	At least the NMOS4 in Fig.3 should be added after resistor R as the secondary ESD protection. For better ESD immunity, both PMOS to VDD and NMOS to VSS should be used there if no conflict with circuit operation. ESD implant can not be used in the secondary protecting devices. The suggested device sizes for secondary protection are: For 5V I/O: NMOS is 20/0.6 and PMOS is 20/0.5 For 1.8V I/O: NMOS is 20/0.20 and PMOS is 20/0.20 If the performance of CDM is concerned, the secondary protection should be put close to the device gate being protected.		(Use 5V devices) (Use 1.8V devices)
ESD.13g^{U}	Contacts and vias should be used as many as possible, and at least capable of bearing 100mA DC current (please calculate it from EM data).		
ESD.14g^{U}	Minimum total width of metal lines connecting bond pad and ESD protecting devices. (see Fig.1)		I 20
ESD.15g^{U}	Minimum Vss and Vdd power ring metal width.		50
ESD.16g^{U}	Bypass discharge cells should be inserted between separated VDD's and VSS's to ensure no ESD damage to internal circuits. It is of special importance to the isolated powers used only by a small circuit (<5K gates) The connections are illustrated in Fig.4. (For more details, please see "Tips for Power Bus".)		
ESD.17g^{U}	All nodes directly connecting to ESD discharge path should follow ESD dimension rules.		
ESD.18g	Minimum gate length for I/O buffer.		Lg Table 1

Table 1 Lg for I/O buffer

	NMOS	PMOS	ESD IMP *
1.8V Device	0.25	0.25	
5V Device	0.6	0.6	0.9

- ESD IMP* for 5V device: ESD mask (no. 110) is a drawing layer.

Table 2 RPO layout vs. ESD protection devices

No.	1	2
i/O Device	**5V/1.8V N/PMOS Regular I/O and 5V NMOS Vdd/Vss protection**	**1.8V NMOS Vdd/Vss protection**
RPO width on drain side (min.)	1.95	No
RPO to poly space	Overlap poly by 0.05	No
Dummy layer for DRC	ESD2DMY	
Illustration	**Fig.5b**	**Fig.5c**

ESD.19g	NMOS and PMOS of I/O buffer should have a non-salicide area on drain side, that is, RPO mask should block drain side of device (except contact region should keep silicided).		
ESD.21g	For regular I/O designed by 5V and 1.8V NMOS (see N1 in Fig.5a): RPO on the drain side needs to overlap poly gate by 0.05um. (see Fig.5b)		
ESD.22g	For all PMOS (see P1 in Fig.5a): RPO on the drain side needs to overlap poly gate by 0.05um. (see Fig. 5b)		
ESD.23g	For 5V power clamp devices, RPO on the drain side needs to overlap poly gate by 0.05um. (see Fig.5b)		
ESD.24g	The minimum width of RPO on drain side (X) for 5V and 1.8V NMOS and PMOS.		X ≥ 1.95 (in Fig.5b)
ESD.25g	The minimum clearance of poly edge to CO edge on source side for NMOS and PMOS		Z ≥ 0.5 (in Fig.5b)
ESD.26g	The minimum clearance of poly edge to CO edge on D/S side for 1.8V power clamp device		Y ≥ 0.25(in Fig.5c)

5.1.2 Additional Two ESD Structures

In this section, we keep supporting the two previous kinds of ESD structures (design rule before T-018-LO-DR-001 V2.7). However, it is recommended to use the updated structures (section 5.1.1) to simplify the ESD device structure.

5.1.2.1 Regular IO

Rule No.	Description		Layout Rule
ESD.29g	NMOS and PMOS of I/O buffer should have a non-salicide area on drain side, that is, RPO mask should block drain side of device (except contact region should keep silicided).		
ESD.30g	For regular 1.8V I/O in NMOS region (see N1 in Fig.5a): RPO to poly spacing is 0.45um. (see Fig.5d)		
ESD.31g	For 5V/1.8V PMOS (see P1 in Fig.5a):RPO to poly spacing is 0.45um. (see Fig.5d)		
ESD.32g	The minimum width of RPO on drain side (X) for 1.8V NMOS without ESD implant and 5V/1.8V PMOS. (see Fig.5d)		X≥ 1.5
ESD.33g	The minimum clearance of poly edge to CO edge on source side for NMOS and PMOS		Z ≥ 0.5 (in Fig.5d)
ESD.18g	Minimum gate length for I/O buffer.		Lg Table 3

Table 3 Lg for I/O buffer

	NMOS	PMOS	ESD IMP *
1.8V Device	0.25	0.25	
5V Device	0.6	0.6	0.9

5.1.2.2 5V Power Clamp (Ncs)

Rule No.	Description		Layout Rule
ESD.34g	For 5V power clamp devices (see Ncs in Fig.5a), the RPO can fully cover the uncontacted poly gate, source/drain (except contact region should keep silicided). (see)Fig.5e)		
ESD.35g	The minimum width of RPO on drain side (X) for 5V power clamp devices.		X ≥ 1.95 (in Fig.5e)
ESD.36g	The minimum clearance of poly edge to CO edge on source side for 5V power clamp devices.		Z ≥ 0.5 (in Fig.5e)
ESD.37g	For RPO DRC purpose, we still maintain a dummy layers in 5V power clamp. The layers should cover all ESD protection devices. **ESD1DMY** is for Vcc/Vss protection (see Fig.5e). By definition, it is adopted ***layer 136*** for **ESD1DMY**.		
ESD.18g	Minimum gate length for I/O buffer.		Lg Table 4

Table 4 Lg for I/O buffer

	NMOS	PMOS	ESD IMP *
5V Device	0.6	0.6	0.9

Tips for Power Bus

The ESD Protection design is not only for the input, output, or power pins; but also for the whole chip to avoid ESD damage to internal circuits. Especially in the mixed signal IC, separated digital and analog powers are used, so the interface devices between the digital and analog circuits are sensitive to ESD damage.

To prevent the problem, inter-power ESD protection circuits should be added according to the following suggestions to have better ESD immunity:

1. Using ESD clamping circuits to provide discharge paths between VDD and VSS under ESD stress.
2. Use low voltage transistor in ESD clamp for low voltage circuit protection; high voltage transistor for high voltage circuit protection.
3. Using ESD conduction circuits connecting separated power lines, as illustrated in Fig. 4.

For applications of ESD conduction circuits, below approach is recommended.

If there are too many power pairs, structure in Fig.4 is recommended. All power lines are connected through ESD conduction circuits to a Common VDD and VSS.

For VDD to VSS ESD clamping circuit, NMOS with gate soft-pulled to VSS is recommended.

The recommended application guidelines for ESD conduction circuit and ESD clamping circuit are:

1. At least 1 Clamping and/or Conduction cell inserted every 1000um of power line.

2. All the layout guidelines are the same as those for IO buffers. An additional guideline is the source side should be treated the same as drain side since ESD pulse can comes from either side.

3. The suggested width for the ESD clamping NMOS is 480um and length is the same as in Table 1.

4. The suggested layout for ESD conduction diodes is finger type with total area larger than 2500um^2, and periphery larger than 1100um. OD's and Contacts for both ends of the diode should be inter-digital layout to keep low series resistance and uniform current flow.

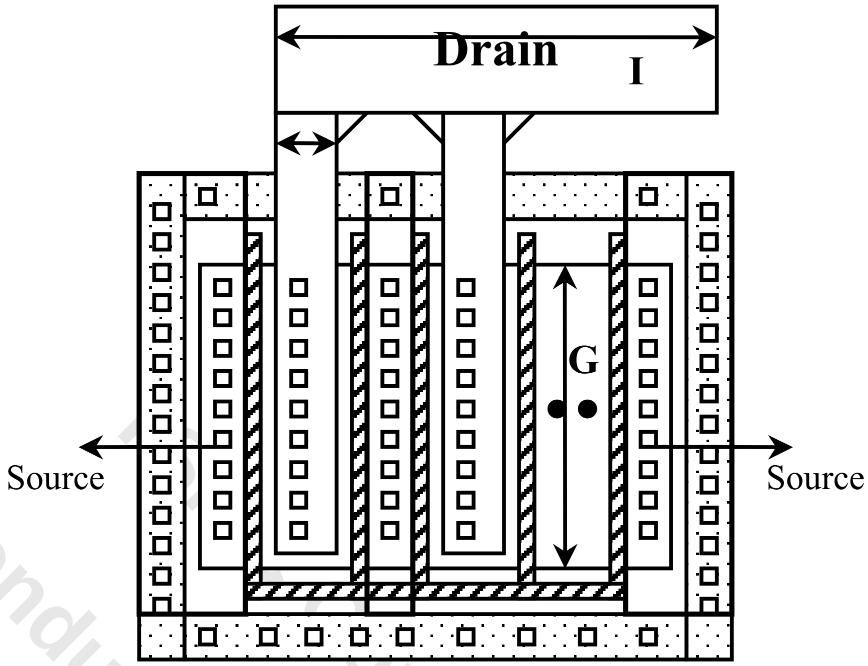


Fig 1 ESD cell layout

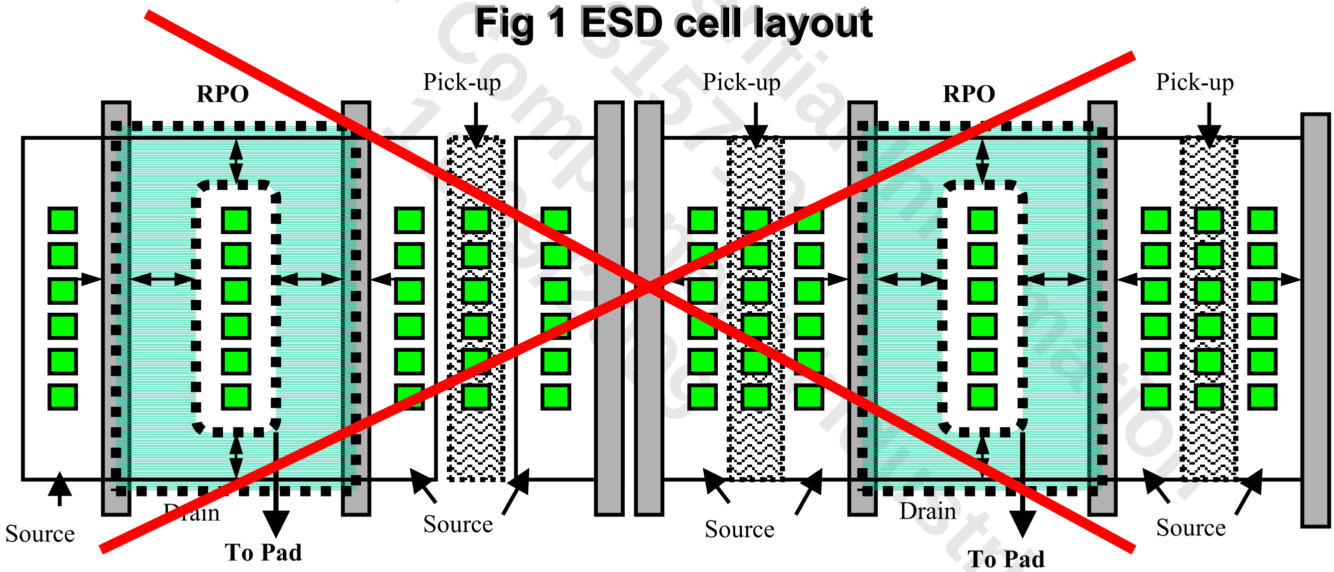


Fig 2. Butting or inserted pickup between source diffusion of ESD devices are prohibited.

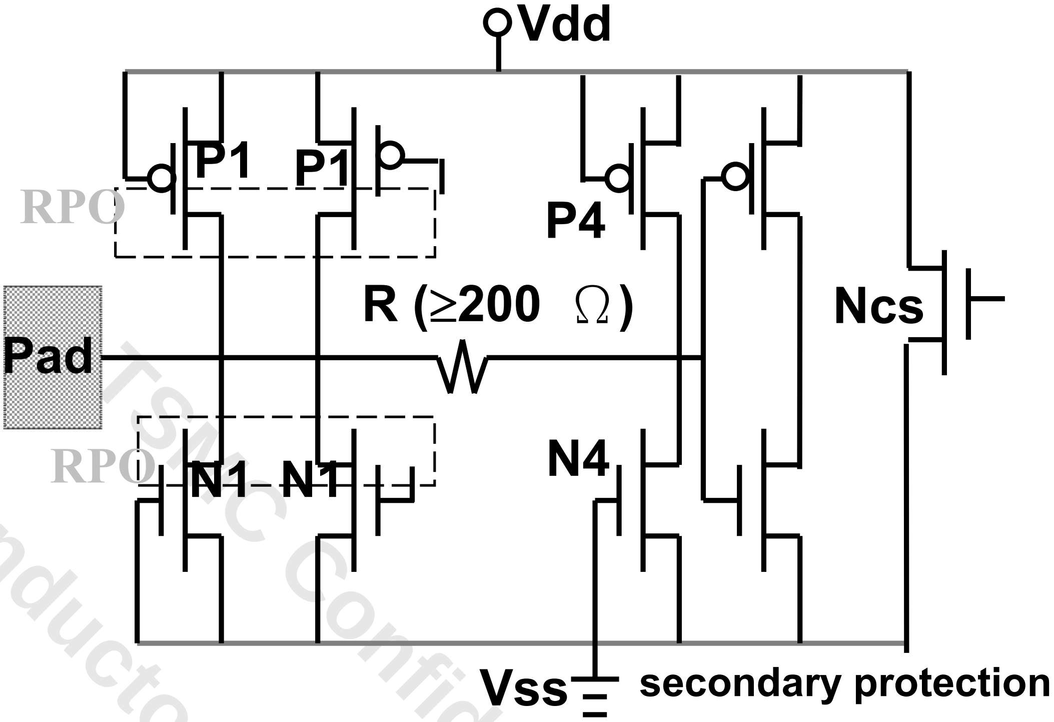


Fig 3. ESD protection circuit

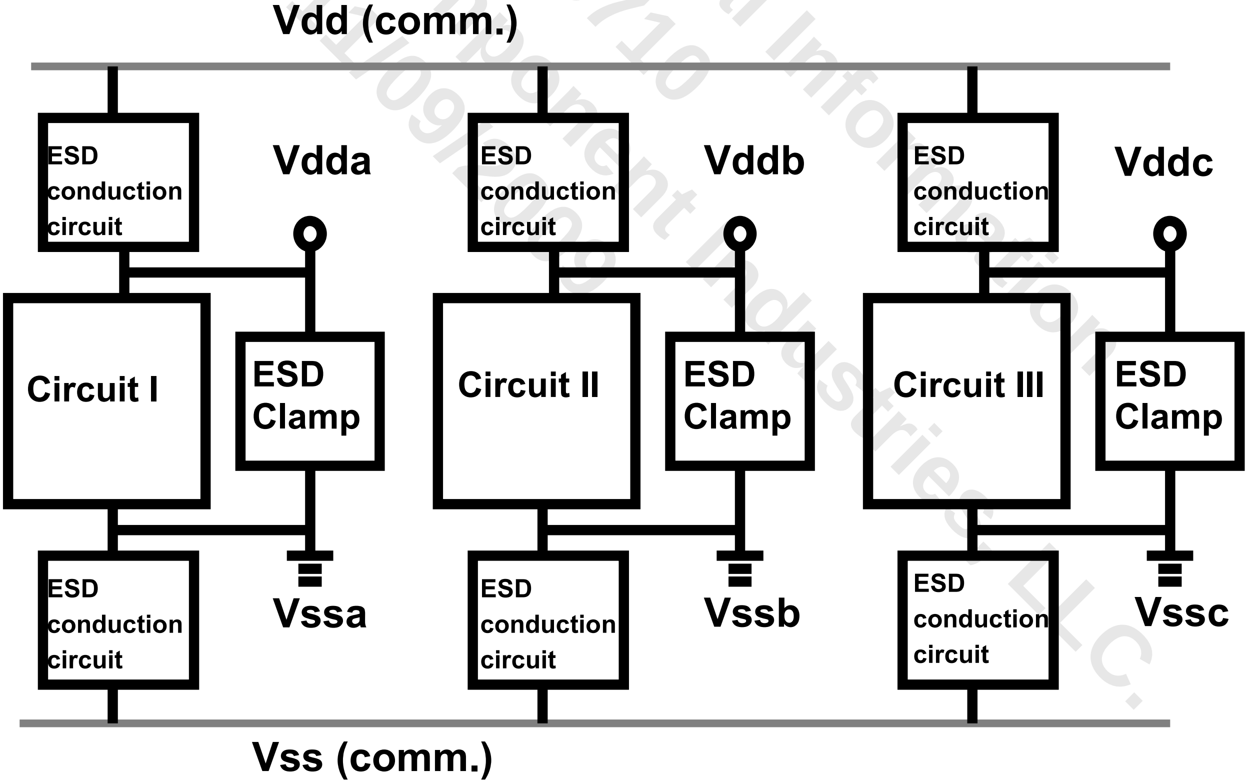
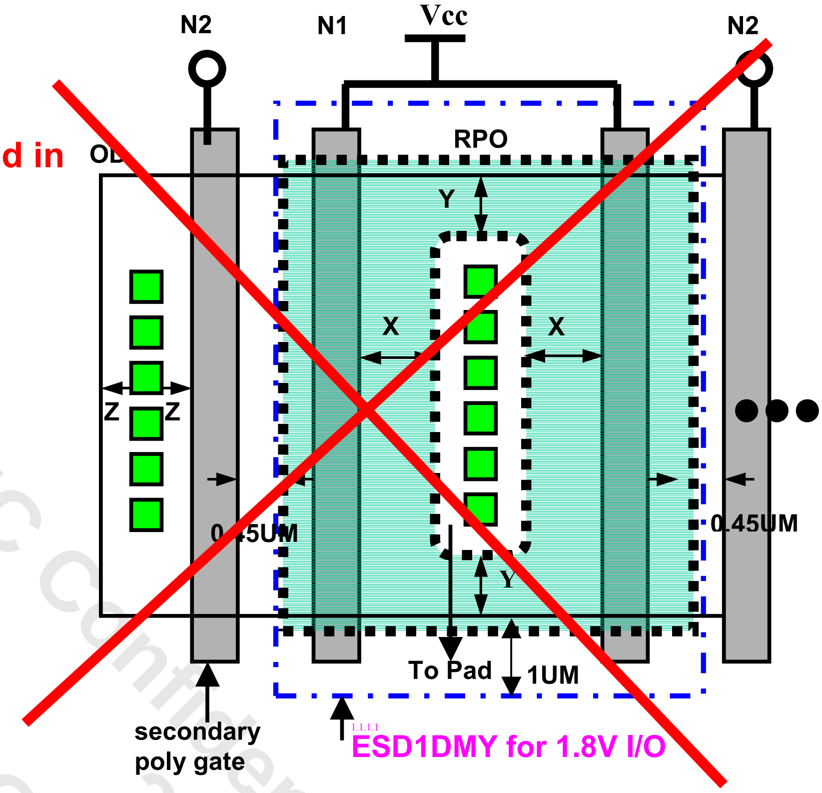
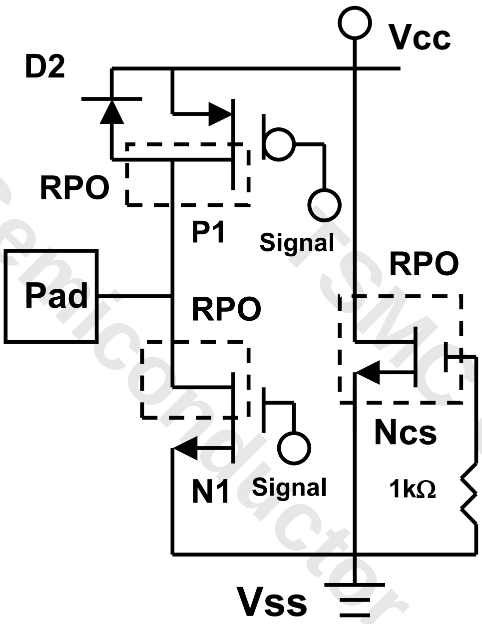


Fig 4. Schematic of a Multiple Power ESD Protection Design

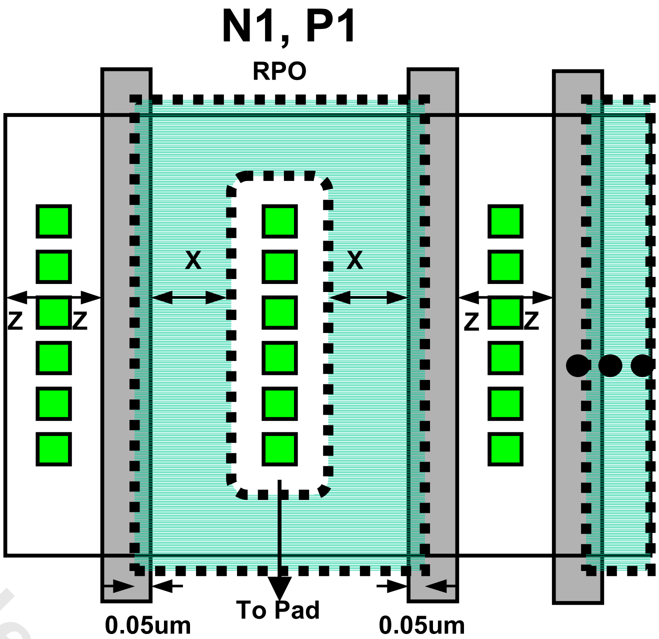
This layout is not supported in TSMC from design rule T-018-LO-DR-001 V2.7.



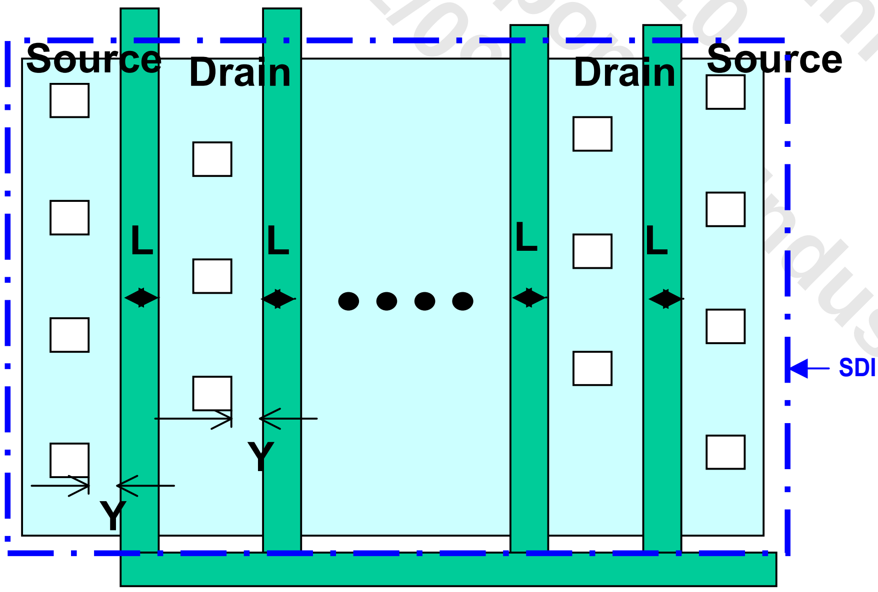
(a)


Vcc
D2
RPO
P1
Signal
RPO
Pad
RPO
Ncs
N1
Signal
1kΩ
Vss

(b)


N1, P1
RPO
X
X
Z
Z
Z
Z
0.05um
To Pad
0.05um

(c)


Source
Drain
Drain
Source
L
L
L
L
Y
Y
SDI

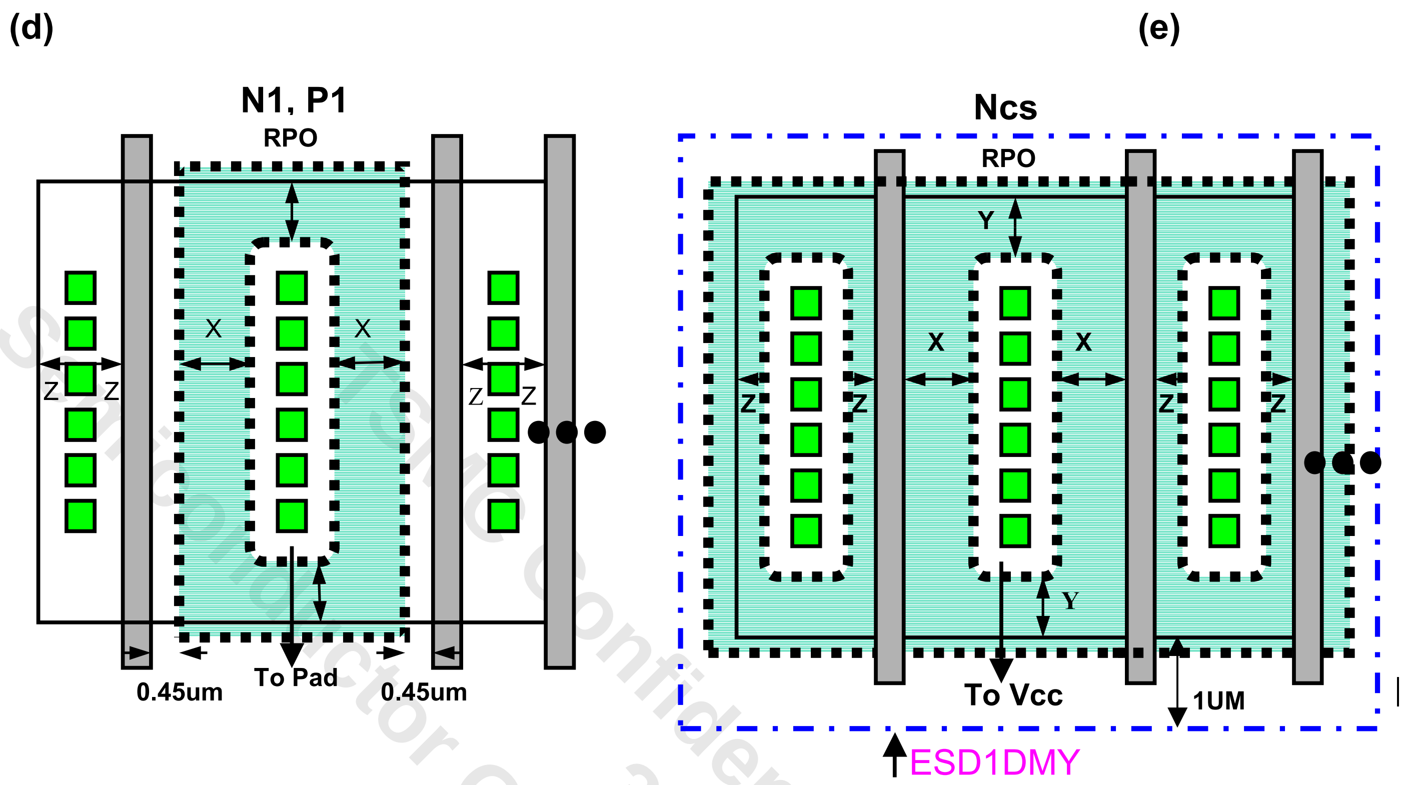
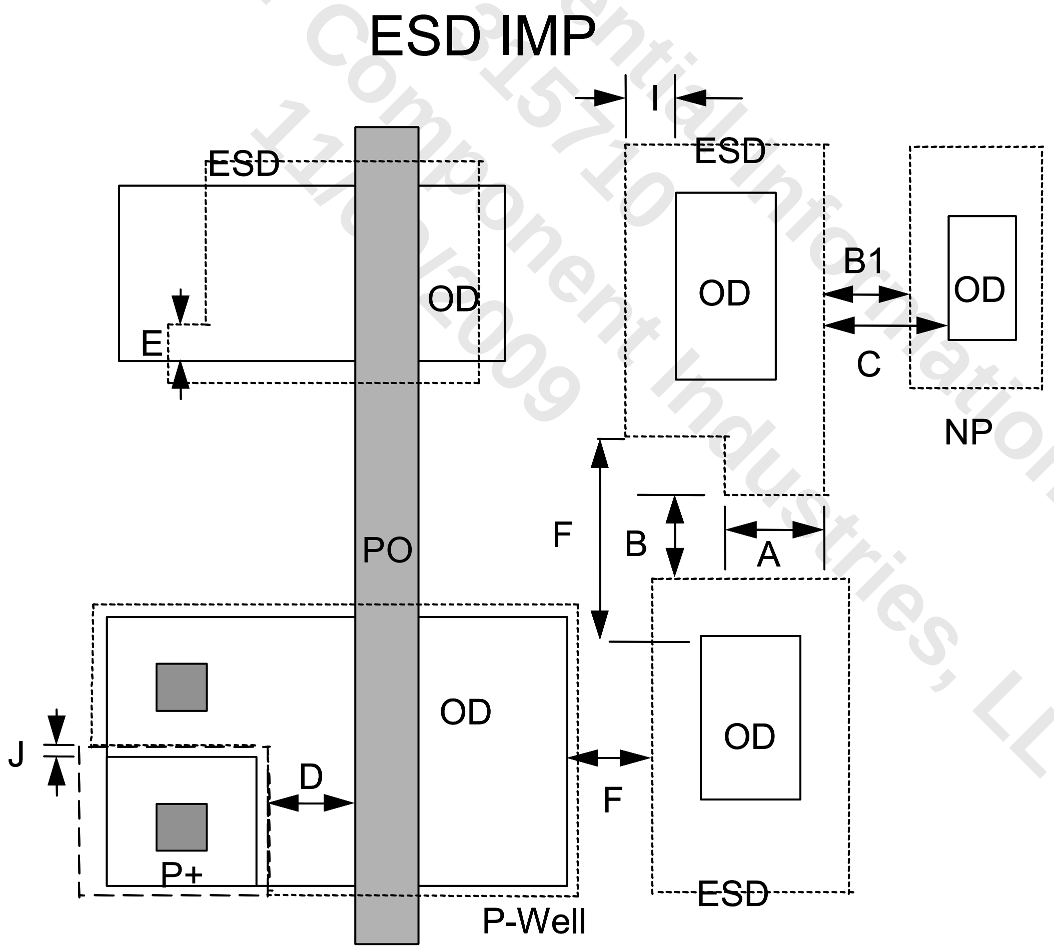


Fig 5. Schematic and the dimensions of ESD device

5.1.3 ESD Implantation Rule (Mask ID: 110)

This implantation layer is an optional layer to improve I/O ESD performance and it is only for 5V I/O NMOS transistors.

Rule No.	Description	Label		Layout Rule
ESD.W.1	Minimum width of an ESD implant region.	A	≧	0.6 um
ESD.S.1	Minimum space between two ESD implant region. Merge if the space is less than 0.6 um.	B	≧	0.6 um
ESD.S.2	Minimum space between ESD implant and NP or PP region.	B1	≧	0.3 um
ESD.C.1	Minimum clearance from an ESD implant region to an NP OD region	C	≧	0.6 um
ESD.C.2	Minimum clearance from an ESD implant region to a N-channel PO gate	D	≧	0.45 um
ESD.O.1	Minimum overlap from an ESD implant edge to an OD region	E	≧	0.45 um
ESD.C.4	Minimum clearance from an ESD implant region to an ESD OD region	F	≧	0.6 um
ESD.E.1	Minimum extension of an ESD implant region beyond an ESD implant OD region.	I	≧	0.25 um
ESD.C.5	Clearance of an ESD implant region over an OD with PP region to define CO with the same potential.	J	＝	0.0 um
ESD.R.1	Overlap of ESD implant and PP on the same Poly region is not allowed.			



5.2 Layout Rule and Guidelines for Latch-Up Prevention

5.2.1 Special Definition in Latch-up Prevention

Term	Definition
I/O pads	Do not include Vdd pad and Vss pad.
Internal circuit	Include NMOS, PMOS, de-coupling capacitors and varactor that do not connect to an IO pad.
Guard-ring	Complete un-broken ring-type OD and M1 with CO as many as possible, connected to Vdd or Vss.
N+ guard-ring	Complete un-broken ring-type (NP AND OD) and M1 with CO as many as possible, connected to Vdd.
P+ guard-ring	Complete un-broken ring-type (PP AND OD) and M1 with CO as many as possible, connected to Vss.
NMOS cluster	A group of NMOSs
PMOS cluster	A group of PMOSs

DRC uses the 2 following methods to recognize a MOS/ ACTIVE which connects to an I/O pad:

1) MOS/ ACTIVE in SDI
2) MOS/ ACTIVE connect to an I/O pad by connection from pad metal

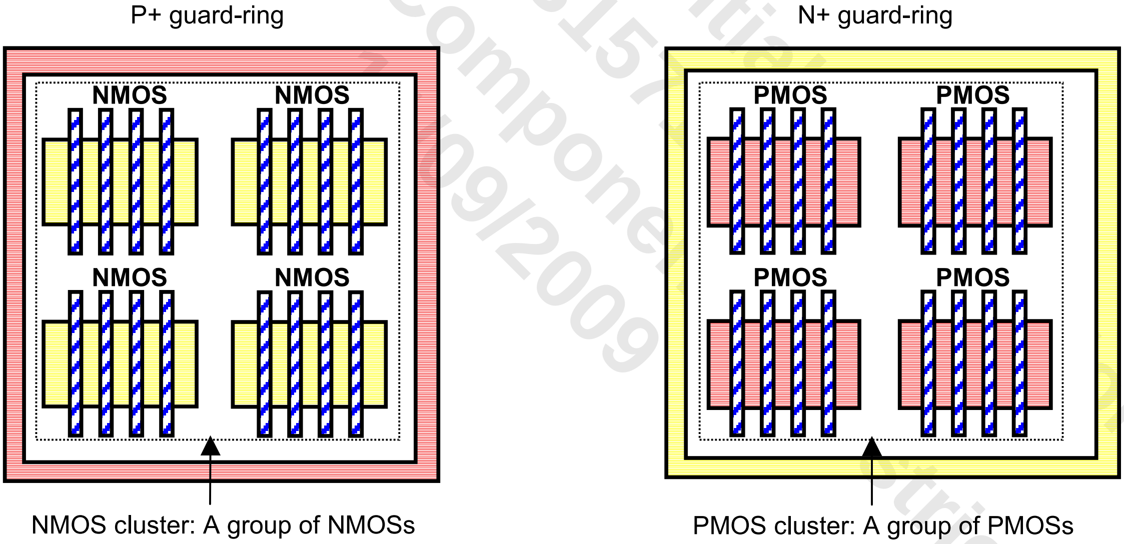


Fig. 5.2.1 Example of NMOS/PMOS cluster

5.2.2 Latch-up Dummy Layers Summary

5.2.2.1 SDI Dummy Layer

SDI (CAD layer: 58) is a DRC layer but not for mask making. It is required to cover all the OD regions of the ESD related circuits (Regular IO, high voltage tolerant I/O, Power Clamp), including MOS and diode, that are connected to the pads. SDI is not necessarily to cover and Well STRAP or ESD guard ring.

5.2.2.2 LUPWDMY Dummy Layer (CAD layer: 255;1)

LUPWDMY is a dummy layer to waive these guidelines, LUP.1g, LUP.2g, LUP.3.1g, LUP.3.2g, LUP.3.3g, LUP.3.4g, LUP.3.5g, LUP.4g, LUP.5.1g, LUP.5.2g, LUP.5.3g, LUP.5.4g, LUP.5.5g.

- Condition:
  - It is not recommended to use this layer before silicon is proven at the package.
  - Please consult TSCM if you would like to follow it as rules and have DRC violations before tapeout.
- Usage:
  - Draw LUPWDMY to fully cover MOS/ACTIVE OD/ Diode regions that are connected to I/O pads, including the source, gate, drain, and diode, but not necessarily to cover Well STRAP, guard-ring.
  - It is for DRC usage but not a tapeout required CAD layer.

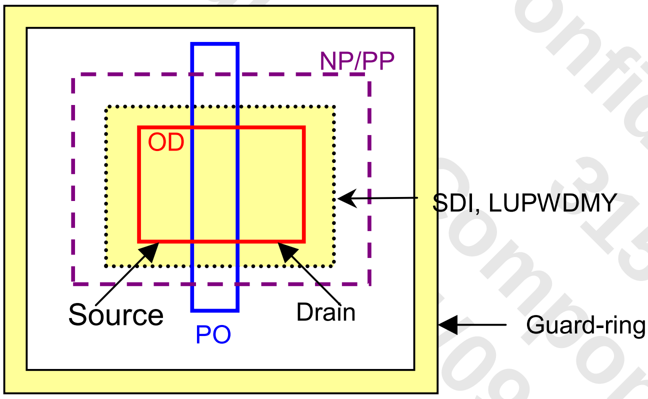
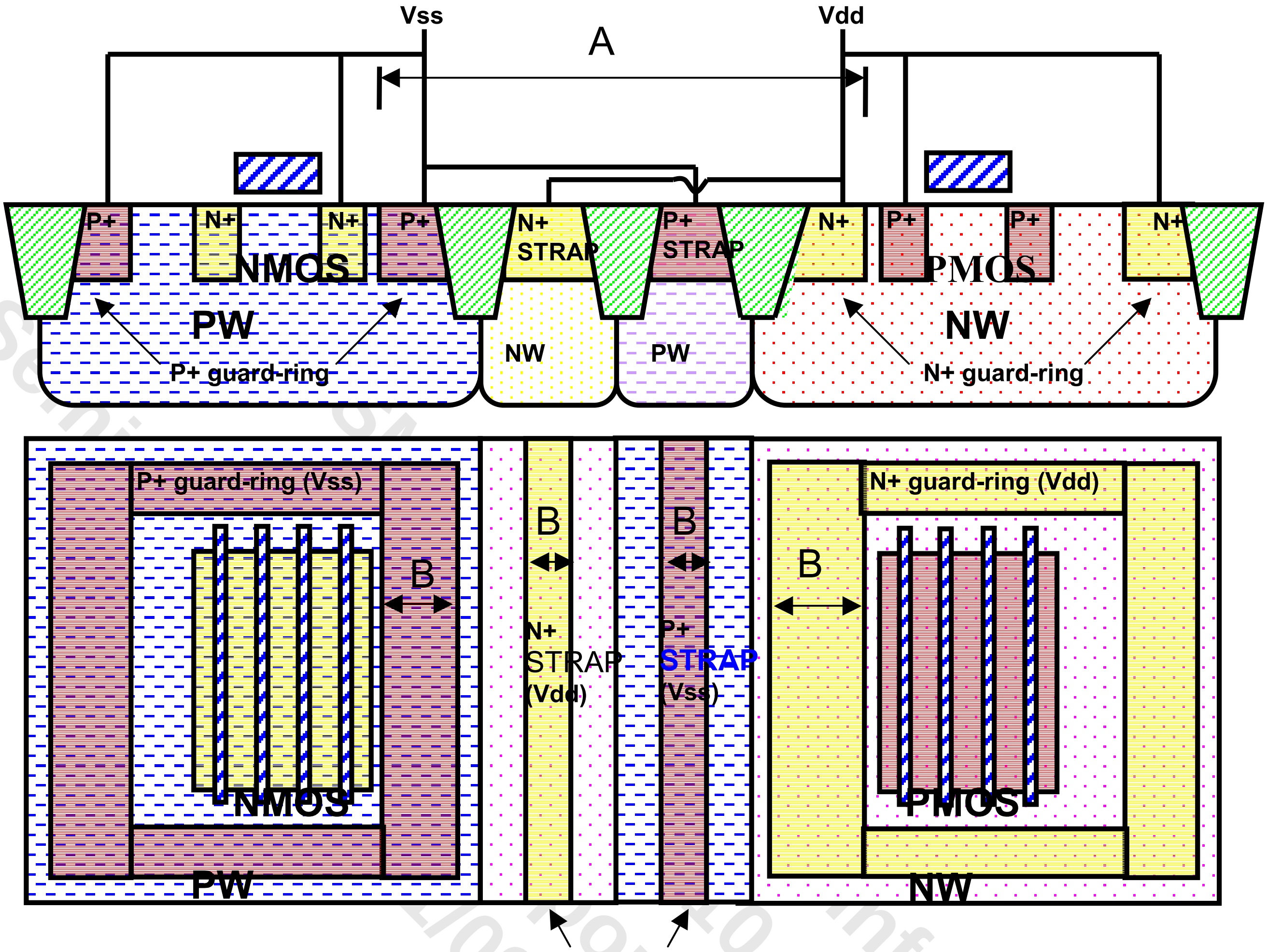


Fig. 5.2.2 Example of SDI/LUPWDMY.

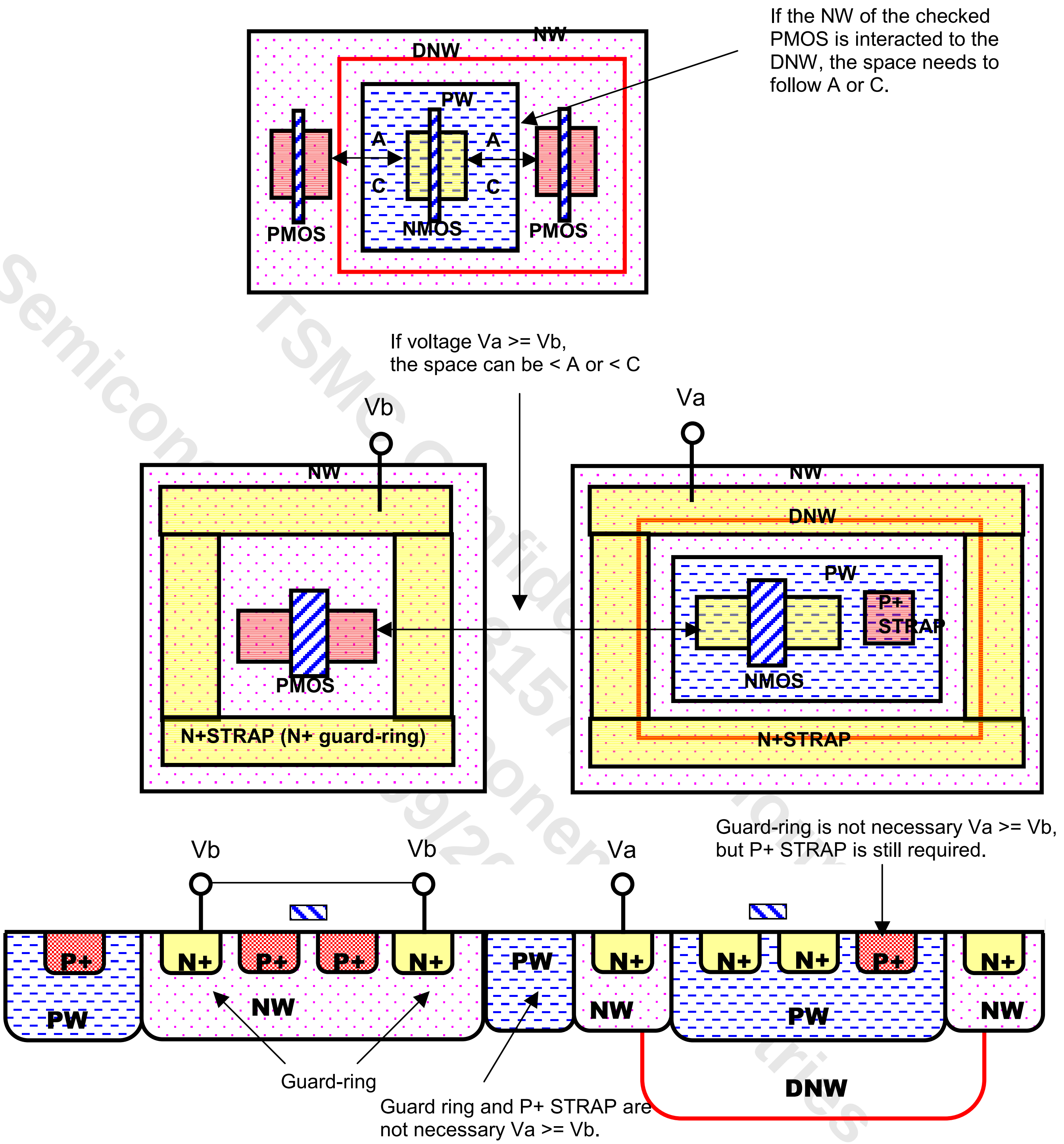
5.2.3 Layout Rules and Guidelines for Latch-up Prevention

Rule No.	Description	Label		Dimension
LUP.1g	Any N+ACTIVE or an N+ACTIVE cluster connected to an I/O pad must be surrounded by a P+ guard-ring. (Figure 5.2.3) Any P+ACTIVE or a P+ACTIVE cluster connected to an I/O pad must be surrounded by a N+ guard-ring. (Figure 5.2.3) Please also refer to LUP.9g for further information.			
LUP.2g	Within 20um space from the MOS connected to an I/O pad, a P+ guard-ring is required to surround an NMOS or an NMOS cluster. And an N+ guard-ring is required to surround a PMOS or a PMOS cluster. (Figure 5.2.5) DRC excludes the guard-ring of NMOS as the following conditions come into existence (Figure 5.2.4): 1) When the NMOS is enclosed by a DNW, and the NW of the checked PMOS [connected to an I/O pad and within 8um space from NMOS enclosed by a DNW] is not interacted to the DNW. 2) If the voltage (Va) of the NW INTERACT DNW is ≥ the voltage (Vb) of the NW of the checked PMOS. However, DRC can only waive same connection.			
	LUP.3.1, LUP.3.2, LUP.3.3, LUP.3.4, LUP.5.1, LUP.5.2, LUP.5.3, LUP.5.4, are exempted as the following conditions come into existence (Figure 5.2.4): 1) When the NMOS is enclosed by a DNW, and the NW of the checked PMOS is not interacted to the DNW. 2) If the voltage (Va) of the NW INTERACT DNW is ≥ the voltage (Vb) of the NW of the checked PMOS. However, DRC can only waive same connection.			
LUP.3.1g	For the 1.8V N/PMOS which connects to an I/O pad directly, (Figure 5.2.3) 1) space between the 1.8V NMOS and the 1.8V PMOS 2) space between the 1.8V PMOS and the 1.8V NMOS	A	≧	3
LUP.3.4g	For the 5V N/PMOS which connects to an I/O pad directly, (Figure 5.2.3) 1) space between the 5V NMOS and the 5V/1.8V PMOS 2) space between the 5V PMOS and the 5V/1.8V NMOS	A	≧	23
LUP. 4g	Width of the N+ guard-ring and P+ guard-ring for the ACTIVE connected to an I/O pad, and also MOS within 20um space from the MOS connected to an I/O pad. (e. g. width of guard-ring of LUP.1 and LUP.2)	B	≧	0.42
LUP.5.1g	For the internal circuits within 20um space from 1.8V MOS which connects to an I/O pad directly, 1) space between the 1.8V NMOS connected to an I/O pad and the PMOS in the internal circuit (Figure 5.2.5) 2) space between the 1.8V PMOS connected to the I/O pad and the NMOS in the internal circuit (Figure 5.2.5)	C	≧	3
LUP.5.4g	For the internal circuits within 40um space from 5V MOS which connects to an I/O pad directly, 1) space between the 5V NMOS connected to an I/O pad and the PMOS in the internal circuit (Figure 5.2.5) 2) space between the 5V PMOS connected to the I/O pad and the NMOS in the internal circuit (Figure 5.2.5)	C	≧	23
LUP.6	1) Any point inside NMOS source/drain {(N+ACTIVE INTERACT PO) NOT PO} space to the nearest PW STRAP in the same PW. (Figure 5.2.6) 2) Any point inside PMOS source/drain {(P+ACTIVE INTERACT PO) NOT PO} space to the nearest NW STRAP in the same NW. (Figure 5.2.6) In SRAM bit cell region, the rule is relaxed from 30um to 40um.	D	≦	30
LUP.7g^U	All the guard-rings and STRAPs should be connected to VDD/VSS with very low series resistance. Use as many contacts and vias as possible.			
LUP.8g^U	A P+ guard-ring should separate a large capacitor and MOS.			
LUP.9g^U	Additional one N+ STRAP and one P+ STRAP are required to be inserted between the P+ guard-ring and N+ guard-ring for LUP.1 (Figure 5.2.3). And the N+ STRAP should isolate the P+ STRAP and the P+ guard-ring. And the P+ STRAP should isolate the N+ STRAP and the N+ guard-ring. DRC cannot check the additional one N+ STRAP and one P+ STRAP.			



To exchange N+ STRAP and P+ STRAP not recommended (LUP.9g)

Figure 5.2.3



For LUP.2, LUP.3.1, LUP.3.2, LUP.3.3, LUP.3.4, LUP.5.1, LUP.5.2, LUP.5.3, LUP.5.4, if voltage Va >= Vb, it is excluded that the NMOS is enclosed by a DNW and the NW of the checked PMOS is not interacted to the DNW, however, DRC can only waive same connection.

Figure 5.2.4

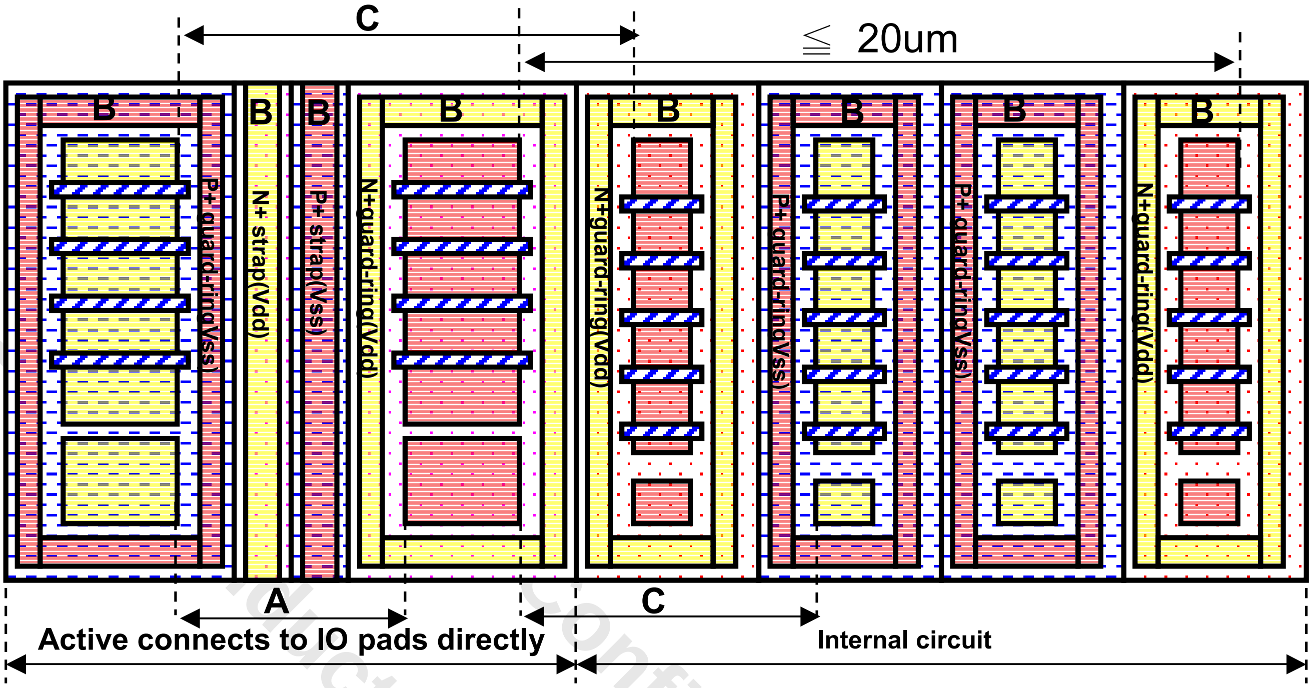


Figure 5.2.5

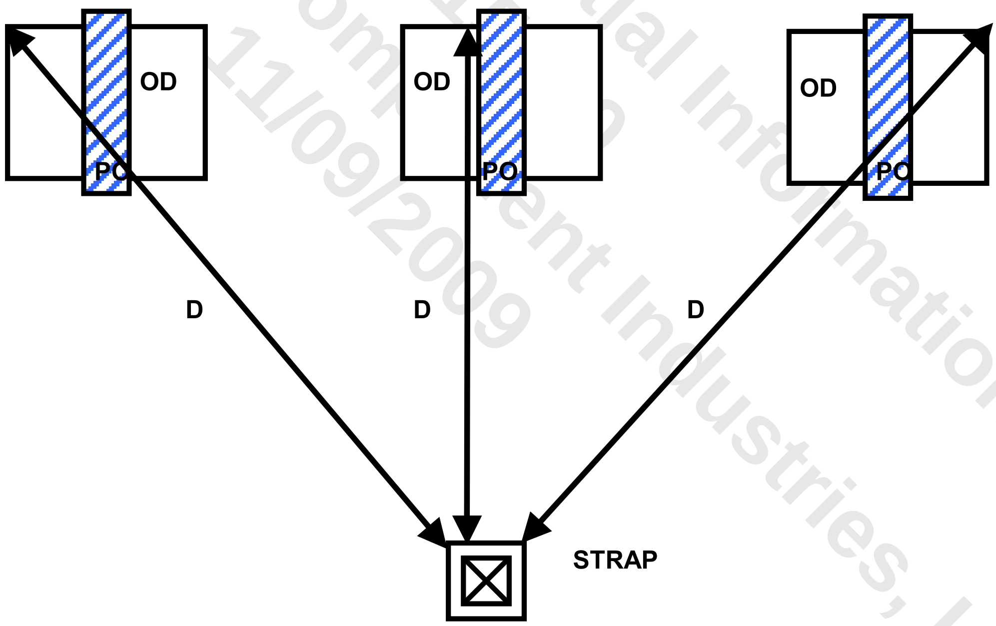


Figure 5.2.6

6 Electrical Parameter Summary

This chapter provides information about the following:

6.1 Available MOS Transistors

6.2 Key Parameters of MOS Transistors

6.3 Key Parameters for Bipolar

6.4 Key Parameters for Junction Diodes

6.5 Passive Device Models

6.6 Interconnect Models

6.7 MIM Capacitor Model

6.8 Inductor Model

The electrical parameters in this chapter are given for T=25℃, unless specified otherwise.

The electrical parameters in this chapter are depended on the following document and version. But, when you design your circuit, please MUST use the updated version.

Technology		Core/IO	Model description	Doc NO.	Version
CM018	G for MS	1.8/5V	0.18um Mixed Signal 1P6M General Purpose II SALICIDE 1.8V/5V	T-018-CM-SP-010	V1.0
		Inductor	0.18um RF 1P6M SALICIDE 1.8V/3.3V	T-018-MM-SP-001	V1.5

- MOS/Bipolar/Diode/Resistor/interconnect/MIM (sec 6.1~6.7) are the same as T-018-CM-SP-010 V1.0.
- Inductor model (sec 6.8) is the same as T-018-MM-SP-001 V1.5.

6.1 Available MOS Transistors

	Model Name		Electric_Tox (Å)		Minimum Length (μm)	
	NMOS	PMOS	NMOS	PMOS	NMOS	PMOS
1.80V_Standard_Vt_MOS	nch	pch	39.81	40.6	0.18	0.18
5.00V_5_MOS	nch_5	pch_5	127	128	0.6	0.5
1.8 V Medium Vt	mench	mepch	39.81	40.6	0.285	0.25
1.8 V Native	nanch	-	39.81	-	0.485	-
5 V Native	nanch5	-	127	-	1.6	-

6.2 Key Parameters of MOS Transistors

6.2.1 1.8V Standard Vt Device:

	W (µm)	L (µm)	Unit	NMOS		PMOS		Definition
ΔL (xl +/-dxl)			um	-0.015±0.0115		-0.015±0.0115		
ΔW(xw+/-dxw)			um	0±0.014		0±0.014		
Electrical_ Tox			Å	39.81±0.800		40.6±0.800		
Vt_gm	10	10	V	0.442		0.432		Vg @Vd=0.1V, Vs=Vb=0
				0.030	-0.030	0.031	-0.031	
	10	0.18		0.514		0.511		
				0.050	-0.050	0.059	-0.060	
	0.22	0.18		0.455		0.489		
				0.090	-0.090	0.090	-0.090	
Vt_lin	10	10	V	0.364		0.436		Vg @Vd=0.1V, Vs=Vb=0
				0.030	-0.030	0.030	-0.030	
	10	0.18		0.443		0.498		
				0.048	-0.043	0.060	-0.056	
	0.22	0.18		0.346		0.477		
				0.085	-0.078	0.084	-0.090	
Vt_sat	10	10	V	0.361		0.433		Vg @Vd=Vdd, Vs=Vb=0
	10	0.18		0.397		0.457		
	0.22	0.18		0.305		0.443		
DIBL	10	0.18	V	0.046585		-0.040769		Vb=0, Vt_lin-Vt_sat
Id_lin	10	0.18	uA/um	160.43		43.533		Id @Vg=Vdd, Vd=0.1V, Vs=Vb=0
	0.22	0.18		194.84		47.551		
Id_sat	10	0.18	uA/um	599.63		258.66		Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0
				-9.2%	10.2%	-13.2%	14.8%	
	0.22	0.18		762.26		280.97		
				-15.2%	18.0%	-16.9%	19.8%	
Ioff	10	0.18	pA/um	14.37		4.48		Id @Vg=0, Vd=1.1Vdd, Vs=Vb=0
				0.398	2.217	0.235	5.375	
Sub Vt slope	10	0.18	mV/dec	89.446		97.315		Slope @Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06
Body effect	10	0.18	V	0.185		0.260		ΔVt_sat @Vb=-Vdd/2 and Vb=0
Isub	10	0.18	nA/um	1.130E+01		3.018E-01		Ibmax @Vs=Vb=0, Vd=Vdd, sweep Vg
Covl	10	0.18	fF/um	3.04E-01		2.59E-01		Cgd @Vg=0, Vd=Vdd, Vs=Vb=0
Cj			fF/um2	0.982		1.11		Vrev=0V
Inverter FO=1 Delay	Wn/Wp= 4/6	0.18	ps/gate	26.69				RO_Td(ring oscillator delay time) @ V=Vdd (Fan_out=1)
				4.39		-3.80		

6.2.2 5V Standard Vt Device:

	W (µm)	L (µm)	Unit	NMOS		PMOS		Definition
ΔL (xl +/-dxl)			um	-0.03±0.0133		-0.03±0.0133		
ΔW(xw+/-dxw)			um	0.01±0.022		0.01±0.022		
Electrical_ Tox			Å	127±6.000		128±6.000		
Vt_gm	10	10	V	0.793		0.759		Vg @Vd=0.1V, Vs=Vb=0
				0.062	-0.062	0.060	-0.061	
	10	0.6/0.5		0.771		0.776		
				0.102	-0.102	0.086	-0.093	
	0.22	0.6/0.5		0.546		0.636		
				0.197	-0.200	0.189	-0.188	
Vt_lin	10	10	V	0.723		0.794		Vg @Vd=0.1V, Vs=Vb=0
				0.064	-0.064	0.066	-0.065	
	10	0.6/0.5		0.722		0.813		
				0.105	-0.105	0.101	-0.100	
	0.22	0.6/0.5		0.511		0.682		
				0.217	-0.217	0.206	-0.201	
Vt_sat	10	10	V	0.714		0.788		Vg @Vd=Vdd, Vs=Vb=0
	10	0.6/0.5		0.678		0.762		
	0.22	0.6/0.5		0.473		0.631		
DIBL	10	0.6/0.5	V	0.044		-0.051		Vb=0, Vt_lin-Vt_sat
Id_lin	10	0.6/0.5	uA/um	56.897		1.73E+01		Id @Vg=Vdd, Vd=0.1V, Vs=Vb=0
	0.22	0.6/0.5		60.502		1.88E+01		
Id_sat	10	0.6/0.5	uA/um	555.18		271		Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0
				-13.3%	13.4%	-12.8%	13.2%	
	0.22	0.6/0.5		678.28		295		
				-30.6%	31.3%	-31.0%	32.7%	
Ioff	10	0.6/0.5	pA/um	0.081053		3.55		Id @Vg=0, Vd=1.1Vdd, Vs=Vb=0
				0.582	3.937	0.662	1.736	
Sub Vt slope	10	0.6/0.5	mV/dec	1.07E+02		1.24E+02		Slope @Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06
Body effect	10	0.6/0.5	V	0.676		-0.881		ΔVt_sat @Vb=-Vdd/2 and Vb=0
Isub	10	0.6/0.5	nA/um	5.124E+03		1.184E+03		Ibmax @Vs=Vb=0, Vd=Vdd, sweep Vg
Covl	10	0.6/0.5	fF/um	2.35E-01		3.06E-01		Cgd @Vg=0, Vd=Vdd, Vs=Vb=0
Cj			fF/um2	1.14		1.49		Vrev=0V
Inverter FO=1 Delay	Wn/Wp= 4/6	0.6/0.5	ps/gate	63.63				RO_Td(ring oscillator delay time) @ V=Vdd (Fan_out=1)
				8.62		-6.71		

6.2.3 1.8V Median Vt Device:

<table>
<tr><th></th><th>W (µm)</th><th>L (µm)</th><th>Unit</th><th colspan="2">NMOS</th><th colspan="2">PMOS</th><th>Definition</th></tr>
<tr><td>ΔL (xl +/-dxl)</td><td></td><td></td><td>um</td><td colspan="2">-0.015±0.0115</td><td colspan="2">-0.015±0.0115</td><td></td></tr>
<tr><td>ΔW(xw+/-dxw)</td><td></td><td></td><td>um</td><td colspan="2">0±0.014</td><td colspan="2">0±0.014</td><td></td></tr>
<tr><td>Electrical_ Tox</td><td></td><td></td><td>Å</td><td colspan="2">39.81±0.800</td><td colspan="2">40.6±0.800</td><td></td></tr>
<tr><td rowspan="6">Vt_gm</td><td rowspan="2">10</td><td rowspan="2">10</td><td rowspan="6">V</td><td colspan="2">0.284</td><td colspan="2">0.144</td><td rowspan="6">Vg @Vd=0.1V, Vs=Vb=0</td></tr>
<tr><td>0.030</td><td>0.030</td><td>-0.031</td><td>0.030</td></tr>
<tr><td rowspan="2">10</td><td rowspan="2">0.3/0.25</td><td colspan="2">0.319</td><td colspan="2">0.262</td></tr>
<tr><td>0.050</td><td>0.060</td><td>-0.059</td><td>0.060</td></tr>
<tr><td rowspan="2">0.22</td><td rowspan="2">0.3/0.25</td><td colspan="2">0.300</td><td colspan="2">0.283</td></tr>
<tr><td>0.095</td><td>0.095</td><td>-0.095</td><td>0.095</td></tr>
<tr><td rowspan="6">Vt_lin</td><td rowspan="2">10</td><td rowspan="2">10</td><td rowspan="6">V</td><td colspan="2">0.231</td><td colspan="2">0.153</td><td rowspan="6">Vg @Vd=0.1V, Vs=Vb=0</td></tr>
<tr><td>0.031</td><td>0.029</td><td>-0.030</td><td>0.029</td></tr>
<tr><td rowspan="2">10</td><td rowspan="2">0.3/0.25</td><td colspan="2">0.266</td><td colspan="2">0.257</td></tr>
<tr><td>0.042</td><td>0.061</td><td>-0.053</td><td>0.061</td></tr>
<tr><td rowspan="2">0.22</td><td rowspan="2">0.3/0.25</td><td colspan="2">0.226</td><td colspan="2">0.280</td></tr>
<tr><td>0.099</td><td>0.092</td><td>-0.090</td><td>0.092</td></tr>
<tr><td rowspan="3">Vt_sat</td><td>10</td><td>10</td><td rowspan="3">V</td><td colspan="2">0.229</td><td colspan="2">0.140</td><td rowspan="3">Vg @Vd=Vdd, Vs=Vb=0</td></tr>
<tr><td>10</td><td>0.3/0.25</td><td colspan="2">0.239</td><td colspan="2">0.221</td></tr>
<tr><td>0.22</td><td>0.3/0.25</td><td colspan="2">0.200</td><td colspan="2">0.246</td></tr>
<tr><td>DIBL</td><td>10</td><td>0.3/0.25</td><td>V</td><td colspan="2">0.027</td><td colspan="2">-0.035</td><td>Vb=0, Vt_lin-Vt_sat</td></tr>
<tr><td rowspan="2">Id_lin</td><td>10</td><td>0.3/0.25</td><td rowspan="2">uA/um</td><td colspan="2">115.2</td><td colspan="2">37.435</td><td rowspan="2">Id @Vg=Vdd, Vd=0.1V, Vs=Vb=0</td></tr>
<tr><td>0.22</td><td>0.3/0.25</td><td colspan="2">122.1</td><td colspan="2">38.655</td></tr>
<tr><td rowspan="4">Id_sat</td><td rowspan="2">10</td><td rowspan="2">0.3/0.25</td><td rowspan="4">uA/um</td><td colspan="2">529.89</td><td colspan="2">275.9</td><td rowspan="4">Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0</td></tr>
<tr><td>-10.1%</td><td>-12.5%</td><td>15.0%</td><td>-12.5%</td></tr>
<tr><td rowspan="2">0.22</td><td rowspan="2">0.3/0.25</td><td colspan="2">602.02</td><td colspan="2">275.98</td></tr>
<tr><td>-17.0%</td><td>-17.7%</td><td>18.9%</td><td>-17.7%</td></tr>
<tr><td rowspan="2">Ioff</td><td rowspan="2">10</td><td rowspan="2">0.3/0.25</td><td rowspan="2">pA/um</td><td colspan="2">327.72</td><td colspan="2">959</td><td rowspan="2">Id @Vg=0, Vd=1.1Vdd, Vs=Vb=0</td></tr>
<tr><td>0.349</td><td>0.167</td><td>4.174</td><td>0.167</td></tr>
<tr><td>Sub Vt slope</td><td>10</td><td>0.3/0.25</td><td>mV/dec</td><td colspan="2">81.974</td><td colspan="2">90.298</td><td>Slope @Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06</td></tr>
<tr><td>Body effect</td><td>10</td><td>0.3/0.25</td><td>V</td><td colspan="2">0.168</td><td colspan="2">0.143</td><td>ΔVt_sat @Vb=-Vdd/2 and Vb=0</td></tr>
<tr><td>Isub</td><td>10</td><td>0.3/0.25</td><td>nA/um</td><td colspan="2">3.853E+01</td><td colspan="2">8.714E+00</td><td>Ibmax @Vs=Vb=0, Vd=Vdd, sweep Vg</td></tr>
<tr><td>Covl</td><td>10</td><td>0.3/0.25</td><td>fF/um</td><td colspan="2">3.82E-01</td><td colspan="2">2.65E-01</td><td>Cgd @Vg=0, Vd=Vdd, Vs=Vb=0</td></tr>
<tr><td>Cj</td><td></td><td></td><td>fF/um2</td><td colspan="2">0.914</td><td colspan="2">0.996</td><td>Vrev=0V</td></tr>
<tr><td rowspan="2">Inverter FO=1 Delay</td><td rowspan="2">Wn/Wp= 4/6</td><td rowspan="2">0.3/0.25</td><td rowspan="2">ps/gate</td><td colspan="4">31.1</td><td rowspan="2">RO_Td(ring oscillator delay time) @ V=Vdd (Fan_out=1)</td></tr>
<tr><td colspan="2">5.35</td><td colspan="2">-4.75</td></tr>
</table>

6.2.4 1.8V Native Vt Device:

	W (µm)	L (µm)	Unit	NMOS		Definition
ΔL (xl +/-dxl)			um	-0.015±0.0115		
ΔW(xw+/-dxw)			um	0±0.014		
Electrical_ Tox			Å	39.86±2.000		
Vt_gm	10	10	V	0.010		Vg @Vd=0.1V, Vs=Vb=0
				0.071	-0.070	
	10	0.5		0.100		
				0.078	-0.078	
	0.22	0.5		0.120		
				0.085	-0.087	
Vt_lin	10	10	V	-0.044		Vg @Vd=0.1V, Vs=Vb=0
				0.070	-0.070	
	10	0.5		0.040		
				0.080	-0.081	
	0.22	0.5		0.045		
				0.090	-0.090	
Vt_sat	10	10	V	-0.101		Vg @Vd=Vdd, Vs=Vb=0
	10	0.5		-0.040		
	0.22	0.5		-0.030		
DIBL	10	0.5	V	0.079659		Vb=0, Vt_lin-Vt_sat
Id_lin	10	0.5	uA/um	84.214		Id @Vg=Vdd, Vd=0.1V, Vs=Vb=0
	0.22	0.5		96.903		
Id_sat	10	0.5	uA/um	578.01		Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0
				-10.0%	10.0%	
	0.22	0.5		699.59		
				-18.0%	18.0%	
Ioff	10	0.5	pA/um	5.78e+5		Id @Vg=0, Vd=1.1Vdd, Vs=Vb=0
				0.117	6.138	
Sub Vt slope	10	0.5	mV/dec	79.684		Slope @Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06
Body effect	10	0.5	V	0.015		ΔVt_sat @Vb=-Vdd/2 and Vb=0
Isub	10	0.5	nA/um	37.951		Ibmax @Vs=Vb=0, Vd=Vdd, sweep Vg
Covl	10	0.5	fF/um	4.26E-01		Cgd @Vg=0, Vd=Vdd, Vs=Vb=0
Cj			fF/um2	0.982333		Vrev=0V

6.2.5 5V Native Vt Device:

	W (µm)	L (µm)	Unit	NMOS		Definition
ΔL (xl +/-dxl)			um	-0.03±0.0133		
ΔW(xw+/-dxw)			um	0.01±0.022		
Electrical_ Tox			Å	127±6.000		
Vt_gm	10	10	V	-0.138		Vg @Vd=0.1V, Vs=Vb=0
				0.060	-0.060	
	10	1.6		-0.192		
				0.068	-0.068	
	1.2	1.6		-0.119		
				0.078	-0.078	
Vt_lin	10	10	V	-0.161		Vg @Vd=0.1V, Vs=Vb=0
				0.062	-0.062	
	10	1.6		-0.219		
				0.071	-0.071	
	1.2	1.6		-0.150		
				0.082	-0.082	
Vt_sat	10	10	V	-0.170		Vg @Vd=Vdd, Vs=Vb=0
	10	1.6		-0.357		
	1.2	1.6		-0.194		
DIBL	10	1.6	V	0.138		Vb=0, Vt_lin-Vt_sat
Id_lin	10	1.6	uA/um	31.119		Id @Vg=Vdd, Vd=0.1V, Vs=Vb=0
	1.2	1.6		31.912		
Id_sat	10	1.6	uA/um	537.38		Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0
				-9.5%	9.5%	
	1.2	1.6		551.26		
				-18.3%	18.5%	
Ioff	10	1.6	pA/um	8.18E+06		Id @Vg=0, Vd=1.1Vdd, Vs=Vb=0
				0.627	1.484	
Sub Vt slope	10	1.6	mV/dec	7.65E+01		Slope @Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06
Body effect	10	1.6	V	0.097		ΔVt_sat @Vb=-Vdd/2 and Vb=0
Isub	10	1.6	nA/um	108.660		Ibmax @Vs=Vb=0, Vd=Vdd, sweep Vg
Covl	10	1.6	fF/um	3.61E-01		Cgd @Vg=0, Vd=Vdd, Vs=Vb=0
Cj			fF/um2	0.1274		Vrev=0V

6.3 Key Parameters for Bipolar

6.3.1 1.8V Bipolar Device (PNP and NPN):

Device	Parameter	TT	SS	FF
PNP10	Vbe	0.6385	0.6433	0.6358
	beta	2.6006	2.2171	2.9798
PNP5	Vbe	0.6428	0.6476	0.6400
	beta	2.6805	2.2799	3.0798
PNP2	Vbe	0.6306	0.6355	0.6278
	beta	2.6082	2.2245	2.9869

Vbe : VB=VC=0, IE=1uA*AREA
Beta : VB=VC=0, IE=1uA*AREA

Device	Parameter	TT	SS	FF
NPN10	Vbe	0.6221	0.6279	0.6186
	beta	10.7460	9.3735	11.9960
NPN5	Vbe	0.6182	0.6240	0.6147
	beta	10.8130	9.5019	11.9710
NPN2	Vbe	0.6099	0.6158	0.6063
	beta	10.4020	9.3751	11.2100

Vbe : VB=VC=0, IE=-1uA*AREA
Beta : VB=VC=0, IE=-1uA*AREA

6.3.2 5V Bipolar Device (PNP and NPN):

Device	Parameter	TT	SS	FF
PNP10_5	Vbe	0.6327	0.6391	0.6283
	beta	2.7529	2.3436	3.1600
PNP5_5	Vbe	0.6298	0.6363	0.6255
	beta	2.7075	2.3050	3.1078
PNP2_5	Vbe	0.6228	0.6292	0.6185
	beta	2.5827	2.1986	2.9648

Vbe : VB=VC=0, IE=1uA*AREA
Beta : VB=VC=0, IE=1uA*AREA

Device	Parameter	TT	SS	FF
NPN10_5	Vbe	0.6308	0.6379	0.6259
	beta	8.5104	7.2985	9.6911
NPN5_5	Vbe	0.6274	0.6346	0.6225
	beta	8.5287	7.3863	9.6103
NPN2_5	Vbe	0.6200	0.6273	0.6150
	beta	8.1973	7.2949	8.9833

Vbe : VB=VC=0, IE=-1uA*AREA
Beta : VB=VC=0, IE=-1uA*AREA

6.4 Key Parameters for Junction Diodes

Junction Diodes:

Device	Junction	CJ	CJSW	CJSWG	BV	N	RS	IS	ISW
		(F/m2)	(F/m)	(F/m)	V		ohm/m2	A/m2	A/m
1.8V Standard Vt	N+/PW	9.810E-04	1.19E-10	3.82E-10	11.25	1.06	1.00E-10	4.980E-07	4.12E-13
	P+/NW	1.120E-03	1.35E-10	4.36E-10	10.2	1.02	1.00E-10	1.760E-07	2.71E-13
	NW/Psub	1.338E-04	5.33E-10	NA	14.75	NA	NA	0.000E+00	9.75E-13
5V Standard Vt	N+/PW	1.140E-03	2.19E-10	2.49E-10	9.5	1.02	5.00E-09	4.000E-07	3.00E-12
	P+/NW	1.490E-03	2.11E-10	2.28E-10	8	1.02	5.00E-09	3.500E-07	7.00E-12
	NW/Psub	1.250E-04	4.90E-10	NA	14	1.02	5.00E-09	2.000E-06	4.00E-12
1.8V Median Vt	N+/PW	9.130E-04	1.04E-10	3.49E-10	11.3	1.005	1.00E-10	2.340E-07	7.68E-13
	P+/NW	1.050E-03	1.26E-10	3.50E-10	11.1	1.005	1.00E-10	1.480E-07	4.06E-13
DNW	DNWPSUB	1.393E-04	9.15E-10	NA	14.3	1.02	1.00E-10	1.900E-06	3.50E-12
	PWDNW	4.660E-04	3.07E-10	NA	15.1	1.02	1.00E-10	5.500E-07	2.00E-12
5V DNW	PWDNW	4.340E-04	3.36E-10	NA	14.5	1.02	1.00E-10	8.000E-07	2.000E-12

The area and perimeter components of junction capacitance listed in the table are at V=0 and T=25C.

- CJ = Area component of junction capacitance (F/m2).
- CJSW = STI perimeter component of junction capacitance (F/m).
- BV = Reverse-Biased Breakdown Voltage of STI-Bounded Junction (V).
- N, RS, IS, and ISW are forward bias related diode parameters.

6.5 Passive Device Models

6.5.1 Resistor Models

Several resistor models are included in this model release. The model naming and valid dimension ranges are reported in the Table 6-1. The model nominal temperature is 25 °C, while the valid temperature range is from –40 to 125 °C. All models contain one typical case (TT_RES) and two corner ones, slow (SS_RES) and fast (FF_RES) corners each.
Most resistors were measured by applying voltages on one node, while grounding the other node and substrate (if connection is available). The voltage sweep was performed from 0 up to +/- 4 V (provided there is no reliability issue). Most of resistance data measured were modeled with the following equation.

$$R(T,V) = R_0 \cdot (1 + TC1 \cdot \delta T + TC2 \cdot \delta T^2) \cdot (1 + VC1 \cdot \delta V + VC2 \cdot \delta V^2) \qquad (6\text{-}1)$$

where $T = T - 25$ (in °C), δV (in volt) is the voltage drop across the resistor, and L is the length of the resistor. R_0 is the resistance value at 25 °C and an infinitesimal voltage, which is related to sheet resistance, R_{sh}, by Eq. (6-2).

$$R_0 = R_{sh} \cdot L / (W - \delta W) \qquad (6\text{-}2)$$

where *W* and *L* are the layout drawn width and length. δW is the width offset.
The median sheet resistance values and their corresponding variations, temperature coefficients, and voltage coefficients extracted based on the methodology described above are reported in Table 6-1. Please note that NW diffusion resistor under STI is very subject to CMP variation. Users are recommended to use NW diffusion resistor under OD for their design. For further details, please refer to TSMC design rule manual.

Name	Structure	Type	TypeVal	Unit	dw	VC1	VC2	VC3	TC1	TC2
rnodrpo	N+OD w/o silicide resistor	Rsh	82.26	ohm/sq	-0.0977u	-2.99E-1	-7.64E-6	2.449	1.47E-3	5.25E-7
		Rend0	1.366E-5	ohm.m	0	1.89E-2	3.92	1.82E-1	7.691E-4	-1.678E-6
rpodrpo	P+OD w/o silicide resistor	Rsh	140.6	ohm/sq	-0.0785u	-6.968	-2.037E-7	2.1	1.383E-3	8.632E-7
		Rend0	2.95E-5	ohm.m	-	0.3	-3.6	1e-2	-1.55E-3	1.1e-6
rnpolyrpo	N+POLY w/o silicide resistor	Rsh	295.3	ohm/sq	0.071u	-1.17E-1	4.1E-6	-1.88	-1.506E-3	2.679E-6
		Rend0	4.3E-5	ohm.m	0	0.5	-9.5	1.432	-1.584E-3	-3.95E-7
rppolyrpo	P+POLY w/o silicide resistor	Rsh	321.8	ohm/sq	0.03u	-9.7E-3	5.5E-6	-1.3	-2.38E-4	8.85E-7
		Rend0	7.3E-5	ohm.m	-	-0.35	13.5	-2.5	-2.086E-3	1.175E-6
rppolyhri	P- POLY w/o silicide resistor	Rsh	1037	ohm/sq	0.0416u	-3.64E-2	4.5E-6	-1.85	-9.2E-4	1.75e-6
		Rend0	5.95E-5	ohm.m	-0.0019	-2.909E-1	-33.02	-8.339e-1	-7.7E-4	1.294E-7
rppoly	P+POLY silicide resistor (W>=2um)	Rsh	7.9	ohm/sq	-0.025u	-7.89E-4	6.19E-3	-	2.88E-3	5.01E-7
rppolyw	P+POLY silicide resistor (W<2um)	Rsh	7.9	ohm/sq	-0.025u	-7.89E-4	6.19E-3	-	2.88E-3	5.01E-7
rnpoly	N+POLY silicide resistor (W>=2um)	Rsh	7.89	ohm/sq	-0.057u	1.35E-3	7.15E-3	-	2.92E-3	2.66E-7
rnpolyw	N+POLY silicide resistor (W<2um)	Rsh	7.89	ohm/sq	-0.057u	1.35E-3	7.15E-3	-	2.92E-3	2.66E-7
rnod	N+OD silicide resistor (W>=2um)	Rsh	6.82	ohm/sq	-0.0765u	7.56E-5	1.24E-3	-	3.35E-3	4.31E-7
rnodw	N+OD silicide resistor (W<2um)	Rsh	6.82	ohm/sq	-0.0765u	7.56E-5	1.24E-3	-	3.35E-3	4.31E-7
rpod	P+OD silicide resistor (W>=2um)	Rsh	7.76	ohm/sq	-0.08u	-2.51E-4	1.03E-3	-	3.44E-3	5.02E-7
rpodw	P+OD silicide resistor (W<2um)	Rsh	7.76	ohm/sq	-0.08u	-2.51E-4	1.03E-3	-	3.44E-3	5.02E-7
rnwod	N-Well under OD resistor	Rsh	411.8	ohm/sq	0.141u	2.77E-3	2.49E-4	-	3.68E-3	9.54E-6
rnwsti	N-well under STI resistor	Rsh	927	ohm/sq	0.182u	8.06E-3	-3.32E-4	-	2.97E-3	1.10E-5
rm1	-	Rsh	0.078	ohm/sq	0.03u	0	0	-	3.43E-3	-1.08E-6
rm2	-	Rsh	0.078	ohm/sq	0.03u	0	0	-	3.43E-3	-1.08E-6
rm3	-	Rsh	0.078	ohm/sq	0.03u	0	0	-	3.43E-3	-1.08E-6
rm4	-	Rsh	0.078	ohm/sq	0.03u	0	0	-	3.43E-3	-1.08E-6
rm5	-	Rsh	0.078	ohm/sq	0.03u	0	0	-	3.43E-3	-1.08E-6
rm6	-	Rsh	0.036	ohm/sq	0.04u	0	0	-	3.60E-3	-1.16E-7
-	RC_N+		11	ohm/ct	0	0	0	-	1.31E-3	3.16E-7
-	RC_P+		10	ohm/ct	0	0	0	-	1.44E-3	1.46E-6
-	RC_PO(N+)		7.8	ohm/ct	0	0	0	-	1.53E-3	-5.7E-8
-	RC_PO(P+)		7.8	ohm/ct	0	0	0	-	1.44E-3	1.7E-7
-	RC_VIA1		6.4	ohm/ct	0	0	0	-	9.58E-4	-4.63E-7
-	RC_VIA2		6.4	ohm/ct	0	0	0	-	9.58E-4	-4.63E-7
-	RC_VIA3		6.4)	ohm/ct	0	0	0	-	9.58E-4	-4.63E-7
-	RC_VIA4		6.4	ohm/ct	0	0	0	-	9.58E-4	-4.63E-7
-	RC_VIA5		2.54	ohm/ct	0	0	0	-	4.94E-4	1.19E-6

Table 6-1: Resistor model table.

6.5.2 Resistor Models Resistor Models for Unsilicided N+/P+/P- Poly Resistors

Three types of unsilicided poly resistor models are available; N+ type, P+ type and the other is P-type. A cross-section schematic of the resistor structure is shown in Fig. 6-1. These resistors were measured by sweeping current on onenode, while grounding the other one. As suggested by TSMC's reliability team, these resistors might encounter a reliability issue if the current density applied is above 500 A/m width. Thus, the valid current density range for these models is between 0 and 500 A/m width. The corresponding voltage range can be obtained using the Ohm's law. TSMC further limits the application of these models only to resistors with width $\geq$ 1m and square number > 2. It is strongly recommended that all users should apply these models within valid current/voltage/dimension ranges. Application beyond the valid range will lead to a significant error. These resistors were modeled with the equivalent circuit shown in Fig. 6-2. In this circuit, the R_{end} component represents the contributions from the interface resistance (R_{int}, due to the depletion of dopant near the interface between revered protection oxide (RPO) and silicide) but do not include the contact resistance R_c, while the R_p component represents the primary contribution of the poly resistor.

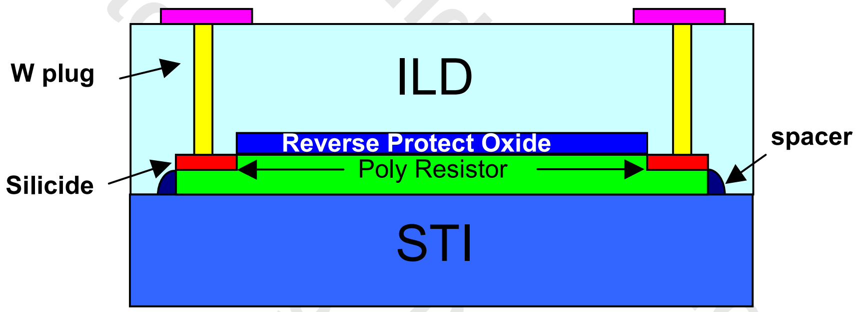


Fig. 6-1: Cross-section schematic of the unsilicided poly resistor.

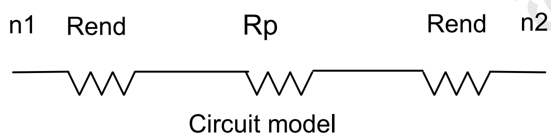


Fig. 6-2: Equivalent circuit used to model the unsilicided poly resistor.

As shown in the equivalent circuit, the total resistance (R) measured is equal to the sum of the R_p and two times of R_{end}, i.e.,

$$R = R_p + 2R_{end} \tag{6-3}$$

In contrast to other resistor models, the voltage dependence of R_p and R_{end} components were modeled with the equations containing hyperbolic-tangent terms.

$$R_{end} = R_{end0} / W \cdot (1 + tce1 \cdot \delta T + tce2 \cdot \delta T^2) \cdot \{1 + vce1 \cdot [\tanh(vce2 \cdot |\delta V_e| + vce3) - \tanh(vce3)]\} \tag{6-4}$$

$$R_p = R_{sh} \cdot (L - \delta L)/(W - \delta W) \cdot (1 + tcp1 \cdot \delta T + tcp2 \cdot \delta T^2) \cdot \{1 + vcp1 \cdot [\tanh(vcp2 \cdot |\delta V_p| / L + vcp3) - \tanh(vcp3)]\} \tag{6-5}$$

where $T = T - 25$ (in °C), δV_p and δV_e (in volt) are the voltage drops across R_p and R_{end} components, respectively. R_{end0} is the R_{end} resistance value at 25 °C and an infinitesimal voltage. δL is the length offset. The use of the empirical hyper-tangent equation, instead of the second order polynomial one, is to avoid the occurrence of zero or negative resistance during the simulation iteration. For temperature dependence modeling, the second order polynomial equation used by other resistor models is also employed here. Finally, the median sheet resistance values and their corresponding variations, R_{end0}, temperature coefficients, voltage coefficients extracted based on the methodology described above are reported in Table 6-2.

Name	Structure	Type	TypeVal	Unit	dw	VC1	VC2	VC3	TC1	TC2
rnodrpo	N+OD w/o silicide resistor	Rsh	82.26	ohm/sq	-0.0977u	-2.99E-1	-7.64E-6	2.449	1.47E-3	5.25E-7
		Rend0	1.366E-5	ohm.m	0	1.89E-2	3.92	1.82E-1	7.691E-4	-1.678E-6
rpodrpo	P+OD w/o silicide resistor	Rsh	140.6	ohm/sq	-0.0785u	-6.968	-2.037E-7	2.1	1.383E-3	8.632E-7
		Rend0	2.95E-5	ohm.m	-	0.3	-3.6	1e-2	-1.55E-3	1.1e-6
rnpolyrpo	N+POLY w/o silicide resistor	Rsh	295.3	ohm/sq	0.071u	-1.17E-1	4.1E-6	-1.88	-1.506E-3	2.679E-6
		Rend0	4.3E-5	ohm.m	0	0.5	-9.5	1.432	-1.584E-3	-3.95E-7
rppolyrpo	P+POLY w/o silicide resistor	Rsh	321.8	ohm/sq	0.03u	-9.7E-3	5.5E-6	-1.3	-2.38E-4	8.85E-7
		Rend0	7.3E-5	ohm.m	-	-0.35	13.5	-2.5	-2.086E-3	1.175E-6
rppolyhri	P- POLY w/o silicide resistor	Rsh	1037	ohm/sq	0.0416u	-3.64E-2	4.5E-6	-1.85	-9.2E-4	1.75e-6
		Rend0	5.95E-5	ohm.m	-0.0019	-2.909E-1	-33.02	-8.339e-1	-7.7E-4	1.294E-7
rppoly	P+POLY silicide resistor (W>=2um)	Rsh	7.9	ohm/sq	-0.025u	-7.89E-4	6.19E-3	-	2.88E-3	5.01E-7
rppolyw	P+POLY silicide resistor (W<2um)	Rsh	7.9	ohm/sq	-0.025u	-7.89E-4	6.19E-3	-	2.88E-3	5.01E-7
rnpoly	N+POLY silicide resistor (W>=2um)	Rsh	7.89	ohm/sq	-0.057u	1.35E-3	7.15E-3	-	2.92E-3	2.66E-7
rnpolyw	N+POLY silicide resistor (W<2um)	Rsh	7.89	ohm/sq	-0.057u	1.35E-3	7.15E-3	-	2.92E-3	2.66E-7
rnod	N+OD silicide resistor (W>=2um)	Rsh	6.82	ohm/sq	-0.0765u	7.56E-5	1.24E-3	-	3.35E-3	4.31E-7
rnodw	N+OD silicide resistor (W<2um)	Rsh	6.82	ohm/sq	-0.0765u	7.56E-5	1.24E-3	-	3.35E-3	4.31E-7
rpod	P+OD silicide resistor (W>=2um)	Rsh	7.76	ohm/sq	-0.08u	-2.51E-4	1.03E-3	-	3.44E-3	5.02E-7
rpodw	P+OD silicide resistor (W<2um)	Rsh	7.76	ohm/sq	-0.08u	-2.51E-4	1.03E-3	-	3.44E-3	5.02E-7
rnwod	N-Well under OD resistor	Rsh	411.8	ohm/sq	0.141u	2.77E-3	2.49E-4	-	3.68E-3	9.54E-6
rnwsti	N-well under STI resistor	Rsh	927	ohm/sq	0.182u	8.06E-3	-3.32E-4	-	2.97E-3	1.10E-5
rm1	-	Rsh	0.078	ohm/sq	0.03u	0	0	-	3.43E-3	-1.08E-6
rm2	-	Rsh	0.078	ohm/sq	0.03u	0	0	-	3.43E-3	-1.08E-6
rm3	-	Rsh	0.078	ohm/sq	0.03u	0	0	-	3.43E-3	-1.08E-6
rm4	-	Rsh	0.078	ohm/sq	0.03u	0	0	-	3.43E-3	-1.08E-6
rm5	-	Rsh	0.078	ohm/sq	0.03u	0	0	-	3.43E-3	-1.08E-6
rm6	-	Rsh	0.036	ohm/sq	0.04u	0	0	-	3.60E-3	-1.16E-7
-	RC_N+		11	ohm/ct	0	0	0	-	1.31E-3	3.16E-7
-	RC_P+		10	ohm/ct	0	0	0	-	1.44E-3	1.46E-6
-	RC_PO(N+)		7.8	ohm/ct	0	0	0	-	1.53E-3	-5.7E-8
-	RC_PO(P+)		7.8	ohm/ct	0	0	0	-	1.44E-3	1.7E-7
-	RC_VIA1		6.4	ohm/ct	0	0	0	-	9.58E-4	-4.63E-7
-	RC_VIA2		6.4	ohm/ct	0	0	0	-	9.58E-4	-4.63E-7
-	RC_VIA3		6.4)	ohm/ct	0	0	0	-	9.58E-4	-4.63E-7
-	RC_VIA4		6.4	ohm/ct	0	0	0	-	9.58E-4	-4.63E-7
-	RC_VIA5		2.54	ohm/ct	0	0	0	-	4.94E-4	1.19E-6

Table 6-2: Resistor model table.

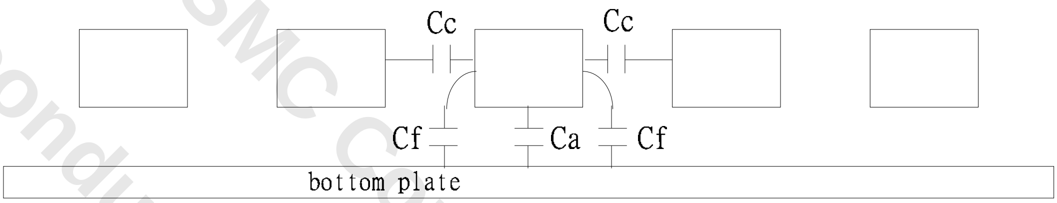
6.6 Interconnect Models

6.6.1 Interconnection line-line capacitance

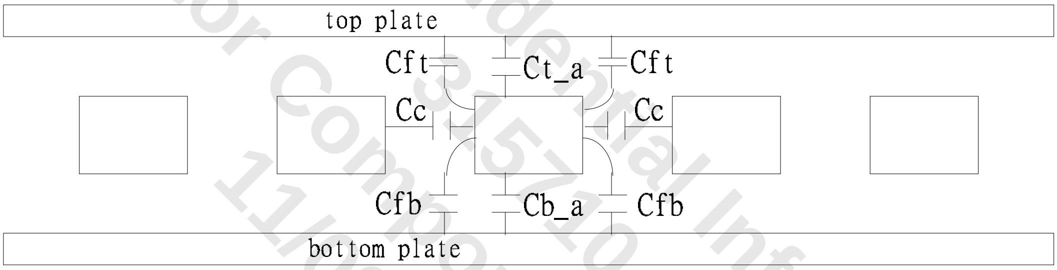
The interconnection line-line capacitance simulation results, using TMA RAPHAEL (v98.4) with five parallel lines above one plate and between two plates, are listed in this section.

The simulation structures are :

Structure A - Conductors array above the infinite plate :



Structure B - Conductors array between two infinite plates :



Note: The figures of structure A and structure B shown before here are schematic. The dielectric patterns between metals are quite complicated. For detail structures please refer to the cross section scheme in the next page.

1) The conduction line is using the min. width of design rule.

2) For structure A, the top layer is used as conduction line layer, and the bottom conduction layer is used as the infinite plate.
   For structure B, the middle layer is used as conduction line layer, and the top and bottom conduction layers are used as the infinite plates.

3) The dielectric thickness uses the "TYPICAL" dielectric thickness in order to take care of process variations rather than measurement thickness of previous data. Moreover, the technology information are listed below:

TECHNOLOGY PARAMETERS FOR TYPICAL CASE:

Conductor layers

Conductor	Thickness	Min. width	Min. space	Distance between conductor layer and substrate under FOX
PO1	2000	0.18μm(DOM)	0.25 μm(DOM)	3500
		0.16 μm(DOS)	0.27 μm(DOS)	
M1	5300	0.23μm	0.23μm	11000
M2	5300	0.28μm	0.28μm	24800
M3	5300	0.28μm	0.28μm	38600
M4	5300	0.28μm	0.28μm	52400
M5	5300	0.28μm	0.28μm	66200
M6	9900	0.44μm	0.46μm	81500

Dielectric layers

Dielectric	Thickness	%Var	Dielectric constant	Comments
FOX	3500	± 17.1%	3.9	See NOTE 4.
ILD	7500	± 21.4%	4.0	See NOTE 1.
IMD1a IMD1b	11800 2000	± 20% ± 3%	3.7 4.2	See NOTE 1.
IMD2a IMD2b	11800 2000	± 20% ± 3%	3.7 4.2	See NOTE 1.
IMD3a IMD3b	11800 2000	± 20% ± 3%	3.7 4.2	See NOTE 1.
IMD4a IMD4b	11800 2000	± 20% ± 3%	3.7 4.2	See NOTE 1.
IMD5a IMD5b	11800 3500	± 20% ± 3%	3.7 4.2	See NOTE 1.
PASS1	10000	± 10%	4.2	See NOTE 2.
PASS2	1500	± 10%	4.2	
PASS3	6000	± 10%	7.9	Conformal material.

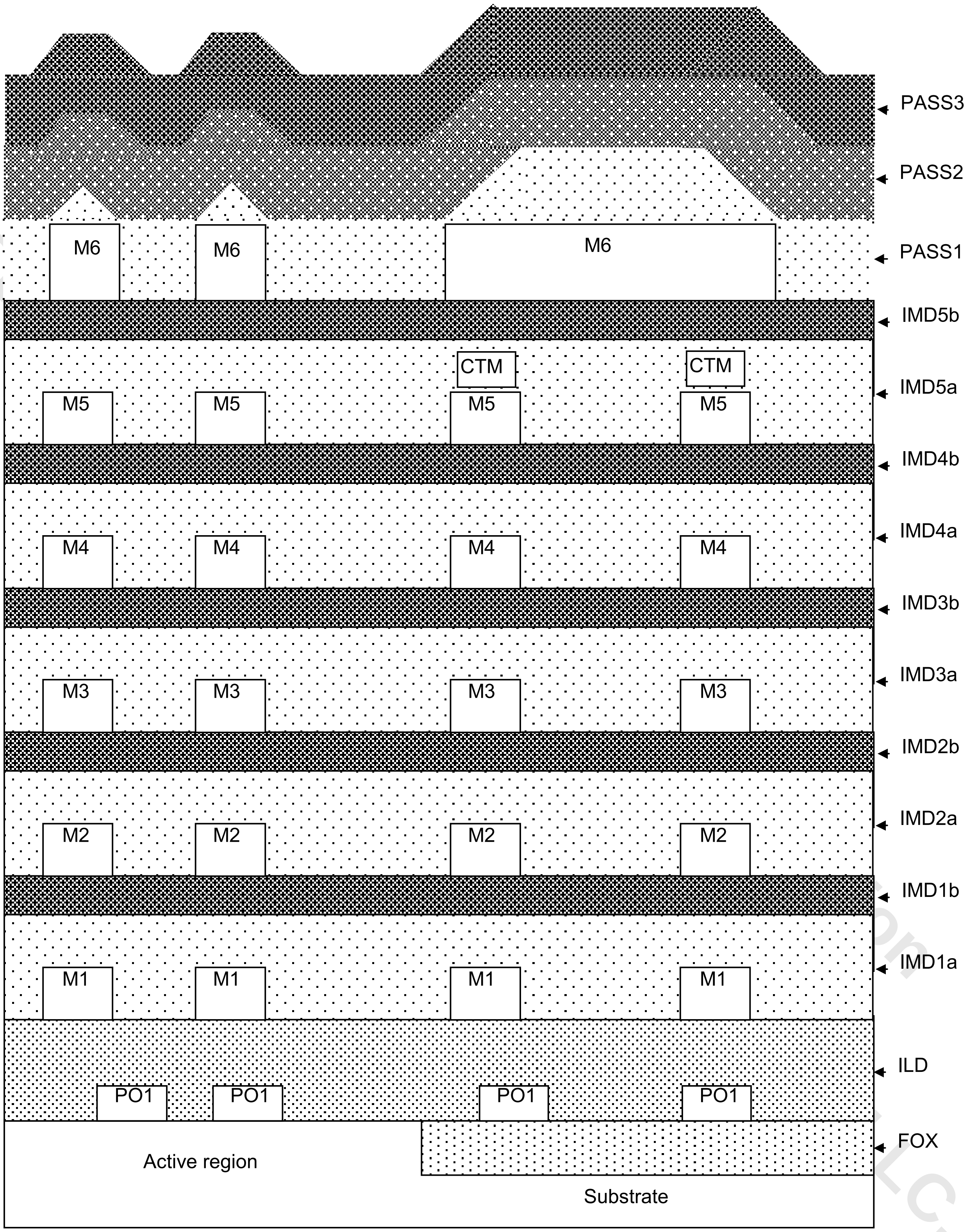
NOTE 1. The dielectric layers of ILD, IMD1b, IMD2b, IMD3b, IMD4b and IMD5b outside the metal are overetched 1000

NOTE 2. The dielectric layer of PASS1 is deposited using HDP approach, which results in facet formation and stationary fronts. The highest height above top metal with minimum width is 5000 ; however, the highest height above top metal with width larger than 2μm is 10000 .

NOTE 3. CTM is only used for the MIM capacitors, not allowed for used on interconnection.

NOTE 4. The thickness of FOX under PO1 is 500Å thicker than that under ILD.

Scheme of cross section of interconnection structure:



4) The method for calculating the max/min dielectric thickness are listed below :

Where $\triangle T_j$'s are the variations of interlayer dielectrics among metals, air, and substrate, and $\triangle \mathrm{total}$ is effective total variation between two layers. Then the min/max value is computed by subtracting or adding $\triangle \mathrm{total}$ from the mean value. The final dielectrics thickness are T_j''.

5) For structure A,
   Ctotal : total capacitance of the top center line
   Cc : line-to-line coupling capacitance of top center line to neighbor line
   Cbottom : Ca + 2 * Cf
   Ca : area capacitance of top layer to bottom layer
   [≡ (line_width) * (εox / dielectric_thickness)]
   Cf : fringe capacitance per side of top center line to infinite bottom plate
   Csum : Ca + 2 * Cf + 2 * Cc

   For structure B,
   Ctotal : total capacitance of the middle center line
   Cc : line-to-line coupling capacitance of middle center line to neighbor line
   Cbottom : Cb_area + 2 * Cfb
   Cb_area : area capacitance of middle layer to bottom layer
   [≡ (line_width) * (εox / dielectric_thickness)]
   Cfb : fringe capacitance per side of middle center line to infinite bottom plate
   Ctop : Ct_area + 2 * Cft
   Ct_area: area capacitance of middle layer to top layer
   [≡ (line_width) * (εox / dielectric_thickness)]
   Cft : fringe capacitance per side of middle center line to infinite top plate
   Csum : (Cb_area + 2 * Cfb) + (Ct_area + 2 * Cft) + 2 * Cc

6) The simulation results of the line-to-line capacitance and the fringe capacitance of min. line-width with various spacing for both structures A & B (**TYPICAL, WORST**, and **BEST** cases) are stored in a 3.5" floppy disk.

6.6.2 TYPICAL INTERCONNECT CAPACITANCE TABLE

*** Structure A ***										
Structure	(as drawn)		(after process bias)							
	width	space	width	space	Ctotal	Cc	Cbottom	Ca	Cf	Csum/Ctotal
	(um)	(um)	(um)	(um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	
PO1-FOX	0.18	0.25	0.16	0.27	1.44E-01	4.66E-02	4.10E-02	1.38E-02	1.36E-02	93.50%
	0.18	1.98	0.16	2	9.92E-02	4.32E-03	8.85E-02	1.38E-02	3.73E-02	97.90%

*** Structure A *** (continued)								
structure	width	space	Ctotal	Cc	Cbottom	Ca	Cf	Csum/Ctotal
	(um)	(um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	
M1-FOX	0.23	0.23	2.43E-01	1.05E-01	1.99E-02	7.35E-03	6.26E-03	94.20%
	0.23	2	9.10E-02	1.44E-02	5.66E-02	7.35E-03	2.46E-02	93.90%
M1-OD	0.23	0.23	2.46E-01	1.04E-01	2.66E-02	1.09E-02	7.89E-03	95.10%
	0.23	2	1.02E-01	1.19E-02	7.30E-02	1.09E-02	3.11E-02	95.10%
M1-PO1(FOX)	0.23	0.23	2.47E-01	1.01E-01	3.40E-02	1.48E-02	9.57E-03	95.70%
	0.23	2	1.12E-01	1.01E-02	8.69E-02	1.48E-02	3.61E-02	96.00%
M1-PO1(OD)	0.23	0.23	2.49E-01	1.02E-01	3.45E-02	1.50E-02	9.77E-03	95.70%
	0.23	2	1.13E-01	1.01E-02	8.83E-02	1.50E-02	3.67E-02	96.10%
M2-FOX	0.28	0.28	2.15E-01	9.28E-02	1.31E-02	3.85E-03	4.63E-03	92.20%
	0.28	2	8.06E-02	2.02E-02	3.19E-02	3.85E-03	1.40E-02	89.80%
M2-OD	0.28	0.28	2.18E-01	9.35E-02	1.43E-02	4.47E-03	4.93E-03	92.50%
	0.28	2	8.25E-02	1.96E-02	3.58E-02	4.47E-03	1.57E-02	90.80%
M2-PO1(FOX)	0.28	0.28	2.16E-01	9.24E-02	1.51E-02	4.92E-03	5.09E-03	92.60%
	0.28	2	8.30E-02	1.88E-02	3.82E-02	4.92E-03	1.67E-02	91.30%
M2-PO1(OD)	0.28	0.28	2.18E-01	9.33E-02	1.52E-02	4.94E-03	5.12E-03	92.70%
	0.28	2	8.37E-02	1.90E-02	3.85E-02	4.94E-03	1.68E-02	91.30%
M2-M1	0.28	0.28	2.19E-01	9.00E-02	2.70E-02	1.11E-02	7.96E-03	94.70%
	0.28	2	9.91E-02	1.33E-02	6.71E-02	1.11E-02	2.80E-02	94.60%
M3-FOX	0.28	0.28	2.15E-01	9.32E-02	1.02E-02	2.45E-03	3.88E-03	91.40%
	0.28	2	7.77E-02	2.23E-02	2.27E-02	2.45E-03	1.01E-02	86.70%
M3-OD	0.28	0.28	2.17E-01	9.40E-02	1.07E-02	2.69E-03	4.00E-03	91.60%
	0.28	2	7.87E-02	2.22E-02	2.44E-02	2.69E-03	1.08E-02	87.40%
M3-PO1(FOX)	0.28	0.28	2.15E-01	9.31E-02	1.10E-02	2.85E-03	4.08E-03	91.60%
	0.28	2	7.84E-02	2.17E-02	2.53E-02	2.85E-03	1.12E-02	87.70%

*** Structure A *** (continued)								
structure	width (um)	space (um)	Ctotal (fF/um)	Cc (fF/um)	Cbottom (fF/um)	Ca (fF/um)	Cf (fF/um)	Csum/Ctotal
M3-PO1(OD)	0.28	0.28	2.17E-01	9.40E-02	1.10E-02	2.85E-03	4.09E-03	91.70%
	0.28	2	7.90E-02	2.19E-02	2.54E-02	2.85E-03	1.13E-02	87.80%
M3-M1	0.28	0.28	2.15E-01	9.27E-02	1.37E-02	4.20E-03	4.74E-03	92.30%
	0.28	2	8.12E-02	1.97E-02	3.37E-02	4.20E-03	1.47E-02	90.10%
M3-M2	0.28	0.28	2.19E-01	9.00E-02	2.69E-02	1.11E-02	7.92E-03	94.70%
	0.28	2	9.90E-02	1.34E-02	6.68E-02	1.11E-02	2.78E-02	94.50%
M4-FOX	0.28	0.28	2.15E-01	9.34E-02	8.64E-03	1.80E-03	3.42E-03	90.90%
	0.28	2	7.66E-02	2.33E-02	1.79E-02	1.80E-03	8.04E-03	84.30%
M4-OD	0.28	0.28	2.17E-01	9.43E-02	8.94E-03	1.93E-03	3.51E-03	91.10%
	0.28	2	7.73E-02	2.34E-02	1.88E-02	1.93E-03	8.42E-03	84.80%
M4-PO1(FOX)	0.28	0.28	2.15E-01	9.33E-02	9.08E-03	2.00E-03	3.54E-03	91.10%
	0.28	2	7.69E-02	2.30E-02	1.93E-02	2.00E-03	8.63E-03	85.00%
M4-PO1(OD)	0.28	0.28	2.17E-01	9.43E-02	9.11E-03	2.01E-03	3.55E-03	91.10%
	0.28	2	7.74E-02	2.33E-02	1.93E-02	2.01E-03	8.65E-03	85.10%
M4-M1	0.28	0.28	2.15E-01	9.31E-02	1.03E-02	2.59E-03	3.87E-03	91.40%
	0.28	2	7.78E-02	2.22E-02	2.32E-02	2.59E-03	1.03E-02	86.80%
M4-M2	0.28	0.28	2.15E-01	9.26E-02	1.35E-02	4.20E-03	4.65E-03	92.30%
	0.28	2	8.11E-02	1.98E-02	3.33E-02	4.20E-03	1.45E-02	89.90%
M4-M3	0.28	0.28	2.19E-01	9.00E-02	2.67E-02	1.11E-02	7.81E-03	94.60%
	0.28	2	9.89E-02	1.35E-02	6.64E-02	1.11E-02	2.76E-02	94.40%
M5-FOX	0.28	0.28	2.15E-01	9.35E-02	7.59E-03	1.42E-03	3.08E-03	90.60%
	0.28	2	7.63E-02	2.41E-02	1.47E-02	1.42E-03	6.63E-03	82.50%
M5-OD	0.28	0.28	2.17E-01	9.44E-02	7.77E-03	1.50E-03	3.13E-03	90.70%
	0.28	2	7.69E-02	2.42E-02	1.52E-02	1.50E-03	6.87E-03	82.80%
M5-PO1(FOX)	0.28	0.28	2.15E-01	9.35E-02	7.88E-03	1.55E-03	3.17E-03	90.70%
	0.28	2	7.64E-02	2.39E-02	1.55E-02	1.55E-03	7.00E-03	83.00%
M5-PO1(OD)	0.28	0.28	2.17E-01	9.44E-02	7.88E-03	1.55E-03	3.17E-03	90.70%
	0.28	2	7.70E-02	2.42E-02	1.56E-02	1.55E-03	7.01E-03	83.00%
M5-M1	0.28	0.28	2.15E-01	9.33E-02	8.60E-03	1.87E-03	3.36E-03	90.90%
	0.28	2	7.69E-02	2.35E-02	1.78E-02	1.87E-03	7.95E-03	84.20%
M5-M2	0.28	0.28	2.15E-01	9.31E-02	1.01E-02	2.59E-03	3.77E-03	91.30%
	0.28	2	7.80E-02	2.24E-02	2.25E-02	2.59E-03	9.95E-03	86.30%
M5-M3	0.28	0.28	2.15E-01	9.26E-02	1.33E-02	4.20E-03	4.56E-03	92.20%
	0.28	2	8.13E-02	2.01E-02	3.26E-02	4.20E-03	1.42E-02	89.50%

*** Structure A *** (continued)								
structure	width	space	Ctotal	Cc	Cbottom	Ca	Cf	Csum/Ctotal
	(um)	(um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	
M5-M4	0.28	0.28	2.18E-01	9.00E-02	2.66E-02	1.11E-02	7.74E-03	94.50%
	0.28	2	9.91E-02	1.37E-02	6.57E-02	1.11E-02	2.73E-02	94.00%
M6-FOX	0.44	0.46	2.58E-01	1.15E-01	6.46E-03	1.82E-03	2.32E-03	92.00%
	0.44	2	1.04E-01	4.04E-02	1.21E-02	1.82E-03	5.12E-03	89.00%
M6-OD	0.44	0.46	2.58E-01	1.15E-01	6.62E-03	1.89E-03	2.36E-03	92.10%
	0.44	2	1.04E-01	4.03E-02	1.24E-02	1.89E-03	5.27E-03	89.20%
M6-PO1(FOX)	0.44	0.46	2.58E-01	1.15E-01	6.71E-03	1.94E-03	2.39E-03	92.10%
	0.44	2	1.04E-01	4.03E-02	1.27E-02	1.94E-03	5.36E-03	89.30%
M6-PO1(OD)	0.44	0.46	2.58E-01	1.15E-01	6.72E-03	1.94E-03	2.39E-03	92.10%
	0.44	2	1.04E-01	4.03E-02	1.27E-02	1.94E-03	5.36E-03	89.30%
M6-M1	0.44	0.46	2.58E-01	1.15E-01	7.33E-03	2.26E-03	2.54E-03	92.30%
	0.44	2	1.05E-01	4.00E-02	1.41E-02	2.26E-03	5.92E-03	89.90%
M6-M2	0.44	0.46	2.58E-01	1.15E-01	8.50E-03	2.87E-03	2.82E-03	92.60%
	0.44	2	1.05E-01	3.94E-02	1.70E-02	2.87E-03	7.04E-03	91.00%
M6-M3	0.44	0.46	2.58E-01	1.15E-01	1.05E-02	3.93E-03	3.27E-03	93.10%
	0.44	2	1.07E-01	3.83E-02	2.19E-02	3.93E-03	8.97E-03	92.40%
M6-M4	0.44	0.46	2.59E-01	1.14E-01	1.48E-02	6.23E-03	4.28E-03	93.90%
	0.44	2	1.10E-01	3.58E-02	3.23E-02	6.23E-03	1.30E-02	94.20%
M6-M5	0.44	0.46	2.64E-01	1.10E-01	3.18E-02	1.50E-02	8.37E-03	95.60%
	0.44	2	1.29E-01	2.89E-02	6.63E-02	1.50E-02	2.56E-02	96.10%

*** Structure B ***													
Structure	(as drawn)		(after process bias)										
	width (um)	space (um)	width (um)	space (um)	Ctotal (fF/um)	Cc (fF/um)	Cbottom (fF/um)	Cb_area (fF/um)	Cfb (fF/um)	Ctop (fF/um)	Ct_area (fF/um)	Cft (fF/um)	Csum/ Ctotal
M1-PO1-FOX	0.18	0.25	0.16	0.27	1.48E-01	4.23E-02	3.46E-02	1.38E-02	1.04E-02	2.62E-02	1.03E-02	7.95E-03	98.10%
	0.18	1.98	0.16	2	1.16E-01	4.39E-04	6.48E-02	1.38E-02	2.55E-02	5.04E-02	1.03E-02	2.00E-02	100.00%
M2-PO1-FOX	0.18	0.25	0.16	0.27	1.44E-01	4.58E-02	3.64E-02	1.38E-02	1.13E-02	7.89E-03	2.81E-03	2.54E-03	94.70%
	0.18	1.98	0.16	2	1.02E-01	2.52E-03	7.81E-02	1.38E-02	3.21E-02	1.82E-02	2.81E-03	7.70E-03	99.80%
M3-PO1-FOX	0.18	0.25	0.16	0.27	1.43E-01	4.61E-02	3.77E-02	1.38E-02	1.19E-02	4.81E-03	1.63E-03	1.59E-03	94.00%
	0.18	1.98	0.16	2	1.00E-01	3.45E-03	8.12E-02	1.38E-02	3.37E-02	1.12E-02	1.63E-03	4.76E-03	99.20%
M4-PO1-FOX	0.18	0.25	0.16	0.27	1.43E-01	4.62E-02	3.84E-02	1.38E-02	1.23E-02	3.48E-03	1.15E-03	1.17E-03	93.80%
	0.18	1.98	0.16	2	9.96E-02	3.85E-03	8.27E-02	1.38E-02	3.44E-02	8.04E-03	1.15E-03	3.45E-03	98.80%
M5-PO1-FOX	0.18	0.25	0.16	0.27	1.43E-01	4.63E-02	3.90E-02	1.38E-02	1.26E-02	2.74E-03	8.83E-04	9.27E-04	93.70%
	0.18	1.98	0.16	2	9.94E-02	4.03E-03	8.35E-02	1.38E-02	3.49E-02	6.29E-03	8.83E-04	2.71E-03	98.50%
M6-PO1-FOX	0.18	0.25	0.16	0.27	1.43E-01	4.63E-02	3.93E-02	1.38E-02	1.28E-02	2.22E-03	7.06E-04	7.56E-04	93.60%
	0.18	1.98	0.16	2	9.93E-02	4.14E-03	8.42E-02	1.38E-02	3.52E-02	5.08E-03	7.06E-04	2.19E-03	98.20%

*** Structure B *** (continued)											
Structure	width (um)	space (um)	Ctotal (fF/um)	Cc (fF/um)	Cbottom (fF/um)	Cb_area (fF/um)	Cfb (fF/um)	Ctop (fF/um)	Ct_area (fF/um)	Cft (fF/um)	Csum/ Ctotal
M2-M1-FOX	0.23	0.23	2.45E-01	1.02E-01	1.49E-02	7.35E-03	3.78E-03	1.83E-02	9.12E-03	4.61E-03	96.80%
	0.23	2	1.10E-01	5.93E-03	4.45E-02	7.35E-03	1.86E-02	5.34E-02	9.12E-03	2.22E-02	99.90%
M2-M1-OD	0.23	0.23	2.47E-01	1.01E-01	2.14E-02	1.09E-02	5.27E-03	1.82E-02	9.12E-03	4.53E-03	97.50%
	0.23	2	1.19E-01	4.25E-03	5.89E-02	1.09E-02	2.40E-02	5.12E-02	9.12E-03	2.10E-02	100.00%
M2-M1-PO1(FOX)	0.23	0.23	2.50E-01	9.91E-02	2.87E-02	1.48E-02	6.93E-03	1.81E-02	9.12E-03	4.49E-03	98.10%
	0.23	2	1.28E-01	3.23E-03	7.22E-02	1.48E-02	2.87E-02	4.92E-02	9.12E-03	2.00E-02	100.00%
M2-M1-PO1(OD)	0.23	0.23	2.50E-01	9.90E-02	2.90E-02	1.50E-02	7.01E-03	1.81E-02	9.12E-03	4.49E-03	98.10%
	0.23	2	1.28E-01	3.19E-03	7.28E-02	1.50E-02	2.89E-02	4.91E-02	9.12E-03	2.00E-02	100.00%
M3-M1-FOX	0.23	0.23	2.43E-01	1.04E-01	1.58E-02	7.35E-03	4.24E-03	7.77E-03	3.45E-03	2.16E-03	95.10%
	0.23	2	9.56E-02	1.07E-02	4.85E-02	7.35E-03	2.06E-02	2.47E-02	3.45E-03	1.06E-02	99.00%
M3-M1-OD	0.23	0.23	2.45E-01	1.03E-01	2.24E-02	1.09E-02	5.77E-03	7.58E-03	3.45E-03	2.07E-03	96.00%
	0.23	2	1.05E-01	8.47E-03	6.39E-02	1.09E-02	2.65E-02	2.36E-02	3.45E-03	1.00E-02	99.30%
M3-M1-PO1(FOX)	0.23	0.23	2.48E-01	1.01E-01	2.98E-02	1.48E-02	7.49E-03	7.51E-03	3.45E-03	2.03E-03	96.60%
	0.23	2	1.15E-01	7.02E-03	7.81E-02	1.48E-02	3.16E-02	2.26E-02	3.45E-03	9.55E-03	99.40%
M3-M1-PO1(OD)	0.23	0.23	2.48E-01	1.01E-01	3.01E-02	1.50E-02	7.57E-03	7.51E-03	3.45E-03	2.03E-03	96.60%
	0.23	2	1.16E-01	6.97E-03	7.87E-02	1.50E-02	3.18E-02	2.25E-02	3.45E-03	9.53E-03	99.40%
M3-M2-FOX	0.28	0.28	2.19E-01	8.93E-02	8.28E-03	3.85E-03	2.22E-03	2.28E-02	1.11E-02	5.84E-03	95.80%
	0.28	2	1.03E-01	9.91E-03	2.31E-02	3.85E-03	9.62E-03	5.93E-02	1.11E-02	2.41E-02	99.10%
M3-M2-OD	0.28	0.28	2.19E-01	8.92E-02	9.45E-03	4.47E-03	2.49E-03	2.26E-02	1.11E-02	5.73E-03	96.00%
	0.28	2	1.04E-01	9.26E-03	2.63E-02	4.47E-03	1.09E-02	5.88E-02	1.11E-02	2.38E-02	99.40%
M3-M2-PO1(FOX)	0.28	0.28	2.19E-01	8.90E-02	1.03E-02	4.92E-03	2.68E-03	2.24E-02	1.11E-02	5.66E-03	96.20%
	0.28	2	1.05E-01	8.85E-03	2.85E-02	4.92E-03	1.18E-02	5.84E-02	1.11E-02	2.36E-02	99.50%
M3-M2-PO1(OD)	0.28	0.28	2.19E-01	8.90E-02	1.03E-02	4.94E-03	2.69E-03	2.24E-02	1.11E-02	5.66E-03	96.20%
	0.28	2	1.05E-01	8.83E-03	2.86E-02	4.94E-03	1.18E-02	5.83E-02	1.11E-02	2.36E-02	99.50%
M3-M2-M1	0.28	0.28	2.22E-01	8.67E-02	2.18E-02	1.11E-02	5.33E-03	2.18E-02	1.11E-02	5.35E-03	97.80%
	0.28	2	1.19E-01	4.96E-03	5.43E-02	1.11E-02	2.16E-02	5.44E-02	1.11E-02	2.17E-02	99.90%
M4-M1-FOX	0.23	0.23	2.43E-01	1.04E-01	1.66E-02	7.35E-03	4.62E-03	5.17E-03	2.13E-03	1.52E-03	94.70%
	0.23	2	9.30E-02	1.24E-02	4.99E-02	7.35E-03	2.13E-02	1.62E-02	2.13E-03	7.01E-03	97.70%

*** Structure B *** (continued)

Structure	width	space	Ctotal	Cc	Cbottom	Cb_area	Cfb	Ctop	Ct_area	Cft	Csum/Ctotal
	(um)	(um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	
M4-M1-OD	0.23	0.23	2.45E-01	1.03E-01	2.33E-02	1.09E-02	6.20E-03	5.01E-03	2.13E-03	1.44E-03	95.60%
	0.23	2	1.03E-01	1.00E-02	6.56E-02	1.09E-02	2.74E-02	1.54E-02	2.13E-03	6.61E-03	98.30%
M4-M1-PO1(FOX)	0.23	0.23	2.47E-01	1.01E-01	3.07E-02	1.48E-02	7.93E-03	4.92E-03	2.13E-03	1.40E-03	96.20%
	0.23	2	1.13E-01	8.45E-03	8.00E-02	1.48E-02	3.26E-02	1.47E-02	2.13E-03	6.27E-03	98.60%
M4-M1-PO1(OD)	0.23	0.23	2.47E-01	1.01E-01	3.10E-02	1.50E-02	8.01E-03	4.92E-03	2.13E-03	1.40E-03	96.20%
	0.23	2	1.14E-01	8.39E-03	8.06E-02	1.50E-02	3.28E-02	1.46E-02	2.13E-03	6.26E-03	98.60%
M4-M2-FOX	0.28	0.28	2.16E-01	9.19E-02	8.93E-03	3.85E-03	2.54E-03	9.72E-03	4.20E-03	2.76E-03	93.80%
	0.28	2	8.63E-02	1.57E-02	2.53E-02	3.85E-03	1.07E-02	2.75E-02	4.20E-03	1.17E-02	97.60%
M4-M2-OD	0.28	0.28	2.16E-01	9.17E-02	1.01E-02	4.47E-03	2.82E-03	9.56E-03	4.20E-03	2.68E-03	94.00%
	0.28	2	8.76E-02	1.49E-02	2.88E-02	4.47E-03	1.22E-02	2.72E-02	4.20E-03	1.15E-02	98.00%
M4-M2-PO1(FOX)	0.28	0.28	2.16E-01	9.16E-02	1.10E-02	4.92E-03	3.02E-03	9.46E-03	4.20E-03	2.63E-03	94.10%
	0.28	2	8.88E-02	1.44E-02	3.13E-02	4.92E-03	1.32E-02	2.71E-02	4.20E-03	1.15E-02	98.20%
M4-M2-PO1(OD)	0.28	0.28	2.16E-01	9.15E-02	1.10E-02	4.94E-03	3.02E-03	9.45E-03	4.20E-03	2.63E-03	94.10%
	0.28	2	8.88E-02	1.44E-02	3.14E-02	4.94E-03	1.32E-02	2.71E-02	4.20E-03	1.15E-02	98.30%
M4-M2-M1	0.28	0.28	2.19E-01	8.92E-02	2.26E-02	1.11E-02	5.74E-03	8.97E-03	4.20E-03	2.38E-03	95.90%
	0.28	2	1.04E-01	9.58E-03	5.88E-02	1.11E-02	2.39E-02	2.50E-02	4.20E-03	1.04E-02	99.30%
M4-M3-FOX	0.28	0.28	2.19E-01	8.96E-02	5.60E-03	2.45E-03	1.57E-03	2.36E-02	1.11E-02	6.23E-03	95.30%
	0.28	2	1.01E-01	1.14E-02	1.54E-02	2.45E-03	6.50E-03	6.07E-02	1.11E-02	2.48E-02	98.00%
M4-M3-OD	0.28	0.28	2.19E-01	8.95E-02	6.07E-03	2.69E-03	1.69E-03	2.34E-02	1.11E-02	6.14E-03	95.40%
	0.28	2	1.01E-01	1.11E-02	1.68E-02	2.69E-03	7.06E-03	6.04E-02	1.11E-02	2.47E-02	98.30%
M4-M3-PO1(FOX)	0.28	0.28	2.19E-01	8.95E-02	6.37E-03	2.85E-03	1.76E-03	2.33E-02	1.11E-02	6.09E-03	95.40%
	0.28	2	1.01E-01	1.10E-02	1.77E-02	2.85E-03	7.41E-03	6.03E-02	1.11E-02	2.46E-02	98.40%
M4-M3-PO1(OD)	0.28	0.28	2.19E-01	8.95E-02	6.38E-03	2.85E-03	1.76E-03	2.33E-02	1.11E-02	6.09E-03	95.40%
	0.28	2	1.01E-01	1.10E-02	1.77E-02	2.85E-03	7.42E-03	6.02E-02	1.11E-02	2.46E-02	98.40%
M4-M3-M1	0.28	0.28	2.19E-01	8.92E-02	8.94E-03	4.20E-03	2.37E-03	2.26E-02	1.11E-02	5.77E-03	95.90%
	0.28	2	1.04E-01	9.54E-03	2.49E-02	4.20E-03	1.04E-02	5.90E-02	1.11E-02	2.39E-02	99.30%
M4-M3-M2	0.28	0.28	2.22E-01	8.67E-02	2.18E-02	1.11E-02	5.33E-03	2.18E-02	1.11E-02	5.35E-03	97.80%
	0.28	2	1.19E-01	4.96E-03	5.43E-02	1.11E-02	2.16E-02	5.44E-02	1.11E-02	2.17E-02	99.90%
M5-M1-FOX	0.23	0.23	2.43E-01	1.04E-01	1.71E-02	7.35E-03	4.89E-03	3.93E-03	1.54E-03	1.19E-03	94.50%
	0.23	2	9.21E-02	1.31E-02	5.09E-02	7.35E-03	2.18E-02	1.21E-02	1.54E-03	5.26E-03	96.70%
M5-M1-OD	0.23	0.23	2.45E-01	1.03E-01	2.38E-02	1.09E-02	6.48E-03	3.78E-03	1.54E-03	1.12E-03	95.40%
	0.23	2	1.02E-01	1.07E-02	6.67E-02	1.09E-02	2.79E-02	1.14E-02	1.54E-03	4.94E-03	97.50%
M5-M1-PO1(FOX)	0.23	0.23	2.47E-01	1.01E-01	3.13E-02	1.48E-02	8.24E-03	3.70E-03	1.54E-03	1.08E-03	96.00%
	0.23	2	1.12E-01	9.07E-03	8.11E-02	1.48E-02	3.31E-02	1.09E-02	1.54E-03	4.68E-03	97.90%
M5-M1-PO1(OD)	0.23	0.23	2.47E-01	1.01E-01	3.16E-02	1.50E-02	8.32E-03	3.70E-03	1.54E-03	1.08E-03	96.10%
	0.23	2	1.13E-01	9.01E-03	8.17E-02	1.50E-02	3.34E-02	1.09E-02	1.54E-03	4.67E-03	98.00%
M5-M2-FOX	0.28	0.28	2.16E-01	9.23E-02	9.57E-03	3.85E-03	2.86E-03	6.58E-03	2.59E-03	1.99E-03	93.10%
	0.28	2	8.31E-02	1.77E-02	2.62E-02	3.85E-03	1.12E-02	1.80E-02	2.59E-03	7.72E-03	95.80%
M5-M2-OD	0.28	0.28	2.16E-01	9.21E-02	1.08E-02	4.47E-03	3.15E-03	6.43E-03	2.59E-03	1.92E-03	93.40%
	0.28	2	8.45E-02	1.69E-02	2.97E-02	4.47E-03	1.26E-02	1.78E-02	2.59E-03	7.62E-03	96.30%
M5-M2-PO1(FOX)	0.28	0.28	2.16E-01	9.20E-02	1.16E-02	4.92E-03	3.35E-03	6.34E-03	2.59E-03	1.87E-03	93.50%
	0.28	2	8.55E-02	1.64E-02	3.22E-02	4.92E-03	1.36E-02	1.77E-02	2.59E-03	7.55E-03	96.60%
M5-M2-PO1(OD)	0.28	0.28	2.16E-01	9.20E-02	1.17E-02	4.94E-03	3.36E-03	6.34E-03	2.59E-03	1.87E-03	93.50%
	0.28	2	8.55E-02	1.63E-02	3.23E-02	4.94E-03	1.37E-02	1.77E-02	2.59E-03	7.55E-03	96.60%
M5-M2-M1	0.28	0.28	2.19E-01	8.96E-02	2.34E-02	1.11E-02	6.15E-03	5.88E-03	2.59E-03	1.65E-03	95.30%
	0.28	2	1.01E-01	1.13E-02	6.04E-02	1.11E-02	2.47E-02	1.63E-02	2.59E-03	6.83E-03	98.20%

*** Structure B *** (continued)

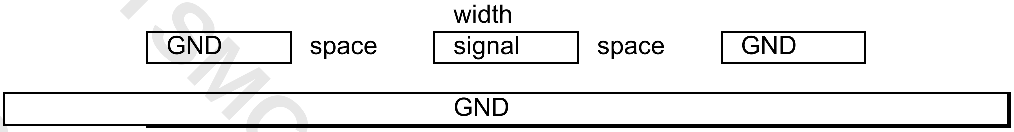
Structure	width (um)	space (um)	Ctotal (fF/um)	Cc (fF/um)	Cbottom (fF/um)	Cb_area (fF/um)	Cfb (fF/um)	Ctop (fF/um)	Ct_area (fF/um)	Cft (fF/um)	Csum/Ctotal
M5-M3-FOX	0.28	0.28	2.16E-01	9.22E-02	6.20E-03	2.45E-03	1.87E-03	1.03E-02	4.20E-03	3.07E-03	93.20%
	0.28	2	8.37E-02	1.74E-02	1.71E-02	2.45E-03	7.30E-03	2.83E-02	4.20E-03	1.21E-02	95.90%
M5-M3-OD	0.28	0.28	2.16E-01	9.22E-02	6.68E-03	2.69E-03	2.00E-03	1.02E-02	4.20E-03	3.00E-03	93.30%
	0.28	2	8.40E-02	1.71E-02	1.85E-02	2.69E-03	7.91E-03	2.82E-02	4.20E-03	1.20E-02	96.30%
M5-M3-PO1(FOX)	0.28	0.28	2.16E-01	9.21E-02	6.99E-03	2.85E-03	2.07E-03	1.01E-02	4.20E-03	2.96E-03	93.40%
	0.28	2	8.43E-02	1.69E-02	1.95E-02	2.85E-03	8.31E-03	2.81E-02	4.20E-03	1.19E-02	96.50%
M5-M3-PO1(OD)	0.28	0.28	2.16E-01	9.21E-02	7.00E-03	2.85E-03	2.07E-03	1.01E-02	4.20E-03	2.96E-03	93.40%
	0.28	2	8.43E-02	1.69E-02	1.95E-02	2.85E-03	8.32E-03	2.81E-02	4.20E-03	1.19E-02	96.50%
M5-M3-M1	0.28	0.28	2.16E-01	9.18E-02	9.60E-03	4.20E-03	2.70E-03	9.61E-03	4.20E-03	2.70E-03	93.90%
	0.28	2	8.70E-02	1.52E-02	2.73E-02	4.20E-03	1.16E-02	2.74E-02	4.20E-03	1.16E-02	97.90%
M5-M3-M2	0.28	0.28	2.19E-01	8.92E-02	2.26E-02	1.11E-02	5.74E-03	8.97E-03	4.20E-03	2.38E-03	95.90%
	0.28	2	1.04E-01	9.58E-03	5.88E-02	1.11E-02	2.39E-02	2.50E-02	4.20E-03	1.04E-02	99.30%
M5-M4-FOX	0.28	0.28	2.19E-01	8.97E-02	4.28E-03	1.80E-03	1.24E-03	2.42E-02	1.11E-02	6.53E-03	95.10%
	0.28	2	1.00E-01	1.20E-02	1.16E-02	1.80E-03	4.92E-03	6.16E-02	1.11E-02	2.53E-02	97.20%
M5-M4-OD	0.28	0.28	2.19E-01	8.97E-02	4.54E-03	1.93E-03	1.31E-03	2.40E-02	1.11E-02	6.47E-03	95.20%
	0.28	2	1.00E-01	1.19E-02	1.24E-02	1.93E-03	5.23E-03	6.14E-02	1.11E-02	2.51E-02	97.40%
M5-M4-PO1(FOX)	0.28	0.28	2.19E-01	8.97E-02	4.70E-03	2.00E-03	1.35E-03	2.40E-02	1.11E-02	6.43E-03	95.20%
	0.28	2	1.00E-01	1.19E-02	1.28E-02	2.00E-03	5.42E-03	6.13E-02	1.11E-02	2.51E-02	97.50%
M5-M4-PO1(OD)	0.28	0.28	2.19E-01	8.97E-02	4.70E-03	2.01E-03	1.35E-03	2.40E-02	1.11E-02	6.43E-03	95.20%
	0.28	2	1.00E-01	1.19E-02	1.29E-02	2.01E-03	5.43E-03	6.13E-02	1.11E-02	2.51E-02	97.50%
M5-M4-M1	0.28	0.28	2.19E-01	8.96E-02	5.87E-03	2.59E-03	1.64E-03	2.35E-02	1.11E-02	6.18E-03	95.40%
	0.28	2	1.01E-01	1.12E-02	1.62E-02	2.59E-03	6.82E-03	6.05E-02	1.11E-02	2.47E-02	98.20%
M5-M4-M2	0.28	0.28	2.19E-01	8.92E-02	8.94E-03	4.20E-03	2.37E-03	2.26E-02	1.11E-02	5.77E-03	95.90%
	0.28	2	1.04E-01	9.54E-03	2.49E-02	4.20E-03	1.04E-02	5.90E-02	1.11E-02	2.39E-02	99.30%
M5-M4-M3	0.28	0.28	2.22E-01	8.67E-02	2.18E-02	1.11E-02	5.33E-03	2.18E-02	1.11E-02	5.35E-03	97.80%
	0.28	2	1.19E-01	4.96E-03	5.43E-02	1.11E-02	2.16E-02	5.44E-02	1.11E-02	2.17E-02	99.90%
M6-M1-FOX	0.23	0.23	2.43E-01	1.04E-01	1.76E-02	7.35E-03	5.12E-03	3.13E-03	1.18E-03	9.73E-04	94.40%
	0.23	2	9.17E-02	1.35E-02	5.16E-02	7.35E-03	2.21E-02	9.47E-03	1.18E-03	4.14E-03	96.00%
M6-M1-OD	0.23	0.23	2.45E-01	1.03E-01	2.43E-02	1.09E-02	6.71E-03	2.99E-03	1.18E-03	9.05E-04	95.30%
	0.23	2	1.02E-01	1.11E-02	6.75E-02	1.09E-02	2.83E-02	8.94E-03	1.18E-03	3.88E-03	96.90%
M6-M1-PO1(FOX)	0.23	0.23	2.47E-01	1.01E-01	3.18E-02	1.48E-02	8.48E-03	2.92E-03	1.18E-03	8.69E-04	96.00%
	0.23	2	1.12E-01	9.39E-03	8.19E-02	1.48E-02	3.36E-02	8.52E-03	1.18E-03	3.67E-03	97.40%
M6-M1-PO1(OD)	0.23	0.23	2.47E-01	1.01E-01	3.21E-02	1.50E-02	8.57E-03	2.92E-03	1.18E-03	8.68E-04	96.00%
	0.23	2	1.13E-01	9.33E-03	8.26E-02	1.50E-02	3.38E-02	8.50E-03	1.18E-03	3.66E-03	97.50%
M6-M2-FOX	0.28	0.28	2.15E-01	9.24E-02	1.01E-02	3.85E-03	3.13E-03	4.97E-03	1.82E-03	1.57E-03	92.80%
	0.28	2	8.20E-02	1.86E-02	2.68E-02	3.85E-03	1.15E-02	1.32E-02	1.82E-03	5.69E-03	94.20%
M6-M2-OD	0.28	0.28	2.16E-01	9.22E-02	1.13E-02	4.47E-03	3.43E-03	4.84E-03	1.82E-03	1.51E-03	93.10%
	0.28	2	8.34E-02	1.78E-02	3.05E-02	4.47E-03	1.30E-02	1.30E-02	1.82E-03	5.61E-03	94.90%
M6-M2-PO1(FOX)	0.28	0.28	2.16E-01	9.21E-02	1.22E-02	4.92E-03	3.64E-03	4.76E-03	1.82E-03	1.47E-03	93.30%
	0.28	2	8.44E-02	1.73E-02	3.29E-02	4.92E-03	1.40E-02	1.29E-02	1.82E-03	5.54E-03	95.20%
M6-M2-PO1(OD)	0.28	0.28	2.16E-01	9.21E-02	1.22E-02	4.94E-03	3.65E-03	4.76E-03	1.82E-03	1.47E-03	93.30%
	0.28	2	8.44E-02	1.72E-02	3.30E-02	4.94E-03	1.40E-02	1.29E-02	1.82E-03	5.54E-03	95.20%
M6-M2-M1	0.28	0.28	2.19E-01	8.97E-02	2.41E-02	1.11E-02	6.49E-03	4.34E-03	1.82E-03	1.26E-03	95.10%
	0.28	2	1.00E-01	1.21E-02	6.14E-02	1.11E-02	2.52E-02	1.18E-02	1.82E-03	4.99E-03	97.20%

*** Structure B *** (continued)											
Structure	width	space	Ctotal	Cc	Cbottom	Cb_area	Cfb	Ctop	Ct_area	Cft	Csum/Ctotal
	(um)	(um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	
M6-M3-FOX	0.28	0.28	2.15E-01	9.26E-02	6.81E-03	2.45E-03	2.18E-03	6.94E-03	2.50E-03	2.22E-03	92.50%
	0.28	2	8.04E-02	1.97E-02	1.77E-02	2.45E-03	7.64E-03	1.81E-02	2.50E-03	7.78E-03	93.60%
M6-M3-OD	0.28	0.28	2.15E-01	9.26E-02	7.31E-03	2.69E-03	2.31E-03	6.81E-03	2.50E-03	2.16E-03	92.60%
	0.28	2	8.07E-02	1.94E-02	1.92E-02	2.69E-03	8.27E-03	1.79E-02	2.50E-03	7.71E-03	94.00%
M6-M3-PO1(FOX)	0.28	0.28	2.15E-01	9.25E-02	7.62E-03	2.85E-03	2.39E-03	6.74E-03	2.50E-03	2.12E-03	92.60%
	0.28	2	8.10E-02	1.92E-02	2.02E-02	2.85E-03	8.69E-03	1.79E-02	2.50E-03	7.69E-03	94.40%
M6-M3-PO1(OD)	0.28	0.28	2.15E-01	9.25E-02	7.64E-03	2.85E-03	2.39E-03	6.74E-03	2.50E-03	2.12E-03	92.60%
	0.28	2	8.10E-02	1.91E-02	2.03E-02	2.85E-03	8.71E-03	1.79E-02	2.50E-03	7.68E-03	94.40%
M6-M3-M1	0.28	0.28	2.16E-01	9.22E-02	1.03E-02	4.20E-03	3.05E-03	6.30E-03	2.50E-03	1.90E-03	93.20%
	0.28	2	8.37E-02	1.74E-02	2.83E-02	4.20E-03	1.20E-02	1.73E-02	2.50E-03	7.42E-03	96.00%
M6-M3-M2	0.28	0.28	2.19E-01	8.96E-02	2.35E-02	1.11E-02	6.19E-03	5.70E-03	2.50E-03	1.60E-03	95.30%
	0.28	2	1.01E-01	1.14E-02	6.05E-02	1.11E-02	2.47E-02	1.57E-02	2.50E-03	6.61E-03	98.10%
M6-M4-FOX	0.28	0.28	2.15E-01	9.24E-02	4.89E-03	1.80E-03	1.54E-03	1.04E-02	3.96E-03	3.20E-03	92.90%
	0.28	2	8.22E-02	1.85E-02	1.30E-02	1.80E-03	5.60E-03	2.75E-02	3.96E-03	1.18E-02	94.30%
M6-M4-OD	0.28	0.28	2.15E-01	9.24E-02	5.16E-03	1.93E-03	1.62E-03	1.03E-02	3.96E-03	3.15E-03	92.90%
	0.28	2	8.24E-02	1.83E-02	1.38E-02	1.93E-03	5.94E-03	2.74E-02	3.96E-03	1.17E-02	94.60%
M6-M4-PO1(FOX)	0.28	0.28	2.15E-01	9.24E-02	5.32E-03	2.00E-03	1.66E-03	1.02E-02	3.96E-03	3.12E-03	92.90%
	0.28	2	8.25E-02	1.83E-02	1.43E-02	2.00E-03	6.15E-03	2.73E-02	3.96E-03	1.17E-02	94.80%
M6-M4-PO1(OD)	0.28	0.28	2.15E-01	9.24E-02	5.33E-03	2.01E-03	1.66E-03	1.02E-02	3.96E-03	3.11E-03	92.90%
	0.28	2	8.25E-02	1.83E-02	1.43E-02	2.01E-03	6.16E-03	2.73E-02	3.96E-03	1.17E-02	94.80%
M6-M4-M1	0.28	0.28	2.16E-01	9.23E-02	6.54E-03	2.59E-03	1.97E-03	9.80E-03	3.96E-03	2.92E-03	93.20%
	0.28	2	8.34E-02	1.76E-02	1.80E-02	2.59E-03	7.70E-03	2.69E-02	3.96E-03	1.14E-02	95.90%
M6-M4-M2	0.28	0.28	2.16E-01	9.19E-02	9.67E-03	4.20E-03	2.73E-03	9.16E-03	3.96E-03	2.60E-03	93.80%
	0.28	2	8.65E-02	1.55E-02	2.74E-02	4.20E-03	1.16E-02	2.60E-02	3.96E-03	1.10E-02	97.70%
M6-M4-M3	0.28	0.28	2.19E-01	8.93E-02	2.27E-02	1.11E-02	5.78E-03	8.52E-03	3.96E-03	2.28E-03	95.80%
	0.28	2	1.03E-01	9.83E-03	5.90E-02	1.11E-02	2.40E-02	2.37E-02	3.96E-03	9.88E-03	99.10%
M6-M5-FOX	0.28	0.28	2.18E-01	9.04E-02	3.52E-03	1.42E-03	1.05E-03	2.16E-02	9.57E-03	6.03E-03	94.70%
	0.28	2	9.58E-02	1.33E-02	9.58E-03	1.42E-03	4.08E-03	5.61E-02	9.57E-03	2.33E-02	96.40%
M6-M5-OD	0.28	0.28	2.18E-01	9.04E-02	3.69E-03	1.50E-03	1.10E-03	2.15E-02	9.57E-03	5.98E-03	94.70%
	0.28	2	9.59E-02	1.33E-02	1.00E-02	1.50E-03	4.27E-03	5.59E-02	9.57E-03	2.32E-02	96.50%
M6-M5-PO1(FOX)	0.28	0.28	2.18E-01	9.04E-02	3.79E-03	1.55E-03	1.12E-03	2.15E-02	9.57E-03	5.95E-03	94.70%
	0.28	2	9.60E-02	1.32E-02	1.03E-02	1.55E-03	4.39E-03	5.59E-02	9.57E-03	2.31E-02	96.50%
M6-M5-PO1(OD)	0.28	0.28	2.18E-01	9.04E-02	3.79E-03	1.55E-03	1.12E-03	2.15E-02	9.57E-03	5.95E-03	94.70%
	0.28	2	9.60E-02	1.32E-02	1.03E-02	1.55E-03	4.39E-03	5.59E-02	9.57E-03	2.31E-02	96.60%
M6-M5-M1	0.28	0.28	2.18E-01	9.04E-02	4.48E-03	1.87E-03	1.30E-03	2.11E-02	9.57E-03	5.78E-03	94.80%
	0.28	2	9.63E-02	1.29E-02	1.23E-02	1.87E-03	5.22E-03	5.53E-02	9.57E-03	2.29E-02	97.00%
M6-M5-M2	0.28	0.28	2.18E-01	9.02E-02	5.92E-03	2.59E-03	1.66E-03	2.05E-02	9.57E-03	5.48E-03	95.00%
	0.28	2	9.72E-02	1.22E-02	1.65E-02	2.59E-03	6.97E-03	5.44E-02	9.57E-03	2.24E-02	98.00%
M6-M5-M3	0.28	0.28	2.18E-01	8.99E-02	9.00E-03	4.20E-03	2.40E-03	1.97E-02	9.57E-03	5.09E-03	95.60%
	0.28	2	9.99E-02	1.04E-02	2.54E-02	4.20E-03	1.06E-02	5.30E-02	9.57E-03	2.17E-02	99.20%
M6-M5-M4	0.28	0.28	2.21E-01	8.74E-02	2.18E-02	1.11E-02	5.34E-03	1.90E-02	9.57E-03	4.71E-03	97.50%
	0.28	2	1.15E-01	5.62E-03	5.51E-02	1.11E-02	2.20E-02	4.88E-02	9.57E-03	1.96E-02	99.90%

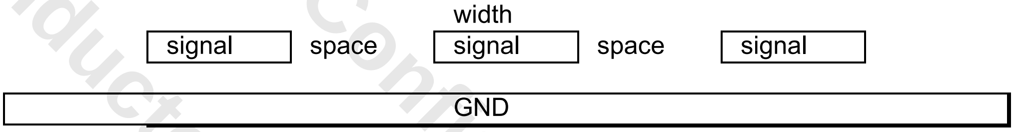
6.6.3 Comparison of metal routing delay between measurement and simulation

The verification of those models is through HSPICE simulation for ring oscillator with metal delay. The ring oscillator contains 17 stages inverter chain with 7 kinds of metal routing load: (a) a reference ring oscillator with short metal length as routing, (b) 1.3mm metal length of structure A with 3 different spacings, and (c) 1.3mm metal length of structure B with 3 different spacings. Structure A and B are shown in the schematic. The units for metal delay extracted from measurement are given as delay in ps. Here, the verification data is from 0.18um 1P6M 1.8V/5 LOGIC technology.

Structure A - Signal line with neighboring power lines:



Structure B - Signal line with neighboring signal lines:



The ring oscillators were measured and simulated with lumped RC at 25°C. The R & C values used in the following tables are calibrated with SEM pictures (the C values are Raphael simulation result by using the dielectric thickness from SEM). The geometry of metal line/space and speed results are listed below:

M1 used as metal routing:

Structure	Width (um)	Space (um)	R (ohm/sq.)	C (fF/um)	measurement Delay (ps)	simulation Delay (ps)
A	0.23	0.23	0.078	2.236e-1	159.1	165.9
A	0.23	0.46	0.078	1.470e-1	110.6	116.8
A	0.23	0.69	0.078	1.211e-1	91.2	94.9
B	0.23	0.69	0.078	3.790e-2	42.9	43.1
B	0.23	1.15	0.078	4.924e-2	49.4	50.2
B	0.23	1.61	0.078	5.781e-2	52.9	55.7

M2 used as metal routing:

Structure	Width (um)	Space (um)	R (ohm/sq.)	C (fF/um)	measurement Delay (ps)	simulation Delay (ps)
A	0.28	0.28	0.076	1.905e-1	124.1	128.6
A	0.28	0.56	0.076	1.267e-1	86.8	90.1
A	0.28	0.84	0.076	1.042e-1	73.5	76.3
B	0.28	0.84	0.076	2.098e-2	28.2	26.2
B	0.28	1.40	0.076	2.757e-2	30.9	29.5
B	0.28	1.96	0.076	3.352e-2	33.5	33.8

6.7 MIM Capacitor Model

Two- terminal and 3-terminal MIM (1.0fF) are provided in this version.

6.7.1 Scaling Rule

The scaling equations for the various elements are empirically determined and shown in Table 6-3.

C_{mim} (F)	1.0fF => cmim_para·(1+v(n2,n3)·6.16e-5+(abs(v(n2,n3))^2)·-2.05e-5)
where,	
cmim_para	1.0fF=>(((wt-0.011u)·(lt-0.011u)·1e12·1.025)+2·((wt-0.011u)+(lt-0.011u))·1e6·0.2425)·1e-15·(1+(temper-25)·-5.225e-5+(temper-25)·(temper-25)·1e-8), where –0.011um is a electrical offset.

Table 6-2: Sub-circuit elements for Base-band MIMCAP.

6.7.2 TCC and VCC

The VCC and TCC characteristics of capacitors are evaluated with 25x25 um^2 .The capacitance shows a parabolic dependence of the DC bias voltage(-5V to 5V in steps of 1V) at 25 ℃, the Vcc1 = 61.6ppm/V , Vcc2 = -20.5 ppm/V^2 for 1.0fF MiMCAP. At 0 V bias different temperature, the Tcc1 and Tcc2 for 1.0fF capacitors is –52.25ppm/℃, -0.01ppm/℃^{2} TCC and VCC characteristics of UDC MiMcap capacitors are close to the results of MiMcap capacitors.

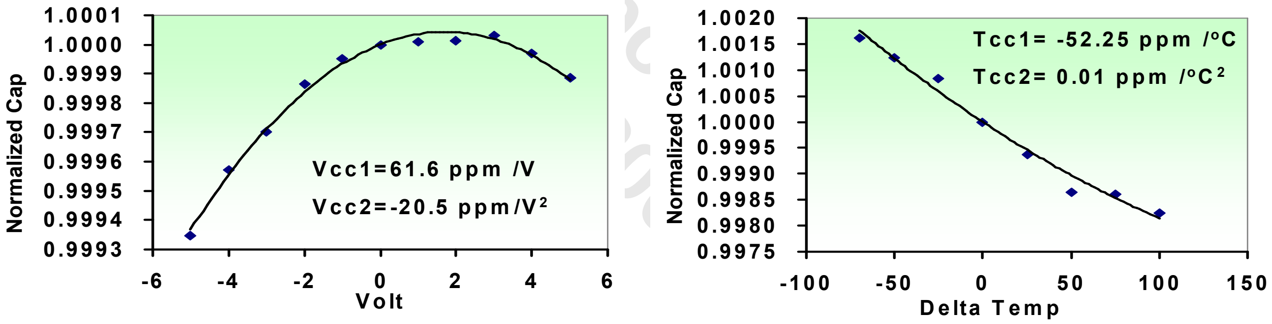
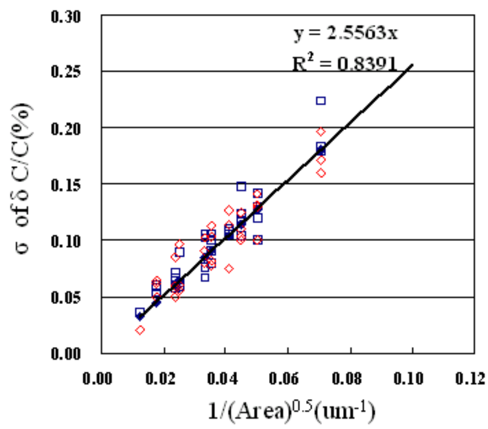


Fig. 6-3: (a) VCC , (b) TCC Plots of 1.0fF MIMCAP

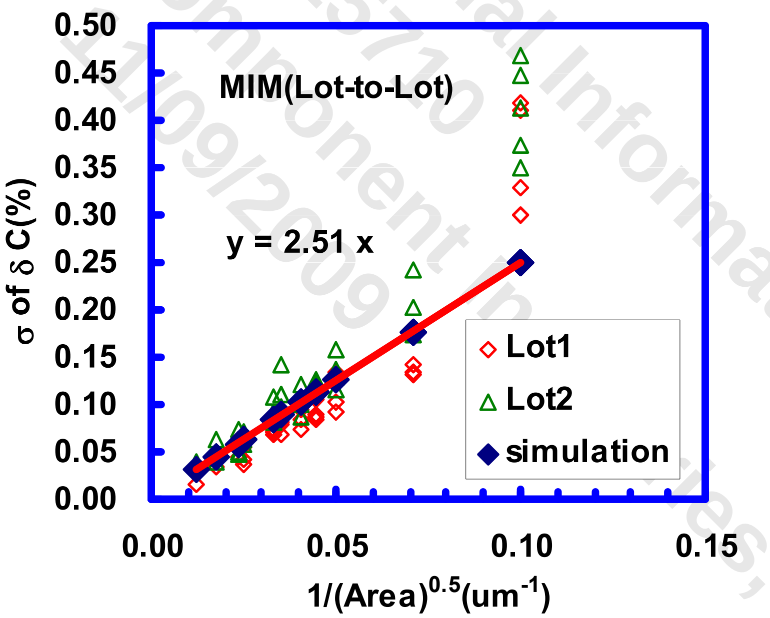
1 Curve fitting of the measured C for VCC uses C(V)=Co[1+Vcc1(V)+Vcc2(V)2], where Co is capacitance at 0V bias.
2 Curve fitting of the measured C for TCC uses C(T)=C(Tnom)[1+Tcc1(T-Tnom)+Tcc2(T-Tnom)2], where Tnom is at 25℃ and C(Tnom) is capacitance at 25℃.
3 Measurements have been carried out using the HP 4284 LCR meter @100KHz.

6.7.3 Mismatch and Statistical Model

The model for this technology has added the capability for mismatch analysis of an identical and closely spaced MiM pair. Random variations in Gaussian distribution of the total capacitance are included in the model to account for the mismatch performance. The designers will need to turn off (mismatchflag=0) or turn on (mismatchflag=1) in the macro model for nominal or Monte-Carlo analysis. The simulation results with the measured data of MiM are shown in Fig.6-4.
Statistical libraries of process (die to die) variation are denoted by MC_MIM for RF and baseband model respectively. The four sigma of the capacitance variation are 10% for the 1.0fF/um^2 MIM .



(a)



(b)

Fig. 6-4: Simulation results of 1000s Monte-Carlo random tests of sigma 2*(C1-C2)/(C1+C2) of 1.0fF/um^2 MIM.

6.8 Inductor Model

6.8.1 Model Usage Guide

Standard and symmetric octagonal spiral inductors using a thick AlCu metal with physical thickness at 2.34 um & 4.6um were fabricated on top of P-substrate and modeled based on the two-port Y-parameter fitting. Three types of scalable inductor models, which are standard (STD), symmetric (SYM), and symmetric with center tap (SYMCT) have been included in this release. The detailed ranges of models are listed in Table 6.8.1.

Table 6.8.1: Modeled spiral inductors

Specification	Standard Inductor				Symmetric Inductor		
Inductance(nH)	0.21 ~ 15.75				0.21 ~ 13.49		
Fixed width(µm)	6	9	15	30	9	15	30
Valid Turns(N)	0.5 ~ 5.5	0.5 ~ 5.5	0.5 ~ 5.5	1.5 ~ 5.5	1 ~ 4	1 ~ 5	1 ~ 5
	1/4 turn increments				Integral turn increments for symmetric without center-tap		
					Odd turn increments for symmetric with center-tap		
Valid Radius(R:µm)	30 ~ 125				30 ~ 120	40 ~ 120	65 ~ 150
Variable Metal Layer	1P4M, 1P5M, 1P6M						
Valid Temperature	-40°C ~ 125°C						
Valid Frequency	min(20GHz, Fsr)						

(a) 20KÅ UTM inductor model scope

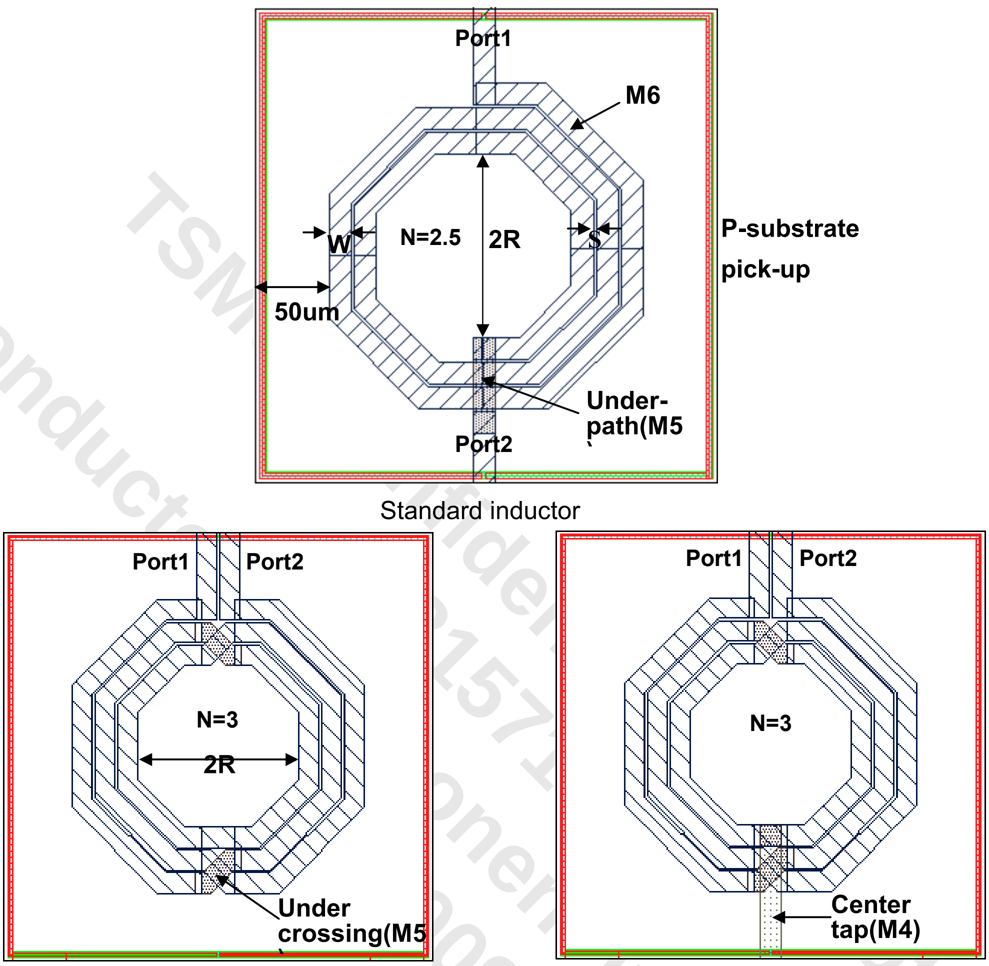
Specification	Standard Inductor				Symmetric			Center Tapped		
Inductance (nH)	0.2 ~ 17.2				0.2 ~ 14.6			0.2 ~ 14.6		
Fixed Spacing	s=3				s = 3			s = 3		
Fixed Width (w: um)	6	9	15	30	9	15	30	9	15	30
Valid Turns (nr)	0.5 ~ 5.5	0.5 ~ 5.5	0.5 ~ 5.5	1.5 ~ 5.5	1 ~ 4	1 ~ 5	1 ~ 5	1 ~ 4	1 ~ 5	1 ~ 5
Valid Radius (rad: um)	30 ~ 125				30 ~ 120	40 ~ 120	65 ~ 150	30 ~ 120	40 ~ 120	65 ~ 150
Turn Increment	0.25 turn increment				Integer turn increment			Odd integer turn increment		
Variable Metal Layer (lay)	1P4M ~ 1P6M (lay=4, 5, and 6)									
Valid Temperature	-40°C ~ 125°C									
Valid Frequency	min(F_{SRF}, 20GHz)									

(b) 40KÅ UTM inductor model scope

The symmetric inductors without center-tap can be used both in a single-ended operation and differential mode operation. Under differential mode operation, a DC biased can be applied at the tap. No device is allowed to be placed underneath the inductor since performance will be affected by the magnetic flux penetrating into the silicon substrate. Designers can change turns (N) and radius (R) to tune inductance (L). For information regarding the inductor design, please refer to the thick metal rule (section 4.5.9).

6.8.2 Inductor Layout

Top views of different inductor layouts with the key design parameters are shown in Figure 6.8.1.



Symmetric inductor

Symmetric inductor with center-tap

Figure 6.8.1: Top views of inductor layouts.

Key inductor parameters are described below:

N: Number of turns
W: Inductor track width
S: Spacing between tracks
R: Inner radius of inductor

6.8.3 Equivalent Circuit Model

A lumped RLC equivalent circuit representation of two-port standard inductor is shown in Figure 6.8.2. The values of each component are extracted through the fitting of the two-port Y-parameters that are obtained after de-embedding the dummy open and through accordingly. Figure 6.8.3 shows the equivalent circuit of a symmetric inductor with and without center-tap (dash-line).

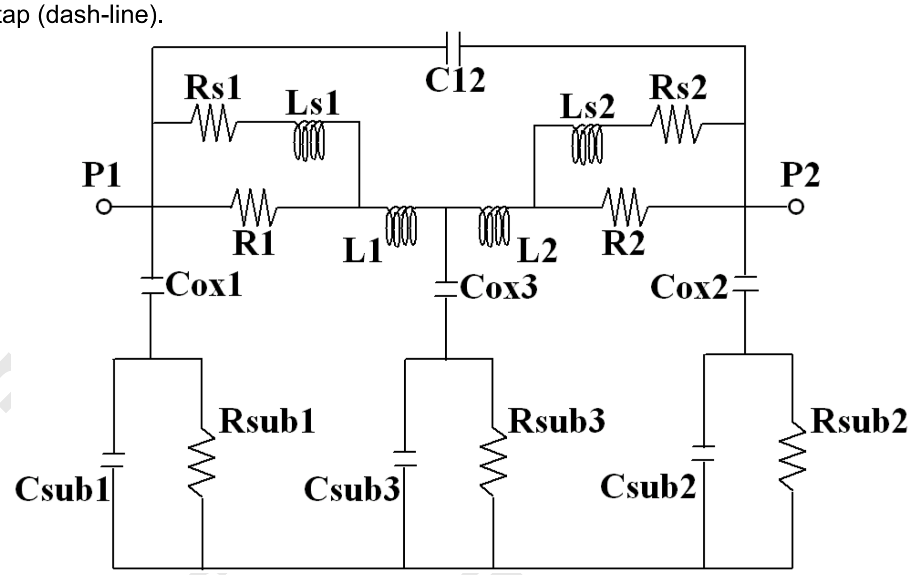


Figure 6.8.2: Equivalent circuit of a standard inductor.

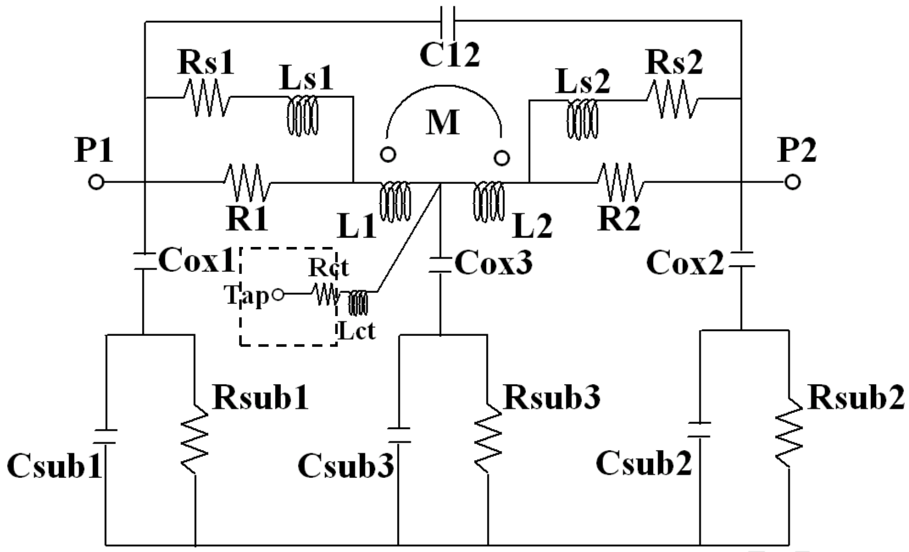


Figure 6.8.3: Equivalent circuit of a symmetric inductor with and without center-tap.

The definitions of the parameters are,

- L1 (and L2): Inductor self-inductance
- M: Mutual inductance
- R1 (and R2): Metal series resistance
- C12: Coupling capacitance between ports 1 and 2
- Cox1 (Cox2 and Cox3): Oxide capacitance between the spiral and substrate
- Rsub1 (Rsub2 and Rsub3): Silicon substrate resistance
- Csub1 (Csub2 and Csub3): Silicon substrate capacitance
- Ls1 (and Ls2): Inductance to model the skin effect of the metal track
- Rs1 (and Rs2): Resistance to model the skin effect of the metal track
- Lct: Inductance due to the center tap metal
- Rct: Resistance due to the center tap metal

6.8.4 Scaling Rules and Model Parameters

Inductance as a function of number of turns (N) and radius (R) is modeled with the empirical equation below.

$$L1=L2=a*N^{b}*DA^{c}*DO^{d}+e*N^{f}+g$$

where a, b, c, d, e, f and g are fitting parameters, DO is outer diameter, DI is inner diameter and DA(average diameter) = (DO+DI)/2. Quality of the model is show in Figure 6.8.4.

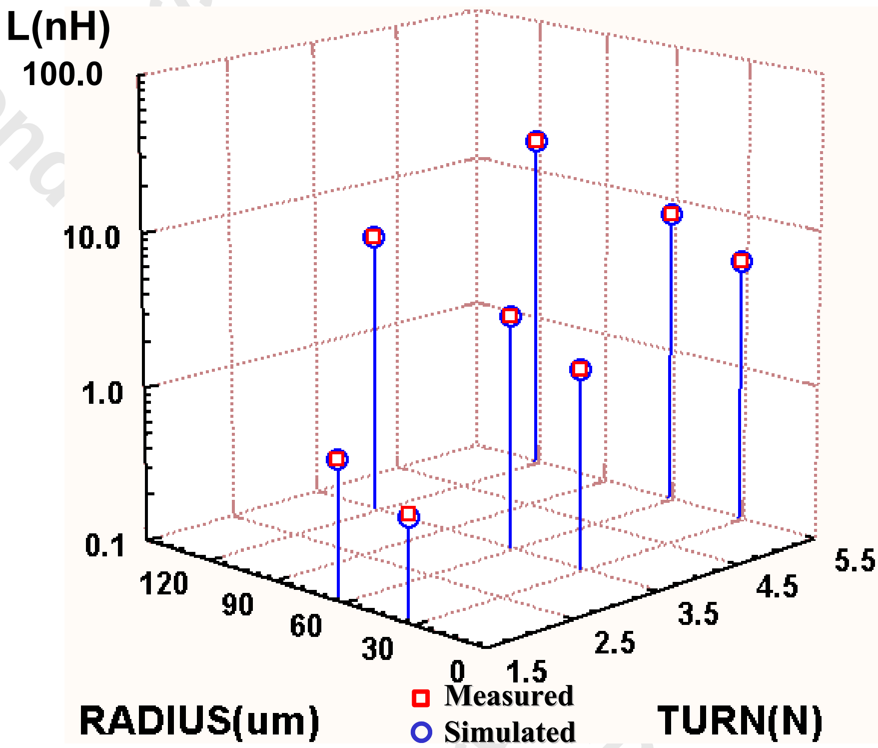


Figure 6.8.4: Inductance (W=15 um) as a function of number of turns and radius @ 0.9GHz

The scaling formulae for other parameters with respect to N and DA are,
For standard inductor,

R1=R2=a*N*DA^2+b*N+c*DA+d*N^2+e
Rs1=Rs2=a*N*DA^2+b*N+c*DA+d*N^2+e
C12=a*N+b*N*DA+c*N^2+d*DA^2+e
Cox1=a*N*DA+b
Cox2=Cox1
Cox3=Cox1+Cox2
Rsub1=a/(N*DA)+b/DA+c/N+d
Rsub2=Rsub1
Rsub3=Rsub1*Rsub2/(Rsub1+Rsub2)
Csub1=1.053e-11/Rsub1
Csub2=Csub1
Csub3=Csub1+Csub2

For symmetric inductor
K=a*N^b*DA^c*DO^d+e*N^f+g

For symmetric with center-tap
Lct=a*N^2+b*N+c
Rct=a*N+b

Fr is the resonance frequency of the inductor under single-end operation, *Qs* (-imagY$_{11}$/realY$_{11}$) is the Q-factor of the inductor under single-end operation, Q_d (imagZ$_d$/realZ$_d$) is the Q-factor of the inductor under differential mode operation and F_{dr} is the resonance frequency of the inductor under differential mode operation.

The differential mode one-port S-parameter S_d and differential mode input impedance Z_d are obtained by using the formulae below,

$$S_d = \frac{S_{11} + S_{22} - S_{12} - S_{21}}{2},$$

$$Z_d = 2Z_o\left(\frac{1+S_d}{1-S_d}\right)$$

where $2Z_o$ is the differential system impedance with Z_o assumed to be 50Ω. S_{11}, S_{12}, S_{21} and S_{22} are the two-port S-parameters of the single-ended mode inductor. All of S_{11}, S_{12}, S_{21}, S_{22}, and S_d were used in the parameter extraction.

Table.2: Scaling rules and model parameters of STD, SYM, and SYMCT with W=15μm

Parameter	STD
L1=L2	$4.381E\text{-}4*N^{1.731}*DA^{2.228}*DO^{-1.034}-19.27*N^{9.96E\text{-}4}+19.34$
Ls1=Ls2	$0.717*N^{1.063}*DA^{-0.104}*DO^{0.181}-0.942*N^{1.113}-0.0492$
R1=R2	$9.897E\text{-}06*N*DA^{2}-0.1242*N+2.602E\text{-}05*DA+0.0843*N^{2}+0.717$
Rs1=Rs2	$3.469E\text{-}06*N*DA^{2}+0.87*N+0.00374*DA-0.0366*N^{2}-0.365$
C12	$14.87*N-1.424E\text{-}03*N*DA-1.239*N^{2}+3.621E\text{-}4*DA^{2}-9.075$
Cox1	0.0471*N*DA+14.27
Cox2	0.0399*N*DA+15.21
Rsub1	62440/(N*DA)+45261.4/DA+1311.3/N-49.659
Rsub2	-11417/(N*DA)+172202/DA+866.29/N+130.12

Parameter	SYM & SYMCT
L1=L2	$4.54E\text{-}4*N^{1.492}*DA^{1.866}*DO^{-0.72}+5.691*N^{-0.00965}-5.656$
Ls1=Ls2	$16.77*N^{0.205}*DA^{0.0685}*DO^{-0.0719}-655.2*N^{0.00502}+638.9$
R1=R2	$7.641E\text{-}06*N*DA^{2}-0.394*N-0.00145*DA+0.155*N^{2}+1.067$
Rs1=Rs2	$4.653E\text{-}06*N*DA^{2}+0.136*N+0.00279*DA+0.085*N^{2}-0.303$
C12	$3.208*N+0.0833*N*DA+0.434*N^{2}-5.02E\text{-}05*DA^{2}-11$
Cox1	0.0391*N*DA+10.45
Rsub1	53011/(N*DA)+45116/DA+1666/N-395.07
K	$0.928*N^{0.366}*DA^{2.44}*DO^{-2.574}+0.901*N^{0.3002}-1.2304$
Lct	$3.75E\text{-}4*N^{2}+0.181625$
Rct	0.075*N+0.645

Table.3: Extracted parameters of STD, SYM, and SYMCT with W=15μm.

STD									
Device	L1	L11	R1	R11	C1	Cox1	Cox2	Rsub1	Rsub2
N=0.5 R=34 μm	0.112	0.013	0.712	0.384	0.500	16.2	16.9	4616.7	3656.9
N=0.5 R=64 μm	0.135	0.028	0.781	0.632	5.379	17.7	18.1	3760.7	2905.4
N=1.5 R=32.1 μm	0.222	0.125	0.860	1.265	13.591	21.1	21.0	1727.3	2417.7
N=1.5 R=62.1 μm	0.372	0.157	1.087	1.569	18.949	25.3	24.6	1380.6	1761.0
N=3.5 R=32.1 μm	0.890	0.410	1.906	2.924	33.284	35.8	33.4	809.5	1674.7
N=3.5 R=62.1 μm	1.531	0.448	2.574	3.382	39.949	45.7	41.8	656.7	1265.6
N=3.5 R=122.1 μm	3.005	0.529	4.658	4.560	61.098	65.5	58.6	528.4	922.2
N=5.5 R=32.1 μm	2.301	0.759	4.057	4.441	43.705	56.9	51.3	533.4	1323.4
N=5.5 R=62.1 μm	3.698	0.792	5.328	5.110	51.676	72.4	64.5	441.2	1046.3
N=5.5 R=122.1 μm	6.898	0.882	9.045	6.861	75.438	103.5	90.8	353.2	781.8

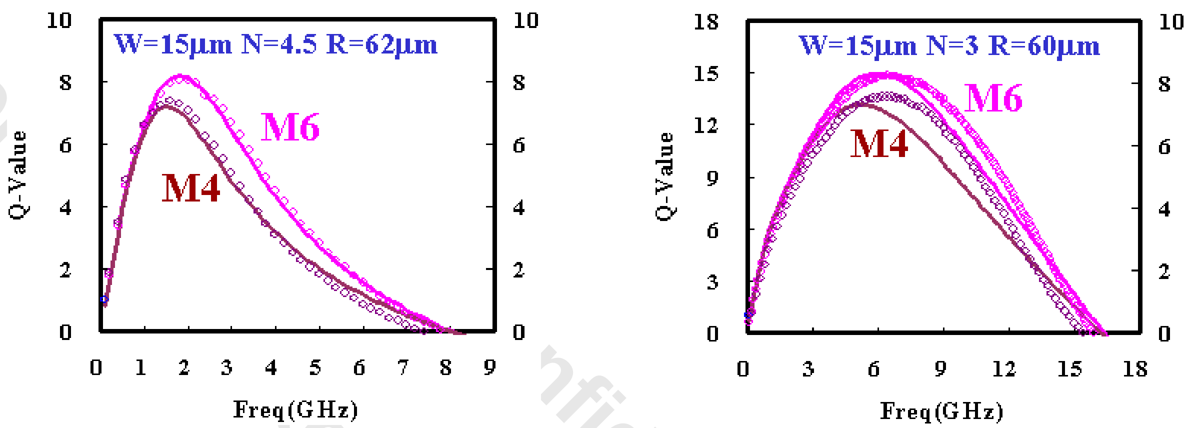
SYM & SYMCT										
Device	L1	L11	R1	R11	C1	Cox	Rsub	K	Lct	Rct
N=1 R=40 μm	0.111	0.012	0.759	0.226	0.099	14.2	2304.7	0.017	0.182	0.72
N=1 R=60 μm	0.152	0.041	0.771	0.380	2.969	15.7	1998.6	0.038	0.182	0.72
N=1 R=120 μm	0.286	0.062	0.955	0.933	10.614	20.4	1656.6	0.053	0.182	0.72
N=3 R=40 μm	0.464	0.239	1.474	1.464	33.937	25.6	647.2	0.339	0.185	0.87
N=3 R=60 μm	0.674	0.318	1.689	1.743	43.335	30.3	532.0	0.386	0.185	0.87
N=3 R=120 μm	1.363	0.424	2.775	2.845	70.562	44.4	377.8	0.457	0.185	0.87
N=5 R=40 μm	1.232	0.616	3.751	3.579	82.467	42.3	280.1	0.524	0.191	1.02
N=5 R=60 μm	1.683	0.710	4.252	4.031	98.393	50.1	212.8	0.571	0.191	1.02
N=5 R=120 μm	3.157	0.858	6.490	5.835	145.20	73.6	110.8	0.659	0.191	1.02

6.8.5 Variable Metal Layer Model

Field oxide capacitance, Coxn, where n is 4, 5 or 6, can be represented with the equation below.

Cox(layer)=Cox(layer=6)*((1/(7.67792+(4.14167)*(layer-2)))/(0.0412463))

The variation of Q with different metal layers (1P4M ~ 1P6M) is caused by the varying capacitance between the spiral and substrate. High Coxn degrades Q. The effect is shown in Figure 6.8.5.



Circle: Measured; Line: Simulated

Figure 6.8.5 20KÅ UTM (a) Standard inductor (b) Symmetric inductor

6.8.6 Corner Model Table

Skew parameters are listed in Table 6.8.4. The worst case is determined on the variation of Q-value.

Table 6.8.4: Corner parameters for inductor model.

WORST CASE PATAMETER VALUES				
component	Parameter	SLOW	Typical	FAST
L, Ls, K, Lct	l_indfac	1.0235	1	0.9762
R, Rs	rm6_indfac	1.1	1	0.9
C12	c12_indfac	1.2236	1	0.7764
Cox	cm6_indfac	1.0509	1	0.9551
Rsub	rsub_indfac	0.8	1	1.2
Rct	rm5_indfac	1.1	1	0.90

6.8.7 Model Error Table

Inductor fitting error between measurement and simulation are summarized in Table 6.8.5 to 6.8.14. For each device four Y-parameter fitting errors are separated with real part and imaginary part. Definition of fitting error is documented in section 12.

Target Parameter		Fitting Error (Real Y-parameter)																	
		Width = 6um								Width = 9um									
	N	0.5	0.5	3.5	3.5	3.5	5.5	5.5	5.5	0.5	0.5	1.5	1.5	2.5	2.5	2.5	4.5	4.5	4.5
	R	39.0	54.0	31.0	61.0	121.1	31.0	61.0	121.1	42.0	57.0	31.4	61.4	31.4	61.4	121.4	31.4	61.4	121.4
Y11(%)		10.7	18.8	14.2	2.5	0.9	15.6	4.6	1.1	10.8	16.6	16.4	0.7	12.5	1.3	1.6	7.3	4.6	2.9
Y21(%)		10.7	18.7	14.2	2.5	1.1	15.6	4.7	1.7	10.8	16.6	16.4	0.6	12.5	1.3	1.7	7.3	4.7	3.1
Y12(%)		10.7	18.8	14.2	2.5	1.1	15.6	4.7	1.6	10.8	16.6	16.4	0.7	12.5	1.3	1.7	7.3	4.6	3.0
Y22(%)		10.7	18.8	14.2	2.6	1.1	15.6	4.7	1.3	10.8	16.6	16.4	0.7	12.5	1.4	1.7	7.4	4.7	2.9
MEAN(%)		10.7	18.8	14.2	2.5	1.0	15.6	4.7	1.4	10.8	16.6	16.4	0.7	12.5	1.3	1.7	7.3	4.6	3.0

Table 6.8.5: Fitting error (real Y-parameter) table for 20KÅ UTM standard inductors (W = 6, 9μm).

Target Parameter		Fitting Error (Imag Y-parameter)																	
		Width = 6um								Width = 9um									
	N	0.5	0.5	3.5	3.5	3.5	5.5	5.5	5.5	0.5	0.5	1.5	1.5	2.5	2.5	2.5	4.5	4.5	4.5
	R	39.0	54.0	31.0	61.0	121.1	31.0	61.0	121.1	42.0	57.0	31.4	61.4	31.4	61.4	121.4	31.4	61.4	121.4
Y11(%)		9.9	18.2	16.0	3.1	0.7	19.5	7.3	2.7	10.7	16.2	16.8	0.7	13.8	1.3	2.6	9.7	7.2	4.6
Y21(%)		10.0	18.2	16.3	5.6	6.7	19.9	9.1	7.9	10.7	16.2	16.8	1.6	13.9	3.2	5.1	10.1	7.9	6.6
Y12(%)		9.9	18.1	16.2	5.6	6.7	19.8	9.0	7.9	10.6	16.1	16.8	1.6	13.8	3.2	5.1	10.0	7.8	6.6
Y22(%)		9.9	18.2	16.0	3.2	0.8	19.5	7.3	2.7	10.7	16.2	16.8	0.7	13.8	1.3	2.6	9.7	7.2	4.6
MEAN(%)		9.9	18.2	16.1	4.4	3.7	19.7	8.2	5.3	10.7	16.2	16.8	1.2	13.8	2.3	3.8	9.9	7.5	5.6

Table 6.8.6: Fitting error (imaginary Y-parameter) table for 20KÅ UTM standard inductors (W = 6, 9μm).

Target Parameter		Fitting Error (Real Y-parameter)																	
		Width = 15um										Width = 30um							
	N	0.5	0.5	1.5	1.5	3.5.	3.5	3.5	5.5	5.5	5.5	1.5	1.5	3.5	3.5	3.5	5.5	5.5	5.5
	R	34.0	64.0	32.1	62.1	32.1	62.1	122.1	32.1	62.1	122.1	34.1	64.1	34.1	64.1	124.1	34.1	64.1	124.1
Y11(%)		16.5	19.7	13.8	5.0	7.1	2.8	2.6	6.1	4.8	7.1	7.0	8.5	1.2	2.7	2.5	1.0	1.8	2.0
Y21(%)		16.5	19.7	13.8	5.0	7.1	2.8	2.7	6.1	4.9	7.3	7.1	8.5	1.3	2.5	1.9	0.6	1.7	3.0
Y12(%)		16.6	19.7	13.8	5.0	7.1	2.8	2.6	6.1	4.7	7.1	7.1	8.5	1.3	2.6	2.1	0.6	1.5	2.8
Y22(%)		16.5	19.8	13.8	5.1	7.1	2.8	2.5	6.1	4.8	7.1	7.0	8.5	1.1	2.6	2.1	0.6	1.5	1.9
MEAN(%)		16.5	19.7	13.8	5.0	7.1	2.8	2.6	6.1	4.8	7.2	7.1	8.5	1.2	2.6	2.1	0.7	1.6	2.4

Table 6.8.7: Fitting error (real Y-parameter) table for 20KÅ UTM standard inductors (W = 15, 30μm).

Target Parameter		Fitting Error (Imag Y-parameter)																	
		Width = 15um										Width = 30um							
	N	0.5	0.5	1.5	1.5	3.5.	3.5	3.5	5.5	5.5	5.5	1.5	1.5	3.5	3.5	3.5	5.5	5.5	5.5
	R	34.0	64.0	32.1	62.1	32.1	62.1	122.1	32.1	62.1	122.1	34.1	64.1	34.1	64.1	124.1	34.1	64.1	124.1
Y11(%)		13.4	19.5	14.7	5.1	9.9	5.6	6.1	12.9	7.6	7.2	11.5	15.3	3.9	4.7	2.8	0.8	1.3	2.3
Y21(%)		13.4	19.5	14.7	5.2	10.2	6.0	6.8	12.9	7.7	7.6	11.4	15.2	3.9	4.6	2.8	0.3	1.1	2.0
Y12(%)		13.4	19.4	14.7	5.1	10.1	5.9	6.7	12.9	7.7	7.6	11.4	15.2	3.9	4.6	2.9	0.3	1.2	2.1
Y22(%)		13.4	19.5	14.7	5.1	10.0	5.6	6.1	12.9	7.6	7.2	11.4	15.3	3.9	4.7	2.8	0.6	1.3	2.3
MEAN(%)		13.4	19.5	14.7	5.1	10.1	5.8	6.4	12.9	7.6	7.4	11.4	15.3	3.9	4.7	2.8	0.5	1.2	2.2

Table 6.8.8: Fitting error (imaginary Y-parameter) table for 20KÅ UTM standard inductors (W = 15, 30μm).

Target Parameter		Fitting Error (Real Y-parameter)														
		Width = 9um									Width = 9um with center-tap					
	N	1	1	1	3	3	3	5	5	5	1	1	1	3	3	3
	R	30	60	120	30	60	120	30	60	120	30	60	120	30	60	120
Y11(%)		20.3	13.4	5.5	6.5	5.2	4.8	7.8	1.3	2.6	6.1	4.1	6.5	6.1	6.8	7.8
Y21(%)		20.3	13.3	5.5	6.5	5.2	4.8	7.9	1.5	2.6	9.6	7.3	12.8	21.9	26.0	21.4
Y12(%)		20.4	13.4	5.4	6.5	5.2	4.8	7.8	1.4	2.5	9.5	7.4	12.7	22.0	26.3	21.7
Y22(%)		20.3	13.4	5.5	6.5	5.2	4.8	7.8	1.3	2.6	5.7	3.4	9.1	2.6	6.3	7.6
MEAN(%)		20.3	13.4	5.5	6.5	5.2	4.8	7.8	1.4	2.6	7.7	5.6	10.3	13.1	16.4	14.6

Table 6.8.9: Fitting error (real Y-parameter) table for 20KÅ UTM symmetric inductors (W = 9μm).

Target Parameter		Fitting Error (Imag Y-parameter)														
		Width = 9um									Width = 9um with center-tap					
	N	1	1	1	3	3	3	5	5	5	1	1	1	3	3	3
	R	30	60	120	30	60	120	30	60	120	30	60	120	30	60	120
Y11(%)		20.9	14.3	5.4	7.0	7.4	8.0	9.3	2.2	3.9	11.8	6.6	6.3	7.8	6.9	7.0
Y21(%)		20.9	14.3	5.6	7.0	7.3	8.0	9.3	2.2	3.8	12.5	6.0	10.0	16.1	24.5	20.2
Y12(%)		20.8	14.2	5.6	6.9	7.5	8.1	9.2	2.3	3.8	12.3	6.0	10.0	16.2	24.5	20.2
Y22(%)		20.9	14.3	5.4	7.0	7.4	8.0	9.3	2.2	3.9	11.0	5.6	9.1	5.4	6.7	7.1
MEAN(%)		20.9	14.3	5.5	7.0	7.4	8.0	9.3	2.3	3.9	11.9	6.1	8.9	11.4	15.7	13.6

Table 6.8.10: Fitting error (imaginary Y-parameter) table for 20KÅ UTM symmetric inductors (W = 9μm).

Target Parameter		Fitting Error (Real Y-parameter)																	
		Width = 15um									Width = 15um with center-tap								
	N	1	1	1	3	3	3	5	5	5	1	1	1	3	3	3	5	5	5
	R	40	60	120	40	60	120	40	60	120	40	60	120	40	60	120	40	60	120
Y11(%)		8.4	8.2	5.1	6.6	5.4	1.4	3.9	1.7	4.6	17.1	10.6	9.6	4.7	5.2	6.8	9.1	9.9	10.7
Y21(%)		8.5	8.2	5.2	6.6	5.4	1.5	4.0	1.8	4.7	38.0	28.0	11.0	25.3	22.1	17.5	26.6	24.0	20.7
Y12(%)		8.4	8.2	5.1	6.5	5.3	1.5	3.9	1.7	4.5	38.0	27.8	11.1	26.4	22.3	17.9	26.5	24.1	20.8
Y22(%)		8.4	8.2	5.1	6.6	5.4	1.4	3.9	1.7	4.6	24.3	14.0	11.1	6.2	6.2	6.2	7.5	8.9	10.2
MEAN(%)		8.4	8.2	5.1	6.6	5.4	1.4	3.9	1.7	4.6	29.3	20.1	10.7	15.6	14.0	12.1	17.4	16.7	15.6

Table 6.8.11: Fitting error (real Y-parameter) table for 20KÅ UTM symmetric inductors (W = 15μm).

Target Parameter		Fitting Error (Imag Y-parameter)																	
		Width = 15um									Width = 15um with center-tap								
	N	1	1	1	3	3	3	5	5	5	1	1	1	3	3	3	5	5	5
	R	40	60	120	40	60	120	40	60	120	40	60	120	40	60	120	40	60	120
Y11(%)		12.5	10.0	4.5	9.2	9.9	1.8	8.7	3.9	5.7	12.4	8.4	10.2	5.5	5.7	5.5	10.0	8.8	9.6
Y21(%)		12.5	10.1	4.8	9.1	9.7	1.9	8.6	3.8	5.7	27.0	20.3	11.2	21.4	20.4	14.8	21.4	20.0	18.7
Y12(%)		12.4	10.0	4.7	9.2	9.8	2.0	8.5	3.7	5.7	27.0	20.4	10.6	21.6	20.6	14.7	21.4	20.0	18.7
Y22(%)		12.5	10.0	4.5	9.2	9.9	1.8	8.7	3.9	5.7	17.2	7.9	12.3	5.3	6.3	5.3	9.1	9.2	9.4
MEAN(%)		12.5	10.0	4.7	9.1	9.8	1.9	8.6	3.8	5.7	20.9	14.3	11.1	13.4	13.2	10.1	15.5	14.5	14.1

Table 6.8.12: Fitting error (imaginary Y-parameter) table for 20KÅ UTM symmetric inductors (W = 15μm).

Target Parameter		Fitting Error (Real Y-parameter)																	
		Width = 30um									Width = 30um with center-tap								
	N	1	1	1	3	3	3	5	5	5	1	1	1	3	3	3	5	5	5
	R	65	90	150	65	90	150	65	90	150	65	90	150	65	90	150	65	90	150
Y11(%)		8.3	3.8	5.0	3.1	2.8	3.7	2.9	3.9	5.2	16.8	11.4	9.6	8.5	10.1	12.3	17.3	17.9	17.6
Y21(%)		8.4	3.8	5.1	3.2	2.9	3.8	3.2	4.2	5.5	43.3	37.3	17.4	30.1	31.7	28.3	37.2	33.8	26.9
Y12(%)		8.3	3.8	5.0	3.3	3.0	3.9	3.0	4.0	5.4	44.8	39.1	19.7	30.5	32.1	28.4	37.4	33.8	26.9
Y22(%)		8.3	3.8	5.0	3.1	2.8	3.6	2.9	3.9	5.2	28.0	24.6	15.7	7.4	7.6	10.6	16.2	17.2	17.1
MEAN(%)		8.3	3.8	5.0	3.2	2.9	3.8	3.0	4.0	5.3	33.2	28.1	15.6	19.1	20.4	19.9	27.0	25.7	22.1

Table 6.8.13: Fitting error (real Y-parameter) table for 20KÅ UTM symmetric inductors (W = 30 μm).

Target Parameter		Fitting Error (Imag Y-parameter)																	
		Width = 30um									Width = 30um with center-tap								
	N	1	1	1	3	3	3	5	5	5	1	1	1	3	3	3	5	5	5
	R	65	90	150	65	90	150	65	90	150	65	90	150	65	90	150	65	90	150
Y11(%)		13.3	8.2	8.4	4.5	3.6	3.8	3.1	1.4	1.4	8.9	5.8	8.5	6.7	7.4	7.9	13.0	13.0	12.5
Y21(%)		13.3	8.3	8.6	4.4	3.5	3.6	3.0	1.6	2.1	20.1	22.3	11.0	26.1	28.0	28.0	33.7	32.4	26.9
Y12(%)		13.3	8.2	8.5	4.5	3.6	3.7	3.0	1.6	2.1	19.8	21.4	10.7	26.3	27.6	28.0	33.7	32.5	26.9
Y22(%)		13.3	8.2	8.4	4.5	3.7	3.8	3.0	1.4	1.4	12.5	11.5	8.0	7.7	6.5	7.8	12.8	12.8	12.3
MEAN(%)		13.3	8.2	8.5	4.5	3.6	3.7	3.0	1.5	1.7	15.4	15.2	9.5	16.7	17.4	18.0	23.3	22.7	19.6

Table 6.8.14: Fitting error (imaginary Y-parameter) table for 20KÅ UTM symmetric inductors (W = 30μm).

Target Parameter		Fitting Error (Real Y-parameter)																					
		Width = 6um						Width = 9um					Width = 15um					Width = 30um					
	N	1.5	3.5	5.5	1.5	3.5	5.5	1.5	5.5	1.5	3.5	5.5	1.5	3.5	1.5	3.5	5.5	1.5	3.5	5.5	1.5	3.5	5.5
	R	60	60	60	120	120	120	60	60	120	120	120	60	60	120	120	120	60	60	60	120	120	120
Y11(%)		7.4	2.2	7.2	7.4	4.6	6.1	7.0	7.8	6.8	4.0	3.9	14.1	8.9	5.3	7.0	7.7	5.5	14.0	13.1	5.2	12.3	13.0
Y21(%)		7.4	2.3	7.3	7.4	4.8	6.2	7.0	7.8	6.7	4.2	3.9	14.0	9.0	5.3	7.2	7.9	5.6	14.2	13.4	5.6	12.2	13.2
Y12(%)		7.4	2.3	7.3	7.4	4.8	6.2	7.0	7.9	6.8	4.2	4.0	14.1	9.2	5.4	7.3	8.0	5.6	14.0	13.2	5.4	11.9	12.8
Y22(%)		7.4	2.4	7.3	7.4	4.7	6.1	7.0	7.8	6.8	4.0	3.7	14.1	8.9	5.3	7.2	7.7	5.5	13.9	12.8	5.3	11.8	12.4
MEAN(%)		7.4	2.3	7.3	7.4	4.7	6.1	7.0	7.8	6.8	4.1	3.9	14.1	9.0	5.3	7.2	7.8	5.6	14.0	13.1	5.4	12.1	12.9

Table 6.8.15: Fitting error (real Y-parameter) table for 40KÅ UTM standard inductors.

Target Parameter		Fitting Error (Imag Y-parameter)																					
		Width = 6um						Width = 9um					Width = 15um					Width = 30um					
	N	1.5	3.5	5.5	1.5	3.5	5.5	1.5	5.5	1.5	3.5	5.5	1.5	3.5	1.5	3.5	5.5	1.5	3.5	5.5	1.5	3.5	5.5
	R	60	60	60	120	120	120	60	60	120	120	120	60	60	120	120	120	60	60	60	120	120	120
Y11(%)		11.2	2.3	1.8	15.9	2.6	0.7	5.5	0.9	5.1	2.9	1.2	6.3	2.5	9.2	1.4	0.6	3.2	2.3	1.4	3.7	1.5	0.6
Y21(%)		11.3	3.6	3.3	15.9	4.6	3.9	5.6	2.5	6.6	4.5	3.5	6.7	3.8	9.2	2.4	1.9	3.3	2.3	1.3	3.9	1.8	0.7
Y12(%)		11.3	3.6	3.4	16.0	4.6	3.9	5.6	2.6	6.6	4.5	3.5	6.7	3.8	9.2	2.4	1.9	3.3	2.3	1.3	3.9	1.8	0.7
Y22(%)		11.2	2.3	1.8	15.9	2.5	0.4	5.5	0.9	5.1	2.8	0.9	6.3	2.4	9.2	1.5	0.6	3.2	2.3	1.3	3.7	1.4	0.5
MEAN(%)		11.3	2.9	2.6	15.9	3.6	2.2	5.6	1.7	5.8	3.7	2.2	6.5	3.1	9.2	1.9	1.2	3.3	2.3	1.4	3.8	1.6	0.6

Table 6.8.16: Fitting error (imaginary Y-parameter) table for 40KÅ UTM standard inductors.

Target Parameter		Fitting Error (Real Y-parameter)															
		Width = 9um					Width = 15um						Width = 30um				
	N	1.0	3.0	1.0	3.0	5.0	1.0	3.0	5.0	1.0	3.0	5.0	3.0	5.0	1.0	3.0	5.0
	R	65	65	120	120	120	65	65	65	120	120	120	65	65	120	120	120
Y11(%)		16.4	1.6	8.3	2.9	14.5	7.8	2.7	16.9	27.3	4.8	11.3	11.3	15.7	16.3	5.9	17.4
Y21(%)		16.4	1.5	8.3	2.8	14.5	7.8	2.7	17.2	27.4	4.8	11.4	11.4	16.0	16.4	5.9	18.7
Y12(%)		16.4	1.5	8.3	2.8	14.7	7.9	2.7	17.2	27.3	4.9	11.4	11.4	16.2	16.3	6.1	18.6
Y22(%)		16.4	1.6	8.3	2.9	14.5	7.8	2.7	16.9	27.4	4.8	11.3	11.3	15.7	16.3	5.8	17.5
MEAN(%)		16.4	1.6	8.3	2.8	14.5	7.8	2.7	17.0	27.4	4.8	11.4	11.4	15.9	16.3	5.9	18.1

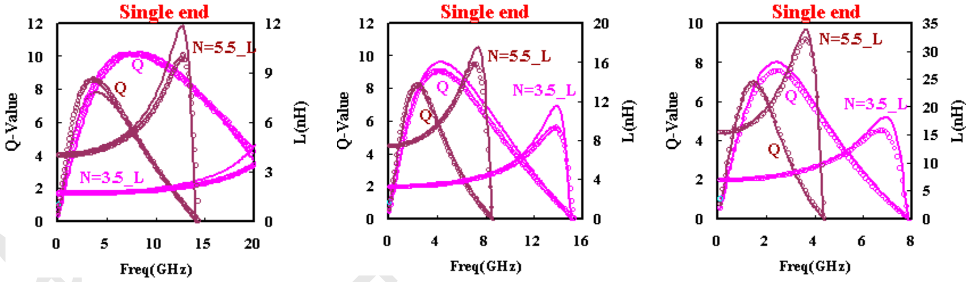
Table 6.8.17: Fitting error (real Y-parameter) table for 40KÅ UTM symmetric inductors.

Target Parameter		Fitting Error (Imag Y-parameter)															
		Width = 9um					Width = 15um						Width = 30um				
	N	1.0	3.0	1.0	3.0	5.0	1.0	3.0	5.0	1.0	3.0	5.0	3.0	5.0	1.0	3.0	5.0
	R	65	65	120	120	120	65	65	65	120	120	120	65	65	120	120	120
Y11(%)		23.5	0.9	11.8	3.4	2.1	9.8	3.0	1.2	8.3	0.5	0.7	0.7	1.3	7.4	0.6	1.3
Y21(%)		23.6	0.7	11.9	3.8	2.2	9.8	3.0	1.0	8.4	0.8	0.8	0.8	0.5	7.5	0.6	0.8
Y12(%)		23.6	0.7	11.9	3.8	2.2	9.8	3.0	1.0	8.4	0.8	0.7	0.7	0.5	7.5	0.6	0.8
Y22(%)		23.6	0.9	11.8	3.5	2.1	9.8	3.0	1.2	8.3	0.5	0.7	0.7	1.4	7.4	0.6	1.4
MEAN(%)		23.6	0.8	11.9	3.6	2.1	9.8	3.0	1.1	8.3	0.7	0.7	0.7	0.9	7.4	0.6	1.1

Table 6.8.18: Fitting error (imaginary Y-parameter) table for 40KÅ UTM symmetric inductors.

6.8.8 Device Characteristics

W = 6 μm 20KÅ UTM Standard Inductor Fitting Results

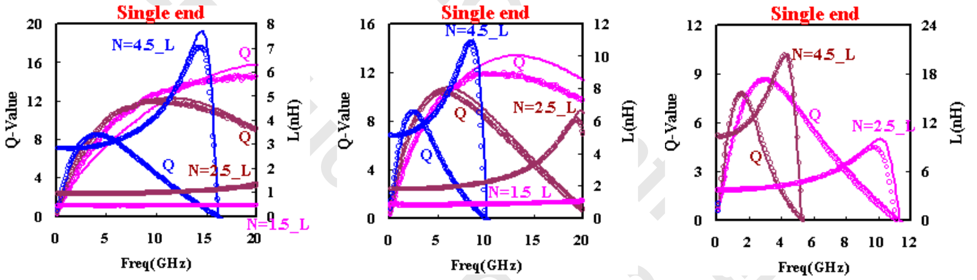


(a) (b) (c)

Circle : Measured
Line : Simulated

Figure 6.8.6: Measured and simulated data of Q and L (a) R=31 μm, (b) R=61 μm, (c) R=121 μm

W = 9 μm 20KÅ UTM Standard Inductor Fitting Results

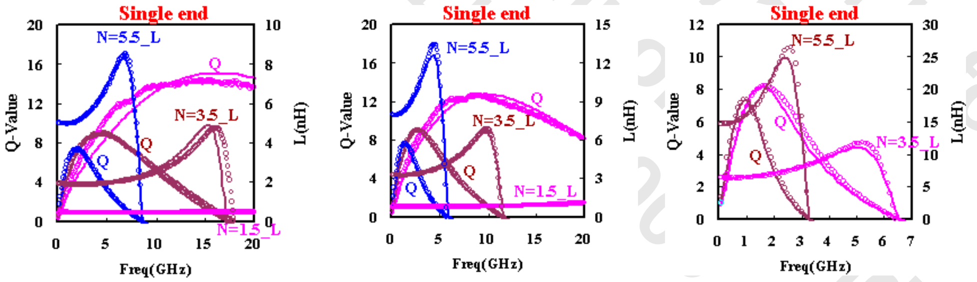


(a) (b) (c)

Circle : Measured
Line : Simulated

Figure 6.8.7:Measured and simulated data of Q and L (a) R=31.4 μm, (b) R=61.4 μm, (c) R=121.4 μm

W = 15 μm 20KÅ UTM Standard Inductor Fitting Results

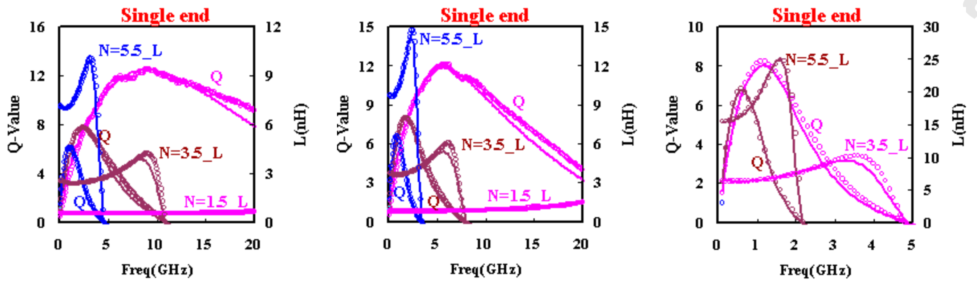


(a) (b) (c)

Circle : Measured
Line : Simulated

Figure 6.8.8:Measured and simulated data of Q and L (a) R=32.1 μm, (b) R=62.1 μm, (c) R=122.1 μm

W = 30 μm 20KÅ UTM Standard Inductor Fitting Results

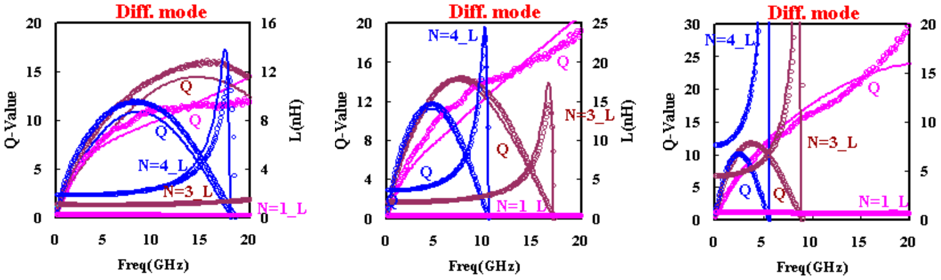


(a) (b) (c)

Circle : Measured
Line : Simulated

Figure 6.8.9:Measured and simulated data of Q and L (a) R=34.1 μm, (b) R=64.1 μm, (c) R=124.1 μm

W = 9 µm 20KÅ UTM Symmetric Inductor Fitting Results

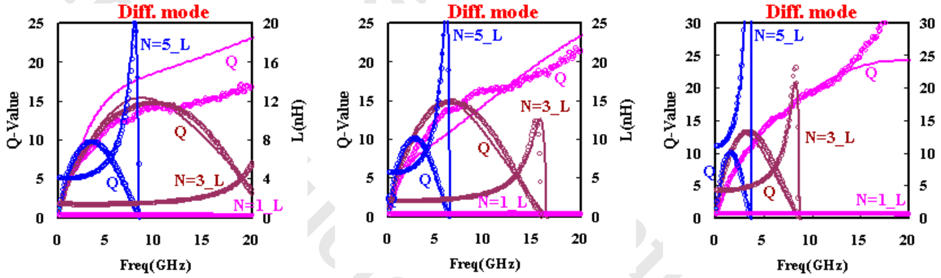


Circle : Measured
Line : Simulated

(a) (b) (c)

Figure 6.8.10: Measured and simulated data of Q and L (a) R=30 µm, (b) R=60 µm, (c) R=120 µm

W = 15 µm 20KÅ UTM Symmetric Inductor Fitting Results

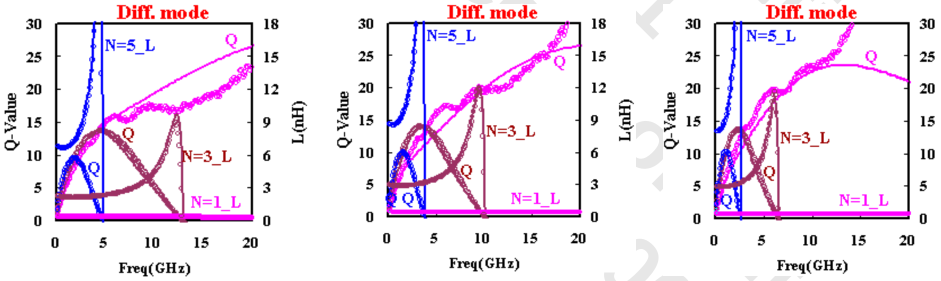


Circle : Measured
Line : Simulated

(a) (b) (c)

Figure 6.8.11: Measured and simulated data of Q and L (a) R=40 µm, (b) R=60 µm, (c) R=120µm

W = 30 µm 20KÅ UTM Symmetric Inductor Fitting Results

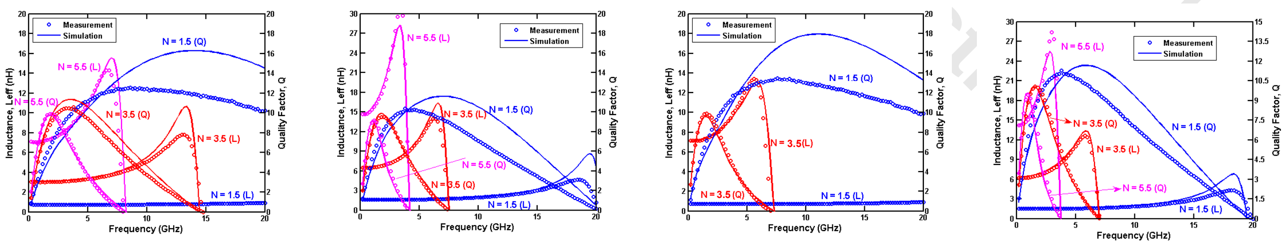


Circle : Measured
Line : Simulated

(a) (b) (c)

Figure 6.8.12: Measured and simulated data of Q and L (a) R=65 µm, (b) R=90 µm, (c) R=150µm

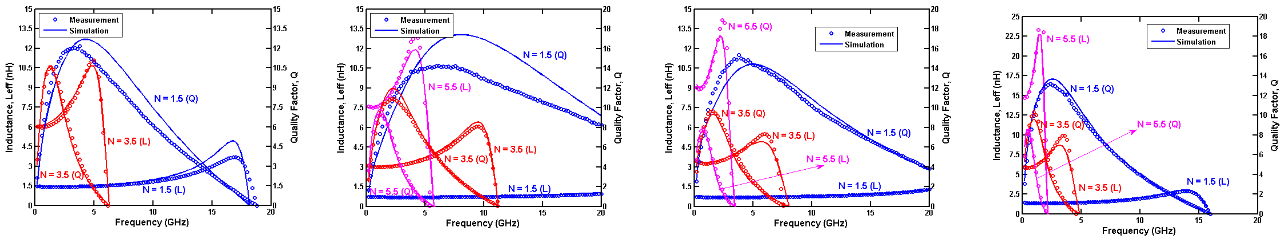
W = 6µm and 9µm, 40KÅ UTM Standard Inductor single-ended Fitting Results



(a) (b) (c) (d)

Figure 6.8.13: Measured and simulated data of Q and L (a) W=6µm R=60µm, (b) W=6µm R=120µm, (c) W=9µm R=60µm, (d) W=9µm R=120µm

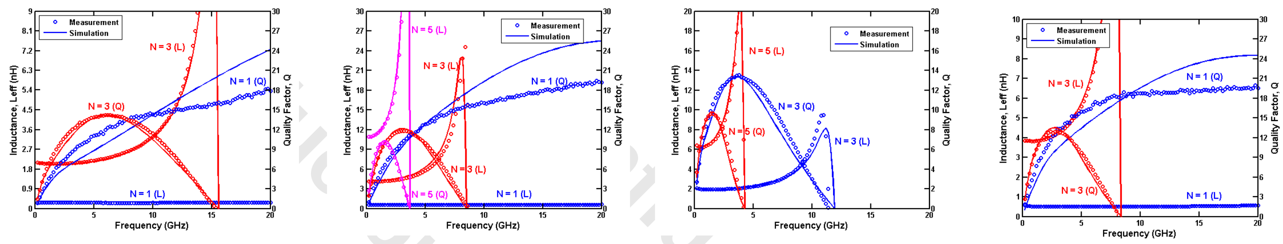
W = 15 μm and 30 μm, 40KÅ UTM Standard Inductor single-ended Fitting Results



(a) (b) (c) (d)

Figure 6.8.14: Measured and simulated data of Q and L (a) W=15μm R=60μm, (b) W=15μm R=120μm, (c) W=30μm R=60 μm, (d) W=30μm R=120μm

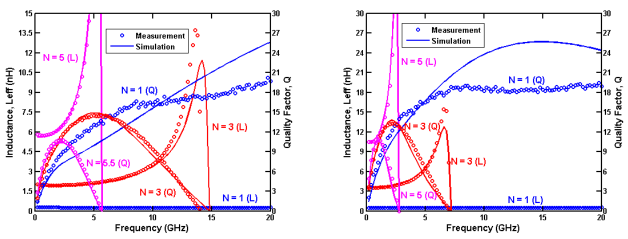
W = 9 μm and 15μm, 40KÅ UTM Symmetric Inductor Differential Fitting Results



(a) (b) (c) (d)

Figure 6.8.15: Measured and simulated data of Q and L (a) W=9μm R=65μm, (b) W=9μm R=120μm, (c) W=15μm R=65 μm, (d) W=15μm R=120μm

W = 30μm 40KÅ UTM Symmetric Inductor Differential Fitting Results



(a) (b)

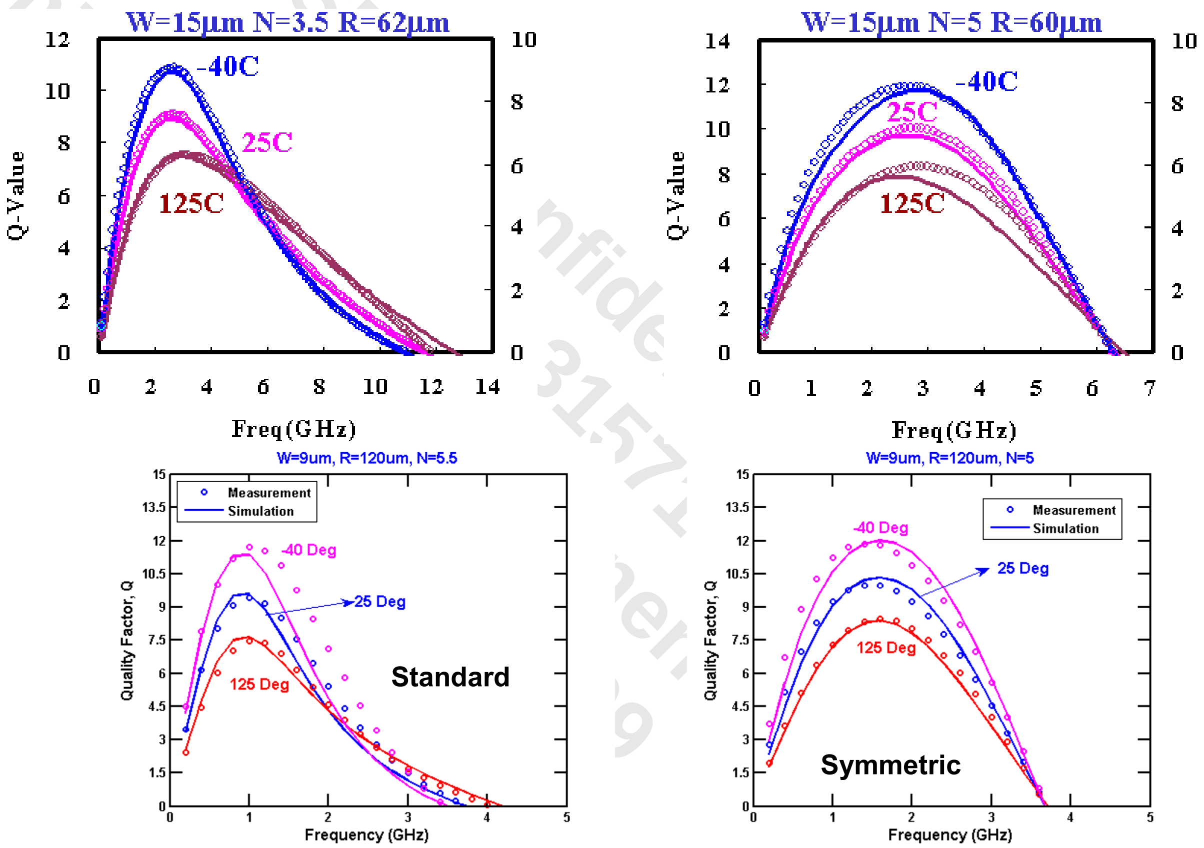
Figure 6.8.16: Measured and simulated data of Q and L (a) W=30μm R=65μm, (b) W=30μm R=120μm.

6.8.9 Temperature Effect Model

Temperature effect was analyzed through characterization of S-parameters. Two types of inductors (standard and symmetric inductor) were measured at three different temperatures (-40C, 25C, and 125C). Temperature effect is handled with the two equations below.

R(T)=R*(0.003286*(temp-25)+1)
Rsub(T)=Rsub*(0.000027*(temp-25)*(temp-25)+0.00644586*(temp-25)+1)

Variation of Q with temperature is attributed to spiral metal resistance and substrate resistance. The spiral metal has a positive TCR, which increases resistance with the temperature. It decreases the Q-value. Although substrate resistance also has a positive temperature coefficient, it enhances Q-value at high frequency. Figure 6.8.16 shows the simulated and measured data at three different temperatures.



Circle: Measured; Line: Simulated

Figure 6.8.16: (a) 20KÅ UTM Standard inductor (b) 20KÅ UTM Symmetric inductor (c) 40KÅ UTM Standard inductor (d) 40KÅ UTM Symmetric inductor