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CMOS RF-ID Design

A Thesis

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Submitted by

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STATEMENT

This dissertation is submitted to Ain Shams University for the degree of Master of Science in Electrical Engineering (Electronics and Communications Engineering).

The work included in this thesis was carried out by the author at the Electronics and Communications Engineering Department, Faculty of Engineering, Ain Shams University, Cairo, Egypt.

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ABSTRACT

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This dissertation demonstrates the design of a CMOS RFID. It begins with an introduction to RFID. The RFID is compared to the other identification techniques. The main features, types, and standards of RFID are discussed.

Next, it presents a design of UHF RFID tag. The system architecture and the communication protocol are explained, and the circuit design of the UHF RFID tag in CMOS technology is presented. The main blocks of the RFID tag are analyzed, designed, and simulated.

Finally, the system design of an inductively coupled RFID tag for temperature sensing is presented. The system architecture and the communication protocol are explained, and the circuit design of the inductively coupled RFID tag for temperature sensing in CMOS technology is presented. The main blocks of the RFID tag are analyzed, designed, and simulated.

Key words: CMOS, RFID, rectifier, inductive link, UHF, telemetry, medical.

SUMMARY

This dissertation demonstrates the different issues of implementing RFID in CMOS technology. The dissertation is divided into five chapters organized as follows:

Chapter One: This chapter is an introduction to RFID. The RFID is compared to the other identification techniques. The main features, types, and standards of RFID are discussed.

Chapter Two: In this chapter, the system design of a UHF RFID tag is presented. The system architecture and the communication protocol are explained.

Chapter Three: In this chapter, the circuit design of the UHF RFID tag in CMOS technology is presented. The main blocks of the RFID tag are analyzed, designed, and simulated.

Chapter Four:

In this chapter, the system design of an inductively coupled RFID tag for temperature sensing is presented. The system architecture and the communication protocol are explained.

Chapter Five:

In this chapter, the circuit design of the inductively coupled RFID tag for temperature sensing in CMOS technology is presented. The main blocks of the RFID tag are analyzed, designed, and simulated.

Finally, the thesis ends by extracting conclusions and stating future work that might be done based on this work.

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List of Symbols

A	Voltage gain of the OTA
C_{env}	Capacitance of the envelope detector
C_g	Input capacitance of the OTA
$C_{gs,D1}$	Capacitance of the envelope diode
C_{int}	Integrator capacitor
C_L	Load capacitance
C_m	Miller capacitance
C_{osc}	Oscillator capacitor
C_{ox}	Gate oxide capacitance per unit area
C_p	Total capacitance at the output node of the OTA
DC_{in}	Input DC voltage to the rectifier cell
DC_{out}	Output DC voltage from the rectifier cell
f	Frequency
g_m	Transconductance of the transistor
$g_{m,int}$	Effective transconductance of the integrator
I_d	Diode Current
I_{dc}	Output DC current
I_{int}	Integrator current
I_n	Peak value of the negative current pulse
I_{osc}	Oscillator current
I_p	Peak value of the positive current pulse
I_{ptat}	Generated PTAT current
I_{ref}	Generated constant current
I_s	Reverse saturation current
k_B	Boltzmann constant
L	Transistor length
n	Order of the transfer function

P_1	Dominant pole
P_2	Non-dominant pole
P_{dc}	Output DC power
P_{dis}	Dissipated power in the transistor
P_{leak}	Leakage power
P_n	Dissipated power in the negative current pulse
P_p	Dissipated power in the positive current pulse
P_{rf}	Available RF signal power
Q_{in}	Input charge transferred to the rectifier in one cycle.
Q_{out}	Output charge transferred to the rectifier in one cycle.
R_{ant}	Input resistance of the antenna
r_e	Equivalent small signal resistance at the emitter of the BJT
R_{env}	Resistance of the envelope detector
R_{in}	Input resistance of the chip
$R_{in,demod}$	Input resistance of the demodulator
$R_{in,rect}$	Input resistance of the rectifier
R_{int}	Leakage resistance of the integrator
R_n	Resistance in CTAT loop
r_o	Output resistance of the transistor
r_{ota}	Output resistance of the OTA
R_{out}	Output resistance
R_p	Resistance in PTAT loop
s_k	Continuous time pole in s-domain
SNR_{th}	The SNR due to thermal noise only
t	Time
T	Period of the input signal
T_b	Width of the RF signal gap
T_{build}	Voltage Build-up time
T_{hi}	Width of pulse at logic ‘1’
T_{lo}	Width of pulse at logic ‘0’
T_n	Width of the negative current pulse

T_{osc}	The period of the generated square wave.
t_p	Width of the triangular leakage current pulse
T_p	Width of the positive current pulse
t_r	Rise time of the clock
T_s	Sampling period
V_{bd}	Breakdown voltage of the transistor
V_{be}	Voltage across the p-n junction
V_d	Voltage across the diode
V_{dc}	Output DC voltage of the rectifier
$V_{dc,single}$	DC voltage generated from a single rectifier cell
Vdd	Positive supply voltage
$Vdda$	Positive analog supply voltage
$Vddd$	Positive digital supply voltage
V_{in}	Input voltage of the rectifier
$V_{int,hi}$	The output of the integrator at logic '1'
$V_{int,lo}$	The output of the integrator at logic '0'
V_m	Output voltage from the envelope detector
V_n	Total integrated output noise voltage
v_n^2	The mean square of the noise voltage
V_p	Peak of the input signal.
V_r	Ripple Voltage
Vss	Negative supply voltage
$Vssa$	Negative analog supply voltage
$Vssd$	Negative digital supply voltage
V_T	Thermal voltage
V_{th}	Threshold voltage
V_{tn}	Threshold voltages of the NMOS transistor
V_{tp}	Threshold voltages of the PMOS transistor
W	Transistor width
z_k	Discrete time pole in z-domain
γ	MOSFET noise parameter

ΔV	swing of the signal voltage amplitude at the integrator output
ΔV_{env}	Voltage drop due to the RF signal gap
η	Conversion efficiency
θ	Start angle of the positive current pulse
λ	Sub-threshold channel length modulation parameter.
μ_n	Electron mobility
μ_p	Hole mobility
ω	Radian frequency
ω_{int}	The cut-off frequency of the integrator

List of Abbreviations

AC	Alternating Current
ADC	Analog to Digital Converter
ASK	Amplitude Shift Keying
BW	Bandwidth
CMOS	Complementary Metal-Oxide-Semiconductor
CT	Continuous Time
CTAT	Complementary-To-Absolute-Temperature
DC	Direct Current
DT	Discrete Time
EAS	Electronic Article Surveillance
EPC	Electronic Product Code
HF	High Frequency
ICC	Integrated Circuit Card
ISM	Industrial Scientific Medical
ISO	International Organization for Standardization
LF	Low Frequency
LG	Loop Gain
MEMS	Micro-Electro-Mechanical Systems
MOS	Metal-Oxide-Semiconductor
MOSFET	Metal-Oxide-Semiconductor Field Effect Transistor
NMOS	N-channel Metal-Oxide-Semiconductor
OCR	Optical Character Recognition
OTA	Operational Transconductance Amplifier
PLL	Phase Locked Loop
PM	Phase Margin
PMOS	P-channel Metal-Oxide-Semiconductor
POR	Power On Reset
PSD	Power Spectral Density

PSK	Phase Shift Keying
PTAT	Proportional-To-Absolute-Temperature
PWM	Pulse Width Modulation
RF	Radio Frequency
RFID	Radio Frequency Identification
SNR	Signal to Noise Ratio
UHF	Ultra High Frequency

Thesis Objective

The objective of this thesis is to explore the RFID technology and demonstrate the design of the RFID tag, which is the challenging part of the RFID system. To achieve this target, the thesis introduces the RFID main features, parameters, applications, and standards. Then the thesis demonstrates the design of the RFID tags by presenting two case studies. The first case study is the design of a passive ultra low power UHF RFID tag. And the second case study is the design of a passive HF RFID temperature sensor.

The thesis consists of three main Parts:

Part I: Introduction.

- Chapter 1: Provides an introduction to RFID.

Part II: UHF RFID tag case study.

- Chapter 2: Presents the system design of the UHF RFID tag.
- Chapter 3: Presents the circuit implementation of the UHF RFID tag.

Part III: HF RFID temperature sensor case study.

- Chapter 4: Presents the system design of the HF RFID temperature sensor.
- Chapter 5: Presents the circuit implementation of the HF RFID temperature sensor.

Chapter 1

Introduction

This chapter begins with an overview over the various types of the automatic identifications systems. Next, it summarizes the history of RFID (Radio Frequency Identification). Finally, it discusses the main features, types, and standards of RFID.

1.1 Automatic Identification Systems

Automatic identification is defined as the identification of objects, animals, and persons with little dependence on the human senses. The automatic identification systems differ according to the technology used and the target application. In the following subsections the main types of automatic identification systems are summarized.

Barcode

A barcode is a machine-readable representation of information (usually dark ink on a light background to create high and low reflectance which is converted to 1s and 0s),

[Wikipedia]. Originally, barcodes stored data in the widths and spacings of printed parallel lines as shown in Figure 1.1, but today they also come in patterns of dots, concentric circles, and text codes hidden within images. Barcodes can be read by optical scanners called barcode readers or scanned from an image by special software.

Figure 1.1: Barcode Example, [www.idautomation.com].

While traditionally barcode encoding schemes represented only numbers, newer versions add new characters such as the uppercase alphabet to the complete ASCII character set and beyond.

To encode more information in the same limited space, another version of the barcode was developed which is the 2D barcode. The 2D barcode do not consist of bars but rather a grid of square cells as shown in Figure 1.2.

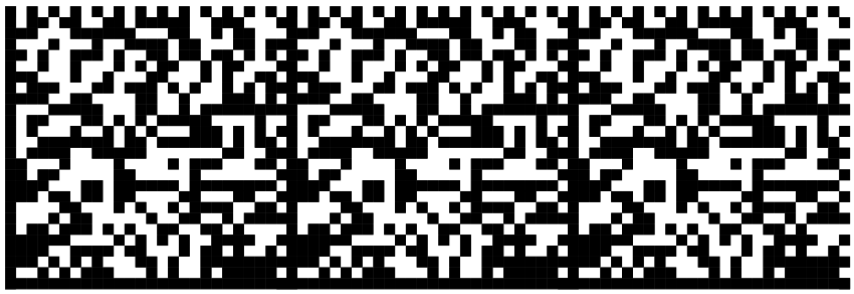


Figure 1.2: 2D barcode, [Wikipedia].

Barcode still has the lower cost among the ID systems. It will cost about US$0.005 to implement a barcode compared to passive RFID which still costs about US$0.07 to US$0.30 per tag, [Wikipedia]. For this reason, barcode has successfully held its own against other identification systems over the past 20 years.

1.1.2 OCR

Optical character recognition, usually abbreviated to OCR, is the mechanical or electronic translation of images of handwritten or typewritten text (usually captured by a scanner) into machine-editable text, [Wikipedia].

Early systems required training (the provision of known samples of each character) to read a specific font as shown in Figure 1.3. "Intelligent" systems with a high degree of recognition accuracy for most fonts are now common. Some systems are even capable of reproducing formatted output that closely approximates the original scanned page including images, columns and other non-textual components.

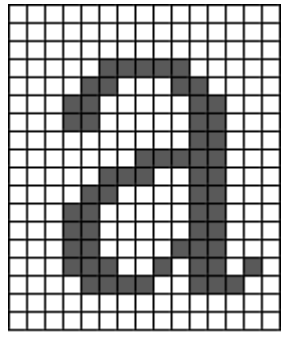


Figure 1.3: OCR special font, [www.toniksupport.co.uk].

1.1.3 Biometrics

Biometrics is the study of methods for uniquely recognizing humans based upon one or more intrinsic physical or behavioral traits. Biometric characteristics can be divided in two main classes, as illustrated in Figure 1.4.

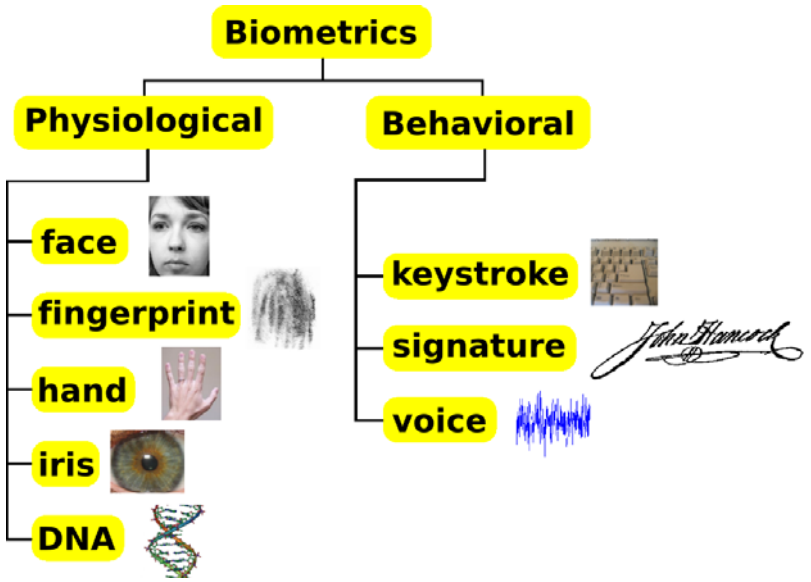


Figure 1.4: Biometric classes, [Wikipedia].

1.1.4 Smart Cards

A smart card, chip card, or integrated circuit card (ICC), is defined as any pocket-sized card with embedded integrated circuits which can process information, [Wikipedia]. A photo of a smart card is shown in Figure 1.5.

Figure 1.5: Smart card, [Wikipedia].

The first smart cards in the form of prepaid telephone smart cards were launched in 1984. Smart cards are placed in a reader, which makes a galvanic connection to the contact surfaces of the smart card using contact springs. The smart card is supplied with energy and a clock pulse from the reader via the contact surfaces.

The main advantage of the smart card is the fact that the data stored on it can be protected against undesired (read) access and manipulation. Smart cards make all services that relate to information or financial transactions simpler, safer and cheaper. The main disadvantage of contact-based smart cards is the vulnerability of the contacts to corrosion and dirt. Readers that are used frequently are expensive to maintain due to their tendency to malfunction.

1.1.5 RFID

Radio-frequency identification (RFID) is an automatic identification method, relying on storing and remotely retrieving data using devices called RFID tags or transponders, [Wikipedia]. The typical RFID system comprises one or few readers that communicate with many tags as shown in Figure 1.6. The RFID tag can be stuck on or incorporated into a product, animal, or person for the purpose of identification using radio waves. Some tags can be read from several meters away and beyond the line of sight of the reader.

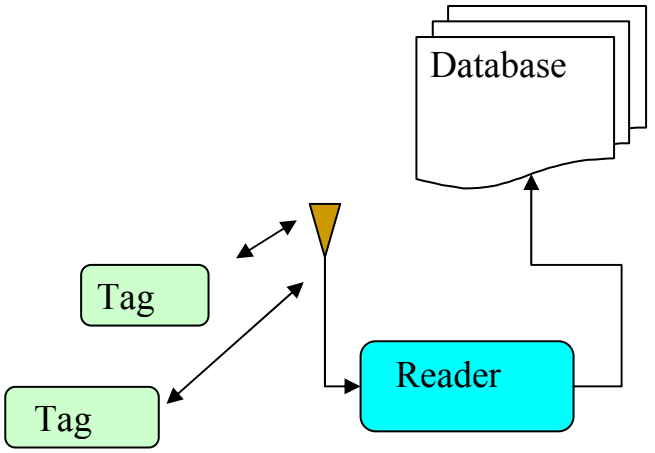


Figure 1.6: RFID system.

RFID systems are very close to the smart cards. Like smart card systems, data is stored on an electronic chip. But, unlike the smart card, the power supply to the chip is achieved without the use of batteries. The power supply is achieved using the RF wave supplied by the RFID reader.

Due to the numerous advantages of RFID systems compared with other identification systems, RFID systems are now beginning to conquer new mass markets. One example is the use of contactless smart cards as tickets for short-distance public transport.

1.1.6 Comparison

As a summary of the previous subsections, a brief comparison between the main types of automatic identification systems is shown in Table 1-1. It can be deduced from the comparison, that RFID has the fastest reading speed and the longest reading distance, which are the main advantages of the RFID.

Table 1-1: Comparison between automatic ID systems.

	Barcode	**OCR**	**Biometry**	**Smart card**	**RFID**
Data quantity (bytes)	1-100	1-100	-	16-64k	16-64k
Readability by machines	Good	Good	Expensive	Good	Good
Readability by people	Limited	Simple	Difficult	Impossible	Impossible
Effect of dirt	High	High	-	possible	No effect
Security	Poor	Poor	Good	Good	Good
Reading speed	Low	Low	Very low	Low	very fast
Reading distance	0-50 cm	0-1 cm	Direct contact	Direct contact	0-10m

1.2 History of RFID

Although the wide scale deployment of RFID technology started in 1990s, the origin of RFID is much earlier. In the following subsections, the evolution history of RFID technology is summarized.

1.2.1 The origin of RFID (1940s)

The concept of identification by means of reflected radio waves was first used in radar, which was invented in 1922, [Landt, 06]. Radar sends out radio waves for detecting and locating an object by the reflection of the radio waves. This reflection can determine the position and speed of an object. At that stage the radar was not intelligent enough to identify the object. The work in radar during World War II was the major step in RFID history. In 1939 the first RFID system was used to identify airplanes. It was named IFF (Identify Friend or Foe). IFF was a tag and track (i.e: to tag an object

and track its movement) technique used by the British allies to identify whether airplanes were friend or foe [Eunni, 06].

The first known paper that can be classified under RFID is the paper published by Harry Stockman, "Communication by Means of Reflected Power," Proceedings of the IRE, pp1196-1204, October 1948, [Landt, 06]. Thirty years would pass before Harry's vision would begin to reach fruition. Other developments were needed: the transistor, the integrated circuit, the microprocessor, development of communication networks, changes in ways of doing business.

1.2.2 RFID Explosion (1960s)

The 1960s were the prelude to the RFID explosion of the 1970s. R. F. Harrington studied the electromagnetic theory related to RFID in his papers "Field measurements using active scatterers" and "Theory of loaded scatterers" in 1963 and 1964, respectively. Inventors were busy with RFID related inventions such as Robert Richardson's "Remotely activated radio frequency powered devices" in 1963.

Commercial activities were beginning in the 1960s. Some companies developed electronic article surveillance (EAS) equipment to counter theft. These types of systems often use '1-bit' tags – only the presence or absence of a tag could be detected, but the tags could be made inexpensively and provided effective anti-theft measures. These types of systems used either microwave or inductive technology.

In the 1970s developers, inventors, companies, academic institutions, and government laboratories were actively working on RFID. Notable advances were being realized at research laboratories and academic institutions. Large companies were also developing RFID technology. The 1970's were characterized primarily by developmental work. Intended applications were for animal tracking, vehicle tracking, and factory automation.

1.2.3 RFID Full Implementation (1980s)

The 1980s became the decade for full implementation of RFID technology, though interests developed somewhat differently in various parts of the world. The greatest interests in the United States were for transportation, personnel access, and to a lesser extent, for animals. In Europe, the greatest interests were for short-range systems for animals, industrial and business applications.

The 1990's were a significant decade for RFID since it saw the wide scale deployment of electronic toll collection in the United States. Important deployments included several innovations in electronic tolling.

For the first time, useful microwave Schottky diodes were fabricated on a regular CMOS integrated circuit. This development permitted the construction of microwave RFID tags that contained only a single integrated circuit, a capability previously limited to inductively-coupled RFID transponders.

With the growing interest of RFID into the item management work and the opportunity for RFID to work along side bar code, it becomes difficult in the later part of this decade to count the number of companies that enter the marketplace.

1.2.4 RFID History Summary

Table 1-2 summarizes the history of RFID.

Table 1-2: Decades of RFID

Decade	Main RFID event
1940s	RFID for military applications (IFF)
1950s	RFID laboratory experiments
1960s	Mature theory of RFID
1970s	RFID entered industry
1980s	Commercial applications
1990s	Wide deployment of RFID

1.3 RFID Applications

It is very difficult to find any field in our daily life where RFID cannot be applied. The applications of RFID are bounded only by human imagination. Whenever identification is needed, RFID is always the best choice. In the following subsections, some popular applications of RFID are summarized.

1.3.1 Contactless Smart Cards

RFID has enhanced the technology of smart cards. The contactless smart cards require only close proximity to an antenna to complete transaction. They are often used when transactions must be processed quickly or hands-free, such as on mass transit systems, where smart cards can be used without even removing them from a wallet, [Wikipedia]

1.3.2 Electronic Barcodes

The main commercial RFID application is replacing the conventional barcodes, introducing what is known as electronic product code (EPC). EPC has many important advantages over the older barcode technology. However, EPC may not ever completely replace barcodes, mainly due to its higher cost, [Hard, 06].

1.3.3 Telemetry

RFID tags can be used as low-cost remote sensors that broadcast telemetry back to a base station (RFID reader).

1.3.4 Patient identification

The record of the patient can be programmed on an RFID tag that can be attached to or even implanted in the patient.

1.3.5 RFID in libraries

This application is very similar to the electronic product code. This technology has slowly begun to replace the traditional barcodes on library items (books, CDs, DVDs, etc.). Samples of such tags are shown in Figure 1.7. However, the RFID tag can contain identifying information, such as a book title or material type, without having to be pointed to a separate database. The information is read by an RFID reader, which replaces the standard barcode reader commonly found at a library circulation desk.

Figure 1.7: RFID tags used in libraries, [Wikipedia].

1.3.6 Access Control

Electronic access control systems using data carriers are used to automatically check the access authorization of individuals to buildings, (commercial or event) premises, or individual rooms.

1.3.7 Animal Identification

Electronic identification systems have been used in stock keeping for almost 20 years. In addition to internal applications for automatic feeding and calculating productivity, these systems can also be used in inter-company identification, for the control of epidemics, quality assurance, and for tracing the origin of animals.

1.3.8 Human implants

Implantable RFID chips designed for animal tagging are now being used in humans, [Huang, 98]. An early experiment with RFID implants was conducted by British professor of cybernetics Kevin Warwick, who implanted a chip in his arm in 1998, [Wikipedia].

1.4 RFID Features

In this section the main features and parameters that characterize the RFID system are discussed. Some of these features are related to the whole RFID system while others are related to only the RFID tag.

1.4.1 Active and Passive RFID Tags

Based on the power source that is used to power the RFID tag, the RFID tags can be categorized into 3 main types: Passive, Semi-Passive, and Active, [Lewis, 04].

Passive tags use the reader field as a source of energy for the chip and for communication from and to the reader. The available power from the reader field, not only reduces very rapidly with distance, but is also controlled by strict regulations, resulting in a limited communication distance of 4 - 5m

Semi-Passive (battery assisted backscatter) tags have built in batteries and therefore do not require energy from the reader field to power the chip. This allows them to

function with much lower signal power levels, resulting in greater distances of up to 100 meters. Distance is limited mainly due to the fact that tag does not have an integrated transmitter, and is still obliged to use the reader field to communicate back to the reader.

Active tags are battery powered devices that have an active transmitter onboard. Unlike passive tags, active tags generate RF energy and apply it to the antenna. This autonomy from the reader means that they can communicate at distances of over several kilometers.

The main differences between the above mentioned types of RFID tags are summarized in Table 1-3.

Table 1-3: RFID tags comparison.

	Passive	**Semi-Passive**	**Active**
Battery	not needed	needed	needed
Life time	Long	medium	Short
communication distance	short (~ 1m)	medium (~ 100m)	long (~ 1km)
Reliability	Reliable	Less reliable	
Cost	cheap	Expensive	Expensive
Power regulations	Strict	Relaxed	Relaxed
Communications	Backscattering	Backscattering	Transmitter
Applications	Barcode, Telemetry	Tracking of trains and containers	

1.4.2 RFID Tag Classes

RFID tags can be categorized according to their capability of storing the data, [Sarma, 03]. The classification of UHF RFID tags based on their operation and functionality was developed by EPCglobal. The layered class structure divides the tags from class 0 through class 4 as detailed below.

1.4.2.1 Class 0 (Read only)

These are the simplest type of tags. The data, which is usually a simple ID number is written only once into the tag during manufacturing. The memory is then disabled from any further updates. Class 0 is also used to define a category of tags called EAS (electronic article surveillance) or anti-theft devices, which have no ID, and only announce their presence when passing through an antenna field. Class 0 tags are always passive and use backscatter technique to communicate with the reader.

1.4.2.2 Class 1 (Write once)

In this case the tag is manufactured with no data written into the memory. Data can be written by the tag manufacturer or by the user – one time. Following this, no further writes are allowed and the tag can only be read. Tags of this type usually act as simple identifiers. Class 1 tags are also passive and use backscatter technique to communicate with the reader.

1.4.2.3 Class 2 (Read/Write)

This is the most flexible type of tags. Users have access to read and write data into the tags memory. They are typically used as data loggers, and therefore contain more memory space than what is needed for just a simple ID number. Class 2 tags are also passive and use backscatter technique to communicate with the reader.

1.4.2.4 Class 3 (Read/Write and battery assisted)

These tags contain on-board sensors for recording parameters like temperature, pressure, and motion, which can be recorded by writing into the tags memory. Class 3 tags are semi-passive tags that have a battery source to operate the internal circuitry. They also use backscattering for reader communication.

1.4.2.5 Class 4 (Read/Write with full transmitter)

These tags are like miniature radio devices which can communicate with other tags and devices without the presence of a reader. This means that they are completely active with their own. Class 4 tags are active tags that have a battery source to supply power to the internal circuitry. These tags are also capable of communicating with other tags that have the same technology.

Table 1-4: RFID tags classes.

Class	Name	Memory	Power	Application
0	EAS	Read only	Passive	Anti-Theft
1	EPC	Read/Write once	Passive	ID
2	EPC	Read/Write	Passive	ID
3	Sensors	Read/Write	Semi-Passive	Sensors
4	Smart Dust	Read/Write	Active	Networking

1.4.3 RFID Frequencies

There are many frequencies where RFID can operate. The frequency of RFID system is chosen mainly according to the application, [Harmon, 03]. The need to exercise care with regard to other radio services significantly restricts the range of suitable operating frequencies available to an RFID system. For this reason, it is usually only possible to use frequency ranges that have been reserved specifically for ISM (Industrial, Scientific, and Medical) applications, and they can also be used for RFID applications.

In addition to ISM frequencies, the entire frequency range below 135 kHz is also suitable, because it is possible to work with high magnetic field strengths in this range, particularly when operating inductively coupled RFID systems.

The most important frequency ranges for RFID systems are therefore 0–135 kHz and the ISM frequencies around 13.56 MHz, 915.0 MHz, and 2.45 GHz.

Choice of field or carrier wave frequency is of primary importance in determining data transfer rates. In practical terms the rate of data transfer is influenced primarily by the frequency of the carrier wave or varying field used to carry the data between the tag and its reader. Generally speaking the higher the frequency, the higher the data transfer or throughput rates that can be achieved, [AIM, 01]. In the following subsections, the main RFID frequency ranges are discussed.

1.4.3.1 Low frequency range (LF) (below 135 kHz)

The range below 135 kHz is heavily used by other radio services because it has not been reserved as an ISM frequency range. The propagation conditions in this long wave frequency range permit the radio services that occupy this range to reach areas within a radius of over 1000 km continuously at a low technical cost. The main advantages of the low frequency range are:

- Normal CMOS technology can be used easily due to the low frequency operation.
- Regulations are much relaxed than ISM bands.
- The wave can penetrate materials like water, tissue, wood, and aluminum.

But the main disadvantages of the low frequency range are:

- Low data rate compared to higher frequencies.
- Does not penetrate or transmit around metals like iron and steel.
- Large antennas compared to higher frequencies.
- Short communication range.
-The low frequency RFID tag is thicker, more expensive, and more complex compared to the high frequencies RFID tag.

1.4.3.2 High frequency range (HF) (13.56 MHz)

The range 13.553–13.567 MHz is located in the middle of the short wavelength range. The propagation conditions in this frequency range permit transcontinental connections throughout the day. This frequency range is used by a wide variety of radio services like press agencies and telecommunications.

Other ISM applications that operate in this frequency range, in addition to inductive radio systems (RFID), are remote control systems, remote controlled models, demonstration radio equipment and pagers. The main advantages of the high frequency range are:

- Normal CMOS technology can be used easily due to the relatively low frequency operation.
- The wave can penetrate materials like water and tissue.
- Simple antenna design (fewer turns of the coil).
- Higher data rate compared to the low frequency range.
- The high frequency RFID tag is thinner and simpler compared to the low frequencies RFID tag.

But the main disadvantages of the high frequency range are:

- Strict governmental regulations.
- Does not penetrate or transmit around metals.
- Large antennas compared to ultra higher frequencies.
- Large tag size compared to ultra higher frequencies.
- Short communication range compared to ultra high frequencies.

1.4.3.3 Ultra high frequency range (UHF) (915.0 MHz)

This frequency range is not available for ISM applications in Europe. Outside Europe (USA and Australia) the frequency ranges 888–889 MHz and 902–928 MHz are available and are used by backscatter (RFID) systems. The main advantages of the high frequency range are:

- Effective around metals
- Long distance operation.
- Small tag size and small antennas compared to lower frequencies ranges.
- Good non-line-of-sight communication
- High data rate.
- Controlled read zone (through antenna directivity)

But the main disadvantages of the ultra high frequency range are:

- Does not penetrate water/tissue
- Governmental regulations are different from country to another.

1.4.3.4 Microwave frequency range (2.45 GHz)

The ISM range 2.400–2.4835 GHz partially overlaps with the frequency ranges used by amateur radio and radiolocation services. The propagation conditions for this frequency range are quasi-optical. Buildings and other obstacles behave as good reflectors and damp an electromagnetic wave very strongly at transmission.

The main advantages of the microwave frequency range are:

- Tag size is smaller.
- Longer communication distance.
- Higher date rate.
- Smaller antennas.
- Good non-line-of-sight communication.
- Controlled read zone (through antenna directivity)
- Effective around metals.

But the main disadvantages of the microwave frequency range are:

- Shared spectrum with other technologies like microwave ovens.
- Tag design is challenging due to high frequency operation.
- Limited number of vendors.
- Governmental regulations are still in progress.

1.4.3.5 RFID frequencies comparison

A brief comparison between the main RFID frequencies is shown in Table 1-5.

Table 1-5: Comparison between the main RFID frequencies.

	LF Low frequency	**HF High frequency**	**UHF Ultra high frequency**	**Microwave frequency**
Frequency	135 kHz	13.56 MHz	915 MHz	2.45 GHz
Read range	~ 1 cm	~ 50 cm	~ 5 m	~ 5 m
Regulation	Unregulated	ISM	ISM	ISM
Main Applications	- Animal identification - data collection systems	- Contactless Smart Cards - Implantable RFID	- Supply chain - Toll collection	- Toll collection
Coupling	Magnetic (near field)	Magnetic (near field)	Far field	Far field
Tag size	⟶ Decrease			
Tag cost	⟶ Decrease			
Data rate	⟶ Increase			

1.5 RFID Standards

As shown in previous sections, there are many applications of RFID, and there are many frequencies were RFID can operate. Although this flexibility and variety of applications are the main advantages of RFID, the too many incompatible RFID standards are the main RFID disadvantages. Since its evolution, the major RFID vendors have produced RFID systems with different frequencies and protocols. This leads to too many variations and confusion.

The lack of open systems interchangeability has severely crippled RFID industry growth as a whole, and the resultant technology price reductions that come with broad-based inter-industry use. Just as standardization enabled the tremendous growth and widespread use of bar code, cooperation among RFID manufacturers will be necessary for promoting the technology developments and refinements that will enable broad-based application growth.

Regulations are mainly concerned with reader power emissions and allocation of frequency bands, while standards define the air interface communication between reader and tag, and include parameters such as:

- Communication protocol.
- Signal Modulation types.
- Data coding and frames.
- Data Transmission rates.
- Anti-collision.

The ISO and the EPCglobal have both been leading figures in this debate, [Sweeney, 05]. The ISO has their 18000 standard and the EPCglobal center has introduced the EPC standard. Some RFID consumers have decided to use the EPC standard, while others want to use ISO standard. This is putting a lot of pressure on the ISO and EPC to come to some kind of an agreement.

1.5.1 ISO Standards

The International Organization for Standardization (ISO) is based in Geneva, and its standards carry the weight of law in some countries. All ISO standards are required to be available for use around the world, so users of ISO RFID standards will not have to worry if their systems comply with the different regulations on frequencies and power output for each country where they do business. The ISO is very active in developing RFID standards for supply chain operations and is nearing completion on multiple standards to identify items and different types of logistics containers.

The most important ISO standard for RFID is ISO 18000 standard which describes the various parameters for air interface communications between the reader and the tag for different frequencies. It is composed of 6 parts, [Finken, 03]:

Part 1: Generic Parameter for Air Interface Communication for Globally Accepted Frequencies

Part 2: Parameters for Air Interface Communication below 135 kHz

Part 3: Parameters for Air Interface Communication at 13.56 MHz

Part 4: Parameters for Air Interface Communication at 2.45 GHz

Part 5: Parameters for Air Interface Communication at 5.8 GHz

Part 6: Parameters for Air Interface Communication in UHF Frequency Band

1.5.2 EPCglobal Standards

EPCglobal is an international organization that aims to encourage and help migration from the conventional bar code to the new EPC (Electronic Product Code). The goal is not to replace existing bar code standards, but rather to create a migration path for companies to move from established standards for bar codes to the new EPC.

Chapter 2

UHF RFID Tag System Design

In this chapter the design of a UHF RFID tag in 0.13 μm standard digital CMOS technology is demonstrated. The chapter starts with system description and design, and then the various blocks of the system are analyzed and designed. Finally the simulations results of the system and the chip layout are shown.

The main concern in designing the passive RFID tag is to consume as low power as possible. Decreasing the power consumption decreases the RF power needed from the reader and thus increasing the range of operation of the RFID tag.

Decreasing the power consumption of the RFID tag can be achieved through three ways:

- Increasing the conversion efficiency of the rectifier: This will be covered in the rectifier design.
- Decreasing the power consumption of the RFID tag blocks: This depends on the nature of each circuit and will be mentioned in each block design.
- Choosing a suitable communication scheme between the RFID reader and the RFID tag: This can be achieved by choosing the suitable frequency, the

communication protocol and the modulation scheme as will be explained in the following subsections.

2.1 Frequency Selection

As was mentioned in the introductory chapter, there are many frequency ranges where the RFID system can operate. The selection of the RFID frequency is mainly dependent on its application. For applications where a long communication range is desired, it is more efficient to operate the RFID system at UHF band (around 900 MHz). As the antenna length should be comparable to the operating wavelength, increasing the frequency of operation can decrease the antenna size. Also the directivity of the RFID reader antenna increases with increasing frequency. So for the same radiated RF power from the RFID reader, the available power at the RFID tag is higher at higher frequency. However, increasing the frequency to the microwave length (2.45 GHz) can complicate the RFID tag design which is not desirable for low cost applications.

In summary, the UHF RFID tag has the advantages of small size, long range, and low cost. It is suitable for applications such that toll collection, telemetry sensors, and object identification.

2.2 System Architecture

The RFID tag is simply a transceiver (transmitter + receiver). The main difference between the RFID tag and the traditional transceivers is the passive operation, i.e. there is no battery to supply DC voltage to the chip. For this reason, another block is needed to supply this DC voltage which is the rectifier. The block diagram of the RFID tag chip is shown in Figure 2.1.

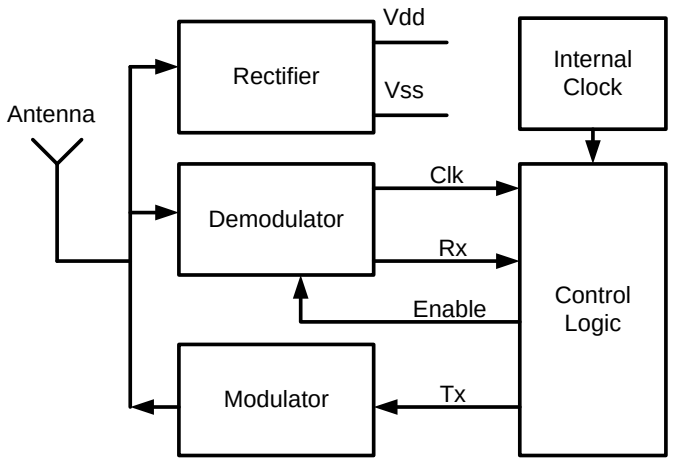


Figure 2.1: RFID tag block diagram.

The main blocks of the RFID tag are:

- Rectifier: This block rectifies the input RF signal and generates the needed DC voltage to power the other blocks of the system. This block is covered in section 3.1.
- Demodulator: This block is the receiver of the system which detects the commands sent by the RFID reader. It also extracts the clock from the received RF signal, which is needed to synchronize the RFID with the RFID reader. This block is covered in section 3.2.
- Control logic: This is the digital part of the system which controls all other blocks of the system. It determines when to receive, when to transmit and when to remain idle. It also stores the ID of the tag which is sent to the RFID reader by the modulator. This block is covered in section 3.3.
- Internal clock: This is an internal clock generator which supplies an internally generated clock to the digital part. This block is covered in section 3.4.
- Modulator: This block is the transmitter of the system which sends the tag ID to the RFID reader. This block is covered in section 3.5.

2.3 Communication Protocol

As mentioned before, decreasing the power consumption and increasing the operation range of the RFID tag can be achieved by properly choosing the communication protocol.

2.3.1 RFID reader versus RFID tag

The RFID system is a communication system between two non-equivalent nodes; the RFID reader and the RFID tag. The RFID reader has the following characteristics:

- The RFID reader is usually stationary.
- The RFID reader has a continuous DC supply.
- The RFID reader has a large size (compared to the RFID tag).
- The RFID reader is usually expensive (as the RFID system has few readers and many tags)

On the other side, the RFID tag has almost the opposite characteristics:

- The RFID tag is usually mobile (attached to moving objects).
- The RFID tag has no continuous DC supply (for passive tags).
- The RFID tag has a small size (compared to the RFID reader).
- The RFID tag has a low cost.

Due to this non-equivalence between the RFID reader and the RFID tag, it is very beneficial to move most of the system complexity to the RFID reader side. This movement relaxes the required specifications from the RFID tag which leads to simplification of its design, and decreasing of its area, and cost.

2.3.2 Modes of operation

The RFID tag passes through four modes of operation as shown in Figure 2.2:

1- Idle mode: In this mode the RFID tag is completely dead. No DC voltage exists in the chip and consequently all the RFID tag blocks are off. All what the RFID tag can do in this mode is to wait for the reader to send the RF signal.

2- Power-up mode: The RFID tag enters this mode when the RFID reader starts to send a continuous RF signal. The RF signal transmitted by the RFID reader is received by all the RFID tags in the neighborhood. The RFID tag stays in this mode until it builds its DC voltage. After the generated DC voltage exceeds a certain threshold, a POR (Power ON Reset) signal is generated to reset the digital part of the chip.

3- Addressing mode: After the RFID reader sends a continuous RF signal to all the RFID tags in the neighborhood, it starts to send the address of the RFID tag to which it wants to communicate. The RFID reader sends the address of the target tag as a sequence of short interrupts in the RF signal. The RFID tag demodulates the received RF signal from the RFID reader and compares the received address with its own address. If the received address is recognized, an ACK (Acknowledgement) signal is generated, and the RFID tag jumps to the reading mode.

4- Reading mode: This is the only mode in which the RFID tag sends information to the RFID reader. After the received address is recognized, the RFID tag starts to send a unique pattern to the RFID reader to inform the RFID reader that the intended RFID tag exists and is ready to receive commands. The RFID tag stays in this mode until it receives a STOP command from the RFID reader, or until the RF signal vanishes.

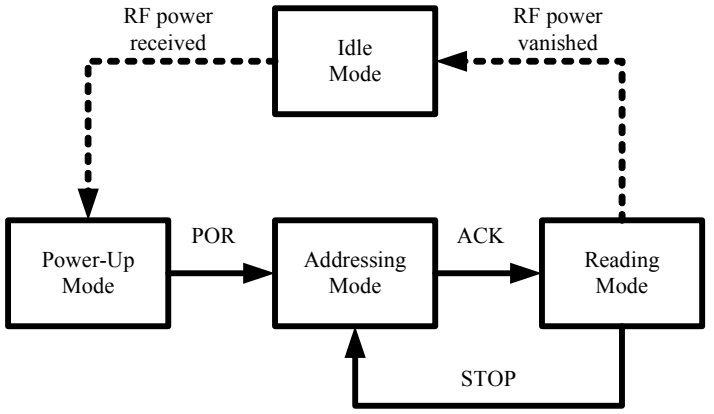


Figure 2.2: Modes of operation.

2.3.3 Communication mechanism

To avoid complicated synchronization circuits, the communication between the reader and the tag is fully controlled by the reader, i.e. the RFID tag cannot send data unless triggered by the RFID reader. The system clock is extracted directly from the received signal from the RFID reader as shown in Figure 2.3.

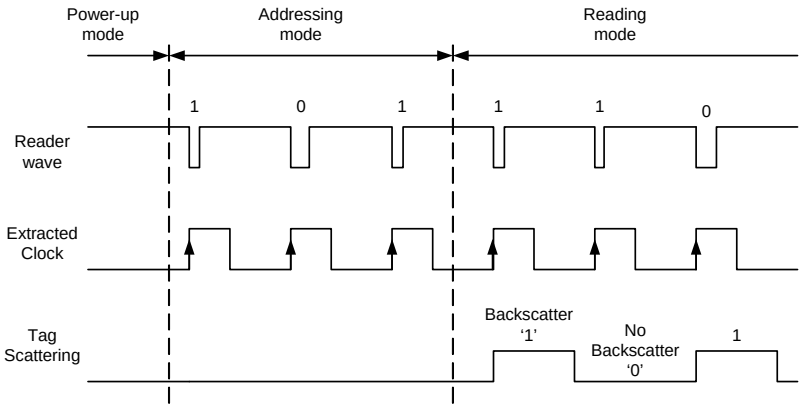


Figure 2.3: Communication mechanism.

The communication between the RFID reader and the RFID tag can be divided according to communication direction to two links:

1- Forward link

This is the communication link from the RFID reader to the RFID tag. In power-up mode, a continuous RF wave is transmitted from the RFID reader to the RFID tag, which is used to power the tag. After entering the addressing mode, the data is sent from the RFID reader to the RFID tag as short gaps in this continuous wave, as shown in Figure 2.3.

2. Reverse Link

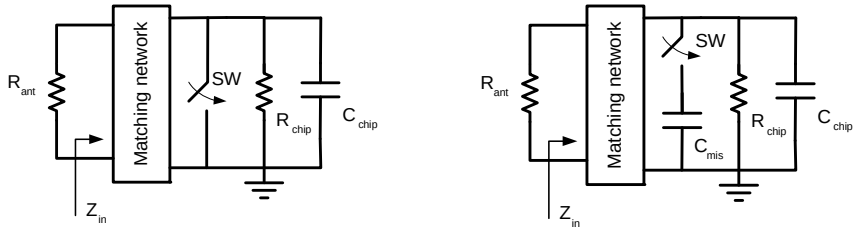
This is the communication link from the RFID tag to the RFID reader. This link is active only in reading mode, where the RFID tag needs to send its data to the RFID reader. The communication in the reverse link is done using backscattering. The reflected wave should be detected by the RFID reader.

2.3.4 Modulation scheme

The modulation type should be chosen carefully to be simple and power efficient. In the forward link, the most suitable modulation type is ASK-PWM (Amplitude Shift Keying – Pulse Width Modulation). In ASK the bits are sent as a short gaps in the RF signal. This modulation type has the advantage of simple and low power detection circuits. PWM (Pulse Width Modulation) is used to differentiate between logic '1' and logic '0'. PWM is chosen in this system as it has the advantage of simple clock extraction and detection circuits. Other modulation schemes are suggested in [Curty, 05], but they need more complexity, and power.

In the reverse link the most suitable modulation scheme is backscattering. Backscattering is a low power modulation scheme in which the RFID tag acts as a reflector which reflects a part of the incident RF wave back to the RFID reader. Backscattering can be either ASK-backscattering or PSK-backscattering, [EPC, 05]. In ASK-backscattering modulation, the chip impedance is varied between perfect match ($R_{in}=R_{ant}$) and complete mismatch ($R_{in}=0$) as shown in Figure 2.4(a), where R_{in} is the

input resistance of the chip and R_{ant} is the impedance of the antenna. In PSK-backscattering modulation, the real part of the chip impedance is kept in match with the antenna, while the imaginary part is varied between two capacitive and inductive values as shown in Figure 2.4(b). A comparison between ASK-backscattering and PSK-backscattering is summarized in Table 1, [Karthaus, 03].



(a) (b)

Figure 2.4: Backscattering types, (a) ASK, (b) PSK.

Table 2-1: Comparison between ASK and PSK backscattering.

	ASK-backscattering	**PSK-backscattering**
Reflected power	Higher	Lower
Available power	Dependent on duty cycle	
Process dependence	Immune	Sensitive
Circuit complexity	Simple	Complex
Detection	Easy	Difficult
Full duplex operation	Not possible	Possible

ASK-backscattering is much simpler and more efficient than PSK-backscattering. The only advantage of PSK is the possibility of full duplex operation, which is not needed for low rate applications of RFID. It was shown in [Karthaus, 03] that PSK-backscattering is better than ASK-backscattering in terms of power, but this comparison

was concerned only with available power to the tag. The complexity and process dependence of the PSK-backscattering makes it less attractive for low cost applications.

Chapter 3

UHF RFID Tag Circuits Design

In this chapter the circuit design of the UHF RFID tag in 0.13 μm standard digital CMOS technology is demonstrated. The various blocks of the system are analyzed and designed. Finally the simulations results of the system and the chip layout are shown.

3.1 Rectifier

As the RFID tag is a passive system, a DC voltage must be generated to bias the circuits of the tag. The rectifier is the main block in the RFID tag as it provides the needed DC voltage to the other blocks of the system. The DC voltage is generated by converting the received RF signal into a DC power. The main challenge in designing the RFID rectifier is to generate the required DC power using the low voltage amplitude of the RF signal with acceptable conversion efficiency.

In this section a simple and sufficiently accurate model for the low power rectifier is derived and verified by simulations. Then, design and optimization procedure of the

rectifier is introduced. Then, some enhancements techniques are discussed. Finally, the simulations results and the achieved specifications are summarized.

3.1.1 Rectifier Model

As the efficiency of the RFID rectifier is the main parameter that limits the operating range of the passive RFID tag, most of the RFID research is directed towards enhancing the efficiency of the rectifier. There are many publications that discuss and model the rectifier circuit to optimize its performance.

The main difference between the analysis of the traditional rectifier and the low power rectifier is the leakage current. In traditional rectifier circuits that are used in some AC powered appliances; the leakage current is much smaller than the forward current. This simplifies the analysis of the rectifier and makes the conversion efficiency very easy to estimate. In low power rectifier circuits where the DC current supplied by the rectifier is small, the leakage current is comparable to the forward current and cannot be neglected. This makes the analysis of the low power rectifier relatively complicated.

In [Curty, 05a] a model for the rectifier was introduced. The model was based on numerical analysis and extraction from simulation results. Although the model is sufficiently accurate, it did not give analytical equations that give sufficient design insight. Recently a model was introduced in [Yi, 07] that was based on analytical equations. The model is accurate but the equations are still too complicated to be dealt with in the design.

In this part of the work, a simple model for the rectifier circuit is introduced. By appropriate modeling of the transistor current and applying suitable approximations, simple equations are derived. The simplicity of derivations and equations makes them more suitable for the design and optimization of the rectifier circuits.

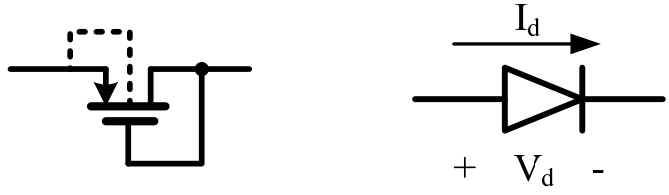
3.1.1.1 Diode Model

The diode is the basic rectification element. From the basic definition, the diode is an electronic device that allows the current to pass in only one direction. The more realistic definition of the diode is a device with a small resistance in one direction and a large resistance in the opposite direction.

The most popular example of the diode is the P-N junction, which is the most common rectification device in discrete electronics. The P-N junction is not suitable for low power rectifier because of its high cut-in voltage. Also P-N junction has large parasitic capacitance which makes it unsuitable for UHF rectifiers.

Schottky diode which is based on metal-semiconductor junction has a better performance. Schottky diode has a small cut-in voltage as well as small parasitic capacitance compared to the P-N junction. The main drawback of the Schottky diode is the special technology it needs. Most of standard CMOS technologies do not support Schottky diodes which makes it unsuitable for low cost applications where a cheap standard digital CMOS technology is preferred.

In standard CMOS process, the diode connected transistor is the basic rectifying element as shown in Figure 3.1. PMOS transistor is preferred, as its bulk effect can be eliminated by connecting its source to the bulk terminal [Kocer, 06].



(a) Diode connected PMOS transistor. (b) Equivalent diode.

Figure 3.1: Diode connected transistor.

The characteristics of the diode connected transistor are very similar to ordinary p-n junction diode. The I-V characteristics of the diode-connected transistor can be divided into 4 regions as shown in Figure 3.2:

1- Forward region ($V_d > V_{th}$), where V_d is the voltage across the transistor and V_{th} is the threshold voltage of the transistor: In this region the transistor is in saturation and a relatively large current can flow in the forward direction. The current in this region is given by [Rabaey, 03]:

$$I_d = K \cdot (V_d - V_{th})^2 \tag{3.1}$$

where $K = \frac{\mu_p C_{ox}}{2} \frac{W}{L}$, μ_p is the mobility of holes, and C_{ox} is the gate capacitance per unit area, *W, L* are the width and the length of the transistor, respectively.

2- Sub-threshold region ($0 < V_d < V_{th}$): In this region a small current flows in the forward direction.

3- Reverse region ($V_{bd} < V_d < 0$), where V_{bd} is the breakdown voltage of the transistor. The equation of the current in this region can be approximated by [Rabaey, 03]:

$$I_d = I_s \cdot (1 + \lambda \cdot V_d) \tag{3.2}$$

where I_s is the reverse saturation current, λ is the sub-threshold channel length modulation parameter.

4- Breakdown region ($V_d < V_{bd}$): In this region a large current flows in the reverse direction. The transistor should not be operated in this region to avoid degradation in efficiency.

3.1.1.2 Rectifier circuit model

Almost all the rectifier circuits are based on the basic circuit shown in Figure 3.3. A large capacitor C_L is added to smooth the rectified output and remove high frequency ripples. For a sufficiently large load capacitance C_L, the output voltage can be

approximated as a perfect DC voltage V_{dc}. A large current spike flows from the input when the input voltage V_{in} is higher than V_{dc} as shown in Figure 3.4. In the reverse region, i.e. when $V_{in} < V_{dc}$, a small current leaks to the input. The exact equation of the current can be derived from equations (3.1) and (3.2).

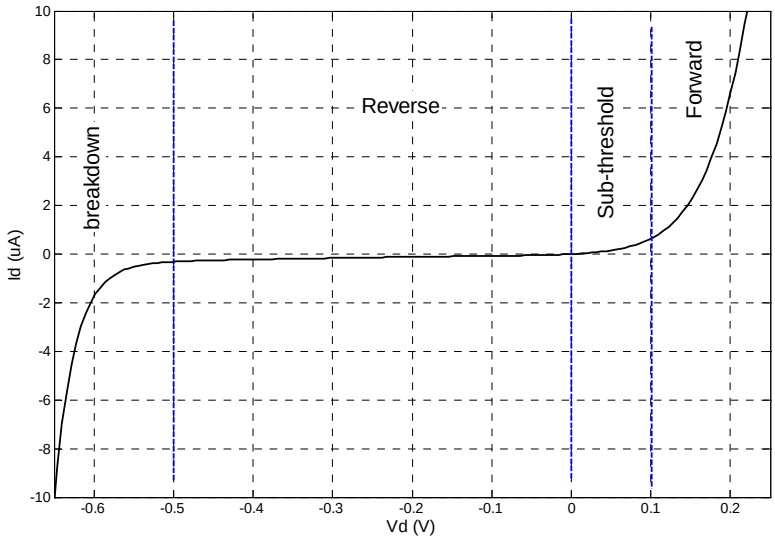


Figure 3.2: I-V characteristics of the diode connected transistor.

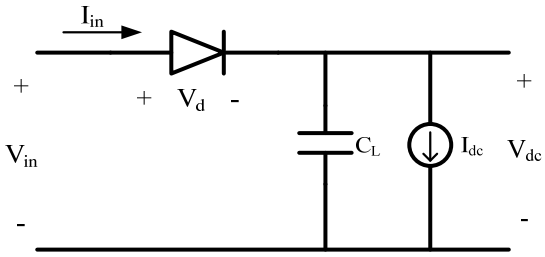


Figure 3.3: Basic rectifier circuit.

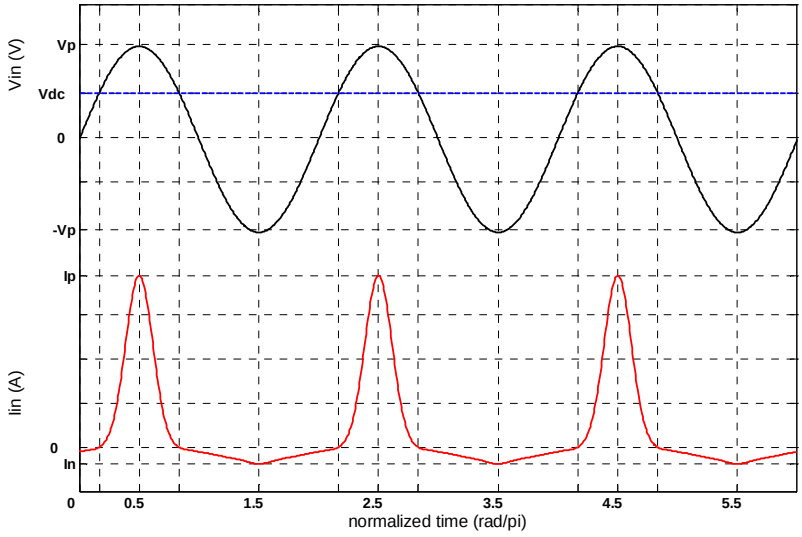


Figure 3.4: Waveforms of the rectifier circuit.

To get simple equations that can be used in design and optimization of the rectifier, an approximation to the waveform of the transistor current will be made. The current spikes in both forward and reverse regions are approximated as triangular pulses as shown in Figure 3.5, [Ashry, 07a]. In the following sub-sections, the proposed model will be used to derive the main rectifier parameters.

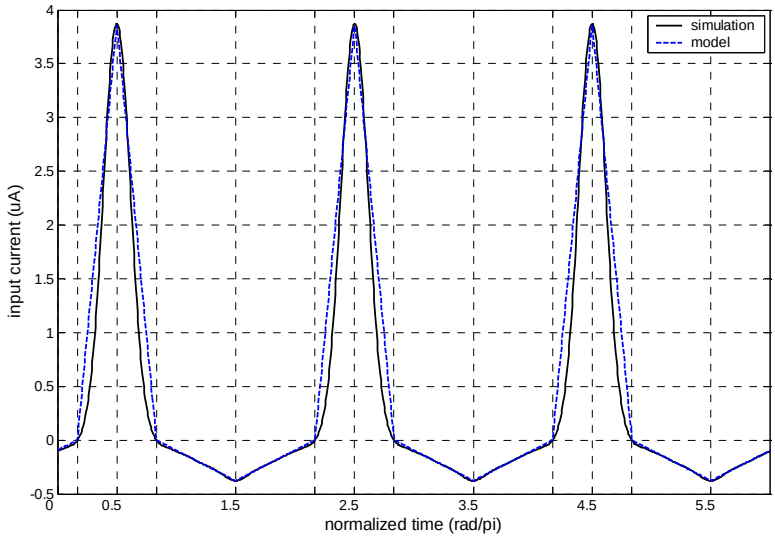


Figure 3.5: Modeling transistor current as triangular pulses

3.1.1.3 Output DC voltage

The objective of the rectifier is to produce a sufficient DC voltage with acceptable efficiency. The output DC voltage V_{dc} can be derived by applying the principle of charge conservation:

$$Q_{in} = Q_{out} \tag{3.3}$$

where Q_{in} and Q_{out} are the input and the output charge transferred to the rectifier circuit in one cycle. The input charge is the integration of the input current I_{in}. It is given by:

$$Q_{in} = \frac{1}{2} I_p T_p - \frac{1}{2} I_n T_n \tag{3.4}$$

where I_p, I_n are the peak value of the positive and the negative current pulses, respectively. T_p, T_n are the widths of the positive and the negative current pulse,

respectively. It can be deduced from Figure 3.4 that the area of the positive pulse is much larger than the negative pulse. So the input charge can be approximated as:

$$Q_{in} \approx \frac{1}{2} I_p T_p \tag{3.5}$$

From equation (3.1), I_p can be derived as:

$$I_p = K \cdot \left(V_p - V_{dc} - V_{th}\right)^2 \tag{3.6}$$

where V_p is the peak of the input signal. From Figure 3.4, T_p is given by:

$$T_p = \frac{T}{\pi}\left(\frac{\pi}{2} - \theta_1\right) \tag{3.7}$$

where θ_1 is start angle of the positive current pulse which is given by:

$$\theta_1 = \sin^{-1}\left(V_{dc} / V_p\right) \tag{3.8}$$

The output charge from the rectifier in one cycle is given by:

$$Q_{out} = I_{dc} T \tag{3.9}$$

where I_{dc} is the output DC current, and T is the period of the input signal. By substituting from equations (3.5) to (3.9) in equation (3.4), we get:

$$\left(1 - \sin\left(\theta_1\right) - \frac{V_{th}}{V_p}\right)\sqrt{\frac{\pi}{2} - \theta_1} = \frac{1}{V_p}\sqrt{\frac{2\pi I_{dc}}{K}} \tag{3.10}$$

By solving for θ_1, it can be approximated to:

$$\theta_1 \approx \sin^{-1}\left(\frac{1}{V_p}\left(V_p - V_{th} - \sqrt{\frac{2\pi I_{dc}}{K}}\right)\right) \tag{3.11}$$

And the output DC voltage is given by:

$$V_{dc} \approx V_p - V_{th} - \sqrt{\frac{2\pi I_{dc}}{K}} \tag{3.12}$$

The derived formula is simple, and physically meaningful. It can be interpreted as follows: The output DC voltage is equal to the peak of the input signal minus the drop across the transistor. The drop across the transistor consists of a constant part which is the threshold voltage, and a variable part corresponds to the over-drive voltage of the transistor.

The simulation of V_{dc} versus V_p at (I_{dc} = 1 μA and W/L = 32) is shown in Figure 3.6. It shows a good agreement between the simulation and the proposed model. For large input signal, the transistor gets into breakdown region and the reverse current increases dramatically. Consequently the approximation in equation (3.5) is no longer valid.

The simulation of V_{dc} versus I_{dc} at (V_p = 0.3 V and W/L = 32) is shown in Figure 3.7. It shows an acceptable agreement between the simulation and the proposed model.

The simulation of V_{dc} versus W/L at (V_p = 0.3 V and I_{dc} = 1 μA) is shown in Figure 3.8. It shows an acceptable agreement between the simulation and the proposed model.

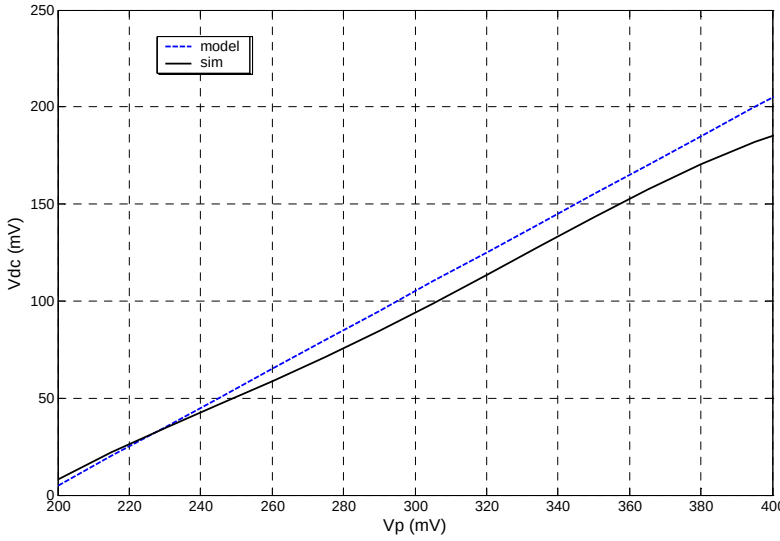


Figure 3.6: Output DC voltage versus the amplitude of the input signal.

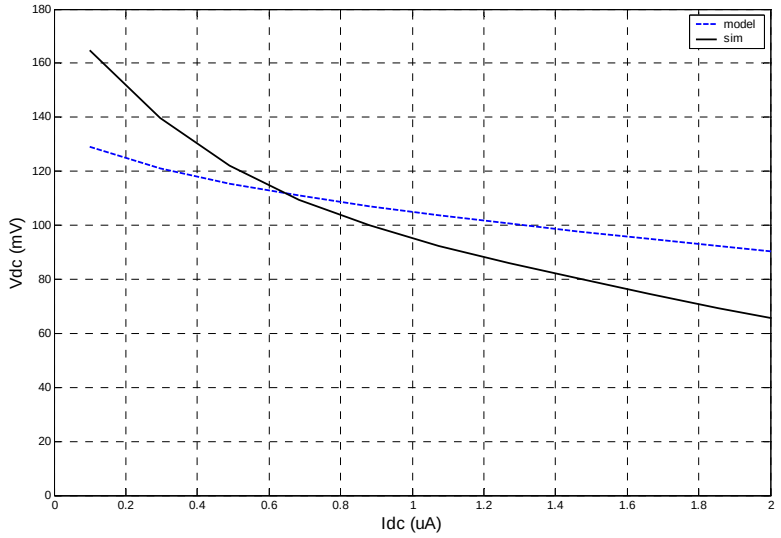


Figure 3.7: Output DC voltage versus the output DC current.

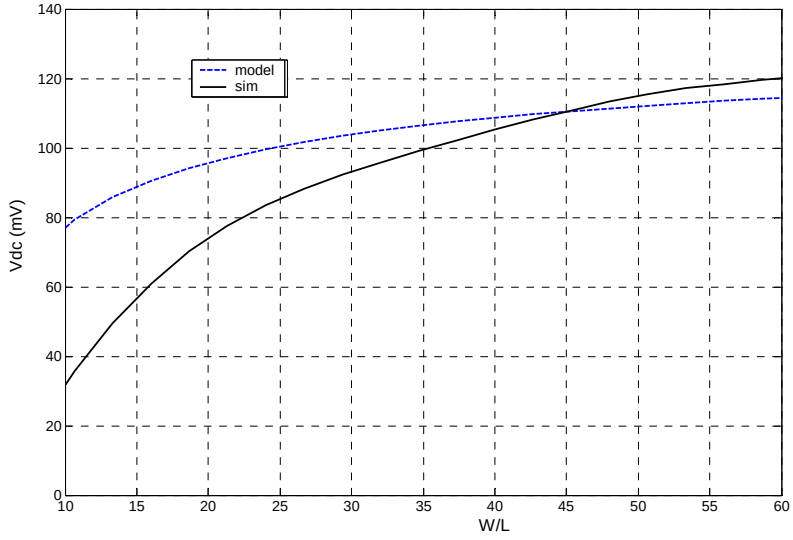


Figure 3.8: Output DC voltage versus the transistor aspect ratio.

3.1.1.4 Efficiency

The efficiency of the rectifier is the ratio between the output power and the input power, and is given by:

$$\eta = \frac{P_{dc}}{P_{dc} + P_{dis}} \tag{3.13}$$

where P_{dc} is the output DC power, and P_{dis} is the dissipated power in the transistor, which is given by:

$$P_{dis} = P_p + P_n \tag{3.14}$$

where P_p and P_n are the dissipated power in the positive and the negative current pulses, respectively. P_p is given by:

$$P_p = \frac{1}{\pi}\int_{\theta_1}^{\frac{\pi}{2}} \left(V_p \sin(\theta) - V_{dc}\right)\cdot I_p \frac{(\theta - \theta_1)}{\left(\frac{\pi}{2} - \theta_1\right)} d\theta \tag{3.15}$$

Unlike the derivation of the output DC voltage, the negative current pulse cannot be ignored, because the reverse voltage across the transistor in reverse is much higher than forward. So P_n is comparable to P_p and is given by:

$$P_n = \frac{1}{\pi}\int_{-\theta_1}^{\frac{\pi}{2}} \left(V_p \sin(\theta) + V_{dc}\right)\cdot I_n \frac{(\theta + \theta_1)}{\left(\frac{\pi}{2} + \theta_1\right)} d\theta \tag{3.16}$$

where I_n is given by:

$$I_n = I_s \cdot \left(1 + \lambda\left(V_p + V_{dc}\right)\right) \tag{3.17}$$

Integrations in equations (3.15) and (3.16) can be solved analytically and it can be shown that P_p is given by:

$$P_p = \frac{V_p I_p}{\pi} f(\theta_1) \tag{3.18}$$

and P_n is given by:

$$P_n = \frac{V_p I_n}{\pi} f(-\theta_1) \tag{3.19}$$

where $f(\theta)$ is given by:

$$f(\theta) = \frac{1 + \left(\frac{\pi}{2}\theta - \frac{\pi^2}{8} - 1 - \frac{\theta^2}{2}\right) \cdot \sin(\theta)}{\frac{\pi}{2} - \theta} \tag{3.20}$$

Substituting from equations (3.6), (3.17), (3.18), and (3.19) in (3.14), we can get:

$$P_{dis} = \frac{V_p}{\pi}\left[K \cdot (V_p - V_{dc} - V_{th})^2 f(\theta_1) + I_s \cdot (1 + \lambda(V_p + V_{dc}))f(-\theta_1)\right] \tag{3.21}$$

And finally the efficiency is given by:

$$\eta = \frac{V_{dc} I_{dc}}{V_{dc} I_{dc} + \frac{V_p}{\pi}\left[K \cdot (V_p - V_{dc} - V_{th})^2 f(\theta_1) + I_s \cdot (1 + \lambda(V_p + V_{dc}))f(-\theta_1)\right]} \tag{3.22}$$

The simulation of η versus I_{dc} at (V_p = 0.3 V and W/L = 32) is shown in Figure 3.9. For small values of input signal amplitude, there is a good agreement between the simulation and the proposed model. For a large input signal, the transistor gets into breakdown region and the reverse current increases and the efficiency of the rectifier decreases drastically. So the maximum efficiency can be achieved when the amplitude of the input signal is equal or slightly lower than the value that causes the transistor to get into breakdown region.

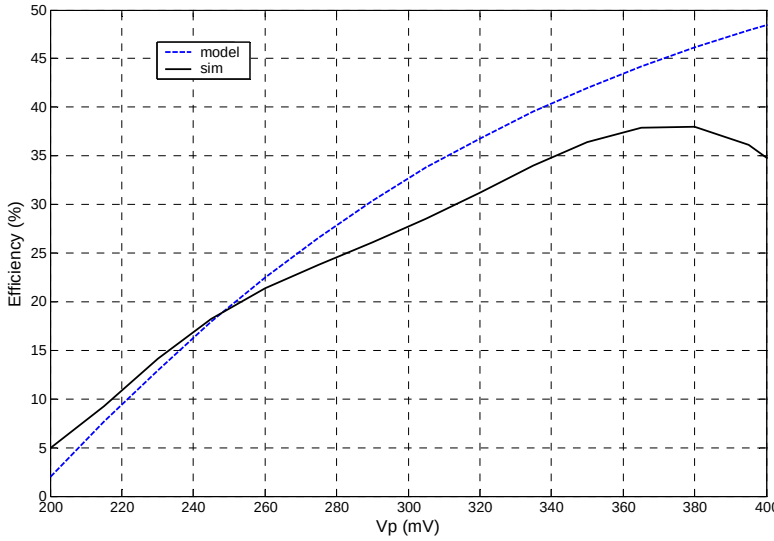


Figure 3.9: Rectifier efficiency versus the amplitude of the input signal.

The simulation of η versus I_{dc} at (V_p = 0.3 V and W/L = 32) is shown in Figure 3.10. It shows that there is an optimum value for the load current that gives maximum efficiency. Rectifier should be designed such that the optimum load current is the actual desired current. This can be achieved by proper sizing of the rectifier transistor.

The simulation of η versus W/L at (V_p = 0.3 V and I_{dc} = 1 μA) is shown in Figure 3.11. It indicates that increasing the aspect ratio of the rectifier transistor enhances the efficiency of the rectifier. But after a certain break-point the increase in the output DC voltage and efficiency is negligible, while the area and the parasitic capacitance of the transistor may degrade the performance. So it is recommended to set the size of the transistor near this break-point for optimum operation of the rectifier.

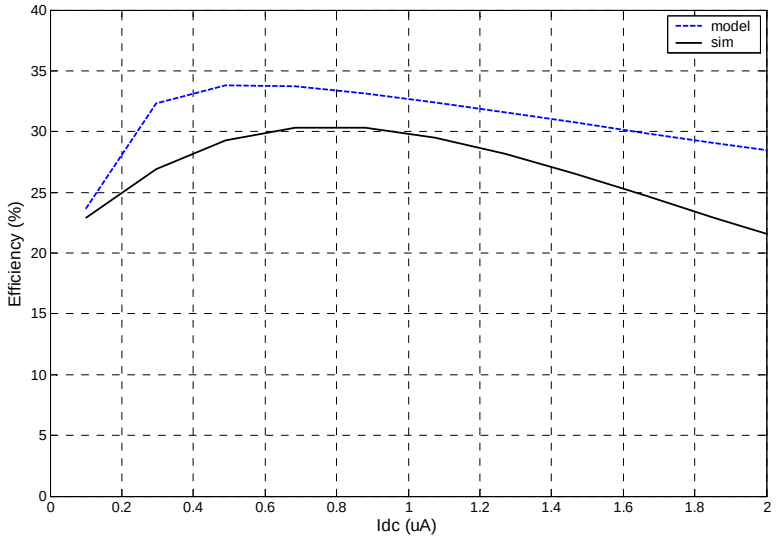


Figure 3.10: Rectifier efficiency versus DC current.

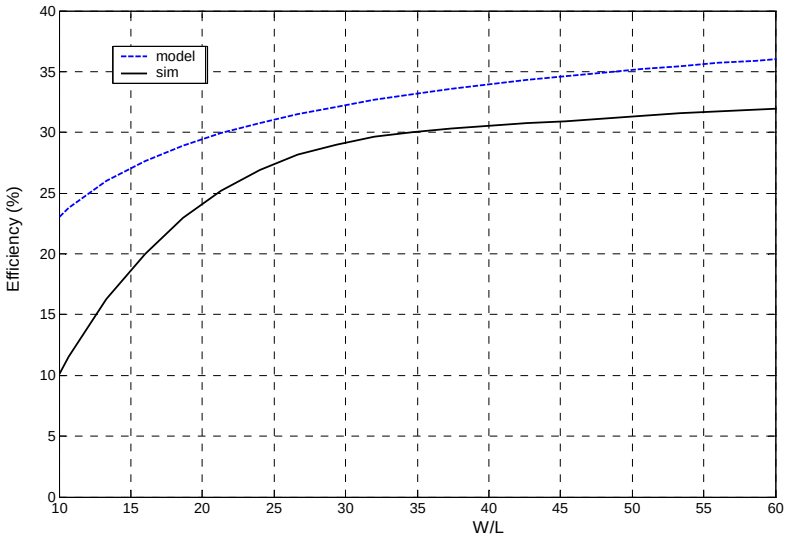


Figure 3.11: Rectifier efficiency versus aspect ratio of the transistor

3.1.2 Rectifier Design

3.1.2.1 Rectifier Cell

The direct rectification operation that was described in the previous section produces low DC voltage that is not sufficient for biasing the circuits of the RFID tag chip. The incident RF signal voltage amplitude is about 400 mV, and the generated DC voltage is only 250 mV. As the minimum required DC voltage is 1 V, a DC voltage doubler circuit is needed. The basic voltage doubler cell is as shown in Figure 3.12. Although there are many other versions of this circuit, this configuration has the advantage of being easy to be cascaded.

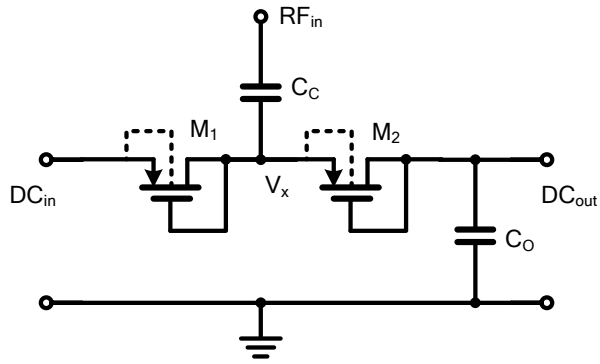


Figure 3.12: Basic voltage doubler cell

The operation of the voltage doubler circuit can be described using Figure 3.13, where the diode connected transistors are replaced with the equivalent diodes. The voltage doubler circuit can be divided into two clamping circuits as indicated by the two dashed boxes in the figure.

The first clamper which is composed of the diode M_1 and the capacitor *Cc* forces the capacitor C_c to charge in the direction indicated by the diode M_1. This introduces a DC voltage drop across the capacitor C_c equals approximately to the peak of the input RF signal at the node RF_{in} plus the input DC voltage DC_{in}. So at steady state the voltage of

the node V_x equals to the voltage of the node RF_{in} shifted by this DC voltage. Mathematically, if the input RF signal voltage is given by:

$$RF_{in} = V_p \cdot \sin(\omega t) \tag{3.23}$$

where V_p is the peak voltage magnitude of the input RF signal. Then the voltage of the node V_x is ideally given by:

$$V_x = DC_{in} + V_p \cdot \sin(\omega t) + V_p \tag{3.24}$$

which indicate that the voltage of the node V_x varies between zero and double the peak value of the input RF signal added to input DC voltage.

The second part of the circuit which is composed of the diode M_2 and the capacitor C_o can be considered as a peak detector which forces the voltage of the output node DC_{out} to charge to the peak value of the voltage of the node V_x. So the output voltage is ideally given by:

$$DC_{out} = DC_{in} + 2 \cdot V_p \tag{3.25}$$

So this circuit adds a DC voltage of $2V_p$ to the input voltage.

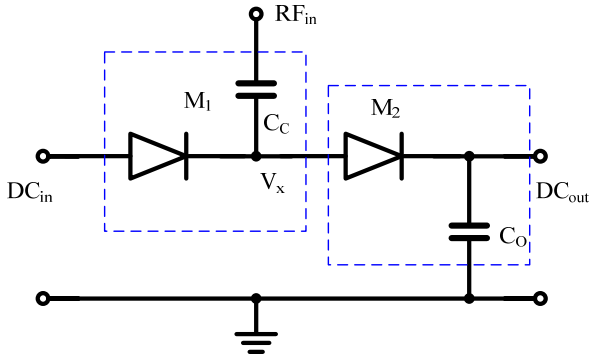


Figure 3.13: The concept of voltage doubler circuit.

In practice there is a DC voltage loss due to the voltage drop across the diodes. The DC voltage generated form a single voltage doubler cell should be modified to be:

$$V_{dc,\sin gle} = 2\left(V_p - V_d\right) \tag{3.26}$$

where V_d is the voltage drop across the diode connected transistor.

As the input RF signal voltage is small, the DC voltage generated form a single voltage doubler cell is much smaller than the needed DC voltage for the chip. To get this DC voltage, several cells are cascaded as shown in Figure 3.14. The final output DC voltage is given by:

$$V_{dc} = n \cdot V_{dc,\sin gle} = 2n \cdot \left(V_p - V_d\right) \tag{3.27}$$

where n is the number of cascaded stages.

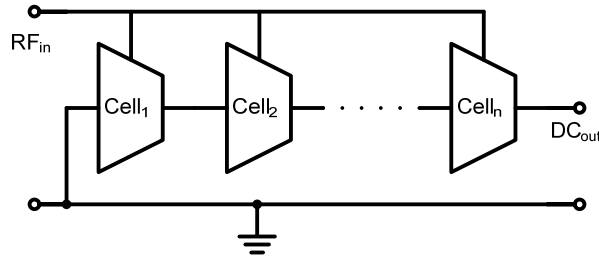


Figure 3.14: Cascaded voltage doubler cells.

3.1.2.2 Rectifier design process

The main challenge in the design of the rectifier is to achieve maximum conversion efficiency. As will be shown, the efficiency of the rectifier is dependent on the magnitude of input RF signal V_p, and the output DC current I_{dc}. So the optimization process must be done at the actual values of V_p and I_{dc}.

The output DC current can be estimated through the initial design of the remaining system blocks. The voltage magnitude of the input RF signal is dependent on the available RF signal power P_{rf}, and the tag chip input resistance R_{in}. If the chip impedance is perfectly matched to the antenna, the voltage magnitude of the input RF signal is given by, [Umeda, 06]:

$$V_p = \sqrt{P_{rf} \cdot R_{in}} \tag{3.28}$$

The input resistance of the tag chip is given by:

$$R_{in} = R_{in,rect} \parallel R_{in,demod} \tag{3.29}$$

where $R_{in,rect}$ is the input resistance of the rectifier, and $R_{in,demod}$ is the input resistance of the demodulator. These are the only two components which draw current from the input RF signal. Because most of the input RF power goes through the rectifier, the input resistance of the chip is approximately equal to the input resistance of the rectifier, i.e $R_{in} \approx R_{in,rect}$. So the equation (2.28) can be written as:

$$V_p = \sqrt{P_{rf} \cdot R_{in,rect}} \tag{3.30}$$

So, for a given RF signal power, the RF signal voltage is dependent on the rectifier. The optimization process for the rectifier can be summarized in the following steps:

- Determine the needed output DC current (I_{dc}) and the output DC voltage (V_{dc}).
- Optimize a single stage rectifier for maximum efficiency at the given output DC current.
- Determine the voltage magnitude of input RF signal (V_p) that gives maximum efficiency.
- Measure the output DC voltage for the single stage rectifier ($V_{dc,single}$) at the maximum efficiency conditions.
- The number of needed cascaded rectifier stages can be found from equation (3.27).
- The input resistance of the rectifier and hence the needed impedance of antenna can be found from equation (3.29).

The design process of the rectifier is illustrated in Figure 3.15.

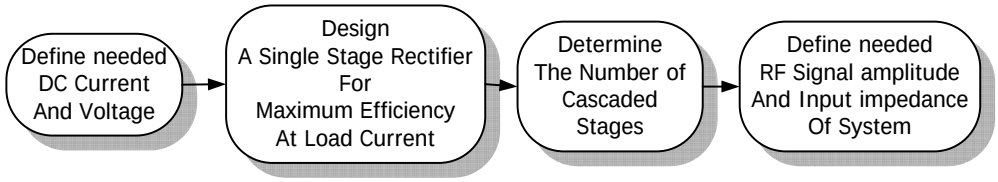


Figure 3.15: The design process of the rectifier.

3.1.3 Enhancement Techniques

As the rectifier is the main block of the RFID tag, a great effort was done to enhance its efficiency. In the following subsections some efficiency enhancement techniques are introduced.

3.1.3.1 Symmetric Supply

The efficiency of the rectifier can be enhanced by using symmetric rather than single supply, i.e., the rectifier will supply both positive and negative DC voltage. Due to symmetric operation, both positive and negative half cycles of the input RF signal are rectified. This increases the efficiency of rectification, and decrease the nonlinearity of input resistance due to rejection of even-order distortion. The enhancement in linearity makes the interface to antenna more efficient, [Curty, 05]. In addition, availability of both positive and negative supplies makes the design of analog blocks more flexible and efficient.

3.1.3.2 Digital and Analog Supplies

It was found that using separate supplies for analog and digital parts can enhance the overall efficiency of the system. This enhancement has many reasons:

- Separation of analog and digital supplies protects the sensitive analog blocks against sharp spikes that arise in digital gates.
- Digital part can operate at relatively lower supply than analog part. So a power saving can be obtained by using a slightly low supply voltage for the digital part.
- Leakage current in digital circuits, which is a strong function of the supply voltage, can be eliminated by using a lower supply for the digital part. This point will be clarified when discussing the digital circuits in section 3.3.

The complete rectifier circuit is shown in Figure 3.16.

3.1.4 Simulations Results

The final simulation results of the rectifier are summarized in the following subsections.

3.1.4.1 Efficiency of the rectifier

As was mentioned in subsection 3.1.1, the efficiency of the rectifier is mainly dependent on the amplitude of the input RF signal. The efficiency of the rectifier is simulated, and the result is shown in Figure 3.17. It can be found from the figure that a maximum efficiency of 32% can be achieved at the optimum value of the input RF signal which is about 0.4 V.

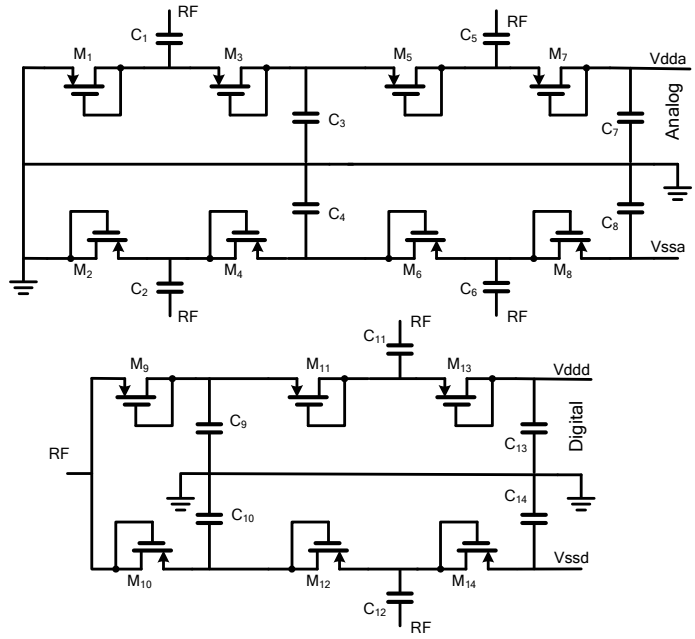


Figure 3.16: The complete rectifier circuit.

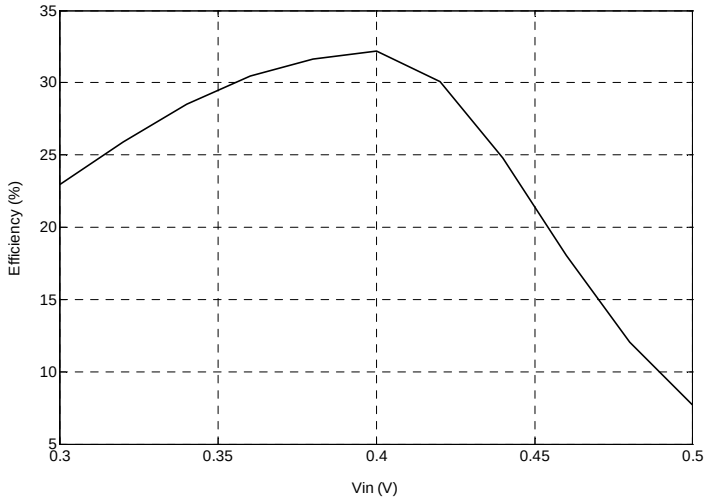


Figure 3.17: Efficiency of the rectifier versus the input RF signal amplitude.

3.1.4.2 Build-up time of the rectifier

It is desirable that the rectifier DC voltage has a short build-up time. The transient simulation result of the rectifier is shown in Figure 3.18. The figure shows that after 20 us, the output DC voltage has approximately settled on the required output DC voltage.

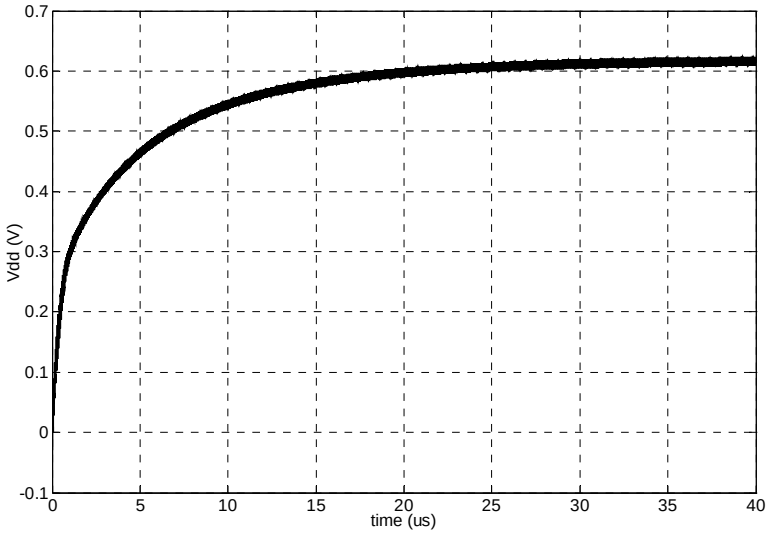


Figure 3.18: Transient simulation of the rectifier.

3.1.4.3 Rectifier Specifications

The achieved specifications of the rectifier are summarized in Table 3-1.

Table 3-1: The rectifier achieved specifications.

Parameter	Sym.	Value
Output DC current	I_{dc}	0.5 μA (analog) 0.5 μA (digital)
Output DC voltage	V_{dc}	1.2 V (analog) 0.8 V (digital)
Conversion Efficiency	η	32%
Ripple Voltage	V_r	10 mV
Voltage Build-up time	T_{build}	20 μs

3.2 Demodulator

The demodulator is the block which is responsible for detecting the data sent by the reader to the tag. In this system, the reader sends the data as short gaps in the RF signal. So a simple envelope detector is used to detect these gaps. The width of the gaps is chosen for optimum operation as was discussed in system design. The envelope detector used should be fast enough to detect short gaps. But in the same time, it should consume minimum power to avoid degrading the overall system performance. These two requirements are contradictory as will be discussed in the envelope analysis.

3.2.1 Envelope Detector

The basic envelope detector is shown in Figure 3.19. When the RF signal is ON, the output voltage tracks the peak of the RF signal voltage. The output voltage is given by:

$$V_m = V_p - V_d \tag{3.31}$$

Where V_p is the peak voltage of the RF signal, V_d is the voltage drop across the envelope detector diode D_1.

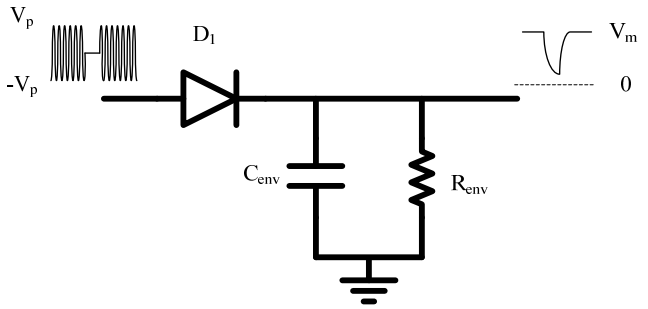


Figure 3.19: Basic envelope detector circuit.

When the RF signal voltage is OFF, the output voltage drops exponentially towards zero. This implies that the comparator that follows the envelope detector should compare the output of the envelope detector to a voltage reference approximately equal to $0.5V_m$. It is desirable to make the comparison level at zero voltage. This requires the output of the envelope detector to drop to a negative value during OFF state of the RF signal. This can be achieved by replacing the ground terminal in the envelope detector circuit with a negative DC voltage as shown in Figure 3.20. The negative DC voltage can be obtained by a simple rectifier section. The complete envelope detector circuit is shown in Figure 3.21.

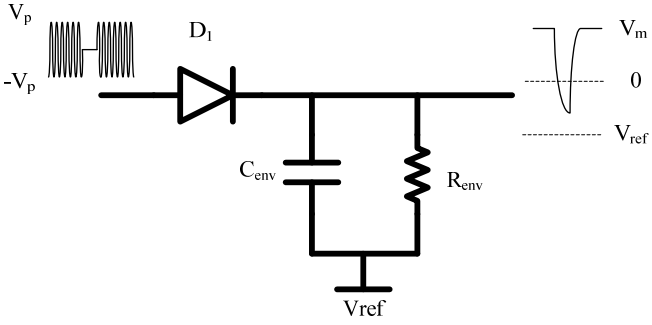


Figure 3.20: Modified envelope detector circuit.

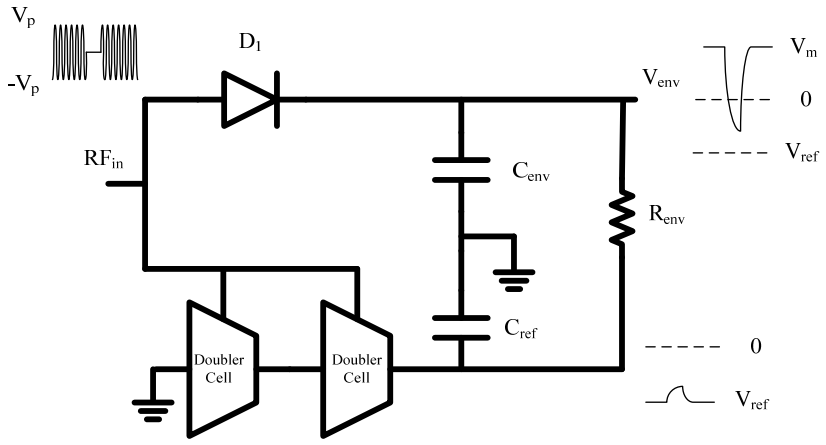


Figure 3.21: Complete envelope detector circuit.

3.2.1.1 Design of the envelope detector

The input and the output waveforms of the envelope detector circuit are shown in Figure 3.22. The values of R_{env} and C_{env} should be chosen carefully for acceptable operation at minimum power consumption. Although the circuit is completely passive, it should draw as minimum current from RF port as possible. In other words the input resistance of the peak detector should be maximum. It can be shown easily that the input resistance of the peak detector is directly proportional to the envelope resistance R_{env}:

$$R_{in,demod} \propto R_{env} \tag{3.32}$$

So, increasing the value of R_{env} reduces the power consumption of the circuit. But increasing the value of R_{env} reduces the slope of discharge of the envelope capacitor C_{env} and the voltage drop due to the RF signal gap ΔV_{env} decreases:

$$\Delta V_{env} \propto \frac{T_b}{R_{env} \cdot C_{env}} \tag{3.33}$$

where T_b is the width of the RF signal gap

Decreasing the value of the envelope capacitor C_{env} increases ΔV_{env}, but the ripple voltage at the peak detector output $V_{r,demod}$ increases:

$$V_{r,de\,\mathrm{mod}} \propto \frac{C_{gs,D_1}}{C_{env}} \tag{3.34}$$

where $C_{gs,D1}$ is the capacitance of the envelope diode.

These tradeoffs can be summarized as follows:

$R_{env} \uparrow \Delta V_{env} \downarrow R_{in,demod} \uparrow$

$C_{env} \uparrow \Delta V_{env} \downarrow V_{r,demod} \downarrow$

Suitable values for R_{env} and C_{env} should be chosen carefully as a compromise between the performance and the power consumption.

3.2.1.2 CMOS Implementation

As in the rectifier, the diode is replaced with a diode connected PMOS transistor. The negative DC voltage is generated using a two cascaded voltage doubler cells similar to that used in the rectifier. To be compatible with standard digital CMOS process, the resistors are replaced with a diode connected transistors with low transconductance. Because the linearity is not an issue, the capacitors used are ordinary MOS capacitors which have poor linearity, but they are more area-efficient than MIM capacitors. The CMOS implementation of the envelope detector circuit is shown in Figure 3.23.

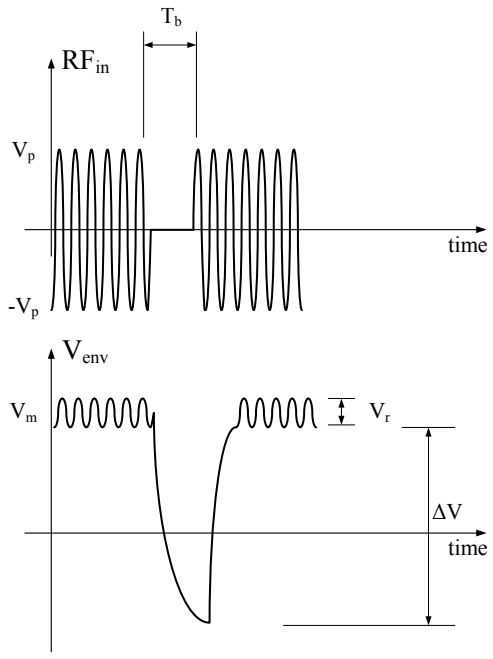


Figure 3.22: Input and output waveforms of the envelope detector circuit.

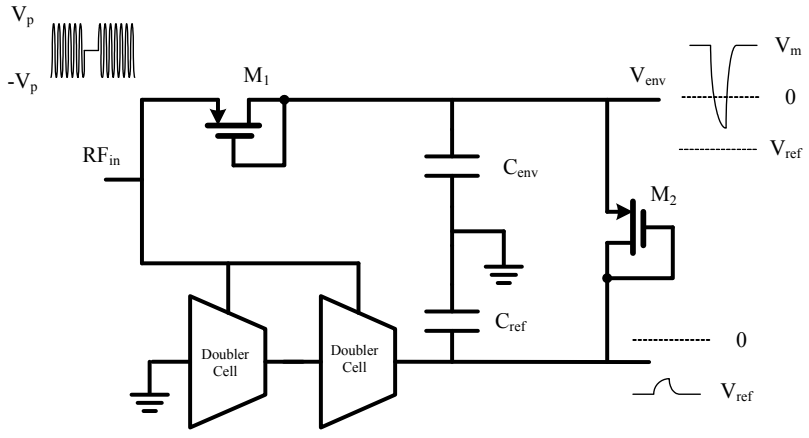


Figure 3.23: The CMOS implementation of the envelope detector.

3.2.2 Comparator

The comparator is a single stage OTA as shown in Figure 3.24. Because the communication bit rate is low, and the input signal to the comparator is relatively high, the gain and bandwidth requirements of the OTA are relaxed. The transistor M_6 is added as a switch to disable the OTA during scattering period. The AC simulation of the OTA gain is shown in Figure 3.25. The stability of the OTA is not an issue here due to its open loop operation, so the phase response of the gain is not shown.

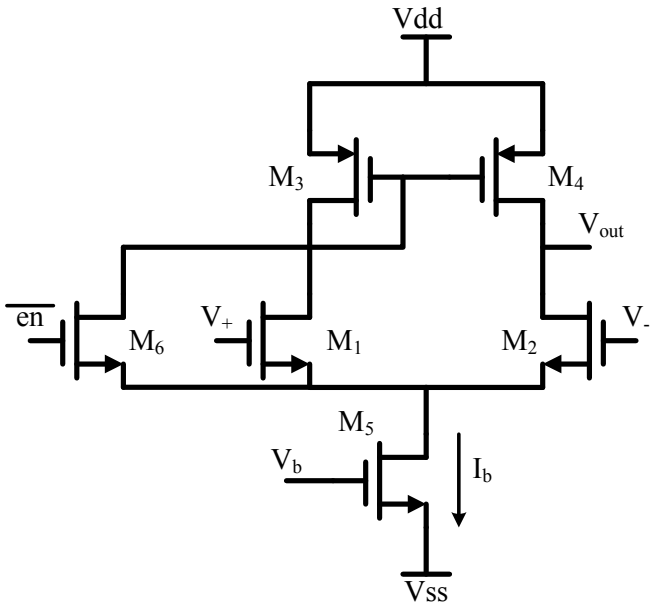


Figure 3.24: Single stage OTA.

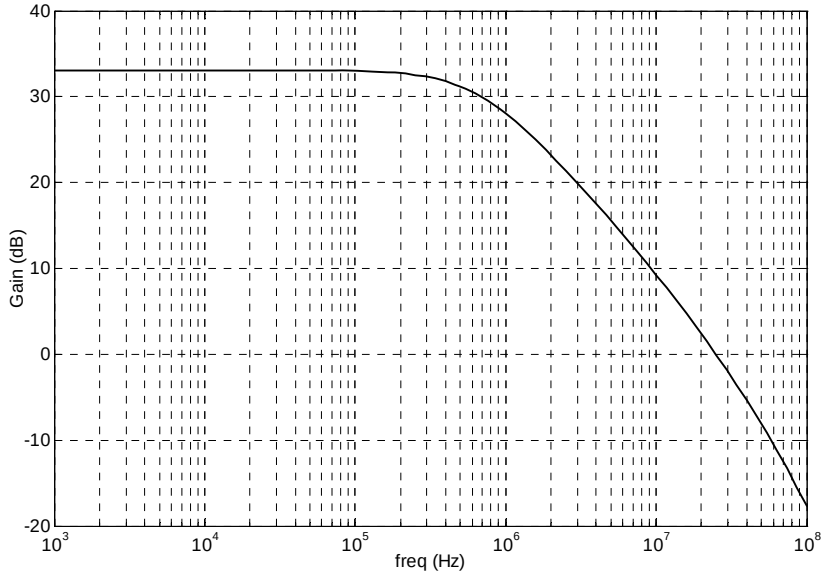


Figure 3.25: The AC simulation of the OTA gain.

The complete demodulator circuit is shown in Figure 3.26. Due to the low driving capability of the OTA, it needs to be buffered with an inverter. But using the ordinary static CMOS inverter can lead to a huge power loss due to the slow rise and fall time of the extracted clock. So, the output of the OTA is buffered using a CMOS current starved inverter. The transient simulation results of the peak detector and comparator are shown in Figure 3.27.

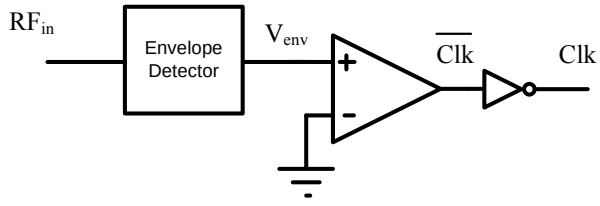


Figure 3.26: The complete demodulator circuit.

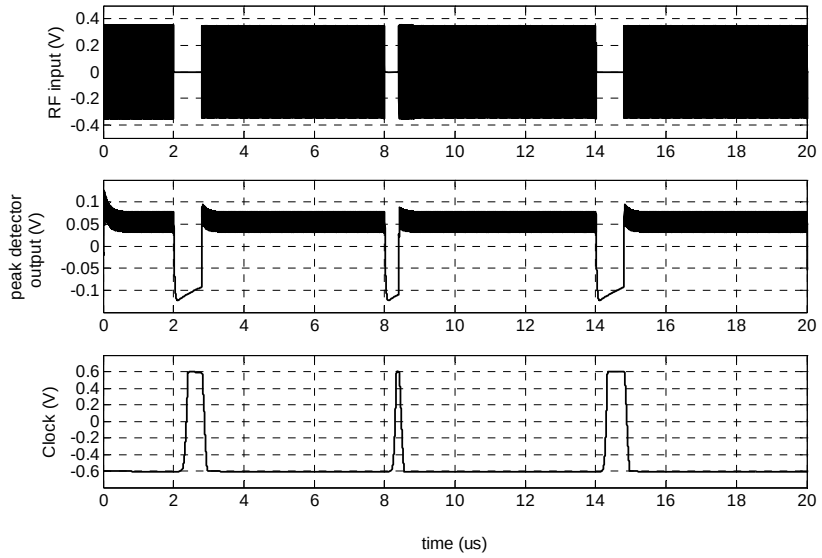


Figure 3.27: Simulation results of the peak detector and comparator.

3.2.3 PWM demodulator

Pulse Width Modulation (PWM) is used to encode the data sent by the RFID reader to the RFID tag. So, the received gaps have two different pulse widths T_{hi}, T_{lo} which correspond to the width of pulse at logic '1' and the width of pulse at logic '0', respectively. This requires a PWM demodulator after the peak detector. The basic circuit for PWM demodulation is based on an integrator followed by a decision device as shown in Figure 3.28.

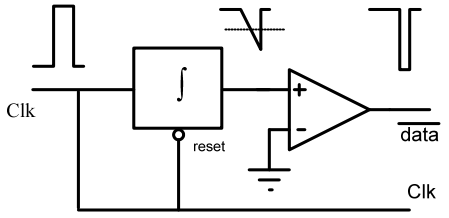


Figure 3.28: Basic PWM demodulator circuit.

The integrator is implemented using a current source and a capacitor. The comparator is similar to the comparator that was used in the envelope detector circuit. The CMOS implementation of the PWM circuit is shown in Figure 3.29. A current starved inverter similar to that used in the peak detector circuit is used to buffer the output of the comparator and drive the digital load.

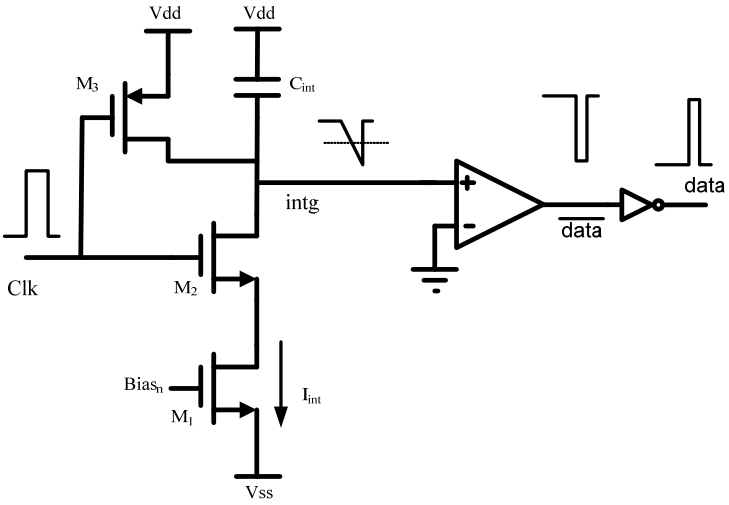


Figure 3.29: The CMOS implementation of the PWM circuit.

3.2.3.1 Design of the integrator

As the clock pulse width can have either one of two different values T_{hi} or T_{lo}, the integrator should give two sufficiently different outputs in each case. The output of the integrator at the end of T_{lo} is given by:

$$V_{\text{int},lo} = Vdda - \frac{I_{\text{int}} \cdot T_{lo}}{C_{\text{int}}} \tag{3.35}$$

and similarly the output of the integrator at the end of the T_{hi} is given by:

$$V_{\text{int},hi} = Vdda - \frac{I_{\text{int}} \cdot T_{hi}}{C_{\text{int}}} \tag{3.36}$$

where *Vdda* is the positive analog supply voltage (typically 0.6 V), I_{int} is the integrator current, and C_{int} is the integrator capacitor. For optimum operation $V_{int,lo}$ and $V_{int,hi}$ should be symmetric around the zero, i.e. $V_{int,lo} = -V_{int,hi}$. So from equation (3.35) and equation (3.36) we have:

$$\frac{I_{\text{int}}}{C_{\text{int}}} = \frac{2 \cdot Vdda}{T_{hi} + T_{lo}} \tag{3.37}$$

and:

$$V_{\text{int},hi} = -V_{\text{int},lo} = Vdda\left(1 - \frac{2 \cdot T_{hi}}{T_{hi} + T_{hi}}\right) \tag{3.38}$$

For *Vdda* equals 0.6 V and T_{lo}, T_{hi} , equal 0.4 μs, 0.8 μs respectively, the values of $V_{int,lo}$ and $V_{int,hi}$ are 0.2 V and -0.2 V respectively which are sufficient to drive the comparator. The values of I_{int} and C_{int} are designed for minimum power (minimum value of I_{int}), with acceptable performance. Decreasing I_{int} decreases the power consumption, but it requires decreasing C_{int} making it comparable to the parasitic capacitance and hence increases the dependence on process variations. The value of I_{int} is 100 nA, and C_{int} is 100 fF. The simulation results of the PWM demodulator are shown in Figure 3.30.

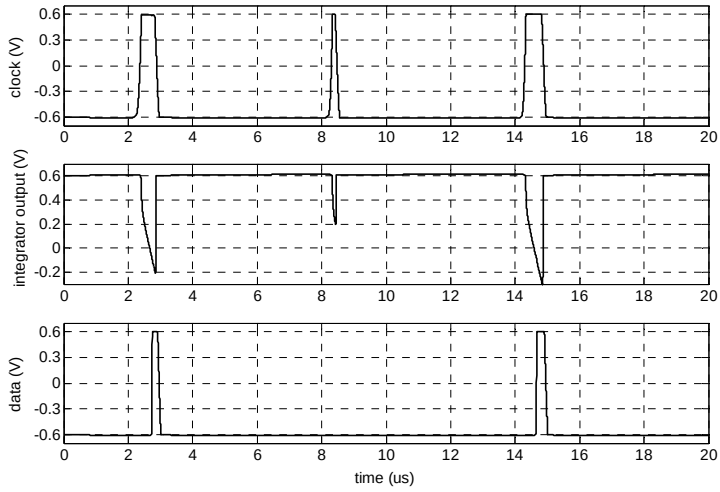


Figure 3.30: Simulation results of the PWM demodulator.

3.3 Digital Control

The digital control block is the block responsible for generating all the control signals needed in the RFID tag system. The design of the digital control is based on understanding the system operation as was explained in the system design section. To simplify the design of the digital control, it is divided to two sub-blocks:

- Mode selector: This sub-block is responsible for determining the mode of operation of the RFID tag.
- Backscattering control: This sub-block is responsible for controlling the period at which the backscattering is active.

3.3.1 Mode Selector

This part is responsible for determining the mode of operation of the RFID tag system. When the system builds its DC voltage, a POR pulse is generated and the system jumps to the addressing mode (Read = 0, Address = 1). In this mode the system is allowed to read the data received by the demodulator. At each positive edge of the extracted clock (Clk_{ext}), a bit is read and stored in the shift register. The read pattern is compared with the specific pattern (011). When the read pattern is equal to (011), the RFID tag system recognizes the RFID reader, and the acknowledgement signal (ACK) goes high. At this positive edge of the ACK signal, the system jumps to reading mode (Read = 1, Address = 0). The mode selector implementation and waveforms are shown in Figure 3.31 and Figure 3.32, respectively.

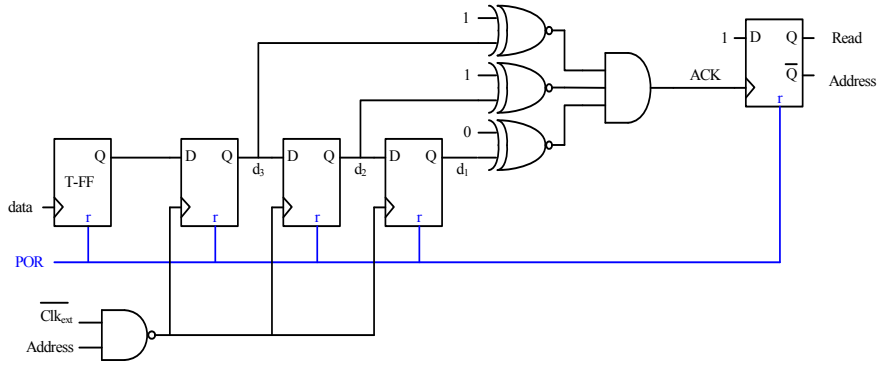


Figure 3.31: Mode selector implementation.

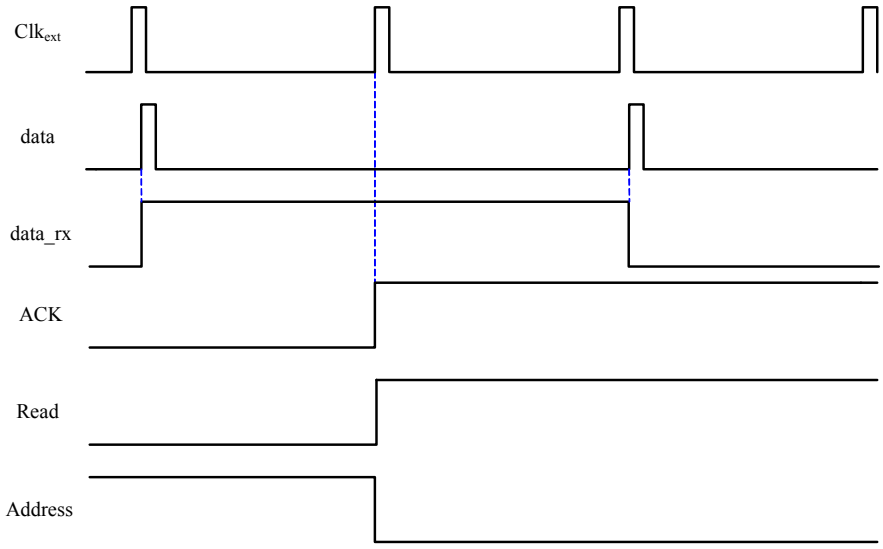


Figure 3.32: Mode selector waveforms.

3.3.2 Backscattering Control

This part is active in reading mode. It controls the backscattering operation to avoid re-injection of the backscattered signal. The backscattering control implementation and its waveforms are shown in Figure 3.33 and Figure 3.34, respectively.

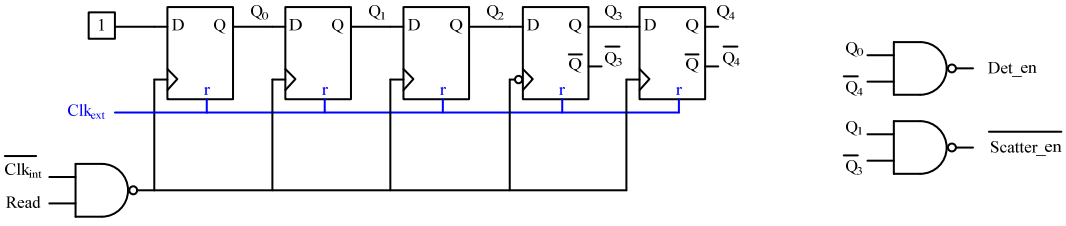


Figure 3.33: Scattering control implementation.

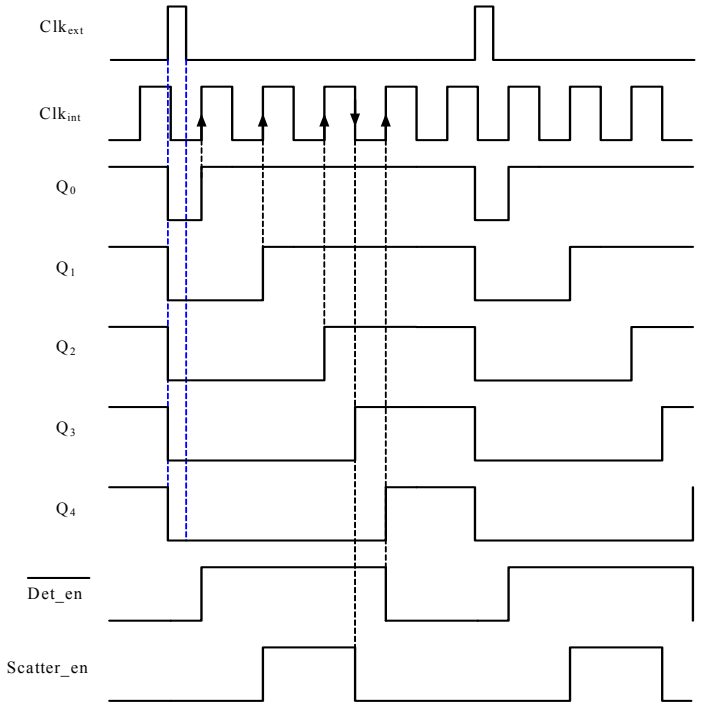


Figure 3.34: Scattering control waveforms.

3.3.3 Implementation issues

The performance of the digital control may be different after implementation due to some issues that will be discussed in this sub-section. Some of these issues can be solved by modifying the implemented logic, while others need a change in the transistor level implementation as will be explained.

3.3.3.1 Scattering glitch problem

Because the external clock and the internal clock are not synchronized, the scattering control waveforms may differ from that in Figure 3.34. If the positive edge of the internal clock is outside the external clock pulse, a short glitch can appear in the scattering control waveform as shown in Figure 3.35.

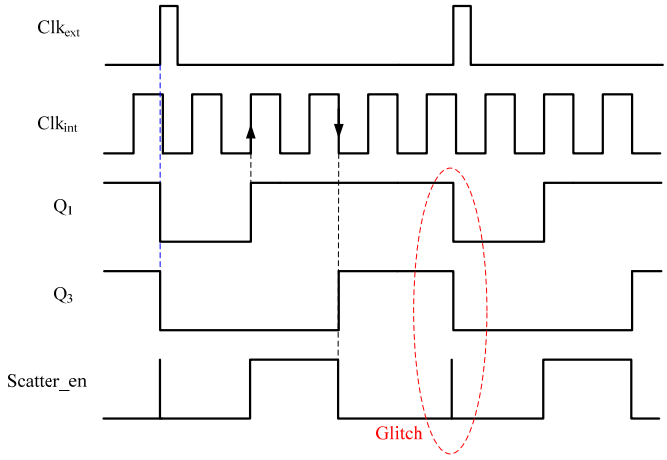


Figure 3.35: Scattering glitch.

The glitch problem can be eliminated by forcing the scattering control signal to be low when the external clock is high. This can be done using two NOR-gates as shown in Figure 3.36.

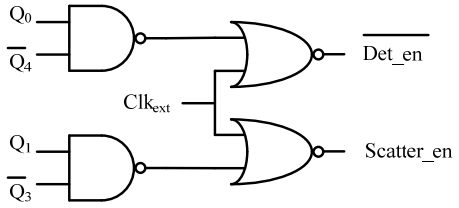


Figure 3.36: Scattering glitch solution.

3.3.3.2 Dead lock problem

The external clock that is used to control the control logic is extracted by the demodulator. But the demodulator is controlled by the control logic, i.e. the control logic determines when the demodulator is on and when it is off. This makes a closed loop containing the demodulator and the control logic. This loop should be studied carefully to avoid the instability of the RFID tag. The instability of the RFID tag can

take one of two scenarios. The first scenario is during reading mode in which the RFID tag is backscattering. The backscattering can be demodulated by the demodulator and re-injected in the control logic, as shown in Figure 3.37. This problem is unlike to occur because the backscattering control sub-block ensures that the demodulator is off during backscattering as shown in Figure 3.34.

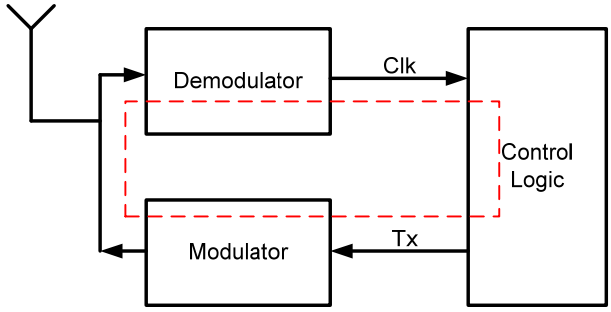


Figure 3.37: Backscattering re-injection problem.

The second scenario is more serious and can lead to a completely dead tag. If for any reason, the demodulator is off, there will be no external clock and the control logic will not be able to enable the demodulator again, as shown in Figure 3.38.

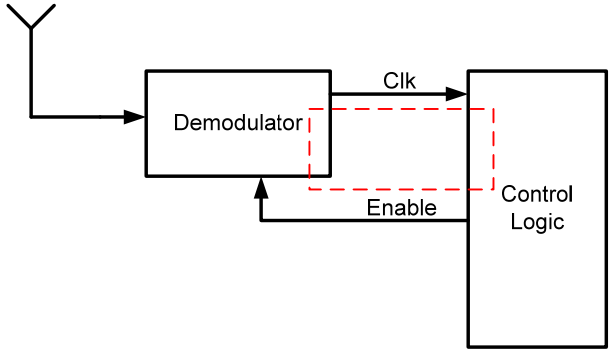


Figure 3.38: Dead lock problem.

The dead lock problem can be eliminated by ensuring that the demodulator is always active as long as the RFID tag is in address mode (READ=0). This can be achieved by adding two AND-gates as shown in Figure 3.39.

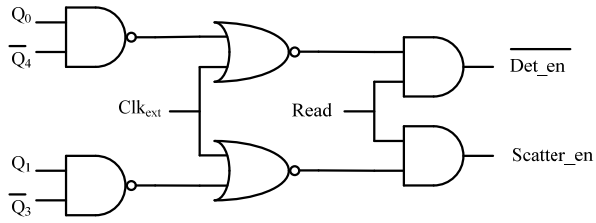


Figure 3.39: Dead lock solution.

3.3.3.3 Direct path current problem

Due to ultra low current operation, the clock extraction circuit cannot produce sharp clock edges. The extracted clock has always a significant rise and fall times. The weak slope clock can lead to an increase in power consumption when applied to the conventional static CMOS gates, [Rabaey, 03]. This increase in power consumption is because the NMOS and PMOS transistors are simultaneously ON for a significant time as shown in Figure 3.40. This causes the current to flow from the *Vdd* to the ground. The direct path current pulse can be approximated as a triangular pulse with a base length given by:

$$t_p = t_r \frac{Vdd - \left(V_{tn} + \left|V_{tp}\right|\right)}{Vdd} \approx t_r \frac{Vdd - 2 \cdot V_{tn}}{Vdd} \tag{3.39}$$

where t_r is the rise time of the clock, *Vdd* is the DC supply voltage, V_{tn}, V_{tp} are the threshold voltages of the NMOS and PMOS transistors, respectively. The height of the triangular current pulse is given by:

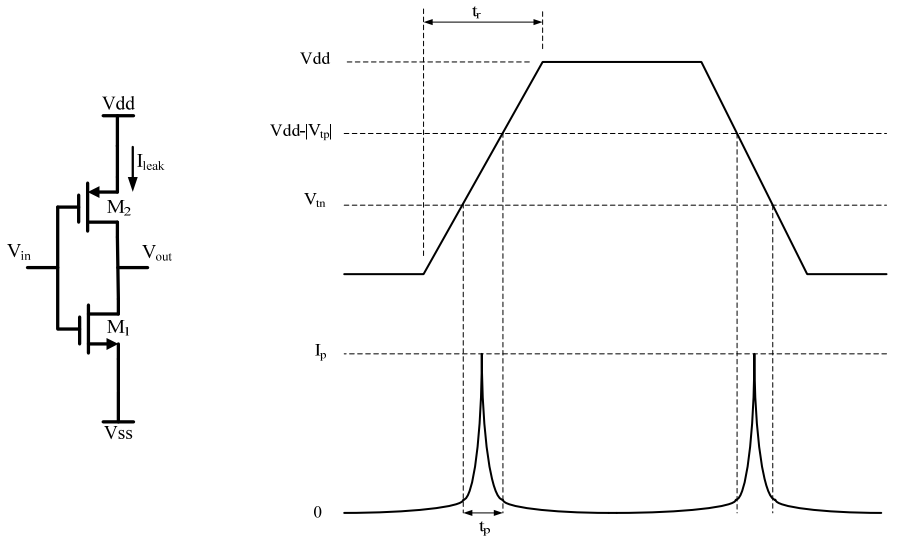
$$I_p = \frac{\mu_n C_{ox}}{2} \left(\frac{W}{L}\right)_n \left(\frac{Vdd}{2} - V_{tn}\right)^2 \tag{3.40}$$

where μ_n is the electron mobility, C_{ox} is the oxide capacitance density, *W, L* are the dimensions of the NMOS transistors. So the average leakage current due to this weak slope clock is equal to this triangular pulse area divided by the period of the clock:

$$I_{leak} = I_p \frac{2 \cdot t_p}{T_b} = 2 \cdot \mu_n C_{ox} \left(\frac{W}{L} \right)_n \left(\frac{Vdd}{2} - V_{tn} \right)^3 \frac{t_r}{Vdd \cdot T_b} \qquad (3.41)$$

where T_b is the clock period. The leakage power due this weak slope clock is given by:

$$P_{leak} = Vdd \cdot I_{leak} = 2 \cdot \mu_n C_{ox} \left(\frac{W}{L} \right)_n \left(\frac{Vdd}{2} - V_{tn} \right)^3 \frac{t_r}{T_b} \qquad (3.42)$$



(a) Inverter circuit. (b) Inverter current waveform.

Figure 3.40: Direct path current problem.

It can be deduced from equation (3.42) that the leakage power can be reduced by reducing the supply voltage or increasing the threshold voltage of the transistors. Increasing the threshold voltage of the transistor can be done by using high threshold voltage transistors. But this solution requires an extra mask which means higher cost. Decreasing supply voltage is the optimum solution in this case. Since the system is

passive and the DC voltage is generated internally, the value of the supply voltage is a design parameter that can be changed easily, [Ashry, 07]. Also decreasing supply voltage decreases the dynamic power consumption which is given by:

$$P_{dyn} = \frac{1}{T_b} Vdd^2 \cdot C_L \tag{3.43}$$

where C_L is the total load capacitance of the gate. The leakage current versus the supply voltage is shown in Figure 3.41.

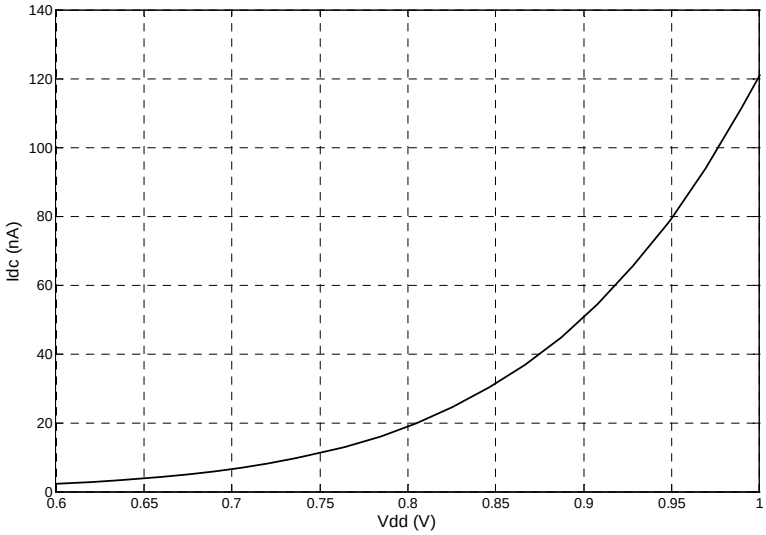


Figure 3.41: Inverter leakage current versus supply voltage.

It can be deduced from Figure 3.41 that decreasing the supply voltage from 1 V to 0.8 V can lead to great power reduction. Simulation results of the inverter using 0.8 V supply voltage are shown in Figure 3.42.

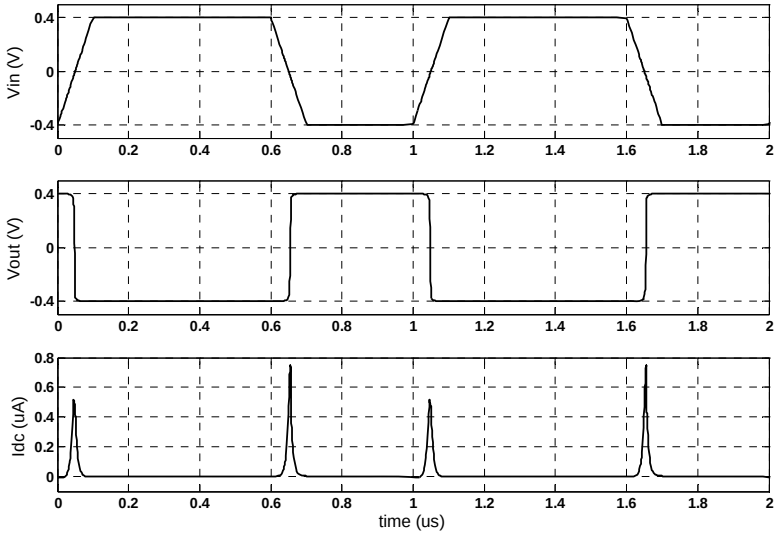


Figure 3.42: Simulation results of the inverter.

3.3.4 Simulation results

The control logic was implemented in transistor level. The simulation results of the mode selector and backscattering control are shown in Figure 3.43 and Figure 3.44, respectively.

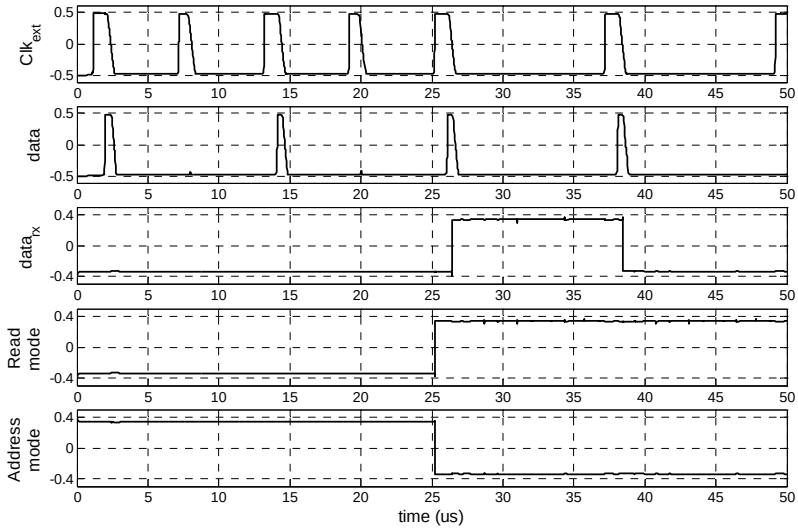


Figure 3.43: Transistor level simulation of the mode selector.

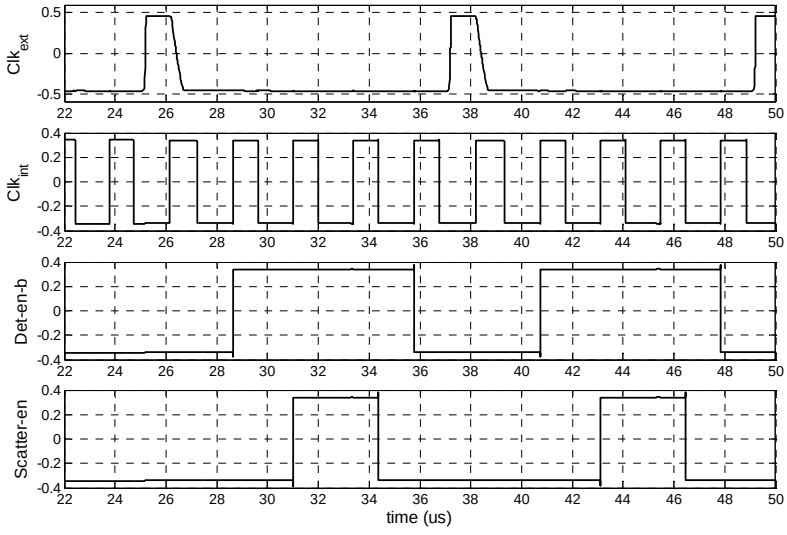


Figure 3.44: Transistor level simulation of the scattering control.

3.4 Oscillator

The clock used in the system is the extracted clock from the incoming RF signal. But for an efficient backscattering, a faster clock is needed to modulate the scattered signal. This section discusses the design of this internal clock generator.

3.4.1 Oscillator candidate topologies

The main topologies that can be used to generate the internal clock are summarized as follows:

- Phase locked loop (PLL): PLL can be used to generate a clock that with an integer multiple of the extracted clock frequency. PLL has the advantage of accurate frequency, but it consumes large power, and so PLL is not suitable for this ultra low application.
- Current starved ring oscillator: Current starved ring oscillator has much lower power consumption than PLL, but for small current, the swing of the output signal can be small, and the oscillation may not start.
- Relaxation Oscillator: Relaxation oscillator is based on the charging and discharging of a capacitor. This topology is suitable for low power and poor accuracy oscillator which is suitable for this application.

3.4.2 Operation principle

The operation of the relaxation oscillator is based on charging and discharging of the capacitor C_{osc} through two current sources as shown in Figure 3.45. The voltage on the capacitor is then applied to a Schmitt trigger circuit which has two comparison levels V_{lo} and V_{hi}. In charging mode the switch S_{up} is closed, and the switch S_{dn} is opened. This allowed the current source I_{up} to charge the capacitor C_{osc}. When the voltage on the capacitor C_{osc} reaches the higher comparison level of the Schmitt trigger V_{hi}, the output of the Schmitt trigger goes high. When the output of the Schmitt trigger goes high, the

switch S_{up} is opened and the switch S_{dn} is closed. In this case the capacitor C_{osc} discharges through I_{dn}. When the voltage on the capacitor C_{osc} reaches the lower comparison level of the Schmitt trigger V_{lo}, the output of the Schmitt trigger goes low. When the output of the Schmitt trigger goes low, the switch S_{dn} is opened and the switch S_{up} becomes closed and the oscillation cycle is repeated. The period of the generated square wave is given by:

$$T_{osc} = \frac{C_{osc}\left(V_{hi} - V_{lo}\right)}{I_{osc}} \tag{3.44}$$

where C_{osc} is the capacitance, I_{osc} is value of the charging current which is assumed to be equal to the value of the discharging current.

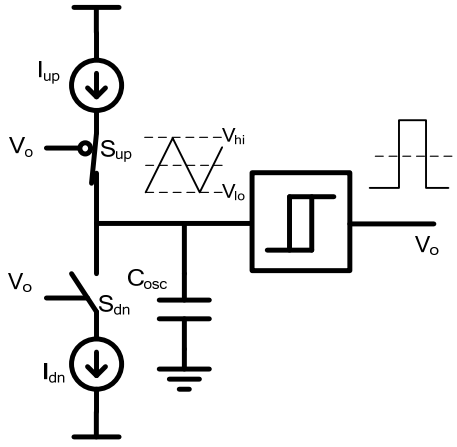


Figure 3.45: Concept of relaxation oscillator.

3.4.3 Circuit implementation

3.4.3.1 Schmitt trigger circuit implementation

The main concern when choosing the suitable circuit topology is the ultra low power consumption. The traditional op-amp based Schmitt trigger is power hungry and not

suitable for ultra low power applications. A simple and low power Schmitt trigger that was suggested in [Curty, 05] is shown in Figure 3.46.

When the input voltage to the Schmitt V_i is higher than the threshold voltage of the transistor M_6 The voltage V_p is approximately zero, M_{10} is on, and the output voltage V_o is high. On the other hand, when the input voltage to the Schmitt V_i is lower than the negative of the threshold voltage of the transistor $M_{7,}$ the voltage V_n is approximately zero, M_{11} is on, and the output voltage V_o is low. So the shown circuit acts as a non-inverting Schmitt trigger with the two comparison levels are $-V_{tp}$ and V_{tn}, where V_{tp} and V_{tn} are the threshold voltages of the PMOS and NMOS transistors respectively. The simulation results of the Schmitt trigger circuit are shown in Figure 3.47.

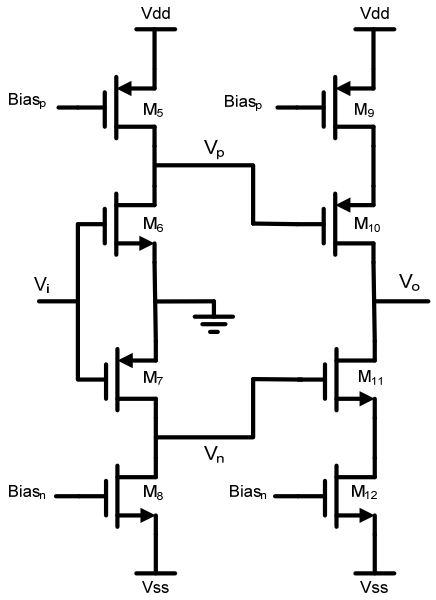


Figure 3.46: Low power Schmitt trigger.

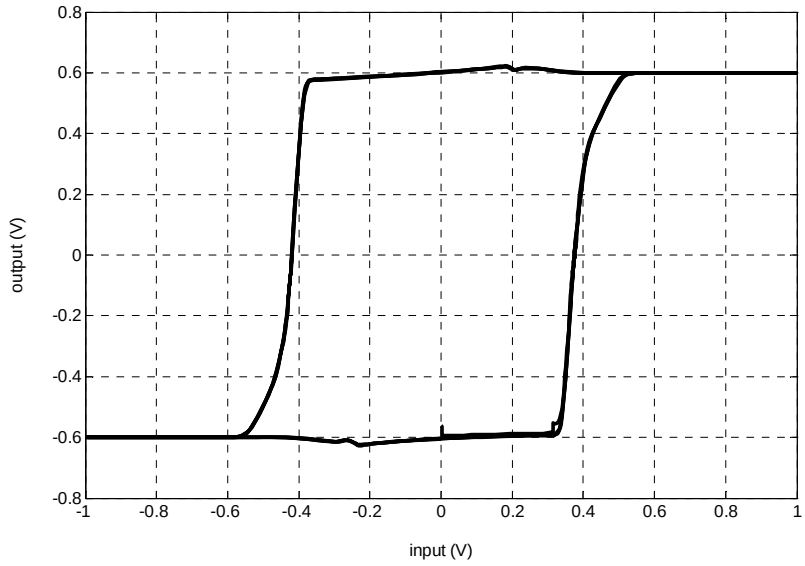


Figure 3.47: Simulation results of the Schmitt trigger circuit.

3.4.3.2 Complete circuit implementation

The complete circuit implementation is shown in Figure 3.48. The switches S_{up} and S_{dn} are implemented using transistors M_2 and M_3, respectively. An OR-gate is added to the output of the oscillator for two reasons: The first reason is to produce a sharp edges square wave with acceptable driving capabilities. The second reason is to ensure the starting of the oscillator, because the oscillator may not start if the output of the oscillator was initially mid-way between the high and low levels. The POR signal forces the output of the oscillator to be high at the end of the power-up mode. The OR-gate is implemented using the traditional static CMOS logic.

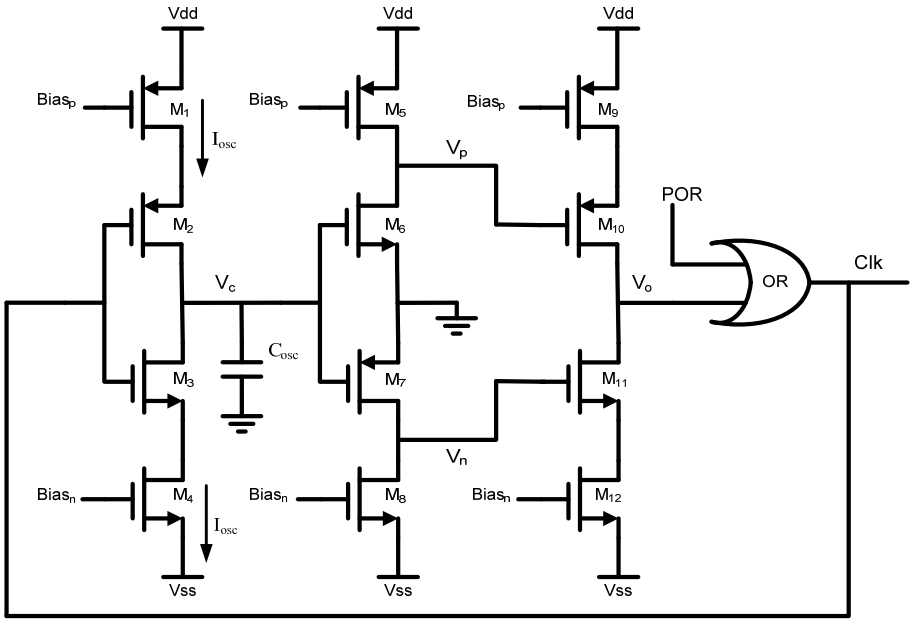


Figure 3.48: Circuit implementation of the oscillator.

The simulation results of the oscillator are shown in Figure 3.49. The period of the generated square wave is now given by:

$$T_{osc} = \frac{C_{osc}\left(V_{tn} + V_{tp}\right)}{I_{osc}} \tag{3.45}$$

where C_{osc} is the capacitance, V_{tn}, V_{tp} are the threshold voltages of the NMOS and PMOS transistors, respectively, I_{osc} is the charging and discharging current value.

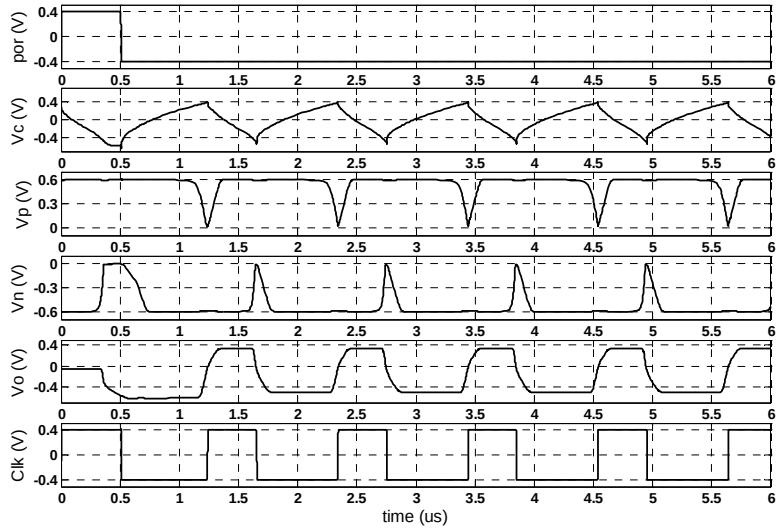


Figure 3.49: Simulation results of the oscillator circuit.

3.5 Modulator

As was described in system design section, the modulation scheme chosen is ASK-backscattering. This scheme has the advantage of simplicity and low power consumption. The modulator is simply a switch that either shorts the input impedance of the chip, or leaves it matched with the antenna as shown in Figure 3.50. The switch is implemented as a single NMOS transistor. The size of the transistor should be large enough to give a low on-resistance, but it should not be too large to avoid loading the control logic circuit which drives it.

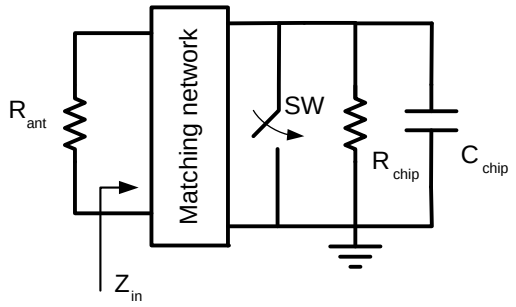


Figure 3.50: ASK-backscattering modulator.

3.6 System Simulation

The designed blocks are integrated and simulated together in circuit-level, to ensure that the RFID tag is working properly. The testbench used to simulate the RFID tag is shown in Figure 3.51. The RF signal supplied by the antenna is modeled as RF source in series with the antenna impedance. The wave forms at the different nodes of the system are shown in Figure 3.52, and Figure 3.53.

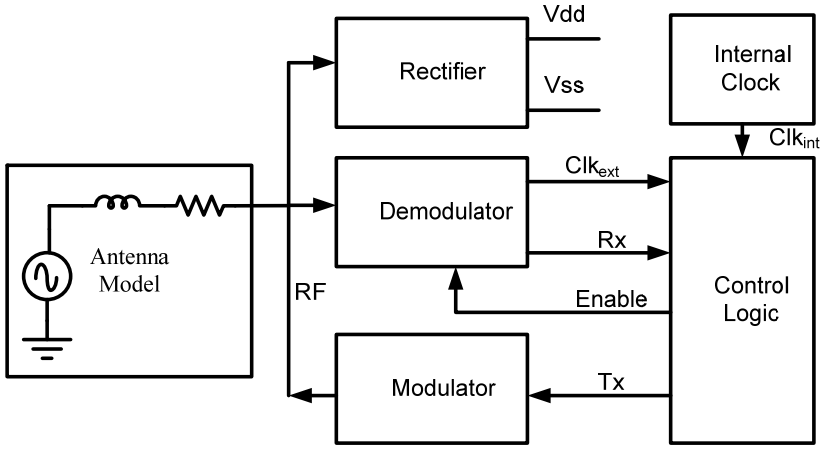


Figure 3.51: UHF RFID tag testbench.

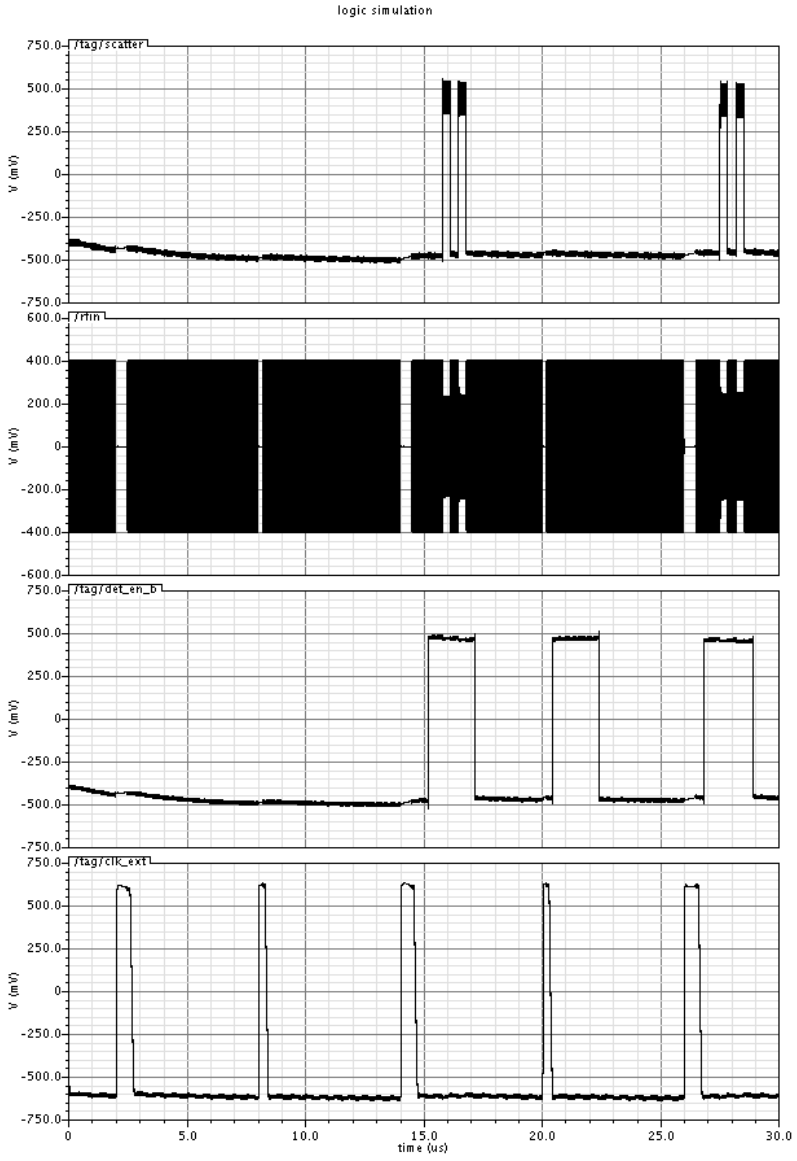


Figure 3.52: UHF RFID tag simulation results (Tx, RF, Tx Enable, Clk_{ext}).

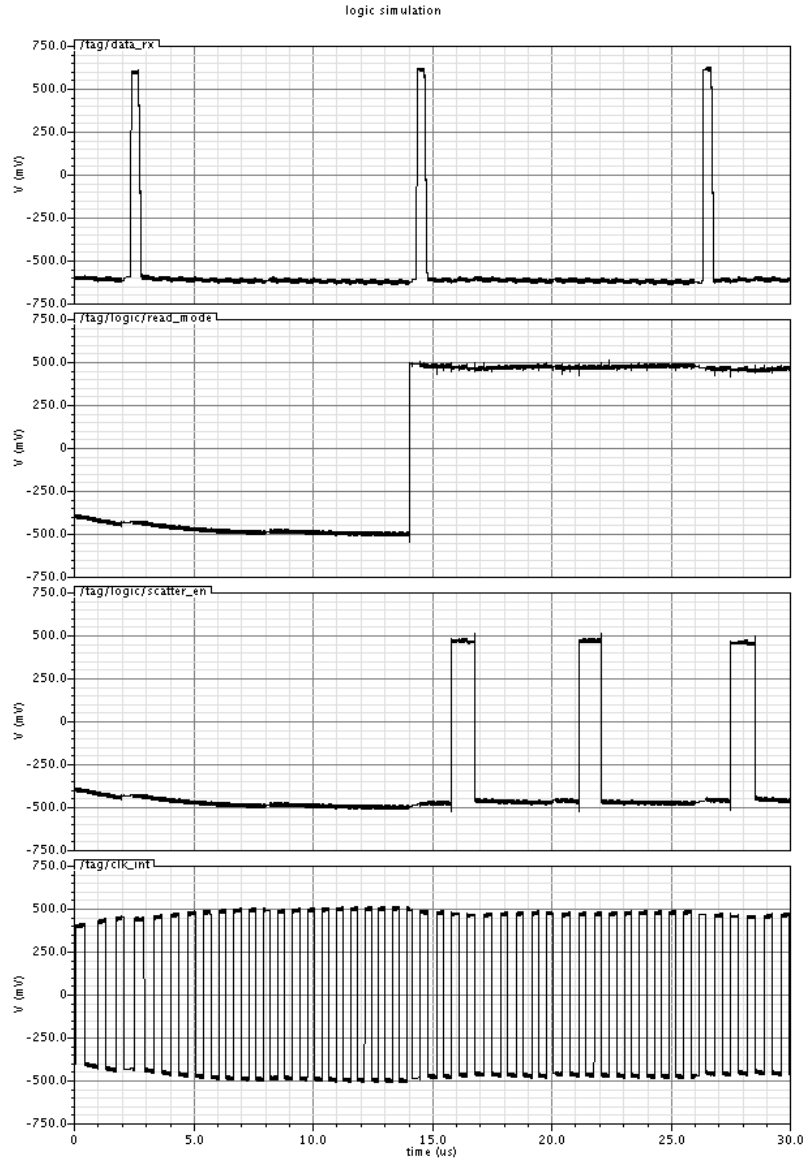


Figure 3.53: UHF RFID tag simulation results (Rx, Read, $Enable_b$, Clk_{int}).

It can be deduced from the simulation results that the RFID tag responds to the received RF signal as expected. The clock and the data are extracted, and the system

jumps to the Read mode, when the pattern is recognized. The RFID tag sends its output as a backscattered sequence, which can be noticed as notches in the RF signal.

3.7 Summary

An RFID tag chip was designed using 0.13 µm standard CMOS process. The power consumption of the digital part is optimized by using separate low supply voltage of 0.8 V. The analog part has a supply voltage of 1.2 V. All the analog circuits are optimized for ultra low power operation. A current consumption of 0.5 µA for digital part and 0.5 µA for analog part was achieved. The area of the chip including the RF pads is 140 µm x 230 µm. The layout of the RFID tag chip is shown in Figure 3.54.

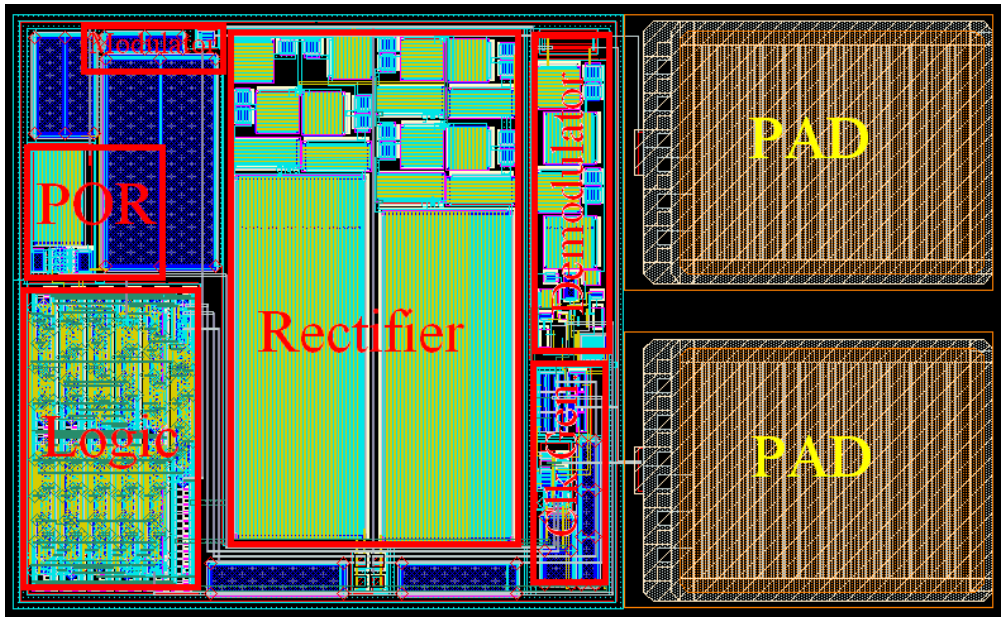


Figure 3.54: UHF RFID Tag chip layout.

A comparison between the achieved specifications and the similar work of some other authors is shown in Table 3-2.

Table 3-2: Performance comparison.

	Process	freq.	power	area	eff.	notes
This work	standard CMOS 0.13 μm	900 MHz	1 μW	0.14 mm x 0.23 mm	32%	simulated
[Karthaus, 03]	CMOS 0.5 μm, Schottky diodes	900 MHz	2.3 μW	NA	18%	measured
[Curty, 05]	0.5 μm Si-on-Sap.	2.4 GHz	1 μW	0.4 mm x 0.5 mm	37%	measured
[Usami, 04]	standard CMOS 0.18 μm	2.4 GHz	1.5 μW	0.3 mm x 0.3 mm	NA	measured

The comparison shows that the achieved simulated work has a competitive area and power consumption. Although [Curty, 05] has achieved a better conversion efficiency, the process used is rather a special expensive process not a standard CMOS technology. Using standard CMOS technology makes the design cheaper to manufacture and easier to integrate with other systems.

Chapter 4

HF RFID Temperature Sensor

This chapter presents the design of an inductively coupled RFID tag to be used as a temperature sensor for medical applications. The RFID tag can be attached to the patient, or implanted just under his skin.

Human body temperatures are so important. The nominal body temperature indicated by the RFID tag is used as one of the vital signs routinely monitored as an indicator of a state of a person or animal health.

The application area of the RFID combined with the temperature sensor can be extended to environmental monitoring, food quality monitoring, and many other industrial applications.

4.1 Frequency Band Selection

As was explained before, the frequency of operation of the RFID system should be chosen carefully for optimum operation. There are some concerns that should be taken into consideration when choosing the frequency of operation of this RFID system:

- The RFID tag is targeting medical applications, so the selected frequency should not be harmful to the patients who are near this RFID system.
- The RFID tag can be implanted in the patient body, so the selected frequency must be capable of penetrating the skin of the human body.
- The RFID reader used to communicate with the RFID tag will not be far from it, so the communication distance need not be very long and the near field communication is more suitable.

Based on the above concerns, the most suitable frequency for this RFID system is the high frequency range (HF) which lies around 13.56 MHz. This frequency band has many advantages to make it the best candidate for operation in medical applications:

- Unlike the UHF and the microwave, the HF range is not harmful to human body. There are no claims that this range has harmful magnetic or thermal effects on the human body.
- The HF range can penetrate the human skin easily. On the other hand the UHF and the microwave ranges are strongly attenuated in human body.
- The HF is low enough to operate efficiently using magnetic coupling. Magnetic coupling or inductive coupling is based on using the antenna in its near field region. This technique is very power efficient for short range communications (< 1 m) which is the case in this application.
- The HF RFID tag is much smaller than its LF counter part, because the size of the coil used in inductive coupling is inversely proportional to the frequency of operation.

4.2 System Architecture

The architecture of the HF RFID tag is not much different than the common RFID tag architecture that was described in the UHF RFID tag in Chapter 2. However, some modifications are applied to meet our medical applications.

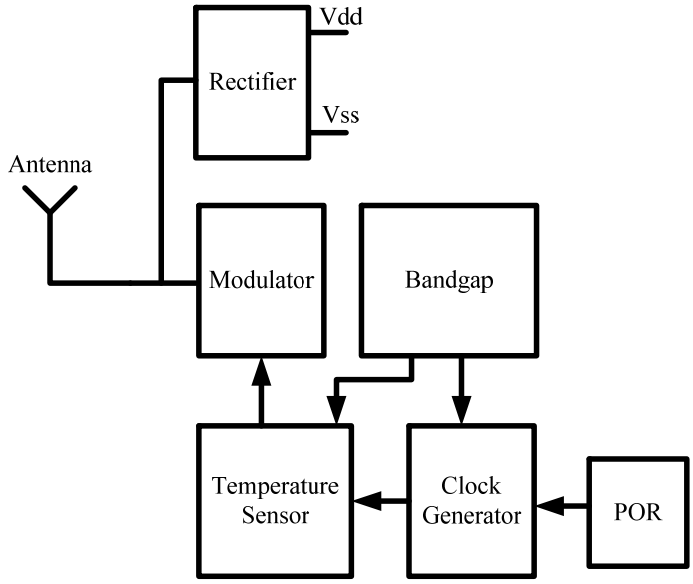


Figure 4.1: HF RFID tag block diagram.

There are some blocks that are almost identical to those used in the UHF RFID tag:

- Rectifier: This is an essential block in any passive RFID tag that provides the DC voltage needed to supply the system blocks.
- Clock generator: This block provides an internally generated square wave to drive the digital circuits in the temperature sensor.
- Modulator: This block is the transmitter of the system which transmits the temperature reading to the RFID reader.

Some blocks that were used in the UHF RFID tag do not exist in this HF RFID tag system architecture:

- Demodulator: The communication protocol of the HF RFID system does not require the RFID reader to send commands to the RFID tag, so the demodulator is no longer needed.
- Control logic: The communication protocol of the HF RFID tag is much simpler than the UHF RFID tag. The control logic needed is much smaller and is implicit in the temperature sensor block.

The extra blocks that were not used in the UHF RFID tag are:

- Bandgap: This block provides a temperature independent current and a Proportional-To-Absolute-Temperature (PTAT) current. Both currents are needed to drive the clock generator and the temperature sensor.
- Temperature sensor: This block is the responsible for sensing the temperature and converting to a digital stream to drive the modulator.

4.3 Communication Protocol

The communication protocol between the RFID reader and the RFID tag is much simpler. In this application there is a single RFID reader and a single RFID tag. So, there is no need for the sophisticated addressing and handshaking protocols which are used in the case of multi RFID tags.

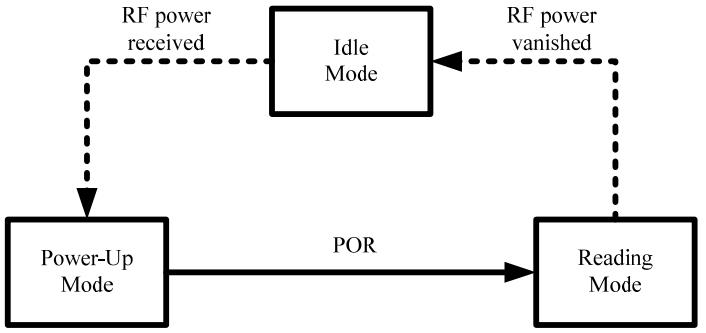


Figure 4.2: Modes of operation.

The RFID tag has three modes of operation as shown in Figure 4.2:

1- Idle mode: In this mode the RFID tag is completely dead. No DC voltage exists in the chip and consequently all the RFID tag blocks are off. All what the RFID tag can do in this mode is to wait for the reader to send the RF signal.

2- Power-up mode: The RFID tag enters this mode when the RFID reader starts to send a continuous RF signal. The RFID tag stays in this mode until it builds its DC voltage. After the generated DC voltage exceeds a certain threshold, a POR (Power ON Reset) signal is generated to reset the chip.

3- Reading mode: In this mode, the RFID tag sends a digital stream that encodes the temperature reading. The RFID tag stays in this mode until the RF signal vanishes.

Chapter 5

HF RFID Temperature Sensor Circuits Design

In this chapter the design of the HF RFID temperature sensor in 0.13 μm standard digital CMOS technology is demonstrated. The chapter starts with system description and design. Then the various blocks of the system are analyzed and designed. Finally the simulations results of the system and the chip layout are shown.

5.1 Rectifier

As was mentioned in the UHF RFID tag, the rectifier is an essential part of the RFID tag. The concept and the circuits used to generate the DC voltage is the same, except for some minor changes:

- The current consumed in the HF RFID tag is more (around 6 μA compared to 1 μA in the UHF RFID tag). This makes the rectifier circuit designed for the UHF RFID not suitable here, because the efficiency of the rectifier is a strong function of the output DC current as was shown in the rectifier analysis listed in section 3.1.1. However, the designed rectifier circuit can be used with the same

optimum efficiency using a simple scaling technique. If m optimized rectifier cells are connected in parallel as shown in Figure 5.1, the output voltage from the combination is the same as a single rectifier cell, while the output current is multiplied by the factor m. The input power to the parallel combination is also multiplied by the factor m, so the conversion efficiency of this parallel combination is the same as the single optimized rectifier cell. So the same rectifier cell that was used in the UHF RFID tag can be used, but the transistors should be scaled up by the current ratio to keep the rectifier working at the same optimum efficiency.

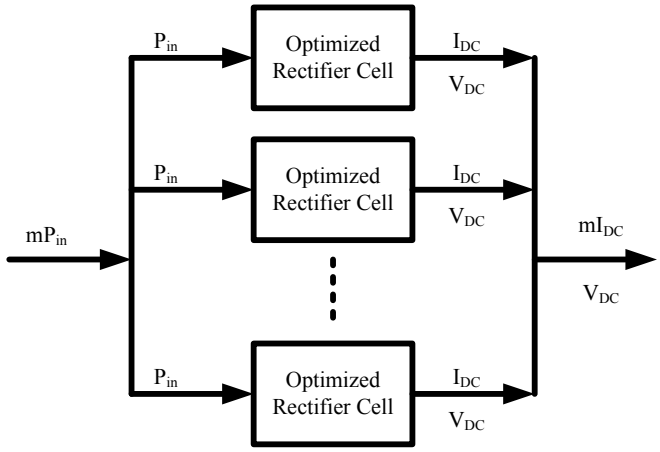


Figure 5.1: Rectifier scaling.

- The second difference between the rectifier circuit in the UHF and HF case is the difference in frequency. The UHF RFID tag works at around 900 MHz, while the HF RFID tag works at 13.56 MHz. To avoid the re-design of the rectifier circuit, a similar scaling technique is used. To keep the impedance of the capacitors the same in the UHF and the HF case, the area of the capacitor is scaled up with the inverse of the frequency ratio. (I.e. the capacitors in the HF rectifier are scaled up by a factor of 900/13 ≈ 67). This technique should be applied to the coupling capacitors as well as the smoothing capacitors.

- Another difference between the rectifier circuit in the HF and the UHF case is the digital and the analog supplies. In the UHF RFID tag, the analog part needs 0.5 μA, and the digital part also needs 0.5 μA. This makes it efficient to separate the analog and digital supplies, because the digital part can save much power if it operates at a lower dc voltage. In the HF RFID tag, the digital part is very small compared to the analog part, and power consumed by the digital gates is negligible compared to the power dissipated in the analog part. So, separating the analog and the digital supplies in the HF RFID tag leads to more complexity without any significant power saving.

5.2 Bias Cell

The bias cell is an important part in any analog design, because it provides the needed bias voltages and currents. However, in this system, the currents generated by the bias cell are not used mainly for biasing the circuits; they are used to measure the temperature of the chip environment. The bias cell generates a Proportional-To-Absolute-Temperature (PTAT) current and a constant current. Both currents are used by the sigma-delta ADC to produce a digital stream that encodes the temperature.

5.2.1 PTAT Current

The Proportional-To-Absolute-Temperature (PTAT) current can be produced using the circuit shown in Figure 5.2. The feedback forces the two nodes x and y to have the same voltage, and the mirroring between M_1 and M_2 forces the current in the two branches to be identical. The voltage of the node x is given by:

$$V_x = V_T \cdot \ln\left(\frac{I_{ptat}}{I_s}\right) \tag{5.1}$$

where V_T is the thermal voltage, and I_s is the saturation current of the BJT Q_1. The voltage of the node y is given by:

$$V_y = V_T \cdot \ln\left(\frac{I_{ptat}}{m \cdot I_s}\right) + I_{ptat} R_p \tag{5.2}$$

where m is the ratio between the emitter area of Q_2 and Q_1. By equating V_x and V_y we get:

$$I_{ptat} R_p = V_T \cdot \ln(m) \tag{5.3}$$

So the output current from this circuit is proportional to the thermal voltage, consequently it is proportional to the absolute temperature.

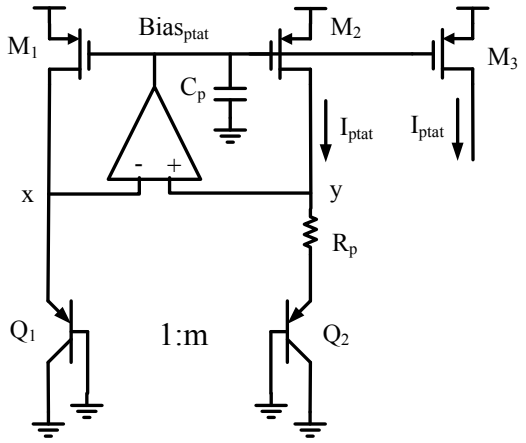


Figure 5.2: PTAT current circuit.

Since the PTAT circuit is based on a feedback loop, the stability of the circuit should be studied to ensure that no instability exist in its operation. Using the small signal model, the loop gain is given by:

$$LG = A \cdot g_m \left(\left(r_o \parallel r_e \right) - \left(r_o \parallel \left(R_p + r_e \right) \right) \right) \tag{5.4}$$

where A is the voltage gain of the OTA, g_m, r_o are the transconductance and the output resistance of the transistors M_1 and M_2, respectively, r_e is the equivalent small signal resistance at the emitters of the BJTs Q_1 and Q_2, respectively. It should be noted that the transistors have the same small signal parameters, because they have the same current and the same size. Also the equivalent small signal resistance of the two BJTs Q_1 and Q_2 are the same because they have the same dc current. If r_o is much larger than R_p and r_e is much smaller than R_p, the loop gain can be approximated as:

$$LG \approx -Ag_m R_p \tag{5.5}$$

The overall loop gain is negative which ensure that the loop is stable at dc, but it should be studied at all frequencies to make sure that it is stable for all frequencies. The dominant pole of the loop exists at the output node of the OTA. The dominant pole is given by:

$$P_1 = \frac{1}{2\pi \cdot r_{ota} C_p} \tag{5.6}$$

where r_{ota} is the output resistance of the OTA, C_p is the total capacitance at the output node of the OTA. The first non-dominant pole of the loop exists at the positive input terminal of the OTA. It is approximately given by:

$$P_2 \approx \frac{1}{2\pi \cdot R_p C_g} \tag{5.7}$$

where C_g is the input capacitance of the OTA. The phase margin of the PTAT loop is given by:

$$PM = \tan^{-1}\left(\frac{P_2}{P_1}\right) \approx \tan^{-1}\left(\frac{r_{ota}}{R_p}\frac{C_p}{C_g}\right) \tag{5.8}$$

The phase margin of the loop can be improved by adding extra capacitance to increase C_p. The simulation results of the PTAT loop are shown in Figure 5.3. It can be deduced

from the figure that the phase margin is about 80 degrees and the gain margin is about 26 dB.

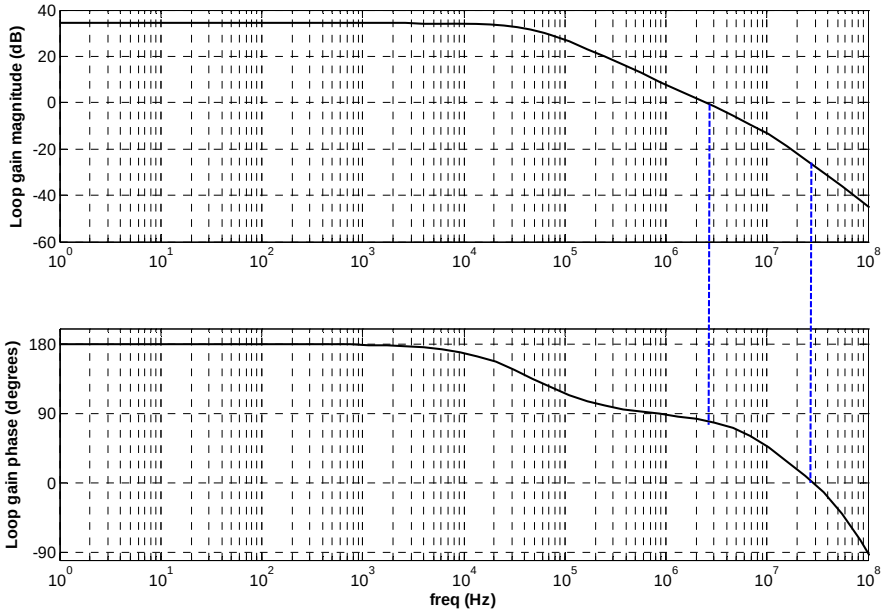


Figure 5.3: Stability of the PTAT loop.

5.2.2 CTAT Current

The constant current can be obtained by adding the PTAT current which has a positive slope with the temperature to another current with a negative slope with temperature. The most common way to generate this current is to produce a current proportional to the voltage across the p-n junction V_{be}. This current is referred to as CTAT (Complementary-To-Absolute-Temperature) current. The feedback loop forces the node z to track the voltage of V_{be} as shown in Figure 5.4, and the CTAT current is given by:

$$I_{ctat} = \frac{V_{be}}{R_n} \tag{5.9}$$

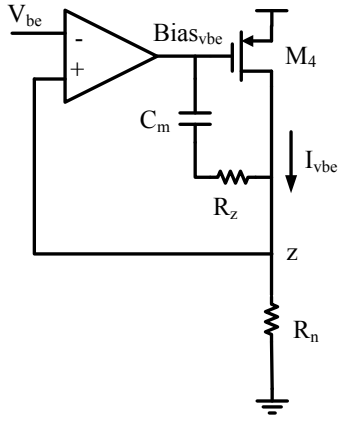


Figure 5.4: CTAT current.

The loop gain of the CTAT loop is given by:

$$LG \approx -Ag_m R_n \tag{5.10}$$

where A is the voltage gain of the OTA, g_m is the transconductance of the transistor M_4. The dominant pole of the CTAT loop also exists at the output node of the OTA and is given by, [Razavi, 01]:

$$P_1 = \frac{1}{2\pi \cdot r_{ota} C_p} \tag{5.11}$$

where r_{ota} is the output resistance of the OTA, C_p is the total capacitance at the output node of the OTA. The non-dominant pole exists at positive input terminal of the OTA and is given by [Razavi, 01]:

$$P_2 \approx \frac{1}{2\pi \cdot R_n C_g} \tag{5.12}$$

where C_g is the input capacitance of the OTA. Miller compensation is used to stabilize the loop. The capacitor C_m is used to split the two poles of the loop, i.e. the dominant pole moves to lower frequencies while the non-dominant pole moves to higher frequencies. After miller compensation, the dominant pole is given by:

$$P_1^{'} = \frac{1}{2\pi \cdot r_{ota} C_m \cdot g_m \cdot R_n} \tag{5.13}$$

and the non-dominant pole is given by:

$$P_2^{'} = \frac{g_m}{2\pi \cdot C_g} \tag{5.14}$$

But miller compensation introduces a RHP zero which degrades the phase margin of the loop, so a resistor R_z is added in series with C_m. If the value of R_z is equal to the inverse of the transconductance g_m, the RHP zero is cancelled, [Razavi, 01]. The simulation results of the CTAT loop are shown in Figure 5.5. It can be deduced from the figure that the phase margin is about 90 degrees and the gain margin is about 12 dB.

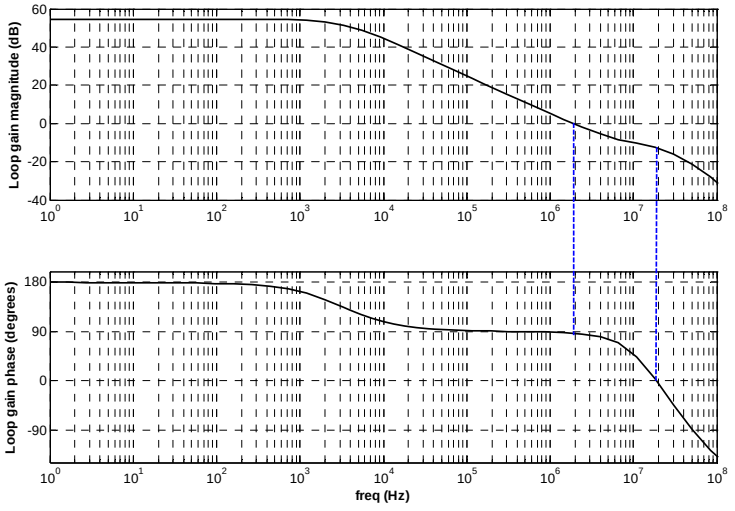


Figure 5.5: Stability of the CTAT loop.

5.2.3 Constant current

The constant current with the temperature is obtained by adding the PTAT current to the CTAT current with proper weights. The complete circuit of the bias cell is shown in Figure 5.6. To ensure the stability of the overall bias cell, a step is applied at the *Vdd*. The simulation results are shown in Figure 5.7. It can be deduced from the step response of the bias cell that no ringing exists and the circuit is stable.

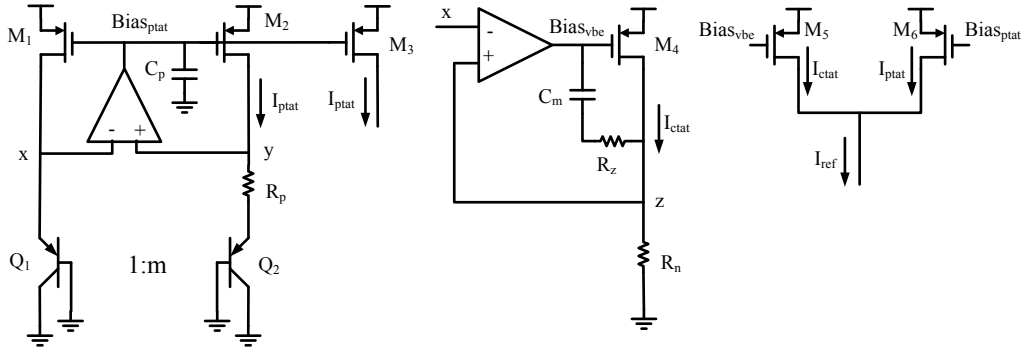


Figure 5.6: Current mode bandgap circuit.

The variation with temperature of the generated PTAT current and the constant current are simulated and shown in Figure 5.8. The ratio between the PTAT current and the reference current should be sufficiently linear with temperature to ensure good accuracy of the temperature reading. The linearity of the current with temperature, and the percentage error in this linearity are shown in Figure 5.9, and Figure 5.10, respectively.

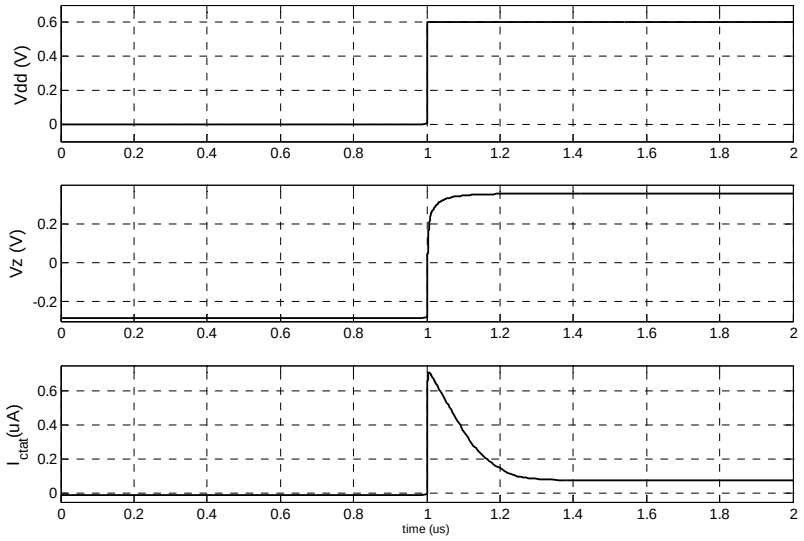


Figure 5.7: Step response of the bandgap circuit.

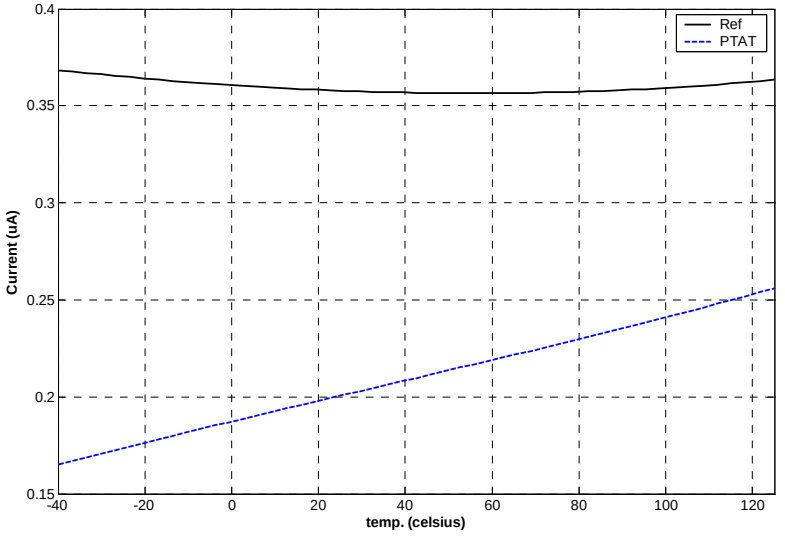


Figure 5.8: PTAT and reference current versus temperature.

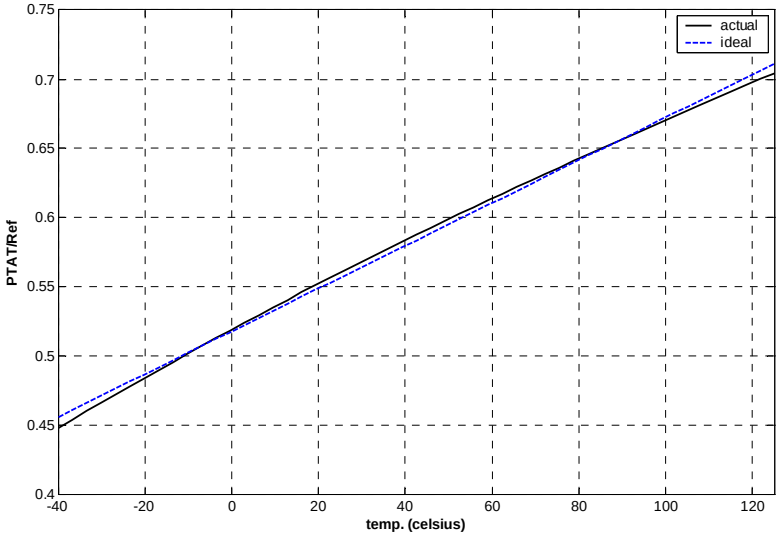


Figure 5.9: Linearity of the PTAT current.

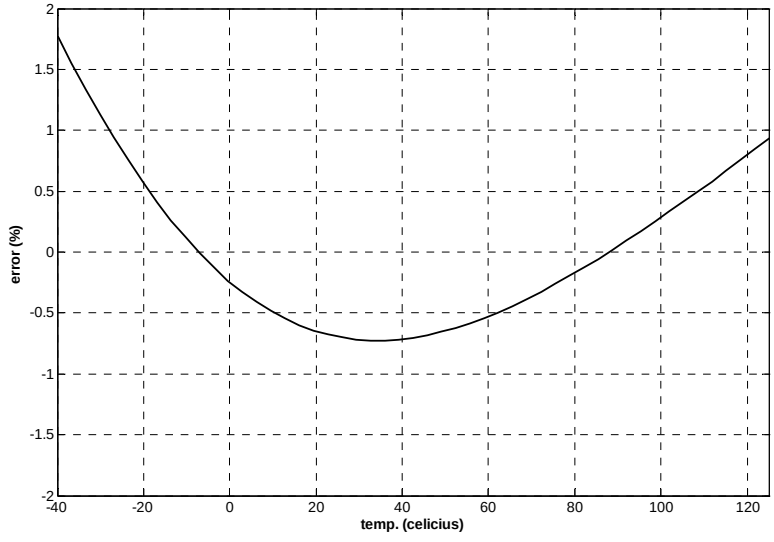


Figure 5.10: Percentage error in PTAT current compared to ideal case.

5.3 Sigma-Delta ADC

5.3.1 Introduction

The purpose of this RFID tag is to sense the temperature and transmit it to the RFID reader. The bias cell generates a proportional-to-temperature current that can be used as a measure of temperature, [Pertijs, 05]. An analog to digital converter is needed to convert this current to the corresponding digital value to be transmitted to the RFID reader. First order continuous-time sigma-delta ADC has the advantage of very simple structure and low power consumption. The block diagram of the first order sigma-delta ADC is shown in Figure 5.11. The measured PTAT current is integrated and then applied to a clocked comparator. The sigma-delta loop ensures that the output stream has an average value equal to the ratio between the PTAT current and the reference current.

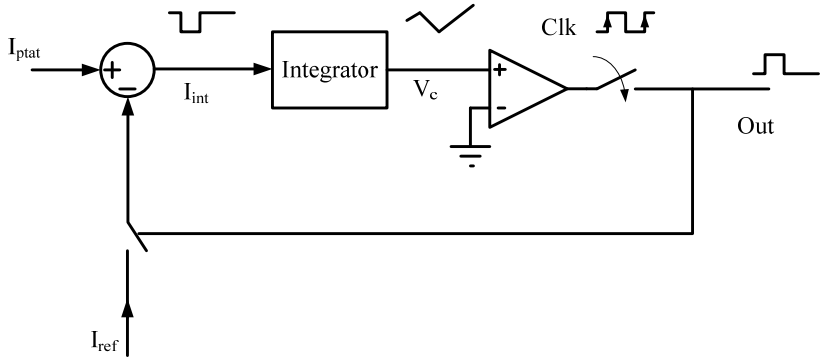


Figure 5.11: Block diagram of the sigma-delta ADC.

5.3.2 Modeling Sigma-Delta ADC in Simulink

In order to study the operation of the sigma-delta ADC, it will be modeled and simulated in system level using Simulink. The modeling starts with the basic ideal blocks, and then the non-idealities of the system are added.

5.3.2.1 Continuous-Time model

The continuous-time model of the sigma-delta ADC is the direct implementation of the system blocks, as shown in Figure 5.12. The continuous-time model is used to simulate the waveforms at the different nodes of the system. The simulation results of the continuous-time model of the sigma-delta ADC are shown in Figure 5.13.

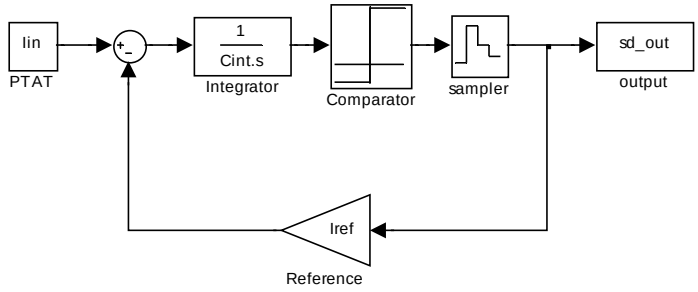


Figure 5.12: Simulink continuous-time model of the sigma-delta ADC.

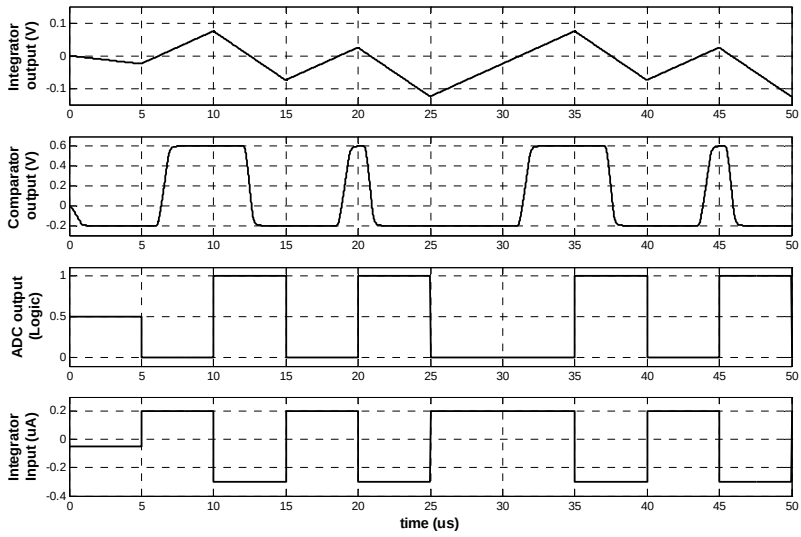


Figure 5.13: Simulink simulation results of the sigma-delta ADC.

5.3.2.2 Discrete-Time Equivalent model

The continuous-time model of the sigma-delta ADC is difficult to analyze and simulate. The simulation of the continuous-time model is very slow, because the time step of the simulation must be much smaller that the sampling period to obtain accurate results. On, the other hand, the discrete time sigma-delta ADC simulation is very fast, because only one sample is needed per clock cycle. So it is desirable to derive a discrete time equivalent model for the continuous time ADC to use it in simulation and optimization.

5.3.2.2.a Discrete-Time Equivalent model Derivation

It was shown in [Shoaei, 94] that any continuous time ADC has a perfectly equivalent discrete time model that can be derived using mapping of poles. The continuous time transfer function is expressed as:

$$H(s) = \sum_{k=1}^{n} \frac{B_k}{s - s_k} \tag{5.15}$$

where B_k is a constant, s_k is the continuous time pole, and n is the order of the transfer function. The equivalent discrete time is given by:

$$H(z) = \sum_{k=1}^{n} \frac{A_k}{z - z_k} \tag{5.16}$$

where z_k is the discrete time pole which is given by:

$$z_k = e^{s_k T_s} \tag{5.17}$$

where T_s is the sampling period. The constant A_k is given by:

$$A_k = \frac{B_k}{s_k}\left(e^{s_k T_s} - 1\right) \tag{5.18}$$

For a special case of the ideal integrator where the single pole of the system lies at the DC, i.e. the continuous time transfer function is given by:

$$H(s) = \frac{1}{s} \tag{5.19}$$

The equivalent discrete time transfer function is given by:

$$H(z) = \frac{T_s}{z-1} \tag{5.20}$$

5.3.2.2.b Ideal Sigma-Delta ADC

The loop filter of the ideal first order sigma-delta ADC is an integrator. The continuous-time transfer function of sigma-delta ADC loop is given by:

$$H(s) = \frac{I_{ref} A}{C_{\text{int}}} \frac{1}{s} \tag{5.21}$$

where I_{ref} is the reference current, C_{int} is the integration capacitance, and A is the gain of the comparator. Using the method derived in the previous section, the discrete-time equivalent model of the ideal sigma-delta ADC is given by:

$$H(z) = \frac{I_{ref} A T_s}{C_{\text{int}}} \frac{1}{(z-1)} \tag{5.22}$$

The discrete-time model of the ideal sigma-delta ADC is shown in Figure 5.14.

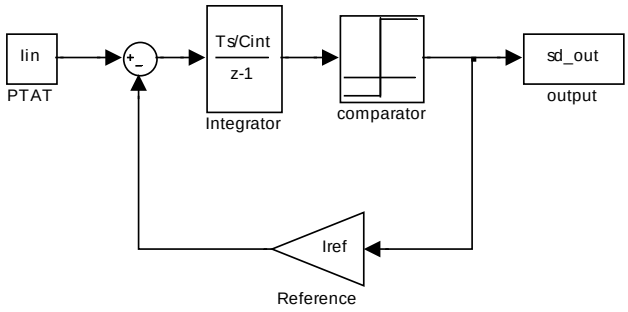


Figure 5.14: Simulink discrete-time model of the ideal sigma-delta ADC.

5.3.2.2.c Effect of the comparator finite BW

In the previous section, the effect of the finite BW of the comparator was neglected, i.e. the comparator was assumed to have an infinite BW. In practice the OTA has a limited BW. When the pole of the comparator is considered, the transfer function of the sigma-delta ADC becomes:

$$H(s)=\frac{I_{ref}}{C_{\text{int}}}\frac{1}{s}\frac{A\omega_p}{s+\omega_p} \tag{5.23}$$

where ω_p is the pole of the comparator. By expanding it to partial fractions we get:

$$H(s)=\frac{I_{ref}A}{C_{\text{int}}}\left(\frac{1}{s}-\frac{1}{s+\omega_p}\right) \tag{5.24}$$

Therefore, the discrete time equivalent model transfer function becomes:

$$H(z)=\frac{I_{ref}AT_s}{C_{\text{int}}}\left(\frac{1}{z-1}-\left(\frac{1-e^{-\omega_p T_s}}{\omega_p T_s}\right)\frac{1}{z-e^{-\omega_p T_s}}\right) \tag{5.25}$$

$$H(z)=\frac{I_{ref}AT_s}{C_{\text{int}}}\left(\frac{1}{z-1}+\frac{N_k}{z-z_k}\right) \tag{5.26}$$

$$H(z)=\frac{I_{ref}AT_s}{C_{\text{int}}}\left(\frac{(N_k+1)z-(z_k+N_k)}{(z-1)(z-z_k)}\right) \tag{5.27}$$

Finally we can put it as a cascaded poles system:

$$H(z)=\frac{I_{ref}AT_s}{C_{\text{int}}}\frac{1}{(z-1)}\left(\frac{(N_k+1)z-(z_k+N_k)}{(z-z_k)}\right) \tag{5.28}$$

The first pole is the ordinary term which accounts for the integration, while the second term accounts for the comparator pole. As the pole of the comparator corresponds to the high impedance output node, it is more realistic to put the second pole after the gain stage of the comparator, as shown in Figure 5.15.

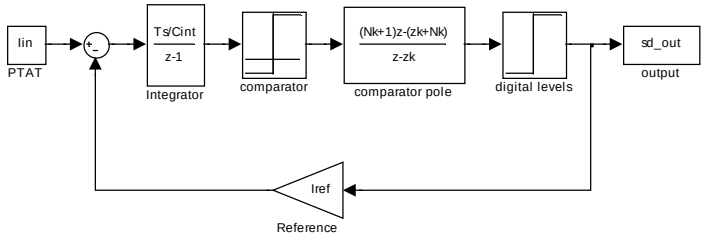


Figure 5.15: Simulink discrete-time model of the sigma-delta ADC with leakage.

5.3.2.2.d Effect of the integrator leakage

In the previous analysis, it was assumed that the integrator is ideal, i.e. it has infinite gain at DC. In practice there is a leakage resistance in parallel with the integrator capacitor which limits the DC gain. It can be modeled as shown in Figure 5.16.

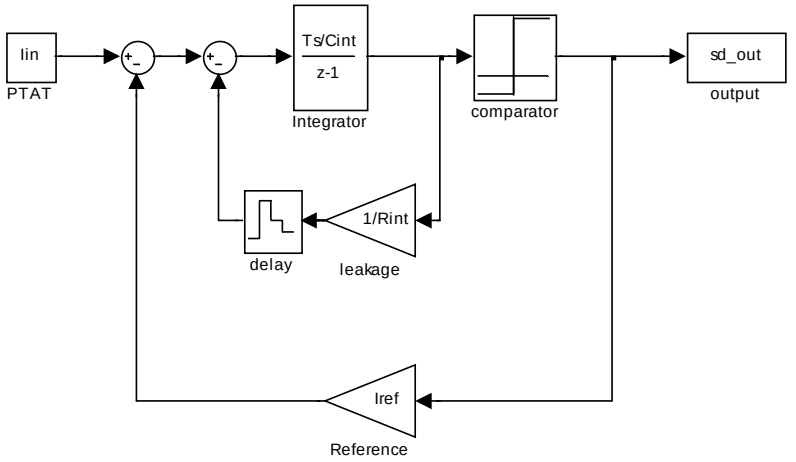


Figure 5.16: Simulink DT model of the sigma-delta ADC with leakage.

The integrator impedance versus frequency is shown in Figure 5.17. Instead of ideal integrator, the frequency response is a low pass filter. The cut-off frequency of the low pass filter is given by:

$$\omega_{\text{int}} = \frac{1}{R_{\text{int}} C_{\text{int}}} \tag{5.29}$$

where R_{int} is the leakage resistance of the integrator. The finite DC gain of the integrator degrades the noise shaping of the sigma-delta ADC. The DC notch of the ideal sigma-delta ADC is flattened as shown in Figure 5.18. This effect degrades the SNR of the sigma-delta ADC, especially for large OSR. To enhance the SNR, the cut-off frequency of the integrator should be moved to the DC. This can be done be increasing either R_{int} or C_{int}. Since R_{int} is difficult to control, the possible solution is to increase C_{int}. The SNR of the sigma-delta ADC enhances as the integrator capacitance C_{int} increases as shown in Figure 5.19. However, increasing the integrator capacitance C_{int} reduces the signal swing at the integrator output which is given by:

$$\Delta V = \frac{I_{ref} T_s}{C_{\text{int}}} \tag{5.30}$$

The decrease in voltage amplitude at the integrator output increases the required gain from the OTA. Designing an OTA with a high gain and sufficient bandwidth is a problem in this low power system. So the value of the integrator capacitance C_{int} is chosen as a compromise between acceptable integrator leakage and sufficient signal swing at the OTA input.

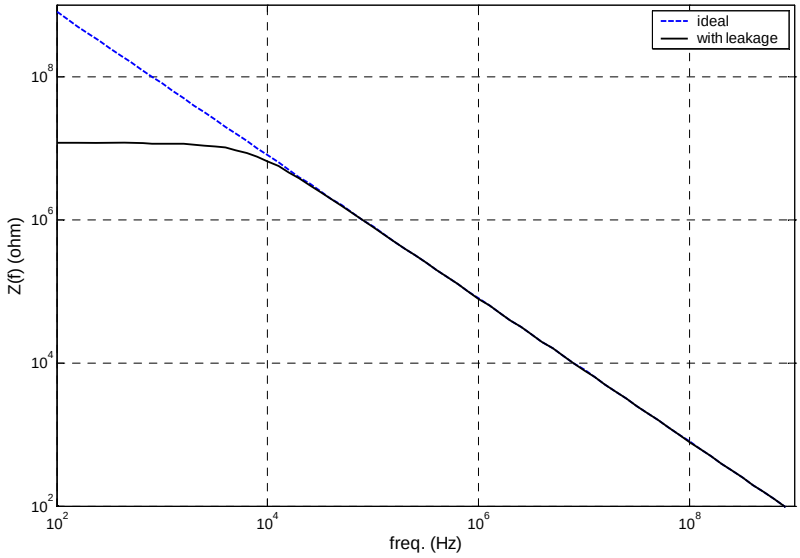


Figure 5.17: Impedance of the integrator with leakage.

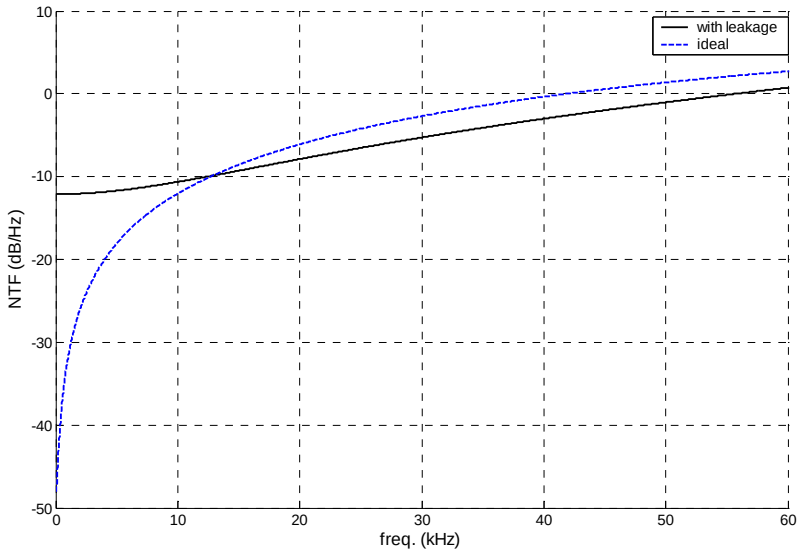


Figure 5.18: Leakage effect on noise shaping.

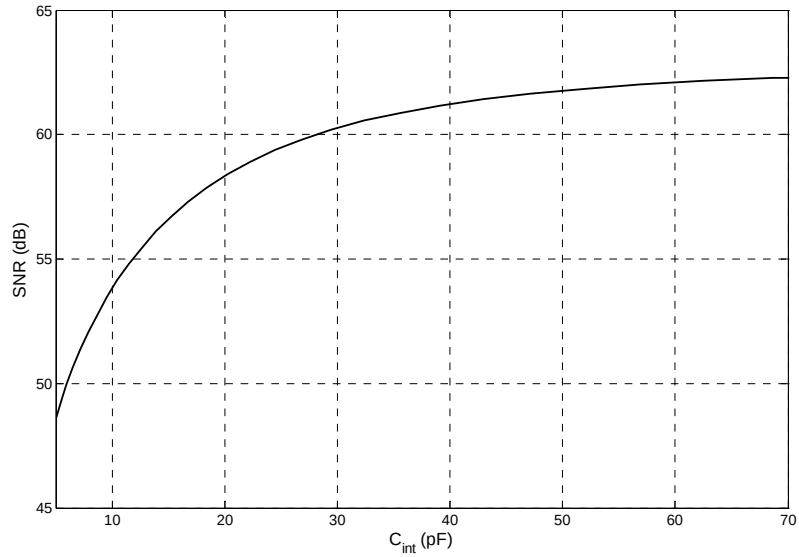


Figure 5.19: SNR of the ADC versus the capacitance of the integrator.

5.3.2.2.e Effect of thermal noise

The noise mentioned in the previous sections is due to quantization errors. The quantization noise is shaped by the ADC loop. However, the quantization noise can be dominated y the thermal noise which is not shaped by the loop because it is added at the input of the ADC. The effect of the thermal noise can be modeled by adding a white Gaussian noise source at the input of the integrator as shown in Figure 5.20.

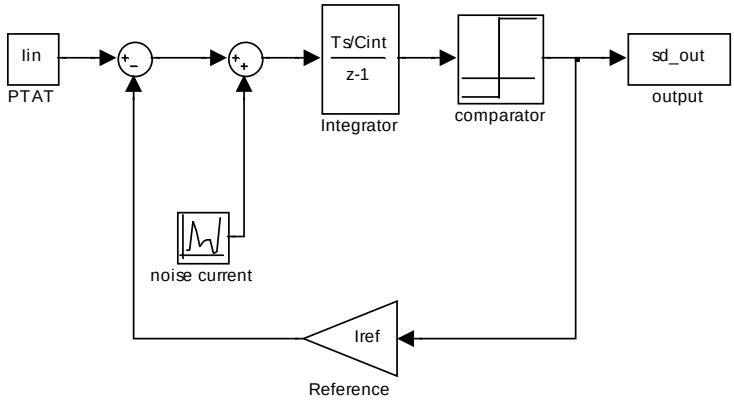


Figure 5.20: Simulink DT model of the sigma-delta ADC with thermal noise.

The value of the noise current is calculated from the circuit implementation of the ADC. The main thermal noise contributors are the transistors connected to the input node of the integrator. The mean square of the noise current which flows into the integrator is given by, [Razavi, 01]:

$$i_n^2 = 4\gamma \cdot k_B T g_{m,\text{int}} \tag{5.31}$$

where γ is a dimensionless process parameter equals 2/3 for long channels and 4/3 for short channel transistors, [Razavi, 01], k_B is the Boltzmann constant, T is the absolute temperature, $g_{m,int}$ is the effective transconductance of all transistors that introduce noise into the integrator. The mean square of the noise voltage at the integrator output is given by:

$$v_n^2 = \frac{R_{\text{int}}^2}{1+\omega^2 C_{\text{int}}^2 R_{\text{int}}^2} i_n^2 \tag{5.32}$$

The total integrated output noise voltage squared is given by:

$$V_n^2 = \frac{1}{2\pi}\int_0^\infty \frac{R_{\text{int}}^2}{1+\omega^2 C_{\text{int}}^2 R_{\text{int}}^2} i_n^2 \cdot d\omega \tag{5.33}$$

which finally gives:

$$V_n = \gamma \cdot g_{m,\text{int}} R_{\text{int}} \sqrt{\frac{k_B T}{C_{\text{int}}}} \tag{5.34}$$

The SNR due to thermal noise only is given by:

$$SNR_{th} = \left(\frac{\Delta V}{V_n}\right)^2 = \left(\frac{I_{ref} T_s}{\gamma \cdot g_{m,\text{int}} R_{\text{int}}}\right)^2 \frac{1}{k_B T C_{\text{int}}} \tag{5.35}$$

which indicates that the SNR is enhanced by decreasing the integrator capacitance C_{int}. This is because the signal power is inversely proportional to the square of the integrator capacitance C_{int}, while the noise power is inversely proportional to only the integrator capacitance C_{int}. This is a trade-off with the noise degradation due to the integrator leakage as was described before.

5.3.2.2.f Complete DT model of the ADC

The final discrete-time model of the sigma-delta ADC is obtained by combining all the effects described above as shown in Figure 5.21. The input to the ADC is a DC current added with a slow sine wave to account for the time variation of the input current.

The simulation results of the discrete-time model are shown in Figure 5.22. This curve is obtained by running the simulation for 2048 samples and averaging it 100 times.

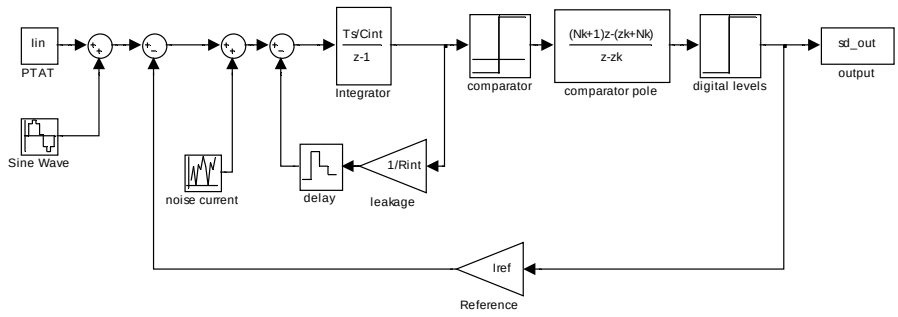


Figure 5.21: Complete DT Simulink model of the sigma-delta ADC.

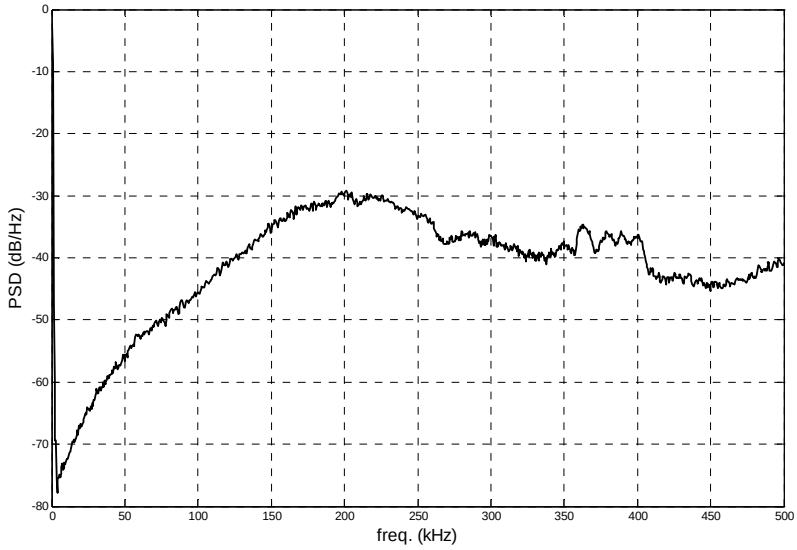


Figure 5.22: Noise shaping simulation.

5.3.3 Circuit Implementation

The implementation of the proposed sigma-delta modulator is straight forward. The PTAT current and reference current are subtracted as currents at node V_c. To implement this subtraction operation, one of the two currents direction needs to be inverted. The current inversion is done by using a simple NMOS current mirror as shown in Figure 5.23.

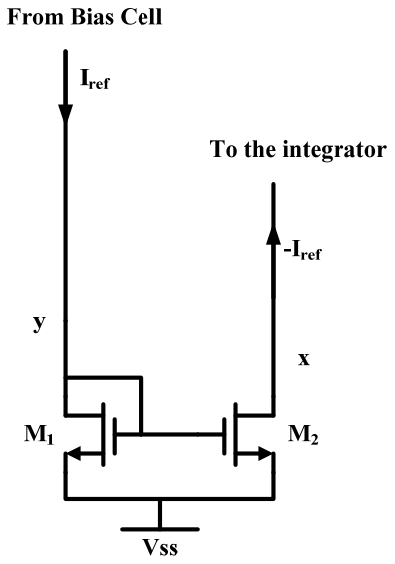


Figure 5.23: Simple current mirror.

The simple current mirror shown in Figure 5.23 is not accurate enough. Although transistors M1 and M2 are in saturation and have the same gate and source voltage, their drain currents are slightly different. This difference is due to the finite output resistance of the transistor, which implies different drain current for different drain voltage. The voltage of node 'y' is determined by the value of the reference current and the dimensions of M1. It was found by simulations that the voltage across the diode connected transistor M1 is about 0.3 V. As *Vss* = -0.6 V, the voltage of node 'y' is approximately -0.3 V. On the other hand, the node 'x' is connected to the input of the

comparator. The negative feedback nature of the system forces the voltage of the node 'x' to be around zero voltage. The 0.3 V discrepancy in the drain voltage between the two transistors M1 and M2 causes the absolute value of the mirrored current to be larger than the reference current. This difference introduces error and degrades the accuracy of the ADC. This mismatch in currents can be solved by using cascode current mirror as shown in Figure 5.24.

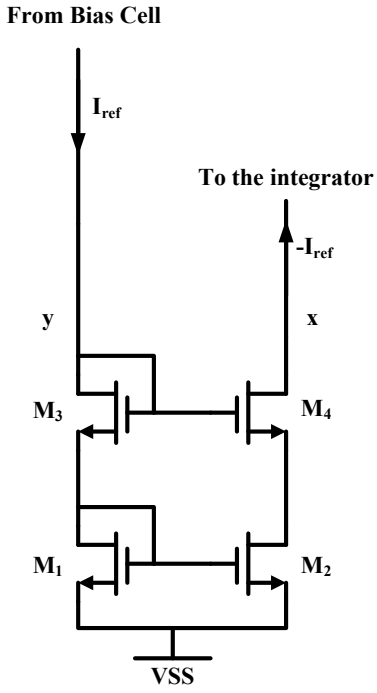


Figure 5.24: Cascode current mirror.

The cascode current mirror gives much better matching between the inverted current and the reference current due to two reasons: First the cascode current mirror has larger output resistance than the simple current mirror. While the output resistance of the simple current mirror is limited by the output resistance of the transistor M2, the output resistance of the cascode current mirror is given by:

$$R_{out} = r_{o4}\left(1 + g_{m4} r_{o2}\right) \tag{5.36}$$

where r_{o2}, r_{o4} are the output resistance of M_2 and M_4, respectively, g_{m4} is the transconductance of M_4. It can be deduced from equation (5.36) that the output resistance of the cascode current mirror is much higher than the simple one.

The second reason for the good matching between the inverted and the reference current is the matching in drain voltages between M_3 and M_4. As the voltage drop across one diode connected voltage is about 0.3 V, the voltage of the node 'y' is approximately zero which equal to the nominal value of the voltage of the node 'x'.

The complete circuit implementation of the sigma-delta ADC is shown in Figure 5.25. The comparator was implemented as a single stage OTA. The OTA is biased by mirroring the reference current using M_{10}. The sampler was implemented as a standard CMOS positive edge triggered D-FF. the reference current switch was implemented as a single NMOS transistor M_5. As the voltage of node 'x' has a limited range about the nominal value, the integrator capacitance need not be of high linearity. So the integrator is implemented as a simple NMOS capacitor.

5.3.4 Circuit Simulation Results

The implemented sigma-delta ADC is simulated in transistor level to ensures that the circuit level simulation results match the system level simulations results. The power spectral density of the ADC output is shown in Figure 5.26. It can be deduced from the figure that the circuit level simulation results is very near to system level simulation results. The circuit level results is not as smooth as system level because it is averaged only 4 times compared to 100 times in system level.

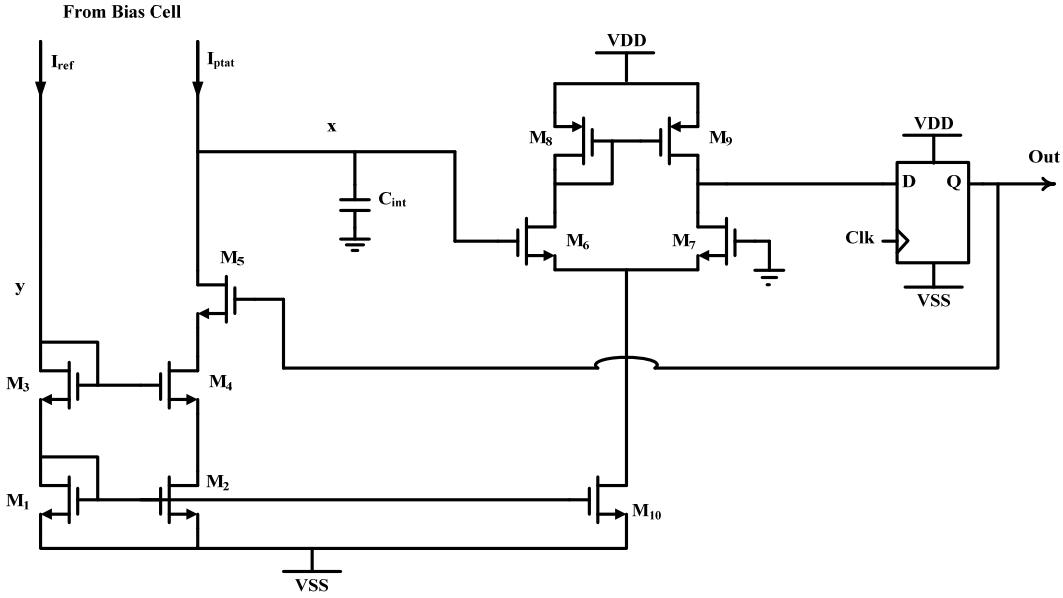


Figure 5.25: Circuit implementation of the sigma-delta ADC.

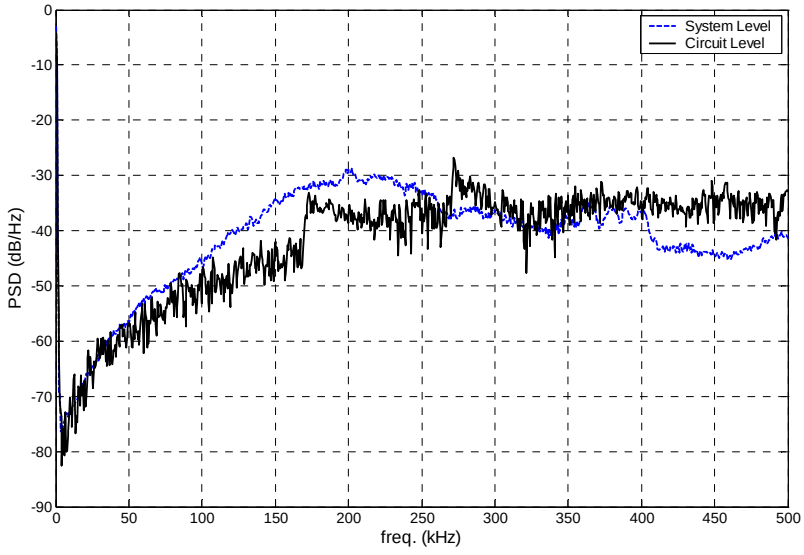


Figure 5.26: Transistor level simulation of the PSD of the ADC output.

5.4 System Simulation

In this section all blocks of the HF RFID temperature sensor are integrated and simulated in transistor level. The testbench of the system is shown in Figure 5.27, and the simulation results are shown in Figure 5.28. The signal received by the RFID tag is modeled by a sine wave source coupled to the input of the RFID tag with a transformer with a weak coupling coefficient, which is a reasonable model of the inductive link actually used.

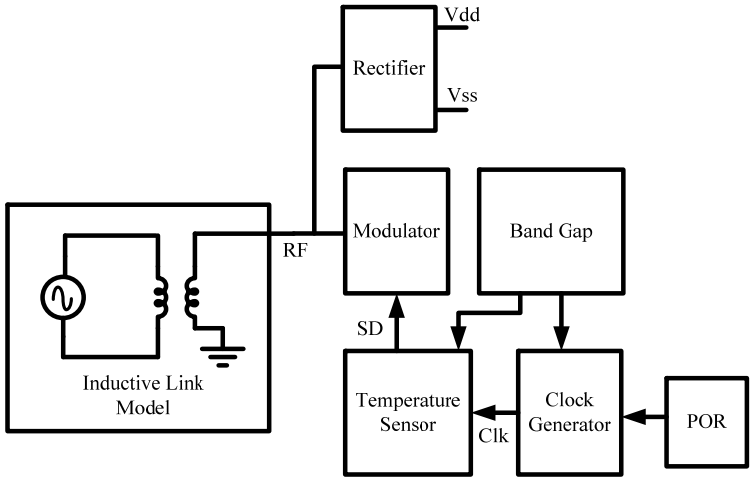


Figure 5.27: HF RFID tag testbench.

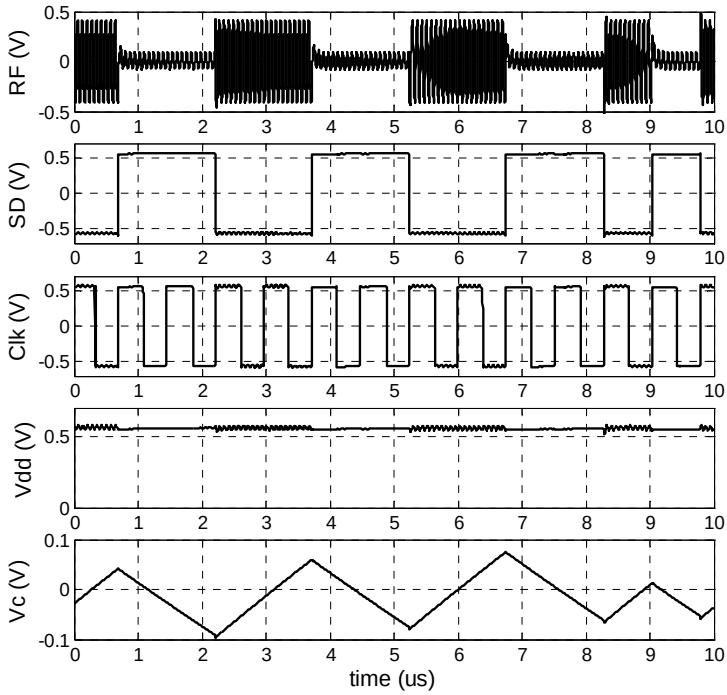


Figure 5.28: Transistor level simulation results of the HF RFID tag.

It can be deduced from the simulation results that the RFID tag responds to the received RF signal as expected. The DC voltage is generated, the internal clock is working, and the sigma-delta ADC is giving the expected output. The output of the RFID tag is sent by backscattering as can be noticed from the gaps in the RF signal.

5.5 Summary

An RFID temperature sensor chip was designed using 0.13 μm CMOS process. The chip has a supply voltage of 1.2 V. All the circuits are optimized for ultra low power operation. The area of the chip is 450 μm x 330 μm. The layout of the RFID tag chip is shown in Figure 5.29.

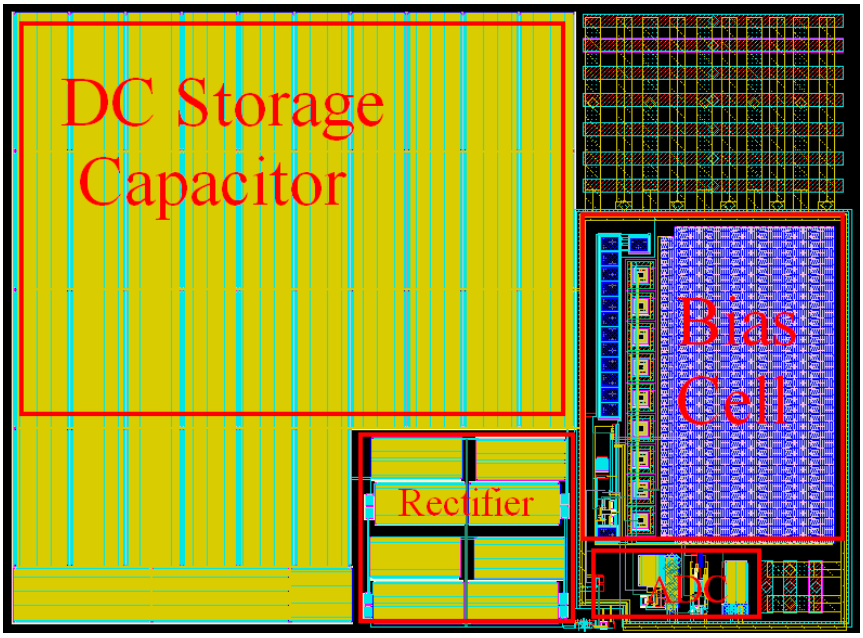


Figure 5.29: HF RFID Temperature Sensor chip layout.

A comparison between the achieved specifications and the similar work of some other authors is shown in Table 5-1.

Table 5-1: Performance comparison.

	Process	freq.	power	area	features	notes
This work	CMOS 0.13 µm	13.56 MHz	7 µW	0.45 mm x 0.33 mm	Temperature sensor	simulated
[Panit, 02]	CMOS 0.8 µm	13.56 MHz	170 µW	5.95 mm^2	64-Bit ID	measured
[Cantatore, 07]	Organic CMOS 0.15 µm	13.56 MHz	300 µW	45 mm^2	64-Bit ID	measured
[Cho, 05]	CMOS 0.25 µm, Schottky diodes	900 MHz	8 µW	0.5 mm x 0.6 mm	Temperature sensor	measured

The comparison shows that the designed chip achieves a competitive area and power consumption compared to the others work. It was difficult to find a detailed published work that has the same application (temperature sensor), and works at the same frequency (13.56 MHz), so the comparison was done to some published works that are reasonable similar to the designed chip.

Conclusions & Future Work

In this thesis, the concept of RFID (Radio Frequency Identification) is discussed. The main features of the RFID is presented and compared to the other identification system.

The thesis demonstrated the design of a UHF (Ultra High Frequency) RFID tag. The RFID tag system is designed to achieve the maximum possible communication range. It was shown that the selection of the operating frequency, the communication protocol, and the modulation scheme have to be chosen carefully according to the application to get the optimum operation.

As the rectifier is the main block in the RFID tag, a significant part of the work was directed towards improving its efficiency. A new simple and relatively accurate model for the rectifier circuit was introduced and verified by simulations.

The UHF RFID tag was then designed on circuit level. The design was simulated in 0.13 μm standard CMOS technology. All system blocks were designed to achieve the required specifications with minimum power consumption. The designed chip consumes only 1 μW and the conversion efficiency is 32%. The area of the chip is only 0.14 mm x 0.23 mm including pads. A summary of the work was introduced and compared to the similar work of other authors.

The designed UHF RFID tag has an ultra low power consumption, ultra small size and low cost. These features make it very suitable for several RFID applications such as product identification, toll collection, and telemetry sensors.

Then, the thesis demonstrated the design of an inductively coupled HF (High Frequency) RFID temperature sensor. The temperature sensing technique was based on the process parameters dependence on temperature. The sensed temperature is converted to digital form using a single bit sigma-delta ADC (Analog to Digital Converter). A complete analysis of the designed sigma-delta ADC was presented. The thermal noise of the system was also analyzed and optimized.

The RFID temperature sensor tag was then designed on circuit level. The design was simulated in 0.13 μm CMOS technology. All system block were designed to achieve the required specifications with minimum power consumption.

The designed RFID temperature sensor works at HF (High Frequency) which is suitable for medical applications. The design can be easily modified to measure the pressure using a MEMS component.

Other future work can be done based on this work. This future work can be summarized in the following points:

1. Silicon verification of the two designs.
2. The design and implementation of the RFID antenna for the UHF RFID tag.
3. The design and implementation of the inductive RFID tag.
4. Integrating the RFID tag chip with the antenna.
5. Verifying the practical operation of the two RFID tags.

References

[AIM, 01] Radio Frequency Identification RFID, A Basic Primer AIM International WP-98/002R; pp. 1-15; Jul. 7, 1999.

[Ashry, 07] Ahmed Ashry, Khaled Sharaf, Magdi Ibrahim, "Ultra Low Power UHF RFID Tag in 0.13µm CMOS", ICM 2007.

[Ashry, 07a] Ahmed Ashry, Khaled Sharaf, Magdi Ibrahim, "A Simple and Accurate Model for RFID Rectifier", Accepted in ICECS 2007.

[Cantatore, 07] Eugenio Cantatore, Thomas C. T. Geuns, Gerwin H. Gelinck, Erik van Veenendaal, "A 13.56-MHz RFID System Based on Organic Transponders", IEEE Journal of Solid-State Circuits, vol. 42, no. 1, pp. 84- 92, Jan. 2007.

[Cho, 05] N. Cho, S.-J. Song, J. Lee, S. Kim, S. Kim, and H.-J. Yoo, "A 8-µW, 0.3-mm^2 RF-Powered Transponder with Temperature Sensor for Wireless Environmental Monitoring", IEEE International Symposium on Circuits and Systems (ISCAS 2005)

[Curty, 05] Curty, J.-P., et al., "Remotely powered addressable UHF RFID integrated system", IEEE J. Solid-State Circuits, Vol. 40, No. 11, 2193-2202, 2005.

[Curty, 05a] J. P. Curty, N. Joehl, "A model for µ-power rectifier analysis and design", IEEE Transactions on circuits and systems, Vol. 52, no. 12, pp. 2771-2779, December 2005.

[EPC, 05] EPC™ Radio-Frequency Identity Protocols - Class-1 Generation-2 UHF RFID Protocol for communications at 860 MHz - 960 MHz -Version 1.0.

[Eunni, 06] Madhuri Bharadwaj Eunni, "A Novel Planar Microstrip Antenna Design for UHF RFID", Master Thesis, University of Kansas, 2006.

[Finken, 03] K. Finkenzeller, RFID Handbook, 2nd ed., John Wiley & Sons, 2003.

[Hard, 06] Hardgrave, B. and Miller, R. "The Myths and Realities of RFID", International Journal of Global Logistics and Supply Chain Management.

[Harmon, 03] Craig K. Harmon, "Basics of RFID Technology", RFID Journal, 2003.

[Huang, 98] Q. Huang and M. Oberle, "A 0.5-mW passive telemetry IC for biomedical applications", IEEE J. Solid-State Circuits, Vol. 33, No. 7, pp. 937-946, July 1998.

[Karthaus, 03] U. Karthaus and M. Fischer, "Fully integrated passive UHF RFID transponder IC with 16.7uW minimum RF input power", IEEE J. Solid-State Circuits, vol. 38, pp. 1602-1608, Oct. 2003.

[Kocer, 06] F. Kocer and M. P. Flynn, "A New Transponder Architecture with On-Chip ADC for Long-Range Telemetry Applications", IEEE Journal of Solid-State Circuits, Vol. 41, No. 5, pp. 557-564, May 2006.

[Landt, 06] J. Landt "Shrouds of Time, The history of RFID", White paper, An Aim Publication, 2001, www.aimglobal.org.

[Lewis, 04] S. Lewis, "A basic introduction to RFID technology and its use in the supply chain", Laran RFID, White paper, 2004.

[Panit, 02] Napong Panitantum, Aperadee Yordthein, Watcharakon Noothong, Apisak Worapishet and Manop Thamsirianunt, "A CMOS RFID transponder", The 2002 International Symposium on Communications and Information Technology (ISCIT) 2002

[Pertijs, 05] M. A. P. Pertijs, "A CMOS Smart Temperature Sensor With a 3σ Inaccuracy of 0.5°C From 50°C to 120°C", IEEE Journal of Solid-State Circuits, Vol. 40, No. 2, February 2005, pp. 454-461.

[Rabaey, 03] J. M. Rabaey, A. Chandrakasan, B. Nikolic, Digital Integrated Circuits: A Design Perspective (2nd ed.), Prentice-Hall, 2003.

[Razavi, 01] B. Razavi**,** Design of Analog CMOS Integrated Circuits, McGraw-Hill, 2001.

[Sarma, 03] S. Sarma, and D. W. Engels, "On the future of RFID tags and protocols", White paper, Auto-ID Center, Massachusetts Institute of Technology, 2003.

[Shoaei, 94] O. Shoaei and M. Snelgrove, “Optimal (Bandpass) Continuous-Time Sigma - Delta Mod-ulator”, Proc. ISCAS 94, London, Eng., v. 5 pp. 489-492 May 30-June 2 1994

[Sweeney, 05] Patrick J. Sweeney II, RFID for Dummies, Wiley, 2005.

[Umeda, 06] T. Umeda, H. Yoshida, S. Sekine, Y. Fujita, T. Suzuki, and S. Otaka, "A 950 MHz Rectifier Circuit for Sensor Network Tags with 10-m Distance", IEEE Journal of Solid-State Circuits, vol. 41, no. 1, pp. 35- 41, Jan. 2006.

[Usami, 04] M. Usami, "An ultra small RFID chip: μ-chip", IEEE Radio Frequency integrated circuits symposium, pp. 241-244, 2003.

[Wikipedia] http://en.wikipedia.org

[Yi, 07] J. Yi, W.H. Ki and C.Y. Tsui, "Analysis and design strategy of UHF micro-power CMOS rectifiers for micro-sensor and RFID applications", IEEE Trans. on circuits and systems, Part I, Vol.54, No.1, pp.153-166, Jan. 2007.