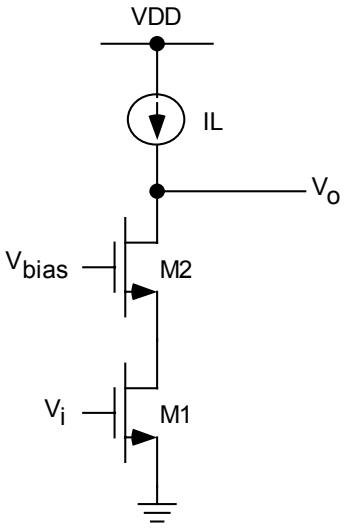
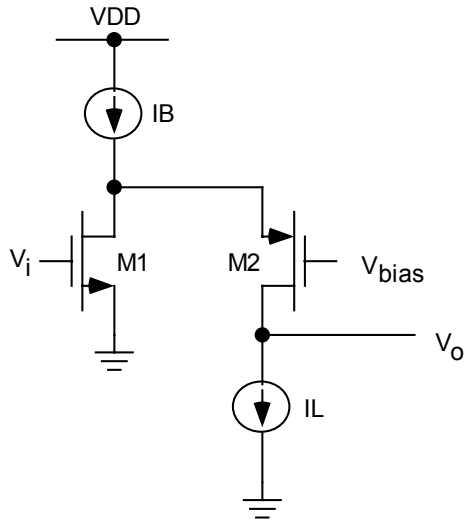
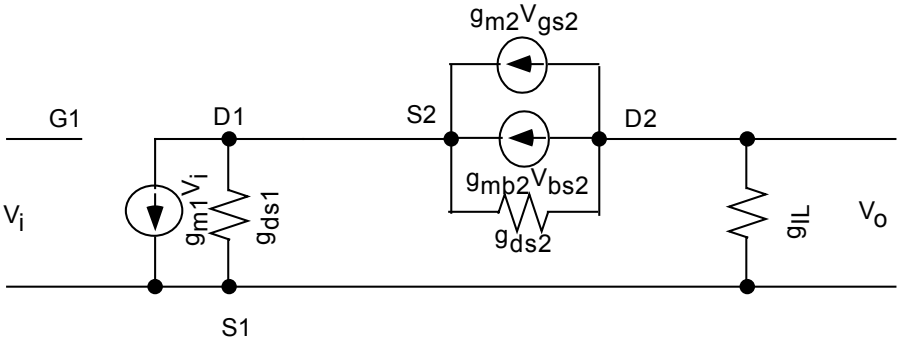
1.0 Folded-Cascode OTA



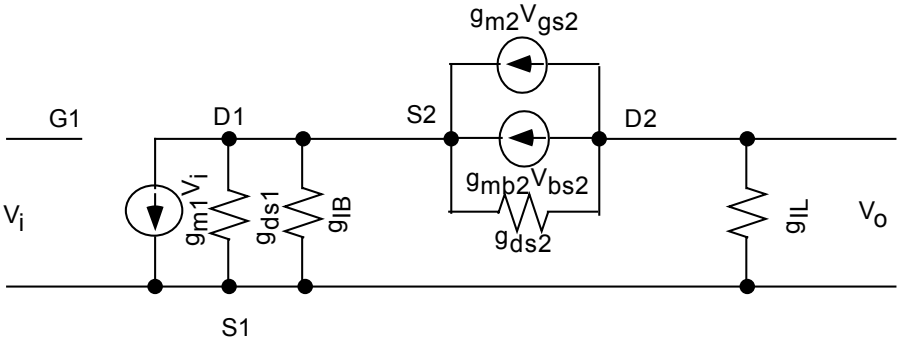
(a) Telescopic Cascode



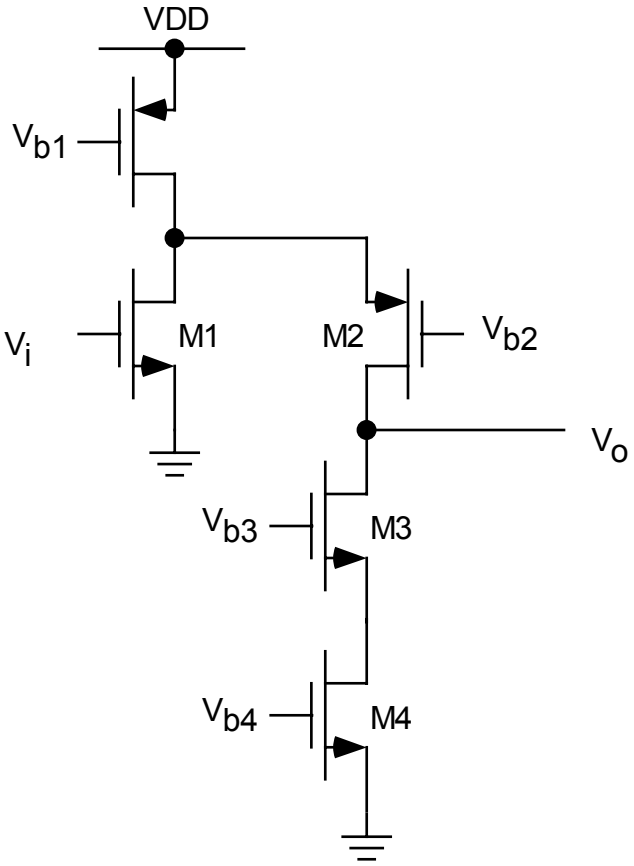
(b) Folded Cascode



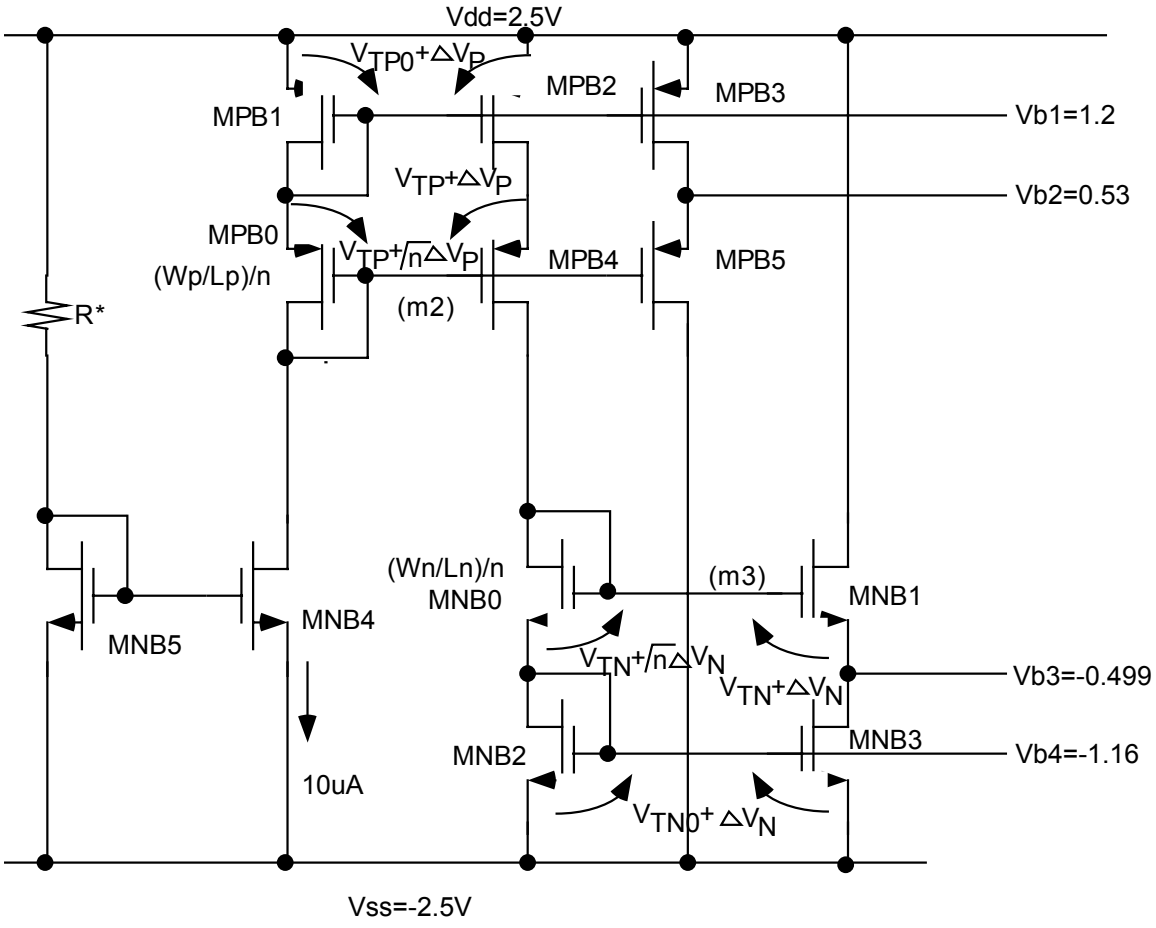
(c) Equivalent Circuit of Telescopic Cascode



(d) Equivalent Circuit of Folded Cascode



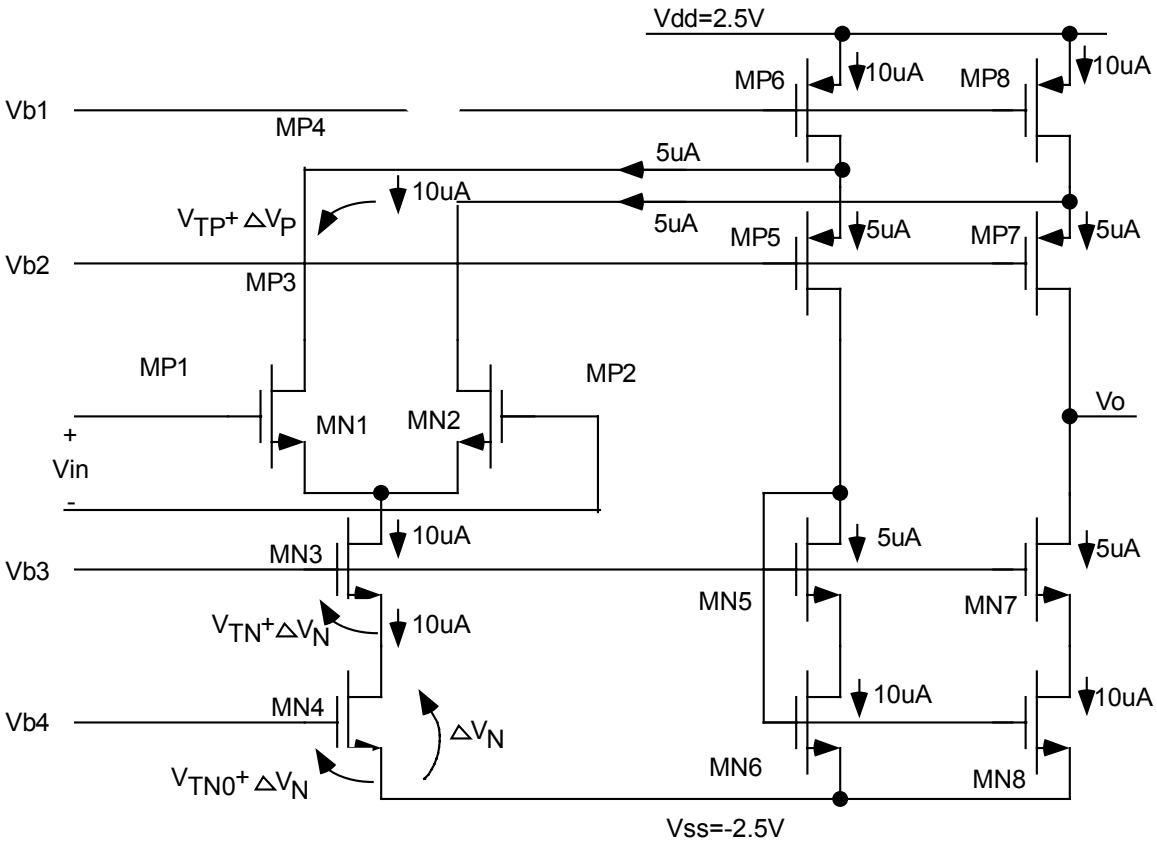
Folded Cascode With Cascode Load



R*=380k (external resistor, adjusted to achieve the desired bias voltages as shown)

(Wn/Ln)=(18L/6L)
(Wn/Ln)/7=(6L/14L)
(Wp/Lp)=(54L/6L)
(Wp/Lp)/7=(9L/7L)

Where the divisor n=7

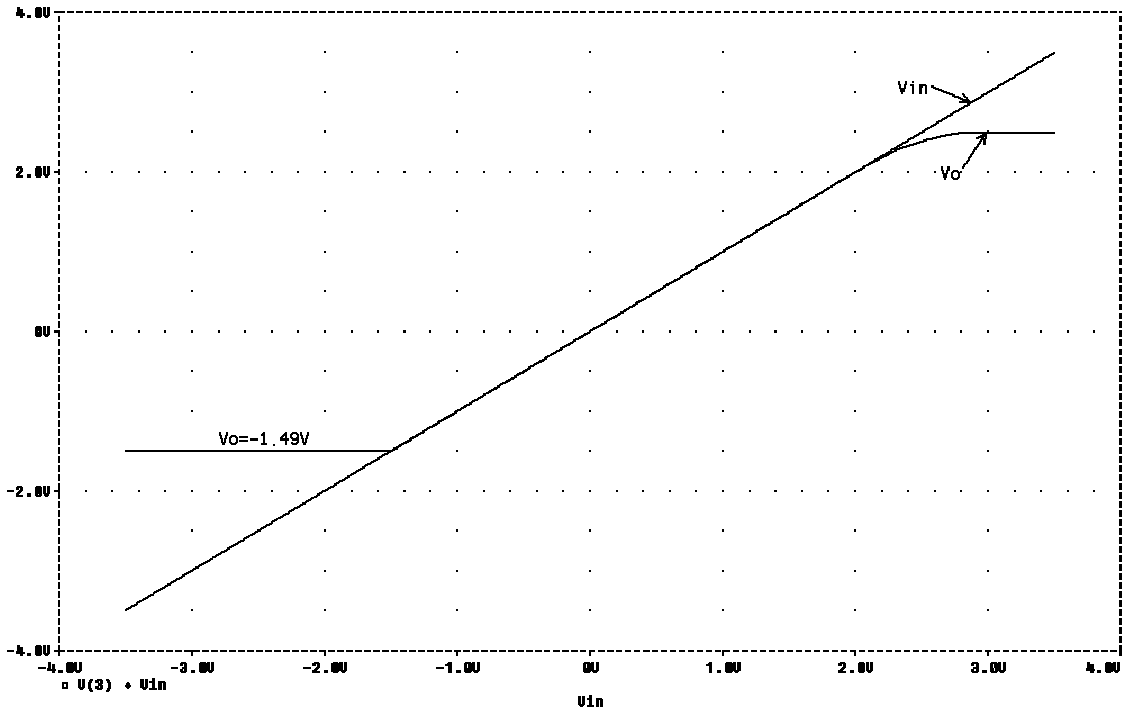


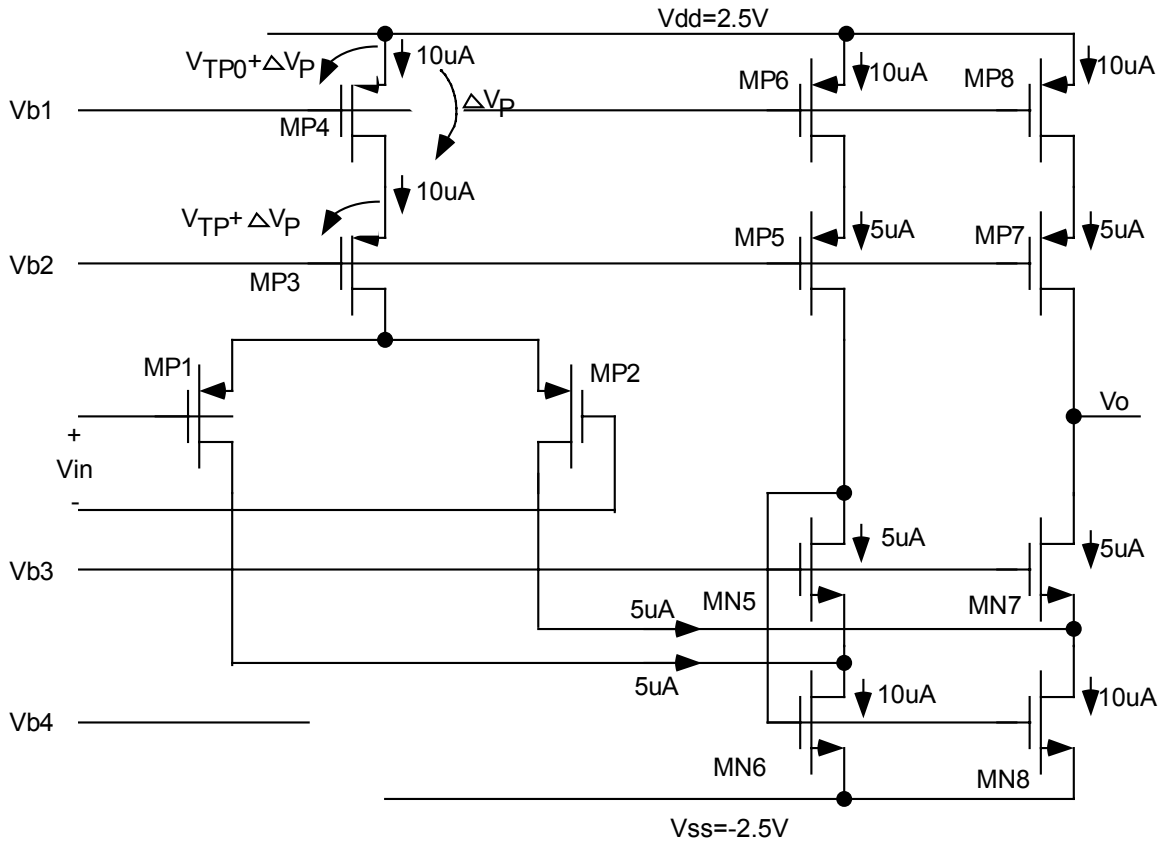
*NOTE: All transistors are 3 -terminal type (D,G,S) with
NMOS bulk (B) connected to VSS, and
PMOS bulk (B) connected to VDD

(Wn/Ln)=(18L/6L)
(Wp/Lp)=(54L/6L)

```
* Filename="wsotadc1.cir"
* Wide-swing OTA
* Simulation using subckt
* NMOS input stage => poor negative CMR
* OTA inputs
Vin 1 0 DC 0V

Xwsota 1 3 3 WSOTA

.SUBCKT WSOTA in+ in- out
* Power supplies
VDD vdd 0 DC 2.5V
VSS vss 0 DC -2.5V

* Wmin=Lmin=6 Lambda for linear analog circuit
.PARAM Wn=10.8U,  Ln=3.6U
.PARAM Wp=32.4U,  Lp=3.6U
.PARAM Wn7=3.6U,  Ln7=8.4U
.PARAM Wp7=5.4U,  Lp7=4.2U
.PARAM IB=10UA

* Biasing Circuit to generates vb1, vb2, vb3, vb4
MPB1 vb1 vb1 vdd vdd PMOS1 W={Wp}  L={Lp}
```

```
MPB2 m1  vb1 vdd vdd PMOS1 W={Wp}  L={Lp}
MPB3 vb2 vb1 vdd vdd PMOS1 W={Wp}  L={Lp}
MPB4 m3  m2  m1  vdd PMOS1 W={Wp}  L={Lp}
MPB5 vss m2  vb2 vb2 PMOS1 W={Wp}  L={Lp}
MPB0 m2  m2  vb1 vb1 PMOS1 W={Wp7} L={Lp7}
MNB0 m3  m3  vb4 vss NMOS1 W={Wn7} L={Ln7}
MNB1 vdd m3  vb3 vss NMOS1 W={Wn}  L={Ln}
MNB2 vb4 vb4 vss vss NMOS1 W={Wn}  L={Ln}
MNB3 vb3 vb4 vss vss NMOS1 W={Wn}  L={Ln}
ISS m2  vss {IB}

* Wide Swing OTA Implementation
MN1 n1  in+  n3  vss NMOS1 W={Wn}  L={Ln}
MN2 n2  in-  n3  vss NMOS1 W={Wn}  L={Ln}
MN3 n3  vb3  n7  vss NMOS1 W={Wn}  L={Ln}
MN4 n7  vb4  vss vss NMOS1 W={Wn}  L={Ln}
MN5 n4  vb3  n5  vss NMOS1 W={Wn}  L={Ln}
MN7 out vb3  n6  vss NMOS1 W={Wn}  L={Ln}
MN6 n5  n4   vss vss NMOS1 W={Wn}  L={Ln}
MN8 n6  n4   vss vss NMOS1 W={Wn}  L={Ln}
MP6 n1  vb1  vdd vdd PMOS1 W={Wp}  L={Lp}
MP8 n2  vb1  vdd vdd PMOS1 W={Wp}  L={Lp}
MP5 n4  vb2  n1  vdd PMOS1 W={Wp}  L={Lp}
MP7 out vb2  n2  vdd PMOS1 W={Wp}  L={Lp}
.ENDS

.MODEL NMOS1 NMOS VTO=1 KP=40U
+ GAMMA=1.0 LAMBDA=0.02 PHI=0.6
+ TOX=0.05U LD=0.5U CJ=5E-4 CJSW=10E-10
+ U0=550 MJ=0.5 MJSW=0.5 CGSO=0.4E-9 CGDO=0.4E-9
.MODEL PMOS1 PMOS VTO=-1 KP=15U
+ GAMMA=0.6 LAMBDA=0.02 PHI=0.6
+ TOX=0.05U LD=0.5U CJ=5E-4 CJSW=10E-10
+ U0=200 MJ=0.5 MJSW=0.5 CGSO=0.4E-9 CGDO=0.4E-9

* Analysis
.DC Vin -3.5V 3.5V .05V
.PROBE
.END
```


4.0V
2.0V
0V
-2.0V
-4.0V
-4.0V
-3.0V
-2.0V
-1.0V
0V
1.0V
2.0V
3.0V
4.0V
Vin
Vo
Vo=-1.49V
V(3)
Vin

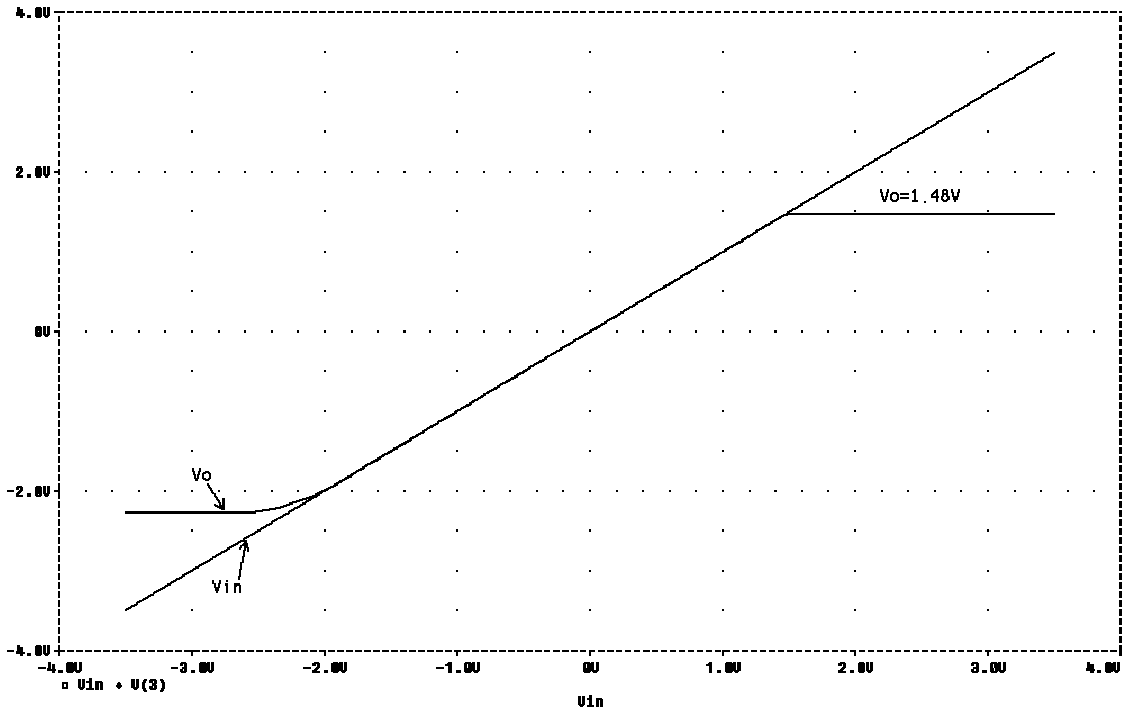


*NOTE: All transistors are 3 -terminal type (D,G,S) with
NMOS bulk (B) connected to VSS, and
PMOS bulk (B) connected to VDD

(Wn/Ln)=(18L/6L)
(Wp/Lp)=(54L/6L)

```
* Filename="wsotadc2.cir"
* Wide-swing OTA
 * Simulation using subckt
* PMOS input stage=>poor positive input CMR
* OTA inputs
Vin 1 0 DC 0V

Xwsota 1 3 3 WSOTA
*Xwsota 1 0 3 WSOTA
*VS 3 0 DC 0V

.SUBCKT WSOTA in+ in- out
* Power supplies
VDD vdd 0 DC 2.5V
VSS vss 0 DC -2.5V

* Wmin=Lmin=6 Lambda for linear analog circuit
.PARAM Wn=10.8U,  Ln=3.6U
.PARAM Wp=32.4U,  Lp=3.6U
.PARAM Wn7=3.6U,  Ln7=8.4U
.PARAM Wp7=5.4U,  Lp7=4.2U
.PARAM IB=10UA
```

```
* Biasing Circuit to generates vb1, vb2, vb3, vb4
MPB1 vb1 vb1 vdd vdd PMOS1 W={Wp}  L={Lp}
MPB2 m1  vb1 vdd vdd PMOS1 W={Wp}  L={Lp}
MPB3 vb2 vb1 vdd vdd PMOS1 W={Wp}  L={Lp}
MPB4 m3  m2  m1  vdd PMOS1 W={Wp}  L={Lp}
MPB5 vss m2  vb2 vb2 PMOS1 W={Wp}  L={Lp}
MPB0 m2  m2  vb1 vb1 PMOS1 W={Wp7} L={Lp7}
MNB0 m3  m3  vb4 vss NMOS1 W={Wn7} L={Ln7}
MNB1 vdd m3  vb3 vss NMOS1 W={Wn}  L={Ln}
MNB2 vb4 vb4 vss vss NMOS1 W={Wn}  L={Ln}
MNB3 vb3 vb4 vss vss NMOS1 W={Wn}  L={Ln}
ISS m2  vss {IB}

* Wide Swing OTA Implementation

MN5 n4  vb3  n5  vss NMOS1 W={Wn}  L={Ln}
MN7 out vb3  n6  vss NMOS1 W={Wn}  L={Ln}
MN6 n5  n4   vss vss NMOS1 W={Wn}  L={Ln}
MN8 n6  n4   vss vss NMOS1 W={Wn}  L={Ln}
MP6 n1  vb1  vdd vdd PMOS1 W={Wp}  L={Lp}
MP8 n2  vb1  vdd vdd PMOS1 W={Wp}  L={Lp}
MP5 n4  vb2  n1  vdd PMOS1 W={Wp}  L={Lp}
MP7 out vb2  n2  vdd PMOS1 W={Wp}  L={Lp}
MP1 n5  in+  n8  vdd PMOS1 W={Wp}  L={Lp}
MP2 n6  in-  n8  vdd PMOS1 W={Wp}  L={Lp}
MP4 n9  vb1  vdd vdd PMOS1 W={Wp}  L={Lp}
MP3 n8  vb2  n9  vdd PMOS1 W={Wp}  L={Lp}
.ENDS

.MODEL NMOS1 NMOS VTO=1 KP=40U
+ GAMMA=1.0 LAMBDA=0.02 PHI=0.6
+ TOX=0.05U LD=0.5U CJ=5E-4 CJSW=10E-10
+ U0=550 MJ=0.5 MJSW=0.5 CGSO=0.4E-9 CGDO=0.4E-9
.MODEL PMOS1 PMOS VTO=-1 KP=15U
+ GAMMA=0.6 LAMBDA=0.02 PHI=0.6
+ TOX=0.05U LD=0.5U CJ=5E-4 CJSW=10E-10
+ U0=200 MJ=0.5 MJSW=0.5 CGSO=0.4E-9 CGDO=0.4E-9

* Analysis
.DC Vin -3.5V 3.5V .05V
.PROBE
.END
```



2.0 Wide-Swing Folded-Cascode OTA

The problem with differential amplifier with nmos input pair is that the positive CMR extends beyond VDD, while the negative CMR is limited by the minimum voltage across the differential input. On the other hand the problem with differential amplifier with pmos input pair is that the positive CMR is limited by the minimum voltage across the differential input, while the negative CMR extend beyond VSS. Figure 2 shows a wide-swing differential amplifier which extends the input CMR beyond the power supply rails by combining both the nmos and pmos input pairs differential amplifiers. The circuit utilized folded-cascode load to increase the output impedance to approach ∞, the output impedance of ideal OTA. To increase the output impedance, (W/L)n=3 and (W/L)p=3*(W/L)n=9 are chosen. To reduce the effect of length modulation (2*DL)=1u, the minumum length L=6u is chosen. Figure 1 shows the biasing circuit which generates the four biasing voltages for the wide-swing folded-cascode OTA. This biasing circuit has been discuss earlier. In the ideal case of ignoring the bulk effects, the ratio needed to achieve the desired biasing voltages is ¼. But with the bulk effects included this ratio needs to be adjusted to guarantee that a [1]10uA current flows in MP3, MP4, MN3, MN4. Experimentation with the given circuit, the best ratio was found to be 1/7. The circuit was simulated to determine its specification:

A_V=93,560
R_o=1.095G
G_m= A_V/R_o=85.44u

This transconductance value of 85.44u was used in all the examples, so that the response of both the ideal OTA and actual OTA implementations can be compared. The wide-swing characteristic is simulated by applying input ranging from –3.5v to 3.5v with a power rails of –2.5v and 2.5v.The wide swing characteristic is important when designing filter circuit with high Q in cascaded filter implementation,

[1] Filename=wsota.doc

where the output of one stage is the input of the next stage. The high Q stage could easily drive the output voltage beyond the power rails.

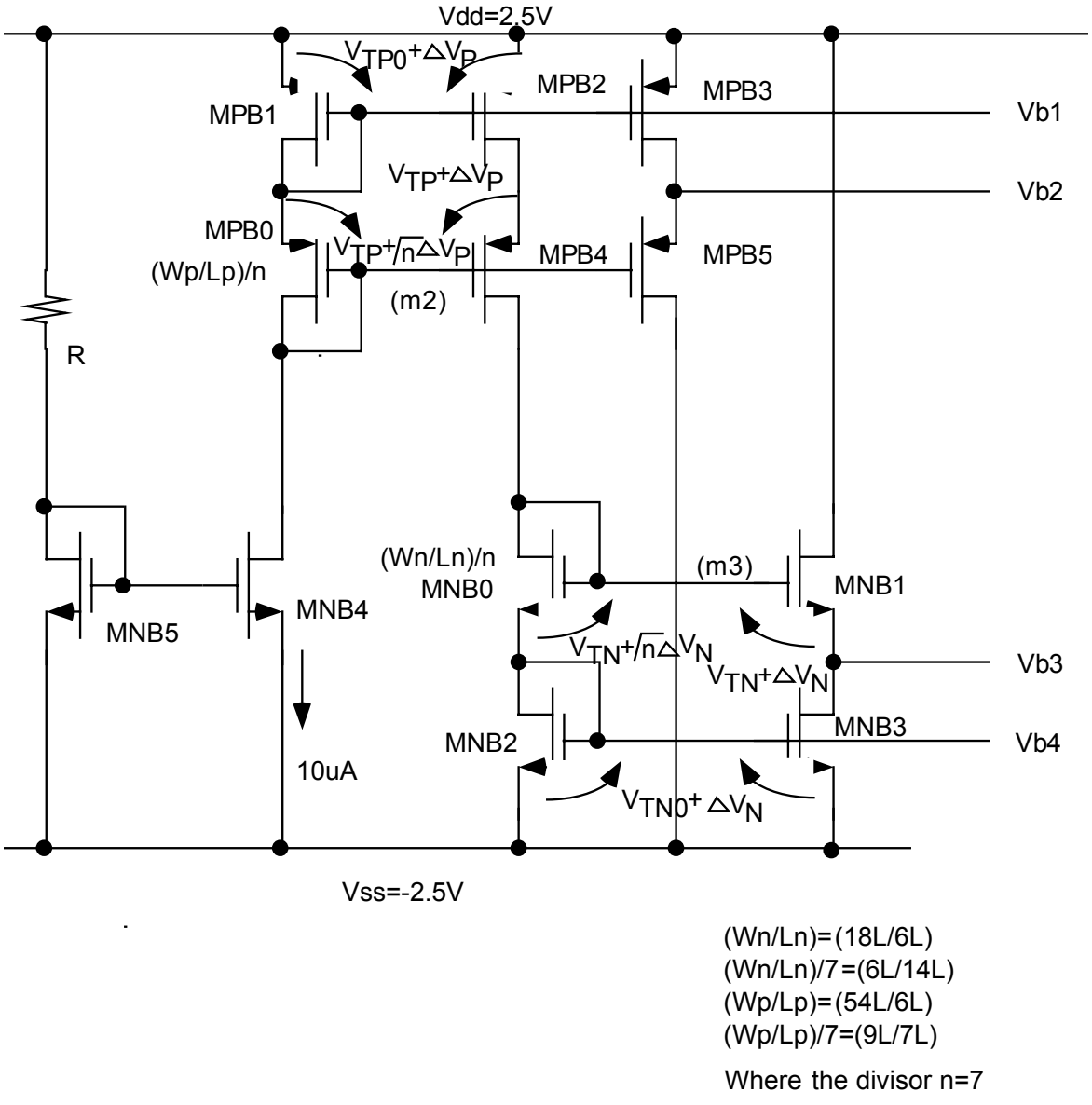


Figure 1. Biasing circuit for the wide-swing folded-cascode OTA.

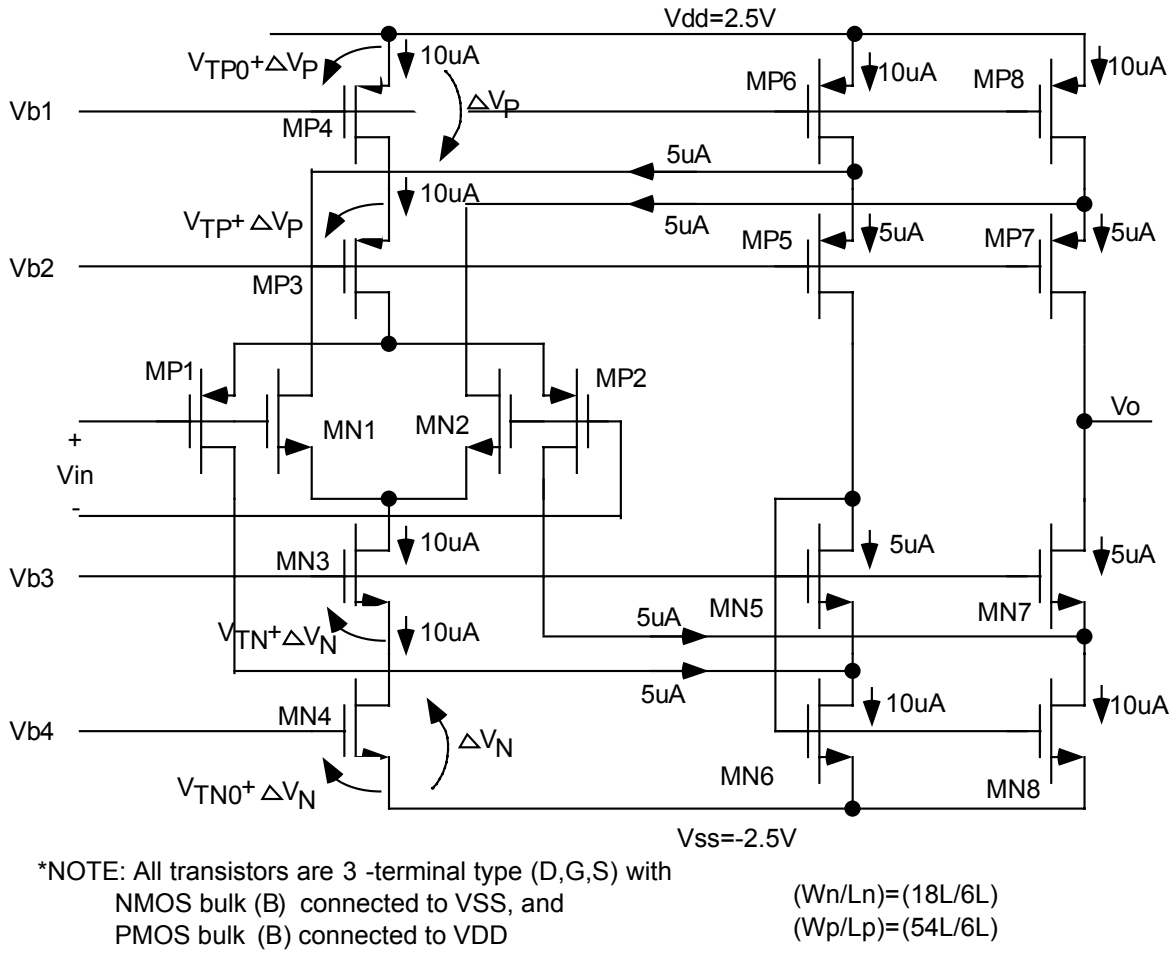


Figure 2. Wide-swing folded-cascode OTA

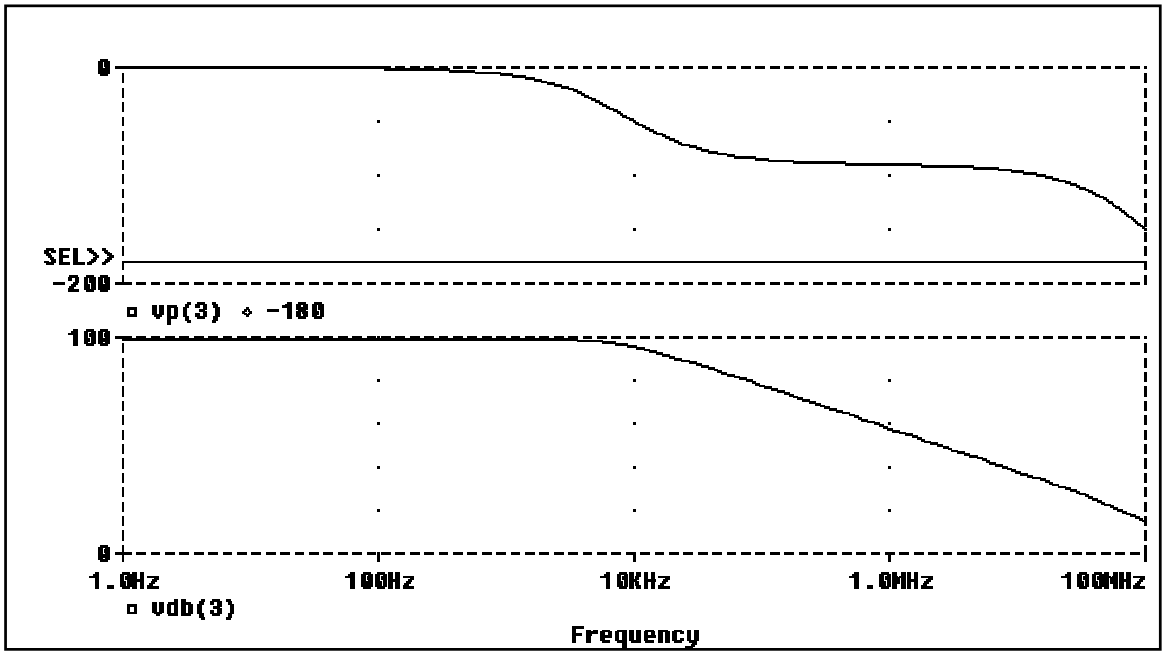
Wide Swing Single Ended OTA Circuit

Wide Swing OTA Netlist

```
* Filename ="wsotatf.cir"
* Wide-swing OTA
* Simulation showing all components
* Wmin=Lmin=6 Lambda for linear analog circuit
.PARAM Wn=10.8U,  Ln=3.6U
.PARAM Wp=32.4U,  Lp=3.6U
.PARAM Wn7=3.6U,  Ln7=8.4U
.PARAM Wp7=5.4U,  Lp7=4.2U

* Power supplies
VDD vdd 0 DC 2.5V
VSS vss 0 DC -2.5V
* OTA inputs
Vin in+ 0 DC 0V AC 1V
Vb  in- 0 DC 0V

* Biasing Circuit to generates vb1, vb2, vb3, vb4
MPB1 vb1 vb1 vdd vdd PMOS1 W={Wp}  L={Lp}
MPB2 m1  vb1 vdd vdd PMOS1 W={Wp}  L={Lp}
MPB3 vb2 vb1 vdd vdd PMOS1 W={Wp}  L={Lp}
MPB4 m3  m2  m1  vdd PMOS1 W={Wp}  L={Lp}
MPB5 vss m2  vb2 vdd PMOS1 W={Wp}  L={Lp}
MPB0 m2  m2  vb1 vdd PMOS1 W={Wp7} L={Lp7}
MNB0 m3  m3  vb4 vss NMOS1 W={Wn7} L={Ln7}
MNB1 vdd m3  vb3 vss NMOS1 W={Wn}  L={Ln}
MNB2 vb4 vb4 vss vss NMOS1 W={Wn}  L={Ln}
MNB3 vb3 vb4 vss vss NMOS1 W={Wn}  L={Ln}
ISS m2  vss 10uA

* Wide Swing OTA Implementation
MN1 n1  in+  n3  vss NMOS1 W={Wn}  L={Ln}
MN2 n2  in-  n3  vss NMOS1 W={Wn}  L={Ln}
MN5 n4  vb3  n5  vss NMOS1 W={Wn}  L={Ln}
MN7 3   vb3  n6  vss NMOS1 W={Wn}  L={Ln}
MN6 n5  n4   vss vss NMOS1 W={Wn}  L={Ln}
MN8 n6  n4   vss vss NMOS1 W={Wn}  L={Ln}
MN3 n3  vb3  n7  vss NMOS1 W={Wn}  L={Ln}
MN4 n7  vb4  vss vss NMOS1 W={Wn}  L={Ln}
MP6 n1  vb1  vdd vdd PMOS1 W={Wp}  L={Lp}
MP8 n2  vb1  vdd vdd PMOS1 W={Wp}  L={Lp}
MP5 n4  vb2  n1  vdd PMOS1 W={Wp}  L={Lp}
MP7 3   vb2  n2  vdd PMOS1 W={Wp}  L={Lp}
MP1 n5  in+  n8  vdd PMOS1 W={Wp}  L={Lp}
MP2 n6  in-  n8  vdd PMOS1 W={Wp}  L={Lp}
MP4 n9  vb1  vdd vdd PMOS1 W={Wp}  L={Lp}
MP3 n8  vb2  n9  vdd PMOS1 W={Wp}  L={Lp}

.MODEL NMOS1 NMOS VTO=1 KP=40U
+ GAMMA=1.0 LAMBDA=0.02 PHI=0.6
+ TOX=0.05U LD=0.5U CJ=5E-4 CJSW=10E-10
+ U0=550 MJ=0.5 MJSW=0.5 CGSO=0.4E-9 CGDO=0.4E-9
.MODEL PMOS1 PMOS VTO=-1 KP=15U
+ GAMMA=0.6 LAMBDA=0.02 PHI=0.6
+ TOX=0.05U LD=0.5U CJ=5E-4 CJSW=10E-10
+ U0=200 MJ=0.5 MJSW=0.5 CGSO=0.4E-9 CGDO=0.4E-9

* Analysis
.AC DEC 10 1Hz 100MegHz
.TF V(3) Vin
```

```
.PROBE
.OP
.END
```

OTA Frequency Response



Theoretical gain calculation of the OTA

At the operating point, the biasing currents are shown in Figure 12.

$$\lambda = \lambda_N = \lambda_P = 0.02$$

$$r_{DS}(P7) = r_{DS}(N7) = \frac{1}{\lambda I_{DSQ7}} = \frac{1}{(0.02)(5E-6)} = 10E6$$

$$r_{DS}(P8) = r_{DS}(N8) = \frac{1}{\lambda I_{DSQ8}} = \frac{1}{(0.02)(10E-6)} = 5E6$$

$$g_m(N1) = g_m(N7) = \sqrt{2\beta_N I_{DSQ}} = \sqrt{2K_N(W_n/L_n)I_{DSQ}} = \sqrt{2(40E-6)(10.6/(3.6-1))(5E-6)} = 40.38E-6$$

$$g_m(P1) = g_m(P7) = \sqrt{2\beta_P I_{DSQ}} = \sqrt{2K_P(W_p/L_p)I_{DSQ}} = \sqrt{2(15E-6)(32.4/(3.6-1))(5E-6)} = 43.23E-6$$

$$R_{ON} = g_m(N7)r_{DS}(N7)r_{DS}(N8) = (37.947E-6)(10E6)(5E6) = 1.8935E9$$

$$R_{OP} = g_m(P7)r_{DS}(P7)r_{DS}(P8) = (40.249E-6)(10E6)(5E6) = 2.01245E9$$

$$R_O = R_{ON}//R_{OP} = \frac{R_{ON}R_{OP}}{R_{ON}+R_{OP}} = \frac{(1.8935E9)(2.01245E9)}{(1.8935E9)+(2.01245E9)} = 1.19E9$$

$$g_m = g_m(N1) + g_m(P1) = (40.38E-6) + (43.23E-6) = 83.61E-6$$

$$A_V = -g_m R_O = -(83.61E-6)(1.19E9) == 9.9E4$$

The OTA is simulated, the results shown below are very closed to the calculated one.

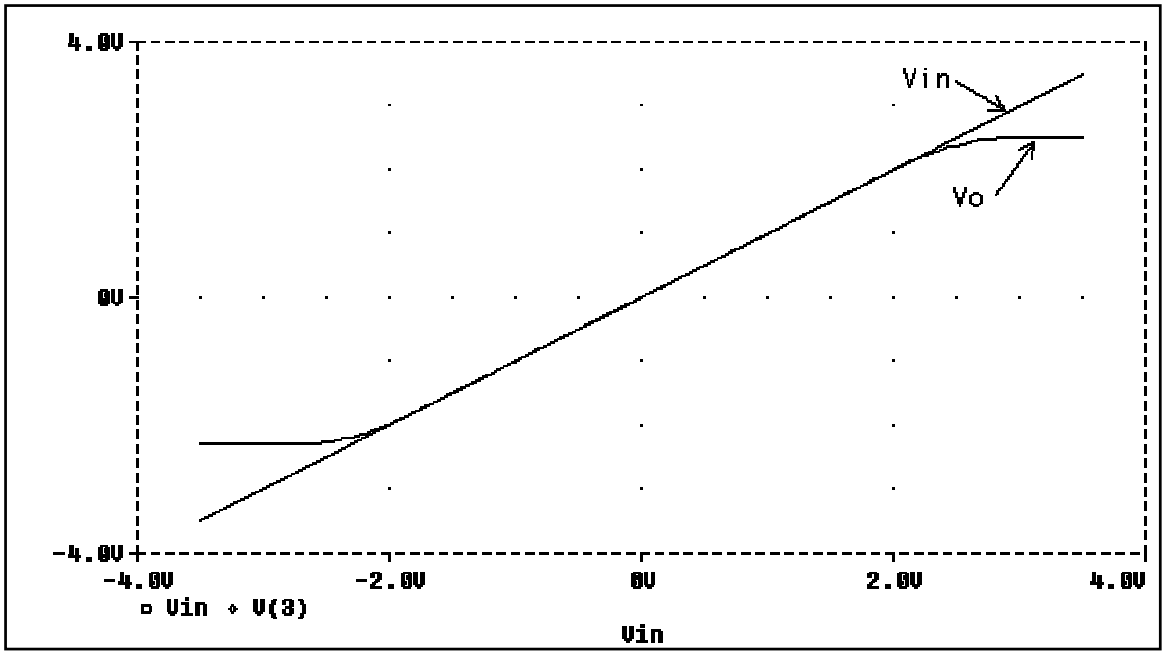
```
****     SMALL-SIGNAL CHARACTERISTICS

      V(3)/Vin =  9.356E+04

      INPUT RESISTANCE AT Vin =  1.000E+20

      OUTPUT RESISTANCE AT V(3) =  1.095E+09
```

$$g_m = \frac{A_V}{R_O} = \frac{9.356E4}{1.095E9} = 85.44\mu$$

OTA Transfer Characteristic

```
* Filename="wsotadc.cir"
* Wide-swing OTA
* Simulation using subckt

* OTA inputs
Vin 1 0 DC 0V

Xwsota 1 3 3 WSOTA

.SUBCKT WSOTA in+ in- out
* Power supplies
VDD vdd 0 DC 2.5V
VSS vss 0 DC -2.5V

* Wmin=Lmin=6 Lambda for linear analog circuit
.PARAM Wn=10.8U,  Ln=3.6U
.PARAM Wp=32.4U,  Lp=3.6U
.PARAM Wn7=3.6U,  Ln7=8.4U
.PARAM Wp7=5.4U,  Lp7=4.2U
.PARAM IB=10UA

* Biasing Circuit to generates vb1, vb2, vb3, vb4
MPB1 vb1 vb1 vdd vdd PMOS1 W={Wp}  L={Lp}
MPB2 m1  vb1 vdd vdd PMOS1 W={Wp}  L={Lp}
MPB3 vb2 vb1 vdd vdd PMOS1 W={Wp}  L={Lp}
MPB4 m3  m2  m1  vdd PMOS1 W={Wp}  L={Lp}
MPB5 vss m2  vb2 vb2 PMOS1 W={Wp}  L={Lp}
MPB0 m2  m2  vb1 vb1 PMOS1 W={Wp7} L={Lp7}
MNB0 m3  m3  vb4 vss NMOS1 W={Wn7} L={Ln7}
MNB1 vdd m3  vb3 vss NMOS1 W={Wn}  L={Ln}
MNB2 vb4 vb4 vss vss NMOS1 W={Wn}  L={Ln}
MNB3 vb3 vb4 vss vss NMOS1 W={Wn}  L={Ln}
ISS m2  vss {IB}

* Wide Swing OTA Implementation
MN1 n1  in+  n3  vss NMOS1 W={Wn}  L={Ln}
MN2 n2  in-  n3  vss NMOS1 W={Wn}  L={Ln}
MN5 n4  vb3  n5  vss NMOS1 W={Wn}  L={Ln}
MN7 out vb3  n6  vss NMOS1 W={Wn}  L={Ln}
MN6 n5  n4   vss vss NMOS1 W={Wn}  L={Ln}
MN8 n6  n4   vss vss NMOS1 W={Wn}  L={Ln}
MN3 n3  vb3  n7  vss NMOS1 W={Wn}  L={Ln}
MN4 n7  vb4  vss vss NMOS1 W={Wn}  L={Ln}
MP6 n1  vb1  vdd vdd PMOS1 W={Wp}  L={Lp}
MP8 n2  vb1  vdd vdd PMOS1 W={Wp}  L={Lp}
MP5 n4  vb2  n1  vdd PMOS1 W={Wp}  L={Lp}
MP7 out vb2  n2  vdd PMOS1 W={Wp}  L={Lp}
MP1 n5  in+  n8  vdd PMOS1 W={Wp}  L={Lp}
```

```
MP2 n6  in-  n8  vdd PMOS1 W={Wp}  L={Lp}
MP4 n9  vb1  vdd vdd PMOS1 W={Wp}  L={Lp}
MP3 n8  vb2  n9  vdd PMOS1 W={Wp}  L={Lp}
.ENDS

.MODEL NMOS1 NMOS VTO=1 KP=40U
+ GAMMA=1.0 LAMBDA=0.02 PHI=0.6
+ TOX=0.05U LD=0.5U CJ=5E-4 CJSW=10E-10
+ U0=550 MJ=0.5 MJSW=0.5 CGSO=0.4E-9 CGDO=0.4E-9
.MODEL PMOS1 PMOS VTO=-1 KP=15U
+ GAMMA=0.6 LAMBDA=0.02 PHI=0.6
+ TOX=0.05U LD=0.5U CJ=5E-4 CJSW=10E-10
+ U0=200 MJ=0.5 MJSW=0.5 CGSO=0.4E-9 CGDO=0.4E-9

* Analysis
.DC Vin -3.5V 3.5V .05V
.PROBE
.END
```



Biasing The OTA Circuit

The goal of the biasing circuit shown in Figure 11 is to generate the biasing voltages needed by the OTA circuit shown in Figure 12 so that the gate to source voltages of the four transistors MN3, MN4, MP3, MP4 are as shown.to generate the same current. That is,

$$I_D(N3) = I_D(N4) = -I_D(P3) = -I_D(P4)$$

$$V_{TN} + \Delta V_N = V_{TN0} + \Delta V_N = -(V_{TP} + \Delta V_P) = -(V_{TP0} + \Delta V_P)$$

$$\Delta V_N = -\Delta V_P \text{ ; since } V_{TN0} = -V_{TP0}$$

Transistor MN3 and MP3 both have non-zero bulk to source voltage. Hence their threshold voltages increase. These values are computed as follows:

$$V_{BS}(N3) = V_B(N3) - V_S(N3) = V_{SS} - (V_{SS} + \Delta V_N) = -\Delta V_N$$
$$V_{TN} = V_{TN0} + \gamma(\sqrt{\phi - V_{BS}} - \sqrt{\phi}) = V_{TN0} + \gamma(\sqrt{\phi + \Delta V_N} - \sqrt{\phi}) = 1 + 1(\sqrt{0.6 + 0.34} - \sqrt{0.6}) = 1.195$$
$$V_{BS}(P3) = V_B(P3) - V_S(P3) = V_{DD} - (V_{DD} + \Delta V_P) = -\Delta V_P$$
$$V_{TP} = V_{TP0} - \gamma(\sqrt{\phi + V_{BS}} - \sqrt{\phi}) = V_{TP0} + \gamma(\sqrt{\phi - \Delta V_P} - \sqrt{\phi}) = -1 - 1(\sqrt{0.6 + 0.34} - \sqrt{0.6}) = -1.19$$

The value of the biasing voltage can now be calculated from the OTA circuit.

$$V_{b4} = V_{TN0} + \Delta V_N + V_{SS} = 1 + 0.34 + (-2.5) = -1.16$$
$$V_{b3} = V_{TN} + \Delta V_N + \Delta V_N + V_{SS} = 1.195 + 2(0.34) + (-2.5) = -0.625$$
$$V_{b2} = V_{DD} + \Delta V_P + V_{TP} + \Delta V_P = V_{DD} + V_{TP} + 2(\Delta V_P) = 2.5 - 1 + 2(-0.34) = 0.82$$
$$V_{b1} = V_{DD} + V_{TP0} + \Delta V_P = 2.5 - 1 - 0.34 = 1.16$$

The biasing circuit must determine the value of the divisor n to achieve the desired biasing voltages. V_{b4} and V_{b1} are satisfied by selecting the same transistor size as that of the OTA circuit. For V_{b3} and V_{b2}, the value of n must be determined to achieve the biasing voltages. The voltage on the biasing circuit side is determined and equated to the corresponding required OTA bias voltage. This is illustrated as follows:

$$V_{b3} = V_{SS} + V_{TN0} + \Delta V_N + V_{TN} + \sqrt{n}\Delta V_N - (V_{TN} + \Delta V_N) = V_{TN0} + \sqrt{n}\Delta V_N + V_{ss}$$

Equating with corresponing equation in the OTA side, one obtains

$$V_{TN0} + \sqrt{n}\Delta V_N + V_{SS} = V_{TN} + 2(\Delta V_N) + V_{SS}$$
$$(\sqrt{n} - 2)\Delta V_N = V_{TN} - V_{TN0}$$
$$n = \left(\frac{V_{TN} - V_{TN0}}{\Delta V_N} + 2\right)^2 = \left(\frac{1.195 - 1}{0.34} + 2\right)^2 = 6.62 \approx 7$$

Similarly, V_{b2} on both sides are equated to obtain n, this value should the same as that obtain for V_{b3}.

$$V_{b2} = V_{DD} + V_{TP0} + \Delta V_P + V_{TP} + \sqrt{n}\Delta V_P - (V_{TP} + \Delta V_P) = V_{DD} + V_{TP0} + \sqrt{n}\Delta V_P$$

Equating with corresponing equation in the OTA side, one obtains

$$V_{DD} + V_{TP0} + \sqrt{n}\Delta V_P = V_{DD} + V_{TP} + 2(\Delta V_P)$$
$$(\sqrt{n} - 2)\Delta V_P = V_{TP} - V_{TP0}$$
$$n = \left(\frac{V_{TP} - V_{TP0}}{\Delta V_P} + 2\right)^2 = \left(\frac{-1.195 - (-1)}{-0.34} + 2\right)^2 = 6.62 \approx 7$$

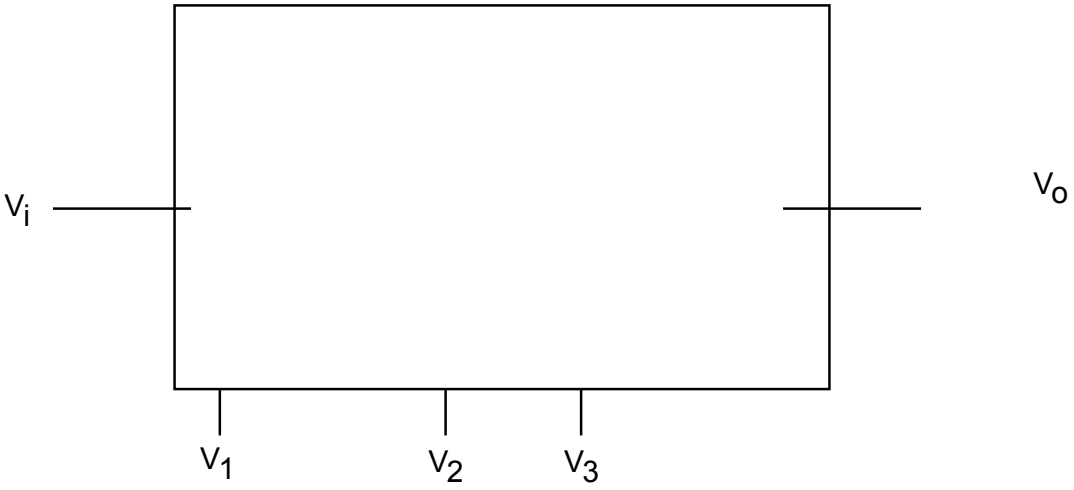
Figure 11 uses n=7 in the final implementation. The circuit using the subckt netlist of OTA in "wsotatf.cir" is simulated to show the internal node voltages. These voltages are shown below:

```
NODE    VOLTAGE      NODE    VOLTAGE      NODE    VOLTAGE      NODE    VOLTAGE
```

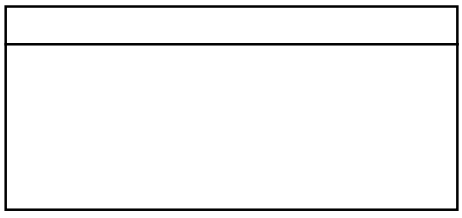
```
(    3)   -1.1560  (   m1)    1.4886  (   m2)   -1.0598  (   m3) 1.4454
(   n1)    2.0839  (   n2)    2.0839  (   n3)   -1.6585  (   n4) 1.1560
(   n5)   -2.1284  (   n6)   -2.1284  (   n7)   -2.1918  (   n8) 1.5124
(   n9)    2.1589  (  in+)    0.0000  (  in-)    0.0000  (  vb1) 1.1771
(  vb2)     .7197  (  vb3)    -.6744  (  vb4)   -1.1587  (  vdd) 2.5000
(  vss)   -2.5000
```

The desired and actual biasing voltages are compared in the following table:

Biasing Voltage	Desired Value	Actual Value with n=7
Vb1	1.16	1.1771
Vb2	0.82	.7197
Vb3	-0.625	-0.6744
Vb4	-1.16	-1.1587



(a)



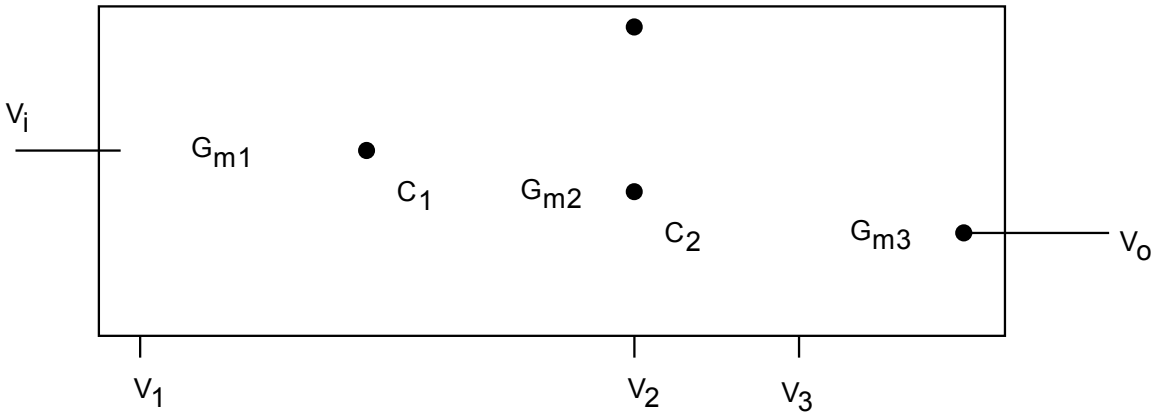
(b)

Actual 2 OTAs Circuit Implementation Netlist

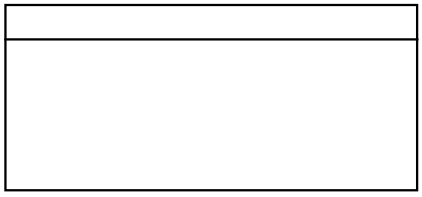
```
*Filename = "univ2_a2.cir"
*Biquad 2nd order filter. fo=100K
```

```
Vin 1 0 DC 0V AC 1V
*LP
*Xs2flt 1 0 0 2 S2FLT
*HP
*Xs2flt 0 0 1 2 S2FLT
*BP
*Xs2flt 0 1 0 2 S2FLT
*BR
Xs2flt 1 0 1 2 S2FLT


.SUBCKT S2FLT v1 v2 v3 v0
.PARAM C=135.98pF
.PARAM Q=1.61803
Xota1 v1 v0 n2 WSOTA
Xota2 n2 v0 v0 WSOTA

C1 n2 v2 {C/Q} IC=0V
C2 v0 v3 {Q*C} IC=0V
.ENDS

.SUBCKT WSOTA in+ in- out
* Power supplies
VDD vdd 0 DC 2.5V
VSS vss 0 DC -2.5V

* Wmin=Lmin=6 Lambda for linear analog circuit
.PARAM Wn=10.8U,  Ln=3.6U
.PARAM Wp=32.4U,  Lp=3.6U
.PARAM Wn7=3.6U,  Ln7=8.4U
.PARAM Wp7=5.4U,  Lp7=4.2U
.PARAM IB=10UA

* Biasing Circuit to generates vb1, vb2, vb3, vb4
MPB1 vb1 vb1 vdd vdd PMOS1 W={Wp}  L={Lp}
MPB2 m1  vb1 vdd vdd PMOS1 W={Wp}  L={Lp}
MPB3 vb2 vb1 vdd vdd PMOS1 W={Wp}  L={Lp}
MPB4 m3  m2  m1  vdd  PMOS1 W={Wp}  L={Lp}
MPB5 vss m2  vb2 vb2 PMOS1 W={Wp}  L={Lp}
MPB0 m2  m2  vb1 vb1 PMOS1 W={Wp7} L={Lp7}
MNB0 m3  m3  vb4 vss NMOS1 W={Wn7} L={Ln7}
MNB1 vdd m3  vb3 vss NMOS1 W={Wn}  L={Ln}
MNB2 vb4 vb4 vss vss NMOS1 W={Wn}  L={Ln}
MNB3 vb3 vb4 vss vss NMOS1 W={Wn}  L={Ln}
ISS m2  vss {IB}

* Wide Swing OTA Implementation
MN1 n1  in+  n3  vss NMOS1 W={Wn}  L={Ln}
MN2 n2  in-  n3  vss NMOS1 W={Wn}  L={Ln}
MN5 n4  vb3  n5  vss NMOS1 W={Wn}  L={Ln}
MN7 out vb3  n6  vss NMOS1 W={Wn}  L={Ln}
MN6 n5  n4   vss vss NMOS1 W={Wn}  L={Ln}
MN8 n6  n4   vss vss NMOS1 W={Wn}  L={Ln}
MN3 n3  vb3  n7  vss NMOS1 W={Wn}  L={Ln}
MN4 n7  vb4  vss vss NMOS1 W={Wn}  L={Ln}
MP6 n1  vb1  vdd vdd PMOS1 W={Wp}  L={Lp}
MP8 n2  vb1  vdd vdd PMOS1 W={Wp}  L={Lp}
MP5 n4  vb2  n1  vdd PMOS1 W={Wp}  L={Lp}
MP7 out vb2  n2  vdd PMOS1 W={Wp}  L={Lp}
MP1 n5  in+  n8  vdd PMOS1 W={Wp}  L={Lp}
MP2 n6  in-  n8  vdd PMOS1 W={Wp}  L={Lp}
MP4 n9  vb1  vdd vdd PMOS1 W={Wp}  L={Lp}
MP3 n8  vb2  n9  vdd PMOS1 W={Wp}  L={Lp}
```

```
.ENDS

.MODEL NMOS1 NMOS VTO=1 KP=40U
+ GAMMA=1.0 LAMBDA=0.02 PHI=0.6
+ TOX=0.05U LD=0.5U CJ=5E-4 CJSW=10E-10
+ U0=550 MJ=0.5 MJSW=0.5 CGSO=0.4E-9 CGDO=0.4E-9
.MODEL PMOS1 PMOS VTO=-1 KP=15U
+ GAMMA=0.6 LAMBDA=0.02 PHI=0.6
+ TOX=0.05U LD=0.5U CJ=5E-4 CJSW=10E-10
+ U0=200 MJ=0.5 MJSW=0.5 CGSO=0.4E-9 CGDO=0.4E-9

* Analysis
.AC DEC 100 1Hz 100MegHz
.PROBE
.END
```



(a)



(b)

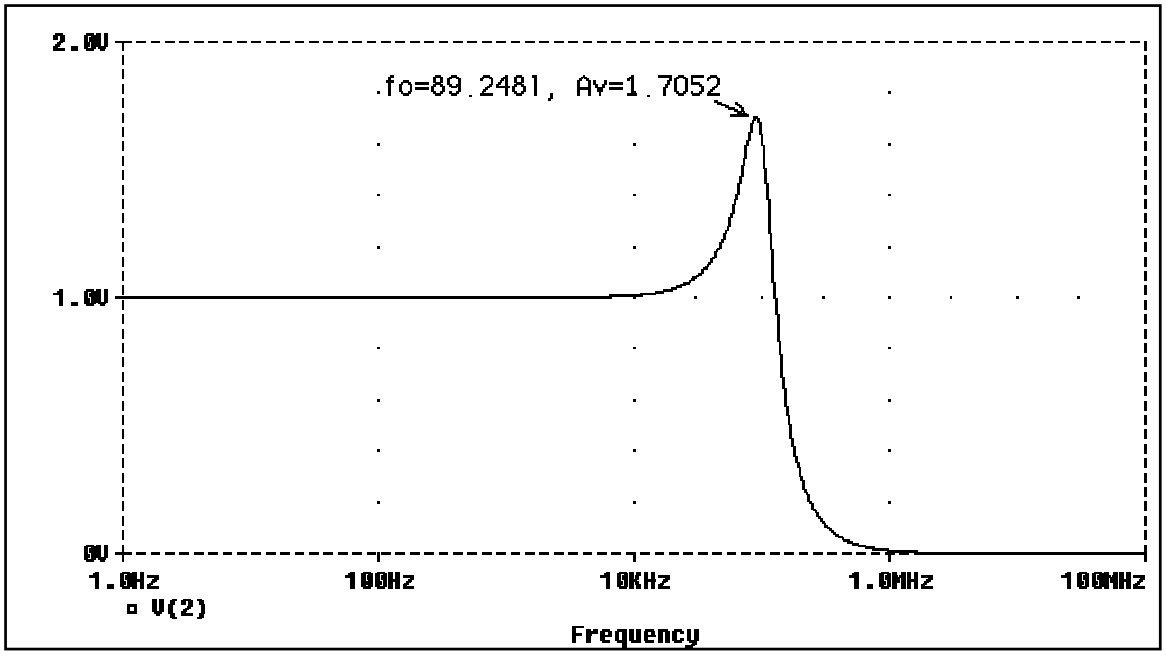
Actual 3 OTAs Circuit Implementation Netlist

```
*Filename = "univ2_a3.cir"
*Biquad 2nd order filter. fo=100K

Vin 1 0 DC 0V AC 1V
*LP
*Xs3flt 1 0 0 2 S3FLT
*HP
*Xs3flt 0 1 0 2 S3FLT
*BP
*Xs3flt 0 0 1 2 S3FLT
*BR
Xs3flt 1 1 0 2 S3FLT

 .SUBCKT S3FLT v1 v2 v3 v0
```

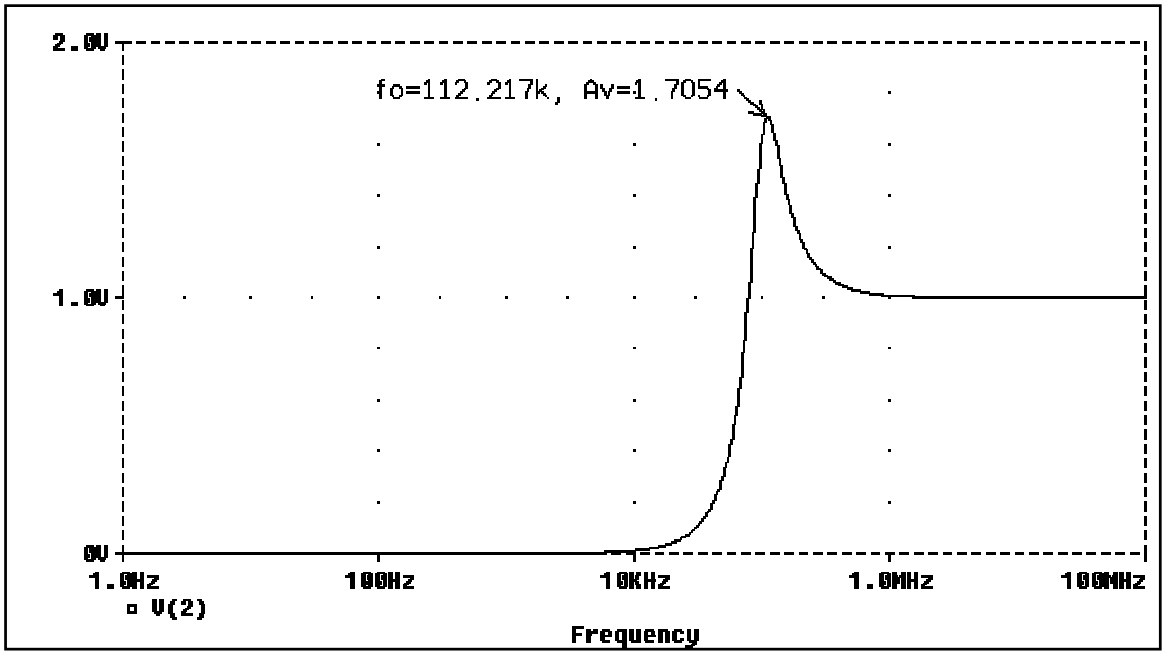
```
.PARAM C=135.98pF
Xota1 v1 v0 n2 WSOTA
Xota2 n2 0  v0 WSOTA
Xota3 v3 v0 v0 WSOTA1
C1 n2 0 {C} IC=0V
C2 v0 v2 {C} IC=0V
.ENDS

.SUBCKT WSOTA in+ in- out
* Power supplies
VDD vdd 0 DC 2.5V
VSS vss 0 DC -2.5V

* Wmin=Lmin=6 Lambda for linear analog circuit
.PARAM Wn=10.8U,  Ln=3.6U
.PARAM Wp=32.4U,  Lp=3.6U
.PARAM Wn7=3.6U,  Ln7=8.4U
.PARAM Wp7=5.4U,  Lp7=4.2U
.PARAM IB=10UA

* Biasing Circuit to generates vb1, vb2, vb3, vb4
MPB1 vb1 vb1 vdd vdd PMOS1 W={Wp}  L={Lp}
MPB2 m1  vb1 vdd vdd PMOS1 W={Wp}  L={Lp}
MPB3 vb2 vb1 vdd vdd PMOS1 W={Wp}  L={Lp}
MPB4 m3  m2  m1  vdd PMOS1 W={Wp}  L={Lp}
MPB5 vss m2  vb2 vb2 PMOS1 W={Wp}  L={Lp}
MPB0 m2  m2  vb1 vb1 PMOS1 W={Wp7} L={Lp7}
MNB0 m3  m3  vb4 vss NMOS1 W={Wn7} L={Ln7}
MNB1 vdd m3  vb3 vss NMOS1 W={Wn}  L={Ln}
MNB2 vb4 vb4 vss vss NMOS1 W={Wn}  L={Ln}
MNB3 vb3 vb4 vss vss NMOS1 W={Wn}  L={Ln}
ISS m2  vss {IB}

* Wide Swing OTA Implementation
MN1 n1  in+  n3  vss NMOS1 W={Wn}  L={Ln}
MN2 n2  in-  n3  vss NMOS1 W={Wn}  L={Ln}
MN5 n4  vb3  n5  vss NMOS1 W={Wn}  L={Ln}
MN7 out vb3  n6  vss NMOS1 W={Wn}  L={Ln}
MN6 n5  n4   vss vss NMOS1 W={Wn}  L={Ln}
MN8 n6  n4   vss vss NMOS1 W={Wn}  L={Ln}
MN3 n3  vb3  n7  vss NMOS1 W={Wn}  L={Ln}
MN4 n7  vb4  vss vss NMOS1 W={Wn}  L={Ln}
MP6 n1  vb1  vdd vdd PMOS1 W={Wp}  L={Lp}
MP8 n2  vb1  vdd vdd PMOS1 W={Wp}  L={Lp}
MP5 n4  vb2  n1  vdd PMOS1 W={Wp}  L={Lp}
MP7 out vb2  n2  vdd PMOS1 W={Wp}  L={Lp}
MP1 n5  in+  n8  vdd PMOS1 W={Wp}  L={Lp}
MP2 n6  in-  n8  vdd PMOS1 W={Wp}  L={Lp}
MP4 n9  vb1  vdd vdd PMOS1 W={Wp}  L={Lp}
MP3 n8  vb2  n9  vdd PMOS1 W={Wp}  L={Lp}
.ENDS

.SUBCKT WSOTA1 in+ in- out
* Power supplies
VDD vdd 0 DC 2.5V
VSS vss 0 DC -2.5V

* Wmin=Lmin=6 Lambda for linear analog circuit
.PARAM Wn=10.8U,  Ln=3.6U
.PARAM Wp=32.4U,  Lp=3.6U
.PARAM Wn7=3.6U,  Ln7=8.4U
.PARAM Wp7=5.4U,  Lp7=4.2U
.PARAM IB=3.8UA
```

```
* Biasing Circuit to generates vb1, vb2, vb3, vb4
MPB1 vb1 vb1 vdd vdd PMOS1 W={Wp}  L={Lp}
MPB2 m1  vb1 vdd vdd PMOS1 W={Wp}  L={Lp}
MPB3 vb2 vb1 vdd vdd PMOS1 W={Wp}  L={Lp}
MPB4 m3  m2  m1  vdd PMOS1 W={Wp}  L={Lp}
MPB5 vss m2  vb2 vb2 PMOS1 W={Wp}  L={Lp}
MPB0 m2  m2  vb1 vb1 PMOS1 W={Wp7} L={Lp7}
MNB0 m3  m3  vb4 vss NMOS1 W={Wn7} L={Ln7}
MNB1 vdd m3  vb3 vss NMOS1 W={Wn}  L={Ln}
MNB2 vb4 vb4 vss vss NMOS1 W={Wn}  L={Ln}
MNB3 vb3 vb4 vss vss NMOS1 W={Wn}  L={Ln}
ISS m2  vss {IB}

* Wide Swing OTA Implementation
MN1 n1  in+  n3  vss NMOS1 W={Wn}  L={Ln}
MN2 n2  in-  n3  vss NMOS1 W={Wn}  L={Ln}
MN5 n4  vb3  n5  vss NMOS1 W={Wn}  L={Ln}
MN7 out vb3  n6  vss NMOS1 W={Wn}  L={Ln}
MN6 n5  n4   vss vss NMOS1 W={Wn}  L={Ln}
MN8 n6  n4   vss vss NMOS1 W={Wn}  L={Ln}
MN3 n3  vb3  n7  vss NMOS1 W={Wn}  L={Ln}
MN4 n7  vb4  vss vss NMOS1 W={Wn}  L={Ln}
MP6 n1  vb1  vdd vdd PMOS1 W={Wp}  L={Lp}
MP8 n2  vb1  vdd vdd PMOS1 W={Wp}  L={Lp}
MP5 n4  vb2  n1  vdd PMOS1 W={Wp}  L={Lp}
MP7 out vb2  n2  vdd PMOS1 W={Wp}  L={Lp}
MP1 n5  in+  n8  vdd PMOS1 W={Wp}  L={Lp}
MP2 n6  in-  n8  vdd PMOS1 W={Wp}  L={Lp}
MP4 n9  vb1  vdd vdd PMOS1 W={Wp}  L={Lp}
MP3 n8  vb2  n9  vdd PMOS1 W={Wp}  L={Lp}
.ENDS

.MODEL NMOS1 NMOS VTO=1 KP=40U
+ GAMMA=1.0 LAMBDA=0.02 PHI=0.6
+ TOX=0.05U LD=0.5U CJ=5E-4 CJSW=10E-10
+ U0=550 MJ=0.5 MJSW=0.5 CGSO=0.4E-9 CGDO=0.4E-9
.MODEL PMOS1 PMOS VTO=-1 KP=15U
+ GAMMA=0.6 LAMBDA=0.02 PHI=0.6
+ TOX=0.05U LD=0.5U CJ=5E-4 CJSW=10E-10
+ U0=200 MJ=0.5 MJSW=0.5 CGSO=0.4E-9 CGDO=0.4E-9

* Analysis
.AC DEC 100 1Hz 100MegHz
.PROBE
.END
```

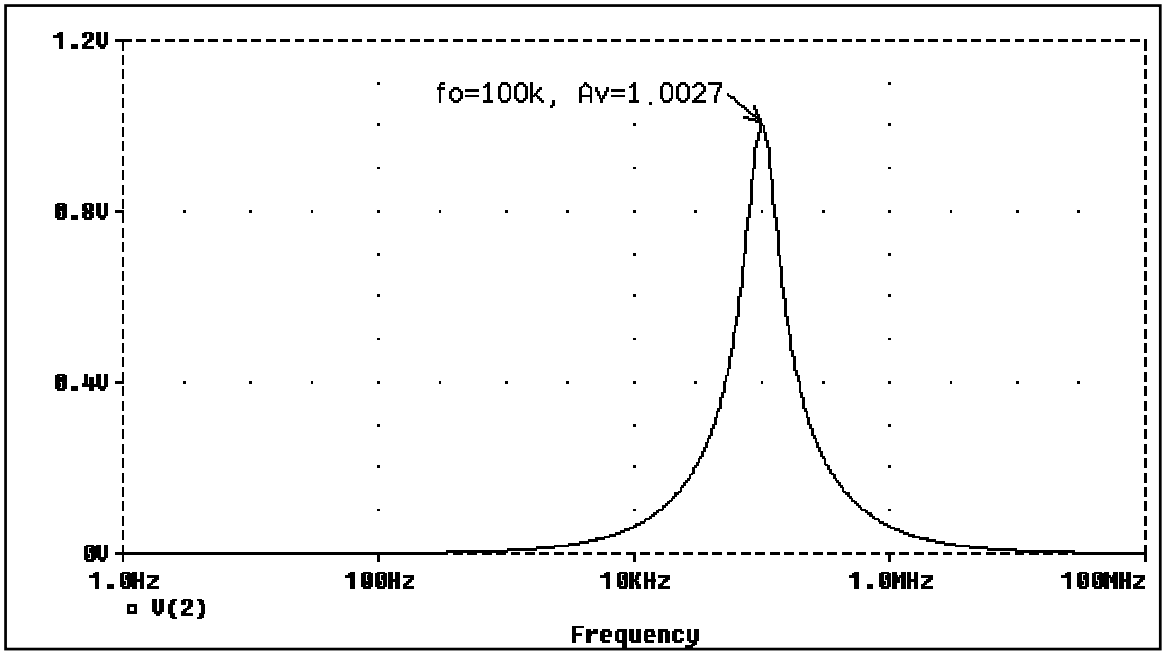
Frequency Response of Actual OTA Circuit Implementation



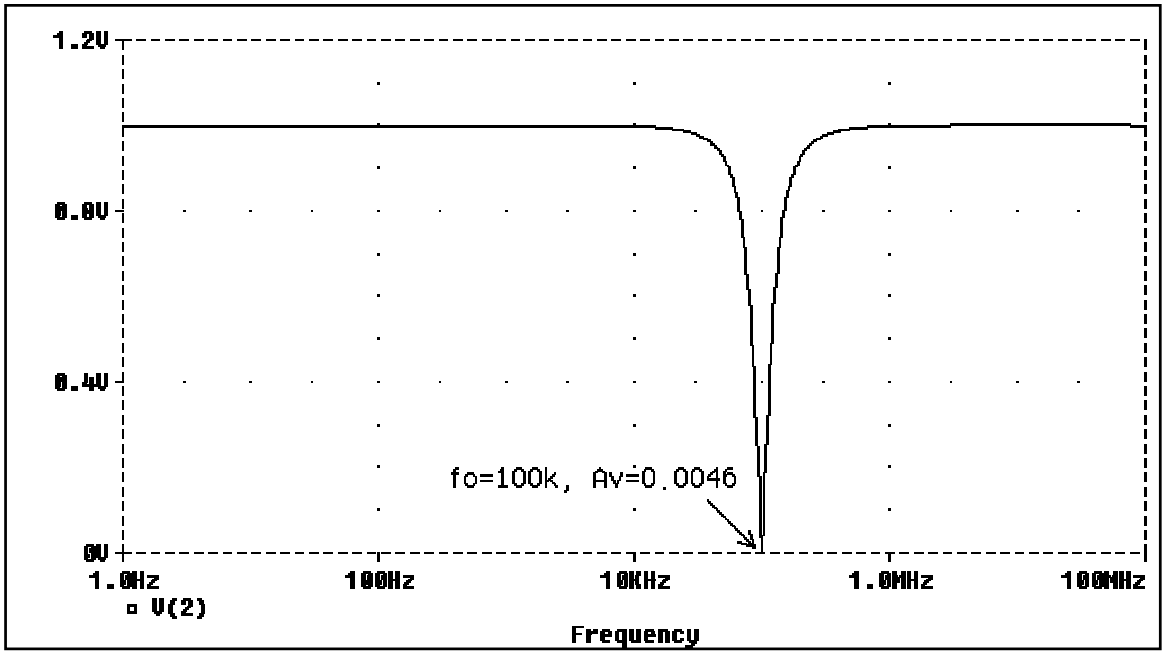
Implemented Second Order Lowpass Filter Response



Implemented Second Order Highpass Filter Response



Implemented Second Order Bandpass Response



Implemented Second Order Bandreject Response