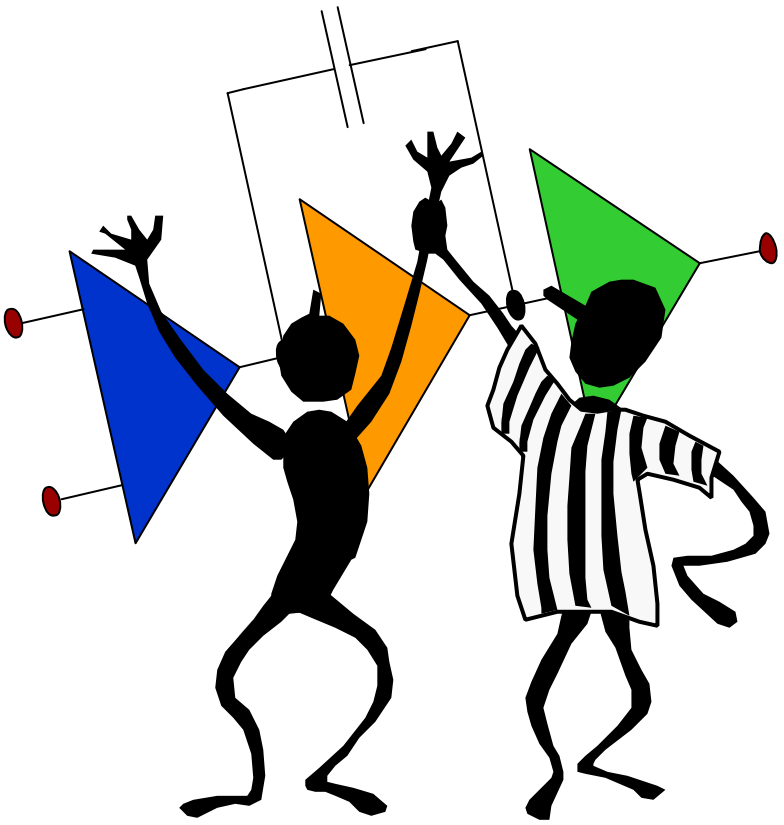
Analog Microelectronics

Advanced Current Mirrors and OpAmp Design



Today's handouts:
(1) Lecture Slides

Outline

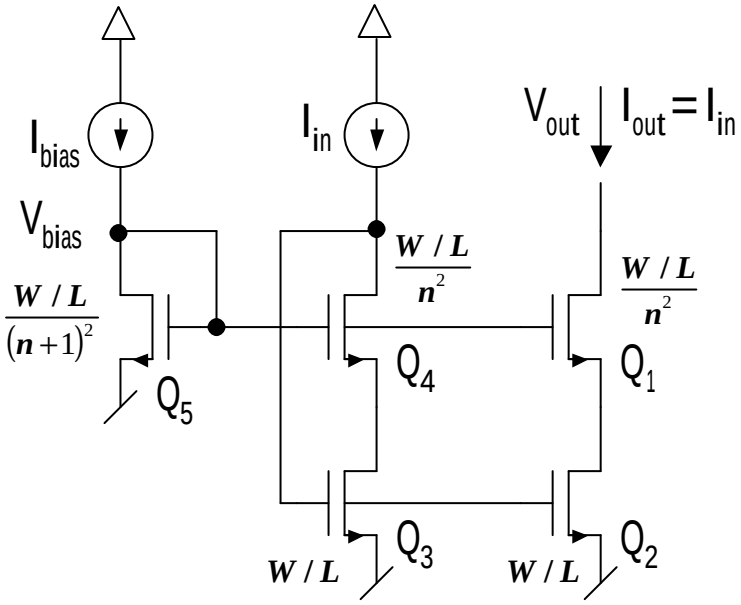
- Johns&Martin
  - advanced current mirrors (chap 6.1)
    - wide-swing current mirrors
    - wide-swing constant-transconductance bias circuit
    - enhanced output-impedance current mirrors (not yet)
    - wide-swing current mirror with enhanced output impedance (not yet)
  - folded-cascode OpAmp (chap 6.2)
    - small signal analysis
    - slew rate
- Exercises (6.8 & 6.10)
  - spice simulations
  - problems

Advanced current mirrors
wide-swing current mirrors

- The classical two-stage OpAmp was dicussed in vlsi27.
- Recently a number of alternate OpAmps designs have been gaining in popularity. They make use of more advanced current mirrors.

- Wide-swing current mirror:
  - as shorter channel lengths are used, it becomes more difficult to achieve reasonable OpAmp gains due to transistor output-impedance degradation caused to short-channel effects.
  - Conventional cascode current mirrors limit the signal swings available.
  - ➔ wide-swing current mirror

Wide-swing current mirrors

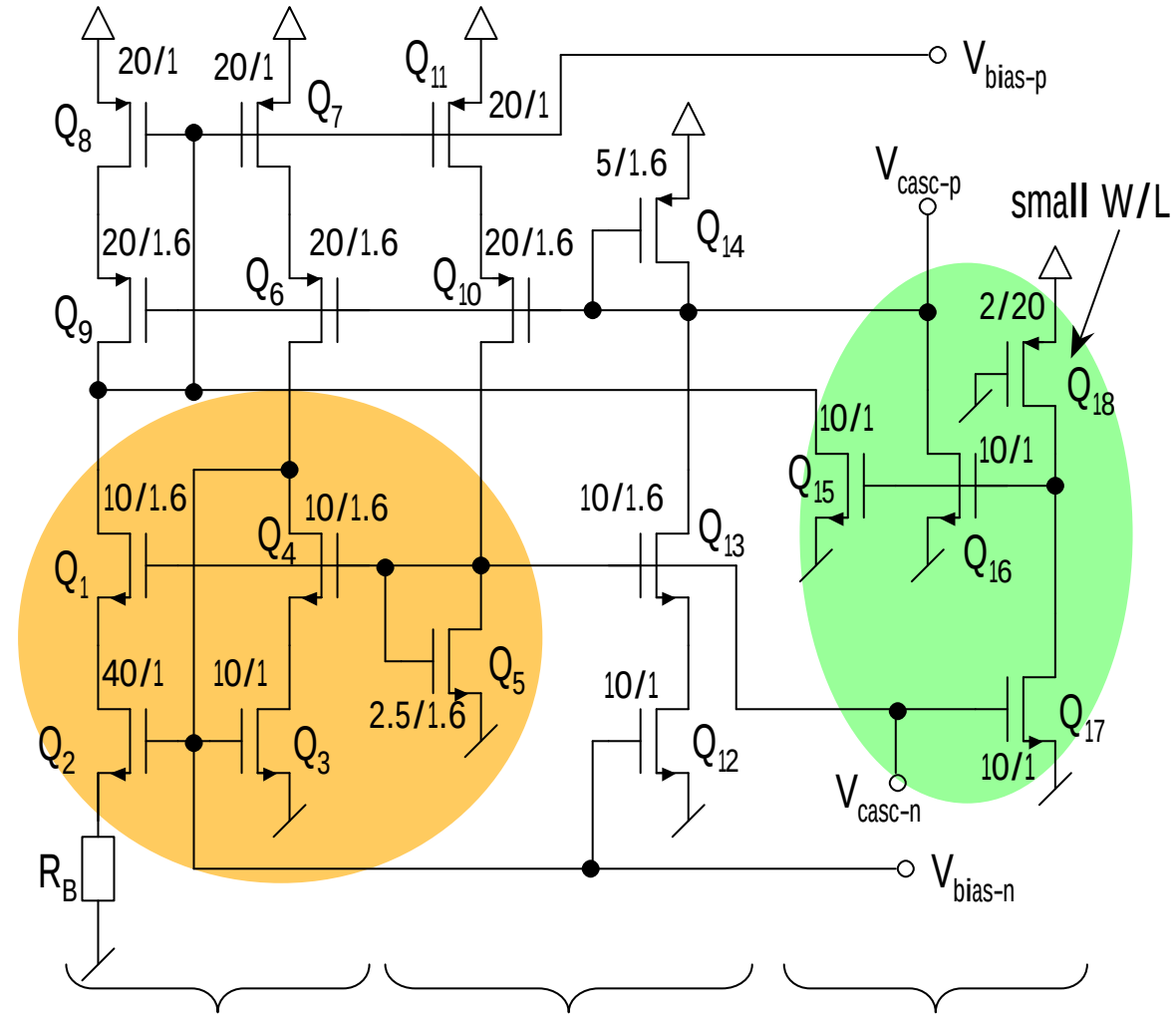


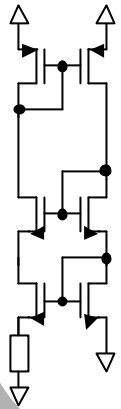
$$V_{out} > (n+1)V_{eff}$$

for Q_4: $V_{tn} > nV_{eff}$

- The basic idea is to bias the drain-source voltages of transistors Q_2 and Q_3 to be close to the mini-mum possible without them going to triode region.
- Choice of I_{bias}:
  - I_{bias} equal to maximum of I_{in} (all fets in saturation)
  - I_{bias} equal to nominal of I_{in} (for larger I_{in}, fets in triode, but probably only during slew-rate)
- Design hints:
  - a common choice for n is unity
  - Q_5 larger (0,1V to 0.15V) in order to offset the increased threshold voltages for Q_1 and Q_4 due to their body effects
  - L of Q_1 , Q_4 and Q_5 are twice minimal channel length, L of Q_2 and Q_3 are just slightly larger than minimal channel length (high frequency poles)

Wide-swing constant-transconductance bias circuit





see vlsi-27 slide 29

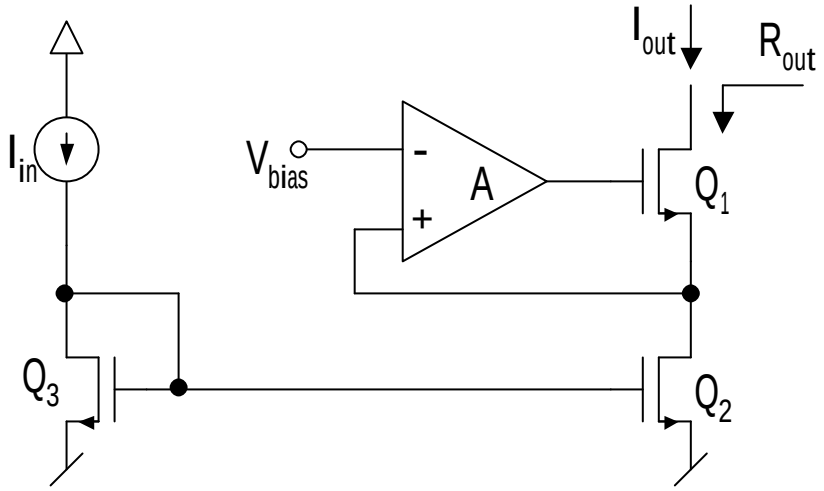
injects current as long as $I_{D's}$ are zero

Enhanced output-impedance current mirror

- Another variation of the cascode current mirror is the enhanced output-impedance current mirror shown as simplified version
- basic idea: use of feedback amplifier to keep the drain-source voltage across Q_2 stable, irrespetive of the output voltage

⇨ the additional amplifier increases the output impedance (see classical cascode current mirror, vlsi-25 slides 16, 17)

$$R_{out} \cong g_{m1} r_{ds1} r_{ds2} (1 + A)$$

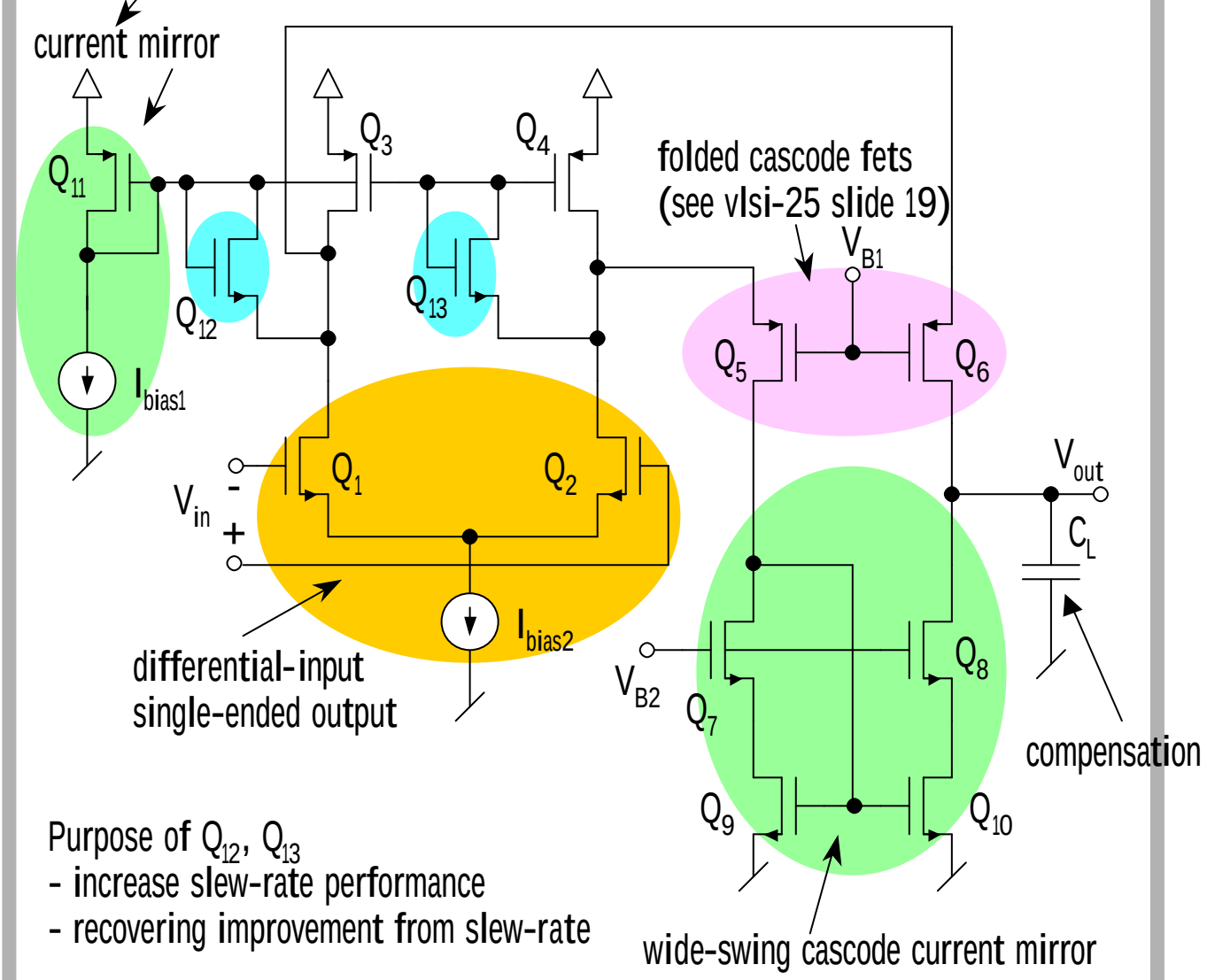


Folded-cascode OpAmp

- many modern integrated CMOS OpAmps are designed to drive only capacitive loads
- capacitive-only loads do not need voltage buffers to obtain low output impedance of the OpAmp
- thus it is possible to realize OpAmps having higher speed and larger signal swings than those who must drive resistive loads
- these improvements are obtained by having only one single high-impedance node at the OpAmp output that drives only capacitive loads
- all internal nodes have relatively low impedance (around g_m) thus the speed is optimized
- the compensation is usually achieved by the load capacitance
- the most important parameter is their transconductance:
  operational transconductance amplifier OTA

Folded-cascode OpAmp con't

may be replaced by a wide-swing
constant-transconductance bias network
and thus V_{B1}, V_{B2} would be V_{casc-n}, V_{casc-p}



Purpose of Q_{12}, Q_{13}
- increase slew-rate performance
- recovering improvement from slew-rate

Design hints:
- I_{bias1} and I_{bias2} should be derived from a single bias network
- any current mirrors should be designed by parallel combination of unit size fets

Folded-cascode OpAmp small-signal analysis

Assumption: g_{m5} and g_{m6} are much larger than g_{ds3} and g_{ds4}
- differential output current from drains of differential pair Q_1 and Q_2 is applied to the load capacitance
- the small-signal current from Q_1 passes directly from source to drain of Q_6 and thus to C_L (indirect for Q_2 to Q_5 and C_L)

$$A_v = \frac{V_{out}(s)}{V_{in}(s)} = g_{m1} Z_L(s) \qquad \text{(for } g_{m1} = g_{m2}\text{)}$$

$$A_v(s) = \frac{g_{m1} r_{out}}{1 + s r_{out} C_L} \qquad r_{out} \cong \frac{g_m r_{ds}^2}{2}$$

(see vlsi-25 slide 20)

for mid-band and high frequencies $A_v \cong \frac{g_{m1}}{sC_L}$

thus the unity-gain frequency is $w_t \cong \frac{g_{m1}}{C_L}$

Design hint:
- for large load capacitances a maximal transconductance of input fets maximizes band width, use n-channel fets
- input bias current 4 times larger than cascode current (maximizing dc gain)

Lead compensation (series resistance R_C to C_L)

$$A_v(s) = \frac{g_{m1}}{\frac{1}{r_{out}} + \frac{1}{R_C + 1/sC_L}} \cong \frac{g_{m1}(1 + sR_C C_L)}{sC_L}$$

R_C can be choosen to place a zero at 1.2 times unity-gain frequency

Folded-cascode OpAmp slew-rate

- The diode connected fets Q_{12} and Q_{13} are turned off during normal operation and have almost no effect
- slew-rate limiting behavior:
  - assume there is a large differential input voltage that causes Q_1 to be turned on hard and Q_2 to be turned off
  - since Q_2 is off, all of the bias current of Q_4 will be directed to through cascode fet Q_5 through n-channel current mirror and out of the load capacitance
  - the output voltage will decrease linearly with a slew-rate given by:

$$SR \cong \frac{I_{d4}}{C_L}$$

  - Q_1 and current source I_{bias} will go into triode region, moving the drain voltage of Q_1 to the negative power supply
  - Q_{12} and Q_{13} clamp the drain voltages so they don't change as much during slew-rate limitation
  - in addition Q_{12} and Q_{13} increase the bias currents for Q_3 and Q_4 and thus for C_L

Exercises VLSI-28

Ex ana6.2 (difficulty: medium): find reasonable fet sizes for the folded-cascode OpAmp: Assume pos/neg 2.5V power supply, power dissipation maximal 2mW, current ratio 4:1 between input and cascode fets, bias current or Q_{11} is 1/30 of Q_3 (thus ignoring it for power dissipation), maximum fet width is 300um, $L = 1.6$um and $V_{eff} = 0.25$V for all except input fets, $W_1 = W_2 = 300$um, rounding widths to 10um, $CL = 10$pF, $u_n C_{ox} = 3u_p C_{ox} = 96$uA/V^2

a) find all fet sizes, unitiy gain frequency,

b) slew-rate with and without clamp fets

c) reasonable lead compensation R_C

Result: a) Q_1 to $Q_4 = 300$um, Q_5, $Q_6 = 60$um, Q_7 to $Q_{10} = 20$um, Q_{11} to $Q_{12} = 10$um, $w_t = 2p$ 38MHz

b) SR = 32V/us,

c) RC = 347W (see Johns/Martin pp271-273)

Coming Up...

- Next topic…

  Comparators

- Readings for next time…

  Johns&Martin: Sections 6.1 and 6.2

- Exercises:

  Have a look at the exercises in *Johns&Martin*.