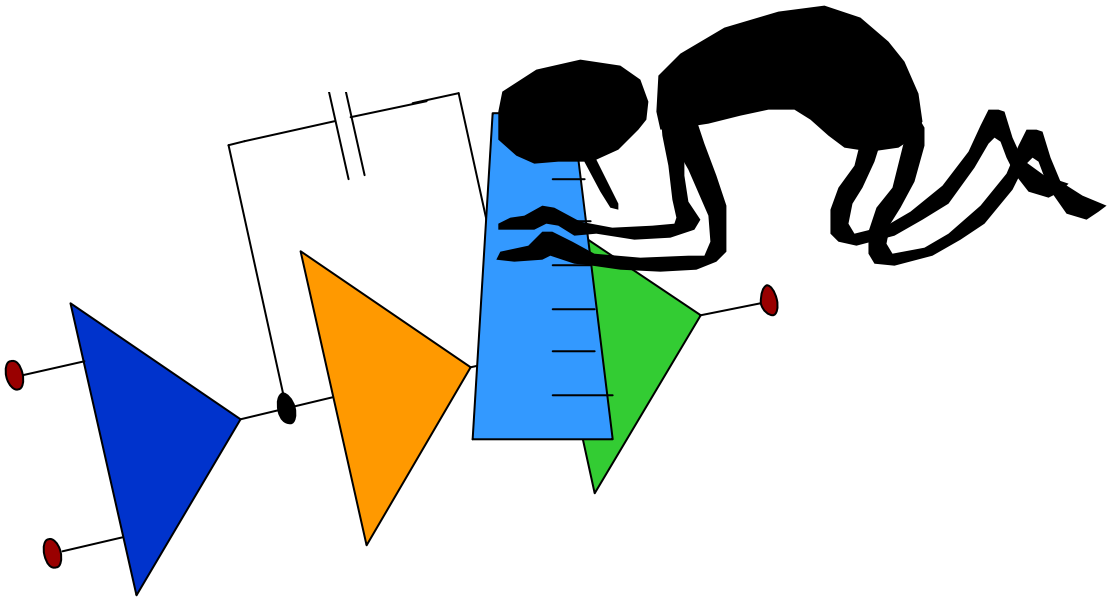
Analog Microelectronics

Basic OpAmp Design
and Compensation



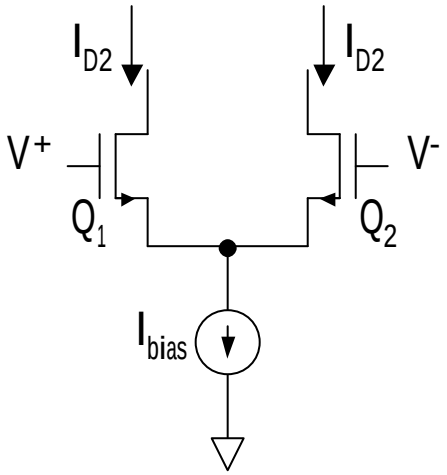
Today's handouts:
(1) Lecture Slides

Outline

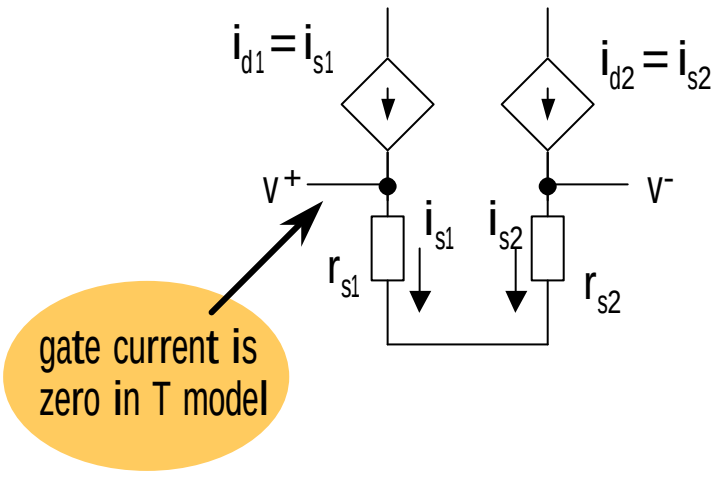
- Johns&Martin
  - MOS differential pair and gain stage (chap 3.8)
  - two-stage CMOS OpAmp (chap 5.1)
    - gain
    - frequency response
    - systematic offset voltage
    - n- or p-channel input stage
  - feedback and OpAmp compensation (chap 5.2)
    - first-order model of closed loop-amplifier
    - linear settling time
    - OpAmp compensation
    - compensation of two-stage OpAmp
    - lead compensation
    - making compensation independent of process and temp
    - biasing OpAmp to have stable transconductance
- Exercises (5.3-5.5)
  - hand calculations
  - spice simulations

MOS Differential Pair and Gain Stage

- most integrated amplifiers have differential input, realized with a differential transistor pair

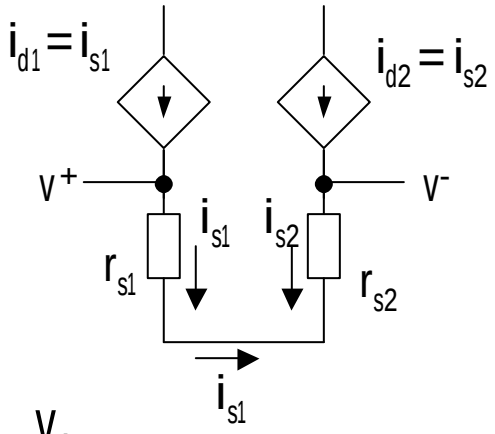


- a low-frequency small-signal equivalent circuit is based on the T model for the MOS transistor



MOS Differential Pair (con't 1)

to simplify analysis the output impedance of the transistor is ignored



Definition:

$$v_{in} \triangleq v^+ - v^-$$

$$i_{d1} = i_{s1} = \frac{v_{in}}{r_{s1} + r_{s2}} = \frac{v_{in}}{1/g_{m1} + 1/g_{m2}}$$

since both Q_1 and Q_2 have the same bias currents, $g_{m1} = g_{m2}$

$$i_{d1} = \frac{g_{m1}}{2} v_{in} \qquad i_{d2} = -\frac{g_{m1}}{2} v_{in}$$

Definition:

$$i_{out} \triangleq i_{d1} - i_{d2}$$

thus:

$$i_{out} = g_{m1} v_{in}$$

MOS Differential Pair (con't 2)

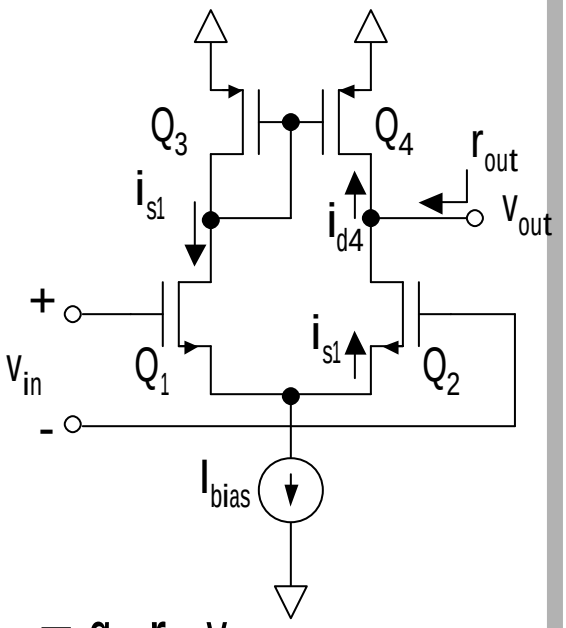
If a differential pair has a current mirror as an active load, a complete differential-input, single-ended-output gain stage can be realized.

to simplify analysis the output impedance of the transistor is ignored

$$i_{d4} = i_{d3} = -i_{s1}$$

and

$$i_{d2} = -i_{s1}$$

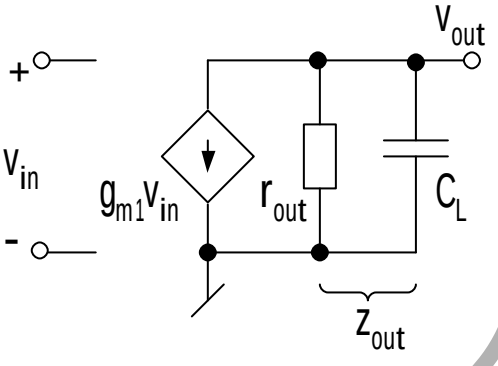


$$v_{out} = (-i_{d2} - i_{d4})r_{out} = 2i_{s1}r_{out} = g_{m1}r_{out}v_{in}$$

this result assumes that the output impedance is purely resistive, if there is also a capacitive load C_L we get:

$$A_v = g_{m1}z_{out} \qquad \text{where} \quad z_{out} = r_{out} \| 1/(sC_L)$$

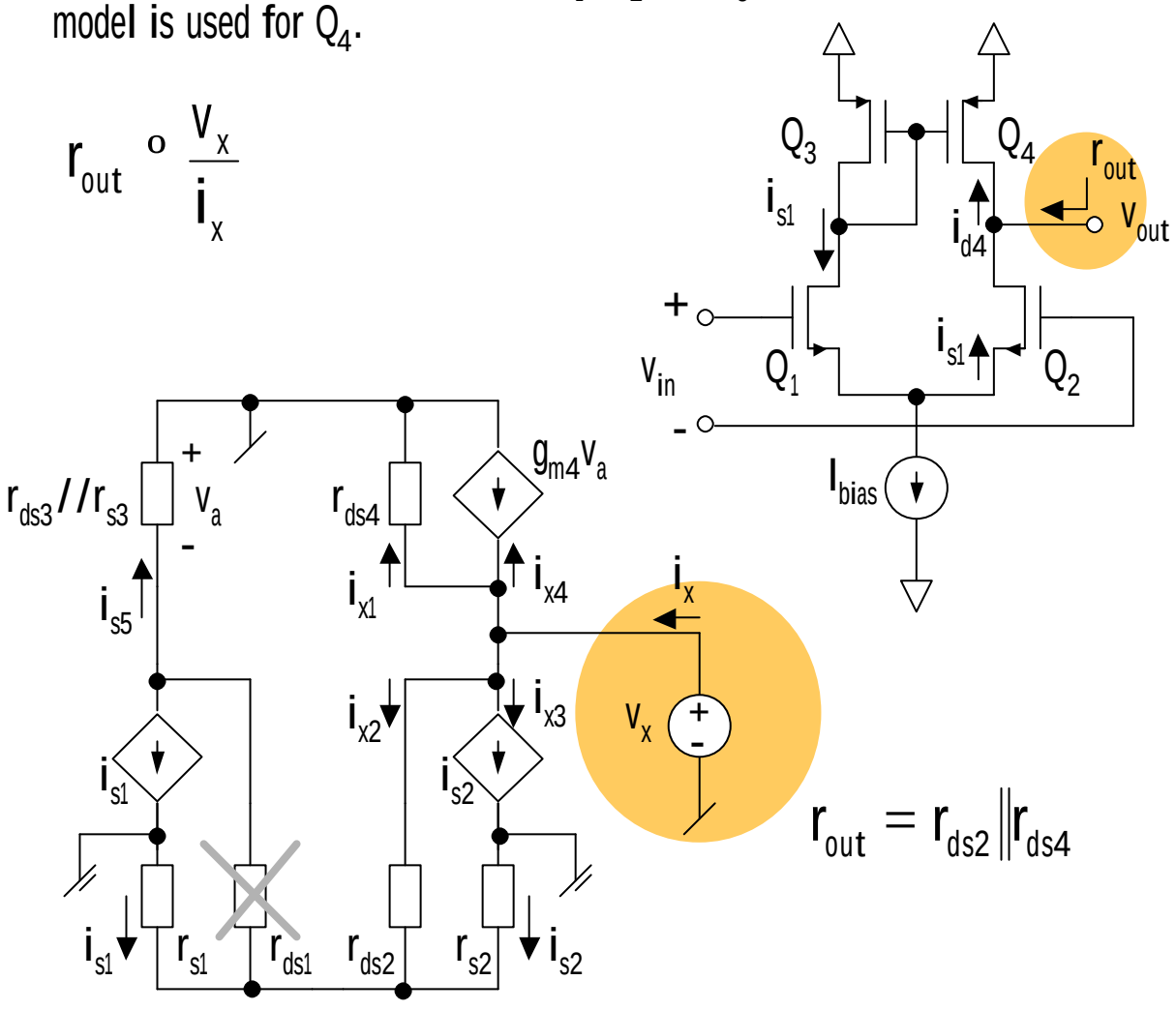
Thus, for this differential stage, a very simple model is used. This model implicitly assumes that the time constant at the output node is much larger than the time constant due to the parasitic capacitances at Q_1 and Q_2



MOS Differential Pair (con't 3)

The evaluation of the output resistance r_{out} is determined by using the small-signal equivalent circuit and applying a voltage at the output node. Note that the T-model is used for Q_1, Q_2 and Q_3, and the the hybrid-π model is used for Q_4.

$$r_{out} \equiv \frac{v_x}{i_x}$$



$$r_{out} = r_{ds2} \| r_{ds4}$$

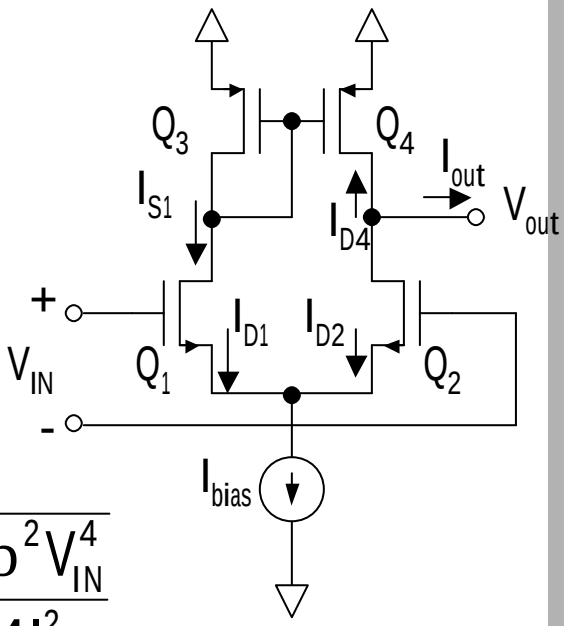
$$A_v = g_{m1}\left(r_{ds2} \| r_{ds4}\right)$$

MOS Differential Pair (con't 4)

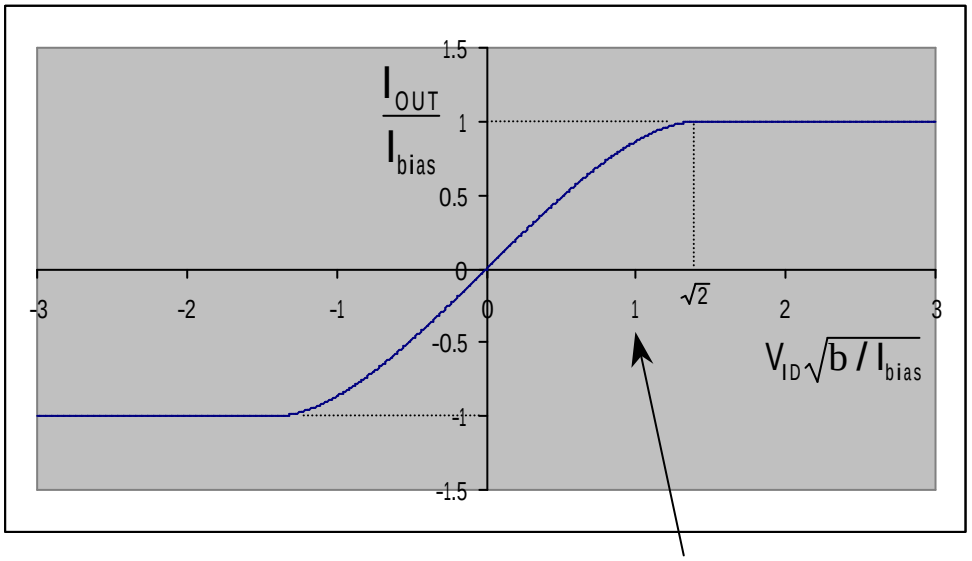
The evaluation of the large signal amplification is determined by using the large-signal transistor model in the active region of the fets.
Note that the T-model is used for Q_1, Q_2 and Q_3, and the the hybrid-p model is used for Q_4.

$$I_D = \frac{m_0 C_{ox}}{2}\frac{W}{L}(V_{GS} - V_{tn})^2$$

$$I_D = \frac{b}{2}(V_{GS} - V_{tn})^2$$



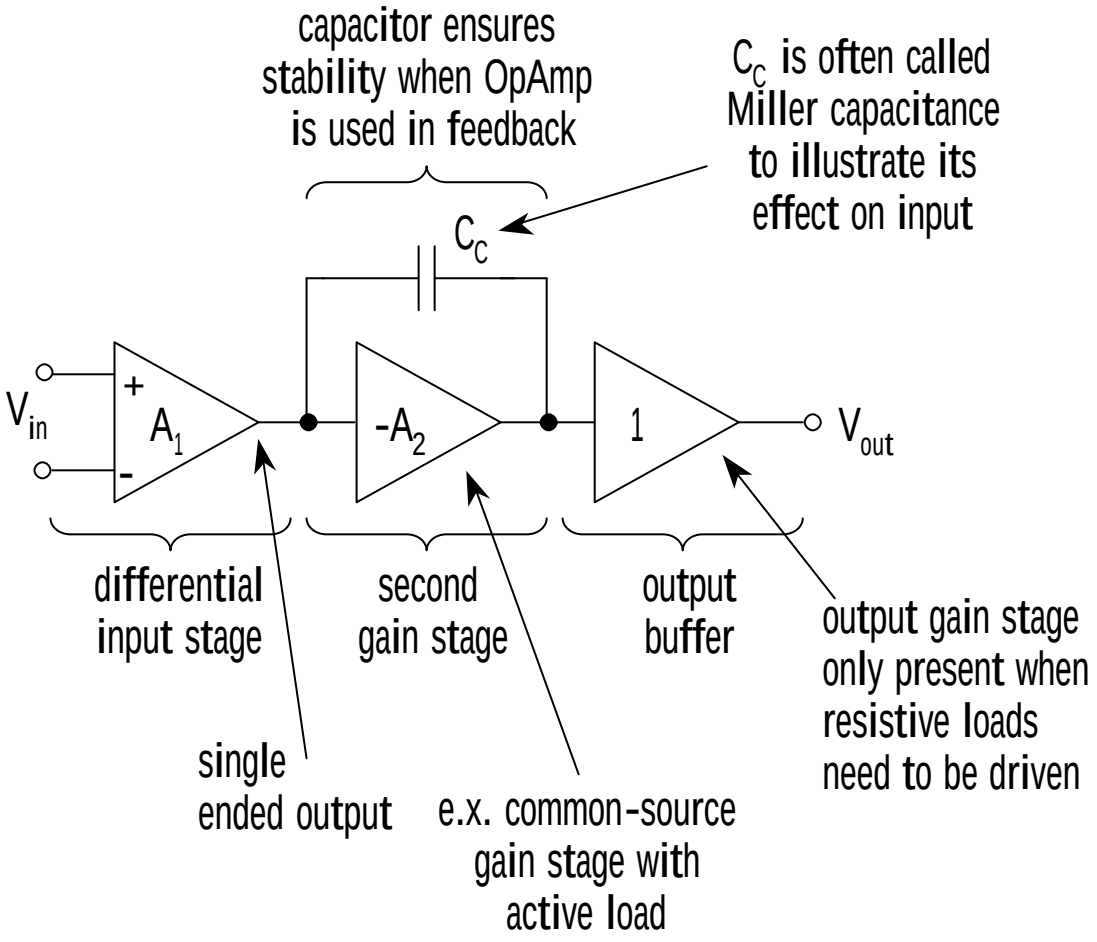
$$I_{OUT} = I_{D1} - I_{D2} = I_{bias}\sqrt{\frac{bV_{IN}^2}{I_{bias}} - \frac{b^2V_{IN}^4}{4I_{bias}^2}}$$



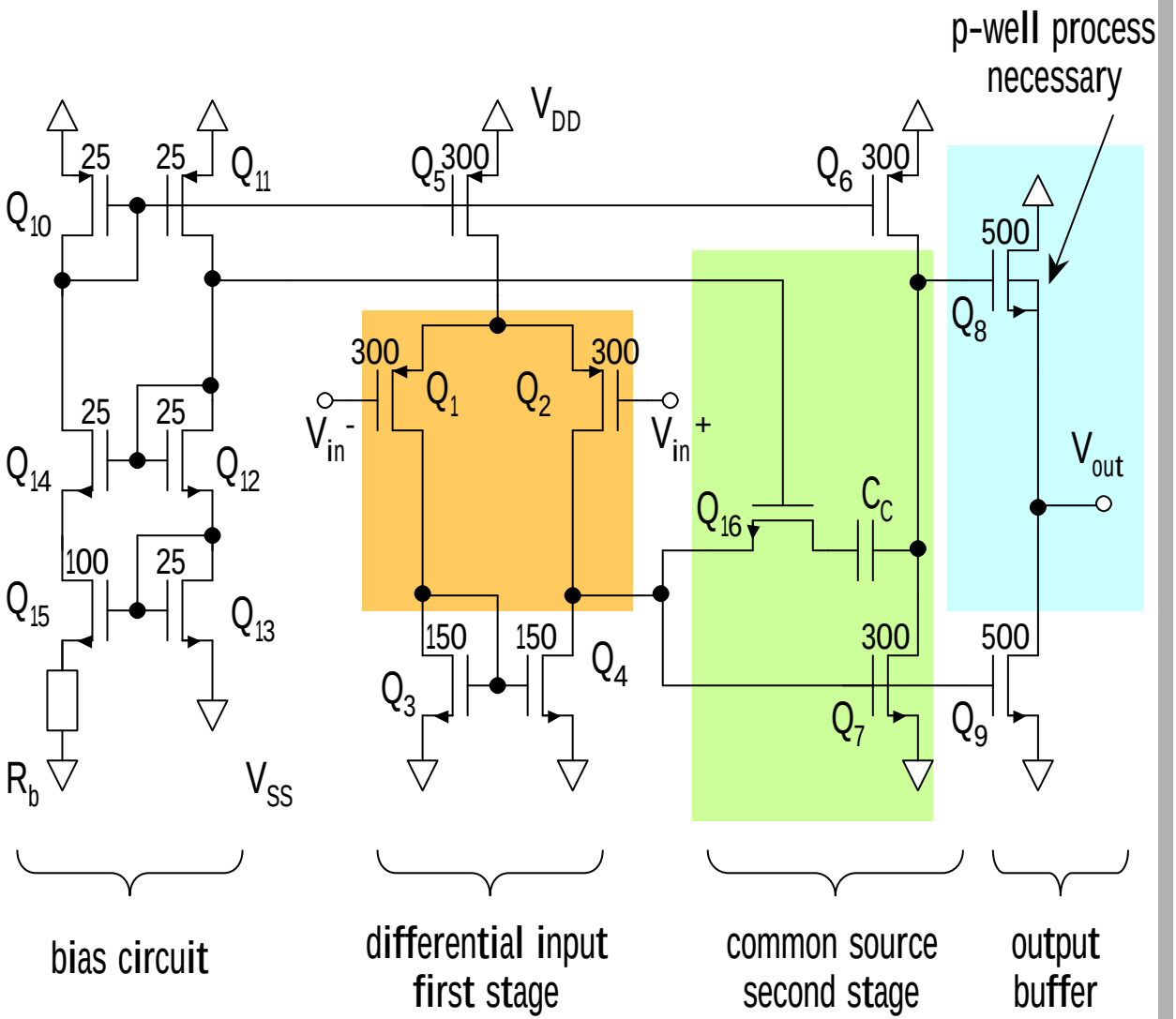
typical value for $I_{bias} = 0.1mA$: $\sqrt{b / I_{bias}} = 5.4$ $V_{IN} = 187mV$

Two-Stage CMOS OpAmp

- Basic OpAmp design are discussed
  - OpAmp gain
  - frequency response
  - slew rate
  - systematic offset voltage
  - n-channel or p-channel input stage



CMOS realization of a two-stage OpAmp



- p-channel input stage
- all transistor lengths are 1.6mm (1mm process)
- reasonable sizes for lengths of the transistors might be somewhere between 1.5 and 2 times the minimum transistor length

Two-Stage OpAmp Gain

- overall gain for low frequency application is the most critical parameter of an OpAmp

gain of the first stage (differential stage)

$$A_{v1} = g_{m1}\left(r_{ds1} \| r_{ds4}\right)$$

$$g_{m1} = \sqrt{2m_p C_{ox}\left(\frac{W}{L}\right)_1 I_{D1}} = \sqrt{2m_p C_{ox}\left(\frac{W}{L}\right)_1 \frac{I_{bias}}{2}}$$

$$r_{dsi} \cong a\,\frac{L_i}{I_{Di}}\sqrt{V_{DGi} + V_{ti}}$$

approximation to the finite output resistance, where a is technology dependent parameter: 5e-6 $V^{1/2}$/m ignoring short channel effects

gain of the second stage (common-source stage)

$$A_{v2} = -g_{m7}\left(r_{ds6} \| r_{ds7}\right)$$

gain of the third stage (common-drain stage)

$$A_{v3} = \frac{g_{m9}}{G_L + g_{m9} + g_{ds8} + g_{ds9}}$$

gain of the third stage with body effect (bulk not connected to source)

$$A_{v3} = \frac{g_{m9}}{G_L + g_{m9} + g_{s8} + g_{ds8} + g_{ds9}}$$

body effect constant $\gamma = 0.5V^{1/2}$
$2\phi_F = 0.7V$

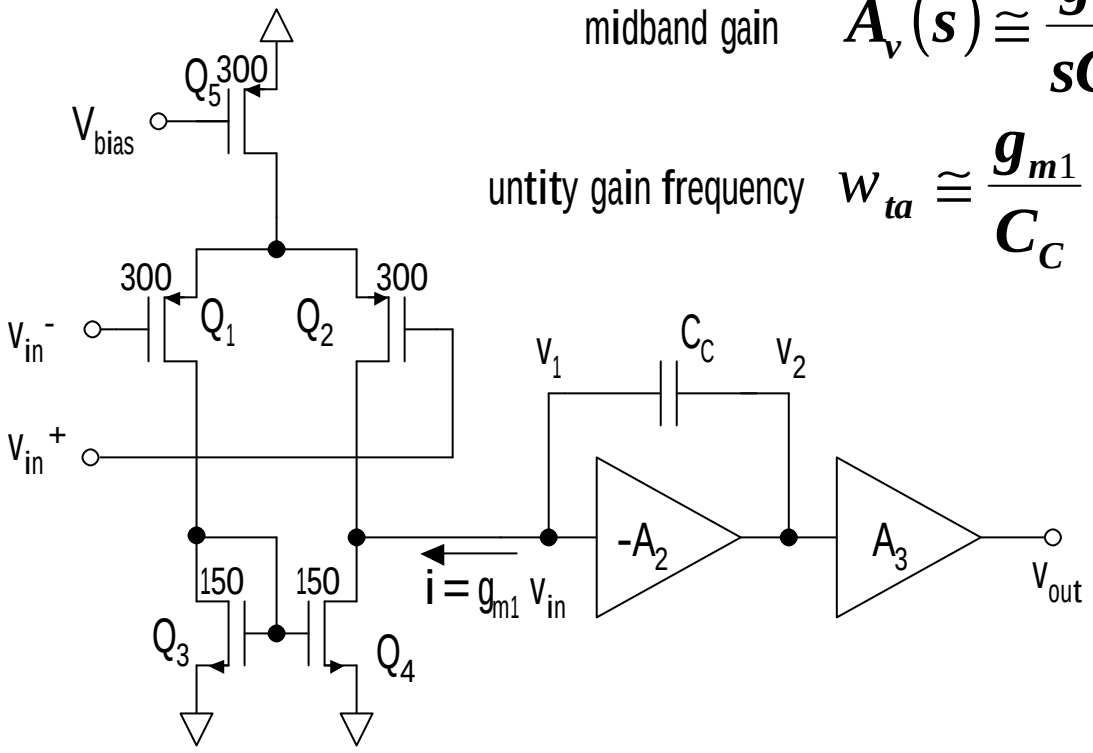
$$g_s = \frac{g_m \gamma}{2\sqrt{V_{SB} + 2\phi_F}}$$

Two-Stage OpAmp Frequency Response

- frequency response where capacitor C_c causes the magnitude of the gain to decrease, but still well below unity gain frequency (open-loop gain = 1)
- ⇨ midband frequency
- only compensation capacitor C_C repsected
- assume Q_{16} is not present (resistor for lead compensation, effect only at unity gain frequency)
- discuss simplified circuit:

midband gain $$A_v(s) \cong \frac{g_{m1}}{sC_C}$$

untity gain frequency $$w_{ta} \cong \frac{g_{m1}}{C_C}$$

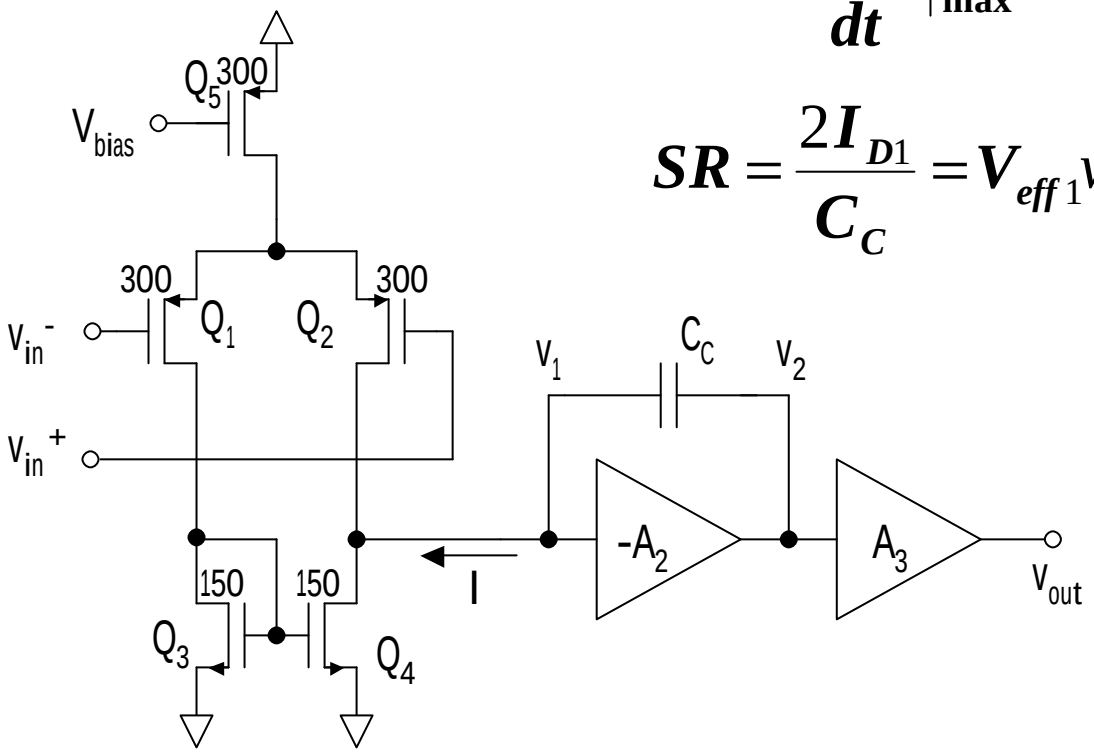


Two-Stage OpAmp Slew Rate

- slew rate SR is the maximum rate the output changes when input signals are large
- at slew rate limitation all current of Q_5 goes either in Q_1 or Q_2
- ⇨ this current has to go through C_C

$$SR \equiv \left. \frac{dv_{out}}{dt} \right|_{\max}$$

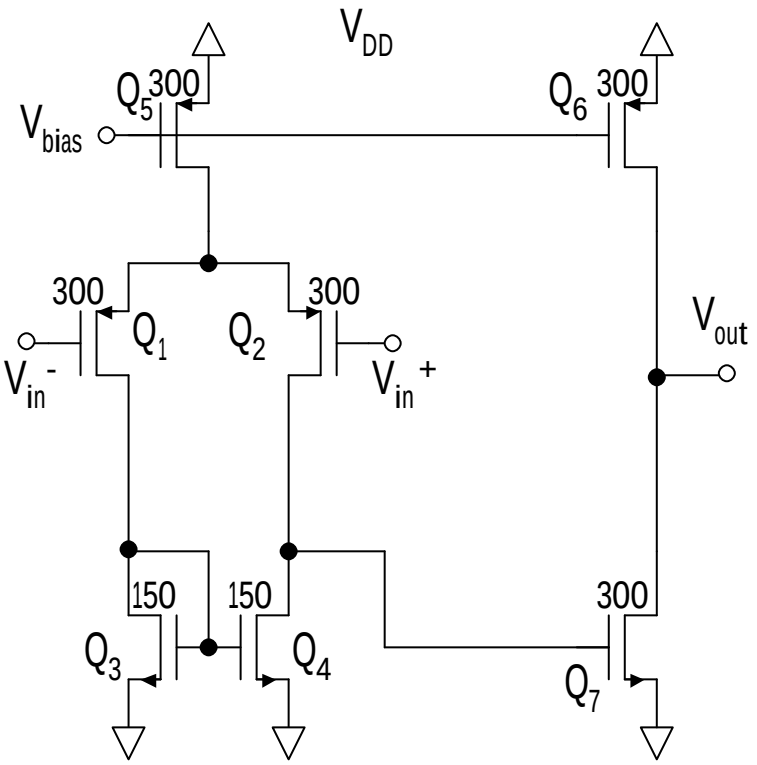
$$SR = \frac{2I_{D1}}{C_C} = V_{eff\,1} w_{ta}$$



increasing V_{eff1} and w_{ta} increases SR
p-channel fet inputs increases SR
increasing V_{eff1} reduces transconductance g_{m1}

Two-Stage OpAmp
Systematic Offset Voltage Cancelation

- two-stage OpAmps may have a systematic input offset voltage if not properly designed
  - the differential input is zero: $v_{in}^{+} = v_{in}^{-}$
  - $I_{D6} = I_{D7}$, which requires a well defined V_{GS7} value



$$\frac{(W/L)_7}{(W/L)_4} = 2\frac{(W/L)_6}{(W/L)_5}$$

Two-Stage OpAmp
n- or p- channel input stage

- comparison between n- and p-channel input stage OpAmps
  - overal dc gain is largely unaffected since both designs have one stage with n-channel and one stage with one or more p-channel driving fets.
  - for a given power dissipation, and therefore bias current, having a p-channel input-pair stage maximizes the slew rate.
  - having a p-channel input first stage implies that the second stage has an n-channel input drive fet. This arrangement maximizes the transconductance of the drive fet of teh 2nd stage, which is critical when high frequency operation is important.
  - output stage: n-channel source follower is preferable because this will have less of a voltage drop (if separate p-well is used). Its higher transconductance reduces the effect of the load cap on the second pole. There is also less degradation on the gain when small load resistances are being driven.
- ⇨ p-channel input fets for the first stage is almost always the best choice

Feedback and OpAmp Compensation

- OpAmps in closed-loop configurations are discussed and how to compensate an OpAmp to ensure that the closed-loop configuration is not only stable but has a good settling characteristic.
- Optimum compensation of OpAmps is typically considered to be one of the most difficult parts in the OpAmp design procedure.
  - first-order model of closed-loop amplifier
  - linear settling time
  - OpAmp compensation
  - compensating the two-stage OpAmp
  - lead compensation
  - making compensation independent of process and temperature
  - biasing an OpAmp to have stable transconductances

First Order Model of Closed-Loop Amplifier

- First order model of transfer function of a dominant-pole compensated OpAmp:

$$A(s) = \frac{A_0}{(1 + s/w_{p1})}$$

real axis dominant pole

unity gain frequency definition $|A(jw_{ta})| \equiv 1 \cong \frac{A_0}{w_{ta}/w_{p1}}$

unity gain frequency of first order OpAmp model $w_{ta} \cong A_0 w_{p1}$

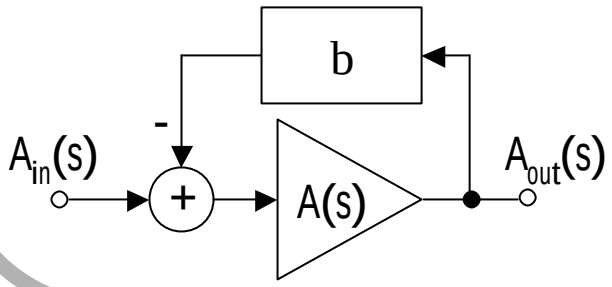
for midband frequencies $w_{p1} << w << w_{ta}$

$$A(s) \cong \frac{w_{ta}}{s}$$

closed-loop gain

$$A_{CL}(s) = \frac{A(s)}{1 + bA(s)}$$

$$A_{CL}(s) = \underbrace{\frac{1}{b}}_{\text{gain}} \frac{1}{(1 + s/bw_{ta})}$$



$$w_{-3dB} \cong bw_{ta}$$

Linear Settling Time

- the settling time performance is an important design parameter of OpAmps
  - the charge transfer in SC circuits is closely related to OpAmps step response
  - settling time is defined as the time it takes for an OpAmp to reach a specified percentage of its final value when a step input is applied
  - linear settling time portion is due to the finite unity gain frequency (independent on output step size)
  - nonlinear settling time portion is due to the slew rate limit (dependent on output step size)
  - ⇨ unity gain frequency estimation for linear settling time portion

-3dB frequency determines the settling-time response for s step input

$$t = \frac{1}{w_{-3dB}} = \frac{1}{bw_{ta}}$$

step response for a closed-loop OpAmp

$$v_{out}(t) = V_{step}\left(1 - e^{-t/t}\right)$$

if slew rate is larger, no SR limit will occur

$$\left.\frac{d}{dt} v_{out}(t)\right|_{t=0} = \frac{V_{step}}{t}$$

OpAmp Compensation (second order model)

- for compensating OpAmps the first order model is insufficient, because it ignores poles and zeros at high frequencies which may cause instabilities.
- a more accurate open-loop transfer model adds one additional pole (real axis poles and zeros):

$$A(s) = \frac{A_0}{(1 + s/w_{p1})(1 + s/w_{eq})}$$

first dominant pole — higher frequency poles

- w_{eq} may be approximated with a set of real-axis poles and zeros:

$$\frac{1}{w_{eq}} \cong \sum_{i=2}^{m} \frac{1}{w_{pi}} - \sum_{i=1}^{n} \frac{1}{w_{zi}}$$

- phase margin PM is an often used measure how far an OpAmp with feedback is from becoming unstable

$$\angle LG(jw) = -90^\circ - \tan^{-1}(w/w_{eq})$$

unity gain of LG

$$PM \equiv \angle LG(jw_t) - (-180^\circ) = 90^\circ - \tan^{-1}(w_t/w_{eq})$$

independent of b ⟶ $w_t = \tan(90^\circ - PM)\, w_{eq}$

OpAmp Compensation (second order model con't)

- Closed-loop gain if b is frequency independent (if w_t is far away from high frequency poles and zeros)

$$A_{CL}(s) = \frac{A_{CL0}}{1 + \frac{s(1/w_{p1} + 1/w_{eq})}{1 + bA_0} + \frac{s^2}{1 + bA_0}}$$

$$A_{CL0} = \frac{A_0}{1 + bA_0} \cong \frac{1}{b}$$

- General equation for a second order transfer function:

$$H_2(s) = \frac{K}{1 + \frac{s}{w_o Q} + \frac{s^2}{w_0^2}}$$

- comparing:

$$w_0 = \sqrt{(1 + bA_0)(w_{p1} w_{eq})} \cong \sqrt{b w_{ta} w_{eq}}$$

$$Q = \frac{\sqrt{(1 + bA_0)(w_{p1} w_{eq})}}{1/w_{p1} + 1/w_{eq}} \cong \sqrt{\frac{b w_{ta}}{w_{eq}}}$$

$$\% \text{ overshoot} = 100^{\frac{-p}{\sqrt{4Q^2 - 1}}}$$

OpAmp Compensation (2nd order transfer function)

- Relationship between Q factor and phase margin
  - transfer function: Q=sqrt(1/2):
    - no peaking
    - widest passband
    - $w_0 = w_{-3dB}$
  - step response: Q<=0.5 (real poles and zeros)
    - no peaking
  - step response: Q > 0.5
    - percentage of overshoot to be calculated

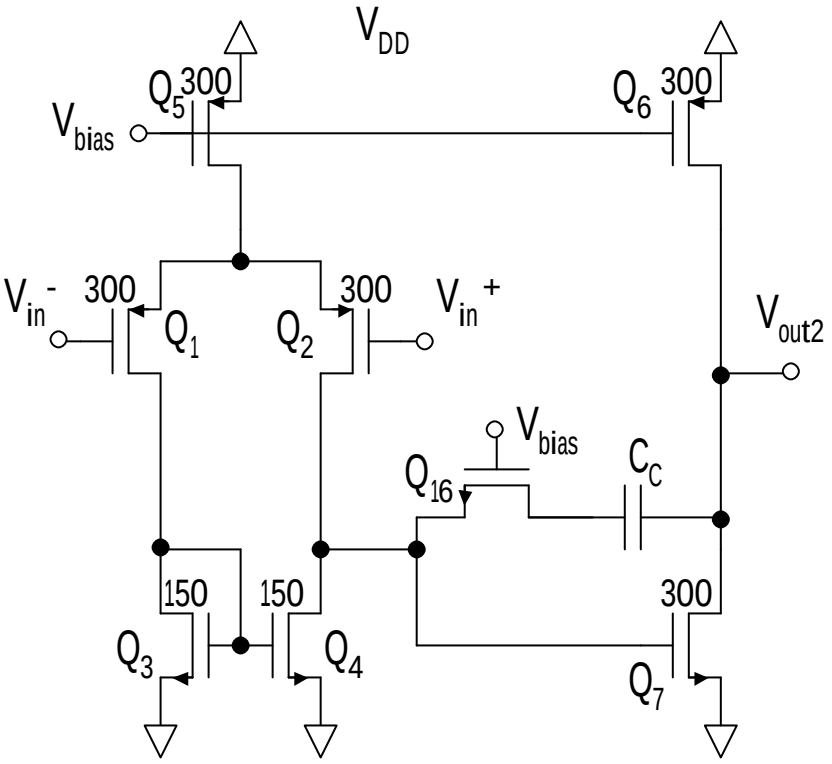
PM	w_t/w_{eq}	Q factor	% overshoot
55	0.700	0.925	13.3%
60	0.580	0.817	8.7%
65	0.470	0.717	4.7%
70	0.360	0.622	1.4%
75	0.270	0.527	0.008%

- Phase margin is much larger than supposed to be necessary (80 to 85)

Compensating the Two-Stage OpAmp

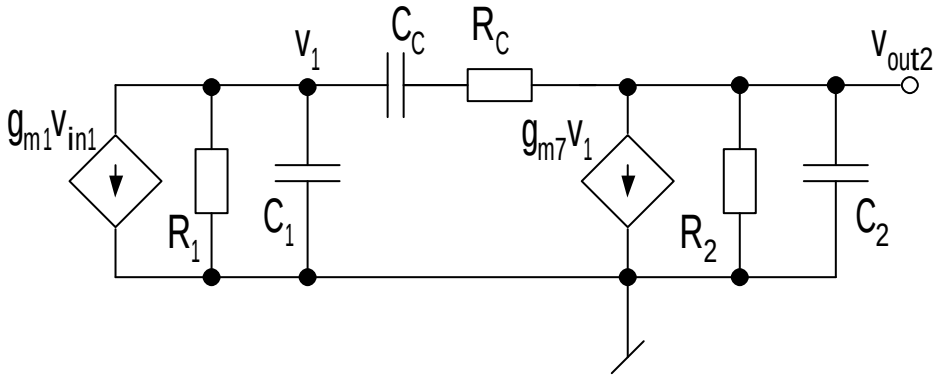
- Capacitor C_C realizes dominant-pole compensation and thereby control w_{p1} and w_{ta} : $w_{ta} = A_0 w_{p1}$
- fet Q_{16} is included to realize a left-half-plane zero at frequencies around or slightly above w_t (lead-compensation). Q_{16} has $V_{ds} = 0V$ and thus is in triode region:

$$R_C = r_{ds16} = \frac{1}{m_n C_{ox} \left(\frac{W}{L} \right)_{16} V_{eff\,16}}$$



Compensating the Two-Stage OpAmp small-signal model

- simplified small-signal model of two-stage OpAmp for compensation analysis



$$R_1 = r_{ds4} \| r_{ds2} \qquad C_1 = C_{db2} + C_{db4} + C_{gs7}$$

$$R_2 = r_{ds6} \| r_{ds7} \qquad C_2 = C_{db7} + C_{db6} + C_{L2}$$

analysis shown in Johns&Martin

dominant pole:

$$w_{p1} \cong \frac{1}{g_{m7} R_1 R_2 C_C}$$

nondominant pole:

$$w_{p2} \cong \frac{g_{m7}}{C_1 + C_2}$$

for $R_C = 0$:

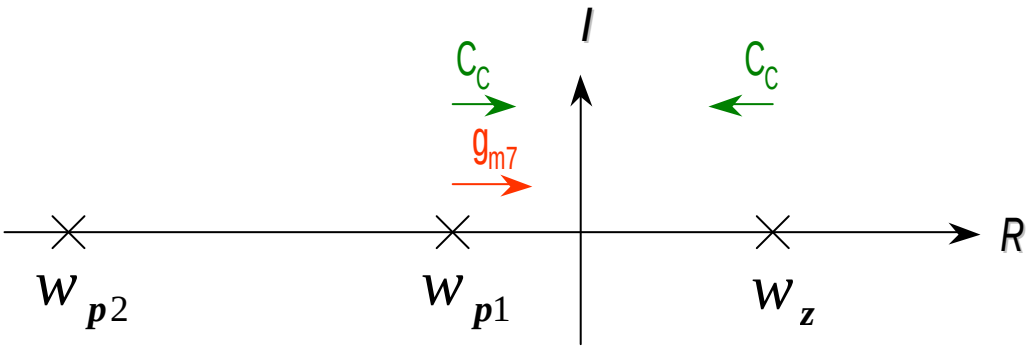
$$w_z = -\frac{g_{m7}}{C_C}$$

lead compemsation (R_C not zero)

$$w_z = \frac{-1}{C_C\left(1/g_{m7} - R_C\right)}$$

Compensating the Two-Stage OpAmp (discussion)

$$D(s) = \left(1 + \frac{s}{w_{p1}}\right)\left(1 + \frac{s}{w_{p2}}\right)$$



$$w_{p1} \cong \frac{1}{g_{m7} R_1 R_2 C_C} \qquad w_z = -\frac{g_{m7}}{C_C}$$

$$w_{p2} \cong \frac{g_{m7}}{C_1 + C_2}$$

- increasing g_{m7} separates poles (pole-splitting)
- however, right-hand plane zero introduces negative phase shift into transfer function
- increasing C_C moves w_{p1} and w_{z1} to low frequency and thus does not help

Compensating the Two-Stage OpAmp (lead compensation)

- with a non-zero R_C, a third pole is introduced, but is at high frequency and has almost no effect
- However the zero opens a number of possibilities:

$$w_z = \frac{-1}{C_C\left(1/g_{m7} - R_C\right)}$$

  - one could eliminate the right-half plane zero:

$$R_C = 1/g_{m7}$$

  - one could choose R_C to be even larger and thus move the right-half-plane zero into the left half plane to cancel the nondominant pole w_{p2}:

$$R_C = \frac{1}{g_{m7}}\left(1 + \frac{C_1 + C_2}{C_C}\right)$$

  - one could choose R_C even larger to move the now left-half-plane zero to a frequency slightly greater than the unity-gain frequency that would result without the resistor - say 20% larger (recommended): $w_z = 1.2w_t$

$$R_C \cong \frac{1}{1.2g_{m1}}$$

Lead Compensation Design Procedure

1. Start by choosing, somewhat arbitrarily, $C_C' \cong 5\text{pF}$
2. Using Spice, find the frequency at which a -125° phase shift exists. Let the gain at this frequency be denoted A' and w_t.
3. Choose a new C_C so that w_t becomes the unity-gain frequency of the loop gain, thus resulting in a 55° phase margin. This can be achieved by taking C_C according to the equation (iterations possible):

$$C_C = C_C' A'$$

4. Choose R_C according:

$$R_C = \frac{1}{1.2 w_t C_C}$$

4. The resulting phase margin is approximately 85° (leaving 5° for process variations). It may be necessary to iterate on R_C to optimize the phase margin
5. If after step 4 the phase margin is not adequate, then increase C_C while leaving R_C constant
6. Replace R_C by a fet with the following size:

$$R_C = r_{ds16} = \frac{1}{m_n C_{ox} \left(\frac{W}{L}\right)_{16} V_{eff\,16}}$$

Compensation Independent of Process and Temperature

- Making lead compensation process and temperature insensitive
- the ratios of all transconductances remain relatively constant over process and temperature variations as all fets depend on the same biasing network:

$$w_{p2} \cong \frac{g_{m7}}{C_1 + C_2} \qquad w_{ta} \cong \frac{g_{m1}}{C_C}$$

- when a resistor is used to realize lead compensation, R_C can also be made to track the inverse of transconductance ($1/g_{m7}$), and thus the lead compensation will be mostly independent of process and temperature variantions:

$$w_z = \frac{-1}{C_C\left(1/g_{m7} - R_C\right)}$$

Compensation Independent of Process and Temperature (con't 2)

Making R_C proportional to $1/g_{m7}$

$$R_C = r_{ds16} = \frac{1}{m_n C_{ox}\left(\frac{W}{L}\right)_{16} V_{eff\,16}}$$

$$g_{m7} = m_n C_{ox}(W/L)_7 V_{eff\,7}$$

The product R_C $1/g_{m7}$ needs to be constant

$$R_C g_{m7} = \frac{(W/L)_7 V_{eff\,7}}{(W/L)_{16} V_{eff\,16}}$$

Therefor, all that remains is to ensure that V_{eff16}/V_{eff7} is independent of process and temperature variations. The ratio can be made constant by deriving V_{gs16} from the same biasing circuit used to derive V_{gs7}

- The following approach results in the possibility of on-chip "resistors", realized by using triode-region fets that are accurately ratioed with respect to a single off-chip resistor -> modern mcircuit design

Compensation Independent of Process and Temperature (con't 3)

if $V_{eff\,13} = V_{eff\,7}$

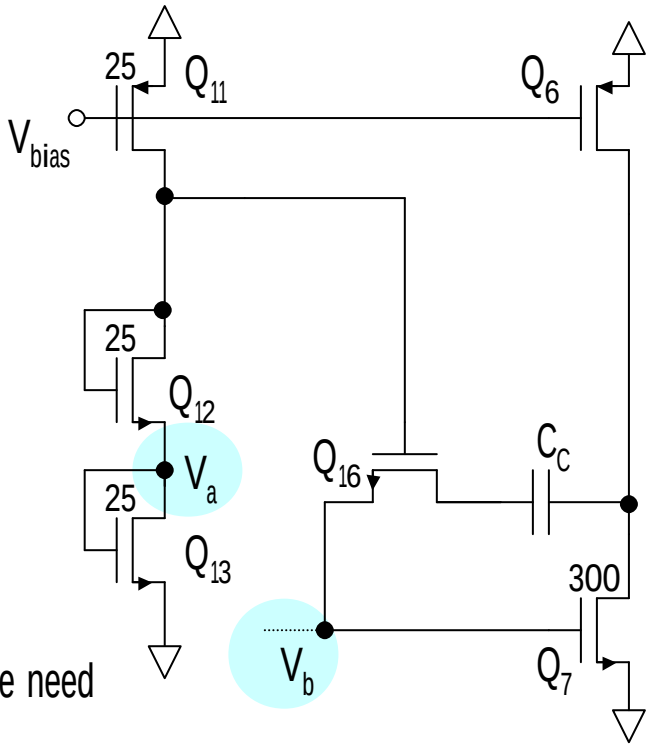
then $V_a = V_b$

then (gates connected)

$$V_{eff\,16} = V_{eff\,12}$$

thus $$\frac{V_{eff\,7}}{V_{eff\,16}} = \frac{V_{eff\,13}}{V_{eff\,12}}$$

to make $V_{eff\,13} = V_{eff\,7}$ we need



$$\sqrt{\frac{2I_{D7}}{m_n C_{ox}(W/L)_7}} = \sqrt{\frac{2I_{D13}}{m_n C_{ox}(W/L)_{13}}}$$

$$\frac{I_{D7}}{I_{D13}} = \frac{(W/L)_7}{(W/L)_{13}}$$

however the current is set by Q_6, Q_{11} $\quad \frac{I_{D7}}{I_{D13}} = \frac{(W/L)_6}{(W/L)_{11}}$

condition to be satisfied

$$\frac{(W/L)_6}{(W/L)_7} = \frac{(W/L)_{11}}{(W/L)_{13}}$$

$$R_C g_{m7} = \frac{(W/L)_7}{(W/L)_{16}} \sqrt{\frac{(W/L)_{12}}{(W/L)_{13}}}$$

as $I_{D12} = I_{D13}$ are equal

Biasing an OpAmp to Have Stable Transconductances

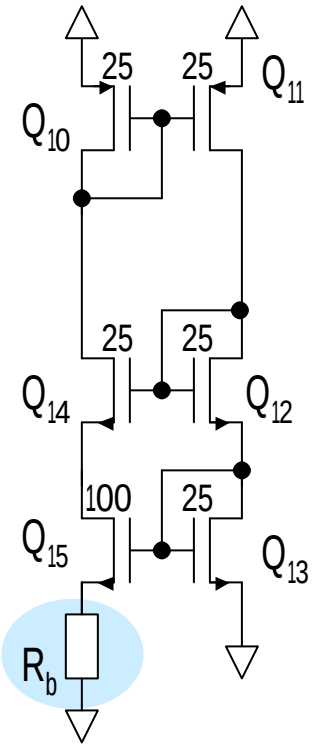
- Fet transconductances are the probably the most important parameters in OpAmps to be stabilized
- the following approach matches transconductances to conductance of a resistor
- as a result, the fet transconductances are independent of power-supply voltage as well as process and temperature variations

assuming $(W/L)_{10} = (W/L)_{11}$

$$g_{m13} = \frac{2\left[1 - \sqrt{\frac{(W/L)_{13}}{(W/L)_{15}}}\right]}{R_b}$$

for $(W/L)_{15} = 4(W/L)_{13}$

$$g_{m13} = \frac{1}{R_b}$$



$$g_{mi} = \sqrt{\frac{m_i (W/L)_i I_{Di}}{m_n (W/L)_{13} I_{D13}}} \times g_{m13}$$

Exercises VLSI-27

Ex ana3.9 (difficulty: easy): Consider a differential pair amplifier shown on transparency vlsi-27/3 where $I_{bias} = 200\mu A$ and all transistors have $W = 100\mu m$ and $L = 1.6\mu m$. Given $\mu_n C_{ox} = 92\mu A/V^2$ and $r_{ds-n} = 8000$ [L (μm)]/[ID (mA)]. Find the output impedance and the gain.

Result: $A_v = 68.6 V/V$, $r_{out} = 64k\Omega$ (see Johns/Martin pp146)

Ex ana5.1 (difficulty: easy): Find the gain of the OpAmp shown on transparency vlsi-27/9. Assume $I_{D5} = 100\mu A$, first stage $V_{DG} = 0.5V$, 2nd and 3rd stage $V_{DG} = 1V$ and bulk of Q_8 connected to V_{SS}. Given $\mu_n C_{ox} = 3\mu_p C_{ox} = 96\mu A/V^2$, $V_{DD} = -V_{SS} = 2.5V$, $R_L = 10k\Omega$, $\gamma = 0.5V^{1/2}$, $\phi_F = 0.35V$, $a = 5e6 V^{1/2}/m$, $V_{tn} = -V_{tn} = 0.8V$.

Result: $A_v = -6092 V/V$ (see Johns/Martin pp224)

Exercises VLSI-27 (con't 2)

Ex ana5.2 (difficulty: easy): Find the unity gain frequency of the OpAmp shown on transparency vlsi-27/9, with $C_C = 5pF$. Assume $I_{D5} = 100\mu A$, first stage $V_{DG} = 0.5V$, 2nd and 3rd stage $V_{DG} = 1V$ and bulk of Q_8 connected to V_{SS}. Given $\mu_n C_{ox} = 3\mu_p C_{ox} = 96\mu A/V^2$, $V_{DD} = -V_{SS} = 2.5V$, $R_L = 10k\Omega$, $\gamma = 0.5V^{1/2}$, $\phi_F = 0.35V$, $\alpha = 5e6V^{1/2}/m$, $V_{tn} = -V_{tn} = 0.8V$.

Result: $f_{ta} = 24.7MHz$ (see Johns/Martin pp227)

Ex ana5.3 (difficulty: easy): Find the slew rate of OpAmp on transparency vlsi-27/9, with $C_C = 5pF$. Assume $I_{D5} = 100\mu A$. What circuit chane could be done to double the slew rate but to keep ω_{ta} and bias currents unchanged?

Result: SR = 20V/ms, to double SR: $C_C = 2.5pF$ and $W_1 = W_2 = 75\mu m$ (see Johns/Martin pp229)

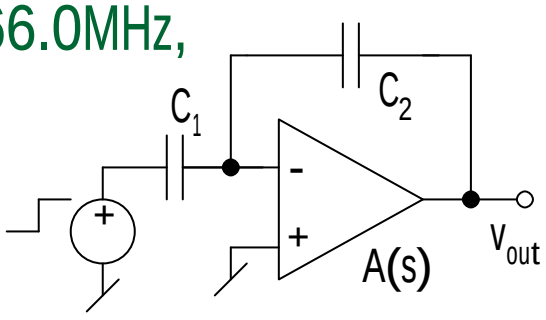
Exercises VLSI-27 (con't 3)

Ex ana5.4 (difficulty: easy): Consider the OpAmp shown on transparency vlsi-27/9, where Q_3 qnd Q_4 are each changed to widths of 120mm and we want the output stage have a bias current of 150mA. Find the new sizes of Q_6 qnd Q_7 such that there is no systematic offset voltage.

Result: $W_6 = 450\text{mm}$, $W_7 = 360\text{mm}$(see Johns/Martin pp231)

Ex ana5.5 (difficulty: easy): One phase of an SC circuit is shown, where the input can be modelled as a voltage step. If 0.1% accuracy is needed in the linear settling-time portion corresponding to 100ns, find the required unity-gain frequency in terms of the capacitance values, C_1 and C_2 and in absolute values. For $C_2 = 10C_1$ and for $C_2 = 0.2C_1$.

Result: $f_{ta} = 12.1\text{MHz}$, $f_{ta} = 66.0\text{MHz}$, (see Johns/Martin pp235)



Exercises VLSI-27 (con't 4)

Ex ana5.7 (difficulty: medium): OpAmp has an open-loop transfer function given by:

$$A(s) = \frac{A_0\left(1 + s/w_z\right)}{\left(1 + s/w_{p1}\right)\left(1 + s/w_2\right)}$$

Assume that $w_2 = 2p$ 50MHz and $A_0 = 10^4$

a) Assuming w_z = inf, find w_{p1} and the unity-gain frequency w_t' so that the OpAmp has a unity-gain phase margin of 55°

b) Assuming $w_z = 1.2\ w_t$' (use w_t' from a), what is the unity-gain frequency w_t. Also find the new phase margin.

Result: a) $w_t' = 2p$ 35MHz, $w_{p1} = 2p$ 4.27kHz, b) $w_t = 2p$ 46.6MHz, PM = -85° (see Johns/Martin pp245)

Coming Up...

- Next topic…

  Advanced Current Mirrors and OpAmps

- Readings for next time…

  Johns&Martin: Sections 3.8 and 5

- Exercises:

  Have a look at the exercises in *Johns&Martin*.