Bandgap Current Reference (RQE Submission)

Matthew C. Guyton and Hae-Seung Lee, MIT

March 13, 2003

Abstract

A simple low-power current source with low sensitivity to temperature and power-supply is presented. Implemented in a 0.35um CMOS process, the 2-terminal circuit directly produces a bandgap-referenced output current without the use of an operational amplifier. This design requires no excess biasing current.

The designed current source employs 6 transistors and 3 resistors. It exhibits 142ppm/degC over a 5-50 degC range. Output resistance is 350kOhm. Power consumed is 160uW measured at 80uA nominal output current and 2V supply.

The same basic design can be used to generate non-integer multiples of bandgap voltage without an op-amp.

1 Introduction

Most analog circuits require reference voltages and currents that do not vary with power supply voltage and temperature. The traditional solution to this problem is the 1.2V bandgap voltage reference. However, converting to a non-integer multiple of this voltage, or to a current reference

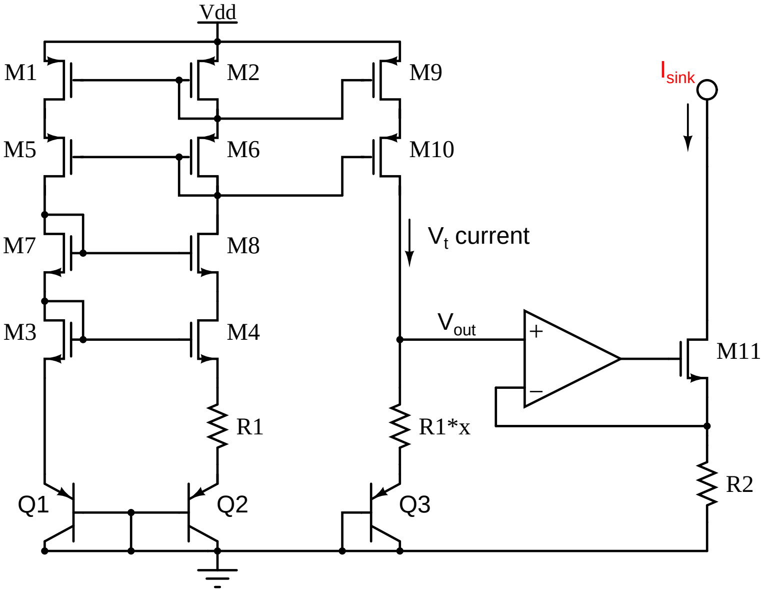

Figure 1: Traditional bandgap current reference [1, Fig. 4.50].

from this voltage source, requires an operational amplifier (see Fig. 1). The use of this extra op-amp leads to increased power consumption and design complexity.

In contrast, it has been shown [2] that a current-mode bandgap reference can be easily modified to generate non-integer multiples of bandgap voltage without using an extra op-amp. Recent designs for bandgap current references [2] [3] [4] have focused on implementations that use an op-amp within the bandgap core. While this topology allows for a smaller supply voltage (by about one gate-source voltage, V_{GS}), the use of an op-amp doubles the biasing current requirement and increases design complexity. This is a useful trade-off for low voltage applications. However, it doesn't make sense to use such a design if the voltage supply requirement is already set by other circuits on the same chip. In such a circumstance, the ideal (lowest power) bandgap current reference would use minimal excess biasing current.

This paper presents a simple 2-terminal bandgap current reference that operates in a 2V

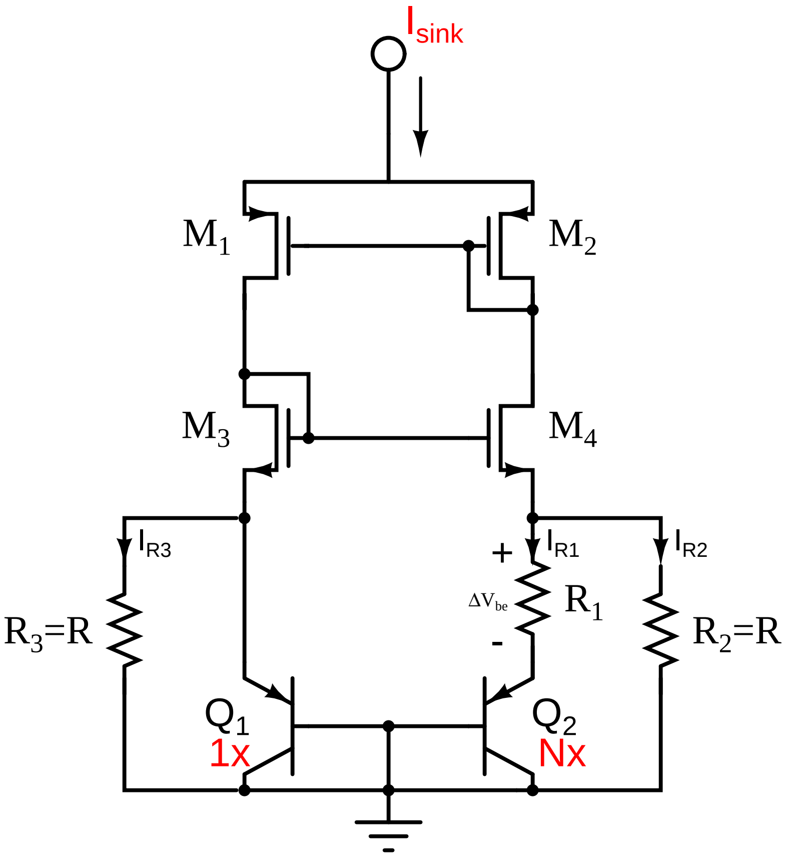

Figure 2: Proposed design. Q_2 is bigger than Q_1 by a factor N.

supply and requires no excess biasing current.

2 Topology

The basic design for our circuit is shown in Fig. 2. The saturation current of Q_2 is larger than that of Q_1 by a factor N (the emitter area ratio). Resistors R_2 and R_3 are the same size. Start-up circuitry is not shown.

Note that this is a two-terminal device that uses no op-amps in the design. No bias current is wasted because all transistors are in the path of the output current, I_{sink}.

Operation

A bandgap reference uses two well-characterized BJT quantities, base-emitter voltage, V_{BE} (-2mV/^{o}C) and thermal voltage, V_T (+0.086mV/^{o}C), to cancel temperature dependence.

In the proposed design, M_1 and M_2 act as a 1:1 current mirror, enforcing the condition that $I_{R3} + I_{C1} = I_{C2} + I_{R2}$. M_3 and M_4 have equal voltages at their source nodes. Thus the voltage across both R_2 and R_3 will be equal to V_{BE} of Q_1, and so $I_{R2} = I_{R3}$. Consequently, $I_{C1} = I_{C2}$.

The current through R_1 is a function of the difference between the base-emitter voltages of Q_1 and Q_2. Thus this current is ΔV_{BE} dependent, where

$$\begin{aligned}\Delta V_{BE} &= V_{BE1} - V_{BE2} \\ &= V_T \ln(I_{C1}/I_{S1}) - V_T \ln(I_{C2}/I_{S2}) \\ &= V_T \ln N \qquad (1)\end{aligned}$$

in which we have used the fact that $N = I_{S2}/I_{S1}$ and $I_{C1} = I_{C2}$. Therefore, given two bipolar transistors with a constant collector current ratio, any quantity that is proportional to ΔV_{BE} is also proportional to thermal voltage, V_T.

The current through the right side of the circuit is $I_{R2} + I_{R1}$. The total current sunk by the circuit is double this value (because of the current mirror) and is equal to

$$I_{sink} = 2\left(\frac{V_{BE1}}{R_2} + \frac{\Delta V_{BE}}{R_1}\right) \qquad (2)$$

Define K to be the resistor ratio needed to cancel out temperature coefficients[1] in Eq. 2

$$K = \frac{R_2}{R_1}$$

Thus total current is determined only by the value of resistor R_2

$$I_{sink} = \frac{2}{R_2}\left(V_{BE1} + K V_T \ln N\right)$$

---

[1] Resistor values R_1, R_2, and R_3 will likely have a temperature coefficient which must be taken into account.

$$= \frac{2}{R_2}\left[V_T \ln(I_{C1}/I_{S1}) + KV_T \ln N\right]$$

$$= \frac{2}{R_2}\left[V_T \ln\left(\frac{KV_T \ln N}{I_{S1}R_2}\right) + KV_T \ln N\right] \quad (3)$$

where we arrived at Eq. 3 by using $I_{C1} = I_{C2} = I_{R1} = \Delta V_{BE}/R_1 = K\Delta V_{BE}/R_2$.

It can be seen from Eq. 3 that, to a first approximation, none of the parameters depend on V_{DD} (i.e. the circuit is self-biasing) and that the output current can be set by solving Eq. 3 for the desired value.

Implementation of Resistor Ratio

For purposes of lab testing, resistor ratio K can be modified by bypassing sections of resistor R_1 using MOS switches M_5 - M_{12} (Fig. 3).

Startup Condition

As is typical for self-biased circuits [1, p.326], this topology has two stable states of operation - the desired state and a zero-current state. The node voltages that make the zero-current state possible are shown in Fig. 4.

Startup circuitry was not included on-chip to minimize complications from extra components. Because every major node of the circuit was connected to a pin, any necessary startup circuitry could be connected externally.

Stability Analysis

Because self-biasing circuits rely on feedback, care must be taken not to create an unstable loop.

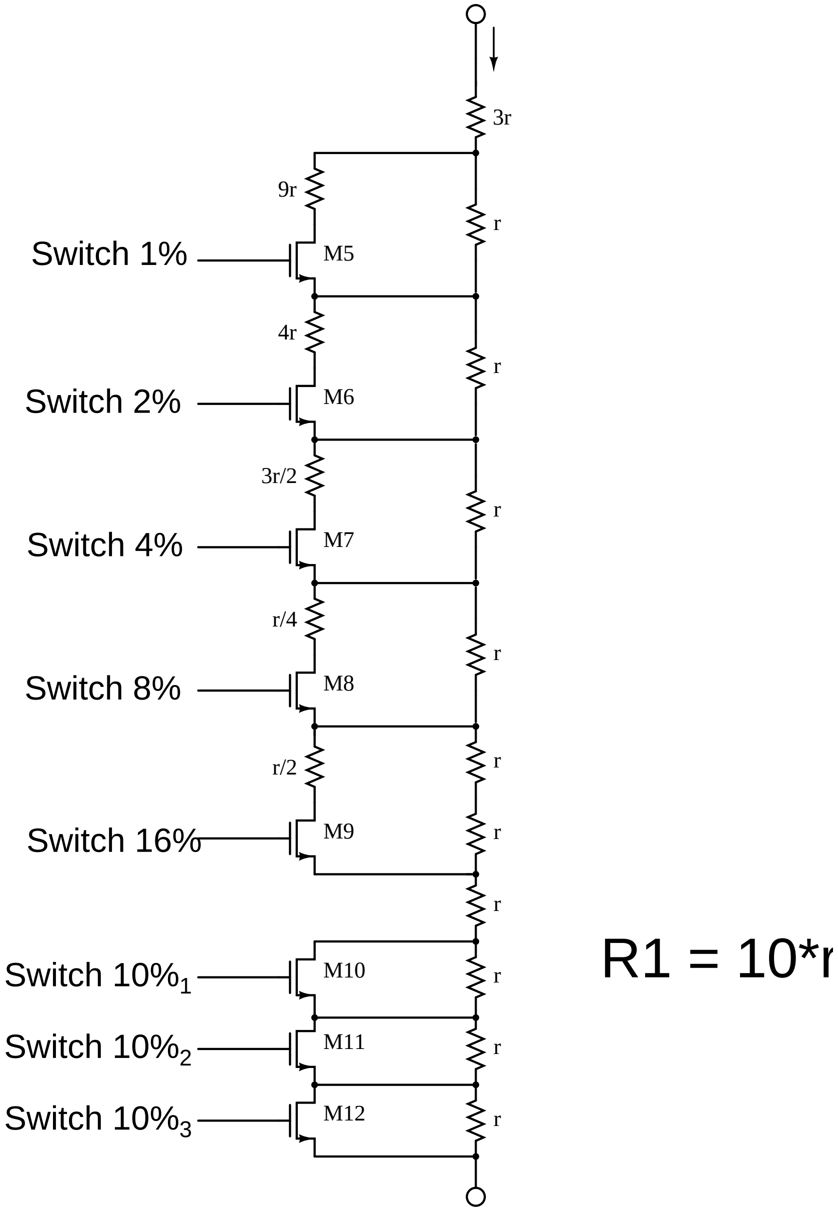

Figure 3: Sub-circuitry used to vary R_1, and therefore resistor ratio K.

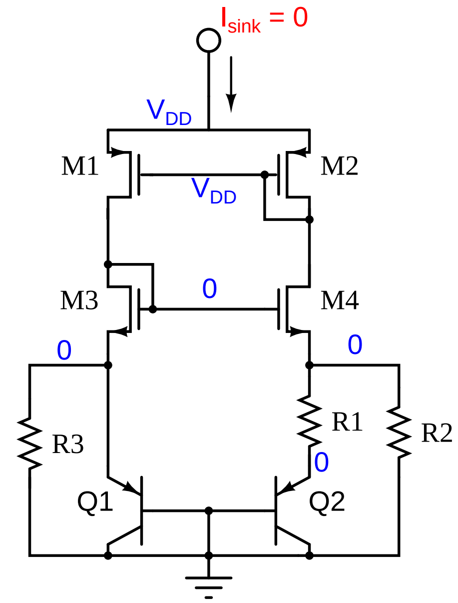

Figure 4: Node voltages for zero-current state.

Suppose a positive disturbance is introduced at the gate of M_4. This disturbance increases V_{GS4}, which increases I_{D4}. The increase in I_{D4} is mirrored through M_1/M_2, increasing the gate voltage of diode-connected M_3. However, the gate of M_3 is shorted to the gate of M_4, and so a positive feedback loop is created. For this feedback loop to be stable,

$$\left|\frac{\Delta V_{G3}}{\Delta V_{G4}}\right| < 1$$

Consider the circuit shown in Fig. 5, which is a modified form of Fig. 2. Because of current mirror M_1/M_2

$$\begin{aligned} I_{C1} = I_{C_2} \Longrightarrow g_{mQ1} &= g_{mQ2} = g_m \quad (BJT) \\ g_{m1} &= g_{m2} \quad (MOS) \\ g_{m3} &= g_{m4} \quad (MOS) \end{aligned}$$

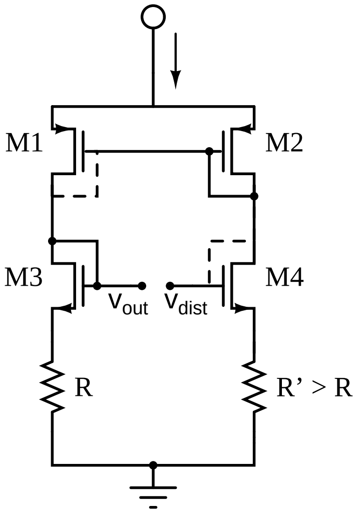

Figure 5: Feedback stability analysis. Dotted lines indicate alternate unstable configuration.

Comparing Fig. 5 with the original Fig. 2, it is clear that

$$\begin{aligned} R &= R_3 || g_m^{-1} \\ R' &= R_2 || (g_m^{-1} + R_1) \end{aligned}$$

But $R_2 = R_3$, therefore $R' > R$.

Let M_2 and M_4 be diode connected as shown. If a disturbance V_{dist} is applied to the gate of M_4 (effectively a common-source amplifier with source degeneration R') then the output voltage generated will be

$$V_{out} = I_{D1}\left(g_{m3}^{-1} + R\right) = g_{m4} V_{dist} \frac{1}{1 + g_{m4} R'} \left(g_{m3}^{-1} + R\right)$$

and so we meet our stability condition

$$\left| \frac{\Delta V_{G3}}{\Delta V_{G4}} \right| = \frac{V_{out}}{V_{dist}} = \frac{1 + g_{m4} R}{1 + g_{m4} R'} < 1$$

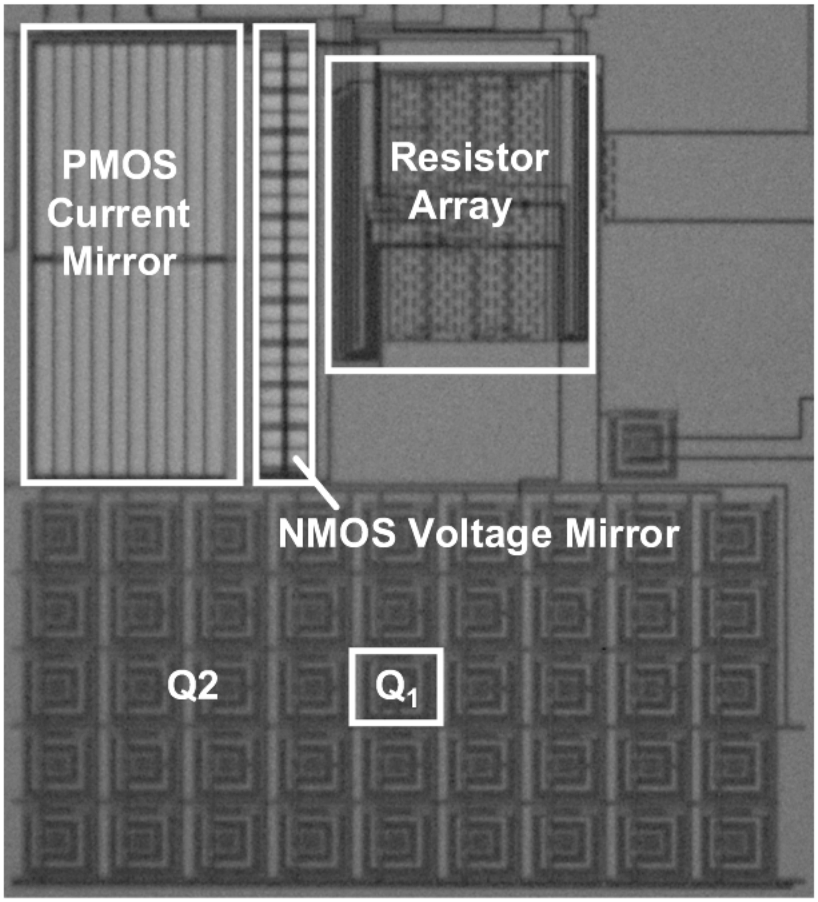

Figure 6: Complete layout.

3 Measurement Results

The two-terminal current reference was fabricated in a standard 0.35μm CMOS process. A die photo is shown in Fig. 6.

Results from a sweep of applied supply voltage are shown in Fig. 7. The chip had an operating voltage of about 2V, at which point it exhibited an average output resistance of 350kΩ. It can be seen that the positive feedback loop causes hysteresis, resulting in a turn-off voltage of about 1.6V.

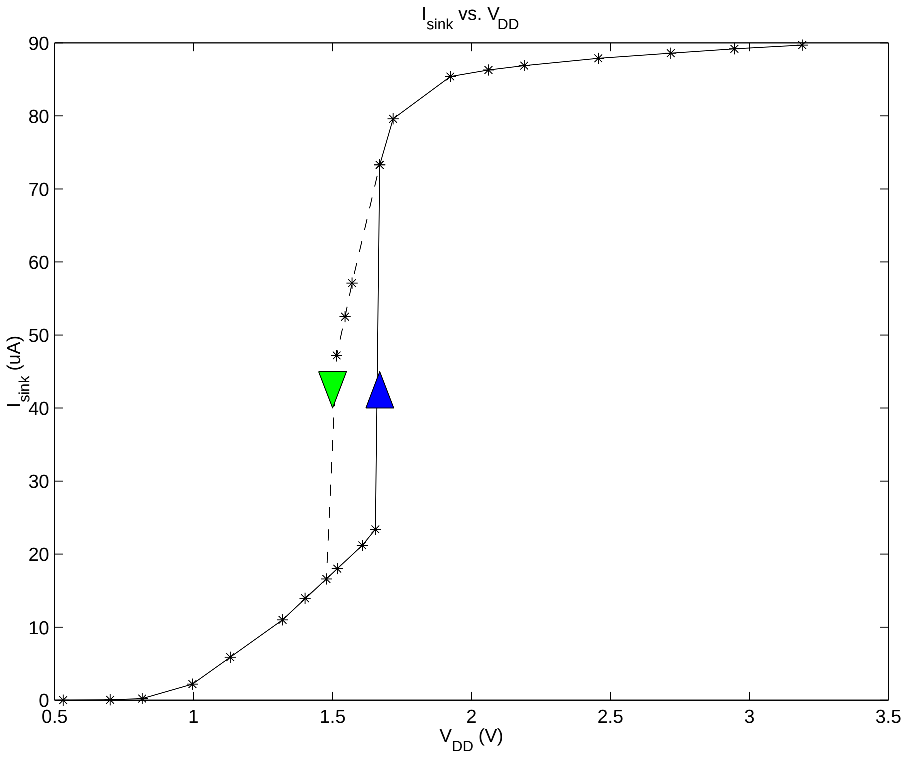

Figure 7: Chip 2 - I_{sink} vs. V_{DD}.

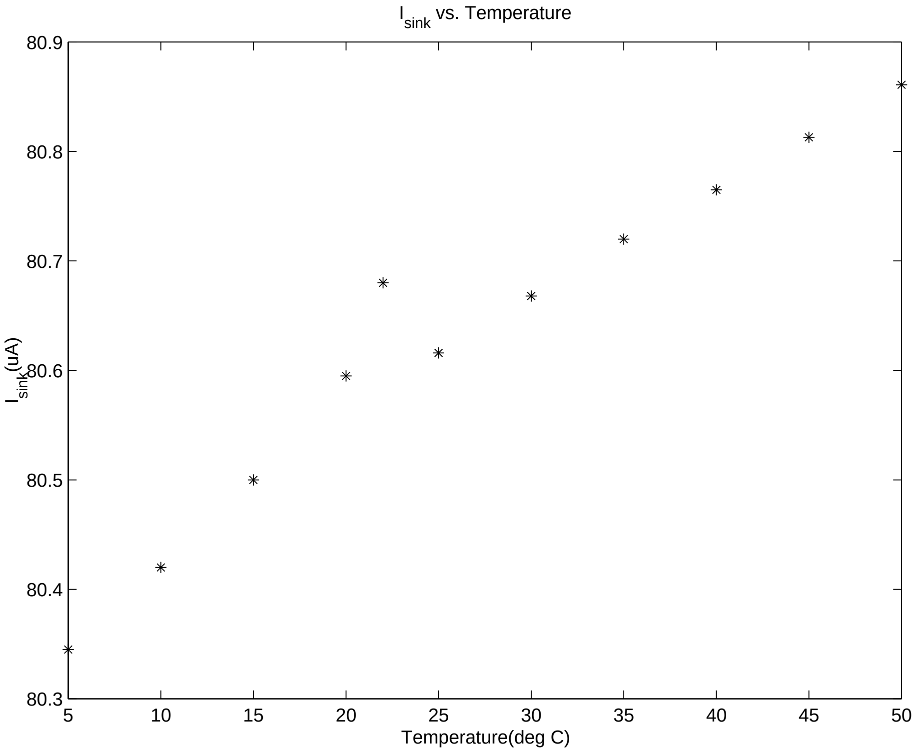

Figure 8: Chip 6 - Temperature sensitivity = 142 ppm/deg C

Fig. 8 shows measured output current as a function of temperature. The average temperature coefficient of the output current was 142 ppm/^{o}C. Lower temperature coefficient could not be achieved because the optimum resistor ratio K was outside the adjustability[2] of R_1. Future redesign with a corrected value of R_1 should result in a much lower temperature coefficient.

---

[2] Minimum implemented K = 9.4. Using data from test measurements, desired K $\simeq$ 8.

A summary of results appears in Table 1.

Table 1: Summary of results for bandgap current reference

Technology	0.35μm CMOS
Area	0.24 mm^2
Output Current (I_{sink})	80μA
Operating Voltage (Von)	2V
Temperature Coefficient (TC_F)	142 ppm/^{o}C
Tested Temperature Range	5^{o}C - 50^{o}C
Output Impedance (R_{out})	350 kΩ

4 Conclusion

This paper demonstrates a two-terminal six-transistor bandgap current reference fabricated in a standard 0.35μm CMOS process. The circuit generates a temperature and power-supply insensitive current without the need for excess biasing current.

References

[1] Paul R. Gray and Robert G. Meyer. *Analysis and Design of Analog Integrated Ciruits.* Wiley, 1993.

[2] H. Banba, H. Shiga, A. Umezawa, T. Miyaba, T. Tanzawa, S. Atsumi, and K. Sakui. A CMOS Bandgap Reference Circuit With Sub-1-V Operation. *IEEE Journal of Solid-State Circuits*, 34(5):670–674, May 1999.

[3] Dean A. Badillo. 1.5V CMOS Current Reference With Extended Temperature Operating Range. *IEEE International Symposium on Circuits and Systems*, 3(III):197–200, 2002.

[4] Andrea Boni. Op-Amps and Startup Circuits for CMOS Bandgap References With Near 1-V Supply. *IEEE Journal of Solid-State Circuits*, 37(10):1339–1343, October 2002.