ECEN474: (Analog) VLSI Circuit Design Fall 2010

Lecture 17: Folded Cascode OTA

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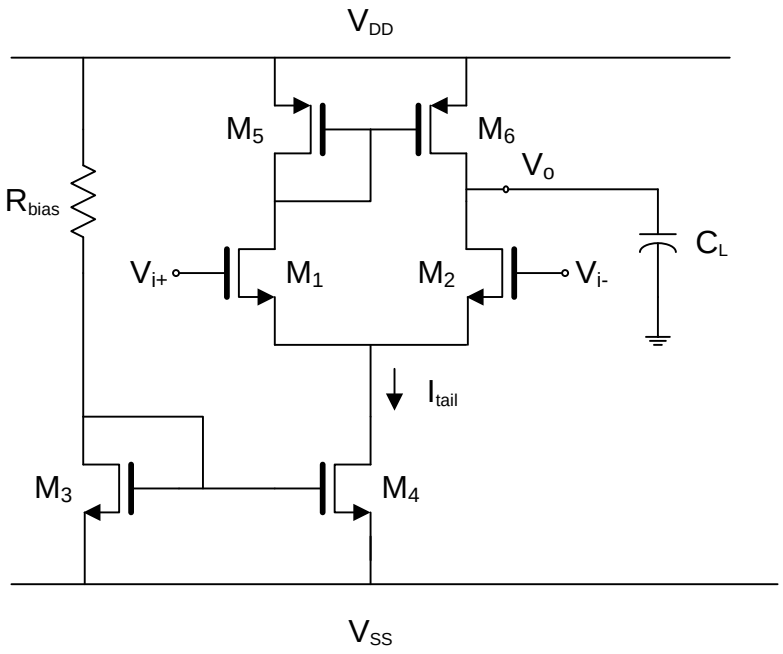
Announcements

- HW4 Due Friday 10/22
- Exam 2 Wednesday Nov 3 9:10-10:10AM

Agenda

- Single-Stage Cascode OTA
- Folded Cascode OTA

Simple OTA

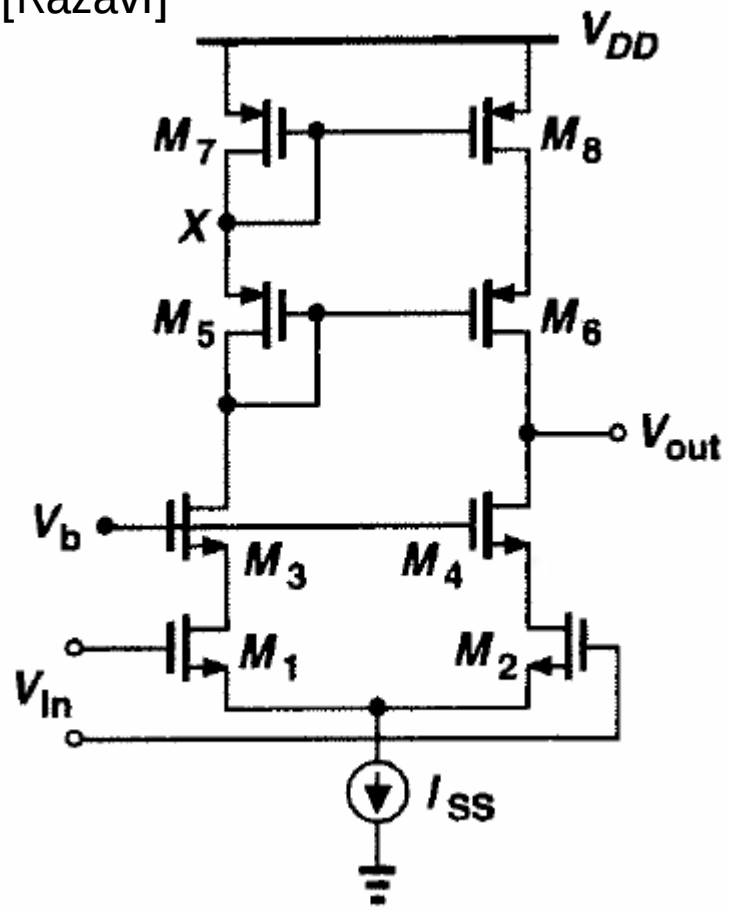


DC Gain $A_v = G_m R_{out} = g_{m1}\left(r_{o2} \parallel r_{o6}\right)$

- Gain is limited by single-transistor output resistance

Single-Stage Cascode OTA

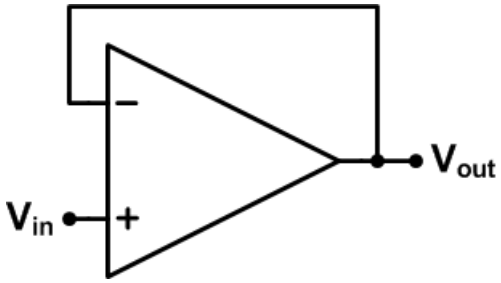
[Razavi]



DC Gain $A_v = G_m R_{out} \approx g_{m1}\left(g_{m4} r_{o2} r_{o4} \parallel g_{m6} r_{o8} r_{o6}\right)$

- Gain is larger by a $g_m r_o$ factor
- Output swing range is limited due to large compliance voltage of cascode current source load

Single-Stage Cascode OTA
Unity Gain Feedback Voltage Range



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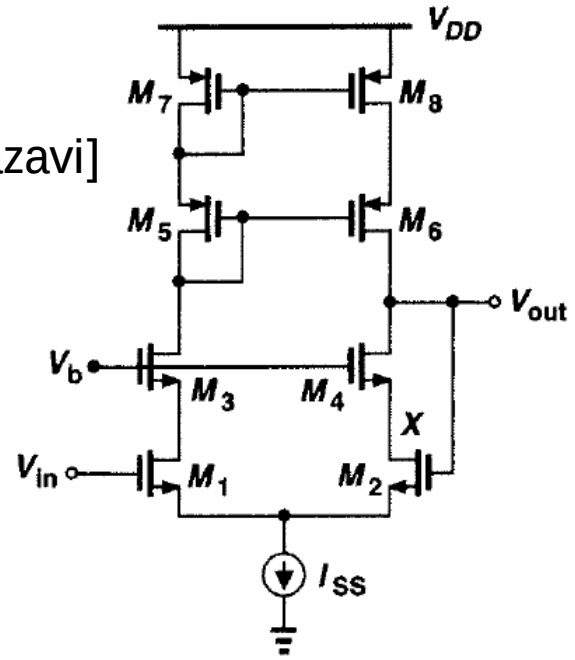


Maximum V_{out} set by M2 saturation

$$V_{out} \le V_x + V_{TH2}$$

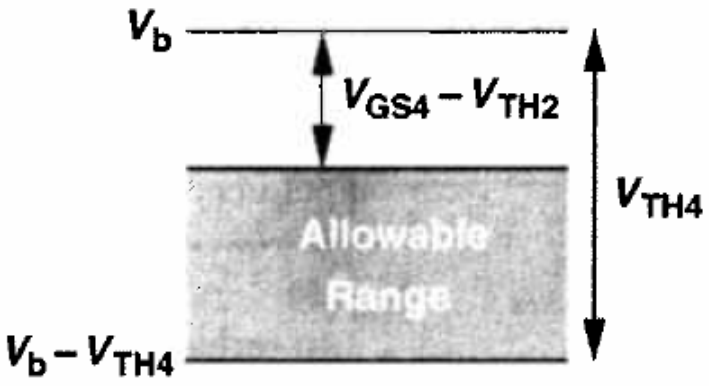
Minimum V_{out} set by M4 saturation

$$V_{out} \ge V_b - V_{TH4}$$

As $V_b = V_x + V_{GS4}$ and plugging V_x into M2 sat condition

Output (& Input) Range $= V_{TH4} - (V_{GS4} - V_{TH2})$

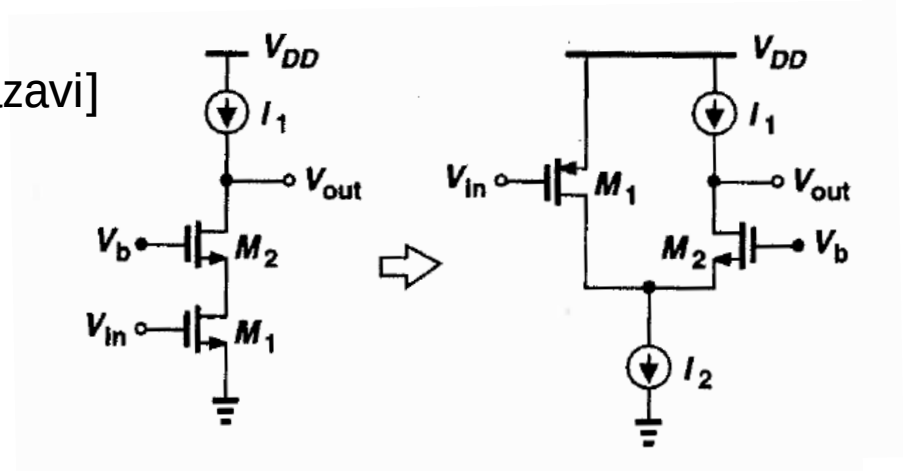
Less than a V_{TH} !!!



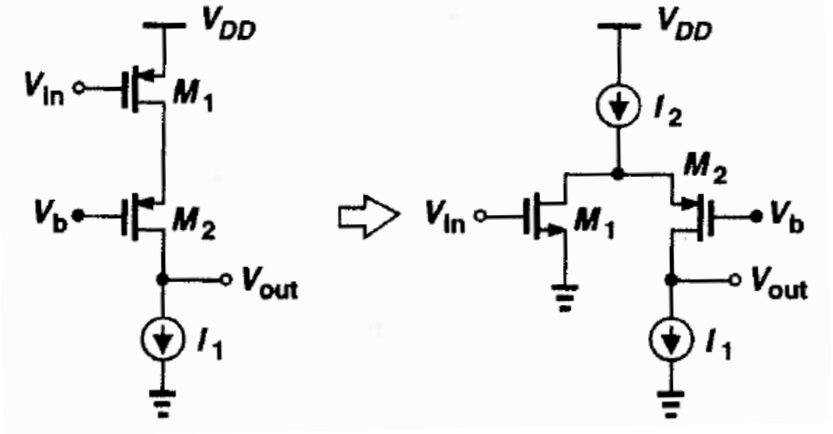
- Cascode configuration constrains output & unity-gain swing

Folded Cascode Circuits

[Razavi]



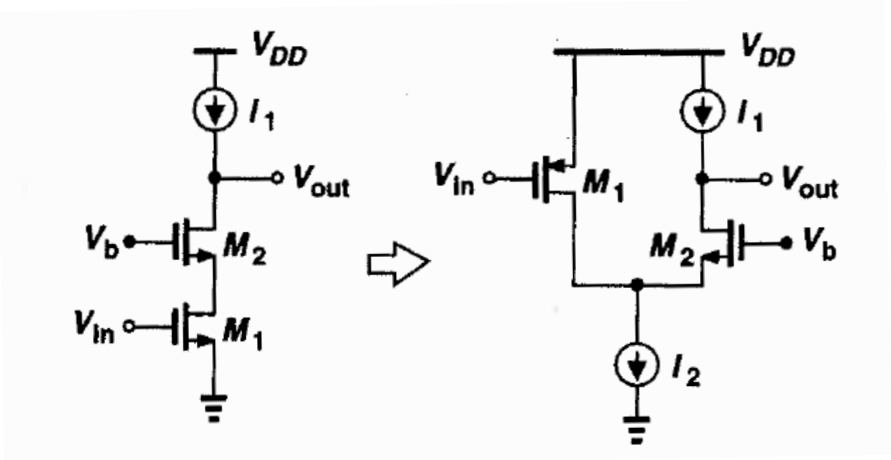
PMOS Input & NMOS Cascode



NMOS Input & PMOS Cascode

- "Folding" about the cascode node will increase input and output swing range

Folded Cascode OTA



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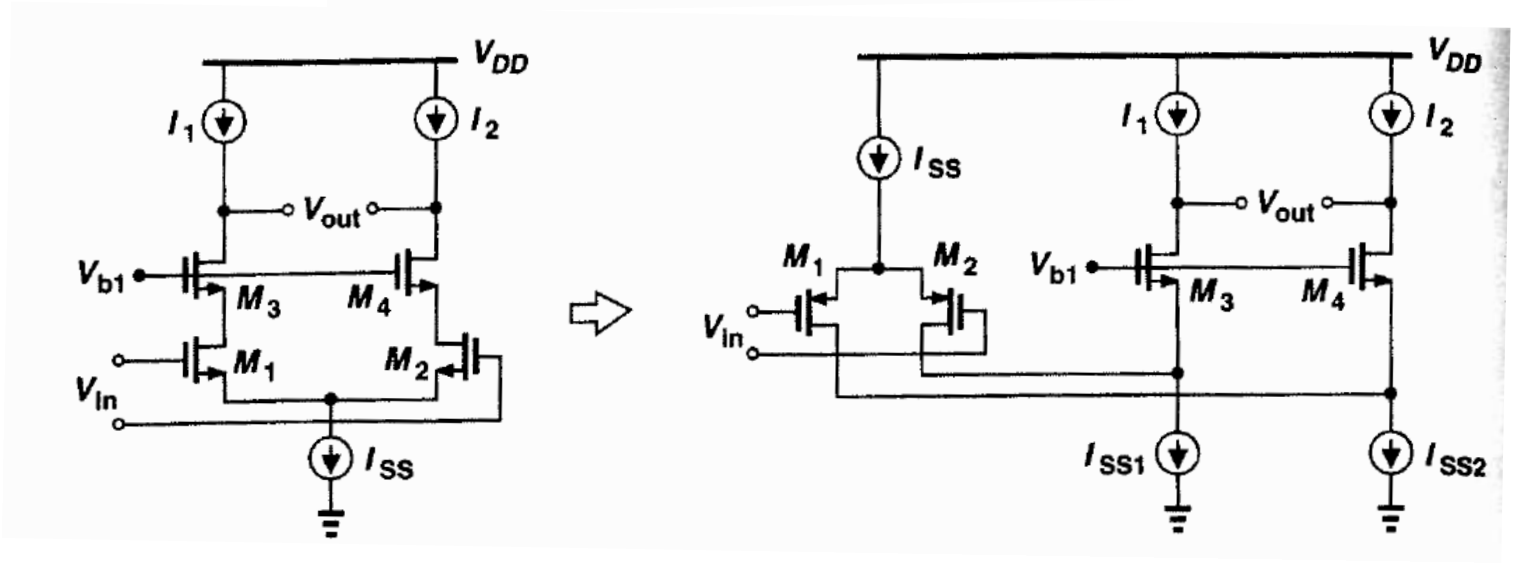
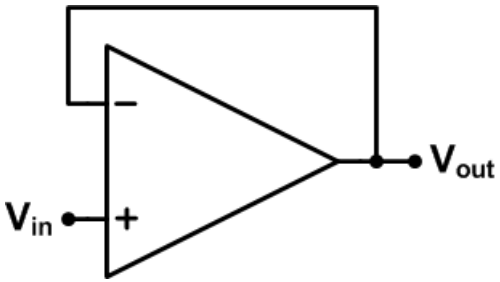
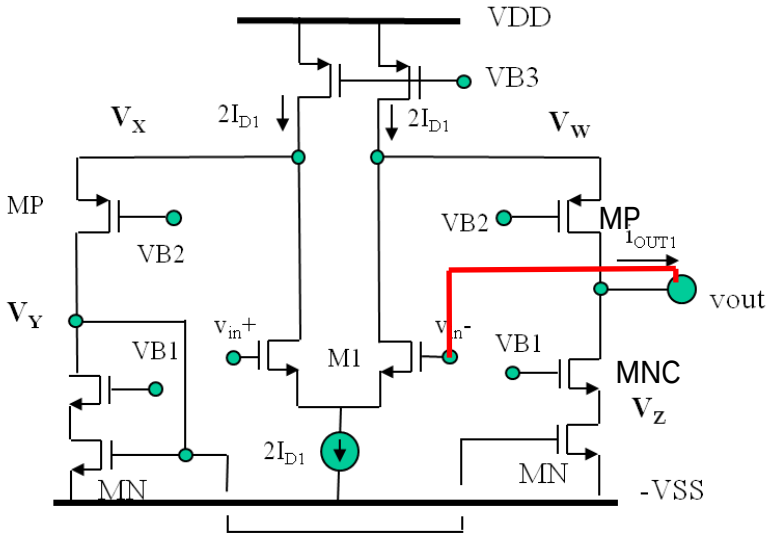


Folded Cascode OTA
Unity Gain Feedback Voltage Range





Maximum V_{out} set by *MP* saturation

$$V_{out} \le V_{b2} + |V_{THP}|$$

Minimum V_{out} set by output NMOS cascode or tail current source saturation

$$V_{out} \ge V_{DSATNC} + V_{DSATN} \quad \textbf{OR} \quad V_{out} \ge V_{DSATI_{Tail}} + V_{GS1}$$

- With proper (high-value) choice of Vb2, a decent output and input swing range can be achieved

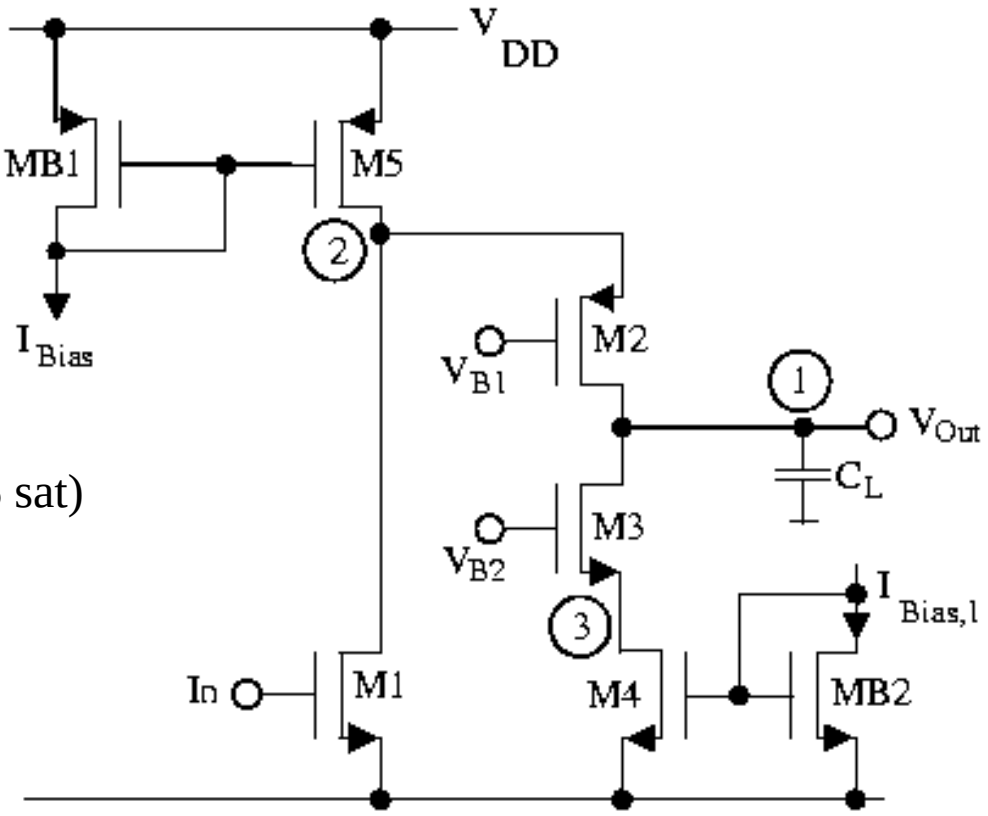
Folded-Cascode OTA: gm, rout and poles?

V_{B1} and V_{B2} must keep M_1

- M_5 in saturation region

$V_{B2} > V_{sat,4} + V_{GS3}$ (for M4 sat)

$V_{B1} < V_{DD} - V_{sat,5} - V_{SG2}$ (for M5 sat)

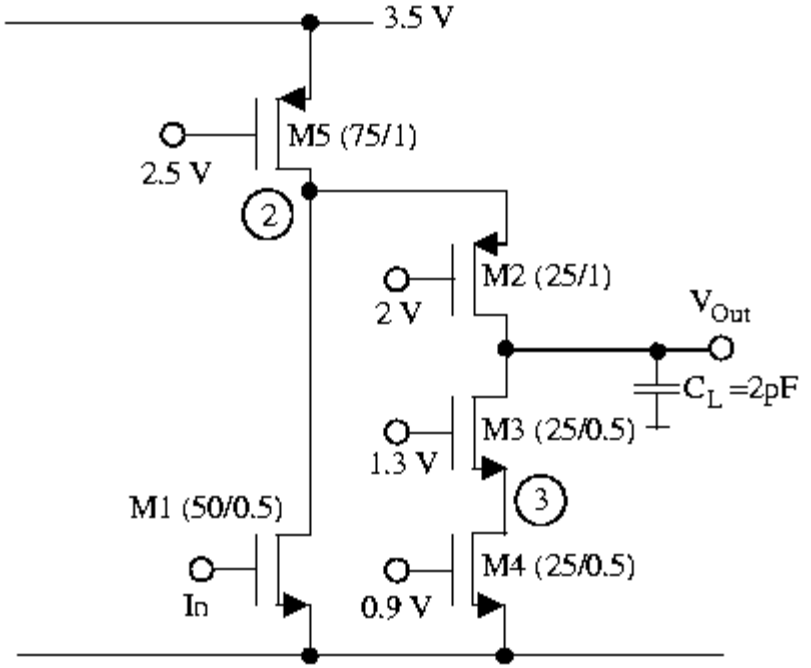


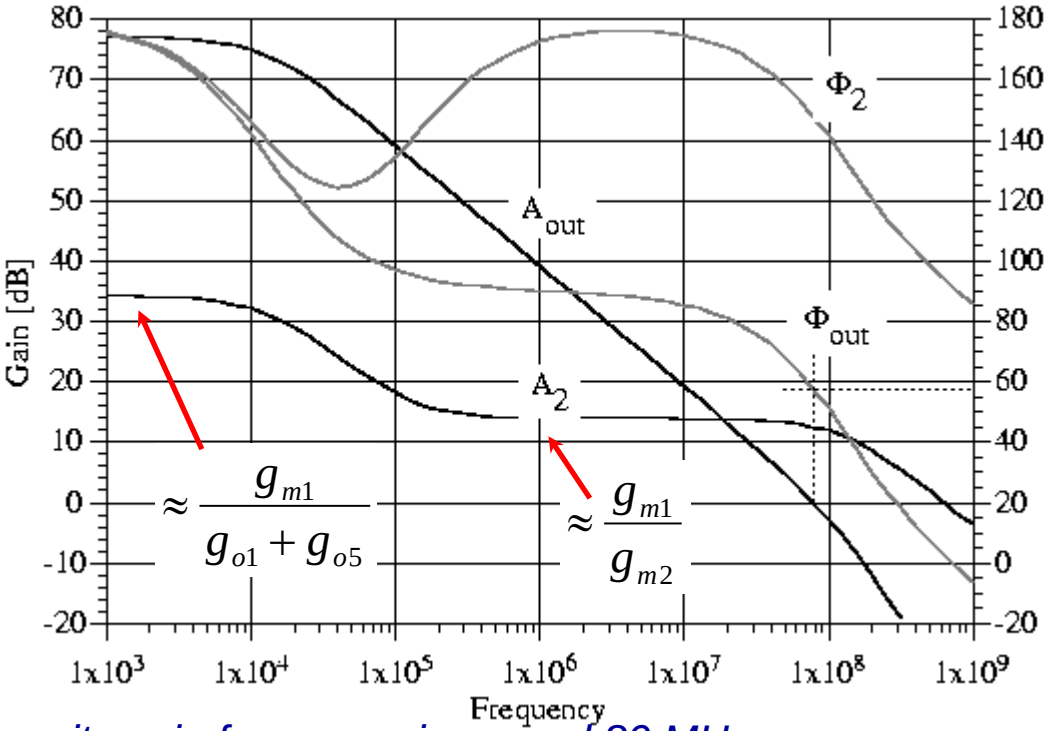
Notice that ID5 biases both M2 and M1

$$G_m = g_{m1} \;\; ; \qquad r_{out} \cong \left(r_{ds2} g_{m2} \left(r_{ds1} \| r_{ds5}\right)\right) \| \left(r_{ds3} g_{m3} r_{ds4}\right)$$

Example: Folded-Cascode OPAMP

Find the gain and the phase from input to output and from input to node 2.



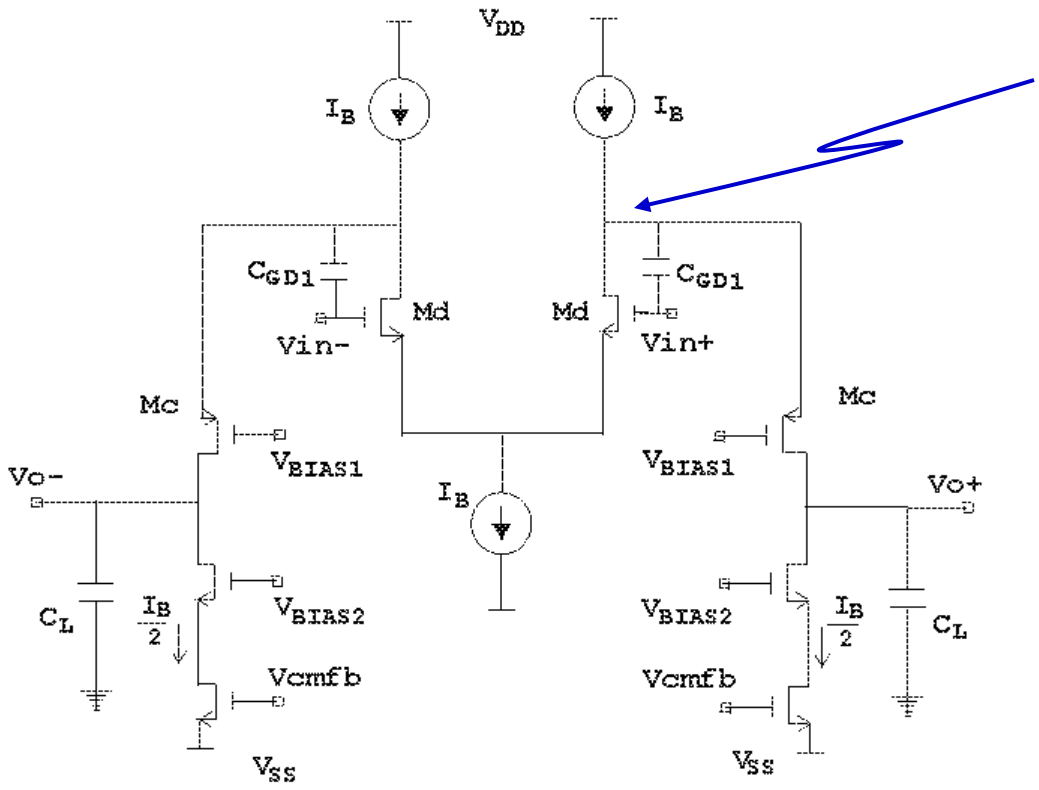


The low frequency gain is 77 dB and the unity gain frequency is around 80 MHz.

The behavior of the gain from the input to node 2 is interesting: above the dominant pole.

$$\omega_{z2} \approx \left(\frac{g_{m2}}{g_{o1}+g_{o5}}\right)\left(\frac{1}{r_{out}C_L}\right)$$

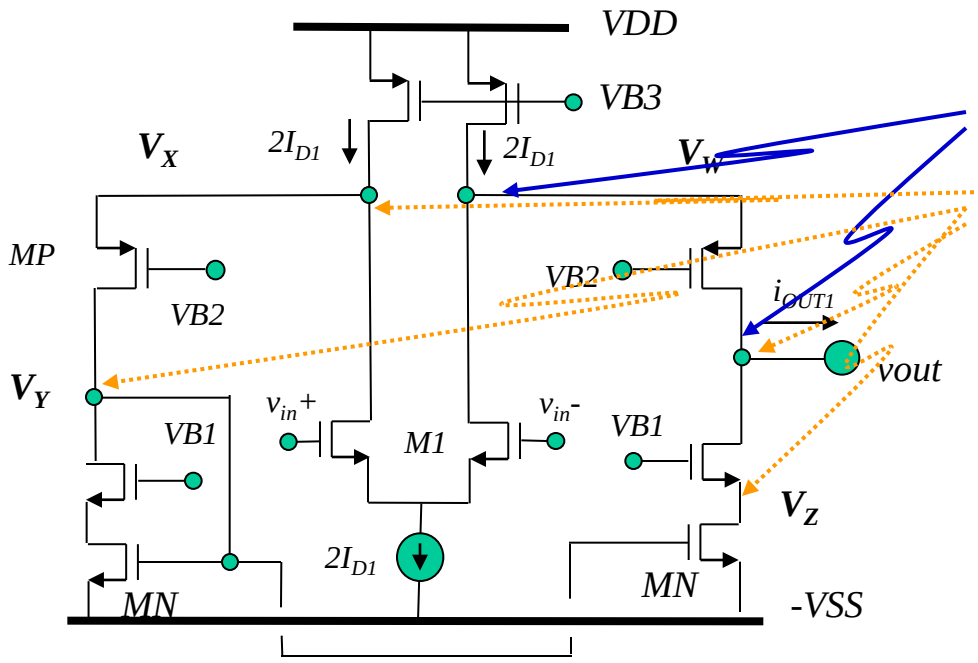
TYPICAL FOLDED CASCODE (One of the most popular circuit in ADCs)



- There is a limitation due the non- dominant pole
- $I_{BIAS} \uparrow \Rightarrow A_{DC} \downarrow$
- $W_{casc} \downarrow \Rightarrow V_{DSAT} \uparrow$

$$\frac{v_o}{v_{in}} = -\frac{g_{md}}{g_o}\frac{1}{\left(1+s\frac{C_p}{g_{mc}}\right)\left(1+s\frac{C_L}{g_o}\right)}$$

FOLDED-CASCODE OTA



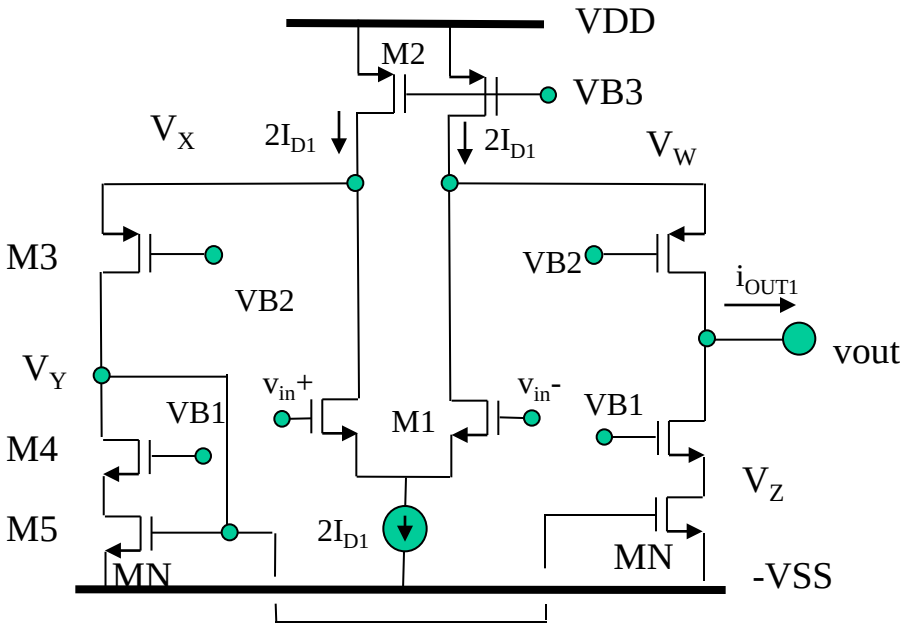
Frequency response:

Righ hand side

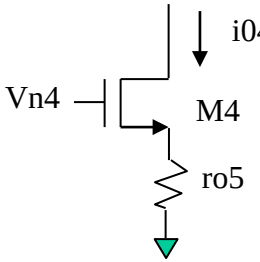
- Righ hand side: 2 poles (at V_W and Vout)
- Left hand side: 4 poles !!! (at V_X, V_Y, V_Z and Vout)

✓**The poles at Vy and Vz are associated to N-type transistors → higher frequencies**

$$A_V(s) \cong g_{m1} R_{out} * \frac{1}{1+\frac{sC_{out}}{g_{out}}} * \frac{1}{1+\frac{sC_{PC}}{g_{mp}}}$$



For cascode transistors



$$i_{04}=\frac{g_{m4}}{1+g_{m4}r_{05}}v_{n4}\cong\frac{v_{n4}}{r_{05}}$$

Remember $i_{eq}^2=\frac{8}{3}kTg_m$

Output referred noise

- M1 produces an output current given by

$$i_{01}=g_{m1}v_{n1}$$

- Each transistor M2 generates a differential output current

$$i_{02}=g_{m2}v_{n2}$$

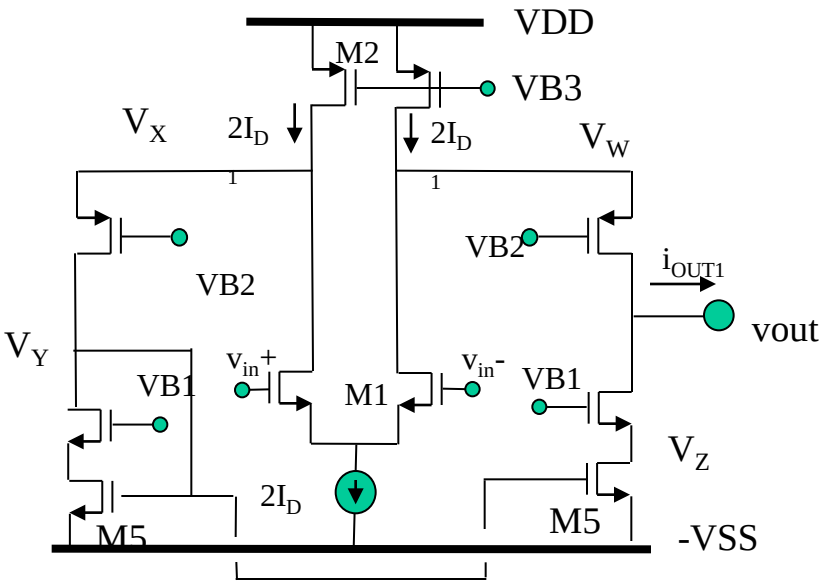
- Similarly, for each transistor M5

$$i_{05}=g_{m5}v_{n5}$$

- At low and medium frequencies, noise contribution of the cascode transistors can be neglected (M3 and M4)

$$\mathbf{i_{out}^2 = 2(i_{eq1}^2 + i_{eq2}^2 + i_{eqn}^2)}$$

FOLDED-CASCODE OTA



Noise density and noise level

⇨The output referred current spectral density is

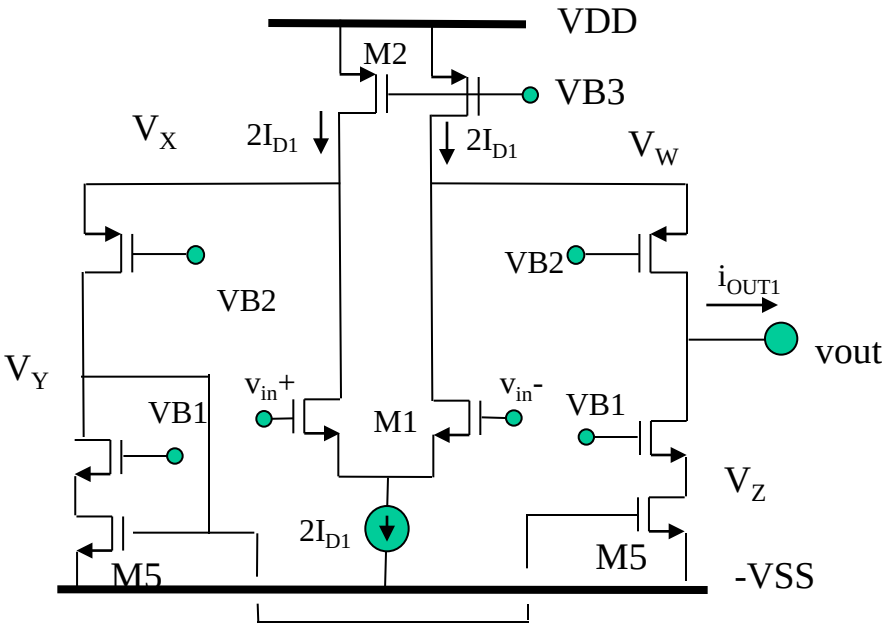
$$i_{0T}^2 = 2\left(g_{m1}^2 v_{n1}^2 + g_{m2}^2 v_{n2}^2 + g_{m5}^2 v_{n5}^2\right)$$

⇨And the input referred noise density becomes

$$v_{eq,in}^2 = 2\frac{g_{m1}^2 v_{n1}^2 + g_{m2}^2 v_{n2}^2 + g_{m5}^2 v_{n5}^2}{g_{m1}^2}$$

⇨**The noise level is**

$$v_{noise} = \sqrt{\int_{BW} v_{eq,in}^2 df} = \sqrt{\int_{BW} 2\left(v_{n1}^2 + \frac{g_{m2}^2 v_{n2}^2}{g_{m1}^2} + \frac{g_{m5}^2 v_{n5}^2}{g_{m1}^2}\right) df}$$



Noise level for the folded-cascode OTA

$$v_{noise} = \sqrt{\int_{BW} 2\left(v_{n1}^2 + \frac{g_{m2}^2 v_{n2}^2}{g_{m1}^2} + \frac{g_{m5}^2 v_{n5}^2}{g_{m1}^2} \right) df}$$

☞**Lets consider thermal noise ($vn^2 = (8/3)KT/(gm)$)**

$$v_{noise} = \sqrt{\int_{BW} \frac{16}{3} kT \left(\frac{1}{g_{m1}} + \frac{g_{m2}}{g_{m1}^2} + \frac{g_{m5}}{g_{m1}^2} \right) df}$$

Or for a dominant (single) pole system with NBW = (π/2)BW

$$v_{noise} \approx \left(\sqrt{\frac{8kT}{g_{m1}}(BW)} \right) \left(\sqrt{1 + \frac{g_{m2}}{g_{m1}} + \frac{g_{m5}}{g_{m1}}} \right)$$

Noise of diff pair **Noise Factor (due to other transistors)**

☞**Low-noise is associated with large gm1 and relatively small gm2 and gm5**

Next Time

- Two Stage Miller OTA