MOSFET DIFFERENTIAL AMPLIFIERS

(READING: Text-Sec. 4.3.5)

INTRODUCTION

Objective

The objective of this presentation is:

1.) Introduce and characterize the amplifiers using active loads

2.) Show how analyze these amplifiers

Outline

- MOS current mirror load differential amplifier
- Summary

MOS DIFFERENTIAL AMPLIFIER WITH A CURRENT MIRROR LOAD

Voltage Transfer Characteristic

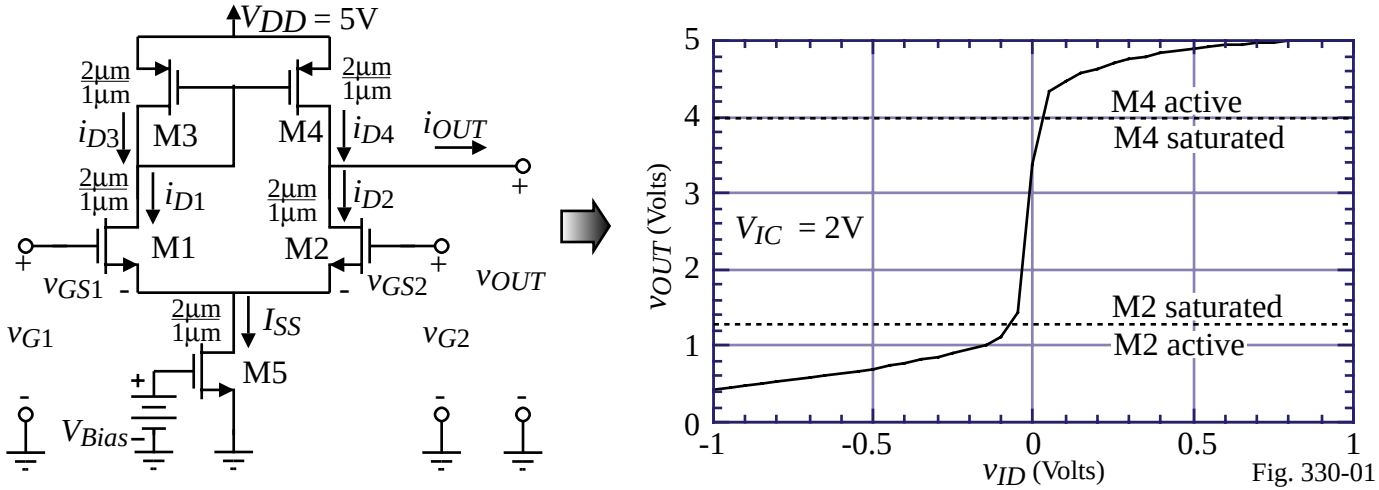

Fig. 330-01

Note: The output signal to ground is equivalent to the differential output signal

→ $V_{o1} - V_{o2} = (i_{D1} - i_{D2})(r_{ds2}//r_{ds4})$ → $v_o/v_{id} = (0.5g_{m1} - [-0.5g_{m2}])\ (r_{ds2}//r_{ds4})$

- Load current mirror transforms the double-ended differential signal into a single-ended signal.

Regions of operation of the transistors:

M2 is saturated when,

$$v_{DS2} \geq v_{GS2} - V_{TN} \rightarrow v_{OUT} - V_{S1} \geq V_{IC} - V_{S1} - V_{TN} \rightarrow v_{OUT} \geq V_{IC} - V_{TN}$$

where we have assumed that the region of transition for M2 is close to $v_{ID} = 0\text{V}$.

M4 is saturated when,

$$v_{SD4} \geq v_{SG4} - |V_{TP}| \rightarrow V_{DD} - v_{OUT} \geq V_{SG4} - |V_{TP}| \rightarrow v_{OUT} \leq V_{DD} - V_{SG4} + |V_{TP}|$$

Input Common-Mode Range (ICMR)

ICMR is found by setting $v_{ID} = 0$ and varying v_{IC} until one of the transistors leaves the saturation region.

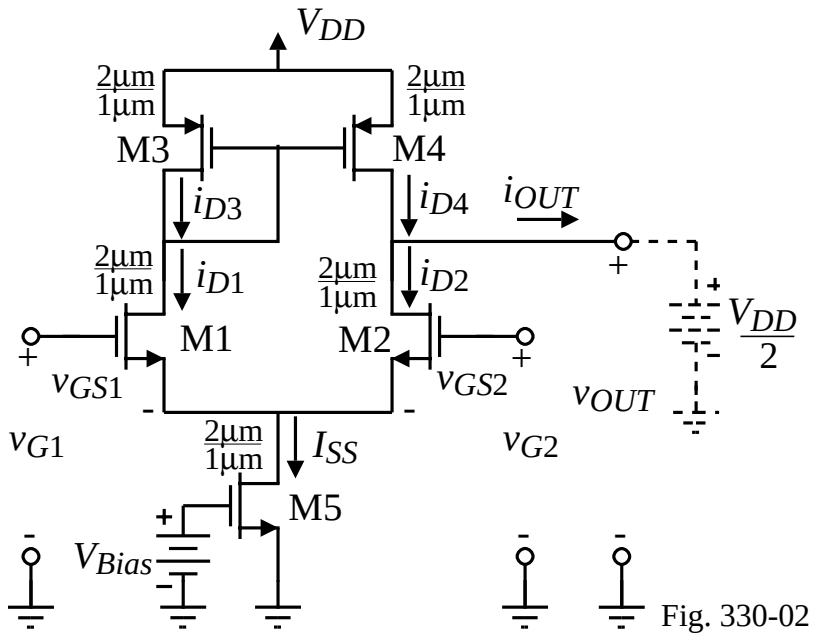

Fig. 330-02

Highest Common-Mode Voltage

Path 1: from G1 through M1 and M3 to V_{DD}:

$$V_{IC}(\max) = V_{G1}(\max) = V_{G2}(\max)$$

$$= V_{DD} - V_{SG3} - V_{DS1}(\text{sat}) + V_{GS1}$$

$$= V_{DD} - V_{SG3} + V_{TN1}$$

Path 2: from G2 through M2 and M4 to V_{DD}:

$$V_{IC}(\max)' = V_{DD} - V_{SD4}(\text{sat}) - V_{DS2}(\text{sat}) + V_{GS2}$$

$$= V_{DD} - V_{SD4}(\text{sat}) + V_{TN2} \qquad \therefore \quad \boxed{V_{IC}(\max) = V_{DD} - V_{SG3} + V_{TN1}}$$

Lowest Common-Mode Voltage (Assume a V_{SS} for generality)

$$\boxed{V_{IC}(\min) = V_{SS} + V_{DS5}(\text{sat}) + V_{GS1} = V_{SS} + V_{DS5}(\text{sat}) + V_{GS2}}$$

where we have assumed $V_{GS1} = V_{GS2}$ throughout the input common-mode voltages.

Example 1 - Calculation of the Worst-Case Input Common-Mode Range of the n-Channel Input, Differential Amplifier

Assume V_{DD} varies from 4 to 6 volts and V_{SS} = 0, and K' varies from 45 to 100 μA/V^2, V_{TP} from 0.7 to 1 V, and V_{TN} from 0.6 to 0.8 V to calculate the input common-mode range of an n-channel input differential amplifier with a PMOS current-mirror load. Assume I_{SS} is 100 μA, $W_1/L_1 = W_2/L_2 = 5$, $W_3/L_3 = W_4/L_4 = 1$, and V_{DS5}(sat) = 0.2 V. Include worst-case variation in K' and V_T in calculations.

Solution

Smallest V_{IC_max}: Smallest V_{DD}, largest V_{SG4}, smallest K', smallest V_{TN},

$$V_{IC}(\max) = 4 - \left(\sqrt{\frac{2 \cdot 50\,\mu A}{45\,\mu A/V^2 \cdot 1}} + 1 \right) + 0.6 = 4 - 2.49 + 0.6 = 2.01 \text{ volts}$$

Highest V_{IC_min}: largest V_{gs2}, smallest K', largest V_{TN},

$$V_{IC}(\min) = V_{SS} + 0.2 + \left(\sqrt{\frac{2 \cdot 50\,\mu A}{45\,\mu A/V^2 \cdot 5}} + 0.8 \right) = 0.2 + 1.47 = 1.67 \text{ volts},$$

which gives a worst-case input common-mode range of 0.34-V with a 5-V power supply.

Reducing V_{DD} by 340mV more will result in a worst-case common-mode range of zero. We have assumed in this example that all bulk-source voltages are zero.

Small-Signal Analysis of the Differential-Mode of the Differential Amplifier

A requirement for differential-mode operation is that the differential amplifier is balanced†.

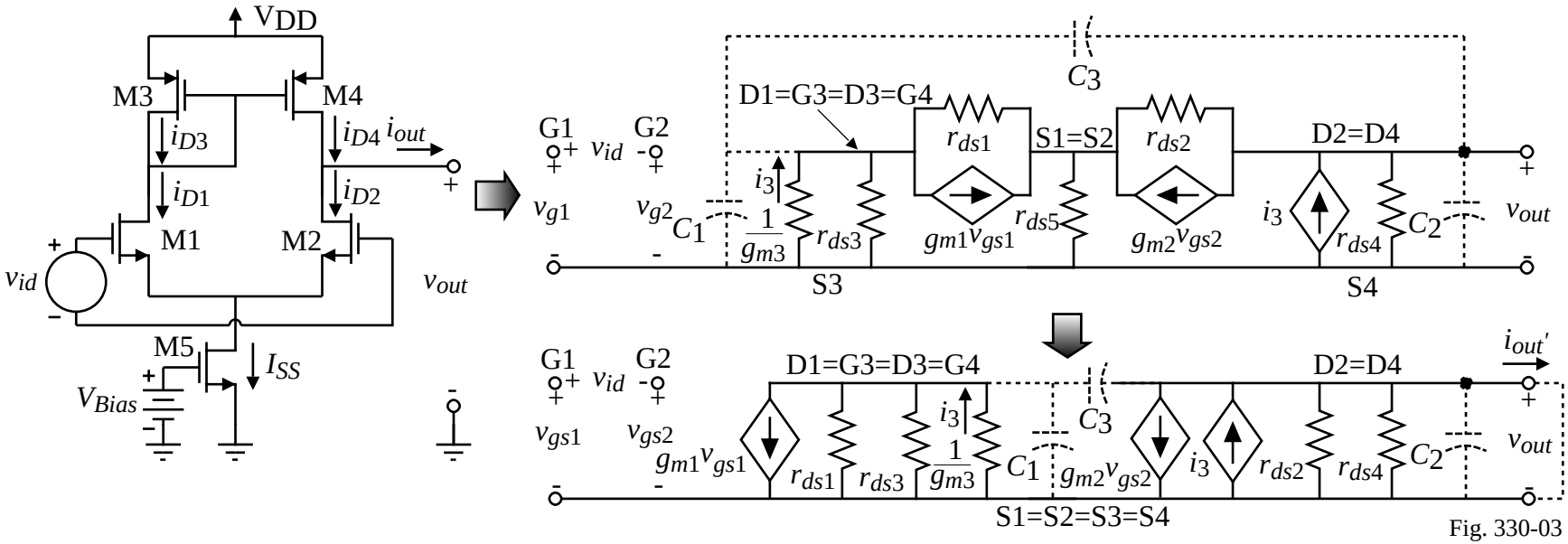

Fig. 330-03

Differential Transconductance: Assume the output of the diff. amplifier is an ac short.

$$i_{out}' = v_{gs1}g_{m1}(r_{ds1}//r_{ds3}//[1/g_{m3}])g_{m4} - v_{gs2}g_{m2} \approx v_{gs1}g_{m1}(1/g_{m3})g_{m4} - v_{gs2}g_{m2}$$

$$\approx v_{gs1}g_{m1} - v_{gs2}g_{m2} = g_{md}v_{id}$$

where $g_{m1} = g_{m2} = g_{md}$ and i_{out}' designates the output current into a short circuit.

† It can be shown that the current mirror causes this requirement to be invalid because the drain loads are not matched. However, we will continue to use the assumption, regardless.

Small-Signal Analysis of the Differential-Mode of the Differential Amplifier - Continued

Output Resistance:

$$r_{out} = \frac{1}{g_{ds2} + g_{ds4}} = r_{ds2} \| r_{ds4}$$

Differential Voltage Gain:

$$A_v = \frac{v_{out}}{v_{id}} = \frac{g_{md}}{g_{ds2} + g_{ds4}}$$

If we assume all transistors are in saturation and replace the small signal parameters of g_m and r_{ds} in terms of their large-signal model equivalents,

$$A_v = \frac{v_{out}}{v_{id}} = \frac{(K'_1 I_{SS} W_1/L_1)^{1/2}}{(\lambda_2 + \lambda_4)(I_{SS}/2)} = \frac{2}{\lambda_2 + \lambda_4}\left(\frac{K'_1 W_1}{I_{SS} L_1}\right)1/2$$

$$\propto \frac{1}{\sqrt{I_{SS}}}$$

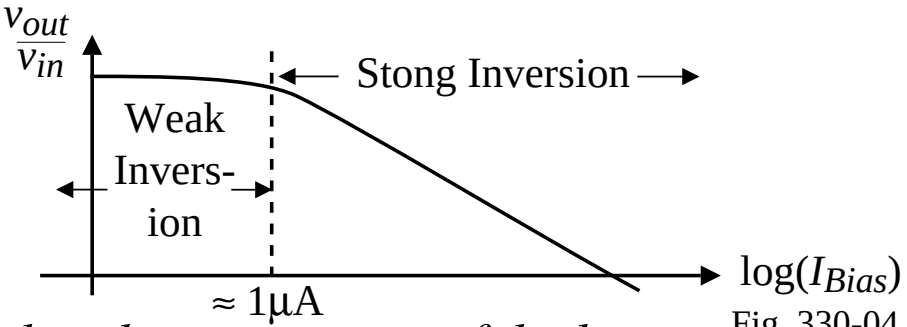

Fig. 330-04

Note the small-signal gain is inversely proportional to the square root of the bias current!

Example: If W_1/L_1 = 2μm/1μm and I_{SS} = 50μA (10μA), then

A_v(n-channel) = 46.6V/V (104.23V/V) A_v(p-channel) = 31.4V/V (70.27V/V)

$$r_{out} = \frac{1}{g_{ds2} + g_{ds4}} = \frac{1}{25\mu A \cdot 0.09V^{-1}} = 0.444M\Omega \ (2.22M\Omega)$$

→ Larger r_{out} implies lower BW!

Small-Signal Analysis of the Common-Mode of the Differential Amplifier

The common-mode gain of the differential amplifier with a current mirror load is ideally zero.

To illustrate the common-mode gain, we need a different type of load so we will consider the following:

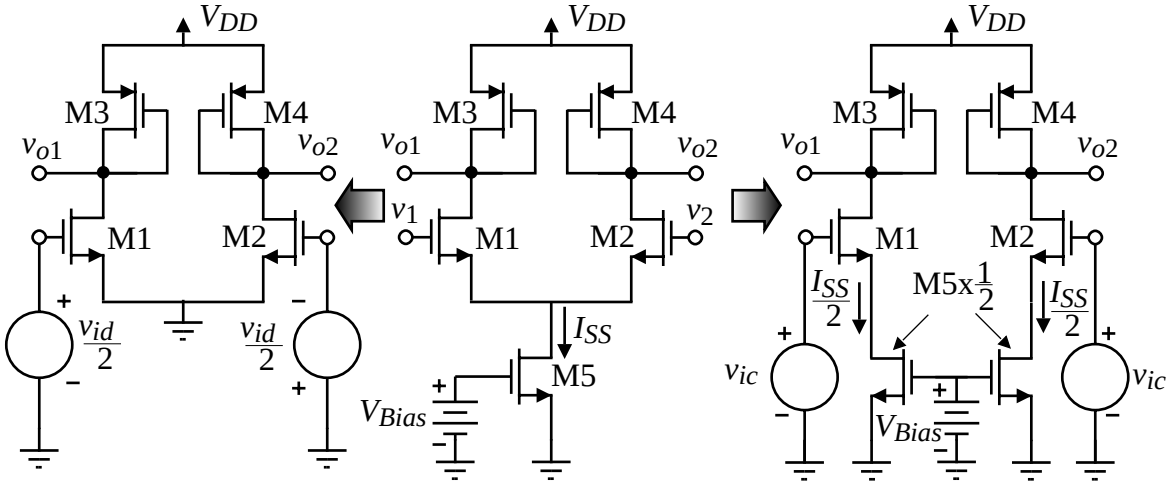

Fig. 330-05

Differential-Mode Analysis:

$$\frac{v_{o1}}{v_{id}} \approx -\frac{g_{m1}}{2g_{m3}} \qquad \text{and} \qquad \frac{v_{o2}}{v_{id}} \approx +\frac{g_{m2}}{2g_{m4}}$$

Note these voltage gains are half of the active load inverter voltage gain.

Small-Signal Analysis of the Common-Mode of the Differential Amplifier – Cont'd

Common-Mode Analysis:

Assume r_{ds1} is large and can be ignored (greatly simplifies the analysis).

$\therefore \quad v_{gs1} = v_{g1} - v_{s1} = v_{ic} - 2g_{m1}r_{ds5}v_{gs1}$

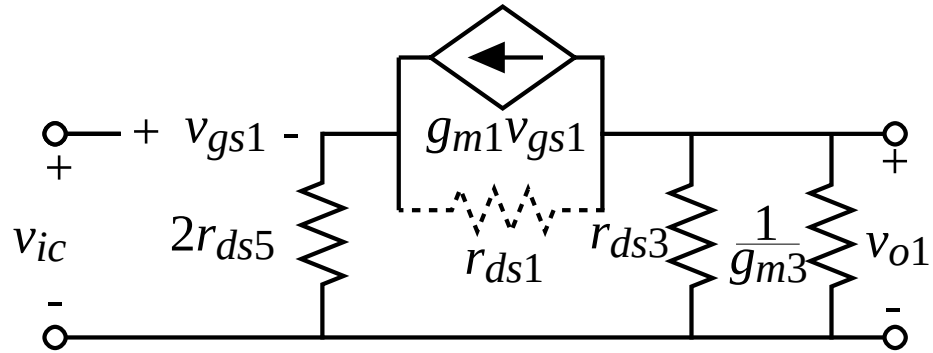

Fig. 330-06

Solving for v_{gs1} gives $$v_{gs1} = \frac{v_{ic}}{1 + 2g_{m1}r_{ds5}}$$

The single-ended output voltage, v_{o1}, as a function of v_{ic} can be written as

$$\frac{v_{o1}}{v_{ic}} = -\frac{g_{m1}[r_{ds3}\|(1/g_{m3})]}{1 + 2g_{m1}r_{ds5}} \approx -\frac{(g_{m1}/g_{m3})}{1 + 2g_{m1}r_{ds5}} \approx -\frac{g_{ds5}}{2g_{m3}}$$

Common-Mode Rejection Ratio (*CMRR*):

$$CMRR = \frac{|v_{o1}/v_{id}|}{|v_{o1}/v_{ic}|} = \frac{g_{m1}/2g_{m3}}{g_{ds5}/2g_{m3}} = g_{m1}r_{ds5}$$

How could you easily increase the *CMRR* of this differential amplifier?

With cascode or Regulated cascade (caution: increasing I_{SS} will do the opposite!)

Frequency Response of the Differential Amplifier

Back to the current mirror load differential amplifier:

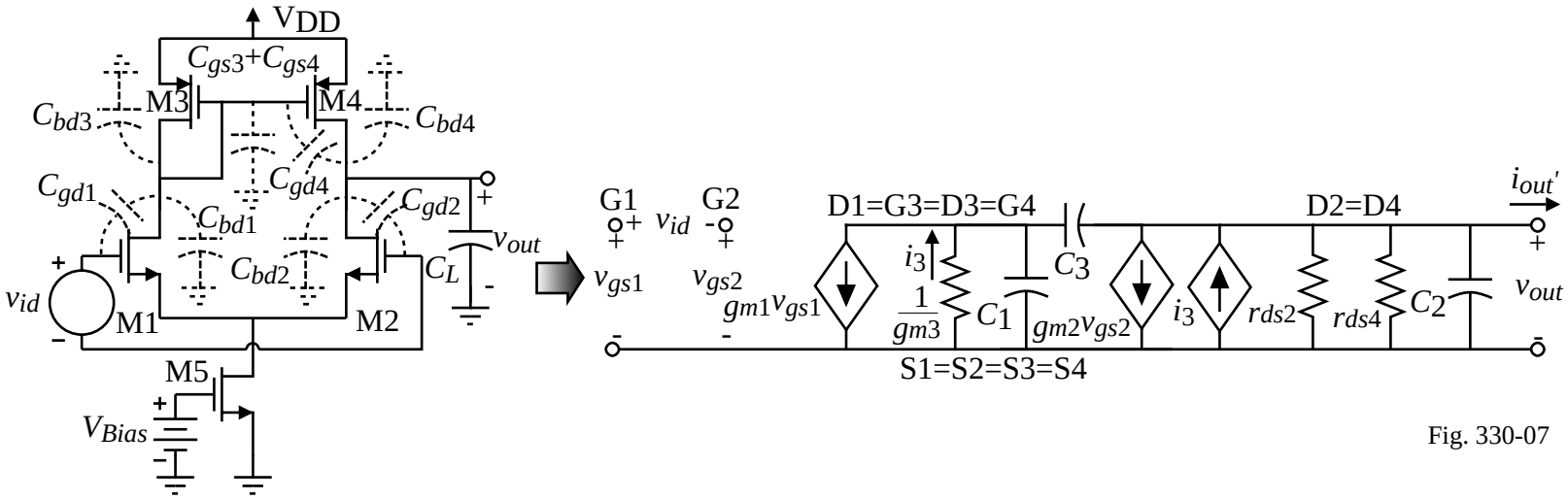

Fig. 330-07

Ignore the zeros that occur due to $C_{gd}1$, $C_{gd}2$ and $C_{gd}4$.

$$C_1 = C_{gd}1 + C_{bd}1 + C_{bd}3 + C_{gs}3 + C_{gs}4,$$

$$C_2 = C_{bd}2 + C_{bd}4 + C_{gd}2 + C_L$$

and $$C_3 = C_{gd}4$$

$$\text{If } C_3 \approx 0,\ V_{out}(s) \approx \frac{gm1}{gds2 + gds4}\left[\left(\frac{gm3}{gm3 + sC_1}\right) V_{gs}1(s) - V_{gs}2(s)\right]\left(\frac{\omega 2}{s + \omega 2}\right),$$

where $\omega 2 = \dfrac{ggs2 + gds4}{C_2}$ → if $C_3 \neq 0$, RHP Zero exists through M1-M4 path

& $C_1' = C_1 + C_{3\_Miller}$ → pole of V_{gs1} path is lower, at $g_{m3}/2\pi C_1'$

Frequency Response of the Differential Amplifier (Cont)

If we further assume $g_{m3}/C_1 >> (g_{ds2}+g_{ds4})/C_2 = \omega_2$,

the frequency response of the differential amplifier reduces to

$$\frac{V_{out}(s)}{V_{id}(s)} \cong \left(\frac{g_{m1}}{g_{ds2}+g_{ds4}}\right)\left(\frac{\omega_2}{s+\omega_2}\right)$$

(A more detailed analysis will be made later)

SUMMARY

- Differential amplifiers are easily analyzed by separating the stimulus into a differential and common mode excitation
- The input common mode range of the differential amplifier is the range of common mode voltages over which the amplifier senses and amplifies the differential voltage
- The common mode rejection ratio of the differential amplifier is the ratio of the differential voltage gain to the common mode voltage gain
- The differential voltage gain of the MOS differential amplifier with a current source or current mirror load is inversely proportional to the square root of the bias current.