[Prob1]

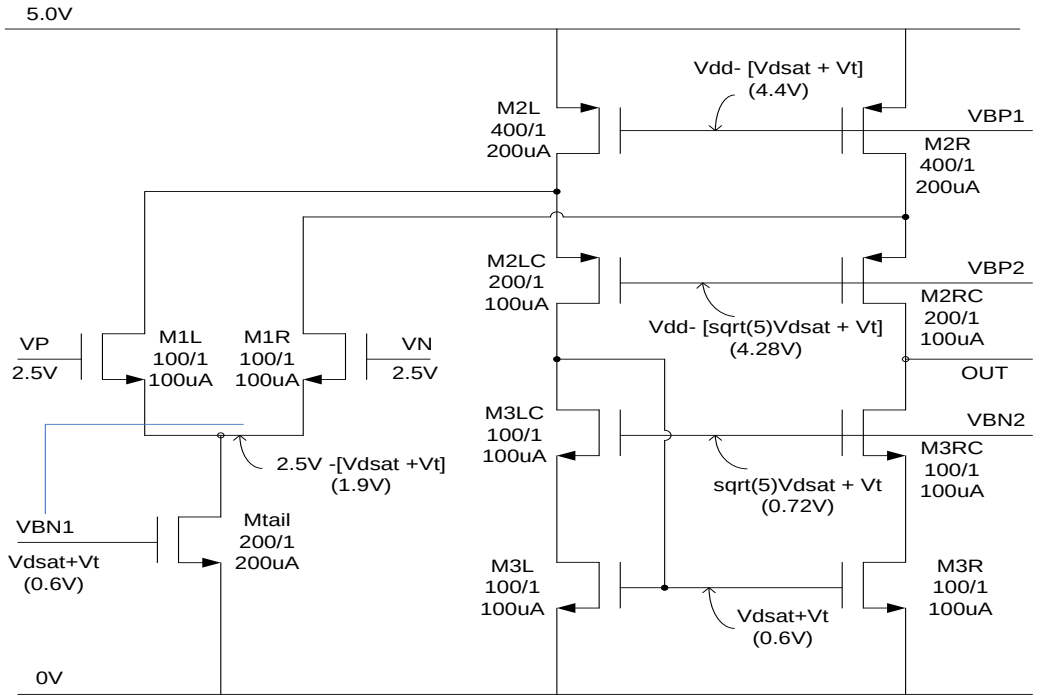


Figure 1. NMOS input folded cascode amplifier

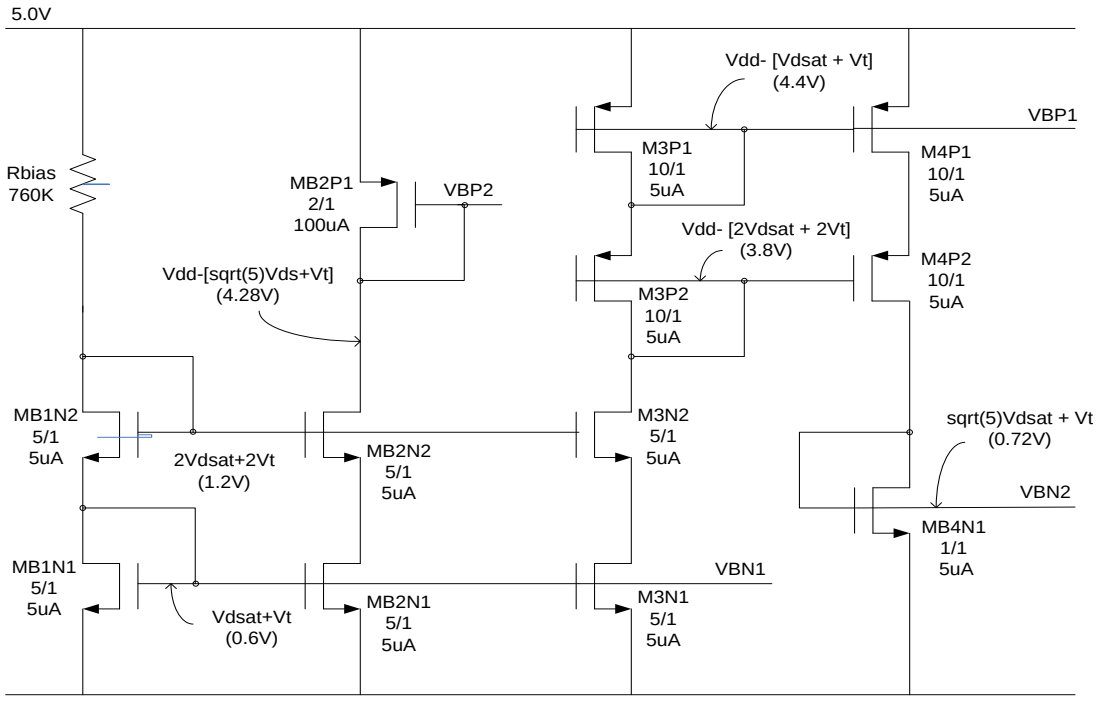


Figure 2. Bias network

		W (um)	Id (uA)	Vdsat (mV)	gm (mS)	Ro (ohms)*
Amplifier	M1L/R	100	100	100	2	100k
	Mtail	200	200	100	4	50k
	M2L/R	400	200	100	4	50k
	M2LC/RC	200	100	100	2	100k
	M3L/LC/R/RC	100	100	100	2	100k
Bias	MB1N1/2, MB2N1/2, MB3N1/2	5	5	100	0.1	2M
	MB3P1/2, MB4P1/2	10	5	100	0.1	2M
	MB2P1	2	5	224	0.045	2M
	MB4N1	1	5	224	0.045	2M

* $(1 + \lambda Vds)$ is assumed to be 1 for simplicity

(1) output impedance

$$Ro = (gm3RC \cdot ro3RC \cdot ro3R)||\{gm2RC \cdot ro2RC(ro2R||ro1R)\}$$
$$= (2mS \cdot 100k \cdot 100k)||\{2mS \cdot 100k \cdot (50k||100k)\} \approx 5MEG$$

(2) gain

$$Gm = gm1 = 2mS$$
$$Av = Gm \cdot Ro \approx 10{,}000$$

[Prob2]

	Hand calculation (uA)	SPICE simulation (uA)
M1L/R	100	112.52
Mtail	200	225.05
M2LC/RC, 3L/LC/R/RC	100	79.34
M2L/R	200	191.87
Bias1	5	5.00
Bias2	5	5.01
Bias3	5	5.01
Bias4	5	5.02

- Measured (unloaded) phase margin : ~15degree
- Load capacitance for 45degree phase margin : ~2.75pF

Folded_cascode.sp

```
* ee140 fa09 hw7 prob1 main
.lib 'ee140_model.lib' TT
.inc 'prob1_amp.sp'
.inc 'prob1_bias.sp'

xamp vp vn vbp1 vbp2 vbn1 vbn2 vdd vss out my_amp
$xbias vbp1_temp vbp2_temp vbn1_temp vbn2_temp vdd vss my_bias
xbias vbp1 vbp2 vbn1 vbn2 vdd vss my_bias

$cload out 0 1p

$ power supply
vdd_supply vdd 0 5.0
vss_supply vss 0 0.0

$ ideal bias supply
$vbp1 vbp1 0 4.4
$vbp2 vbp2 0 4.276
$vbn1 vbn1 0 0.6
$vbn2 vbn2 0 0.724

$ common/differential mode input
vic vn 0 2.5
vid vp vn dc=0 ac=1

$ DC sweep
.dc vid -2.5 2.5 10m

$ AC analysis
.meas ac av_10 find vm(out) at=10
.meas ac av_100k find vm(out) at=100000
.meas ac av_1meg find vm(out) at=1000000
.meas ac amp_f3db when vm(out)='av_10/1.414'
.meas ac amp_fu when vm(out)=1
.meas ac phase_at_fu find vp(out) at=amp_fu
.meas ac phase_margin param = '180+phase_at_fu'

.ac dec 10 1 1000g
$ pole-zero analysis
.pz v(out) vid

$ options
.options nomod post
.op

.end
```

Prob1_amp.sp

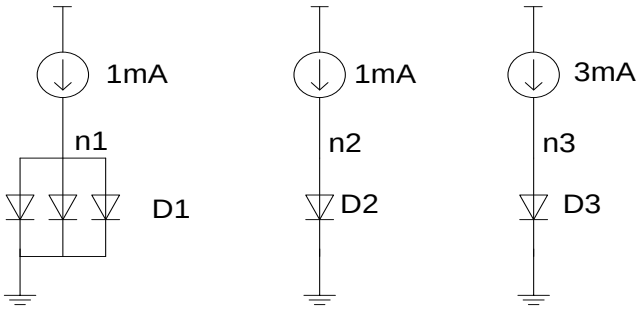
```
$ ee140 fa09 hw7 prob1 amp
```

```
.SUBCKT my_amp vp vn vbp1 vbp2 vbn1 vbn2 vdd vss out

$ gm stage signal path
X1l lp vp tail tail nmos w=100u l=1u
X1r rp vn tail tail nmos w=100u l=1u
Xtail tail vbn1 vss vss nmos w=200u l=1u

$ impedance stage (pmos load)
X2l lp vbp1 vdd vdd pmos w=400u l=1u
X2r rp vbp1 vdd vdd pmos w=400u l=1u
X2lc mn vbp2 lp lp pmos w=200u l=1u
X2rc out vbp2 rp rp pmos w=200u l=1u

$ impedance stage (nmos load)
X3l ln mn vss vss nmos w=100u l=1u
X3r rn mn vss vss nmos w=100u l=1u
X3lc mn vbn2 ln ln nmos w=100u l=1u
X3rc out vbn2 rn rn nmos w=100u l=1u
.ENDS
```

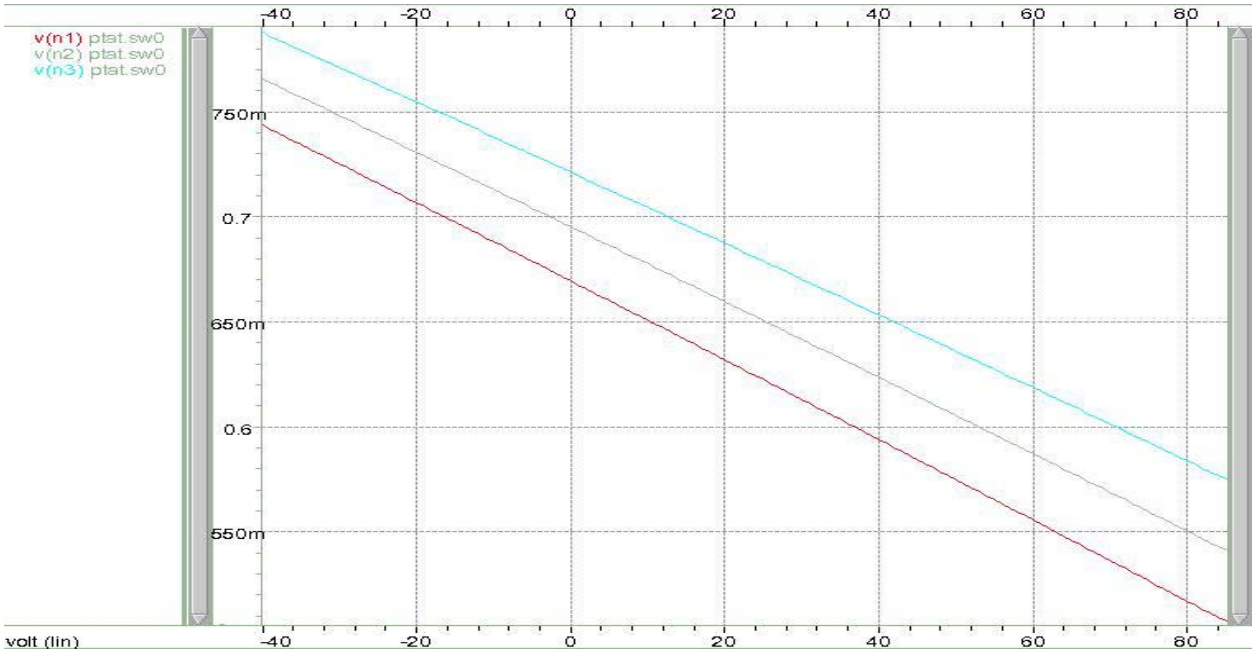
Prob1_bias.sp

```
$ ee140 fa09 hw7 prob1 bias circuit
.SUBCKT my_bias vbp1 vbp2 vbn1 vbn2 vdd vss
Rbias vdd bias2 760k
Xb1n2 bias2 bias2 vbn1 vbn1 nmos w=5u l=1u
Xb1n1 vbn1 vbn1 vss vss nmos w=5u l=1u

Xb2p1 vbp2 vbp2 vdd vdd pmos w=2u l=1u
Xb2n2 vbp2 bias2 bias3 bias3 nmos w=5u l=1u
Xb2n1 bias3 vbn1 vss vss nmos w=5u l=1u

Xb3p1 vbp1 vbp1 vdd vdd pmos w=10u l=1u
Xb3p2 bias4 bias4 vbp1 vbp1 pmos w=10u l=1u
Xb3n2 bias4 bias2 bias5 bias5 nmos w=5u l=1u
Xb3n1 bias5 vbn1 vss vss nmos w=5u l=1u

Xb4p1 bias6 vbp1 vdd vdd pmos w=10u l=1u
Xb4p2 vbn2 bias4 bias6 bias6 pmos w=10u l=1u
Xb4n1 vbn2 vbn2 vss vss nmos w=1u l=1u

.ENDS
```

[Prob3]



(1) voltage vs. temperature (℃)



* X-axis : temperate (℃), Y-axis:V

From the SPICE measurements, the temperature coefficients are

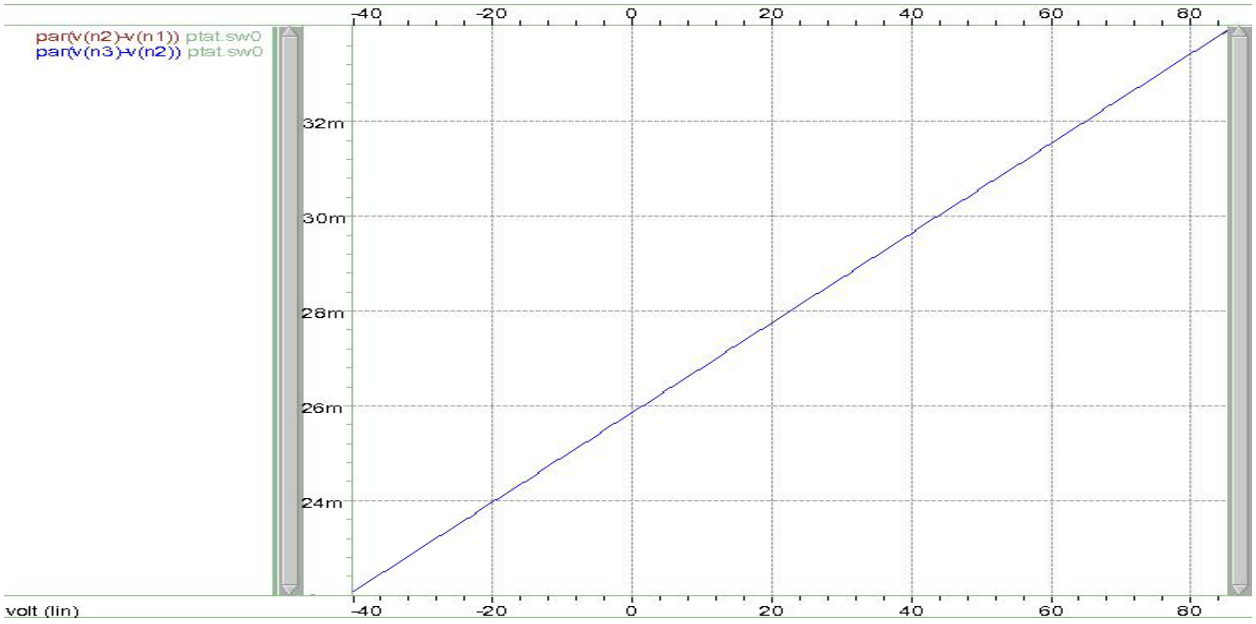
$$\left.\frac{\partial V_{D1}}{\partial T}\right|_{T=27℃} = -1.89mV/℃, \quad \left.\frac{\partial V_{D2}}{\partial T}\right|_{T=27℃} = -1.80mV/℃, \quad \left.\frac{\partial V_{D3}}{\partial T}\right|_{T=27℃} = -1.71mV/℃. .$$

The coefficients are different for three configurations. That is because, as shown in the following expression, the coefficient depends on the values of I_D and I_S.

$$I_D = I_S \cdot exp\left(\frac{V_D}{V_{TH}}\right) \qquad \therefore V_D = V_{TH} \cdot ln\left(\frac{I_D}{I_S}\right) = V_{TH}\left(ln(I_D) - ln(I_S)\right)$$

$$\therefore \ \frac{\partial V_D}{\partial T} = \frac{V_{TH}}{T} \cdot \ ln\left(\frac{I_D}{I_S}\right) - \frac{V_{TH}}{I_S} \cdot \frac{\partial I_S}{\partial T}$$

(2) voltage difference vs. temperature



* X-axis : temperate (℃), Y-axis:V(delta)

From the measurement, it can be observed that $V_{D3} > V_{D2} > V_{D1}$, and the difference between V_{D3} and V_{D2} is same as that of V_{D2} and V_{D1}. Also, the temperature coefficients of the voltage differences are same (two curves overlap in the plot) as the measurement values show below.

$$\frac{\partial(V_{D3}-V_{D2})}{\partial T}\Big|_{T=27℃} = +94.67\mu V/℃, \qquad \frac{\partial(V_{D2}-V_{D1})}{\partial T}\Big|_{T=27℃} = +94.67\mu V/℃$$

This can be verified by the following equations.

$$V_{D3} - V_{D2} = V_{TH} \cdot \ln\left(\frac{3I_D}{I_S}\right) - V_{TH} \cdot \ln\left(\frac{I_D}{I_S}\right) = \frac{K_B T}{q} \cdot \ln(3)$$

$$V_{D2} - V_{D1} = V_{TH} \cdot \ln\left(\frac{I_D}{I_S}\right) - V_{TH} \cdot \ln\left(\frac{I_D}{3I_S}\right) = \frac{K_B T}{q} \cdot \ln(3)$$

$$\therefore \quad \frac{\partial(V_{D3} - V_{D2})}{\partial T} = \frac{\partial(V_{D2} - V_{D1})}{\partial T} = \frac{K_B}{q} \cdot \ln(3) \cong +94.6\mu V/℃$$

This ΔV is PTAT (Proportional To Absolute Temperature) because (1) it intersects zero when temperature is zero, and (2) the slope, $\frac{K_B}{q} \cdot \ln(3)$ is constant against temperature.

Ptat.sp

```
* ee140 fa09 hw7 prob3 PTAT
.model subDiode D
```

```
i1 0 n1 1mA
d1 n1 0 subDiode m=3
i2 0 n2 1mA
d2 n2 0 subDiode
i3 0 n3 3mA
d3 n3 0 subDiode

.plot dc par('v(n3)-v(n2)')
.plot dc par('v(n2)-v(n1)')

.dc temp -40 85 1
.meas dc d1_temp_coeff deriv v(n1) at=27
.meas dc d2_temp_coeff deriv v(n2) at=27
.meas dc d3_temp_coeff deriv v(n3) at=27
.meas dc delta32_temp_coeff deriv par='v(n3)-v(n2)' at=27
.meas dc delta21_temp_coeff deriv par='v(n2)-v(n1)' at=27

.options post
.op
.end
```

[Prob4]

From (4.263) in GHLM, the output voltage is expressed as follows.

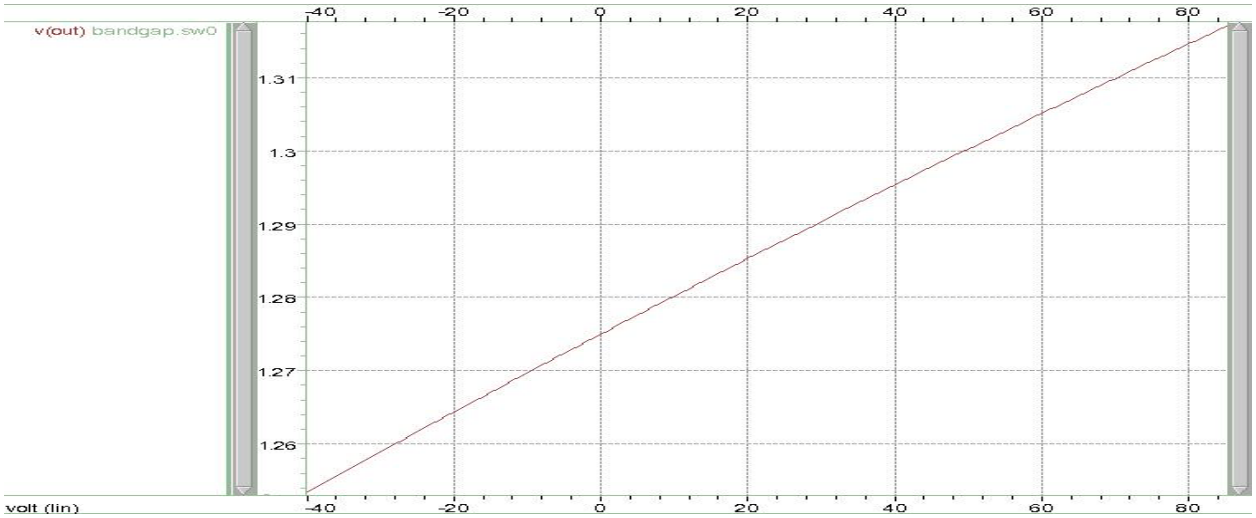
$$V_{out} = V_{D2} + V_{TH}\left(1 + \frac{R_2}{R_3}\right)\ln\left(3 \cdot \frac{R_2}{R_1}\right)$$

$$\therefore \ \frac{\partial V_{out}}{\partial T} = -1.80mV/℃ + \left(1 + \frac{R_2}{R_3}\right)\ln(3) \cdot 86\mu V/℃$$

When the resistor ratio, $\frac{R2}{R3}$ is 25,

$$\frac{\partial V_{out}}{\partial T} = -1.80mV/℃ + (1 + 25)\ln(3) \cdot 86\mu V/℃ \cong 660\mu V/℃.$$

The simulated output voltage vs. temperature plot is as follows.

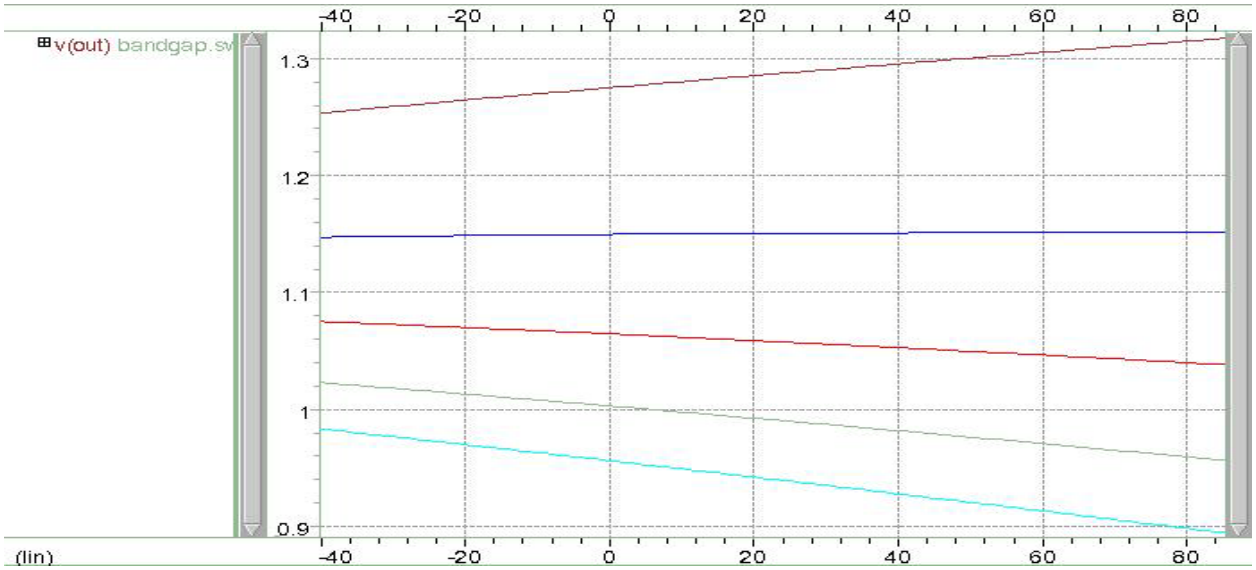


* X-axis : temperate (℃), Y-axis:V(out)

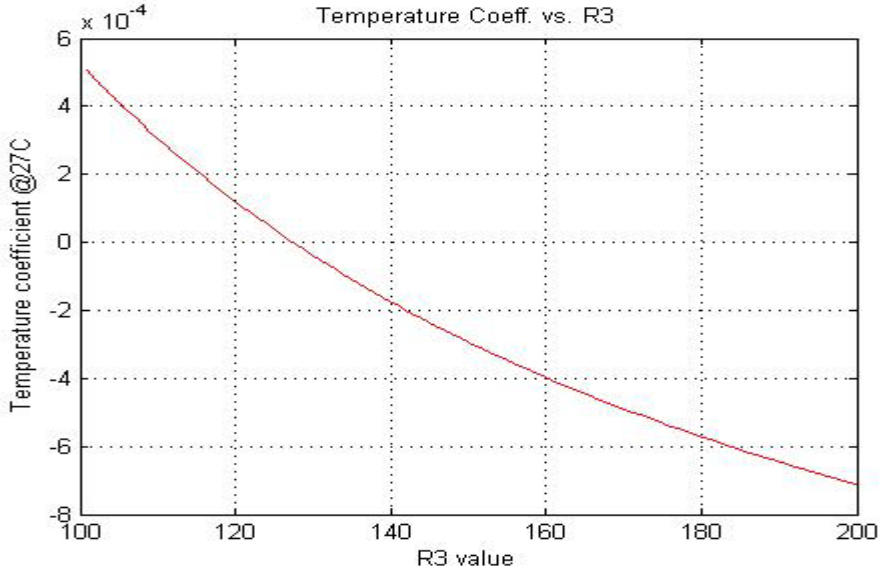
The measured coefficient is $504.4\mu V/℃$. The difference between the hand calculation and the simulation came from the different temperature dependence of the resistor values. Ignoring the resistor temperature coefficients, the resistor ratio for zero temperature dependency can be calculated as ,

$$\frac{R_2}{R_3} = \frac{1.80mV}{94.67\mu V} - 1 \approx 18.$$

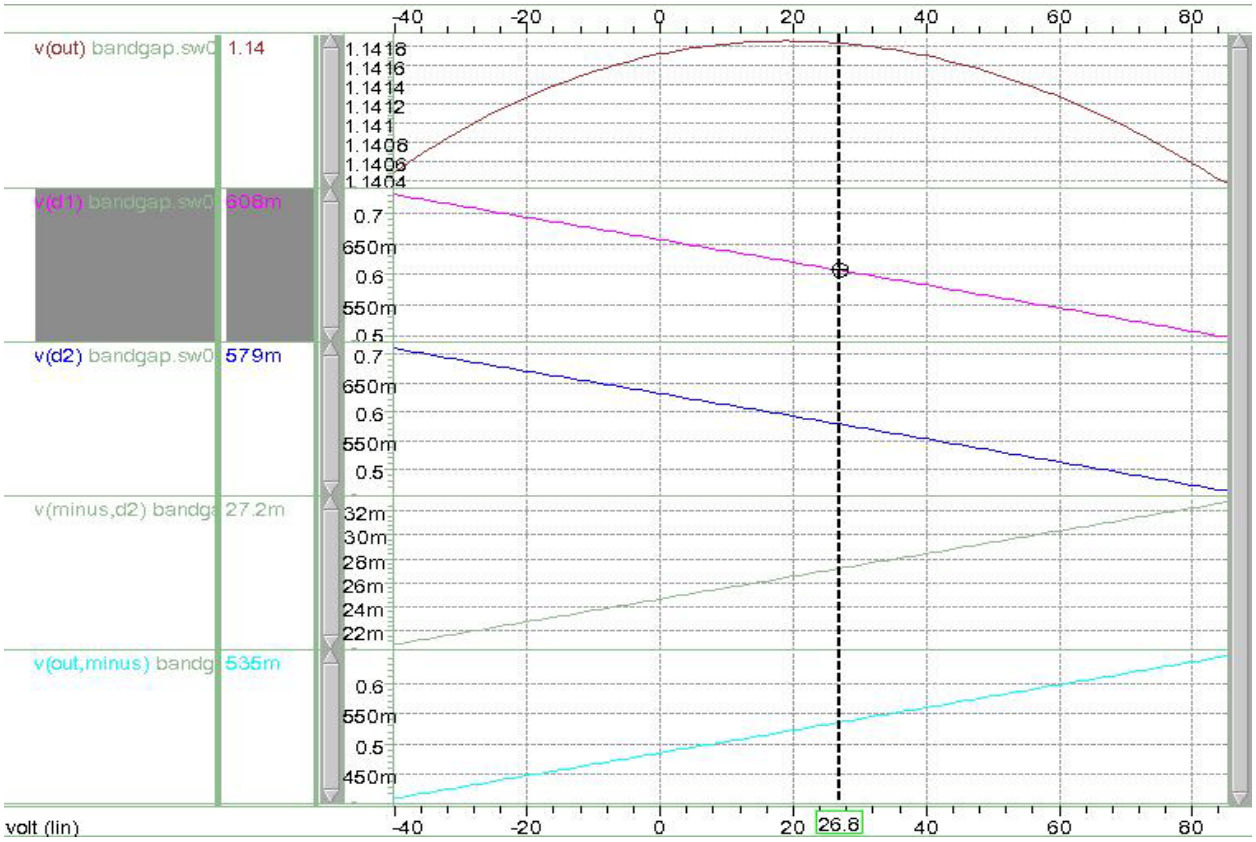
The simulated temperature dependency plots with different resistance ratio from 12.5 to 25 are shown below.



* X-axis : temperate (℃), Y-axis:V(out)



When R3= 127, $\frac{R_2}{R_3} \approx 19.7$, the voltages are changed by temperature as follows. The output voltage variation is about 1.5mV.



* X-axis : temperate (°C), Y-axis:Voltage

bandgap.sp

```
* bandgap w/ ideal amp

.model subDiode D
.param r3_val = 127

d1 d1 0 subDiode
d2 d2 0 subDiode m=3

r1 out d1 2.5k tc=0.001
r2 out minus 2.5k tc=0.001
r3 minus d2 r3_val tc=0.001

* ideal opamp
eamp out 0    d1 minus  1000

.print dc v(minus, d2) v(out, minus)

.dc temp -40 85 1
$.dc temp -40 85 1 sweep r3_val lin 100 100 200

$.meas dc temp_coeff deriv v(out) at=27

.options post
.op
.end
```

[Prob5]

(1) Input range : The op-amp input voltages(V(minus), V(d1)) vary from 500mV to 730mV (~ Vdsat+Vt). The NMOS input folded cascode we built in Prob1 can't handle this input range. But the op-amp from the project 1 works for this range.

(2) Output loading : Depending on the resistor values, the op-amp gain can drop significantly. The folded cascode and the amp from the project1 might not be able to have enough gain if R values are not large enough or if we don't add an output stage to the amps.