國 立 成 功 大 學

電 機 工 程 研 究 所

碩 士 論 文

可調節的低壓降穩壓器之設計與實現

Design and Implementation of an Adjustable Low Dropout Voltage Regulator

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Design and Implementation of an Adjustable Low Dropout Voltage Regulator

by

Bing-You Gau

A thesis submitted to the graduate division in partial
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可調節的低壓降穩壓器之設計與實現

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摘　　要

在這篇論文中，我們提出一個可調節的低壓降穩壓器。這個可調節的低壓降穩壓器可以透過外部控制訊號加以控制，進而轉換兩個以上不同等級的穩定輸出電壓。在論文裡有提到不同種類有關於如何實現可調節的低壓降穩壓器的架構，他們不但功率耗損以及面積都不小，而且轉換電壓需要非常長的時間。利用本篇論文所提出的具調節功能之參考電壓產生器以及動態放電路徑所組成的可調節之低壓降穩壓器擁有較低的功率消耗、較低的使用面積、較快速的轉換時間以及很高的延展性。本篇論文裡所設計的具調節功能之參考電壓產生器的架構非常簡單，而且他所消耗的靜態電流只有 7 微安培，同時參考電壓產生器所產生的參考電壓值所擁有的溫度係數都低於 35 ppm/°C。除此之外，當設計者想要增加輸出電壓的數目時，只需要再增加額外的兩極連接電晶體並且適當的調整電晶體尺寸後就可以達到目的。因此利用所設計的具調節功能之參考電壓產生器而做出來的可調節之低壓降穩壓器具有很高的延展性。此篇論文中所設計之可調節的低壓降穩壓器只需要 1.6 毫秒，從 2.5 伏特高輸出電壓轉換到 1.0 伏特低輸出電壓。

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Adjustable Low Dropout Voltage Regulator

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Abstract

In this thesis, we present an adjustable low dropout (LDO) voltage regulator. Through external control signals, the adjustable low dropout voltage regulator can switch between two or more stable output voltages. Several structures of adjustable LDO linear regulators not only consume large power and area, but also require extremely long recovering time from discharging process. Our proposed adjustable LDO linear regulator consisted of a new adjustable reference voltage generator and a dynamic discharging path has the features of lower power consumption, smaller area, shorter transform time and higher extendibility. The structure of the proposed adjustable reference voltage generator is easy to realize and consumes only 7μA. Both temperature coefficients of the generated reference voltages are below 35ppm/°C. Moreover, if designers want to increase the number of output voltages, they only needs to add extra diode-connected transistors in the current structure. The transform time of the proposed voltage regulator is only about 1.6 m sec for output voltage discharging from 2.5V to 1.0V.

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Chapter 1

Introduction

There are large demands for low dropout (LDO) voltage linear regulators inside the automotive applications, advanced microprocessors and portable equipments such as cellular phones, pagers, camera recorders, and laptops. The linear regulators are responsible to provide stable and accurate internal voltages for devices at low supply-voltage. With the increase of the systems' complexity, the number of LDO voltage regulators inside the system also increases. This phenomenon reveals that the designer should concern about the area and power of linear regulators to prevent the overhead in the system. An alternative way to reduce the number of linear regulators is to design an adjustable linear regulator which can provide more than one stable internal voltage. And the internal voltages can be selected through external control signals. Such kind of design can replace more than two of the traditional single-output liner regulators because of its flexibility. In other words, the adjustable linear regulators can be applied to the multi-supply systems or complicated power management. The challenges will be to generate stable and accurate internal voltages generated by the adjustable linear regulator.

1.1 Preliminary

In the past, many ICs are fabricated in CMOS technology operating at 5V supply voltage and this has led to a large number of systems with a 5V supply on the PCB's [2]. As technology advances, the supply voltage has scaled down to 3.3V or lower for 0.35μm and 0.18μm technologies. In order to reduce the power consumption and cost of ICs, the IC manufacturers need to use advanced technology. Problems occurs when the system needs to include not only the circuits driven by the high supply voltage, but also several low-power components by a low supply voltage. For the sake of achieving both low-power operation and single power supply of the integrated system, an on-chip dc-to-dc converter, as shown in Fig. 1-1 and Fig. 1-2, is inevitably needed to bridge the supply gap [1]. For example, if the system has two different digital circuits which are constructed by TSMC 0.35μm 5V transistors and TSMC 0.35μm 3.3V transistors separately, it needs an on-chip dc-to-dc converter to transform the external 5V supply voltage to internal 3.3V supply voltage for driving circuits composed of TSMC 0.35μm 3.3V transistors.

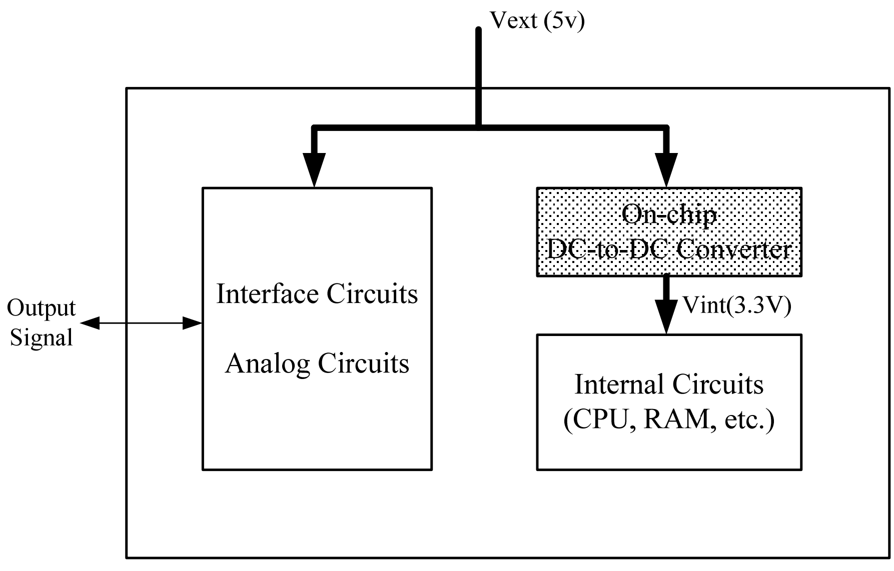

Fig. 1-1 System LSI with an on-chip dc-to-dc converter [1]

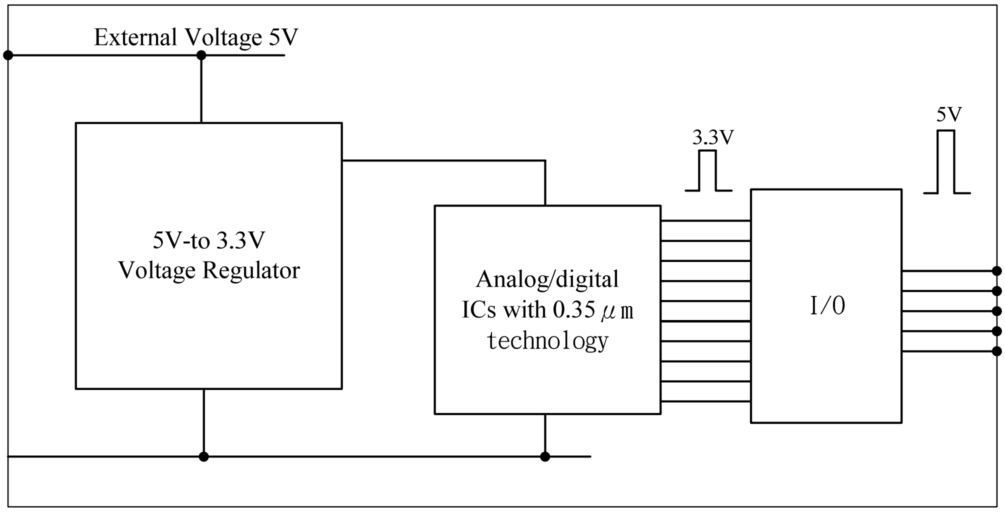

Fig. 1-2 Typical IC application of the regulator [2]

In general, there are several options of architectures about the on-chip dc-to-dc converter using in the system LSI. The common architecture of dc-to-dc converter in the market is classified into two kinds [3][4]: 1.) switching-type voltage regulator[1][5][6][7]; 2.) series-type voltage regulator [1][2][3][4][8][9][10]. In the following paragraphs, the qualities, differences and operation are described in detail.

1. Switching-type voltage regulator:

The switching-type voltage regulator, also called switch-mode regulator, is widely utilized in the power supply design requiring high efficiency and high power. The switching-type voltage regulator transfers energy to the load in discrete current pulse by turning on/off one or more power switches which are connected in series with the load. Then the current pulses are converted to continuous current through an inductive and capacitor filter. The main advantage of the switching-type voltage regulator is that it has higher efficiency than the series-type voltage regulator. It is because that when the power switch is turn off (operating at cut-off region), it dissipates no power. When the power switch is turn on (operating at triode region), it dissipates only a little power because of small drop voltage across power switch. With this manner, the input power can be transferred to the load without seriously loss of power. Consequently, it can achieve high power efficiency, typically in the range between 70 and 90%, and is independent of the difference between input and output voltage. The switching-type voltage regulator, however, has several disadvantages, such as the requirement of external inductance and large capacitor which are hard to be integrated inside the chip, and weak transient response. Furthermore, it includes more output noises and ripples than these of the series-type voltage regulator. This is because of electromagnetic and radio-frequency interference (RFI) generated by the inductor [11][12]. The simplified block diagram of a conventional switching-type voltage regulator is shown in Fig. 1-3.

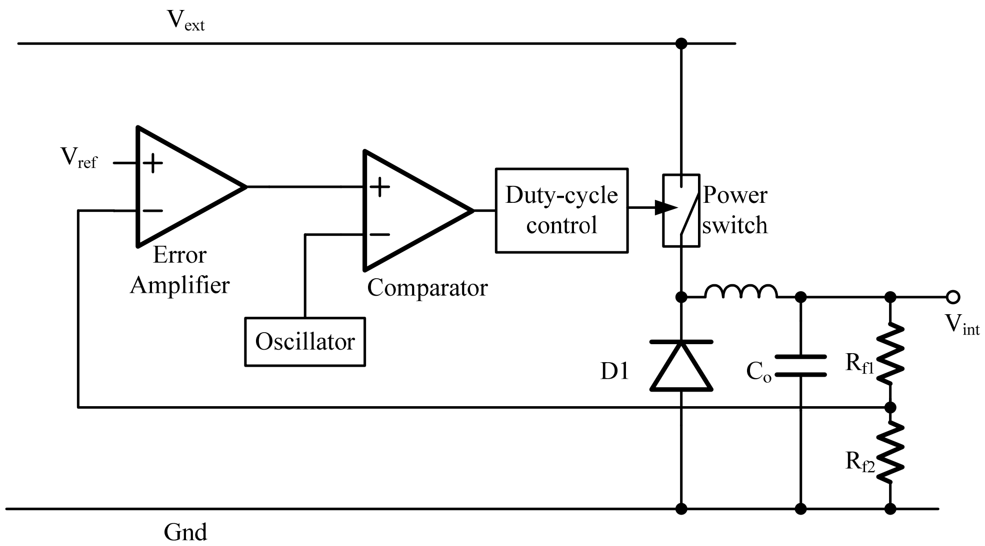

Fig. 1-3 The block diagram of conventional switching-type voltage regulator

The operation of the switching-type voltage regulator is described as follows. In the beginning, the output voltage (V_{int}) is sent to one of the inputs of the error amplifier through the feedback path constructed by resistors R_{f1} and R_{f2}. Then the error amplifier amplifies the difference between the reference voltage and the feedback signal and transfer to the comparator. Afterwards, the comparator compares the outputs come from the error amplifier and the oscillator, and produces corresponding voltage level to the duty-cycle control circuit. Finally, the duty-cycle control circuit generates a stream of pulses to control the on-off time of the power switch.

2. Series-type voltage regulator:

The structure of series-type voltage regulator is simpler than switching-type voltage regulator. It is composed of a reference voltage generator, an error amplifier, feedback resistors, and a series pass transistor. The simplified block diagram of series-type voltage regulator is shown in Fig. 1-4.

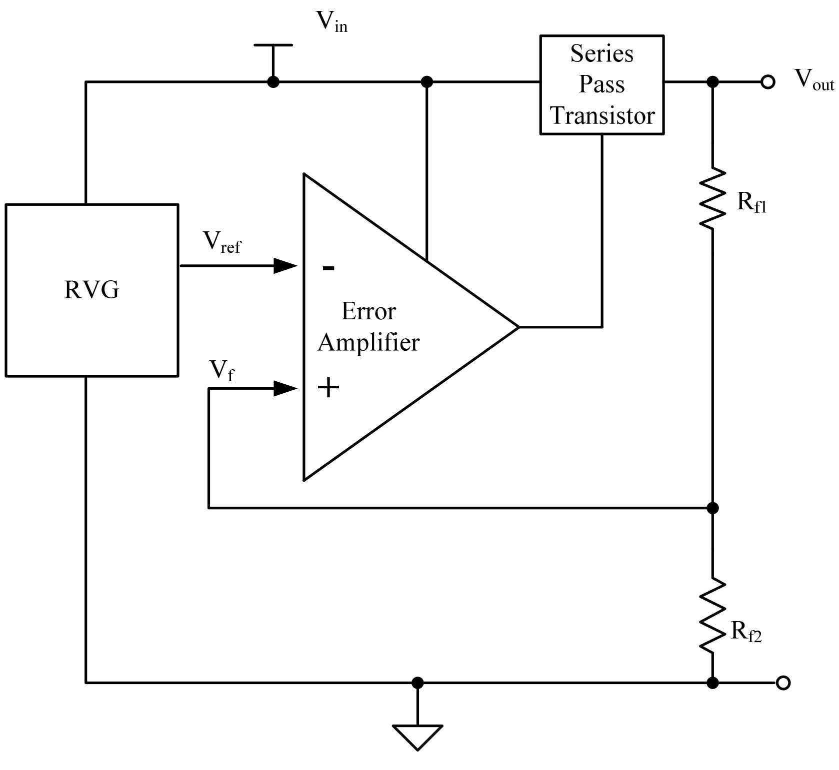

Fig. 1-4 The block diagram of traditional series-type voltage regulator

The operation of series-type voltage regulators is described in the following. The reference voltage generator (RVG) is responsible for providing a stable and accurate reference voltage V_{ref} which can resist temperature and input voltage variation. The error amplifier is used to amplify the difference of the reference voltage V_{ref} and the feedback signal V_f which is sent from the output of the regulator through the feedback resistor R_{f1} and R_{f2}. At last, the output signal of the error amplifier regulates the output voltage by controlling the drop voltage across the series pass transistor, which connects the input voltage and the load. The relation between the reference voltage V_{ref} and the output voltage Vout is given by Eq. 1-1 where the R_{f1} and R_{f2} are feedback resistors.

$$V_{out} = V_{ref} \times \frac{R_{f1} + R_{f2}}{R_{f2}} \qquad \text{Eq. 1-1}$$

The major advantages of the series-type voltage regulator are good transient response, and smaller noise. Furthermore, the series-type voltage regulator occupies less PCB layout area than the switching-type voltage regulator because of simple structure and no need of the external inductance. However, the series-type voltage regulator can not achieve as high power efficiency as switching-type voltage regulator. It is due to the dependence on ratio of input-to-output voltage.

With the advancement of technology, the system-on-chip has become the main trend from now on. Therefore, the series-type voltage regulator most likely be adapted for the multi-supply system in the hear future.

1.2 Motivation

A lot of portable devices such as cell phones, PDAs and laptop computers are in great demand today [3][13][14]. This trend motivates the system designers to spend more efforts in reducing the power consumption of the circuits inside the products to prolong the battery life. Although there are many techniques about decreasing the power consumption of the system, the most popular way is to reduce the supply voltage of the system. That is because the supply voltage plays an important role in the power formula. Therefore, many SOC designers prefer to integrate power management within the system and also increase the cells' operation-modes for collaborating with the power management unit. In other words, the system operates under multiple supply voltages. The design of such a system becomes more complicate.

The power management is responsible to control several voltage regulators to operate under different modes, such as sleep mode or active mode, according to the power management's policy. Then the whole system can achieve low power consumption as each component works under proper operation mode. A typical block diagram of power management is shown in Fig. 1-5. The lithium battery generates a supply voltage between 2.97V (minimum) and 4.2V (maximum). The power management, driven by lithium battery, is composed of a control unit and several LDO linear regulators to produce several stable supply voltages for the internal function blocks. While the number of functional blocks inside the system increases, there would be more different LDO linear regulators should be used for coordinating with power management.

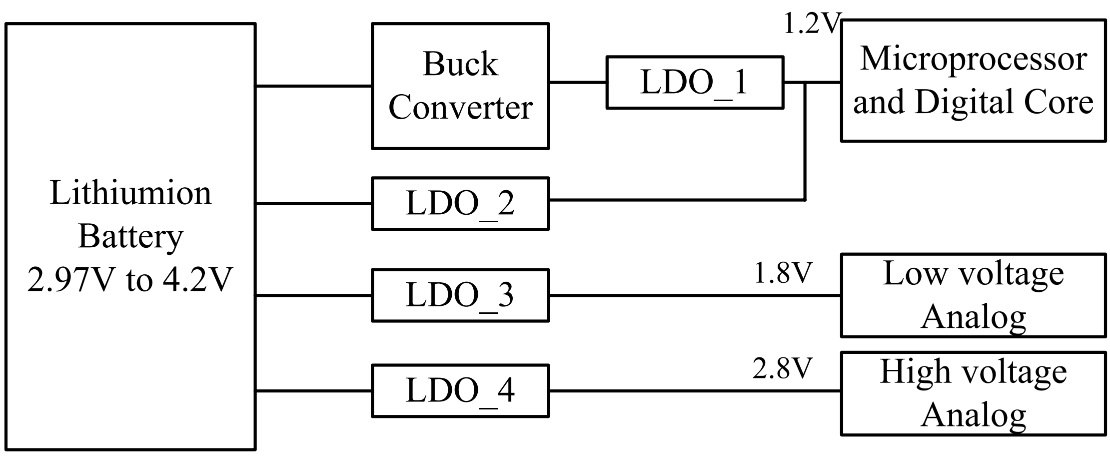

Fig. 1-5 Block diagram for typical power management [14]

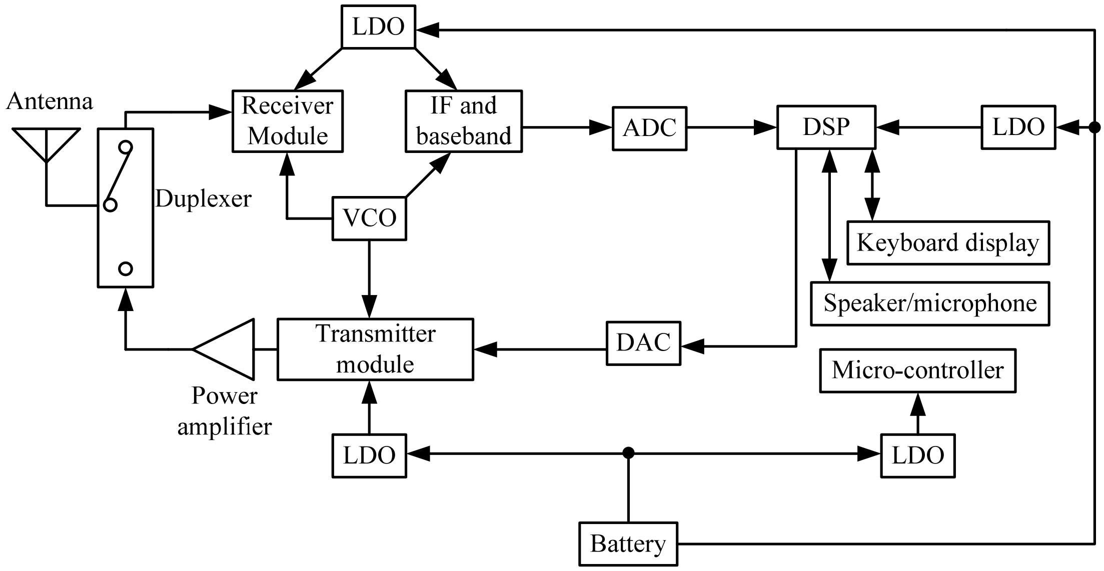

Fig. 1-6 Typical application of LDO in digital cellular phone [9]

Fig. 1-6 shows a typical application of low dropout linear regulators utilized in digital cellular telephones [9]. In this application, it needs four LDO linear regulators to provide internal stable voltages for internal components to work at low supply voltages. In general, there are more LDO linear regulators used for the cellular telephone in the future.

In the traditional design of LDO linear regulators, they only generate one single stable output voltages. So the system designers have to select a number of different LDO linear regulators for different internal components. While the complicate system needs more LDO linear regulators in the future, the designer has to worry about the PCB layout area and power consuming of the LDO linear regulators. It is because these two factors limit the number of LDO linear regulators used in a system. Recently, a lot of approaches have been proposed to reduce power and area of LDO linear regulators. However, there is still another efficient way to improve LDO linear regulators. That is to design an adjustable LDO linear regulator. An adjustable LDO linear regulator means it can be controlled to provide more than one stable output voltages. According to the control signal, it can be adjusted to provide certain expected internal voltage. This design obviously can replace two or more than two of traditional single-output LDO linear regulators. It means the system designer can use a few of adjustable LDO linear regulators to replace a lot of traditional LDO linear regulators in order to save more PCB layout area and power. Besides, the adjustable LDO linear regulator can be more adaptive to the needs of power management. However, it is very important to be sure that the adjustable LDO linear regulator will not consume too much power and PCB layout area.

1.3 Our Contributions

In this thesis, we propose two components to improve the quality of the adjustable LDO linear regulator. One is the novel adjustable reference voltage generator which can generate two stable reference voltages. The structure is simple and purely constructed by CMOS transistors. It consumes small area along with low power consumption and has high extendibility. Another one is the technique to speed up the transform time, since the adjustable LDO linear regulator needs significant amount of time to transform from the high voltage to the low voltage.

1.4 Thesis Organization

The rest of the thesis is organized as follows. In Chapter 2, we will define terms, and describe fundamental operations of traditional LDO linear regulators as well as design issues related to the LDO linear regulators. In Chapter 3, several structures of adjustable LDO linear regulators will be analyzed and compared. In Chapter 4, an adjustable LDO linear regulator that is composed of the proposed adjustable reference voltage generator, a two-stage error amplifier and dynamic discharging path is presented. Following that, the

Layout, post-layout simulating results will be discussed in Chapter 5. Finally, we will draw conclusions in Chapter 6.

Chapter 2

Fundamentals of LDO Linear Regulators

In this chapter, fundamental operations and concepts of LDO linear regulators are described. In addition, several basic structures of LDO linear regulators will be discussed, such as NMOS-type LDO linear regulators, PMOS-type LDO linear regulators, and improved NMOS LDO linear regulators. Then, a number of terms about LDO linear regulators are presented [16][17]. Each kind of LDO linear regulator has its own pros and cons. The system designer has to choose the LDO linear regulators according to system requirements. After that, considerations and design issues are discussed while designing the LDO linear regulators.

2.1 Structure and Principle of Operation

Fig. 2-1 shows the functional block diagram of a typical LDO linear regulator. The LDO linear regulator is composed of a reference voltage generator (RVG), an error amplifier, a series pass transistor, and a feedback network. The operation principle is described in the following. The reference voltage generator is used to generate a stable and accurate reference voltage. Then the error amplifier detects the difference between the output voltage V_{out} and the reference voltage V_{ref}, then turns on/off the series pass transistor to regulate the output voltage.

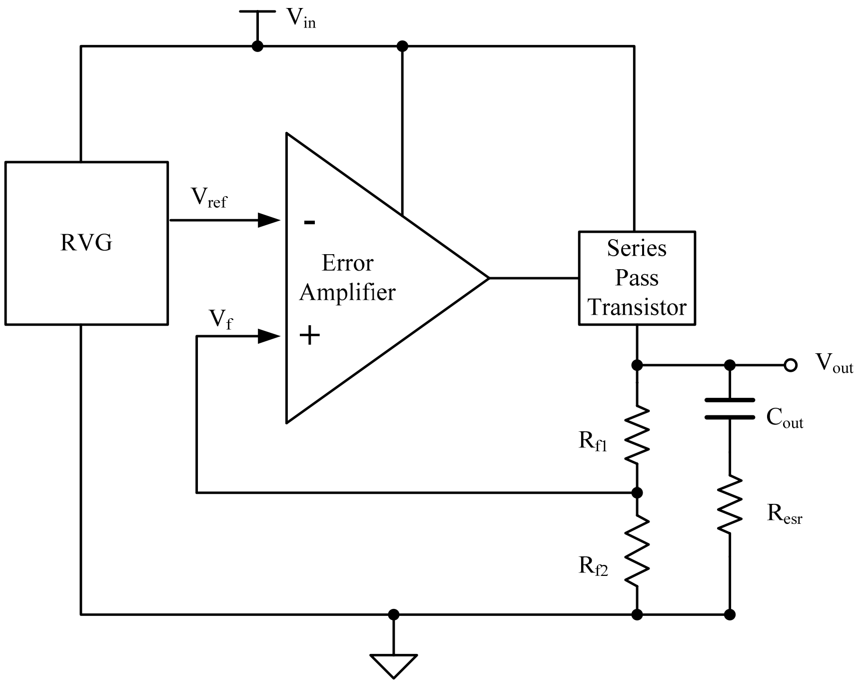

Fig. 2-1 Functional block diagram of a low dropout linear regulator

Fig. 2-2 shows a simplified block diagram of LDO linear regulator [14]. This LDO linear regulator is a negative feedback system constructed from an error amplifier, a series pass transistor, and the feedback network. While the feedback signal V_f is not the same as reference voltage V_{ref}, the error amplifier begins to change the control signal V_{ea} of series pass transistor. According to the control signal V_{ea}, the series pass transistor which connects input voltage and output voltage will increase or decrease the current through it self.

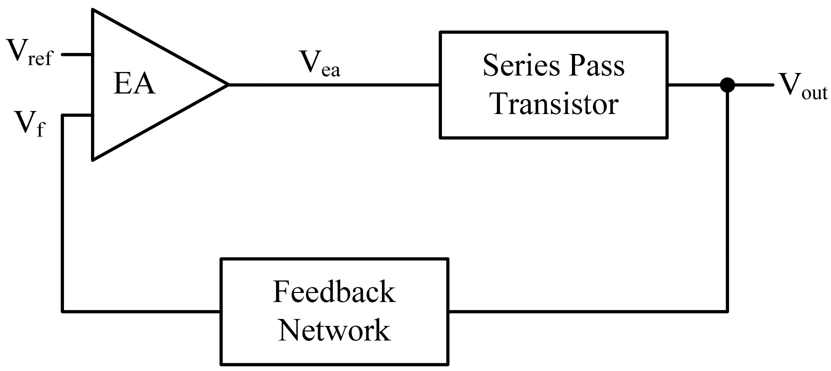

Fig. 2-2 Simplifier block diagram of LDO linear voltage regulator [14]

2.2 Terms and Definitions

This section presents several terms and definitions about LDO linear regulators [16][17]. Such as dropout voltage, quiescent current, power efficiency, load regulation, line regulation, power supply rejection, output noise, transient response, range of stable ESR, accuracy, and power dissipation.

2.2.1 Dropout Voltage

Dropout voltage is defined as the minimum difference between the input voltage and the output voltage of LDO linear regulator while the LDO linear regulator is under regulation region. Fig. 2-3 shows the input/output characteristics of the chip TPS76733 which is a LDO linear regulator operating at 3.3V. The dropout voltage of the chip TPS76733 is typically 300mV while the loading current is equal to 1A [16]. As the input voltage V_{in} increases to 3.6V, the LDO linear regulator enters the regulation region. In this region, the output of LDO linear regulator remains regulated. It means the output voltage is almost independent of the variations of input voltage or load current. As the input voltage is less than 2.5V, the output voltage is no longer regulated. As the input voltage stays inside the range between 2.5V and 3.6V, the LDO linear regulator is under dropout region. In the dropout region, the series pass transistor behaves as a resistor and dropout voltage is expressed in terms of its on-resistance (R_{ON}). The dropout voltage is given in Eq. 2-1, where the R_{ON} is the on-resistance of series pass transistor, I_o is the loading current.

$$V_{dropout} = I_o \times R_{ON} \qquad \text{Eq. 2-1}$$

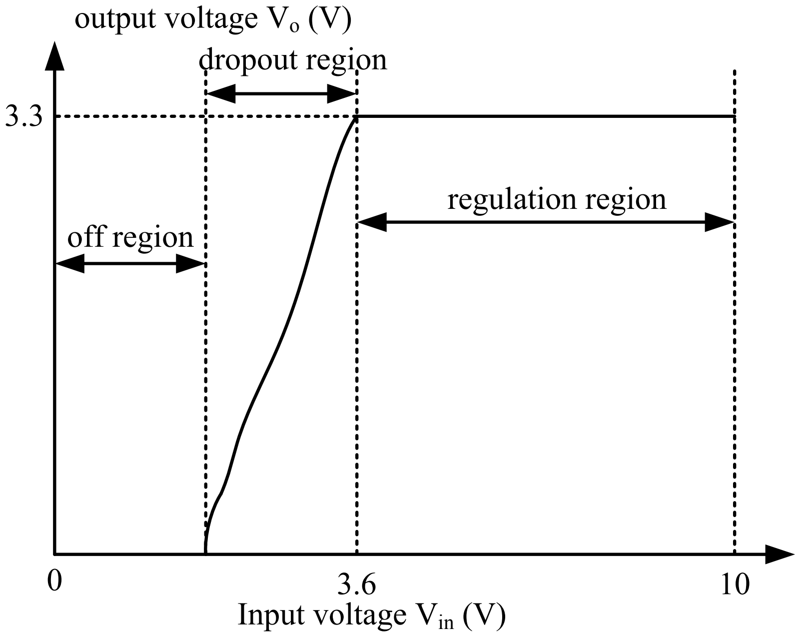

Fig. 2-3 Dropout Region of TPS76733 (3.3V LDO) [16]

The dropout voltage is the key factor of power efficiency. Because the dropout voltage reveals that the power dissipating on the series pass transistor.

2.2.2 Quiescent Current

Quiescent current, which is also called ground current, is defined as the difference between the input current and the output current which is shown in Fig. 2-4 [16]. The quiescent current is expressed as shown in Eq. 2-2.

$$I_q = I_i - I_o \qquad \text{Eq. 2-2}$$

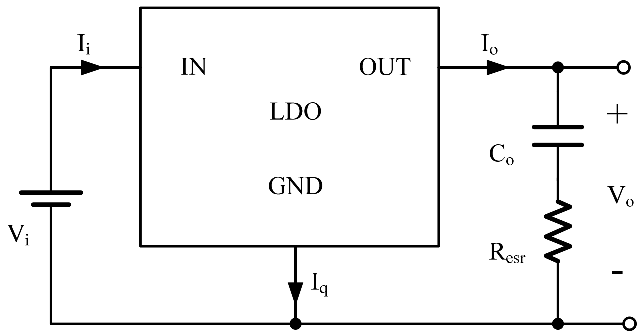

Fig. 2-4 Quiescent Current of the LDO linear regulator [16]

Quiescent current includes the gate drive current of the series pass transistor and the bias current used for biasing the error amplifier, feedback network, and the reference voltage generator. Low quiescent current is necessary for prolonging the battery's life. It is a key factor in the design of the LDO linear regulator especially for the portable equipments. Limits to low quiescent current, however, affects the transient output voltage variation and frequency response of LDO linear regulators. Typically, more quiescent current flow is necessary for improving the performance of LDO linear regulators.

Driving current of the series pass transistor is different between bipolar and MOS transistors. The driving current of bipolar transistors is increasing as load current increasing because bipolar transistors are current-driven devices. For MOS transistors, the driving current is almost constant because they are voltage-driven devices.

2.2.3 Power Efficiency

The power efficiency is defined as the ratio of input power and output power which is shown in Eq. 2-3 and depicted in Fig. 2-5 where I_{out} and I_q are the output current and the quiescent current of LDO linear regulators, V_{in} and V_o are the input voltage and output voltage of LDO linear regulators [16].

The power efficiency is mostly limited by the quiescent current and the dropout voltage of LDO linear regulators. Hence the low quiescent current and the low dropout voltage are the main goals of designing a LDO linear regulator with high efficiency.

$$Power\ Efficiency = \frac{I_{out} \cdot V_o}{\left(I_q + I_{out}\right) \cdot V_{in}} \qquad \text{Eq. 2-3}$$

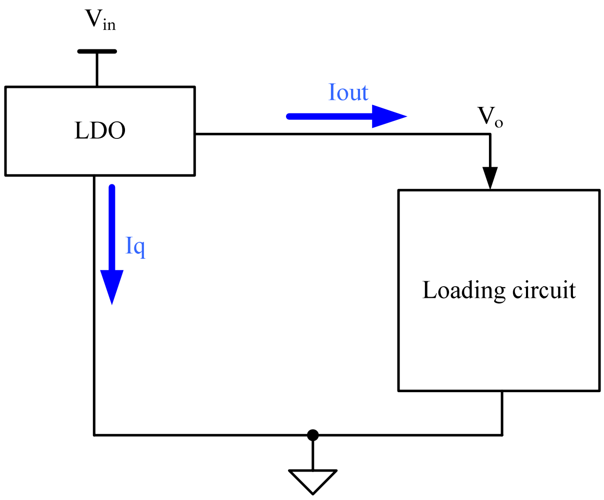

Fig. 2-5 Power efficiency of LDO linear regulator

2.2.4 Load Regulation

The load regulation means the ability of LDO linear regulators to resist the variation of loading current which can be expressed in Eq. 2-4 and depicted in Fig. 2-6, where A is the gain of the error amplifier, R_{f1} and R_{f2} are the feedback resistors, and g_{mp} is the transconductance of the series pass transistor. The load regulation is a steady-state parameter, and all of the frequency components can be omitted.

$$Load\ regulation = \frac{\Delta V_o}{\Delta I_o} \approx \frac{1}{g_{mp}A} \cdot \left(\frac{R_{f1} + R_{f2}}{R_{f2}} \right) \qquad \text{Eq. 2-4}$$

According to Eq. 2-4, the load regulation can be improved by increasing the loop gain of LDO linear regulator which is constructed by the gain of error amplifier and the transconductance of series pass transistor. However, increasing the loop gain of LDO linear regulators will also influences the frequency response. There is a trade off between these two factors.

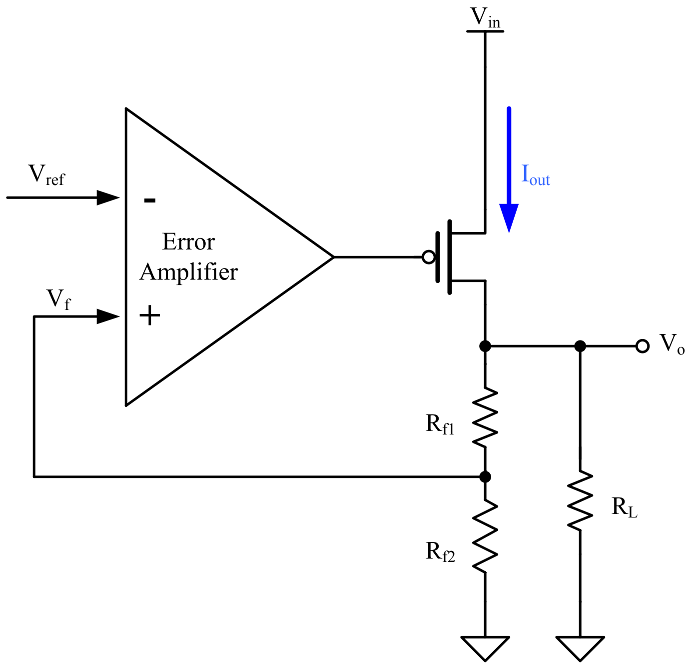

Fig. 2-6 PMOS type LDO linear regulator

2.2.5 Line Regulation

The line regulation is defined as the ability of LDO linear regulators resisting the variation of supply voltage which is expressed in Eq. 2-5 and depicted in Fig. 2-6, where R_{op} is the equivalent resistance of series pass transistor, R_{f1} and R_{f2} are the feedback resistors, A is the gain of error amplifier, R_L is the load resistor, g_{mp} is the transconductance of series pass transistor [16]. Like load regulation, the line regulation is also a steady-state parameter, that is, regardless of all frequency components.

$$\textit{Line regulation} = \frac{\Delta V_o}{\Delta V_{in}} \approx \frac{1}{R_L + R_{op}} \cdot \left(\frac{R_{f1} + R_{f2}}{g_{mp} R_{f2} A} \right) \qquad \text{Eq. 2-5}$$

According to Eq. 2-5, the same as the line regulation, it can be improved by increasing the loop gain of LDO linear regulators.

2.2.6 Power Supply Rejection

The power supply rejection is the ability of LDO linear regulators to prevent the regulated output voltage from fluctuations caused by the variations of input voltage. It is defined in Eq. 2-6 and Fig. 2-7. The quality of power supply rejection is mostly associated with the frequency response of closed-loop feedback system of LDO linear regulators. In general, power supply rejection is specified at 120 Hz, and its value is in the order of 60-80 dB depending on system requirement. However, the power supply rejection in the frequency band between 100 kHz and 1 MHz is especially important in the applications such as the output of a dc-to-dc switch mode power supply (SMPS) that is used to power the linear regulator [16].

$$Power\ supply\ rejection\ =\ \frac{Vo,\ ripple}{Vi,\ ripple}\ at\ all\ frequencies \qquad \text{Eq. 2-6}$$

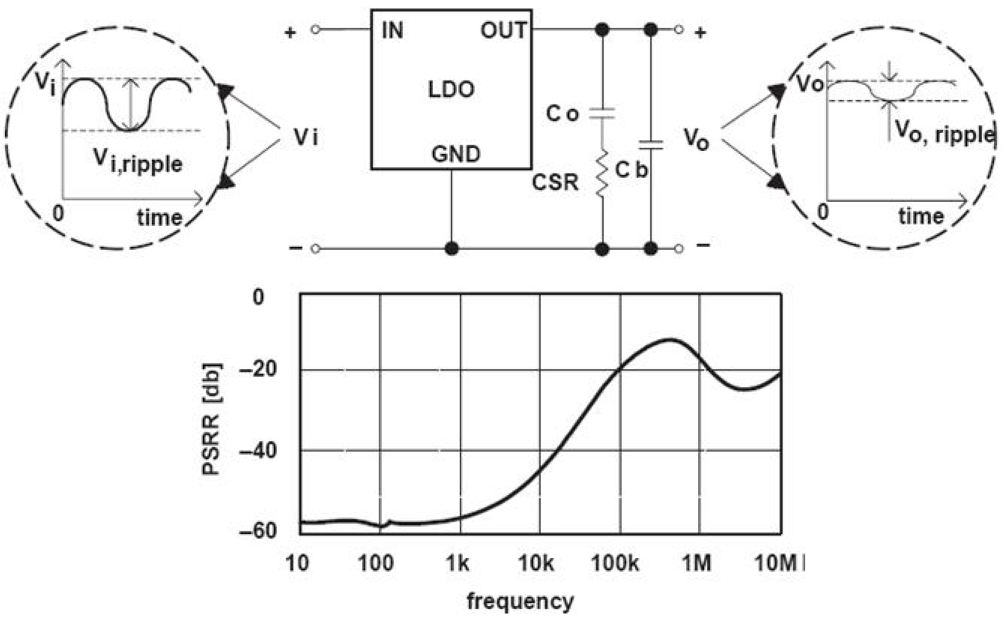

Fig. 2-7 Power supply rejection [16]

2.2.7 Output Noise

Output noise voltage is the RMS output noise voltage over a given range of frequencies between 10 Hz to 100 kHz as shown in Fig. 2-8 while the input voltage is ripple-free and the load current has no variation [16]. The source of noise output voltage is generated from the LDO linear regulator itself. Typical value of the output noise voltage is in the range of 50μV-500μV. The major output noise is caused by the internal voltage reference. In order to reduce these errors, there are several methods including adding an external bypass capacitor to the output of the reference voltage generator, or some signal processing techniques such as auto-zeroing [18], chopping techniques [19], and auto-calibration [20].

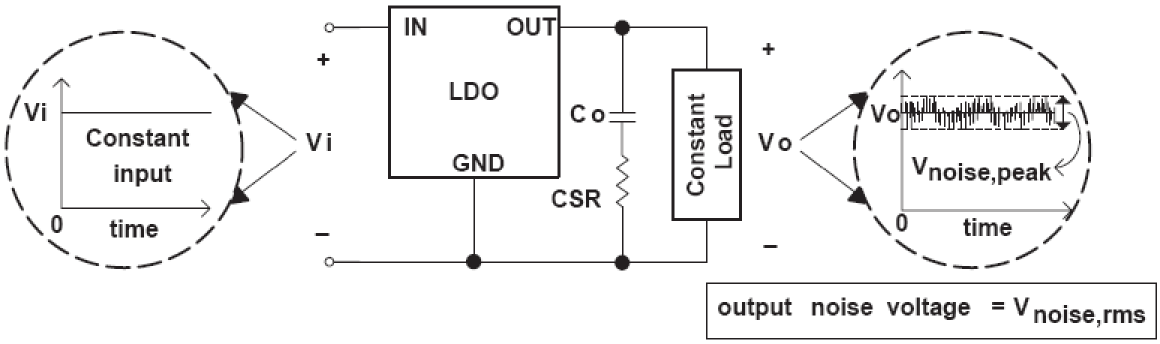

Fig. 2-8 Output noise voltage [16]

2.2.8 Stable Range of ESR

The stability and the transient response are greatly related to the equivalent series resistor (ESR) of the output capacitor. The manufacturers of LDO linear regulators usually provide a figure expressing the stable range of the output capacitor's equivalent series resistor as shown in Fig. 2-9 [16]. In Fig. 2-9, the curve shows that the value of the output capacitor's equivalent series resistor should be in the range between 9Ω and 0.01Ω.

Otherwise, the LDO linear regulator may be unstable.

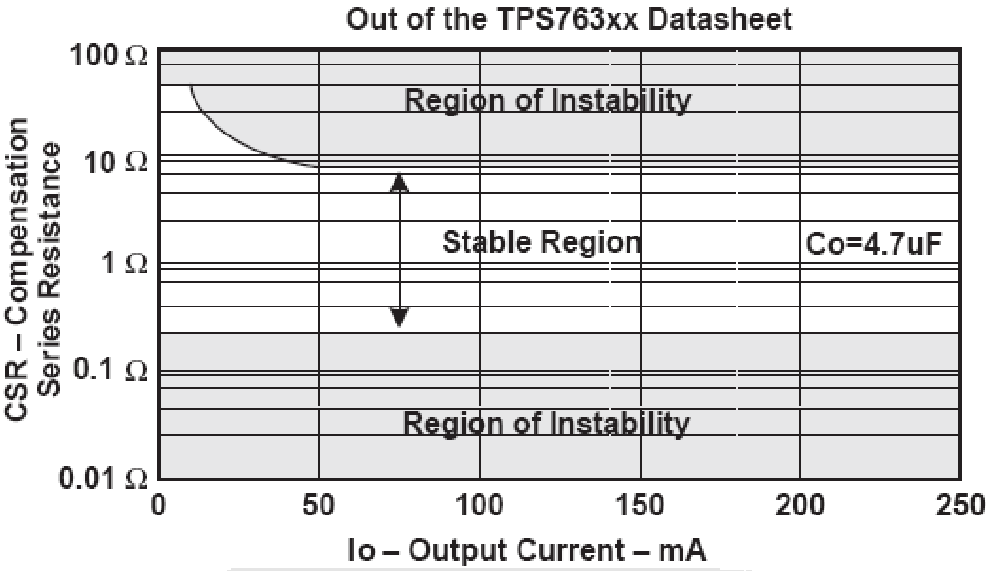

Fig. 2-9 Stable range of ESR [16]

2.2.9 Accuracy

The overall accuracy of the LDO linear regulators is greatly affected by many error sources, such as line regulation, load regulation, drift of the reference voltage, drift of the error amplifier, the tolerance of feedback resistors, and the temperature coefficients of feedback resistors. The accuracy is expressed in Eq. 2-7, where $\triangle V_{LR}$, $\triangle V_{LDR}$, $\triangle V_{o,ref}$, $\triangle V_{o,a}$, $\triangle V_{o,r}$, $\triangle V_{TC}$ are output voltage variations caused by finite line regulation, finite load regulation, drift of reference voltage, drift of error amplifier's output voltage, feedback resistors tolerance, and temperature coefficient, respectively [16].

$$Accuracy \approx \frac{|dV_{LR}| + |dV_{LDR}| + \sqrt{dV^2_{o,ref} + dV^2_{o,a} + dV^2_{o,r} + dV^2_{TC}}}{V_o} \times 100 \quad \text{Eq. 2-7}$$

Fig. 2-10 shows a LDO linear regulator which has tolerant feedback resistors and drift reference voltage, where $\triangle R_{f1}$ and $\triangle R_{f2}$ are tolerances of R_{f1} and R_{f2}, V_d is the drift of reference voltage, R_L is the load resistance.

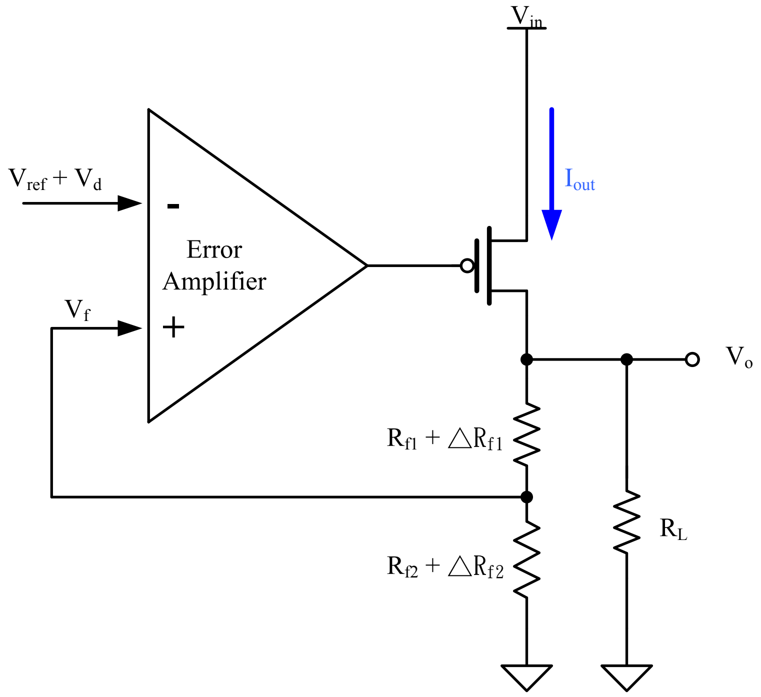

Fig. 2-10 A LDO linear regulator with offset feedback resistors and drifting reference voltage

2.2.10 Power Dissipation

One of the primary limitations of LDO linear regulator is the heat generated from the internally integrated circuits. While the heat rises, the temperature of chip also increases. Finally, the junction temperature may exceed maximum allowable junction temperature T_{jmax} which is set by the process and destroy the chip. The range of maximum junction temperature is between 150 and 170°C in CMOS technologies. For the sake of preventing the overhead of junction temperature, the heat generated from the internally integrated circuits should be expelled out from the chip through surrounding package to the ambient. And this will let the chip experience an increase in temperature with respect to ambient. The maximum allowable power dissipation of LDO linear regulator is restricted by thermal resistance between junction and ambience, and the allowable maximum junction temperature. The allowable power dissipation is expressed in Eq. 2-8, where T_{jmax} is the maximum allowable junction temperature, T_A is the temperature of ambient; θ_{JA} is the thermal resistance between junction and ambience [21].

$$Power\ dissipation(max) = \frac{T_{j\,\max} - T_A}{\theta_{JA}} \qquad \text{Eq. 2-8}$$

The thermal resistance θ_{JA} can be separated into two sub-thermal resistances as shown in Eq. 2-9, where θ_{JC} is the thermal resistance existing between junction and case, θ_{CA} is the thermal resistance existing between case and ambience.

$$\theta_{JA} = \theta_{JC} + \theta_{CA} \qquad \text{Eq. 2-9}$$

The junction-to-case thermal resistance is fixed and depends on devices' design, size and types of the package, and die size. The case-to-ambience thermal resistance is controllable by placing a suitable size of heatsink in contact with the package. A heatsink is constructed by metal material, usually with fins, clamped to the devices' package to facilitate heat flow from case to ambience. While a heatsink is applied, the thermal resistance existing between case and ambience can be expressed in Eq. 2-10, where θ_{CS} is the thermal resistance of the mounting surface, and θ_{SA} is the thermal resistance of the heatsink [21].

$$\theta_{CA} = \theta_{CS} + \theta_{SA} \qquad \text{Eq. 2-10}$$

The mounting surface is usually a thin insulating washer to provide electrical isolation between case and heatsink. The combination of the package and heatsink which is greatly adaptive to a given application is determined by allowable junction temperature, maximum expected power dissipation, and the maximum ambient temperature.

2.3 Design Issues of LDO

Although the architecture of LDO linear regulators is simple, there are several considerations and design issues in designing LDO linear regulators. Otherwise, it is most likely to get a LDO linear regulator which has unexpected characteristics, unsatisfied performance and unstable output voltage.

In this section, several design issues will be described: First one is different types of series pass transistor their characteristics, followed by the stability analysis. Finally, the transient response of LDO linear regulators will be presented.

2.3.1 Series Pass Devices Design Issues

There are a lot of options of series pass devices made with different technology process applied for LDO linear regulators, such as Bipolar, BiCMOS, or CMOS. These different types of series pass devices have their own characteristics, advantages and disadvantages [22]. With different types of series pass devices, the LDO linear regulators also have different qualities. The principle of selecting series pass devices is according to the application's specifications. The LDO linear regulators can be classified based on utilization of series pass devices, such as NPN-Darlington, NPN, PNP, PMOS and NMOS. Fig. 2-11 shows these five types of series pass devices topologies. The major comparison of these devices depends on two parameters: quiescent current and dropout voltage. Since the Bipolar-based series pass devices belong to the current-driven element, they can deliver a huge output current for the loading circuit. However, they also cause large quiescent current and decrease power efficiency. On the other hand, the MOS-based series pass devices belong to voltage-driven elements. This means their driving current is dependent on the gate voltage and not as large as Bipolar-based elements. But the quiescent current of the MOS-based devices is quite small, and makes regulators achieve high power efficiency.

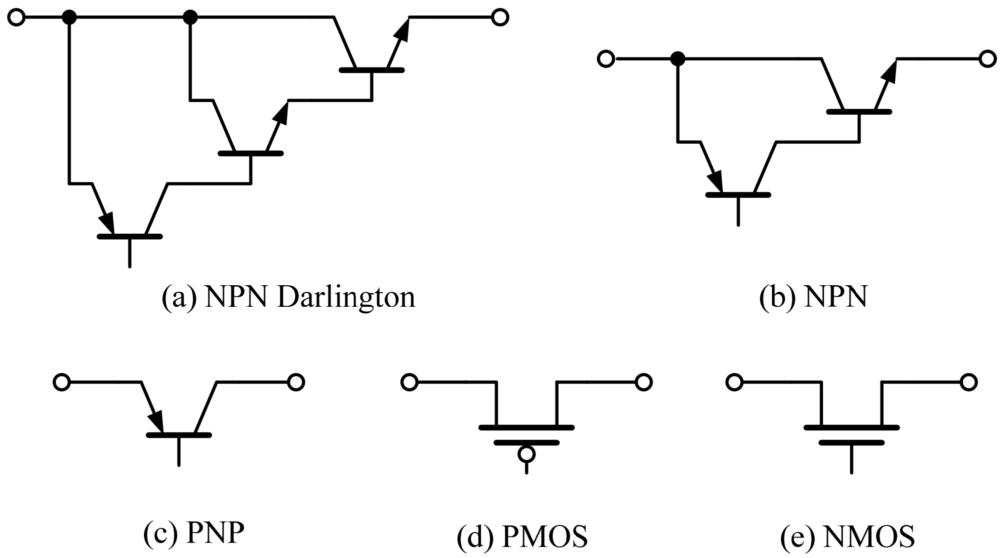

Fig. 2-11 Series pass devices topologies [22]

The LDO linear regulator which uses NPN Darlington-type series pass transistor, as shown in Fig. 2-11 (a), typically requires at least 1.6V of difference between input and output voltage. However, the LDO linear regulators usually operate under the condition which has only 0.5V difference between input and output voltage. The advantage of using NPN Darlington type series pass transistor is because of its high current gain. It needs less driving current than other Bipolar-based devices. The dropout voltage of LDO linear regulator with NPN Darlington type series pass transistor is shown in Eq. 2-11.

$$V_{drop}\ (NPN\ Darlington) = 2V_{BE} + V_{CE(SAT)} \cong 1.6 \sim 2.5\ V \quad \text{Eq. 2-11}$$

The NPN type series pass transistor is constructed by a single NPN transistor driven by a PNP transistor. It is very adaptive to the LDO linear regulators which convert from 5V to 3.3V [43]. The dropout voltage of LDO linear regulator with NPN type series pass transistor is shown in Eq. 2-12.

$$V_{drop}\ (NPN) = V_{BE} + V_{CE(SAT)} \geq 0.9V \quad \text{Eq. 2-12}$$

The PNP type series pass transistor is a single PNP transistor. Its major advantage is the small dropout voltage. The dropout voltage of LDO linear regulator with PNP type series pass transistor is shown in Eq. 2-13.

$$V_{drop}\ (PNP) = V_{CE(SAT)} \approx 0.1 \sim 0.4V \qquad \text{Eq. 2-13}$$

Fig. 2-11 (d), (e) show the NMOS and PMOS type series pass transistors. A lot of applications choose the LDO linear regulators with MOS-based series pass transistor because of the requirement of low quiescent current. The major advantage of the NMOS type series pass transistor is its low output resistance. This characteristic makes the output voltage of LDO linear regulator change slightly while the loading current is under variation. In addition, NMOS type LDO linear regulators have wider bandwidth and almost need no external component such as capacitor. But the NMOS-type series pass transistor has a disadvantage of high dropout voltage. Its dropout voltage is at least equal to or larger than one gate-to-source voltage V_{gs}. Besides, the body effect increases the threshold voltage of NMOS type series pass transistor, and make the dropout voltage to be larger [3]. An approach has been proposed to improve the high dropout voltage of NMOS type LDO linear regulators, that is, utilizes a charge pump to provide gate-voltage of NMOS type series pass transistor [15]. Since the charge pump can provide a gate-voltage which is larger than the supply voltage, it can decrease the dropout voltage of the NMOS type LDO linear regulator. However, using charge pump to generate a gate-voltage of NMOS type series pass transistor which is higher than supply voltage may raise reliability issues.

Fig. 2-12(a) shows a NMOS type linear regulator and Fig. 2-12(b) illustrates an improved one with charge pump to prove gate-voltage.

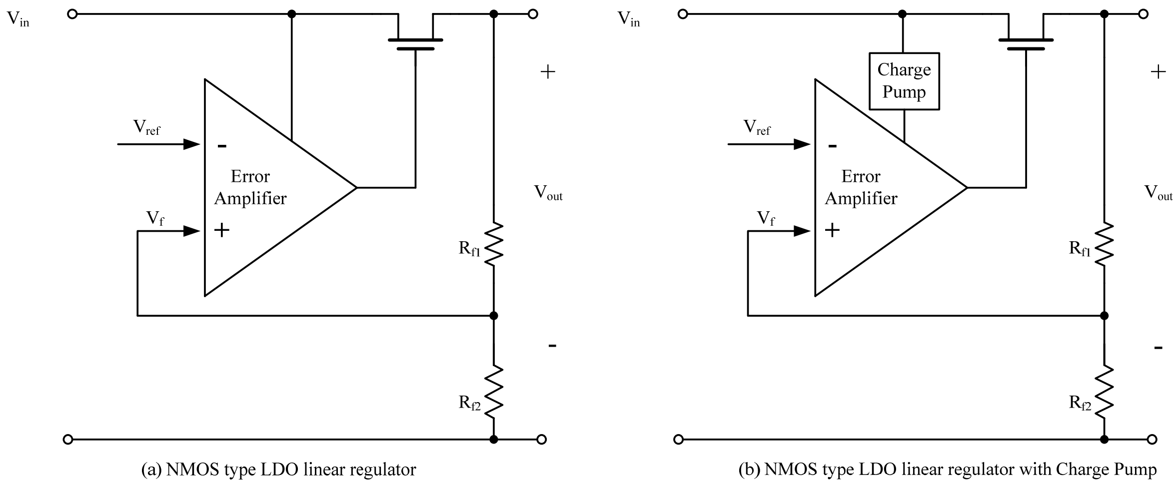

Fig. 2-12 (a) NMOS type LDO linear regulator (b) NMOS type LDO linear regulator with charge pump

The advantage of LDO linear regulators with PMOS type series pass transistor is its low dropout voltage, which is less than NMOS type LDO linear regulator without additional circuits like charge pump. The dropout voltage of the PMOS type LDO linear regulators is dependent on on-resistance of the PMOS type series pass transistor, which can be controlled by the size or the gate-driving voltage of the PMOS type series pass transistor. Eq. 2-14 expresses the dropout voltage of PMOS type series pass transistor.

$$V_{dropout} = I_o \times R_{ON} \qquad \text{Eq. 2-14}$$

PMOS type LDO linear regulators generally suffer from stability problems caused by two low-frequency poles which are located at the gate of PMOS series pass transistor and the output of LDO linear regulator. For this reason, they typically need an external output capacitor which has large capacitance with equivalent series resistor to enhance the stability. Fig. 2-13 shows a PMOS type LDO linear regulator which has output capacitor C_L and equivalent series resistor R_{esr}.

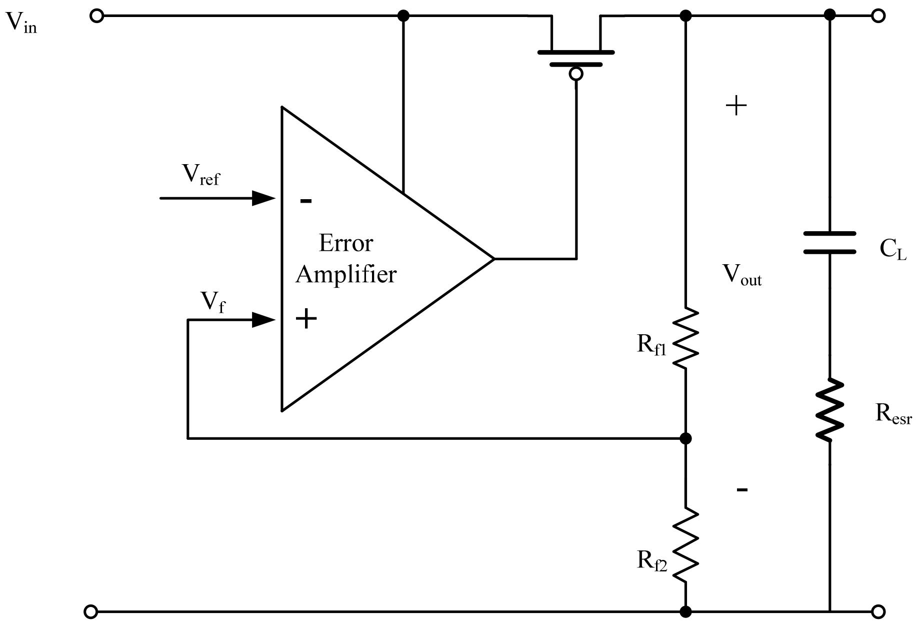

Fig. 2-13 PMOS type LDO linear regulator

In this thesis, the PMOS type series pass transistor is adopted for the design of adjustable linear regulators. It is because the PMOS type series pass transistor has the characteristic of low dropout voltage without charge pump which may have reliability problem as well as the increase in quiescent current. Table 2-1 shows the comparison of several characteristics of different type series pass devices [17].

Parameter	Darlington	NPN	PNP	NMOS	PMOS
Output Current	High	High	High	Medium	Medium
Quiescent Current	Medium	Medium	Large	Low	Low
Dropout Voltage	Vce(sat)+2Vbe	Vce(sat)+Vbe	Vce(sat)	Vds(sat)+Vgs	VSD(sat)
Speed	Fast	Fast	Slow	Medium	Medium

Table 2-1 Comparison of series pass devices

2.3.2 Frequency Response Design Issues

As mentioned in previous section, the PMOS type LDO linear regulators have essential problems of stability. It is because that there are two low-frequency poles which are generated from the output-node of LDO linear regulators and the gate-node of PMOS type series pass transistor. So these LDO linear regulators need the external output capacitor to enhance the stability. Fig. 2-14 shows the small signal model of a PMOS type LDO linear regulator. In the following, a number of analyses and calculations are discussed.

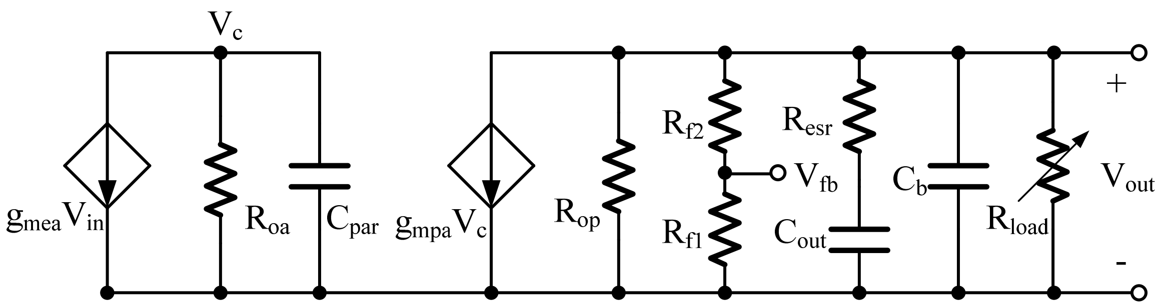

Fig. 2-14 Small signal model of the PMOS type LDO linear regulator

The open loop gain is calculated as Eq. 2-15, where g_{mea} and g_{mpa} are the transconductance of the error amplifier and the output series pass transistor respectively, C_{par} is the parasitic capacitance of the output node of the error amplifier, R_{oa} is the output resistance of the error amplifier, R_{f1} and R_{f2} are feedback resistors.

$$A_f(a) = \frac{V_{fb}}{V_{in}} = g_{mea} \times \left[R_{oa} \, // \, \frac{1}{sC_{par}} \right] \times g_{mpa} \times \frac{R_{f1}}{R_{f1} + R_{f2}} \times Z_{out} \qquad \text{Eq. 2-15}$$

And Z_{out} is expressed in Eq. 2-16, where R_{op} is the on-resistance of the series pass transistor, C_{out} is the external capacitor, R_{esr} is the equivalent series resistors of C_{out}, C_b is the bypass capacitor.

$$Z_{out} = R_{op} \, // \, \frac{1}{sC_b} \, // \left(\frac{1}{sC_{out}} + R_{esr} \right) // \left(R_{f1} + R_{f2} \right) \qquad \text{Eq. 2-16}$$

In general, the value of feedback resistors is very large in order to cease leakage current, and the value of equivalent series resistor is very low. So the Z_{out} can be calculated as Eq. 2-17 in the assumption of $R_{esr} << R_{op} << R_{load}$, $R_{op} << (R_{f1} + R_{f2})$.

$$Z_{out} \approx \frac{R_{op} \times (1 + sC_{out} \times R_{esr})}{(1 + s \times (R_{op} \times C_{out})) \times (1 + sR_{esr} \times C_b)} \qquad \text{Eq. 2-17}$$

According to Eq. 2-15, Eq. 2-16, and Eq. 2-17, there are three poles and one zero inside the transfer function of open loop gain [24]. These three poles and one zero are expressed in Eq. 2-18, Eq. 2-19, Eq. 2-20, and Eq. 2-21, where λ is the parameter of channel-length modulation, I_{out} is the current through the series pass transistor.

$$f_{p1} \approx \frac{1}{2\pi \cdot R_{OT} \cdot C_{out}} \cong \frac{\lambda \cdot I_{out}}{2\pi \cdot C_{out}} \qquad \text{Eq. 2-18}$$

$$f_{p2} \approx \frac{1}{2\pi \cdot R_{g2} \cdot C_{OT}} \qquad \text{Eq. 2-19}$$

$$f_{p3} \approx \frac{1}{2\pi \cdot R_{g1} \cdot C_{g2}} \qquad \text{Eq. 2-20}$$

$$f_{z1} \approx \frac{1}{2\pi \cdot R_{esr} \cdot C_{out}} \qquad \text{Eq. 2-21}$$

Since the dominant pole f_{p1} and the second-dominant pole f_{p2} are located at low frequency, the phase margin is not big enough. For the purpose of increasing the phase margin, the location of the zero should be placed near the second-dominant pole f_{p2} for achieving pole-zero cancellation. And the third pole f_{p3} should be placed after the unity-gain frequency of loop response.

As shown in Eq. 2-18, the location of the dominant pole f_{p1} is not fixed. It is dependent on the loading current. While the loading current is small, the dominant pole will stay at low frequency. But after the increase of loading current, the dominant pole is pushed to a high frequency, and the other poles still stay in the original location. It means the phase margin will shrink while the loading current is increasing. This causes the LDO liner regulator to be unstable. Fig. 2-15 shows a typical frequency response of LDO linear regulators under different loading current levels. The blue (dotted) line is the frequency response of loop gain under small loading current, and the green line is the frequency response of loop gain under large loading current. The distance between f_{p1} and f_{p1}' is dependent on the range of the loading current.

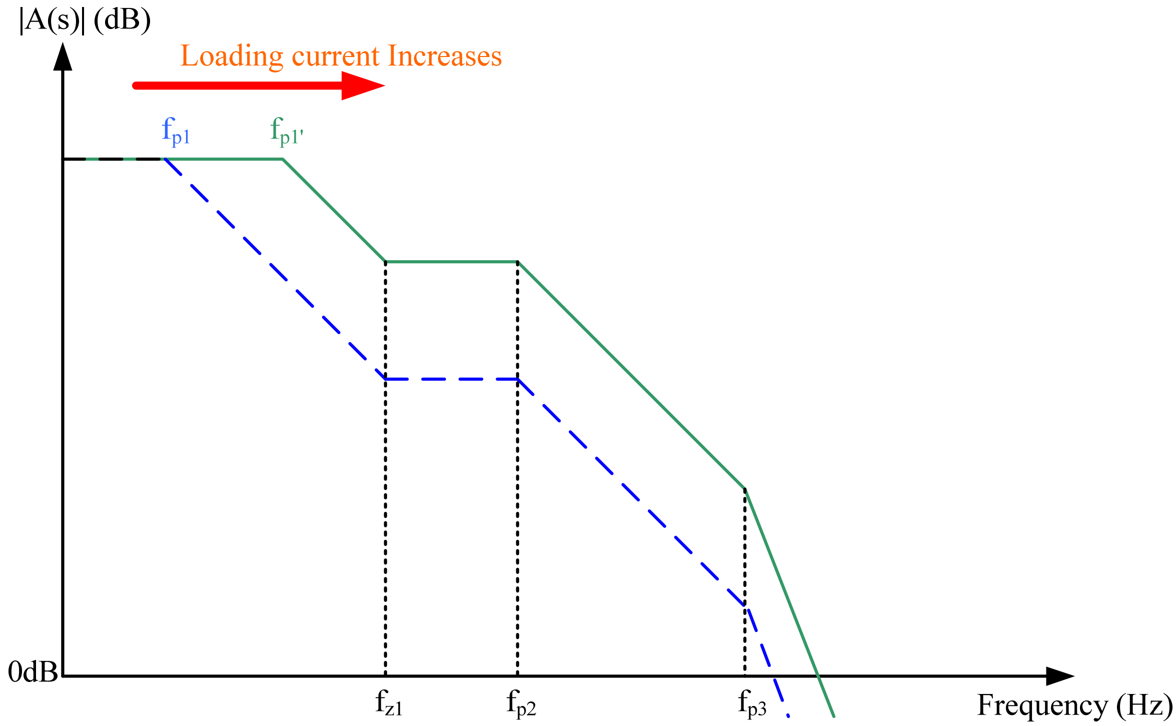

Fig. 2-15 LDO linear regulator's frequency response under two different loading current levels

2.3.3 Transient Response Design Issues

The transient response is a very important factor, which is specified as the maximum allowable output voltage variation for a sudden step-change of the load current. Digital systems usually have multiple operation modes. While switching from one mode to another mode, a temporary glitch may appear at the output of the LDO linear regulators resulting in the loop response delay. In general, most digital circuits do not accept high amount of the temporary glitch. This glitch may cause the digital circuits enter unexpected state and get functional error [25]. For this reason, many applications specify the limitation about the amount of overshoot and undershoot at the output voltage of LDO linear regulators. Fig. 2-16 shows the transient response of typical LDO linear regulators, and Fig. 2-17 shows a typical block diagram of a PMOS type LDO linear regulator. In the following, the analyses of transient response according to Fig. 2-16 and Fig. 2-17 are discussed.

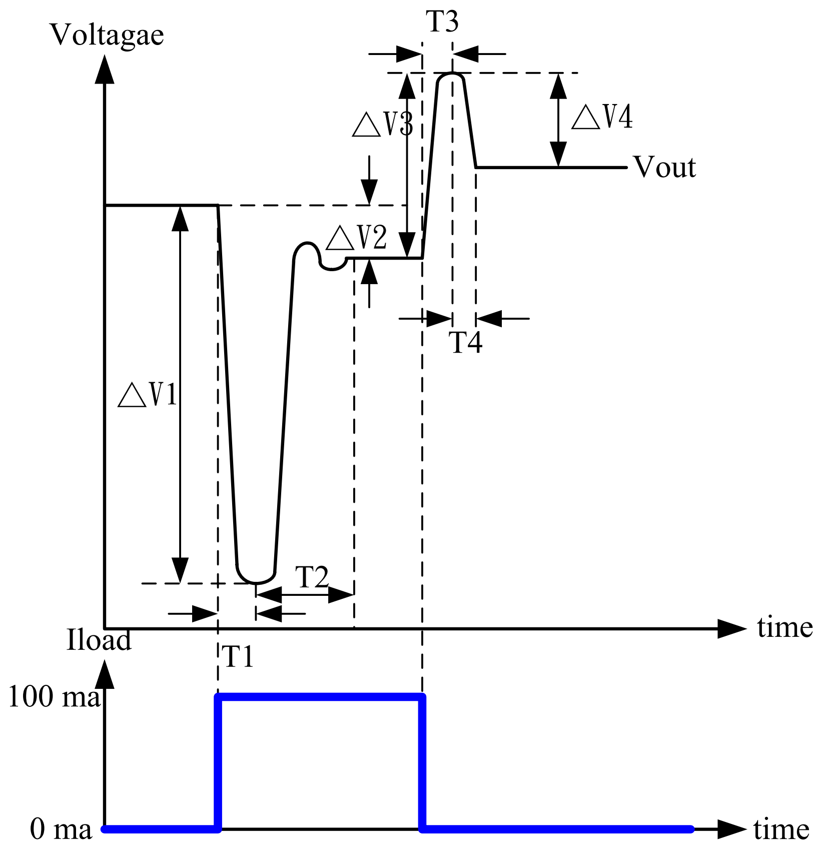

Fig. 2-16 Transient Response of LDO linear regulators under a sudden step-change of load current

During the time interval T1, where the loading current has a step-rising, most of the load current is provided by the output capacitor. It is because of limited bandwidth of LDO linear regulators and the feedback loop can not work in time. The transient voltage variation (undershoot) △V1 is described in Eq. 2-22, where T1 is related to closed-loop bandwidth and the output slew rate current of the error amplifier [26], C_{out} is the output capacitor, C_b is the bypass capacitor which is used to eliminate the high frequency noise for the loading circuit, and $\triangle V_{esr}$ is the output voltage variation due to the presence of equivalent series resistor R_{esr} which is generated from the output capacitor C_{out}.

$$\Delta V1 \approx \frac{I_{max}}{C_{out} + C_b} \cdot T1 + \Delta V_{esr} \qquad \text{Eq. 2-22}$$

During the time interval T2, the feedback loop begins to work properly. The output voltage of LDO linear regulators begin to increase and settle to its final stable voltage level, where $\triangle V2$ is the difference between the output voltage under small loading current and that under large loading current. The final settling voltage is associated with the load regulation of the LDO linear regulators, and the time interval T2 is mostly dependent on the speed of the series pass transistor fully charging the output capacitor and the phase margin of the feedback loop. While the load current has a suddenly step-falling, the feedback loop also can not respond in time. So the series pass transistor still charges the output capacitor and results in an overshoot variation at the output voltage of LDO linear regulators. The transient output voltage variation (overshoot) $\triangle V3$ is described in Eq. 2-23, where the time interval T3 is related to the closed-loop bandwidth and the output slew rate current of the error amplifier.

$$\Delta V3 \approx \frac{I_{max}}{C_{out} + C_b} \cdot T3 + \Delta V_{esr} \qquad \text{Eq. 2-23}$$

During the time interval T4, the output voltage of LDO linear regulators begins to settle to its final stable voltage level. The time interval T4 is dependent on the current through the feedback resistors and the output capacitor. It can be expressed in Eq. 2-24.

$$T4 \approx \frac{C_{out} + C_b}{V_{ref}} \left(R_{f2} \right) \cdot \Delta V4 \qquad \text{Eq. 2-24}$$

According to Eq. 2-24, the time interval T4 is mainly dependent on the value of feedback resistance R_{f1}, R_{f2} and output capacitor C_{out}. However, the values of the feedback resistors are usually very large in order to cease the leakage current flowing through them. In addition, the value of output capacitor is also very large in order to maintain the stability of LDO linear regulators and reduce the amount of overshoot and undershoot at the output voltage. Consequently, in the traditional design of LDO linear regulators, the time interval T4 is significantly larger than T2. In other words, the operation of discharging the output voltage needs more time than the operation of charging the output voltage.

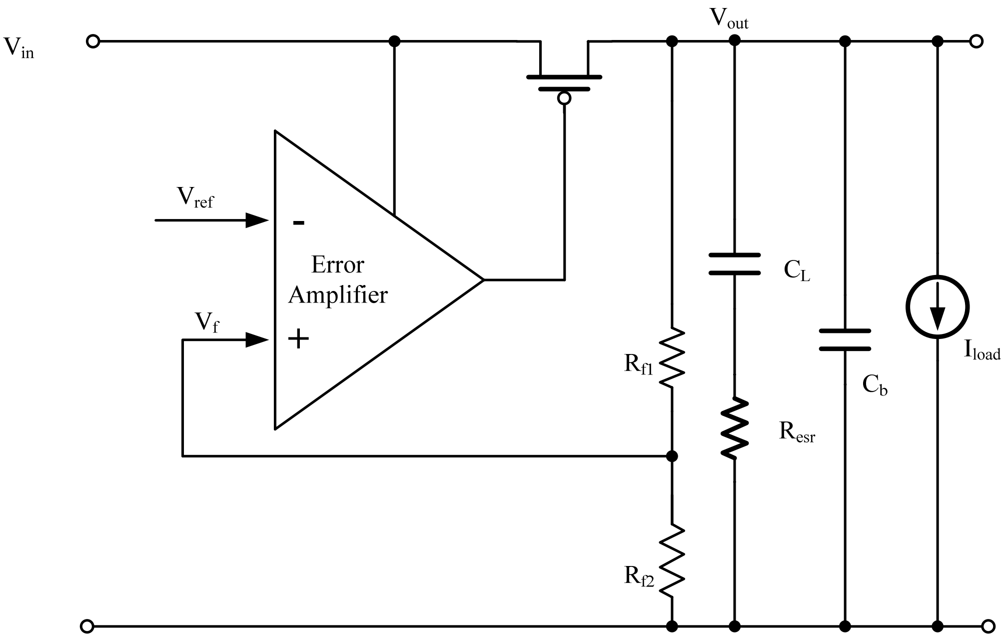

Fig. 2-17 Typical block diagram of a PMOS type LDO linear regulator

Chapter 3

Structure Analysis of Adjustable LDO Linear Regulators

To ease the needs of energy-efficient SOC, components in SOC may be designed with several operation modes. Hence, each component may need several supply voltages at different operation mode, and the chip becomes to a multi-supply system. In this situation, designers may use several LDO linear regulators to provide different DC voltages to satisfy each component which has more than one operation mode. As the size of components shrink a lot of amount, the number of components included in a system increases. If a component needs more than two supply voltages, the designer should pick up two proper LDO linear regulators to feed the component and design an extra control unit or an interface for efficiently controlling these LDO linear regulators. Consequently, the multi-supply system will require many LDO linear regulators to support all of the components which have more than one operation mode, especially in the future. Therefore, approaches to prevent the overhead of power consumption and PCB area resulted from LDO linear regulators should be solved.

Although the easiest way is to spend effort in reducing the area of LDO linear regulators, it can not solve the problem efficiently. It is because the area of LDO linear regulators is mainly dependent on the series pass transistor, which is responsible to provide the load current. Since the component is very complex and multi-functional, it must need a large driving current for the operation. So the area of one single LDO linear regulator can not be shrunk too much because of the requirement of the component's driving current. Furthermore, designers of multi-supply system may not be familiar with the characteristics of LDO linear regulators, it is not suitable for designers to waste time in designing an extra control unit or an interface, which is used for integrating and controlling several LDO linear regulators to provide required internal voltages for different operation modes of the component.

For the sake of preventing from the excessive area and power resulted from LDO linear regulators, it is necessary to design a new type LDO linear regulator which can generate more than one stable output voltage. Moreover, the new type LDO linear regulator should have an internal control unit to effectively select the expected internal voltage without perplexing the system designers. This kind of LDO linear regulators is called adjustable LDO linear regulators.

In the following, we classify four different possible methods to design an adjustable voltage regulator. Each of them has its own advantages and disadvantages based on their structures.

3.1 Duplication type Adjustable LDO linear regulators

The first structure of the adjustable LDO linear regulator is called duplication type adjustable LDO linear regulator (DP-ALDO). As shown in Fig. 3-1, this structure is composed of a multiplexer MUX and three LDO linear regulators, where Vref1, Vref2, Vref3 circuits are different specified reference voltage generators, and series regulator1, series regulator2, series regulator3 are composed of different error amplifiers and series pass transistors respectively. Since these three LDO linear regulators have complete structure and are independent to each other, they can have different specified output voltages and characteristics, such as dropout voltage, quiescent current, transient response, power efficiency, accuracy, and etc. And the characteristics of these LDO linear regulators are dependent on the requirement of applications. The operation of this adjustable LDO linear regulator is described as follows. The external supply voltage is used to drive the LDO linear regulators, and the multiplexer. Then the output voltages of LDO linear regulators are transferred to the input of the multiplexer whose select signal is connected to the external control signal and controlled by the system designer or power management units. The expected output voltage of certain LDO linear regulator can be selected by the multiplexer and then transfer to the load circuit.

This type of adjustable LDO linear regulator is quite simple for the designer to realize. Because LDO linear regulators utilized in the adjustable LDO linear regulator are independent to each other and their qualities can be decided by designer according to the requirement of applications. However, this kind of adjustable linear regulator has its drawbacks. The power and the area of this adjustable LDO linear regulator are still related to the number of LDO linear regulators. Although this method is simple, it is not an efficiently way to deign an adjustable LDO linear regulator with low power and small area.

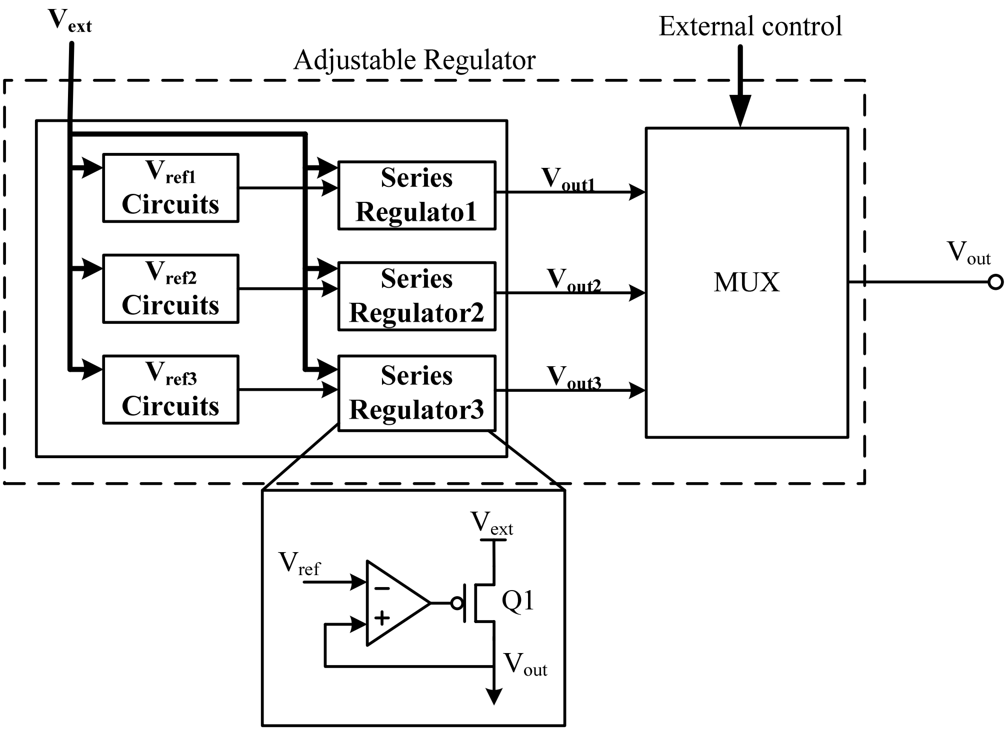

Fig. 3-1 Block diagram of a duplication type adjustable LDO regulator (DP-ALDO)

3.2 Half-Duplication type LDO linear regulators

From the previous discussion, it is necessary to be sure that, the power consumption and area cost of an adjustable LDO liner regulator that is capable of providing N output voltages, should be less than the sum of power consumption and area cost of N LDO linear regulators. In Eq. 3-1 and Eq. 3-2 show the constraints of the method designing an adjustable LDO linear regulator, where ALDO means Adjustable LDO linear regulators.

$$Power\ (ALDO\ \text{- -}N\ output\ voltages) \leq \sum_{N} Power\ (LDO\ \text{- -}\ one\ output\ voltages) \qquad \text{Eq. 3-1}$$

$$Area\ (ALDO\ \text{- -}N\ output\ voltages) \leq \sum_{N} Area\ (LDO\ \text{- -}\ one\ output\ voltages) \qquad \text{Eq. 3-2}$$

The second structure of the adjustable LDO linear regulator is called half duplication type adjustable LDO linear regulator (HDP-ALDO). It is derived from the first structure and it is shown in Fig. 3-2. For the sake of saving the power consumption and area cost of adjustable LDO linear regulators, the second structure integrates three series regulators into one but keeps the number of reference voltage generator the same. A multiplexer is utilized to select expected reference voltage and transfer it to the series regulator. As mentioned earlier, most area is cost by the series pass transistor of LDO linear regulators, which is mainly dependent on the requirement of Load current. Therefore, the second structure of adjustable LDO linear regulator greatly reduces the area of adjustable LDO linear regulator. However, the power consumption is not reduced very much when compensating to that of the first structure. It is mainly due to the quiescent current by the reference voltage generators. As one can observe that the second structure is still keep using numbers of reference voltage generators.

Although the second structure has smaller area than the first structure, its complexity of the design is not as simple as the first one. In the first structure, several LDO linear regulators have their own structure and are independent to each other. But the second structure has only one series regulator, and the series regulator is needed to be shared with different reference voltage generators. In other words, the series regulator should be adaptive to not only single reference voltage generator but also many. There is a common quality between the first and the second structure. That is, both of them use the duplicated structure of complete or partial LDO linear regulators. While the requirement of output voltage's number increases, they also need to add more duplicate structure of partial or completer LDO linear regulators. As mentioned in the previous section, the second structure reduces greatly area cost by merging numbers of series regulators to only one. But the power consumption of the second structure does not improved too much. It is because the number of reference voltage generators inside the first structure is sill the same as the first structure.

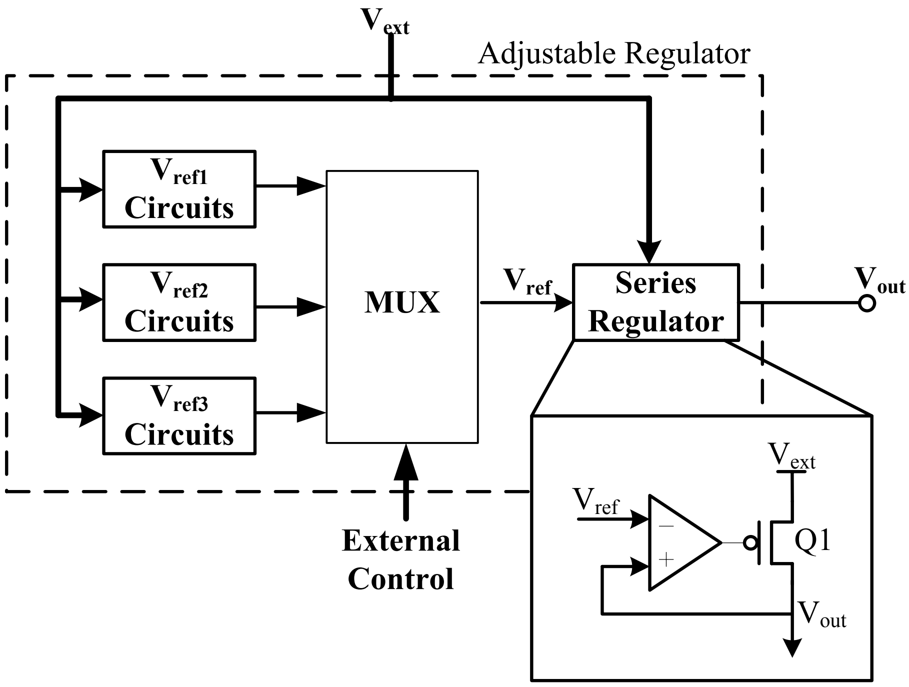

Fig. 3-2 Block diagram of a half duplication type adjustable LDO regulator (HDP-ALDO)

In the following, the third and the fourth structure, which use only one single structure of the LDO linear regulator, are described in next two sections.

3.3 Adjustable Feedback path type Adjustable LDO linear regulators

The third structure is called adjustable feedback path type adjustable LDO linear regulator (AFP-ALDO). It is improved from a simple LDO linear regulator as shown in Fig. 3-3 [27]. Most components of the third structure are the same as a simple LDO linear regulator, such as the error amplifier, the series pass transistor, and the reference voltage generator. The only different part is the feedback resistors which are programmable in the third structures. The operation of the third structure is described in the following. As the same as the traditional LDO linear regulators, the output voltage is associated with the reference voltage Vref and the feedback resistors R_a and R_b as shown in Eq. 3-3.

$$V_{out} = V_{ref} \times \frac{R_a + R_b}{R_b},\ R_a = R_{f1} + R_{f2}\ or\ R_{f2} \qquad \text{Eq. 3-3}$$

While the external control signal is set to low, the MCL transistor is turned off. It means the feedback transistor R_a is equal to R_{f1} + R_{f2}, and the output voltage of the adjustable LDO linear regulator is expressed in Eq. 3-4.

$$V_{out\ (MCL\ =\ OFF;\ R_a\ =\ (R_{f1}\ +\ R_{f2}))} = V_{ref} \times \frac{(R_{f1} + R_{f2}) + R_b}{R_b} \qquad \text{Eq. 3-4}$$

As the external control signal changes to high, the MCL transistor is turned on. Then the feedback transistor R_a is equal to R_{f2} because the MCL transistor acts as a short path and makes the feedback resistor R_{f2} to be ignored. The output voltage of the adjustable LDO linear regulator is presented in Eq. 3-5.

$$V_{out\ (MCL\ =\ ON;\ R_a\ =\ R_{f2})} = V_{ref} \times \frac{R_{f2} + R_b}{R_b} \qquad \text{Eq. 3-5}$$

According to Eq. 3-4 and Eq. 3-5, the output voltage is mainly controlled by the external control signal through MCL transistor. As the MCL transistor is turned off, the adjustable LDO linear regulator is set to a higher output voltage. On the other hand, the adjustable LDO linear regulator is changed to a lower output voltage while the MCL transistor is turned on.

Obviously, this structure is better than the first and the second structure in power consumption and area. It is because the third structure is quite similar to the traditional LDO linear regulators. The only different part is the extra resistor and the MCL transistor. While the number of output voltage needs to increase, it only needs to add extra resistors and MCL transistors. In general, the third structure is better than the first and the second one. It is because the third structure has smaller power consumption and area than the first and the second structure. But the value of extra feedback resistor is still needed to be concerned. Since the value of feedback resistors is usually designed with large value to suppress leakage current, the size of feedback resistors and extra feedback resistors are also very big. With the number of output voltage increases, the adjustable LDO linear regulator needs more extra feedback resistors and cost more area. For example, assume the value of resistor R_b is equal to 90kΩ, the reference voltage is 0.9V and the expected output voltages are 2.5V and 1V respectively. According to Eq. 3-3 ~ Eq. 3-5, the resistors R_{f1} and R_{f2} should be set to 150kΩ and 10k. As the number of expected output voltage or the value of expected output voltages increases, the value of feedback resistors also increases. Therefore, the extendibility to have more output voltages is still limited greatly by the area of feedback resistors.

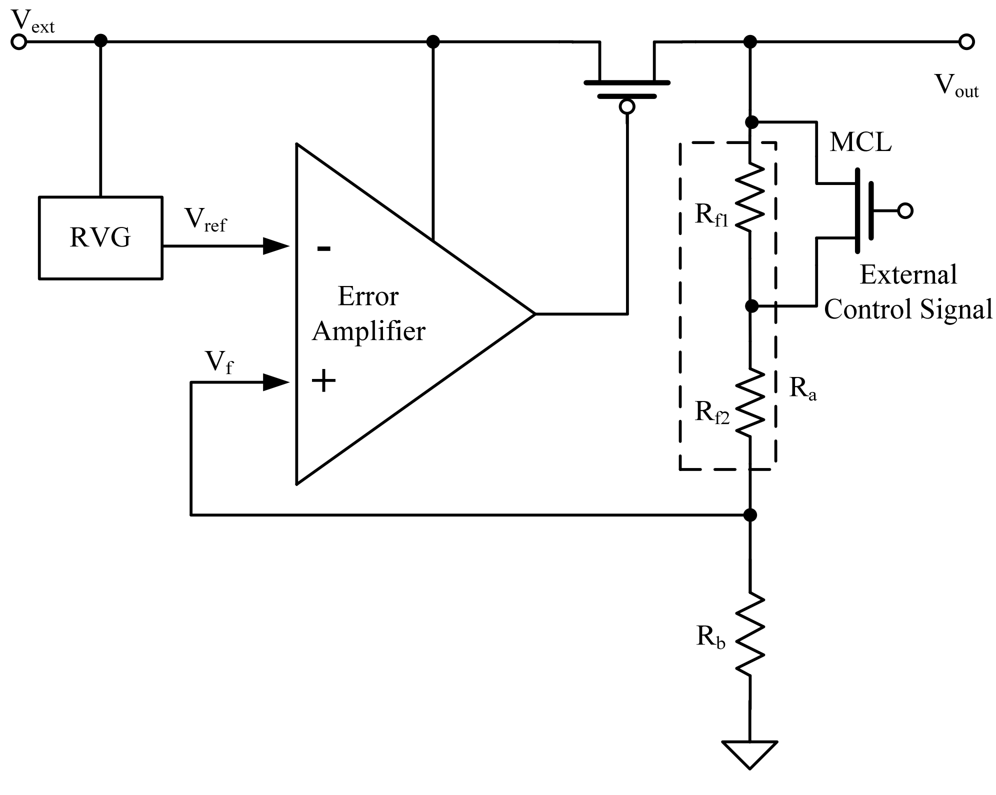

Fig. 3-3 Block diagram of an adjustable feedback path type adjustable LDO linear regulator (AFP-ALDO)

3.4 Adjustable Reference Voltage Generator type LDO linear regulators

The fourth structure called adjustable reference voltage generator type LDO linear regulator (ARVG-ALDO) is similar to the third one. The difference is in the reference voltage generator as shown in Fig. 3-4, not in the feedback network. In the second structure, it uses several reference voltage generators and a multiplexer to provide expected reference voltage and transfers it to the series regulator. The fourth structure tries to integrate these reference voltage generators into one and combine it with the multiplexer. In other words, the fourth method is to develop an adjustable reference voltage generator capable of generating more than one stable reference voltages [30]. Then the designer have to design the adaptive error amplifier, series pass transistor, feedback network, and etc, to incorporate with it. The major design limitation of an adjustable reference voltage generator capable of providing N-output voltages is that its power consumption and area cost should not exceed the sum of the power consumption and the area cost of N traditional single output reference voltage generator as expressed in Eq. 3-6 and Eq. 3-7.

$$Power\ (ARVG\ \text{--}\ generates\ N\ Vref) \leq \sum_{N} Power\ (Traditional\ RVG\ \text{--}\ single\ output) \qquad \text{Eq. 3-6}$$

$$Area\ (ARVG\ \text{--}\ generates\ N\ Vref) \leq \sum_{N} Area\ (Traditional\ RVG\ \text{--}\ single\ output) \qquad \text{Eq. 3-7}$$

According to Eq. 3-6 and Eq. 3-7, it is necessary to figure out a method to integrate numbers of reference voltage generators such as merging the bias circuits of them, and etc. It shall be noted that one need to guarantee the stability of reference voltages.

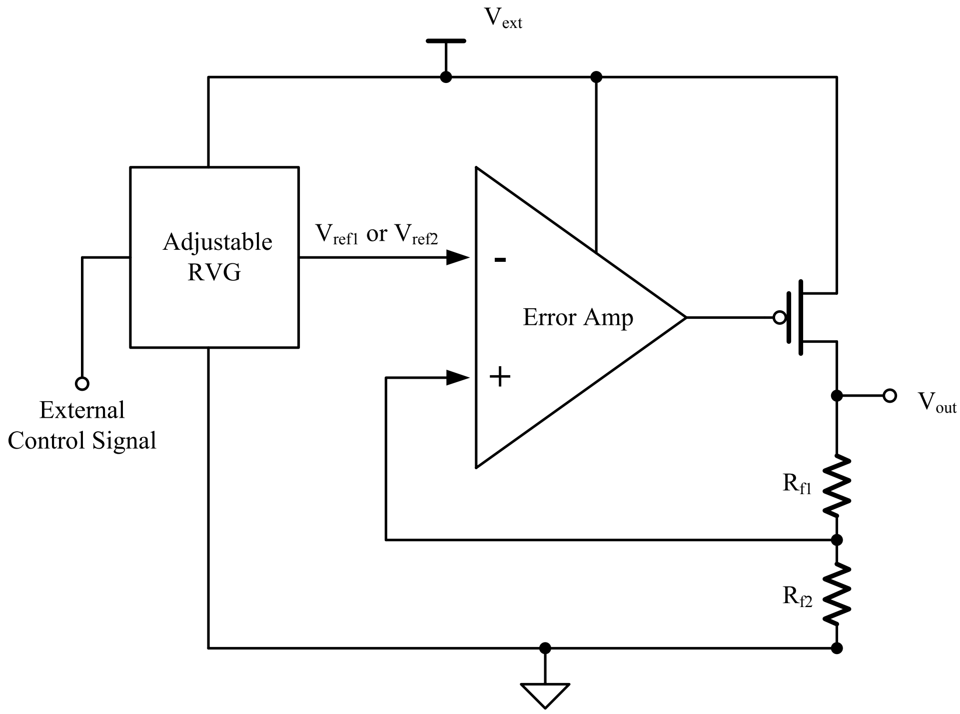

Fig. 3-4 Block diagram of an adjustable reference voltage generator type LDO linear regulator (ARVG-ALDO)

3.5 Summary

In this section, we compare differences of different structures and summarized in Table 3-1. The compared parameter includes area and the power consumption of these structures, design complexity of them, and the extendibility. The design complexity means how much time the designer has to spend on realizing the structure, and the extendibility reveals the possibility of increasing the number of output voltage.

Since the first structure uses independent LDO linear regulators with multiplexer, it is easily realized without worrying about the interference between LDO linear regulators. However, this structure's power consumption and area of this structure are very large. So the extension of this structure is not very well resulted from the consideration of power and area. The second structure is more extendable than the first structure because of its less area coast. But the design complexity is not simpler than the first one. It is because the designer has to worry about the design of the error amplifier, series pass transistor, and the feedback resistors in order to make them adaptive to all of the reference voltage generators. The third and the forth structure are quite similar. Both of them are developed by improving a single traditional LDO linear regulator, and their power consumption and area are extremely less than the first and the second structure. Therefore, the extendibility of them is better than the first and the second structure. But the third structure uses extra feedback resistors, which are designed with very large value for reducing leakage current, to derive other output voltages. Hence the third structure has a larger area cost than the fourth one.

It shall be noted that the power consumption and area of the forth structure still depend on the number of output voltage. For increasing the extendibility of the fourth structure, it is necessary to design an adjustable reference voltage generator with low power, low area, and high stability. In this thesis, a new adjustable reference voltage generator is proposed to overcome these problems. By using our proposed adjustable reference voltage generator, it has better extendibility with smaller power consumption and area.

Parameter	DP-ALDO	HDP-ALDO	AFP-ALDO	ARVG-ALDO
Area	Very Large	Large	Medium	Small
Power	Very Large	Very Large	Small	Small
Design complexity	Simple	Normal	Hard	Hard
Extendibility	Very Hard	Hard	Simple	Simple

Table 3-1 Compared result between four different structures

Chapter 4

Proposed adjustable LDO linear regulator

In this chapter, a new adjustable reference voltage generator is proposed to construct the adjustable LDO linear regulator. In addition, for the sake of improving the transient response, a dynamic discharging path is designed to speed up the recovering time. In the following paragraphs, the structures of the traditional reference voltage generator are discussed firstly. Following that, the proposed adjustable voltage generator is presented. Finally, the design of a two-stage error amplifier and the dynamic discharging path are presented.

4.1 Structure of Reference Voltage Generators

The function of Reference Voltage Generator is to generate a stable reference voltage capable of resisting the supply voltage [33] and the temperature variation [31][32]. There are numbers methods to construct reference voltage generators. In general, a bandgap voltage reference [28], which can be implemented by using parasitic vertical bipolar-transistors in standard CMOS technology [37], is utilized because of its low temperature-dependence [34]. Fig. 4-1 shows a conceptual block diagram of bandgap references [29]. Since the bias sources referenced to the base-to-emitter voltage V_{BE} (on) and the thermal voltage V_t have opposite temperature coefficient, the output voltage V_{out} can be deigned to achieve almost zero temperature coefficient through properly weighting. However, the CMOS technology has become the mainstream in circuit design due to its relatively low fabrication cost and PCB layout area. Besides, the bandgap voltage reference which uses parasitic bipolar-transistors results in substrate current injection [38]. In some applications, such as DRAM, the substrate is pumped to a negative voltage. The substrate current caused by the bandgap voltage reference will make the charge-pump continuously running and bring out unwanted power dissipation.

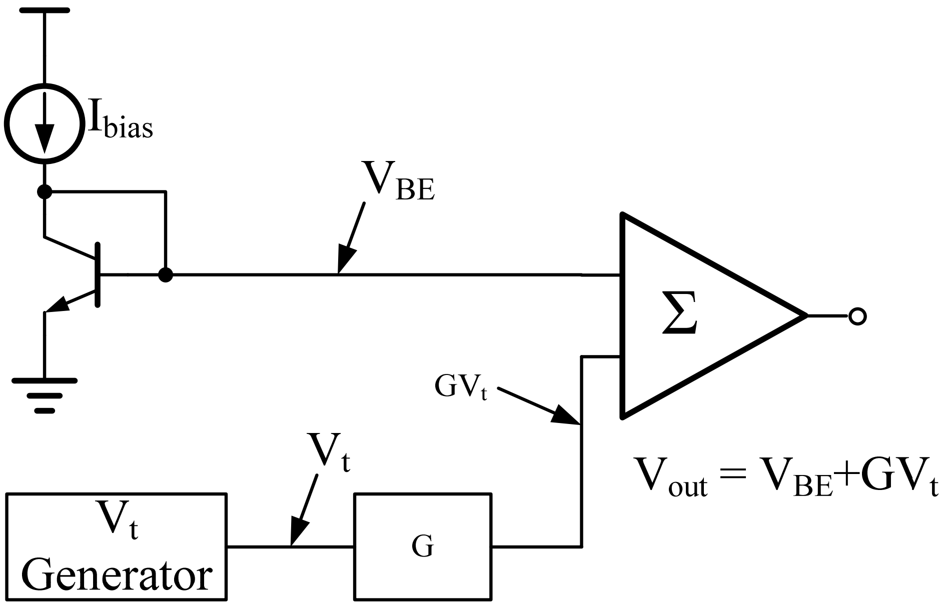

Fig. 4-1 Conceptual block diagram of bandgap references [29]

There is an alternative way to realize the reference voltage generator. That is a CMOS technology voltage reference, which is based on the difference of threshold voltages derived from enhancement and depletion transistors [36], or Ion-Implanted transistors [35]. Moreover, the difference of thresholds voltage can be designed according to the flat-band voltage difference with different gate materials [39], and work-function difference with different gate dopings [40]. However, these solutions proposed above are not applicable in standard low-cost CMOS technologies since additional fabrication steps are needed. Therefore, another structure called Beta Multiplier Voltage Reference, which only uses standard CMOS technology, is presented [41]. The beta multiplier voltage reference is basically composed of a self-biasing current mirror as shown in Fig. 4-2, where M5-M8 transistors are start-up circuit, M1-M4 transistors are reference voltage generator, and R is the biasing resistor. The size of M2 transistor is designed to be larger than M1 transistor to conform to the characteristic of Eq. 4-1, where V_{GS1} and V_{GS2} are the gate-to-source voltage of M1 and M2 transistor respectively. In the following, the reference voltage and its temperature coefficient are described in Eq. 4-2 and Eq. 4-3 by assuming the body effect is neglected.

$$V_{GS1} = V_{GS2} + I \times R \qquad \text{Eq. 4-1}$$

$$V_{ref} = V_{GS1} = \frac{2}{R \cdot \beta_1}\left(1 - \frac{1}{\sqrt{K}}\right) + V_{thn} \qquad \text{Eq. 4-2}$$

$$\frac{dV_{ref}}{dT} = \frac{dV_{thn}}{dT} - \frac{2}{R \times \beta_1} \cdot \left(1 - \frac{1}{\sqrt{K}}\right) \cdot \left(\frac{1}{R} \cdot \frac{dR}{dT} + \frac{1}{KP(T)} \cdot \frac{dKP(T)}{dT}\right)$$

Eq. 4-3

As expressed in Eq. 4-3, as the temperature increases, the value of resistance raises. But the threshold voltage and the transconductance parameter of the transistors decrease. Base on combining these opposite temperature coefficient, a temperature insensitive reference voltage is able to achieve. However, this structure has tuning difficulties. It is because the tuning factors of resistor R, and the MOS transistor's size cause biasing current and reference voltage to interfere with each other [42]. Thus, an improved beta multiplier voltage reference is proposed in [42]. Before explaining the tuning difficulty of traditional beta multiplier voltage reference and introducing improved one, there are some characteristics about the temperature coefficient of MOS transistors should be discussed firstly in the following.

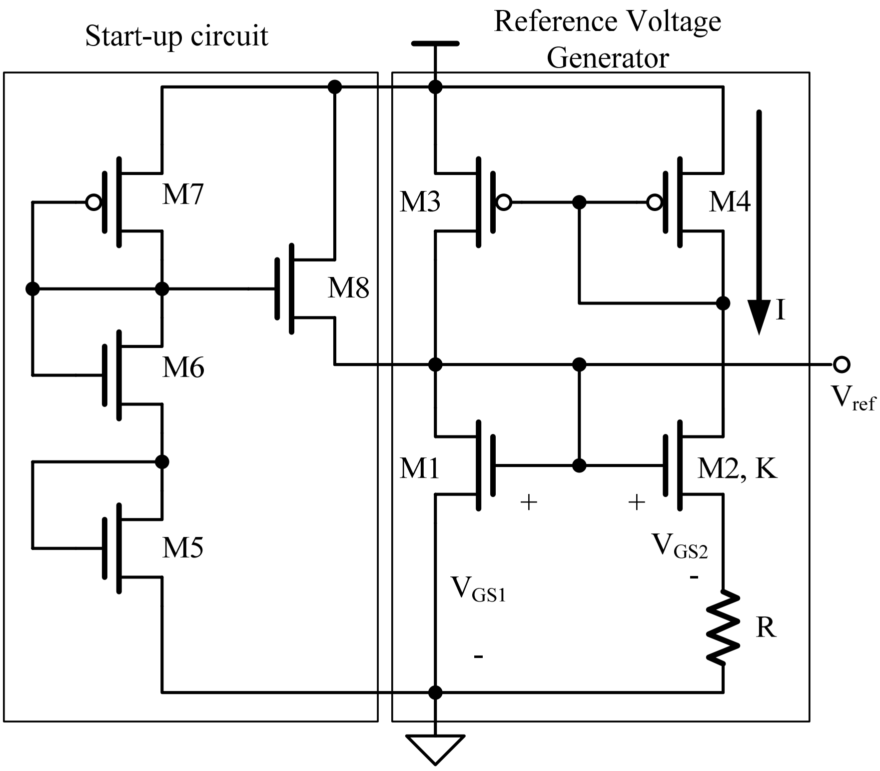

Fig. 4-2 The schematic of traditional Beta Multiplier Voltage Reference [41]

The temperature dependence of MOS transistor's drain current is associated with the operation region. With different operation regions, the characteristics of drain current are also different. While the MOS transistors operate under strong inversion or weak inversion region, the drain current is expressed in Eq. 4-4 and Eq. 4-5 respectively, where I_{DS} is the drain to source saturation current, μ is the mobility of holes or electrons, C_{ox} is the oxide thickness, W/L is the ration of width and length of the MOS transistor, V_{th} is the threshold voltage, V_{GS} is the gate-to-source voltage, and (kT/q) is the thermal voltage [44].

$$I_{DS} = \frac{\mu C_{ox} W}{2L} \times \left(V_{GS} - V_{th}\right)^2 \qquad \text{Eq. 4-4}$$

$$I_{DS} = I_{DO} \times \frac{W}{L} \times e^{q\left(\left(V_{GS} - V_{th}\right)/\left(N0.kT\right)\right)};\ I_{DO} = \mu C_{ox} \times \left(\frac{kT}{q}\right)^2 \times e^{1.8} \qquad \text{Eq. 4-5}$$

According to Eq. 4-4 and Eq. 4-5, while the MOS transistor operates under strong inversion region, the value of V_{GS} is larger than V_{th}. Since μ has greater negative temperature dependence than V_{th}'s, the drain current I_{DS} has a negative temperature coefficient as operating under strong inversion region. On the other hand, the drain current I_{DS} have a positive temperature coefficient while the MOS transistor operates under weak inversion region due to the greatly positive temperature dependence of I_{DO}. By observing the temperature coefficient of drain current I_{DS} varying from positive value to negative value, we can find out a biasing point of the MOS transistor where its drain current I_{DS} has minimum temperature dependence. Based on simulating results, the biasing point is located in the strong inversion region after the weak inversion region. Fig. 4-3 shows this characteristic in terms of the I_{DS} and V_{GS}, where the pink and blue line represents the MOS transistor operating at room temperature and high temperature respectively, and CP denotes the proper biasing point across by the blue and pink line. As shown in Fig. 4-3, the left side of CP expresses I_{DS} with positive temperature dependence (PTAT: proportional to absolute temperature), and the right side of CP expresses I_{DS} with negative temperature dependence (IPTAT: inverse proportional to absolute temperature). While the MOS transistor operates at the bias point CP, it is insensitive to the temperature variation. In Fig. 4-4, a simplified schematic of reference voltage generator is illustrated. It is constructed by a current source with the positive temperature coefficient and a diode-connected MOS transistor. Since the bias current generated by the current source has the positive temperature coefficient, the diode-connected MOS transistor should operate below biasing point CP so as to achieve low temperature dependence.

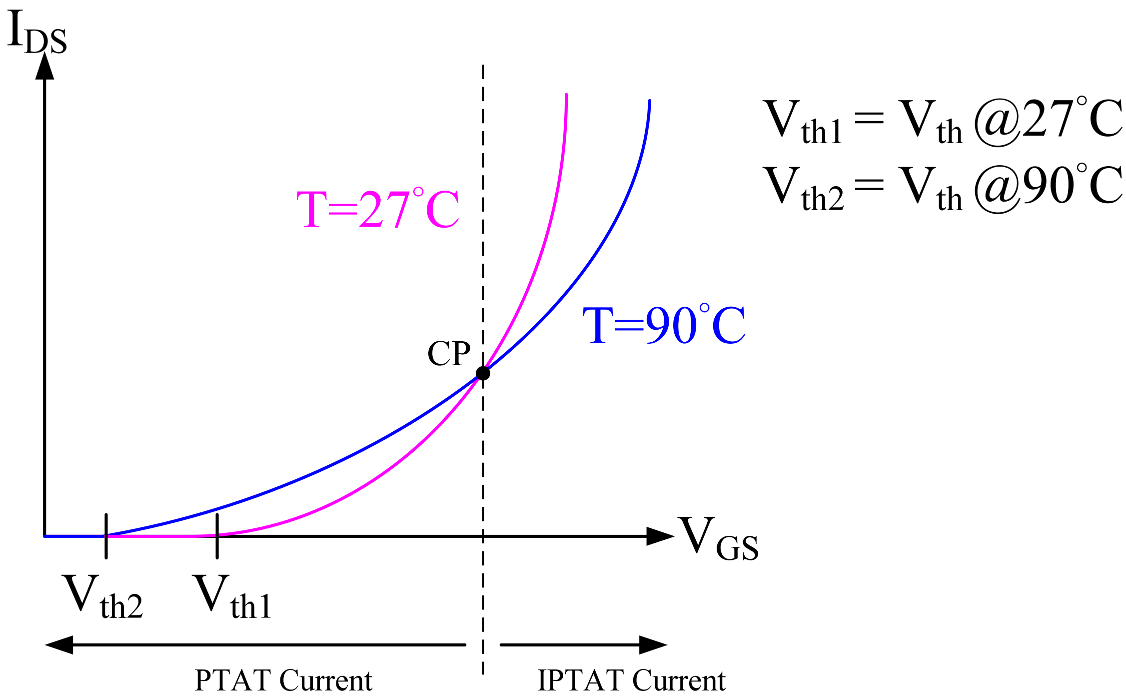

Fig. 4-3 I_{DS} VS V_{GS} under different temperature

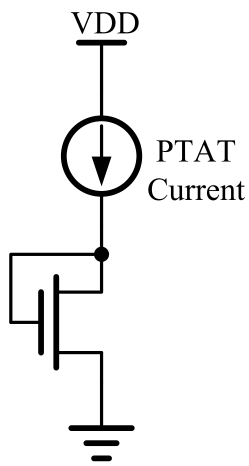

Fig. 4-4 V_{ref} generation

The traditional beta multiplier voltage reference, which is constructed by a self biasing current mirror as shown in Fig. 4-5, has problems in tuning the bias point. The bias current generated from the current mirror it self is expressed in Eq. 4-6. Since μ_n has greater negative temperature coefficient than resistor's positive temperature coefficient (the typical temperature coefficient of the threshold voltage, transconductance parameter and resistance of n+ resistor is -3000ppm/°C, -1.5/T, and 2000ppm/°C [41]), the bias current has positive temperature dependence. For the sake of making reference voltage have less sensitivity to the temperature, it is necessary to adjust the size of transistor M1 to make it operate below bias point CP. However, as tuning the size of transistor M1, it also influences the bias current and makes bias point CP move to another location. It is because both of the bias current and the bias point CP are all decided by transistor M1. In other words, the bias point CP and the temperature coefficient of bias current are much interlink in the traditional structure of beta multiplier voltage reference.

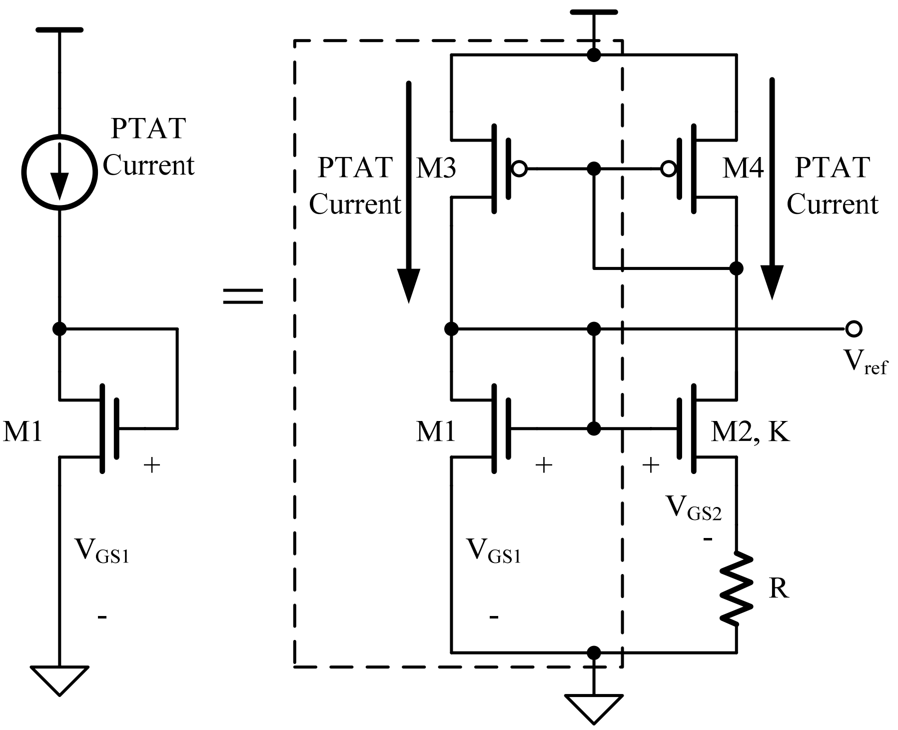

Fig. 4-5 The schematic of traditional Beta Multiplier Voltage Reference and simplified structure

$$I = \frac{2}{\mu_n C_{oxN}(\frac{W}{L})_N \times R^2} \times \left(1 - \frac{1}{\sqrt{K}}\right)^2 \qquad \text{Eq. 4-6}$$

Due to the tuning difficulty, the improved beta multiplier voltage reference separates the bias current generator and the reference voltage generator as shown in Fig. 4-6, where the current mirror is composed of M1~M4 transistors, and M5, M6 transistors construct a voltage reference generator. This is achieved by mirroring the generated bias current through transistor M5 and passing it to the diode-connected transistor M6. In this way, the bias current and the reference voltage can be tuned independently. The reference voltage V_{ref} is developed by the diode-connected transistor M6 depending on the bias current as expressed in Eq. 4-7. More over, the value of reference voltage can be designed by using a stack of diode-connected transistors. Fig. 4-7 shows a reference voltage generator using two diode-connected transistors to generate a higher reference voltage, and V_{ref} is expressed in Eq. 4-8.

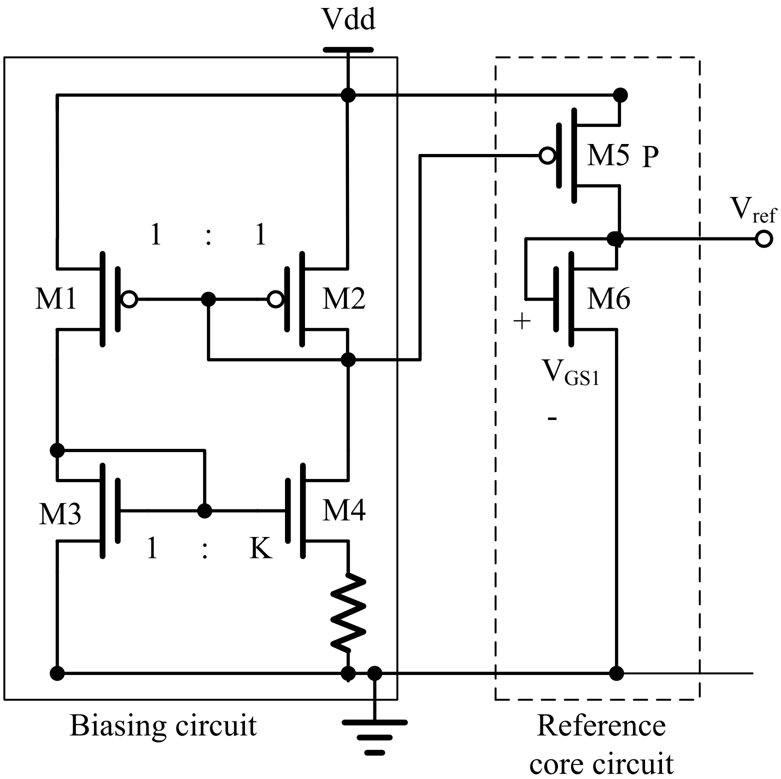

Fig. 4-6 The structure of improved beta multiplier voltage reference

$$V_{ref} = V_{th6} + \frac{2}{\mu_n \times Rs} \times \left(1 - \frac{1}{\sqrt{K}}\right) \times \sqrt{\frac{1}{C_{oxN} \times \left(\frac{W}{L}\right)_N}} \times \sqrt{\frac{1}{C_{ox6} \times \left(\frac{W}{L}\right)_6}} \quad \text{Eq. 4-7}$$

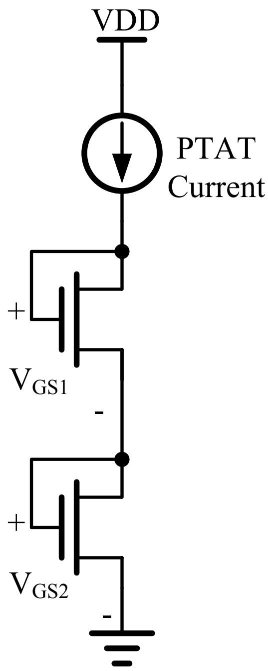

Fig. 4-7 Vref generated by two diode-connected transistors

$$V_{ref} = \sum_{i=1}^{2} V_{th\,i} + \frac{2}{\mu_n \times Rs} \times \left(1 - \frac{1}{\sqrt{K}}\right) \times \sqrt{\frac{1}{C_{oxN} \times \left(\frac{W}{L}\right)_N}} \times \sum_{i=1}^{2} \sqrt{\frac{1}{C_{oxi} \times \left(\frac{W}{L}\right)_i}} \quad \text{Eq. 4-8}$$

Consequently, the improved beta multiplier voltage reference has higher flexibility in tuning temperature coefficient of the reference voltage, and choosing expected reference voltage. In addition, its structure very simple and cost much less area than bandgap voltage reference. In the next section, a design of adjustable reference voltage generator, which is modified from improved beta multiplier voltage reference, is presented.

4.2 Proposed Adjustable Reference Voltage Generator

The function of adjustable reference voltage generator is to generate more than one stable reference voltages through a multiplexer controlled by an external control signal to select expected reference voltage, and pass it to the error amplifier. The most important design target is to be sure that the generated reference voltages can stay unchanged under the variation of temperature and supply voltage. An adjustable reference voltage generator based on modified bandgap structure is proposed in [10], and its structure is shown in Fig. 4-8. It is realized by adding three gain stages to the traditional bandgap reference voltage generator in order to provide different reference voltages. In general, the bandgap reference voltage generator is responsible to produce a temperature-insensitive reference voltage. But the bandgap reference voltage generator shown in Fig. 4-8, which is composed of M1 ~M5 transistors, is responsible to generate a temperature-sensitive output voltage and then through extra gain stages to generate expected reference voltages with less temperature dependence. The reference voltages are expressed in Eq. 4-9, where V_{G1} ~ V_{G3} are the expected reference voltages, V^{*}_{GAP} is the output voltage of bandgap reference, V_{EB} is the emitter-to-base voltage, and the V_{SG7}, $V_{SG7'}$, $V_{SG7''}$ are the source-to-gate voltages of transistors M7, M7', M7'' respectively.

$$\begin{aligned} V_{G2(G1,\,G3)} &= V^{*}{}_{GAP} + V_{SG7(SG7',\,SG7'')} \\ &= V_{EB} + R_2 \times I_{GT} + V_{SG7(SG7',\,SG7'')} \end{aligned} \qquad \text{Eq. 4-9}$$

This structure, which uses extra two transistors to produce a reference voltage with less temperature dependence, only occupies a small area. It means this structure has high extendibility in increasing the number of output voltages without worry about area overhead. However, this structure is based on the bandgap voltage reference, and the disadvantages of bandgap voltage reference discussed earlier also exist in this structure. In addition, as the number of reference voltage raises, the designer has to spent more time in tuning the extra transistors in order to make reference voltages independent to temperature variation. In the following paragraph, a new adjustable reference voltage generator, which has higher extendibility and cost smaller area and power, is presented.

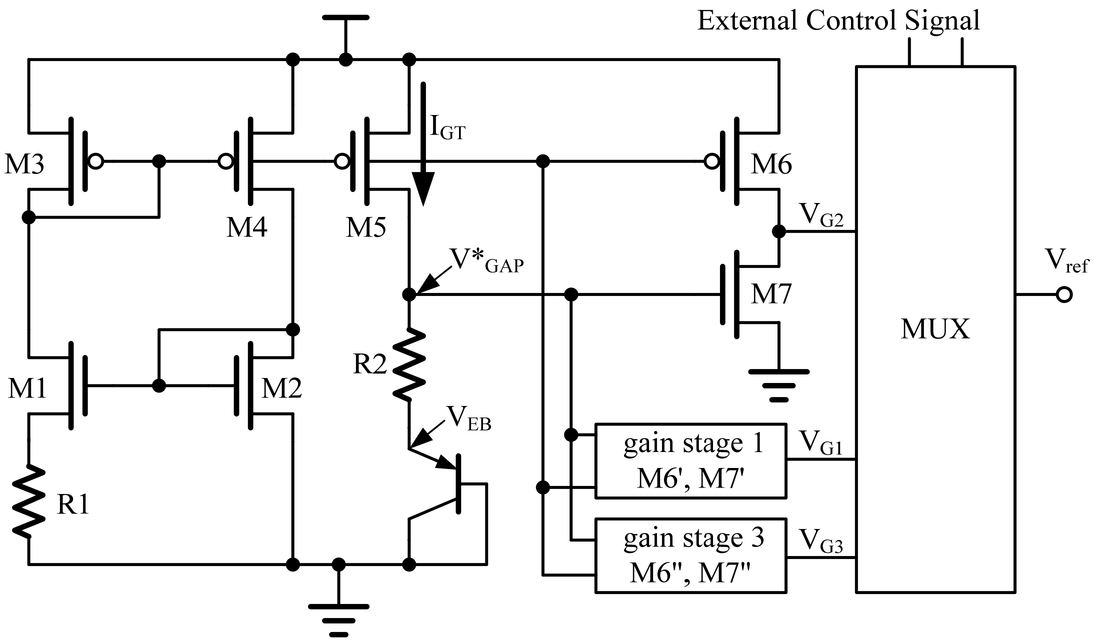

Fig. 4-8 The schematic of an adjustable reference voltage generator based on bandgap structure [10]

According to the previous description, the improved beta multiplier voltage reference is introduced. It uses simple structure and easy tuning technique to achieve a temperature-insensitive reference voltage. In addition, the value of the reference voltage can be regulated by deciding the number of diode-connected transistors. As the number of diode-connected transistor increases, the value of the reference voltage also raises. On the base of these advantages, a new adjustable reference voltage generator utilizing the conception of beta multiplier voltage reference is proposed in the thesis. The structure of this new adjustable reference voltage generator is shown in Fig. 4-9, where the biasing circuit is composed of transistors M4 ~ M7; transistors M1, M2, M8 are responsible for the first reference voltage generation, and transistors M3, M9 are responsible for the second one.

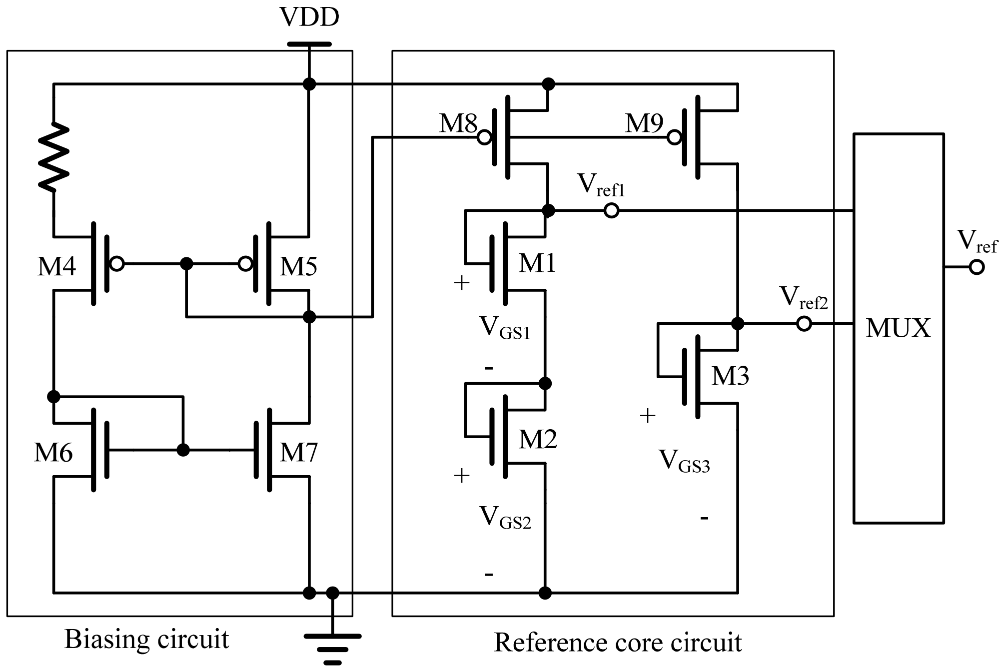

Fig. 4-9 The structure of proposed adjustable beta multiplier voltage reference

As shown in Fig. 4-9, the first reference voltage is generated by stacking two gate-to-source voltages, and the second one is generated by utilizing only one. So the first reference voltage is higher than the second one. The method of tuning reference voltages to become temperature-independent is the same as the traditional beta multiplier voltage reference. The regulating process is described in the following. In the beginning, try to find out the bias point of diode-connected transistors. And then, uses bias circuit to generate associated bias current to make diode-connected transistors operate below the bias point. Finally, try to tune the size of diode-connected transistors slightly in order to derive optimizing results. This structure has the same advantages as the previous structure proposed in [10], such as small area cost and power consumption. In addition, this structure uses pure CMOS technology and has no disadvantages of bipolar transistors. However, the area cost and power consumption increase a lot while the number of reference voltage raises. It is because the structure needs to add extra bias currents and stacks of diode-connected transistors. Therefore, the extendibility is less than the previous structure proposed in [10]. For the sake of increasing the extendibility, it is necessary to modify the structure to reduce area cost and power consumption.

Since the reference voltage can be regulated by choosing the number of diode-connected transistors, it is possible to design an adjustable stack of diode-connected transistors as shown in Fig. 4-10. This figure shows a simplified schematic of adjustable reference voltage generator, where transistors M1, M2 are stack of diode-connected transistors, and MC is the extra transistor controlled by external control signal. While MC transistor is turned off, the bias current flows through both diode-connected transistor M1, M2 and generates a higher reference voltage. As transistor MC is strongly turned on, the bias current will go through transistors M1, MC and ignore transistor M2. In this situation, node X is nearly connected to ground, and the two diode-connected transistors are transformed to one. Hence the reference voltage is transformed to a lower value result from single diode-connected transistor. Obviously, the function of transistor MC is the same as the multiplexer, so the output of reference voltage generator does not require extra multiplexer.

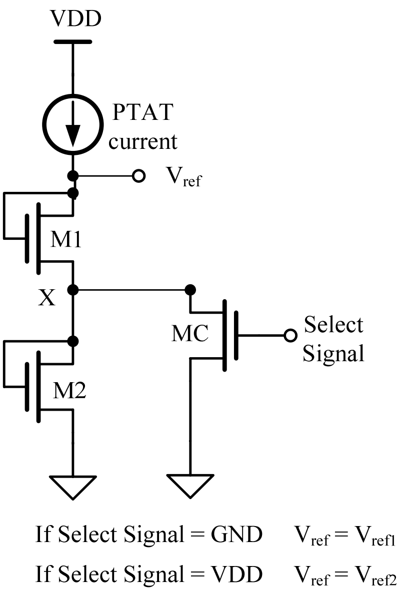

Fig. 4-10 The simplified schematic of an adjustable reference voltage generator

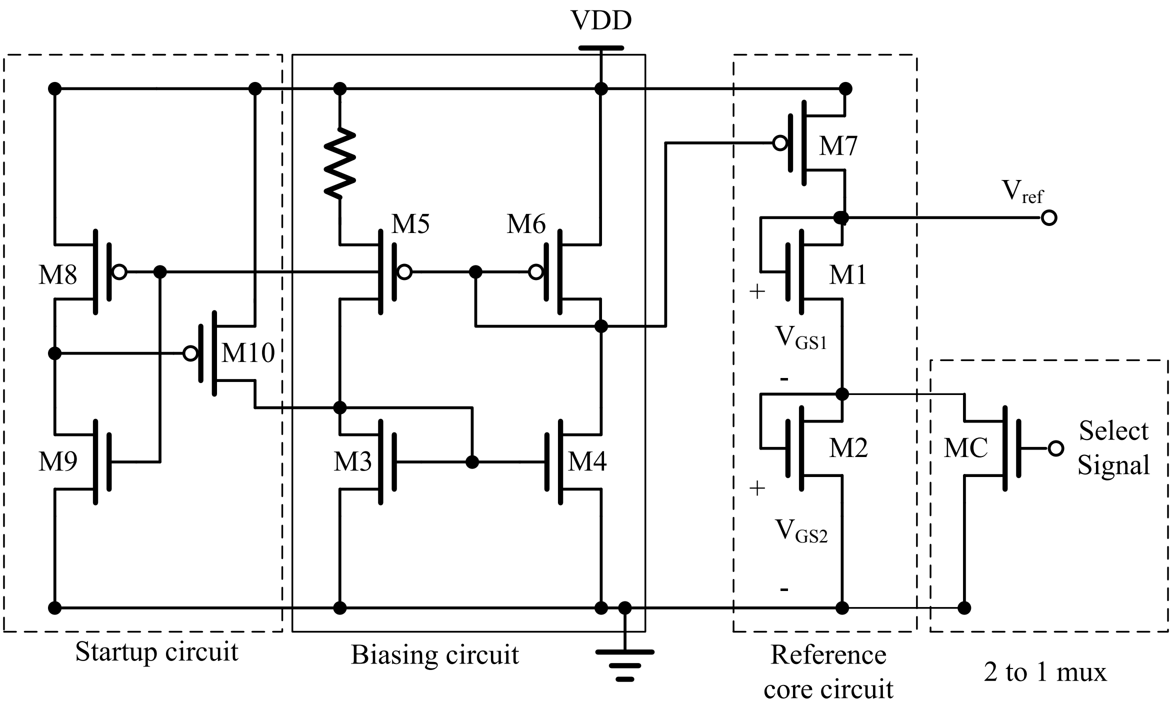

Fig. 4-11 The structure of the proposed adjustable reference voltage generator through modification

The detail structure of this reference voltage generator is shown in Fig. 4-11, where transistors M8 ~ M10 construct start-up circuit, transistors M3 ~ M6 are self-biasing current mirror, transistor M7 is responsible to mirror the bias current, and transistors M1, M2, MC construct adjustable stack of diode-connected transistors. The reference voltages under different select signal are expressed in Eq. 4-10, where V_{ref1} is the higher reference voltage and V_{ref2} is the lower one. It is important to notice the amount of transistor MC's drain-to-source voltage $V_{DS(MC)}$. Because this small across-voltage can cause little drift on bias point and increase the temperature-dependence. So the size of transistor MC should be designed largely for reducing this across-voltage and make V_{ref2} almost equal to V_{GS1}. According to the simulation result, the across-voltage can be reduced to 60μV or less by using proper size of MC transistor (W/L = 50μ/1μ). Therefore, the bias point does not drift too much and the temperature-dependence of reference voltage is not influenced a lot.

$$\begin{aligned} V_{ref1} &= V_{GS1} + V_{GS2} \\ V_{ref2} &= V_{GS1} + V_{DS(MC)} \approx V_{GS1} \end{aligned} \qquad \text{Eq. 4-10}$$

By comparing Fig. 4-8, Fig. 4-9, and Fig. 4-11, we can find out the modified structure cost smallest power and area. It is because that it uses only one bias current path mirrored by transistor M7 to generate two different reference voltages. In addition, as the number of reference voltage raises, it only needs to add an extra diode-connected transistor and a transistor MC. Hence, the power consumption only increases a little resulted from the gate-current of transistor MC. And the area cost also raises only a little, because it only needs additional diode-connected transistors and the bypass transistor MC but no extra multiplexer. The tuning difficulty is the same as the previous structure. By searching bias point, the temperature-dependence of reference voltages can be regulated to minimum by tuning each size of diode-connected transistors. According to these advantages, the proposed adjustable reference voltage generator has great extendibility than original structures in Fig. 4-8 and Fig. 4-9 because of low area cost and power consumption. Moreover, the reference voltages can achieve extremely low temperature coefficient by proper tuning work. Table 4-1 concludes the comparison between the ARVG proposed in [10] and in the thesis.

Design / Parameter	ARVG by E. Kussener	Proposed ARVG
Area	1BJT, 11 transistors, 2 resistors	11 transistor, 1 resistor
Power	5 bias current	3 bias current
Temperature Coefficient	300ppmV/˚C (Min)	31ppmV/˚C (Max)
Extendibility (Increases 1 output voltage)	Need to add 3 transistors and 1 bias current	Need to add 2 transistors and no bias current

Table 4-1 Comparison between the ARVG proposed in [10] and in the thesis

4.3 Error Amplifier

The error amplifier is utilized to compare the output signal passed by feedback resistors and the reference voltage, and then amplifies the difference between these two signals in order to control the driving current of the series pass transistor. According to Eq. 2-4 and Eq. 2-5, the line regulation and the load regulation are quite associated with the open loop gain which is composed of error amplifier's gain and series pass transistor's gain. In order to reduce these two terms, the gain of the error amplifier should be large [45]. The error amplifier proposed in this thesis is shown in Fig. 4-12. It is composed of two moderate-gain stages. The first stage is a differential-pair single-ended operational amplifier constructed by transistors M1 ~ M4 and M8, where transistors M3, M4 are active load, and transistors M1, M2 are differential pair. It is used to detect the difference between input voltages (V_{ref} and V_f) and generate an error signal to the second stage. The second stage is a common-source amplifier composed of transistors M5 and M9, where transistor M9 is a mirrored current source. Due to the cascade architecture, the open loop gain is produced by the product of these two gain-stages. So the open loop gain is larger than the traditional voltage regulator using single-stage error amplifier [46]. The output swing of the second gain-stage is higher than the first gain-stage for the sake of completely turning on or off the series pass transistor MP. There is an important design issue of error amplifier which is used to incorporate with adjustable reference voltage generator. Since the adjustable reference voltage generator can generate more than one reference voltages, the error amplifier should have wide input range in order to accept these reference voltages. As the number of reference voltage increases, the input range should raise as well.

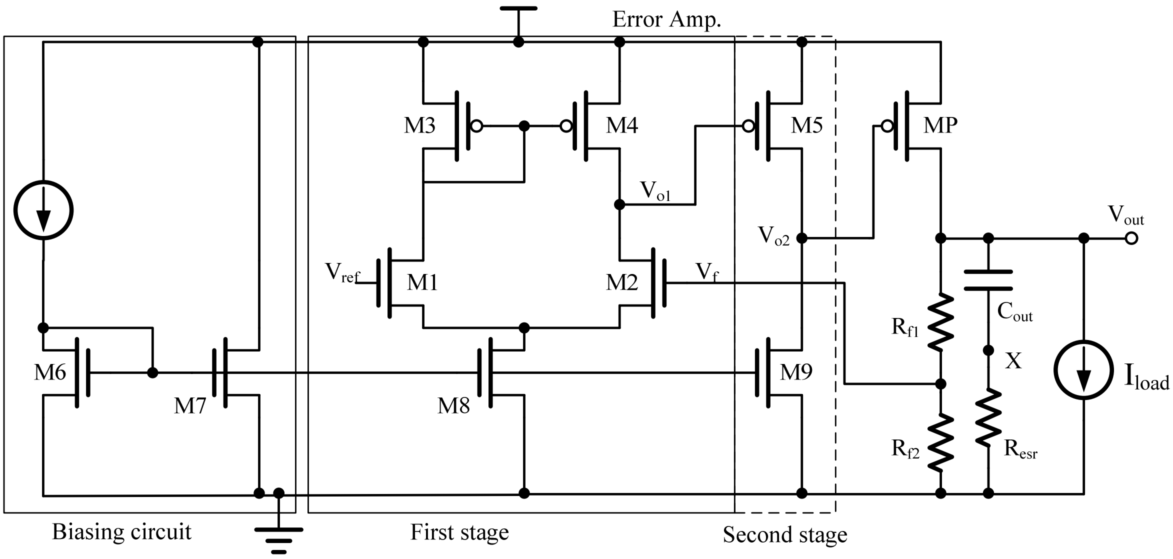

Fig. 4-12 The structure of LDO linear regulator utilizing two-stage error amplifier

4.4 Proposed Dynamic Discharging Path

The transient response of LDO linear regulators has been described in section 2.3.3. According to Fig. 2-16 and Fig. 2-17, the overshoot and undershoot appearing in LDO linear regulators' output voltage is caused by the suddenly changing of loading current. In the cause of maintaining the performance and the stability of the load circuits, the recovering time should be reduced as much as possible. The recovering time can be separated into two parts: One is the time interval cost by recovering output voltage from undershoot-condition, another one is the time interval cost by recovering output voltage from overshoot-condition. In the traditional design of LDO linear regulators, the recovering time of the overshoot-condition is quite larger than the undershoot condition [48], and the reason is described in the following. While the overshoot condition occurs, the error amplifier turns off the series pass transistor to stop the driving current, and the output voltage begins to discharge through the feedback resistors and the load circuit until the output voltage return stable. But the value of feedback resistors is generally designed very large to cease leakage current. So the discharge path has large impedance and makes the recovering time extremely large [47]. Fig. 4-13 and Fig. 4-14 show the simulation results of undershoot-condition and overshoot-condition, where the loading current changes step from 0ma to 100ma and 100ma to 0ma respectively. From the simulation results, we can find out the recovering time of overshoot-condition (440μ sec) is much larger than the undershoot-condition (2μ sec). Although the variation of output voltage is not too large during discharging process, this problem becomes more serious in adjustable LDO linear regulators. Since the discharging path has large impedance and needs a lot of recovering time, while the adjustable LDO linear regulator transforms from a higher output voltage to a lower one, the discharging time becomes extremely large.

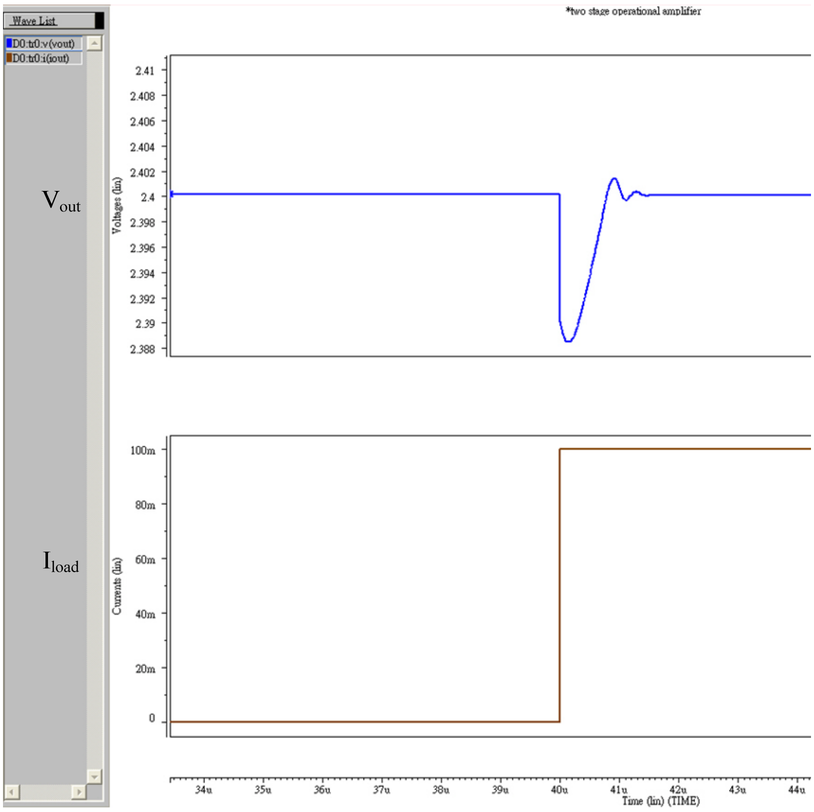

Fig. 4-13 Step-rising load current (Iload = 0 to 100 mA) causes undershoot-condition (recovering time = 2µsec)

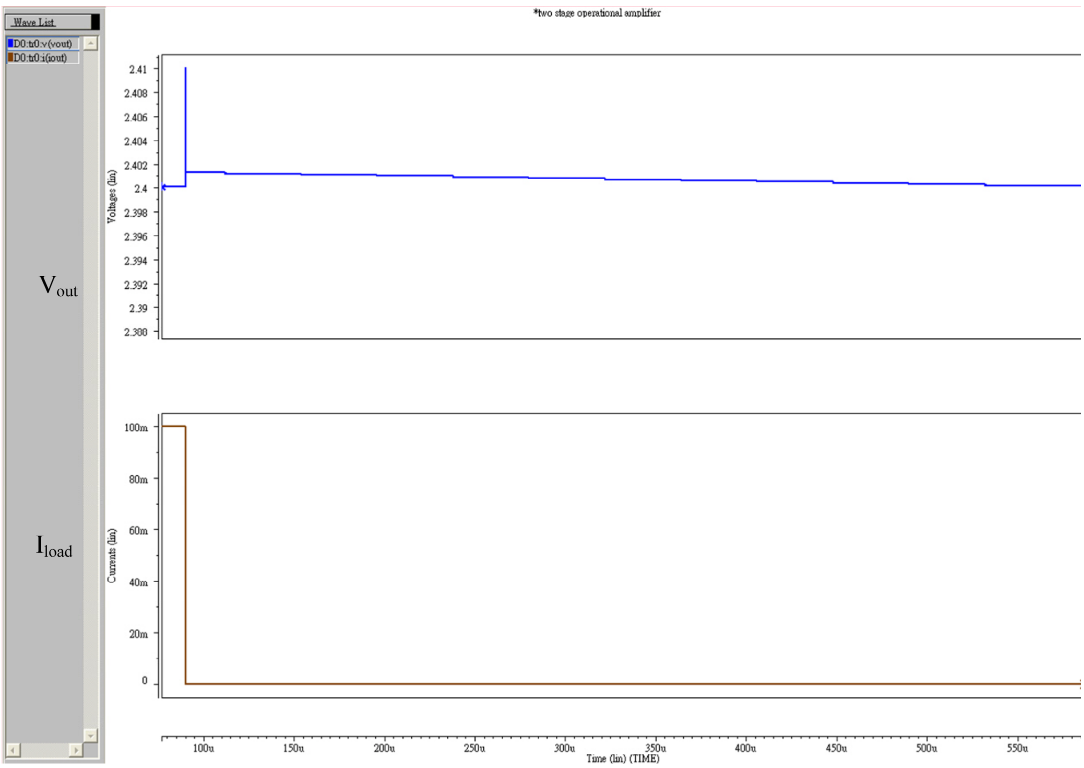

Fig. 4-14 Step-falling load current (Iload = 100 to 0 mA) causes overshoot-condition (recovering time = 440µsec)

The discharging time is mainly dependent on the amount of the difference between output voltages. Fig. 4-15 shows an example of discharging process, where the output voltage discharges from 2.4V to 1V through feedback resistors R_{f1} (7.15k) and R_{f2} (230k). Since the impedance of discharging path composed of feedback resistors is quite large (237.15k), the discharging current is very small and causes an extremely long discharging time as shown in Fig. 4-16 (about 850m sec). This long discharging time decreases the performance of load circuits a lot. Because the load circuits can not work correctly until the adjustable LDO linear regulator achieves expected output voltage. The only way to solve this problem is to add an extra discharging path on the output node in order to accelerate the discharging process. The discharging path can be classified into two parts: one is the static discharging path, such as resistors or active loads. But the static discharging path always causes large leakage current, and decreases the power efficiency. Another one is the dynamic discharging path. It only works under the discharging process, and will be turned off while the process is terminated. In the following paragraph, a dynamic discharging path is presented.

A dynamic discharging path composed of a level-shift buffer and a discharging transistor (NMOS) is presented in this case. Fig. 4-17 and Fig. 4-18 show the block diagram and the detail structure of the dynamic discharging path. According to Fig. 4-18, while the overshoot-condition appears, the value of feedback signal V_f is larger than the reference voltage V_{ref}. This situation causes transistor M2 drains more current than transistor M1 and makes the output signal of the first gain-stage (V_{o1}) decreases. As the signal V_{o1} decreases, there is a positive glitch appearing in the output signal of the second gain-stage (V_{o2}) and strongly turn off the series pass transistor. At this moment, the positive glitch will be regulated by the level-shift buffer and generates a control signal V_{o3} to turn on the discharging transistor and begin to discharge the output voltage.

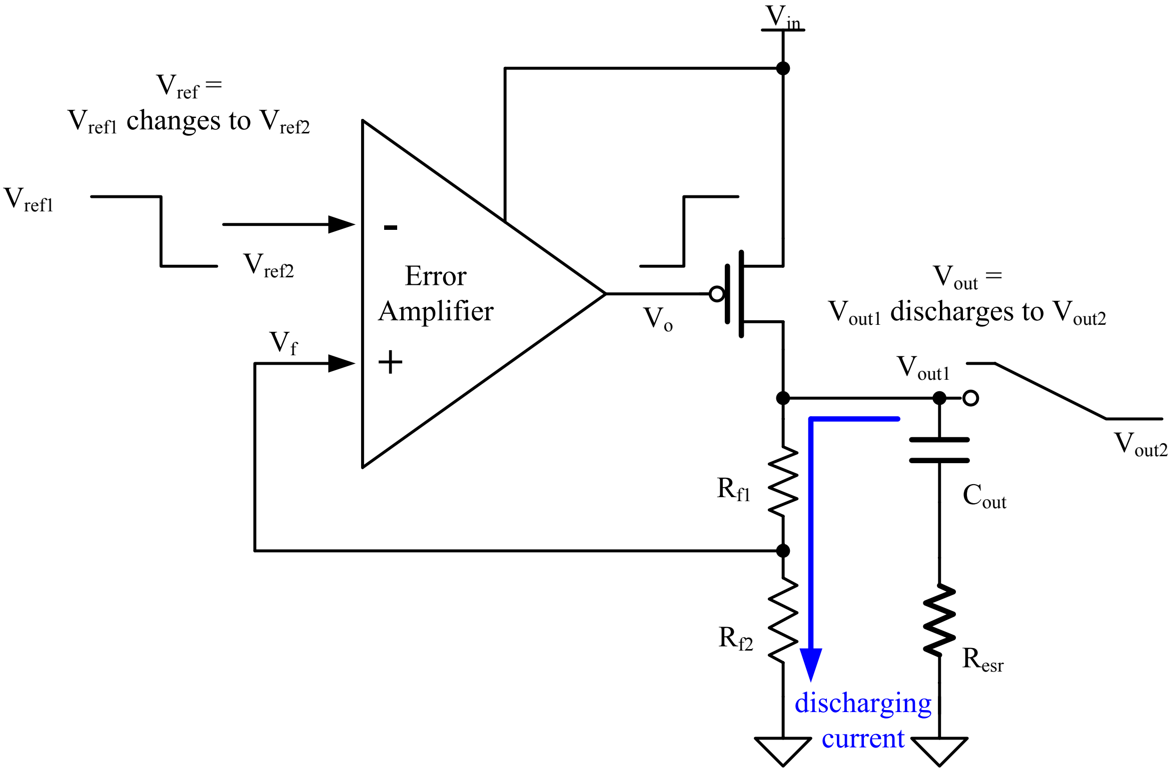

Fig. 4-15 An example of traditional LDO linear regulator's discharging process

(Vout discharges from 2.4V to 1V)

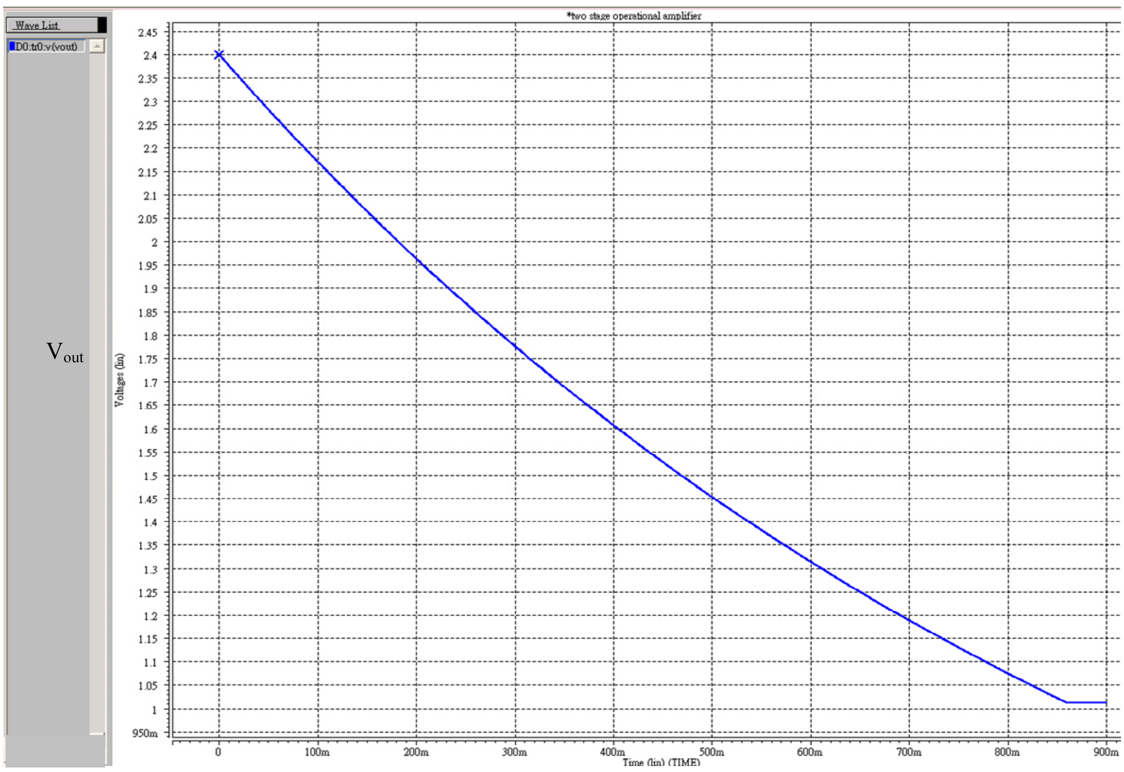

Fig. 4-16 Simulation result of discharging time (850m sec) while output voltage discharges from 2.4V to 1V

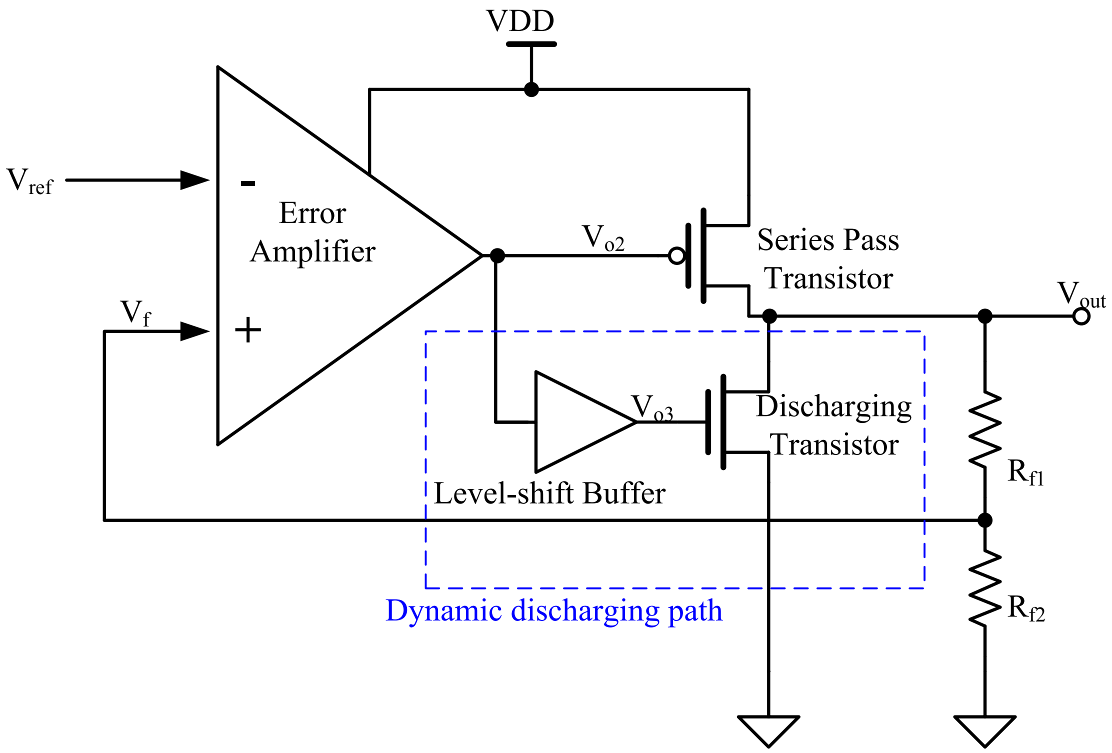

Fig. 4-17 The block diagram of dynamic discharging path

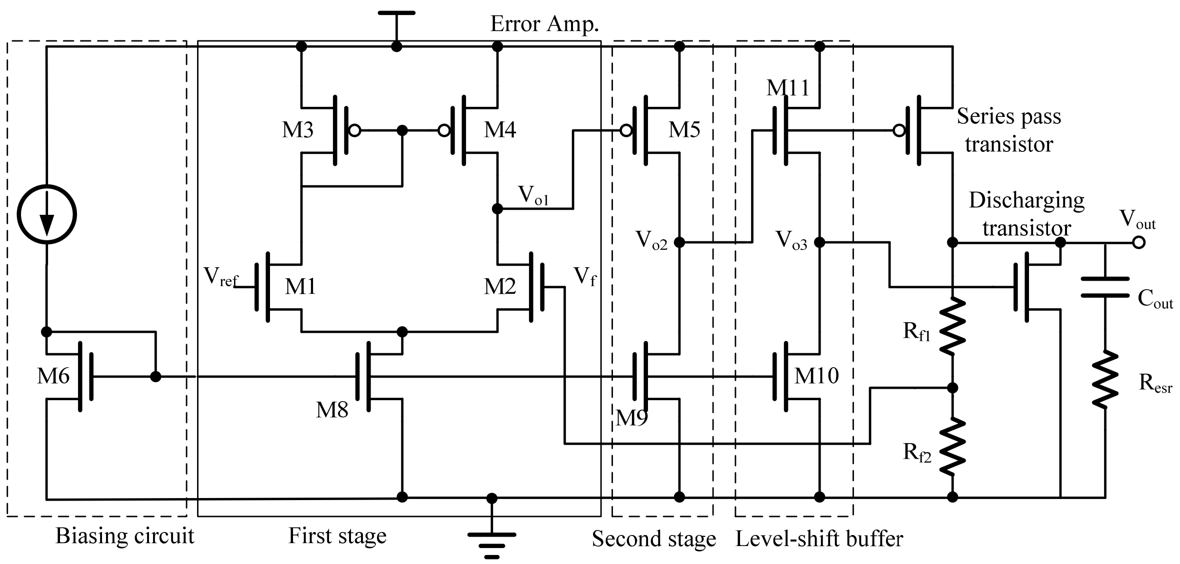

Fig. 4-18 The detail schematic of dynamic discharging path

As the output voltage is discharged to the expected level, the feedback signal V_f will equal to reference voltage V_{ref}, and eliminate the positive glitch. While the positive glitch is gone, the control signal V_{o3} also turns off the discharging transistor and stops to draw current from the output node. Fig. 4-19 and Fig. 4-20 show the simulation results of the signal V_{out}, V_{o3} and the discharging current of the discharging transistor, where the recovering time of the overshoot-condition is only 6μ sec. By comparing the simulation results of Fig. 4-14, Fig. 4-16, Fig. 4-19, Fig. 4-20 and Fig. 4-21, we can know the great contribution of the dynamic discharging path. With using the dynamic discharging path, the transform time of output voltages and the recovering time of overshoot-condition are greatly reduced. The reduced transform time and recovering time are mainly dependent on the discharging current created by the dynamic discharging current. By proper designing the operational range of level-shift buffer and the discharging transistor's size, the discharging current can be more adaptive to the requirement of the applications. There is a trade-off between the performance and the power of adjustable LDO linear regulator. If the dynamic discharging path is designed to be capable of drawing large current for achieving high performance, it also cost a huge leakage current as it is turned off, and consumes a lot of static power. This trade-off should be considered with the application requirement and properly designs the discharging current. Table 4-2 shows the comparison of transform time, recovering time, and leakage current of adjustable LDO linear regulators with high operating current, low operating current of dynamic discharging path, and without dynamic discharging path.

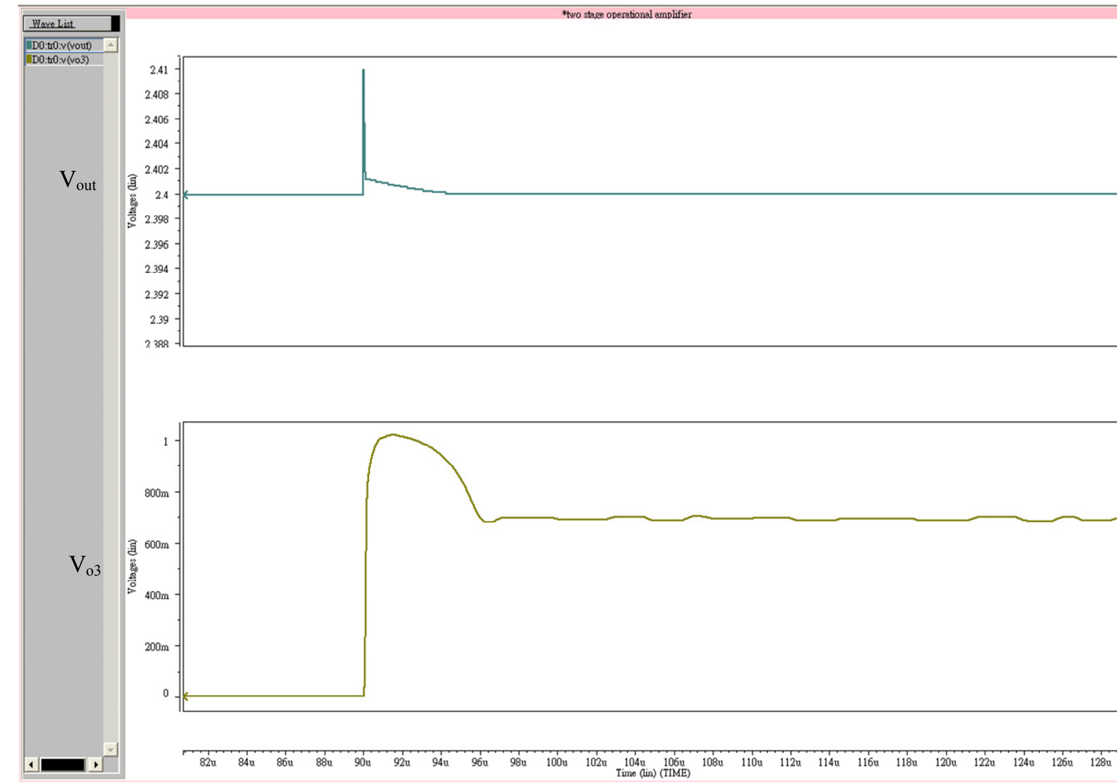

Fig. 4-19 Simulation result of Vout and Vo3 under the overshoot-condition (recovering time = 6μ sec)

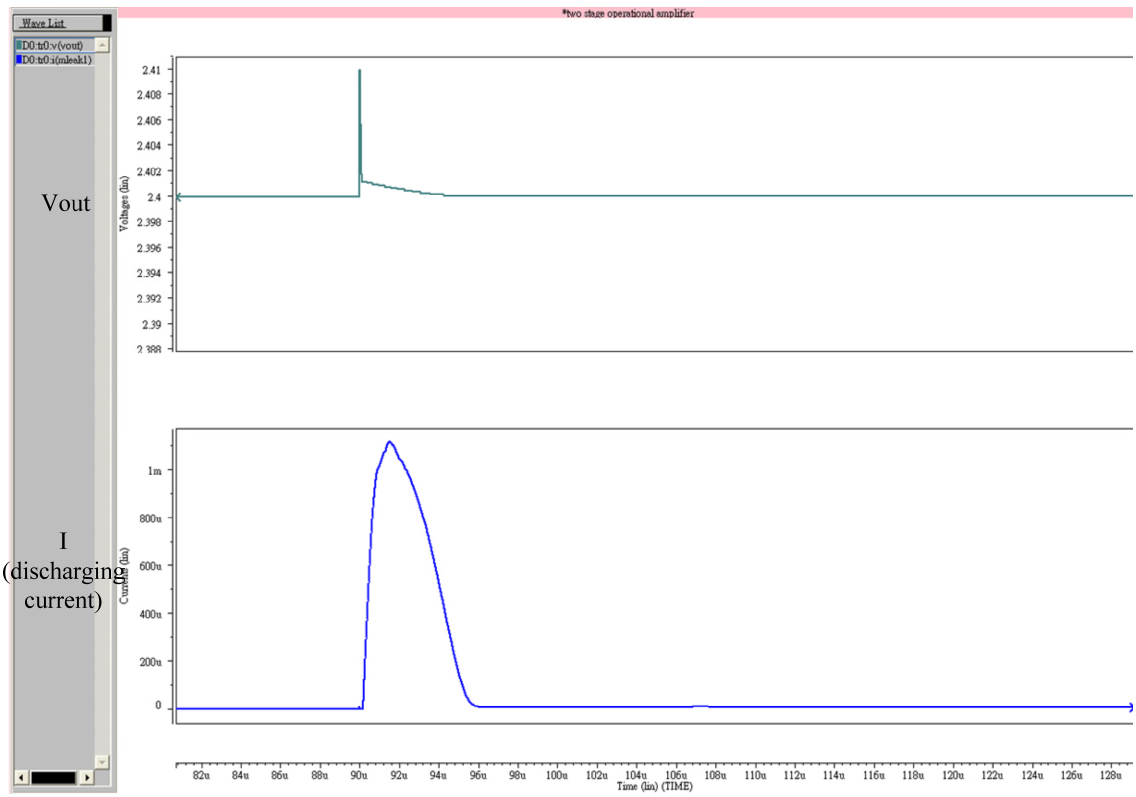

Fig. 4-20 Simulation result of Vout and the current of the discharging transistor under the overshoot-condition

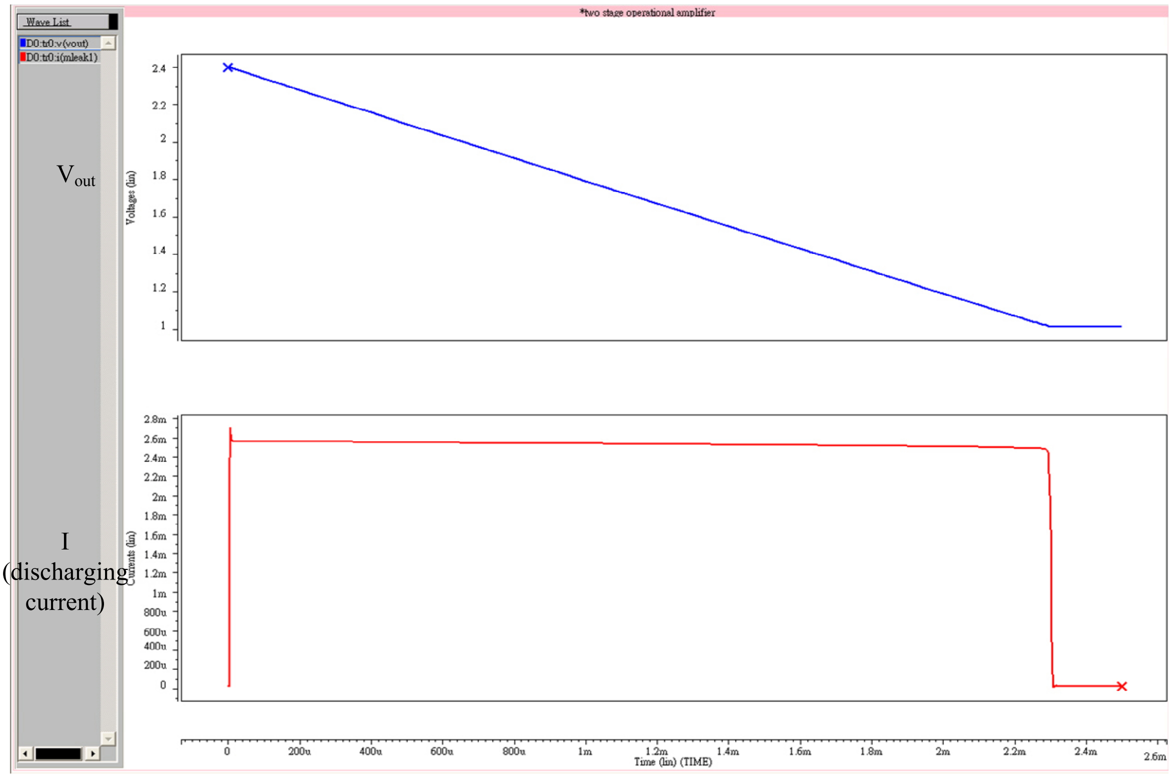

Fig. 4-21 Simulation result of discharging time (about 2.3m sec) while output voltage discharges from 2.4V to 1V with dynamic discharging path

Parameter	Without Dynamic discharging path	With Dynamic discharging path (low current)	With Dynamic discharging path (high current)
Transform time	850m sec	2.3m sec	238μ sec
Recovering time	440μ sec	6μ sec	1.8μ sec
Leakage current	0μ A	6.5μ A	106.8μ A

Table 4-2 Comparison of transform time and leakage current

Chapter 5

Simulation Results

In this chapter, the layout of an adjustable LDO linear regulator and associated issues are discussed in the first section. The second section presents the post-layout simulation results of the adjustable LDO linear regulator.

5.1 Layout Considerations

In the layout of a LDO linear regulator circuit, the series pass transistor occupies more than half of the whole chip's area and the other circuitry only take up a minor portion of the silicon area. It is because in the general design of LDO linear regulators, the series pass transistor is designed to generate huge driving current to the load circuit. For the sake of alleviating RC delay down long gate lines, the series pass transistor is constructed by paralleled smaller transistors. In addition, the lines which connect the supply node and the output node should be designed as wider as possible, and the category of metal should be used as more as possible. One of the major considerations of layout is latch-up prevention. The most likely place for latch-up to occur is the series pass transistor that causes large parasitic, and it needs guard-rings to prevent latch-up. Fig. 5-1 and Fig. 5-2 show the whole chip's layout and the block diagram of the proposed adjustable LDO linear regulator respectively. In this layout, several double guard-rings are utilized for latch-up prevention. The metal width of the lines connecting the input node and the output node are larger than 60μm for avoiding metal migration problems.

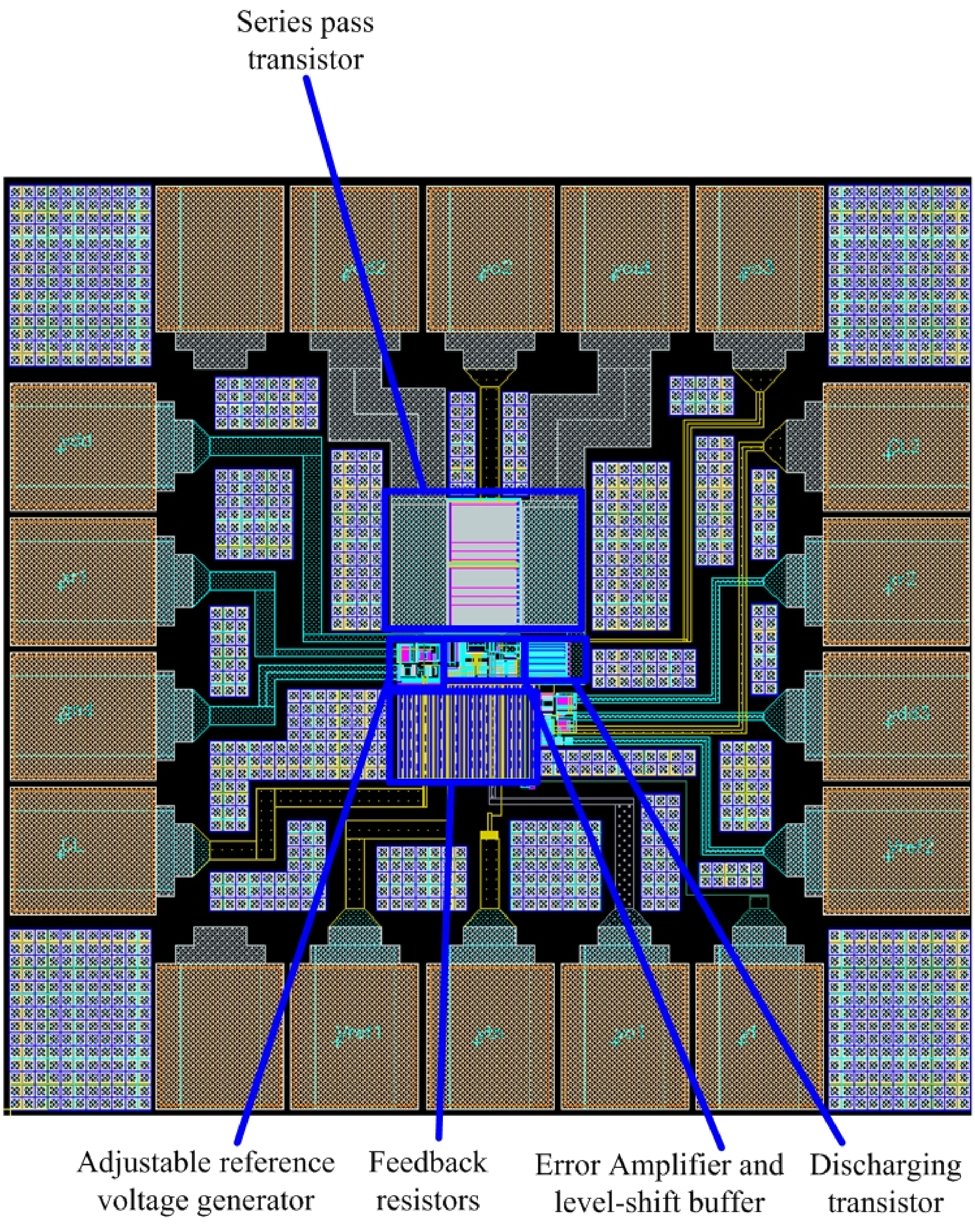

Fig. 5-1 Layout of adjustable LDO linear regulator

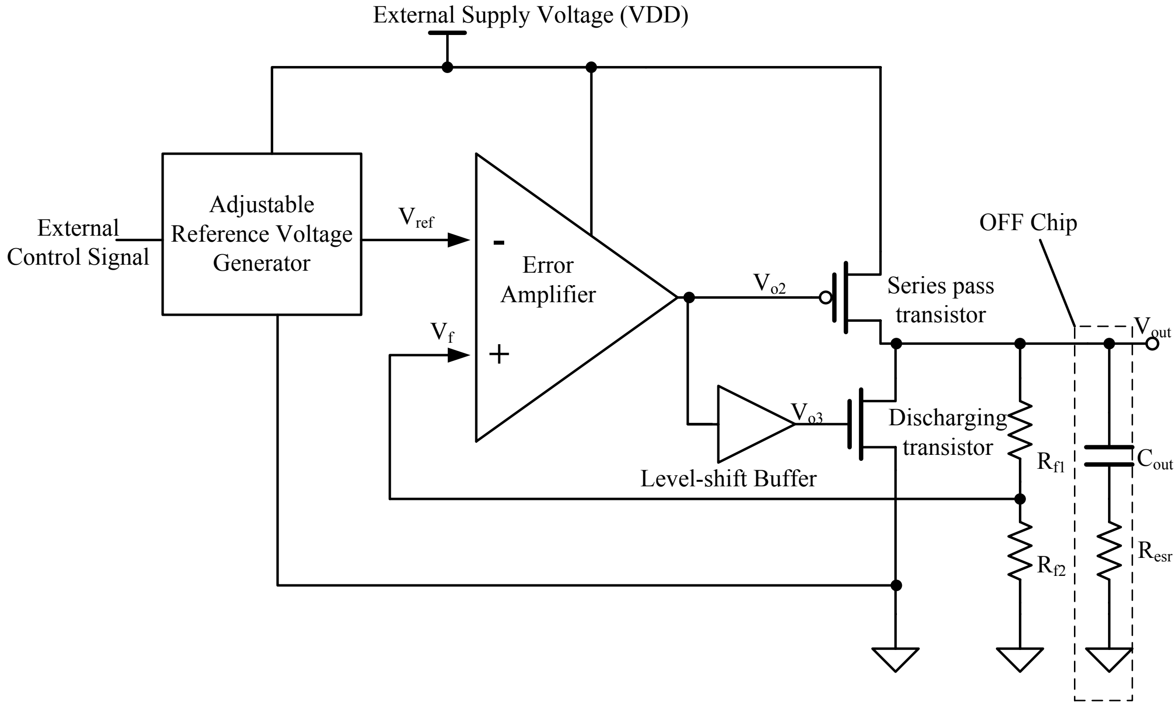

Fig. 5-2 Block diagram of the proposed adjustable LDO linear regulator

5.2 Simulation Results

The block diagram of the proposed adjustable LDO linear regulator is shown in Fig. 5-2, and the specification is described in Table 5-1.

Parameter	External Control Signal = 0V	External Control Signal = 3.3V
Reference Voltage (V_{ref})	2.3276 V	0.981 V
Output Voltage (V_{out})	2.5 V	1.0 V
Supply Voltage	3.3V	3.3V

Table 5-1 Specification of the proposed adjustable LDO linear regulator

In the post-layout simulation of the proposed adjustable LDO linear regulator, an output capacitor 4.2μF and its equivalent series resistance 0.1Ω are added. The simulation results are described graphically in Fig. 5-3 ~ Fig. 5-10, including temperature variations, load current variations, transformations between output voltages, and the characteristics of the input-to-output voltage. Fig. 5-3 and Fig. 5-4 show the transient response of the proposed adjustable LDO linear regulator under the simulated conditions that a full load current change from 0μA to 100mA, the fall time and rise time of the current pulse are both 0.1n seconds. The results show the maximum output variation under a full load current change is below 15mV. Fig. 5-5 and Fig. 5-6 show the behavior of reference voltages and output voltages under the simulating conditions that temperature changes from 0°C to 100°C. The results reveal that the temperature coefficients of output voltages are both below 35ppm/°C. Fig. 5-7 and Fig. 5-8 show the input-to-output's characteristics. The simulation results show that the dropout voltage is about 0.5V. Fig. 5-9 and Fig. 5-10 show the transformation between the output voltages while the control signal is changed. As the control signal rises from logic 0 to logic 1, the output node is discharged from 2.5V to 1.0V. By utilizing the dynamic discharging path, the discharging time is about 1.6m second. On the other hand, as the control signal falls from logic 1 to logic 0, the output node is charged from 1.0V to 2.5V through the series pass transistor, and the charging time is about 70μ second. The leakage current and the discharging time are mainly dependent on the size of the discharging transistor. As the size of the discharging transistor is large, the discharging time can be reduced, but the leakage current will be increased. Table 5-2, Fig. 5-11 and Fig. 5-12 show the simulation results of the discharging time and leakage current under different sizes of discharging transistor.

Table 5-3 and Table 5-4 present the summaries of simulation results under different external control signal and the chip's information.

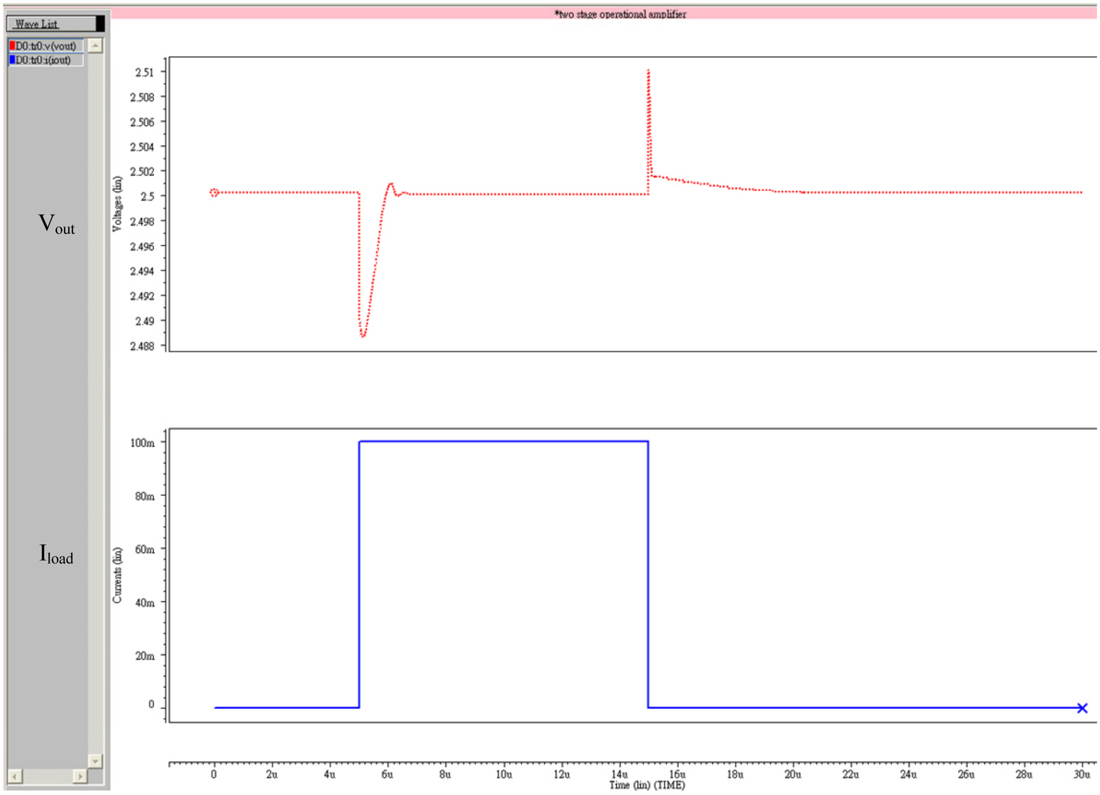

Fig. 5-3 Variation of the first output voltage (2.5 V) under a full load current change (Iload = 0 ~ 100 mA)

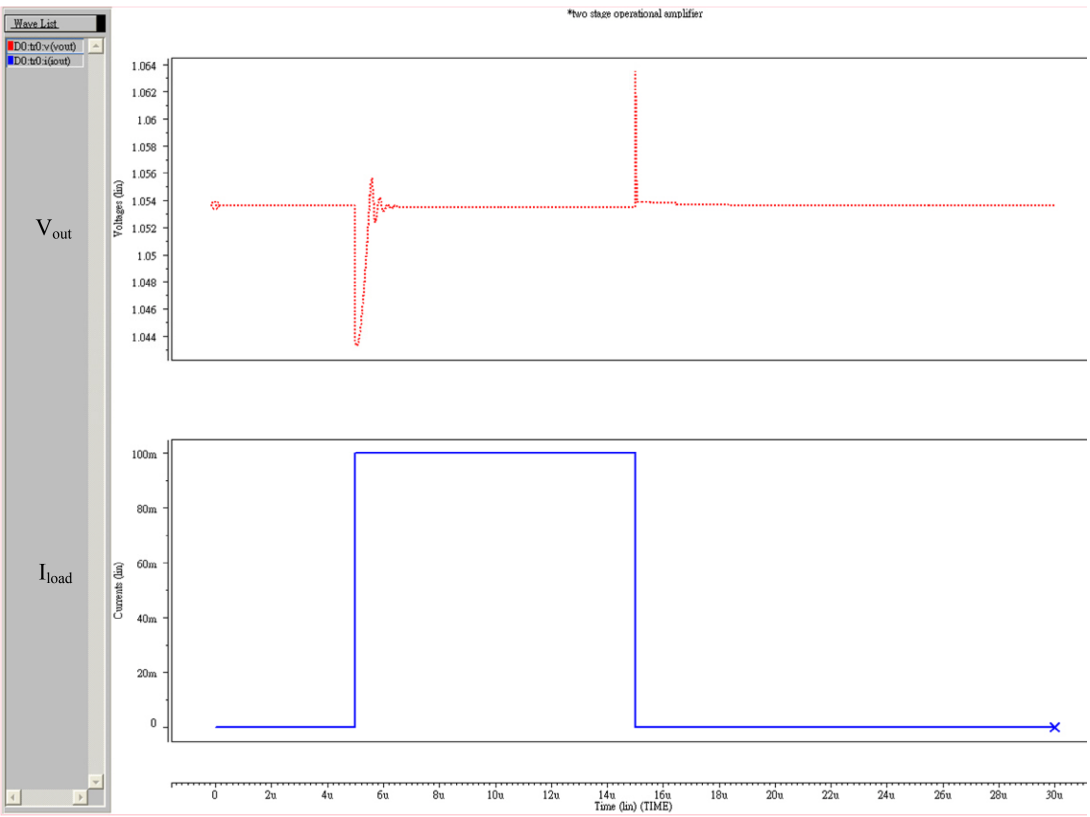

Fig. 5-4 Variation of the first output voltage (1.0 V) under a full load current change (Iload = 0 ~ 100 mA)

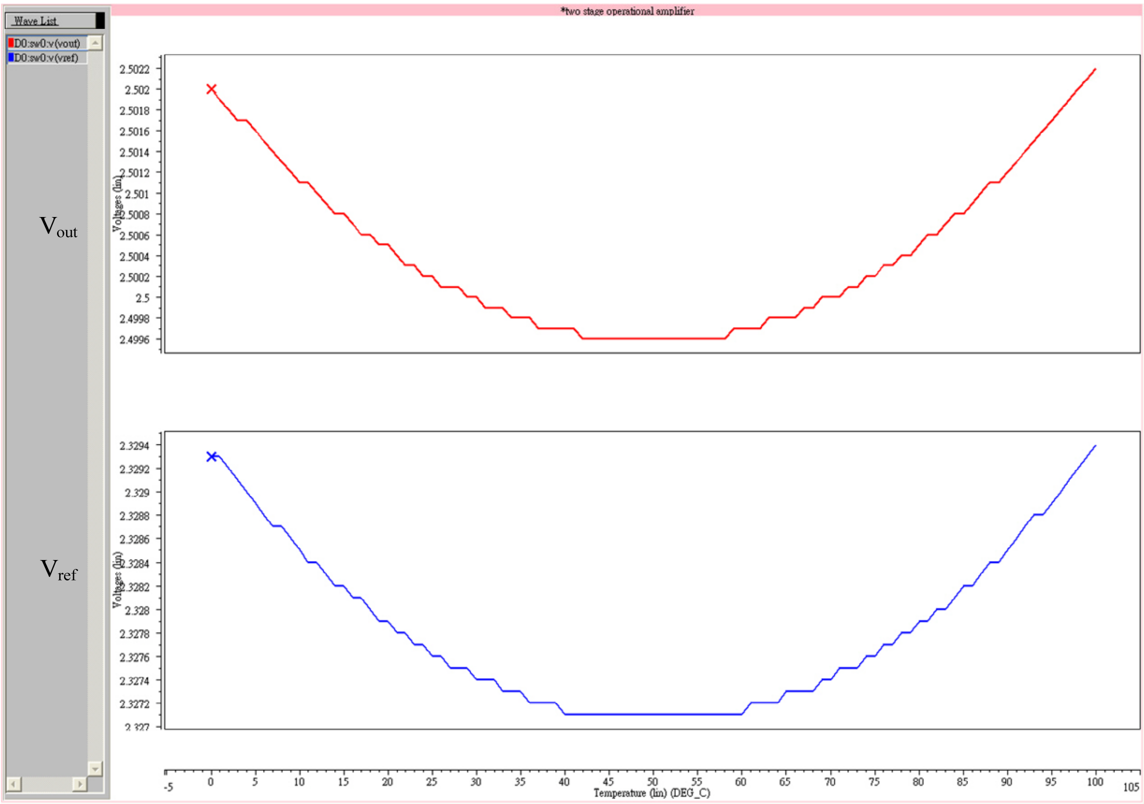

Fig. 5-5 Temperature behavior of the first output voltage (2.5 V) and reference voltage (2.3276 V)

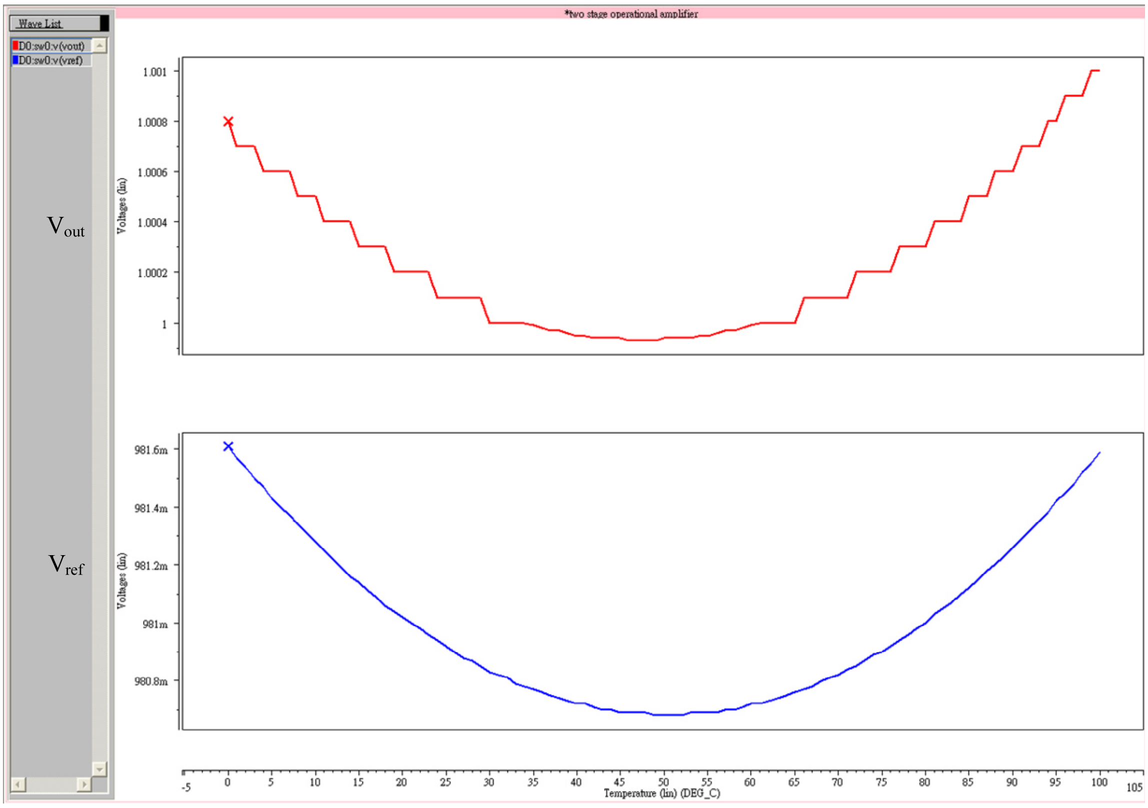

Fig. 5-6 Temperature behavior of the first output voltage (1.0 V) and reference voltage (0.981 V)

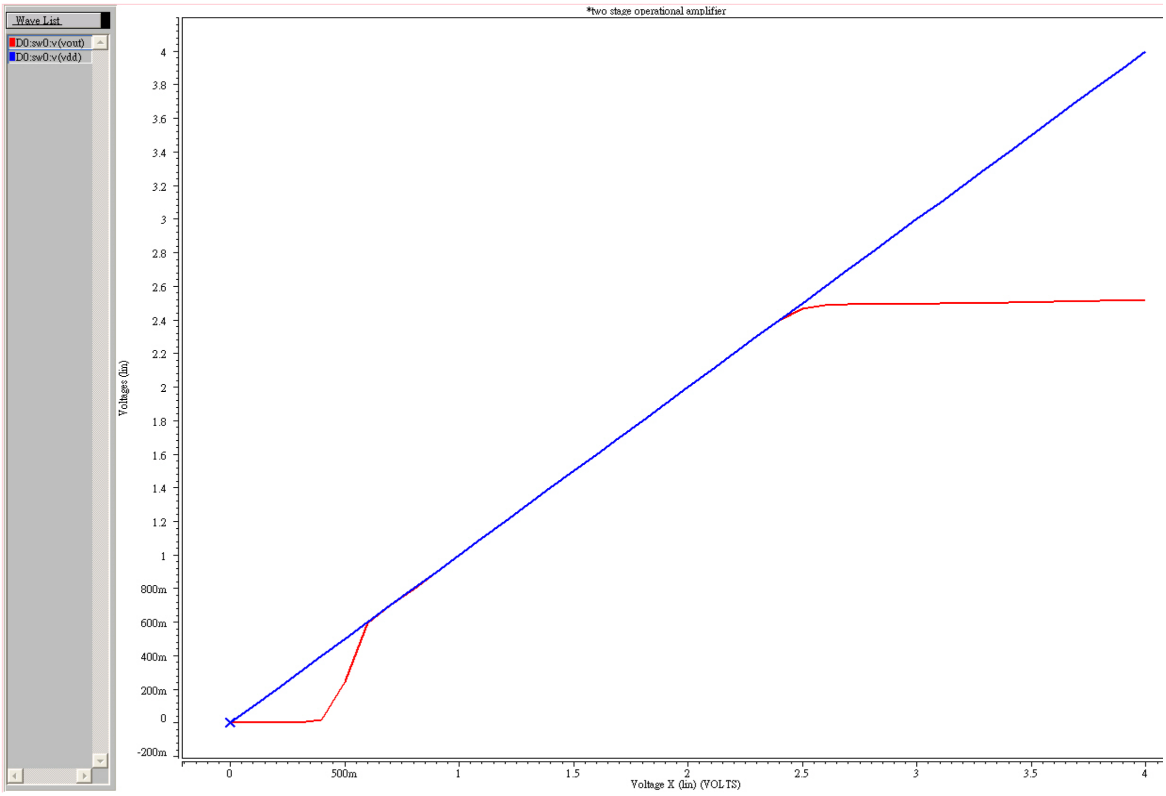

Fig. 5-7 Input/Output voltage characteristics of the firs output voltage (2.5 V)

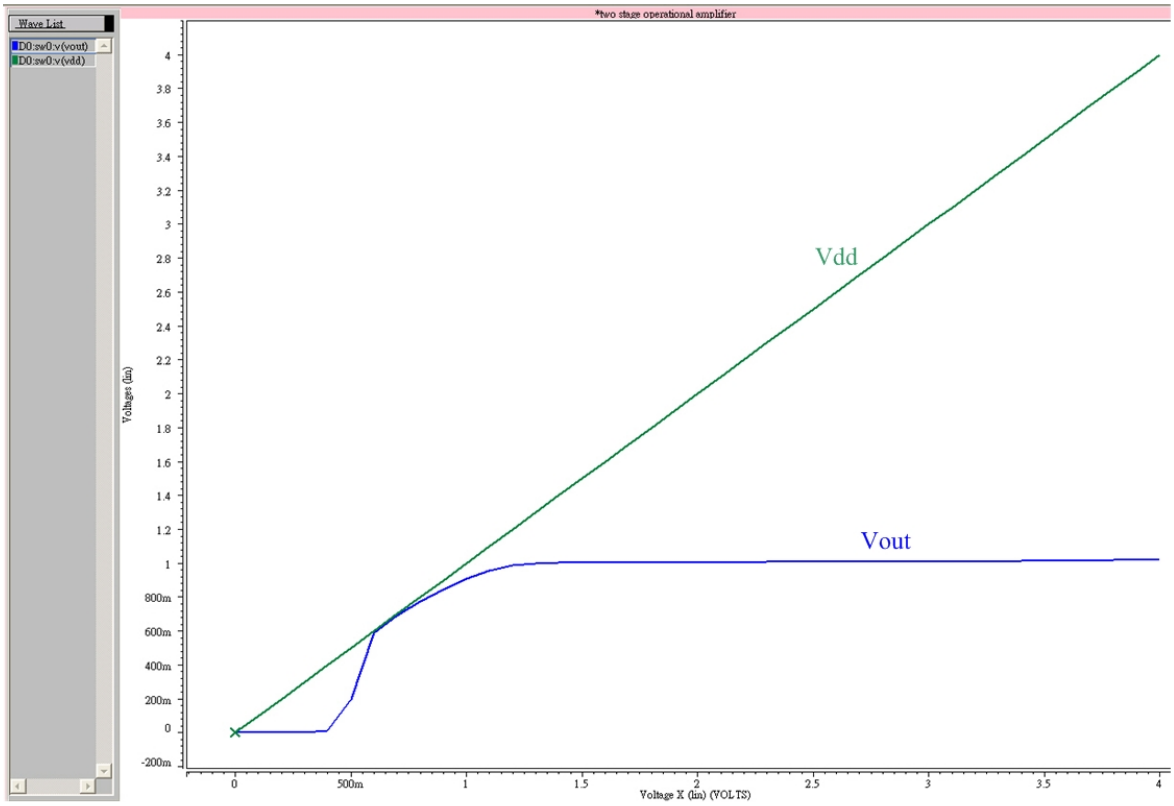

Fig. 5-8 Input/Output voltage characteristics of the firs output voltage (1.0 V)

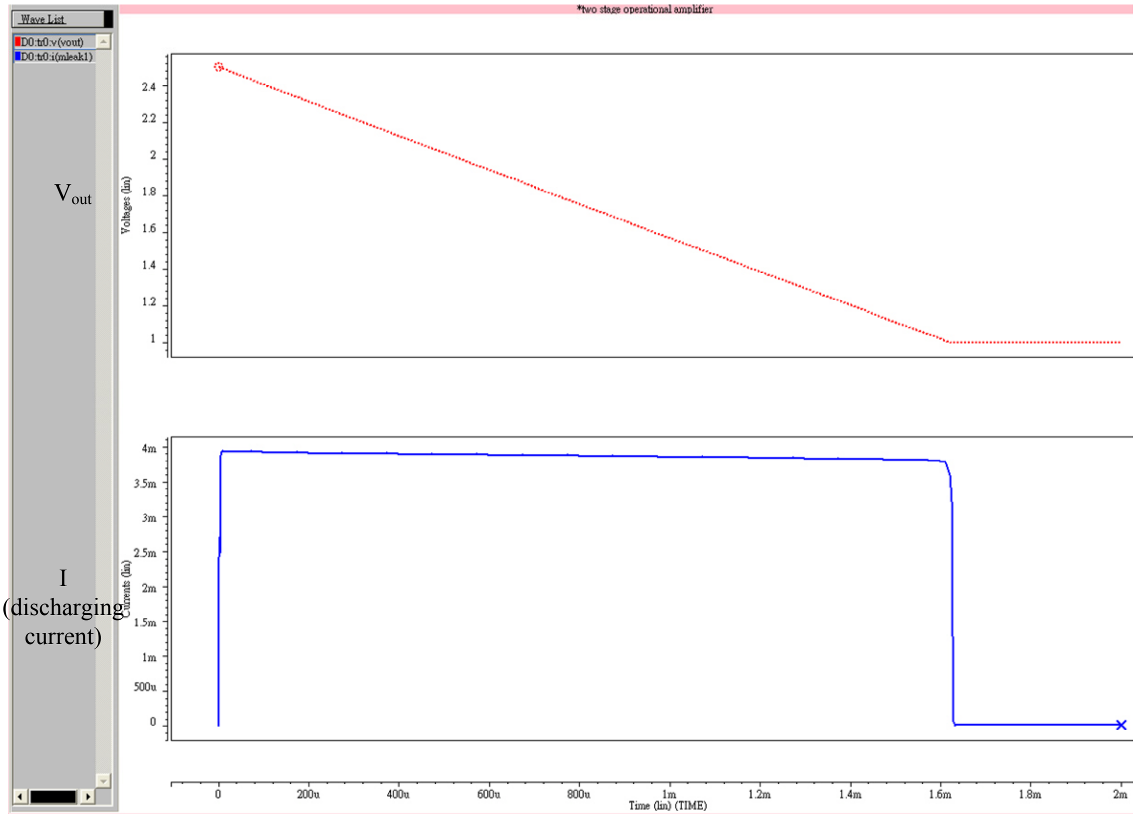

Fig. 5-9 Simulation of output voltage discharges from 2.5 V to 1.0 V

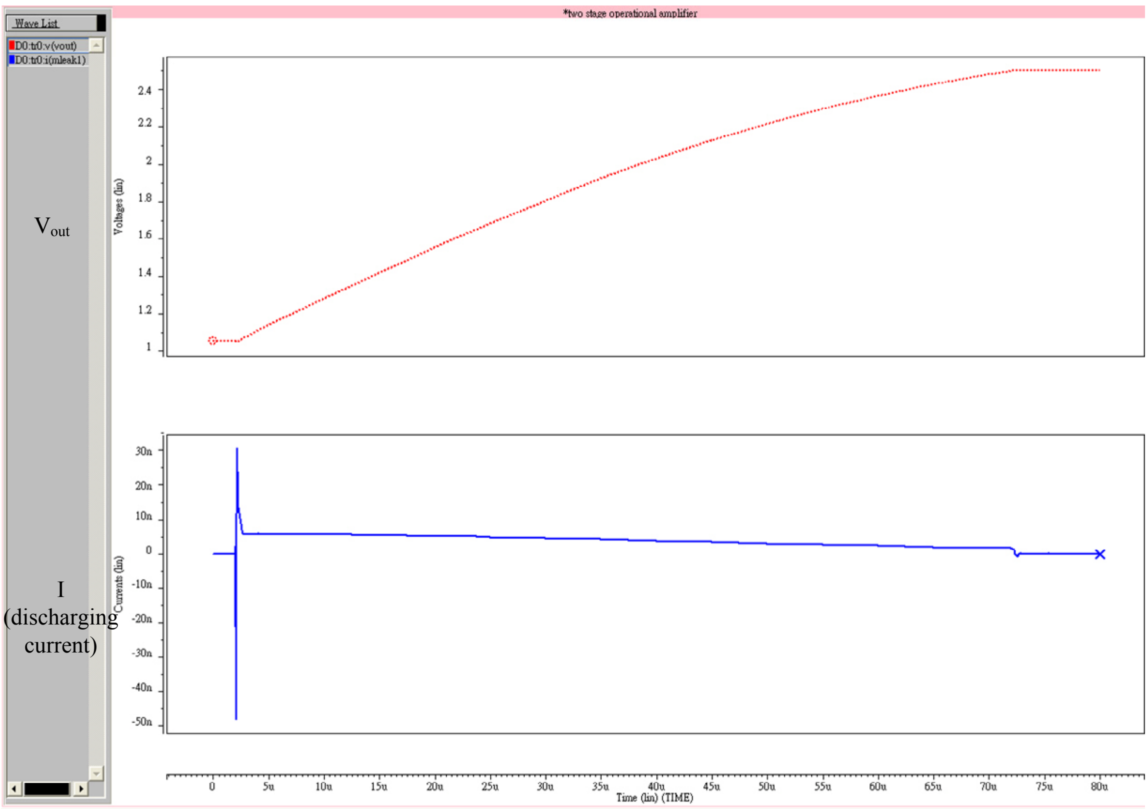

Fig. 5-10 Simulation of output voltage charges from 1.0 V to 2.5 V

Parameter / Size (μm)	Discharging time (μs)	Leakage current (μA)
0	850000	0
200	1570	18.7
400	790	29.68
800	398	46.08
1600	202	70.26

Table 5-2 Discharging time and leakage current under different sizes of the discharging transistor

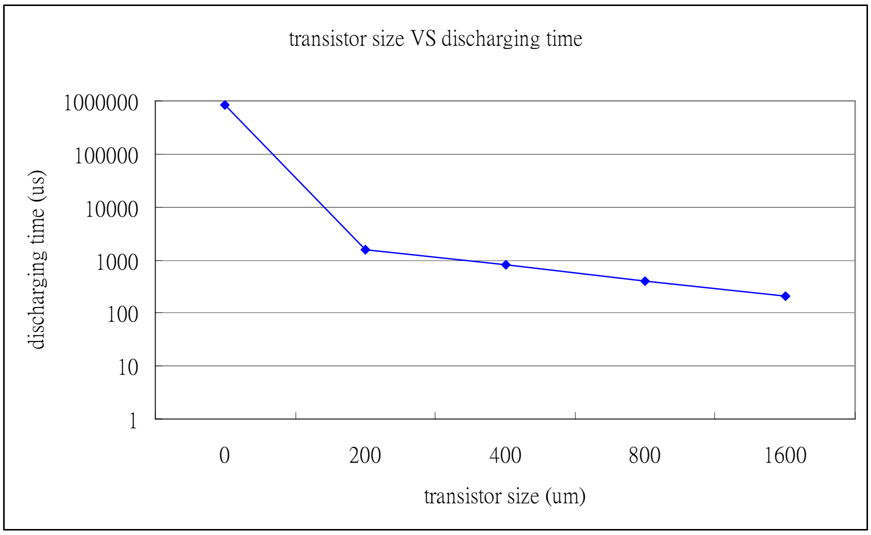

Fig. 5-11 Discharging time under different sizes of the discharging transistor

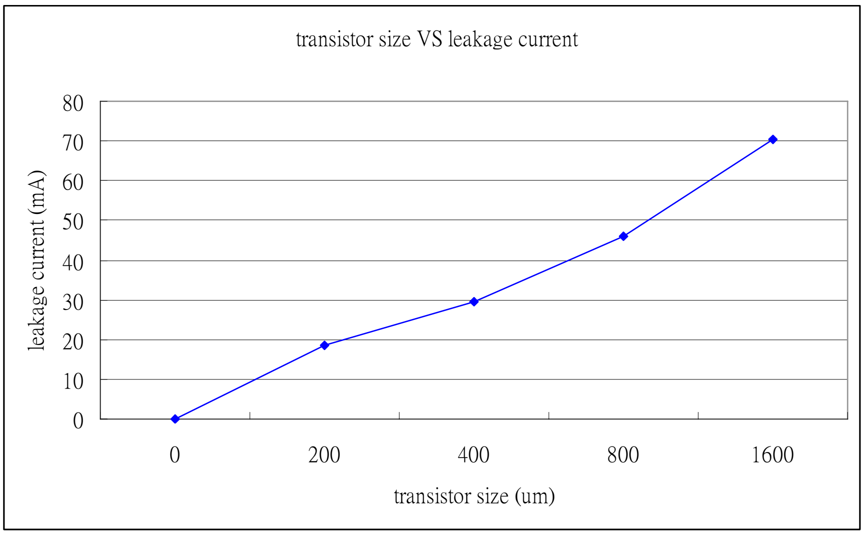

Fig. 5-12 Leakage current under different sizes of the discharging transistor

Specifications (External Control Signal)	External Control Signal	
	0V	3.3V
Power supply voltage(Vin)	3.3V	
Output voltage (Static characteristic)	2.5V	1.0V
Change in output voltage (△Vout) (@Iload from 0mA to 100mA)	12mV	10mV
Change in output voltage (△Vout) (@Vin from 2.97 to 3.63V)	65mV	65mV
Temperature Coefficient 0˚C to 100˚C	24 ppm/˚C	10 ppm/˚C
Load regulation (Static characteristics) 0mA＜Iload＜100mA	1µ V/mA	1µ V/mA
Line regulation (Static characteristics) 2.97 V＜Vdd＜3.63 V	15 mv / V	7 mv / V
Response time (@ Iload: from 0 to 100 mA)	2µ sec	1.5µ sec
Response time (@ Iload: from 100 to 0 mA)	6µ sec	5µ sec

Table 5-3 Summary of Simulation Results under different External Control Signal

Name	Proposed Adjustable LDO linear regulator
Technology	TSMC 0.18µm 1P6M
Area (included pads)	520*500µm^2
Power Consumption (@ Iload = 0mA)	256.5972µ W
Quiescent current in ARVG	7µ A
Leakage current in discharging path	20µ A
Transformation time (from 2.5V to 1.0V)	1.7m sec
Transformation time (from 1.0V to 2.50V)	38µ sec

Table 5-4 Information of the proposed Adjustable LDO linear regulator

5.3 Corner Case Simulation of Adjustable Reference Voltage Generator

The circuits which are realized in CMOS technology are sensitive to the process variations. Since the adjustable reference voltage generator is designed by utilizing CMOS technology, the temperature-dependence of the reference voltages is affected by the process variation. Moreover, the absolute value of reference voltages which is generated from the stack of threshold voltages is also influenced by the process variation. Therefore, additional trimming work is required to compensate the process variation. Fig. 5-13 shows the schematic of reference voltage generator with relevant trimming options. The resistors R1 and R2 are used to regulate the bias current which is generated from the self biasing current. The MP and MN transistor is used to properly tune the bias point in order to reduce the temperature-dependence of the reference voltage. The results of simulating reference voltage's temperature-dependence in different corner case are shown in Table 5-5 and Fig. 5-17, Fig. 5-18.

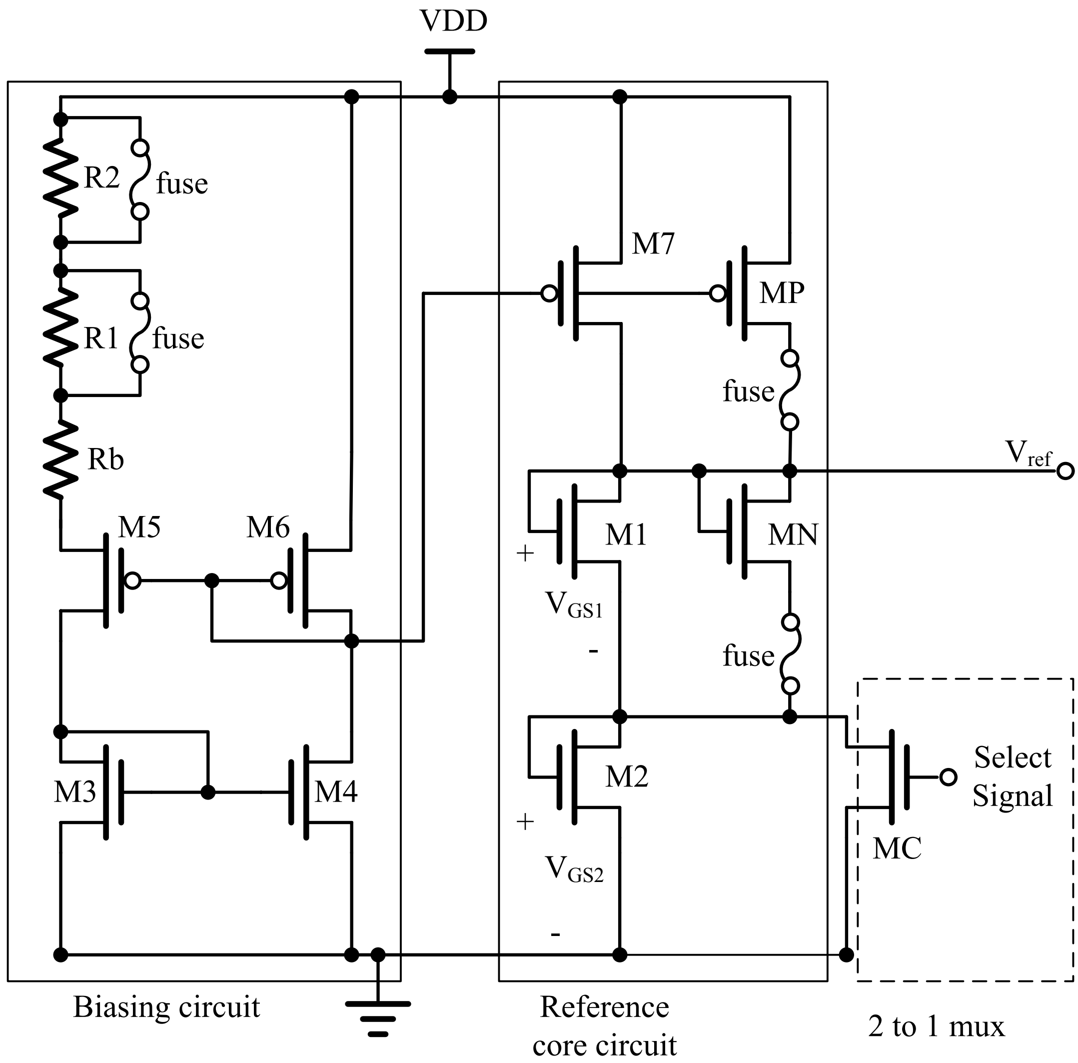

Fig. 5-13 Schematic of adjustable reference voltage regulator with relevant trimming options

Corner / Terms	TT	FF	SS	SF	FS
Vref1	2.3283 V	2.1834 V	2.4771 V	2.4213 V	2.2408 V
Vref1's TC	24 ppm/°C	25 ppm/°C	28 ppm/°C	31 ppm/°C	26 ppm/°C
Vref2	0.9812 V	0.9277 V	1.0354 V	1.0163 V	0.9483 V
Vref2's TC	10 ppm/°C	10 ppm/°C	11 ppm/°C	12 ppm/°C	10 ppm/°C

Table 5-5 Corner case simulation of adjustable reference voltage generator

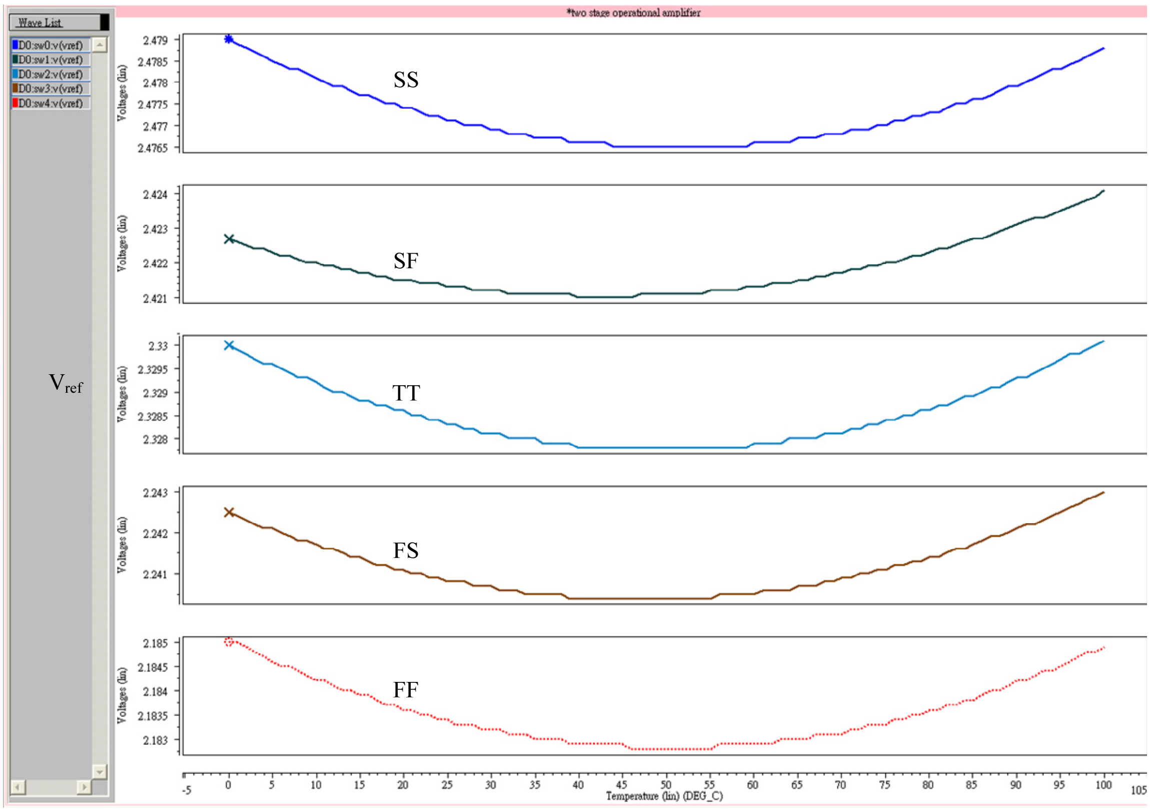

Fig. 5-14 Temperature behavior of the first reference voltage in different corner case

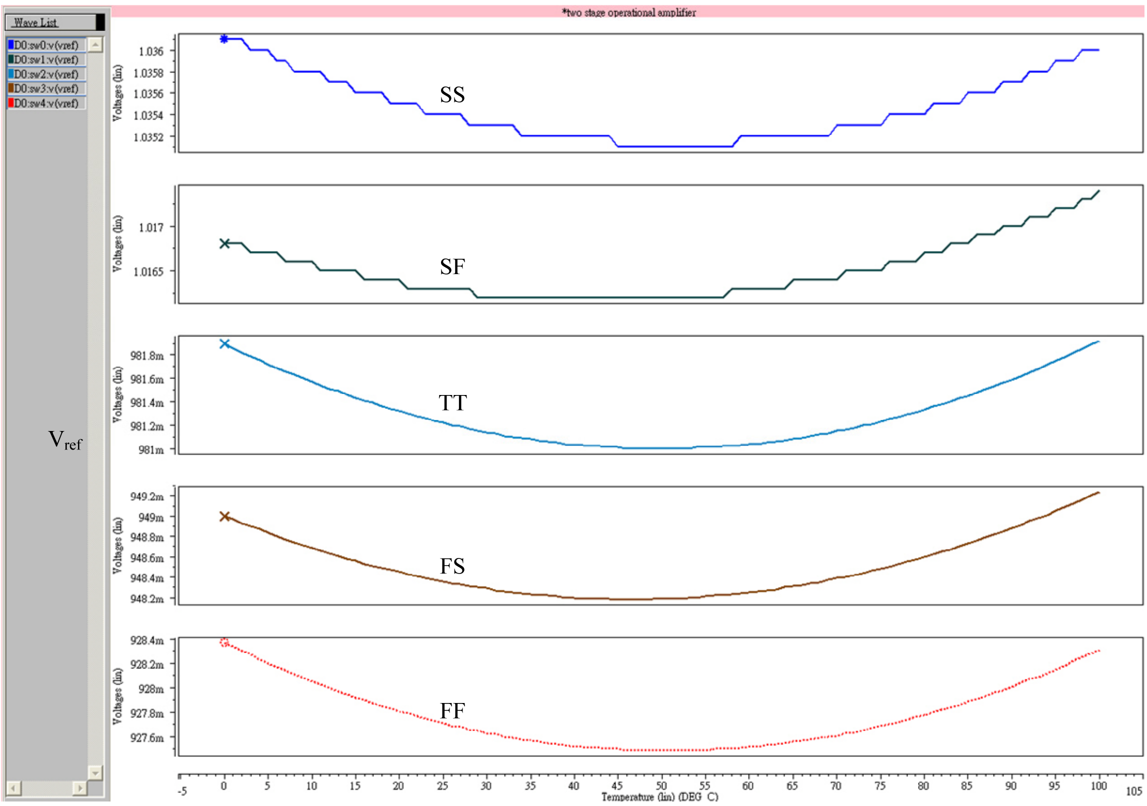

Fig. 5-15 Temperature behavior of the first reference voltage in different corner case

According to the simulation results, we can find out the temperature-coefficient of reference voltages is below to 40 ppm/°C. However, the absolute value of reference voltages is still affected by the process variation. So the output voltage should be modulated by the feedback resistors in order to achieve expected value. The method of modulation is shown in Fig. 5-16, where resistors R1 ~ R5 are used to regulate the value of feedback path, and transistors MCL1 ~ MCL4 are used to bypass the resistors or not controlled by Vc1 ~ Vc4. The simulation results of output voltages under load current variation in different corner case are shown in Fig. 5-17 and Fig. 5-18.

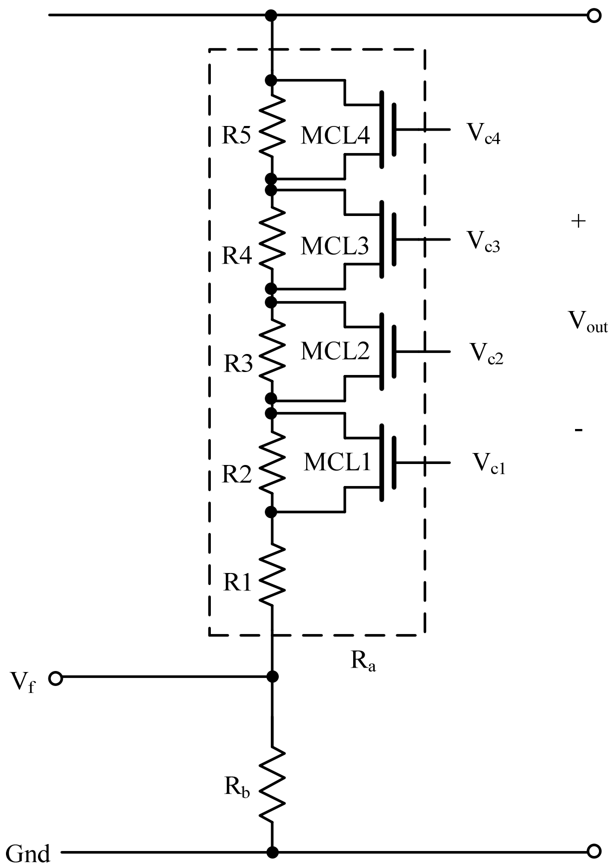

Fig. 5-16 Feedback path with trimming options

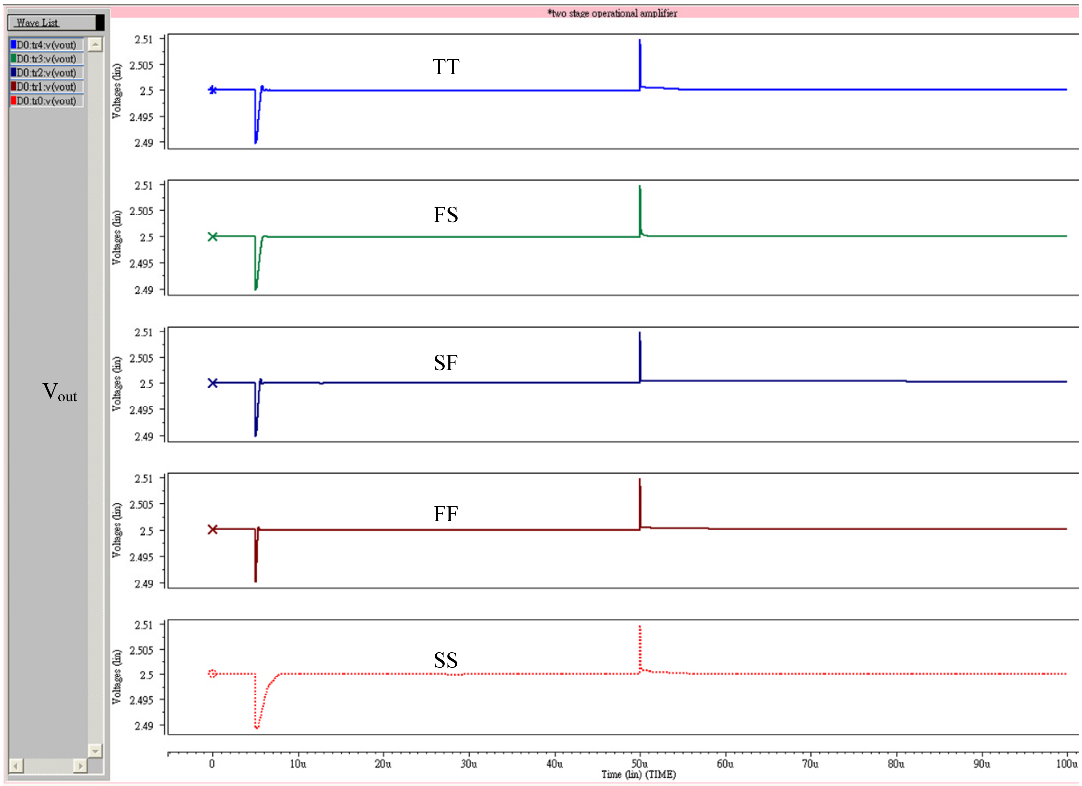

Fig. 5-17 Corner case simulation of the first output voltage (2.5V) under a full load current change (Iload = 0 ~ 100 mA)

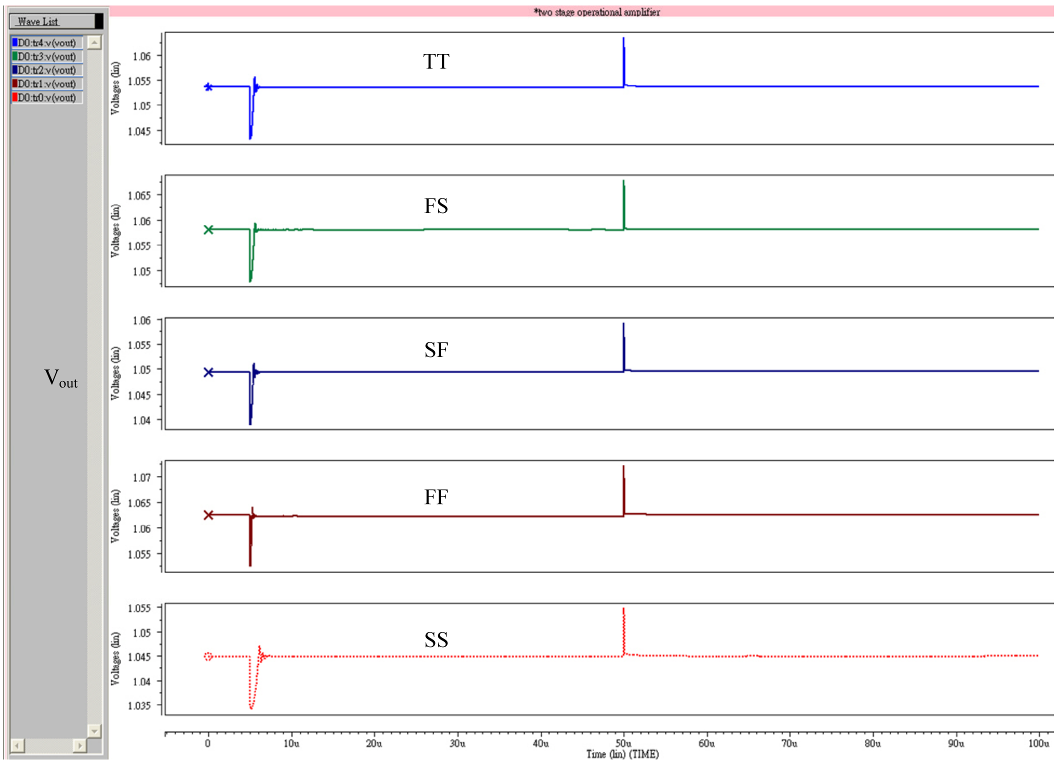

Fig. 5-18 Corner case simulation of the second output voltage (1.0V) under a full load current change (Iload = 0 ~ 100 mA)

Chapter 6

Conclusions and Future Work

6.1 Conclusions

In this thesis, the design and implementation of an adjustable low dropout voltage regulator is presented. There are mainly four different structures discussed in the thesis, and their advantages/disadvantages and characteristics are compared to each other. The proposed adjustable reference voltage generator, which is modified from the traditional beta multiplier voltage reference, has great extendibility because of low power consumption and some area. In addition, its structure is simple and the tuning technique is easier than other adjustable reference voltage generator circuit.

In the traditional design of low dropout voltage regulator, the transient response is mostly dependent on the feedback resistance and requires a large discharging time. The problem of transient response becomes serious in the design of adjustable low dropout voltage regulators. It is because that the amount of the difference between output voltages is quite large, and the feedback resistors can not efficiently discharging the output voltage. We proposed a dynamic discharging path. It can efficiently speed up the discharging process and reduce the recovering time. With using dynamic discharging path, the performance of load circuit can be increased without limit to the bad transient response of traditional low dropout voltage regulators. The structure of dynamic discharging path is very simple, and the amount of discharging current can be regulated easily by properly designing the level-shift buffer.

6.2 Future Work

In the future, we can further extend the previous research to increase the number of reference voltages efficiently. It is possible to producing reference voltages by utilizing diode-connected transistors with low threshold voltage. Since the threshold voltage is lower, the amount of difference between reference voltages is also small. So the number of diode-connected transistor can be raised.

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