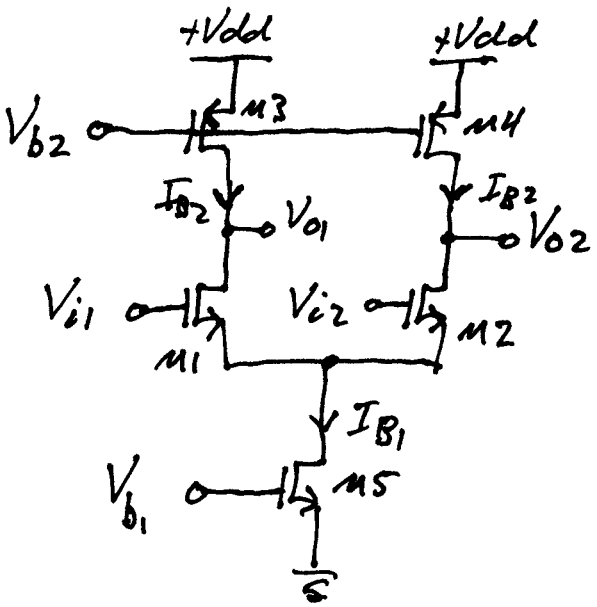
Single-Stage Diff. Amps

- As seen in the diff. pair notes, active loading is required to achieve high gain, just as seen in the CS amp discussion.
- One option is to apply I-source loading (as in CS-amp)



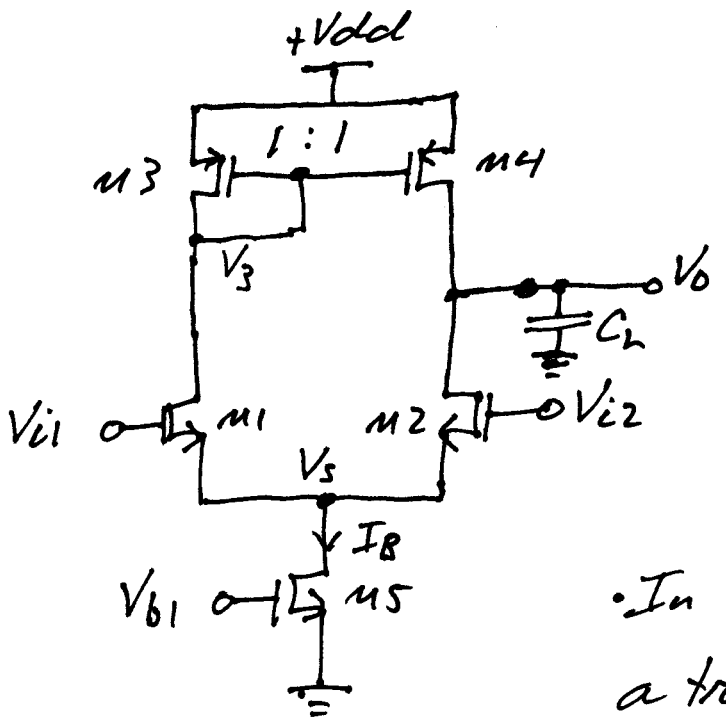
- SSm same as before with $R_L = r_{ds_{3,4}}$

$$\Rightarrow A_{dm} = \frac{v_{od}}{v_{id}} = -g_{m_{1,2}}\left(r_{ds_{1,2}} \| r_{ds_{3,4}}\right)$$

- Note: $v_{od} = v_{o1} - v_{o2}$; if only <u>one</u> output is used $\Rightarrow$ half gain!

- However, there is a biasing problem: we must have: $I_{B1} = 2 \cdot I_{B2} \Rightarrow$ with such high imped. at V_o, even small differences due to I-mirror errors in generating V_{b1} & V_{b2} may cause V_{OC} to push $M_{3,4}$ or $M_{1,2}$ into triode.
- This circuit requires <u>active feedback</u> to control V_{b1} & V_{b2}: Common-Mode feedback (<u>CMFB</u>).

- CMFB circuits will be introduced at the end of the semester.
- Another solution which avoids the need for CMFB & converts the diff. output into a single-ended output is a I-mirror load (similar to "self-biasing" in ref circuits):



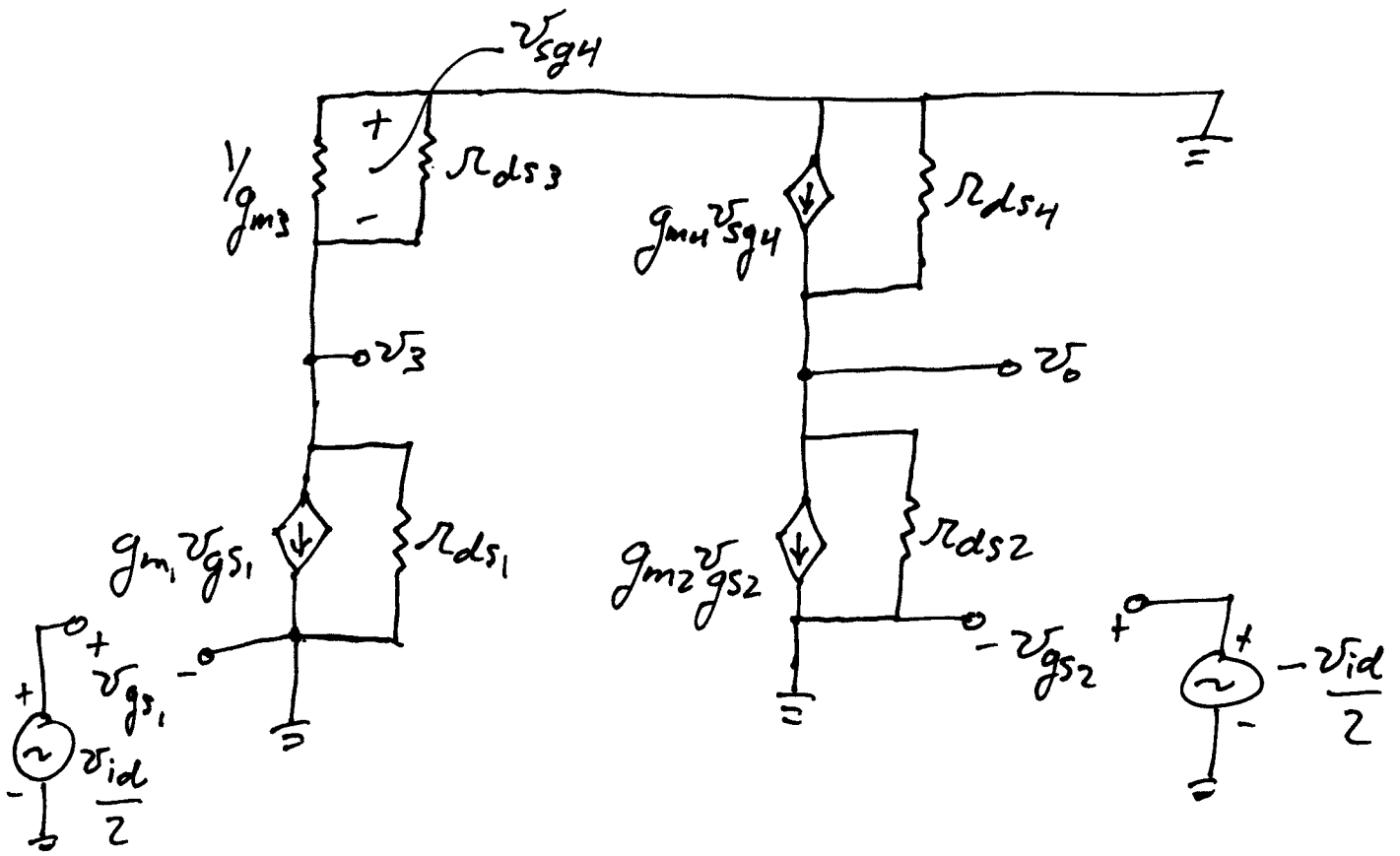
- Now only a single bias is used, I_B
- The mirror $M_{3,4}$ provides biasing & mirrors gain from M_1 to the single ended output, V_o.
- In the SSM, V_s is no longer a true small-signal gnd.
- However, it is still low imped. & the approx of $V_s = 0$ for diff inputs still gives good results & intuitive design-oriented insight.

* To solve SSM: (same as a/ R_L loading)
- Diff input: $V_s \approx 0$.
- Common input: split M5 to two 2·Rdss & open circuit @ V_s.

- Also, use I-mirror of $M_{3,4}$ to transfer current gain of M_1 to V_o. We will show details below, but move directly to output node in the future (& assume perfect I-mirror).

- Solve diff. gain: $A_{dm} = \dfrac{v_o}{v_{id}}$ ← single ended / ← differential

→ set $v_s \approx 0$



$$\Rightarrow v_{gs1} = \frac{v_{id}}{2} = -v_{gs2} \; ; \; v_{sg4} = -v_3$$

$$v_3 = -\left(g_{m1}\frac{v_{id}}{2}\right)\left(r_{ds1} \| r_{ds3} \| \frac{1}{g_{m3}}\right) \overset{\text{neglecting } r_{ds}}{\approx} -\left(g_{m1}\frac{v_{id}}{2}\right)\left(\frac{1}{g_{m3}}\right)$$

$\Rightarrow \frac{v_{sg4}}{g_{m4}} = \left(\frac{g_{m1} v_{id}}{2}\right)\left(\frac{1}{g_{m3}}\right) g_{m4}$

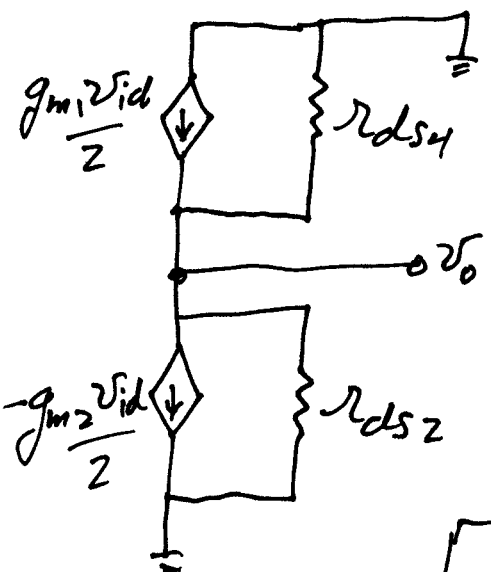
$= \left(\frac{g_{m1} v_{id}}{2}\right)$ $\Rightarrow$ by neglecting r_{ds1} & r_{ds3}, can assume i-source of M4 is equal to source of M1!

↑ Current from M_1

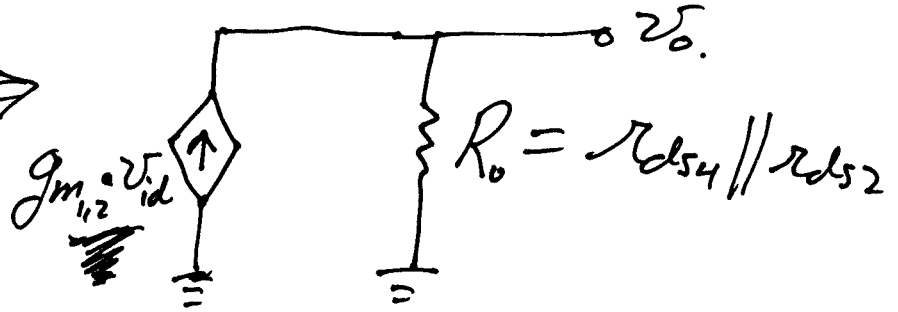
device transconductance.

$\Rightarrow$ Right-half circuit is modeled as:

• for $g_{m3} = g_{m4}$; $g_{m1} = g_{m2}$



$\Rightarrow$



$\Rightarrow$ $\boxed{A_{dm} = \frac{v_o}{v_{id}} = g_{m1,2} \cdot R_o}$ ← Same as CS-amp.

• Note: A_{dm} is non-inverting because of the definition of $V_{id} = V_{i1} - V_{i2}$ $\Rightarrow$ (+) non-inverting input is V_{i1} & (−) inverting input is V_{i2}.

In general, you can find the (+) & (−) inputs by starting at a given input & counting the # of inv. & non-inv. stages from input to output. For pg. 2, from V_{i1},

two stages: (−) · (−) = (+) ⇒ non-inverting input.
↑ M1, CS ↑ M4, CS

- from M2: (−) = (−) ⇒ inverting input.
↑ M2, CS

- The CMRR can be solved from the SSm as well. We will not show details here, but qualitatively it can be seen that variations in $\uparrow V_{IC} \Rightarrow \uparrow V_S \Rightarrow \uparrow I_B \Rightarrow \uparrow I_{O1} + \uparrow I_{O2}$
↑ $V_{GS1,2}$ × const. ↑ due to ↓ of M_5

- Since $\uparrow I_{O1} = \uparrow I_{O2} = \frac{\uparrow I_B}{2}$, if I-mirror M_3 & M_4 is ideal ⇒ $\underline{\uparrow I_{D4} = \uparrow I_{O2}}$ } two cancel & result in no change in V_O ⇒ $\underline{A_{cm} \approx 0}$

• Thus $CMRR = \frac{A_{dm}}{A_{cm}} \approx \infty$

• In reality M_3/M_4 I-mirror is not ideal ∴ CMRR depends on $\left[g_{m1,2}(2r_{ds5})\right] \neq g_{m3,4} \cdot R_o$

↑ quality of I_B ; quality of I-mirror.

$\Rightarrow CMRR \approx g_{m1,2}(2r_{ds5}) \cdot g_{m3,4} \cdot R_o$

→ e.g. see [Gray/Meyer] 4.3.5.

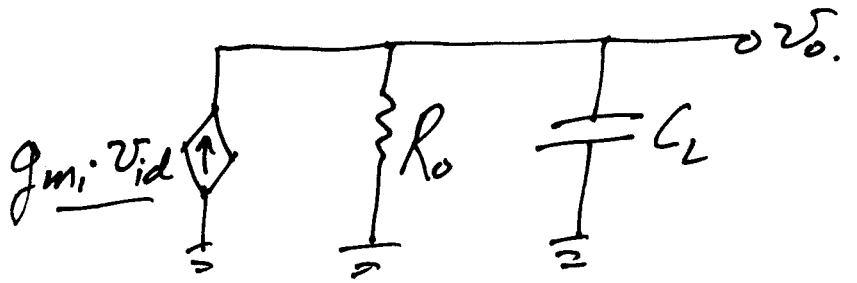
• Solve for approx BW: ZVTC requires adding all τ_i's ⇒ many caps even in simple circuit of pg 2. Also, now there are two signal paths to the output with different delays in each path → requires modification to ZVTC for exact solution.

⇒ 1st: we will search for a dominant τ_i with large R_{Di} & C_i ⇒ if there is a clear dominant τ_i that affects both signal paths, then we can neglect smaller τ_i's for BW estimate.

- for pg 2 circuit: only large impedance node is $v_o \Rightarrow$ dominant τ_o, especially if C_L = large.

- Note: By neglecting smaller τ_i's in ZVTC, the method is no longer guaranteed to be conservative, and may overestimate the BW.

- Include C_L in simplified ssm of pg 4:



$A_{dm} = g_{m_1} \cdot R_o$

$R_o = r_{ds_4} \| r_{ds_2}$

$BW \simeq \dfrac{1}{2\pi R_o C_L}$

- Next: Consider large-signal & biasing constraints on input & output signals for the A_{dm}, R_o & BW estimates to be valid.

$\Rightarrow$ primary constraint: all devices active.

- Consider first DC biasing of input & output.
- We need to know V_O to determine op-modes.
- Generally, V_O must be forced to a desired point by applying V_{IO} (DC diff. input) for biasing.
- Define: $V_{OFFSET} = V_{off}$ = "offset voltage"

V_{off} = V_{IO} required to force V_O to desired DC operating point.

- If $V_{IO} = 0$, find V_O in pg2 fig: assume 1st that I-mirror M3/M4 is ideal:

$\Rightarrow I_{D1} = I_{D2} \Rightarrow$ for matched devices

$$\begin{cases} I_{D1} = K_{1,2}(V_{IC} - V_S - V_t)^2(1 + \lambda(V_3 - V_S)) \\ I_{D2} = K_{1,2}(V_{IC} - V_S - V_t)^2(1 + \lambda(V_O - V_S)) \end{cases}$$

$\Rightarrow \underline{V_3 = V_O}$

* If this is desired $V_O \Rightarrow \underline{V_{off} = 0}$.

$\Rightarrow$ In reality: M3/M4 is not perfect I-mirror & matching is not perfect $\Rightarrow V_{off} \neq 0$ ($100's\ \mu V$ to mV)

• Let's neglect these errors: $V_{off}=0$, $V_{ID}=0$.

$V_O = V_3$ (DC op)

• Now, solve input common mode range (ICMR) to maintain active operation:

$$(V_{IC})_{max} = V_{dd} - V_{SG3} + V_{t1} = V_{dd} - V_{ov3} - V_{t3} + V_{t1}$$

$M_{1,2}$ Triode

may cancel or be small + or −

$$\simeq V_{dd} - V_{ov3} \Rightarrow \text{Can get close to } V_{dd}!$$

$$V_{ov3} = \sqrt{\frac{I_3}{K_3}}$$

$$(V_{IC})_{min} = 0 + V_{ov5} + V_{GS1,2} = V_{ov5} + V_{ov1} + V_{t1}$$

$2V_{ov} + V_t$!

M_5, Triode

$\Rightarrow$ at least 1V above GND (or $-V_{SS}$).

Note: use p-mos diff pair $\Rightarrow$ - close to GND. (within V_{ov})

- $2V_{ov} + V_t$ below V_{DD}

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- Output voltage range:

$(V_o)_{max} = V_{dd} - V_{ov4}$ ⇐ close to V_{dd}.

↑ M_4, Triode

$(V_o)_{min} = V_{IC} - V_{t2}$ ⇐ Limited by V_{IC} ⇒ not good!

↑ M_2, triode

- Note: Limits for ICMR & (V_o) range are the extreme limits. At these points, only infitesimally small ac signals can be applied & maintain active devices. To amplify larger signals, V_{IC} or V_o will have to be appropriately biased away from these limits.

- The last large-signal limitation we will adress is slew-rate (SR), which limits the amount of current that can be supplied to caps during transients.

• Since $i_c = C\frac{dv}{dt} \Rightarrow SR_c^+ = \left(\frac{dv}{dt}\right)_{max+} = \frac{I_c^+}{C}$ 11/16

$SR_c^- = \left(\frac{dv}{dt}\right)_{max-} = \frac{I_c^-}{C}$, where

I_c^+ = max positive current that can be delivered to C with large Vid.

I_c^- = max negative current . . .

• For fig on pg. 2 ⇒ consider C_L:

$I_{C_L}^+ = I_B \rightarrow$ large +Vid ⇒ M_2 cutoff, $I_{D4} = I_B$

$I_{C_L}^- = I_B \rightarrow$ large -Vid ⇒ M_1, M_3, M_4 cutoff

$I_{D2} = I_B$

⇒ SR limits are generally achieved when one or more devices enter <u>cut-off</u>.

⇒ For pg 2: $\boxed{SR_{C_L} = \frac{I_B}{C}}$ ← both pos & neg. (Symmetrical).

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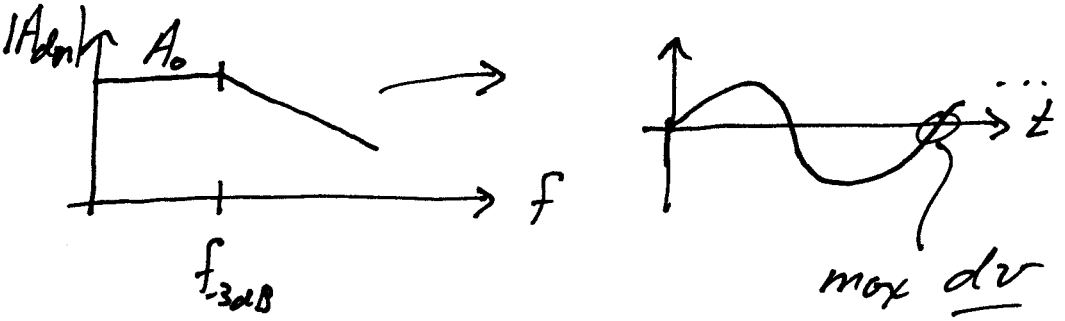
- Relationship between SR & BW:

→ BW: small-signal estimate of ~~max~~ freq. where signals are attenuated by -3dB (0.708), regardless of absolute amplitude.

SR: large-signal limitation on $\frac{dv}{dt}$ due to finite bias current ⇒ devices enter cut-off, directly dependant on signal amplitude.

- from SSM:



- for $v_{in} = V_i \sin \omega_x t$, expect:

$v_o = V_o \sin \omega_x t$, $\frac{V_o}{V_i} = A_o$ for $\omega_x < \omega_{-3dB}$,

(neglecting ~~@~~ -3dB attenuation & -45° phase shift @ f_{-3dB}).

$$\Rightarrow \left.\frac{dv_o}{dt}\right|_{t=0} = \left. V_o \omega_x \cos \omega_x t \right|_{t=0}$$

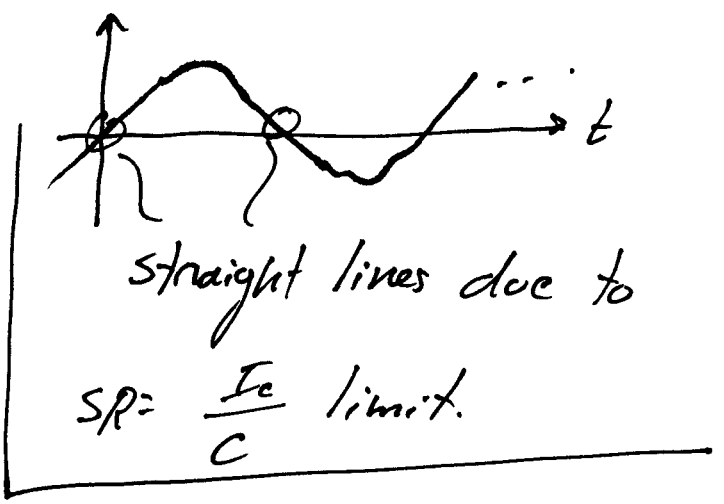
$$= \underline{\underline{V_o \omega_x}}$$

- Therefore, ssm predicts $\frac{dv}{dt}$ up to $\underline{V_o \omega_x}$

with ω_x up to $\omega_{-3dB} \Rightarrow \frac{dv}{dt}$ up to $\underline{V_o \cdot \omega_{-3dB}}$

- If SR limit: $SR < V_o \cdot \omega_{-3dB} \Rightarrow$ will have a large-signal SR limit near zero crossings.

leading to distortion:



- For step response:

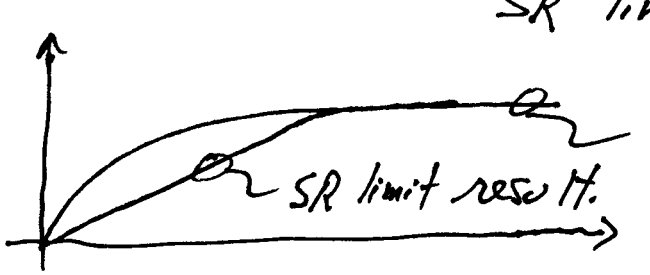
ssm w/ single pole @ f_{3dB}:

$$v_o = V_o (1 - e^{-t/\tau})$$

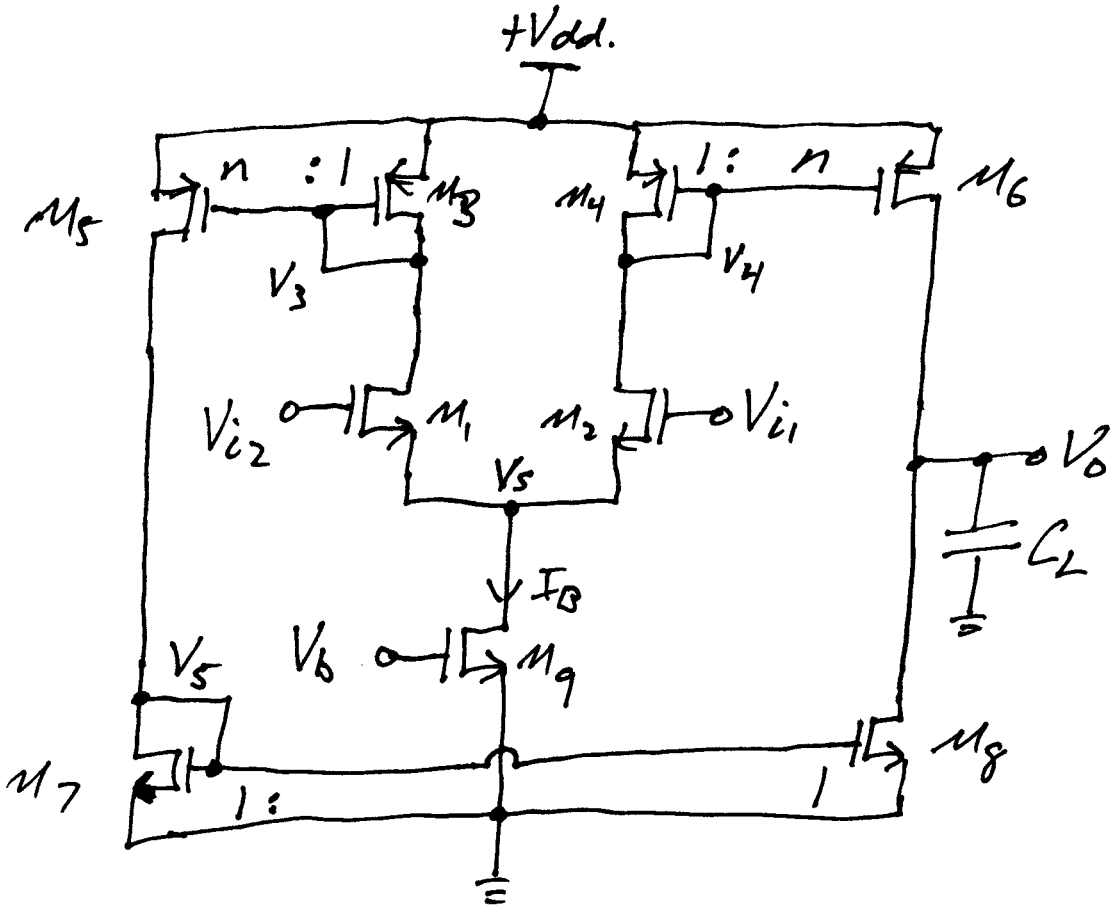
$$\Rightarrow \left.\frac{dv_o}{dt}\right|_{t=0} = \frac{V_o}{\tau}, \quad \tau = \text{time constant} \approx \frac{1}{\omega_{-3dB}}$$

$\Rightarrow \underline{V_o \cdot \omega_{-3dB}}$; if $SR < V_o \cdot \omega_{-3dB} \Rightarrow$ will have SR limit behavior.

$\Rightarrow$

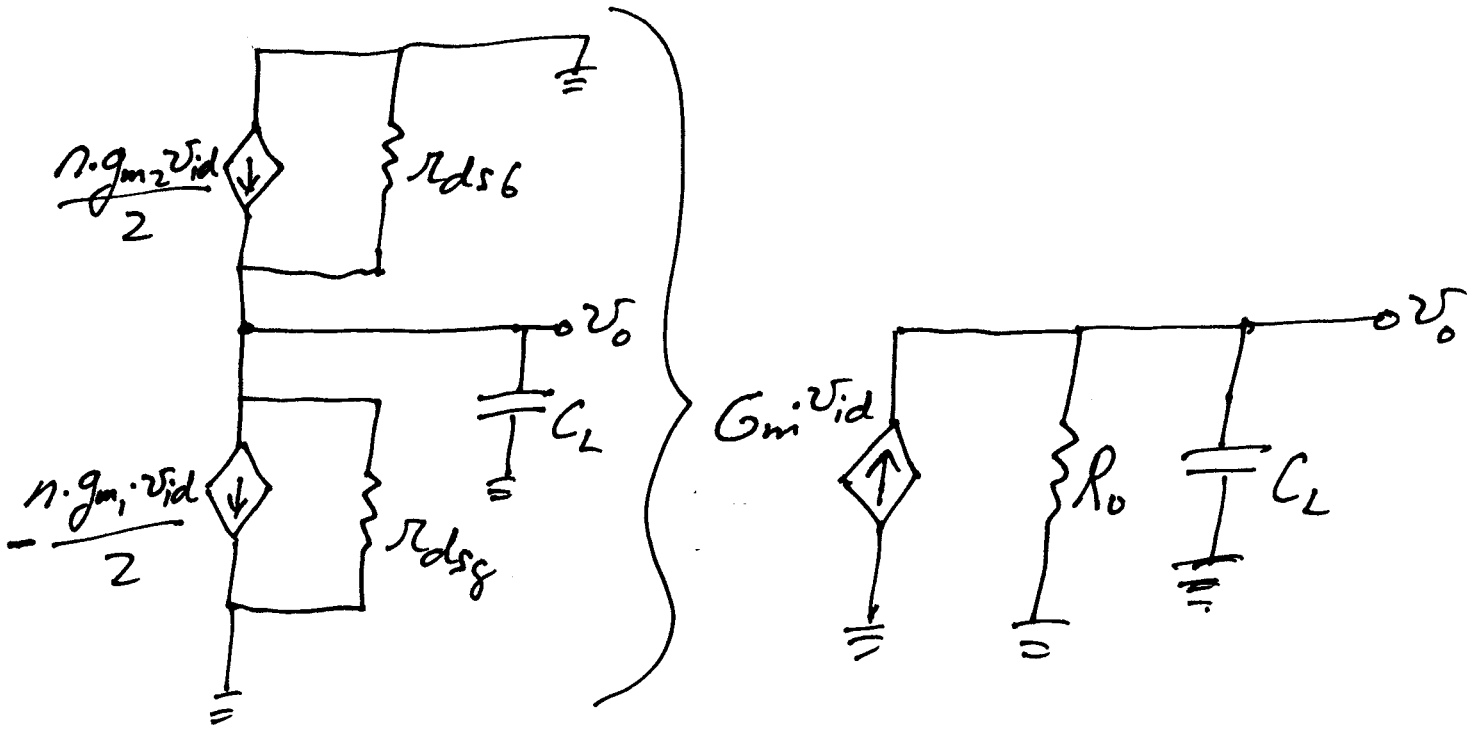


- A common single-stage amp that improves (V_o)range over pg.2, uses current mirrors to achieve wide (V_o)range:



- Essentially the same as pg.2, but with i'mirrors summing currents to output @ M6/M8.
- For SSm: again let $V_s \approx 0$ for v_{id}., use ideal i'mirrors to estimate gain to output. Only diff from pg.2 is gain of n in $M_{4/6}$ + $M_{3/5}$ mirrors.

⇒ SSm at output:



$$G_m = n \cdot g_{m1,2} = n \cdot 2 \cdot \sqrt{K_{1,2} \frac{I_B}{2}}$$

$$R_o = r_{ds6} \| r_{ds8} = \frac{1}{\frac{n \cdot \lambda_6 I_B}{2}} \Big\| \frac{1}{\lambda_8 \left(n \frac{I_B}{2}\right)}$$

$$BW \approx \frac{1}{2\pi R_o C_L}, \quad A_{dm} = G_m \cdot R_o.$$

$$\Rightarrow A_{dm} \cdot BW = \text{"gain} \cdot \text{Bw product"} = \frac{G_m}{2\pi C_L}$$

↳ independant of R_o. ⇒ more on this later.

- DC limitations & SR essentially same as pg 2.

$$(V_{IC})^{+}_{max} = V_{dd} - V_{SG3} + V_{t1} = V_{dd} - V_{ov3} + V_{t1} - V_{t3}$$

$$(V_{IC})_{min} = V_{ov4} + V_{ov1} + V_{t1}$$

$$\left.\begin{aligned}(V_o)_{max} &= V_{dd} - V_{ov6} \;;\; (V_o)_{min} = V_{ov8}\end{aligned}\right\} \text{improved!}$$

$\Rightarrow$ near "rail-to-rail" output!

$$SR^{+} = SR^{-} = \frac{n \cdot I_B}{C_L}$$

- Total DC power loss ("quiescent power")

$$\Rightarrow V_{dd} \cdot I_{TOT} = V_{dd}\left(\frac{n I_B}{2} + I_B + \frac{n I_B}{2}\right)$$

$$P_Q = V_{dd} \cdot I_Q = V_{dd}(I_B(n+1))$$

- Note: pg14 circuit is called "Symmetrical OTA"

Since M_1/M_2 loading is symmetrical. $\Rightarrow$ OTA = operational transconductance amplifier (Vid to current output).

high output imped.

& Next: design procedure given specs...