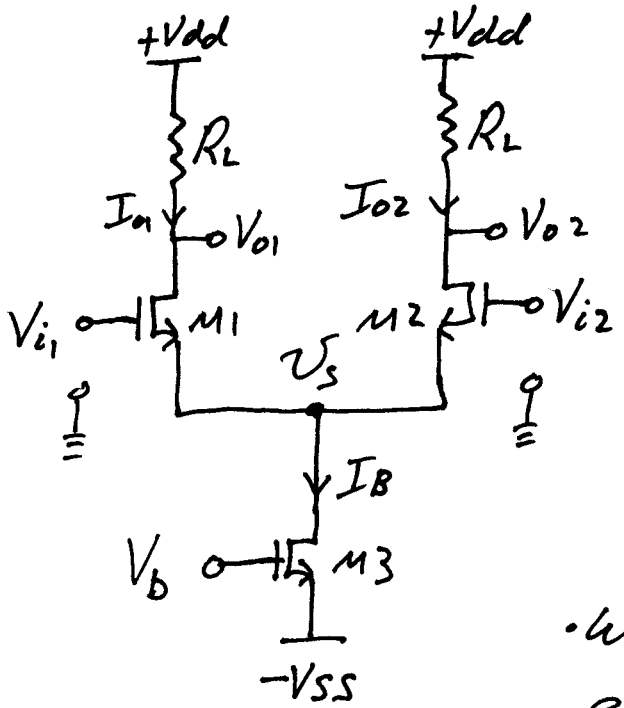


# Differential Pair

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• Consider a basic source-coupled diff-pair:



• Can solve <sup>SSM</sup> w/ superposition:

$$V_{o1} = A_{v1} \cdot v_{i1} + A_{v2} \cdot v_{i2}$$

$$\left. \begin{aligned} A_{v1} &= \frac{v_{o1}}{v_{i1}} \Big|_{v_{i2}=0} \\ A_{v2} &= \frac{v_{o1}}{v_{i2}} \Big|_{v_{i1}=0} \end{aligned} \right\} \begin{array}{l} \text{solutions} \\ \text{may} \\ \text{be} \\ \text{difficult} \end{array}$$

• We will show that it is easier to solve if we take advantage of symmetry by re-defining the inputs:

## Common-Mode:

$$V_{ic} = \frac{V_{i1} + V_{i2}}{2}, \quad V_{oc} = \frac{V_{o1} + V_{o2}}{2} \left\{ \begin{array}{l} V_{i1} = V_{ic} + V_{id}/2 \\ V_{i2} = V_{ic} - V_{id}/2 \end{array} \right.$$

## Diff-mode

$$V_{id} = V_{i1} - V_{i2}, \quad V_{od} = V_{o1} - V_{o2} \left\{ \begin{array}{l} V_{o1} = V_{oc} + V_{od}/2 \\ V_{o2} = V_{oc} - V_{od}/2 \end{array} \right.$$

• From here, there are two key equations that govern circuit operation:

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$$\left. \begin{aligned} (1) \quad V_{id} &= V_{gs1} - V_{gs2} \\ (2) \quad I_{o1} + I_{o2} &= I_B \end{aligned} \right\} \#$$

- Consider first the DC response:

1) Common-mode only:  $V_{id} = 0 \Rightarrow V_{gs1} = V_{gs2}$

$\Rightarrow$  if  $k_1 = k_2$  (matched devices) & all devices active.

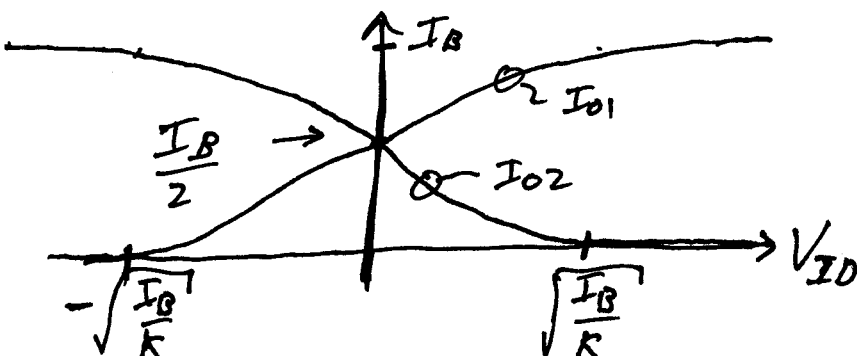
$$\Rightarrow I_{o1} = I_{o2} = I_B/2$$

$$\Rightarrow V_{o1} = V_{o2} = V_{oc} = V_{dd} - \frac{I_B R_L}{2} ; \underline{V_{od} = 0}$$

# Note: ideally, both CM & DM output are indep. of the CM input

$\Rightarrow$  This allows simple cascading of stages & if true in ssm results in rejection of common noise.

2) Differential-mode:  $V_{ic} = \text{constant}$ , sweep  $V_{id}$



$$\begin{aligned} V_{id} &= V_{ov1} - V_{ov2} \\ &= \frac{\sqrt{I_{o1}} - \sqrt{I_{o2}}}{\sqrt{K_{1,2}}} \end{aligned}$$

• As we  $\uparrow V_{ID}$ , the bias current is diverted 3/6 from  $M2$  to  $M1$ , this continues until

$I_{O1} = I_B$ ,  $I_{O2} = 0 \Rightarrow M2$  cut-off boundary.

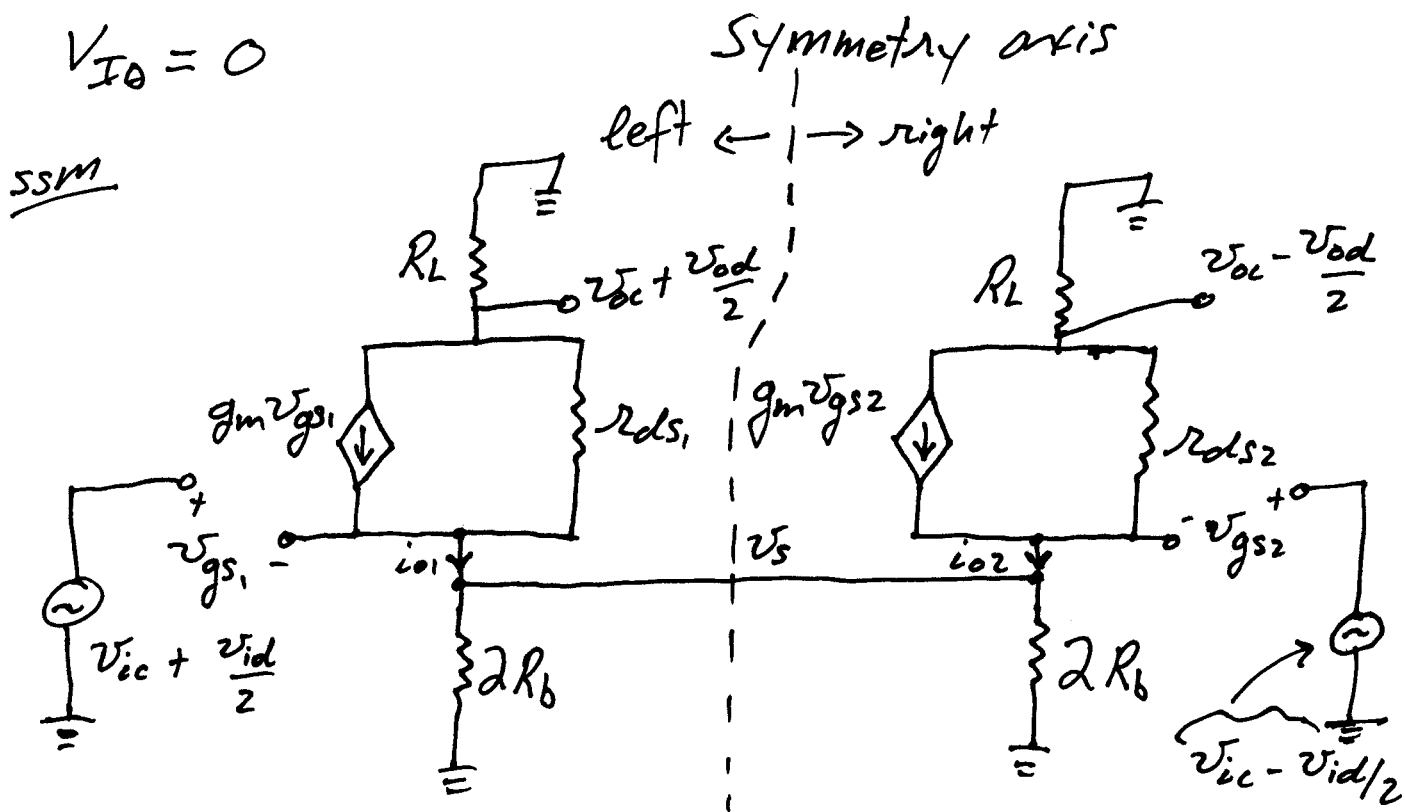
$$\Rightarrow @ V_{ID} = \begin{cases} +\sqrt{\frac{I_B}{k_{i,2}}} \Rightarrow M2 \text{ cutoff boundary} \\ -\sqrt{\frac{I_B}{k_{i,2}}} \Rightarrow M1 \text{ cutoff boundary} \end{cases}$$

$\Rightarrow$  Therefore, we can control the sensitivity of the input stage by adjusting  $I_B$  &  $k_{i,2}$ .

• Next, consider the SSM at the DC op-point:

$V_{IC} = \text{constant}$  (all devices active)

$$V_{ID} = 0$$



• The output resistance of the bias current source  $I_B$  (M3) has been modeled as  $R_b$  & split into two  $2 \cdot R_b$  in parallel to create a symmetric circuit.

• Now, we can use super-position to analyze CM & DM small-signal inputs separately:

$$A_{dm} = \left. \frac{v_{od}}{v_{id}} \right|_{v_{ic}=0}, \quad A_{cm} = \left. \frac{v_{oc}}{v_{ic}} \right|_{v_{id}=0} \left. \vphantom{\frac{v_{od}}{v_{id}}} \right\} \begin{array}{l} \text{with perfect} \\ \text{symmetry, there} \\ \text{is no} \\ \text{coupling CM} \rightarrow \text{DM} \\ \text{or DM} \rightarrow \text{CM.} \end{array}$$

• For CM only:  $v_{id}=0 \Rightarrow v_{od}=0$

$$\Rightarrow i_{o1} = i_{o2} = -\frac{v_{oc}}{R_L} \left. \vphantom{-\frac{v_{oc}}{R_L}} \right\} \begin{array}{l} \text{since currents are matched,} \\ \text{zero current flows between} \\ \text{left \& right half circuits.} \end{array}$$

• For DM only:  $v_{ic}=0 \Rightarrow v_{oc}=0 \Rightarrow i_{o1} = -i_{o2} = -\frac{v_{od}}{2} \cdot \frac{1}{R_L}$

$\Rightarrow$  Since  $i_{o1} = -i_{o2}$ , zero current flows into bias resistor  $2 \cdot R_b \Rightarrow$  zero volts at source node  $v_s$  on axis of symmetry.

• These results are true in general for 5/6  
 fully symmetrical circuits & allow  
 "half-circuit analysis" by:

(1) for CM only: all branches crossing the  
 axis of symmetry become open-circuit.  
 (since zero current flows in them)

(2) for DM only: all nodes on the axis  
 of symmetry become small-signal ground.  
 (since they have zero volts).

• Now, the  $A_{dm}$  &  $A_{cm}$  gains can be solved using  
 general CS-amp gain equations "by inspection".

$$A_{dm} = -g_{m_{1,2}} R_{out} ; R_{out} = r_{ds_1} \parallel R_L \quad (\text{with } v_s = \text{gnd})$$

$$A_{cm} = \frac{-g_{m_{1,2}} r_{ds_1} \cdot R_L}{R_L + r_{ds_1} + 2R_b + g_{m_{1,2}} r_{ds_1} (2R_b)} \quad (\text{w/ open circuit at } v_s \text{ axis})$$

• Ideally:  $A_{dm} \rightarrow \infty$  (high DM gain)

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$A_{cm} \rightarrow 0$  (reject all CM noise)

• Figure of merit is how well ~~DM~~ DM is amplified over CM  $\Rightarrow$  "Common-Mode Rejection Ratio" = CMRR.

$$\text{CMRR} = \frac{A_{dm}}{A_{cm}} \rightarrow \infty \text{ ideally.}$$

• From Pg 5, for circuit of Fig. on Pg. 1,

$$\underline{\text{CMRR}} = \frac{R_L + r_{ds1} + 2R_b + g_{m1,2} r_{ds1,2} (2R_b)}{R_L + r_{ds1}}$$

$\Rightarrow$  Dominated by  $g_m r_{ds} (2R_b)$  term

$\Rightarrow$  need good bias  $I_b$  for good CMRR!

note:  $R_b = r_{ds3}$  for case of pg1.

• Next: How to achieve large  $A_{dm}$ ?  $\Rightarrow$  large  $R_L$ .

$\Rightarrow$  active loading (same as CS amp before)