Chapter 10

AMPLIFIER DESIGN EXAMPLE

10.1 Introduction

Just like any analog building block, designing an amplifier with high performance is quite an art! Since such a multi-dimensional problem typically involves so many conflicting specifications, it is impossible to develop a standard procedure.

First of all, there exist so many different circuit configurations to choose from. Depending on the specifications, one may be more suitable than others. Even after a particular configuration has been selected, there are still problems with choosing right parameters to meet and/or to optimize given specifications. Many times, some "reasonable" assumptions need to be made and to be verified later. In case a specification is not met or some assumption is found invalid, an iteration of the whole design cycle may be required.

Nevertheless, some guidelines can be developed to help with the design. This chapter attempts to describe these guidelines through a specific example. After choosing a particular circuit configuration and giving it some justification, we will consider in details how a CMOS amplifier can be designed to meet certain specifications.

10.2 Circuit Configuration

For the purpose of illustration, let us assume that the typical two-stage CMOS amplifier shown in Fig. 10.1 is chosen as a good compromise among all requirement of gain, power consumption, and low supply voltage.

Non-cascode configuration is used to enable an operation at low supply voltages. A cascade is used to achieve a high overall gain. PMOS transistors are used as the input devices to minimize the noise and the offset voltage. Finally, a compensation capacitor is necessary to stabilize the circuit with some given phase margin.

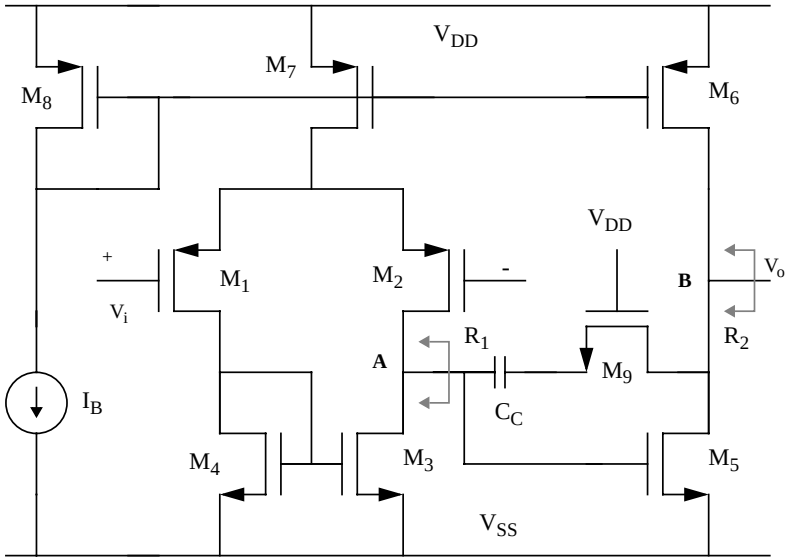

Fig. 10.1 Schematic of a CMOS amplifier to be designed

10.3 Design Equations

After the circuit configuration is determined, it is important to investigate and derive, if necessary, its design equations. Here, the design equations are summarized as follows.

The low-frequency gain can be easily obtained to be

$$|A_0| = (g_{m_1}R_1)(g_{m_5}R_2) \tag{10.1}$$

The two dominant poles are given by

$$|p_1| = \frac{1}{(1 + g_{m_5} \times R_2)C_C R_1} \tag{10.2}$$

$$|p_2| = \frac{g_{m_5}C_C}{C_A C_B + C_A C_C + C_C C_B} \approx \frac{g_{m_5}}{C_A + C_B} \tag{10.3}$$

where C_A and C_B are the total capacitance seen at nodes A and B, respectively.

The unity-gain frequency can be derived to be

$$\omega_o = \frac{g_{m_1}}{C_C} \tag{10.4}$$

With respect to the phase margin, the second pole and the unity-gain frequency are related as

$$|p_2| = \begin{cases} \omega_o & \text{for} \quad PM = 45° \\ 2\omega_o & \text{for} \quad PM = 60° \end{cases} \tag{10.5}$$

The right-half plane introduced by the compensation capacitor can be eliminated if the equivalent resistance of M9 is chosen to be

$$R_{M_9} = \frac{1}{g_{m_5}} \tag{10.6}$$

The slew rate can be calculated as

$$SR = \frac{I_B}{C_C} = \frac{I_B}{g_{m_1}}\omega_o \tag{10.7}$$

To minimize the systematic offset voltage, it is necessary that

$$V_{gs_3} = V_{gs_4} = V_{ds_4} = V_{gs_5} \tag{10.8}$$

and

$$V_{gs_6} = V_{gs_7} \tag{10.9}$$

As a result,

$$\frac{(W/L)_3}{(W/L)_5} = \frac{(W/L)_4}{(W/L)_5} = \frac{I_B/2}{I_{D_5}} \tag{10.10}$$

and

$$\frac{(W/L)_6}{(W/L)_7} = \frac{I_{D_6}}{I_{D_7}} = \frac{I_{D_5}}{I_{D_7}} = \frac{1}{2}\frac{(W/L)_5}{(W/L)_3} \tag{10.11}$$

If the devices are perfectly matched, due to the current mirror as an active load, the common-mode rejection ratio is infinitely large,

$$CMRR = \frac{A_{dm}}{A_{cm}} \approx \infty \tag{10.12}$$

In case not enough information is given, the following useful rules of thumb can be used:

i) The second stage is biased at higher current than the input stage, i.e. $g_{m5} > g_{m1}$.

ii) The compensation capacitor and the load capacitor are equal, i.e. $C_C = C_L$.

iii) The transconductance is maximized by biasing the input devices such that

$$V_{DS_{sat}} = V_{GS} - V_T = 0.2V \tag{10.13}$$

Note: Typically, the load capacitance must be specified. The compensation capacitor can then be calculated depending on the given specifications.

1. Power Constraint: If the power constraint is given, the bias current can be determined. Combined with the slew rate, the compensation capacitor can be estimated.

2. Noise Constraint: If the noise constraint is given, the transconductance of the input devices can be determined. Combined with the desired unity-gain bandwidth and phase margin, the compensation capacitor can be estimated.

10.4 Design Procedure

As an illustration, let us design the amplifier to meet the following specifications.

Parameters	Specifications
Low-frequency gain A_0	≥ 90 dB
Unity-gain frequency f_0	≥ 10 MHz
Slew rate SR	≥ 5 V/μs
Phase margin PM	≥ 60^o
CMRR	≥ 50 dB
Load Capacitor C_L	10 pF

From Eq. 10.5, to meet the minimum requirement of the phase margin, we should have

$$|p_2| = 2\omega_o \qquad \text{for} \qquad PM = 60° \tag{10.14}$$

Combining with Eqs. 10.3-10.4 to get

$$\frac{g_{m_5}}{C_A + C_B} \approx \frac{g_{m_5}}{C_L} = 2\frac{g_{m_1}}{C_C} = 2\omega_o \tag{10.15}$$

Since no power constraint is provided, as a rule of thumb, we can assume that

$$C_C = C_L = 10pF \tag{10.16}$$

As a result, the transconductances are given by

$$g_{m_5} = 2\omega_o \times C_L = 2 \times 2\pi \times 10M \times 10p = 1.26mA/V \tag{10.17}$$

$$g_{m_1} = \omega_o \times C_C = 2\pi \times 10M \times 10p = 0.63mA/V \tag{10.18}$$

From the slew-rate specification, we can obtain

$$I_B = SR \times C_C = 10V/\mu \times 10pF = 100\mu A \tag{10.19}$$

With the information obtained, the rest, including the gain and the CMRR, are well defined. Before the transistors' aspect ratios W/L's are determined, it is important to verify whether these specifications are met.

From Eq. 10.1 and 10.12, the overall gain and the common-mode rejection ratio are given by

$$|A_0| = (g_{m_1}R_1)(g_{m_5}R_2) = 0.63m \times \frac{1}{2 \times 0.02 \times 50\mu} \times 1.26m \times \frac{1}{2 \times 0.02 \times 100\mu} = 100dB \tag{10.20}$$

$$CMRR \approx \infty \tag{10.21}$$

where the channel length modulation factors for both PMOS and NMOS are assumed to be 0.02 V^{-1}.

Note: If, for some reason, one of these specifications were not met, all the design steps would have needed to be repeated with different assumptions. For example, if a higher CMRR were desired, the input transconductance could have been increased or a cascode bias current could have been used.

Here, since all the specifications have been met, we can go ahead with calculating the W/L's aspect ratios as follows.

From Eqs. 10.18-10.19,

$$\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2 = \frac{g_{m_1}^2}{I_B \times \mu_p C_{ox}} = \frac{0.63m^2}{100\mu \times 20\mu} = 315 \tag{10.22}$$

It follows that

$$\left(\frac{W}{L}\right)_3 = \left(\frac{W}{L}\right)_4 = \left(\frac{W}{L}\right)_2 \times \frac{\mu_p C_{ox}}{\mu_n C_{ox}} = 315 \times \frac{20\mu}{50\mu} = 126 \tag{10.23}$$

where it is assumed that $\mu_n C_{ox} = 50\ \mu A/V^2$ and $\mu_p C_{ox} = 20\ \mu A/V^2$.

From Eqs. 10.10, 10.11, and 10.15,

$$I_{D_5} = I_{D_6} = 2I_{D_1} = I_B = 100\mu A \tag{10.24}$$

$$\left(\frac{W}{L}\right)_5 = 2\left(\frac{W}{L}\right)_3 = 252 \tag{10.25}$$

$$\left(\frac{W}{L}\right)_6 = \left(\frac{W}{L}\right)_7 = \left(\frac{W}{L}\right)_8 = 2\left(\frac{W}{L}\right)_2 = 630 \tag{10.26}$$

Finally, the aspect ratio of M_9 can be calculated using Eq. 10.6 to be, assuming that V_{DD} = 3V, V_T = 1V, and V_o = 0V,

$$\left(\frac{W}{L}\right)_9 = \frac{1}{\mu_n C_{ox}(V_{GS_9} - V_T)R_{M_9}} = \frac{g_{m_5}}{\mu_n C_{ox}(V_{GS_9} - V_T)} = \frac{1.26m}{50\mu \times 2} = 12.6 \tag{10.27}$$

10.5 References

1. Gray & Meyer, "MOS Op Amp Design - A Tutorial Review," *IEEE JSSC*, pp. 969-982, Dec. 1982.

2. Mallya and Nevin, "Design Procedure of Fully Differential Folded Cascode CMOS Op Amp," *IEEE JSSC*, pp. 1737-1740, Dec. 1989