CMOS COMPARATOR

1. Comparator Design Specifications

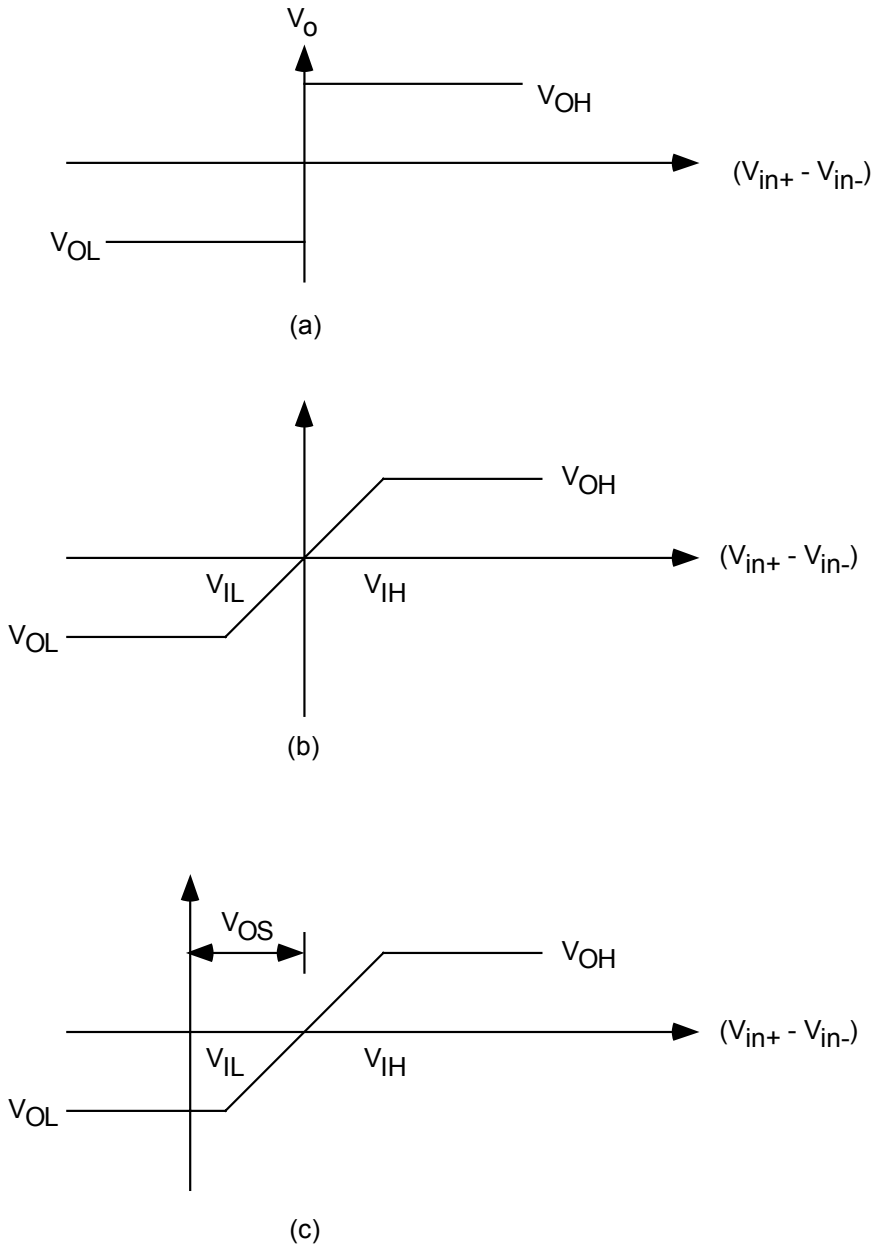


Figure 1. Comparator Transfer Characteristics.

A comparator is a circuit that has binary output. Ideally its output shown in Figure 1(a) is defined as follows:

$$V_O = \begin{cases} V_{OH} & \text{if } V_{in+} - V_{in-} > 0 \\ V_{OL} & \text{if } V_{in+} - V_{in-} < 0 \end{cases}$$

This is not realizable because its gain is infinity. Figure 1(b) shows a realizable first order transfer characteristic of a comparator. Its output is defined as follows:

$$V_O = \begin{cases} V_{OH} & \text{if } (V_{in+} - V_{in-}) > V_{IH} \\ A_V(V_{in+} - V_{in-}) & \text{if } V_{IL} < (V_{in+} - V_{in-}) < V_{IH} \\ V_{OL} & \text{if } (V_{in+} - V_{in-}) < V_{IL} \end{cases}$$

Another nonideal characteristic of practical comparator is the present of input offset. That is the output does not change until the input difference reached the input offset Vos. Figure 1(c) shows this transfer characteristic. Its output is defined as follows:

$$V_O = \begin{cases} V_{OH} & \text{if } (V_{in+} - V_{in-}) > V_{IH} \\ A_V(V_{in+} - V_{in-}) - A_V V_{OS} & \text{if } V_{IL} < (V_{in+} - V_{in-}) < V_{IH} \\ V_{OL} & \text{if } (V_{in+} - V_{in-}) < V_{IL} \end{cases}$$

The input offset can be minimized or ignored by proper layout.

If the input step is sufficiently small the output should not slew and the transient response will be a linear response. The settling time is the time needed for the output to reach a final value within a predetermined tolerance, when excited by a small signal. Small-signal settling time is determined by the gain bandwidth product of the amplifier, this will be shown in the opamp circuit section later. If the input step magnitude is sufficiently large, the comparator will slew by virtue of not having enough current to charge or discharge the compensating and/or load capacitances. The slew rate is determined from the slope of the output waveform during the rise or fall of the output. Slew rate is limited by the current-sourcing/sinking capability in charging the output capacitor.

Settling time is important in analog signal processing. It is necessary to wait until the amplifier has settled to within a few tenths of a percent of its final value in order to avoid errors in the accuracy of processing analog signals. A longer settling time implies that the rate of processing analog signals must be reduced.

In the following design, a 10mV signal must be resolved using the comparator in Figure 2 and 3. The power supply rails are VDD=5V and VSS=-5V. That is, the output will swing by 10V (from –5V to 5V) when the input signal swing by 10mV(from –5mV to 5mV). The comparator gain must be at least 10,000 (=10V/10mV). The following specifications will be used in designing the comparator in Pwell and Nwell processes.

VDD=5V, VSS=-5V, AV>10000 , -3<CMR<3, -4.5<Vo<4.5, SR=10V/us.

2. Designing the Comparator with NMOS Input Drivers

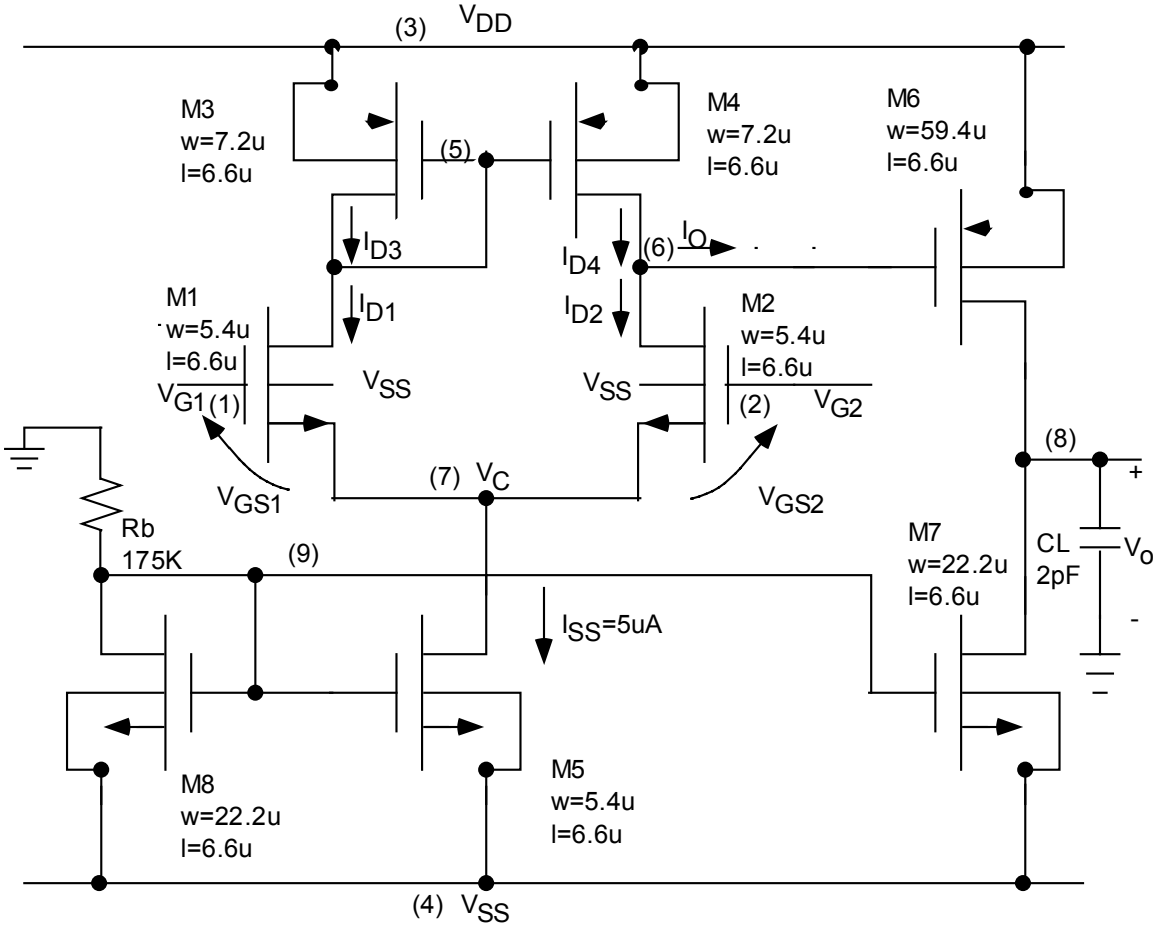


Figure 2. The CMOS Comparator Implementation with NMOS input drivers.

Figure 2 shows the comparator schematic diagram implemented with NMOS input drivers.

1. Determine the current drive requirement of M7 to satisfy the SR specification, if $C_L = 2\text{pF}$

$$I_{D7} = C_L\left(\frac{dV}{dt}\right) = C_L(SR) = (2E-12)(10E6) = 20\text{uA}$$

2. Determine the size of M6 and M7 to satisfy the output-voltage swing requirement.

$$V_{DS7(SAT)} = V_{O(min)} - V_{SS} = -4.5-(-5) = 0.5 = V_{GS7} - V_{N0} = \Delta V$$

$$V_{DS7(SAT)} = \sqrt{\frac{2I_{DS7}}{\beta_7}} = \sqrt{\frac{2I_{DS7}}{K_N(W/L)_7}}$$

$$(W/L)_7 = \frac{2I_{DS7}}{K_N(V_{DS7(SAT)})^2} = \frac{2(20E-6)}{(40E-6)(0.5)^2} = 4$$

Similarly,

$$V_{SD6(SAT)} = V_{DD} - V_{O(max)} = 5 - (4.5) = 0.5$$

$$(W/L)_6 = \frac{2I_{SD6}}{K_P (V_{SD6(SAT)})^2} = \frac{2(20E-6)}{(15E-6)(0.5)^2} = 10.666$$

3. Calculate the gain of the second stage.

$$A_{V2} = -\left(\frac{g_{m6}}{g_{ds6} + g_{ds7}}\right) = -\frac{\sqrt{2K_P I_{SD6}(W/L)_6}}{I_{SD6}(\lambda_P + \lambda_N)} = -\frac{\sqrt{2(15E-6)(20E-6)(10.666)}}{(20E-6)(0.02+0.02)} = 100$$

4. Calculate the gain of the first stage to satisfy the overall gain.

$$A_V = A_{V1} A_{V2} \geq 10000$$
$$A_{V1} \geq 10000 / A_{V2} = 100$$

5. Determine the first stage biasing current using the minimum allowable size of (W/L)=1, and minimum output offset.

(a) Consider M4 and M6.

Using the minimum size for M4, determine the current I_{SD4} that mirror with M6. That is,

$$I_{SD4} = \frac{(W/L)_4}{(W/L)_6} I_{SD6} = \frac{1}{10.666}(20uA) = 1.875uA$$

(b) Consider M5 and M7.

Using the minimum size for M5, determine the current I_{DS5} that mirror with M7. That is,

$$I_{DS5} = \frac{(W/L)_5}{(W/L)_7} I_{DS7} = \frac{1}{4}(20uA) = 5uA$$
$$I_{SD4} = I_{DS5}/2 = 2.5uA = I_{SD3}$$
$$I_{DS2} = I_{DS1} = I_{DS5}/2 = 2.5uA$$

(c) Select the larger of the two I_{SD4} and adjust the size of M4

$$(W/L)_4 = \frac{I_{SD4}}{I_{SD6}}(W/L)_6 = \frac{2.5E-6}{20E-6}(10.666) = 1.333$$

6. Determine the size of M1 to satisfy the gain requirement.

$$A_{V1} = \frac{g_{m1}}{g_{ds2} + g_{ds4}} = \frac{\sqrt{2K_N I_{DS1}(W/L)_1}}{I_{DS1}(\lambda_N + \lambda_P)}$$

$$(W/L)_1 = \frac{[A_{V1} I_{DS1}(\lambda_N + \lambda_P)]^2}{2K_N I_{DS1}} = \frac{[(100)(2.5E-6)(0.02+0.02)]^2}{2(40E-6)(2.5E-6)} = 0.5$$

Let $(W/L)_1$ be the minimum size of 1. Then re-calculate the gain of the first stage.

$$A_{V1} = \frac{g_{m1}}{g_{ds2} + g_{ds4}} = \frac{\sqrt{2K_N I_{DS1}(W/L)_1}}{I_{DS1}(\lambda_N + \lambda_P)} = \frac{\sqrt{2(40E-6)(2.5E-6)(1)}}{(2.5E-6)(0.02+0.02)} = 141.42$$

$$A_V = A_{V1} A_{V2} = (141.42)(100) = 14142$$

7. The minimum size of M5 (=1) in step 5(b) can be adjusted to satisfy the negative input CMR of –3V.

$$V_{G1(min)} = V_{SS} + V_{DS5(SAT)} + \sqrt{\frac{2I_{DS1}}{K_N(W/L)_1}} + V_{T1}$$

$$V_{DS5(SAT)} = V_{G1(min)} - V_{SS} - \sqrt{\frac{2I_{DS1}}{K_N(W/L)_1}} - V_{T1}$$

$$= -3 - (-5) - \sqrt{\frac{2(2.5E-6)}{(40E-6)(1)}} - 1 = 0.65$$

$$V_{DS5(SAT)} = \sqrt{\frac{2I_{DS5}}{K_N(W/L)_5}}$$

$$(W/L)_5 = \frac{2I_{DS5}}{K_N(V_{DS5(SAT)})^2} = \frac{2(5E-6)}{(40E-6)(0.65)^2} = 0.59$$

Select the larger of the two, $(W/L)_5$=1. No adjustment needed, since this is the value used earlier in the calculation.

8. The minimum size of M3(=1) in step 5(a) can be adjusted to meet the positive input CMR of 3V.

$$V_{G1(max)} = V_{DD} - \sqrt{\frac{2I_{SD3}}{K_P(W/L)_3}} - |V_{T3}| + V_{T1}$$

$$(W/L)_3 = \frac{2I_{SD3}}{K_P(V_{DD} - V_{G1(max)} - |V_{T3}| + V_{T1})^2} = \frac{2(2.5E-6)}{(15E-6)(5-3-|-1|+1)^2} = \frac{1}{12}$$

Select the larger of the two, $(W/L)_3$=1. No further adjustment needed.

9. Determine the size of M8 to provide as the main current mirror for the comparator.

For V_{DS5}=0.5V and V_{DS7}=0.5V, this voltage corresponds to the value of V_{G8}=-3.5V or V_{GS8}=1.5V. Let I_{SD8}=20uA.

$$(W/L)_8 = \frac{2I_{DS8}}{K_N(V_{GS8} - V_{TN})^2} = \frac{2(20E-6)}{(40E-6)(1.5-1)^2} = 4$$

The external resistor Rb connected between V_{G8} and ground must be chosen to provide the required current for M8 of 20uA.

$$R_b = \frac{0 - V_{G8}}{I_{DS8}} = \frac{0-(-3.5)}{20E-6} = 175K$$

10. Select the width of each transistor.

PAR	M1	M2	M3	M4	M5	M6	M7	M8
I(uA)	2.5	2.5	2.5	2.5	5	20	20	20
T	N	N	P	P	N	P	N	N
W/L	1	1	1.333	1.333	1	10.666	4	4
W(u)	5.6	5.6	7.46	7.46	5.6	59.73	22.4	22.4
L(u)	6.6	6.6	6.6	6.6	6.6	6.6	6.6	6.6
Leff(u)	5.6	5.6	5.6	5.6	5.6	5.6	5.6	5.6

Finding the W, L to the nearest multiple of λ=0.6.

PAR	M1	M2	M3	M4	M5	M6	M7	M8
I(uA)	2.5	2.5	2.5	2.5	5	20	20	20
T	N	N	P	P	N	P	N	N
W/L	1	1	1.333	1.333	1	10.666	4	4
W(u)	5.4	5.4	7.2	7.2*	5.4*	59.4*	22.2*	22.2
L(u)	6.6	6.6	6.6	6.6	6.6	6.6	6.6	6.6
Leff(u)	5.6	5.6	5.6	5.6	5.6	5.6	5.6	5.6

*Adjusted to satisfy the balance condition to minimize the input offset voltage, Vos:

$$\frac{(W/L)_6}{(W/L)_4} = 2\frac{(W/L)_7}{(W/L)_5}$$

$$\frac{59.4}{7.2} = 2\frac{22.2}{5.4}$$

$$8.25 \approx 8.22$$

3. Designing the Comparator with PMOS Input Drivers

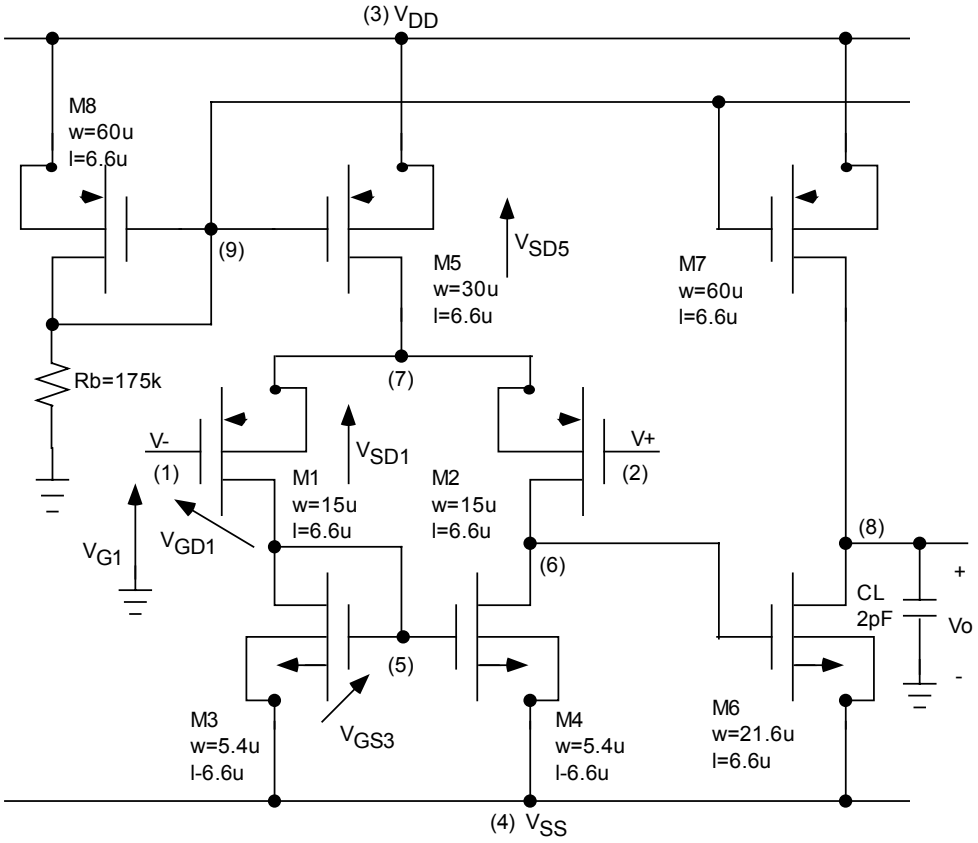


Figure 3. CMOS Comparator Implementation with PMOS input drivers.

Figure 3 shows the comparator schematic diagram implemented with PMOS input dricers.

1. Determine the current drive requirement of M7 to satisfy the SR specification, if $C_L = 2pF$

$$I_{D7} = C_L\left(\frac{dV}{dt}\right) = C_L(SR) = (2E-12)(10E6) = 20uA$$

2. Determine the size of M6 and M7 to satisfy the output-voltage swing requirement.

$$V_{SD7(SAT)} = V_{DD} - V_{O(max)} = 5 - 4.5 = 0.5$$

$$V_{SD7(SAT)} = \sqrt{\frac{2I_{SD7}}{\beta_7}} = \sqrt{\frac{2I_{SD7}}{K_P(W/L)_7}}$$

$$(W/L)_7 = \frac{2I_{DS7}}{K_P(V_{DS7(SAT)})^2} = \frac{2(20E-6)}{(15E-6)(0.5)^2} = 10.666$$

Similarly,

$$V_{DS6(SAT)} = V_{O(min)} - V_{SS} = -4.5 - (-5) = 0.5$$

$$(W/L)_6 = \frac{2I_{DS6}}{K_N (V_{DS6(SAT)})^2} = \frac{2(20E-6)}{(40E-6)(0.5)^2} = 4$$

3. Calculate the gain of the second stage.

$$A_{V2} = -\left(\frac{g_{m6}}{g_{ds6} + g_{ds7}}\right) = -\frac{\sqrt{2K_N I_{DS6}(W/L)_6}}{I_{DS6}(\lambda_N + \lambda_P)} = -\frac{\sqrt{2(40E-6)(20E-6)(4)}}{(20E-6)(0.02+0.02)} = 100$$

4. Calculate the gain of the first stage to satisfy the overall gain.

$$A_V = A_{V1} A_{V2} \geq 10000$$
$$A_{V1} \geq 10000 / A_{V2} = 100$$

5. Determine the first stage biasing current using the minimum allowable size of 1, and minimum output offset.

(a) Consider M4 and M6.

Using the minimum size for M4, determine the current I_{SD4} that mirror with M6. That is,

$$I_{DS4} = \frac{(W/L)_4}{(W/L)_6} I_{DS6} = \frac{1}{4}(20uA) = 5uA$$
$$I_{SD5} = 2I_{DS4} = 2(5uA) = 10uA$$

(b) Consider M5 and M7.

Using the minimum size for M5, determine the current I_{DS5} that mirror with M7. That is,

$$I_{SD5} = \frac{(W/L)_5}{(W/L)_7} I_{SD7} = \frac{1}{10.666}(20uA) = 1.875uA$$
$$I_{DS4} = I_{SD5}/2 = 1.875/2 = 0.937uA = I_{DS3}$$
$$I_{SD2} = I_{SD1} = I_{SD5}/2 = 1.875/2 = 0.937uA$$

(c) Select the larger of the two I_{SD4} and adjust the size of M4 if necessary.

The larger I_{SD4} = 5uA from 5(a). No adjustment needed, since this is the value use in calculation.

6. Determine the size of M1 to satisfy the gain requirement.

$$A_{V1} = \frac{g_{m1}}{g_{ds2} + g_{ds4}} = \frac{\sqrt{2K_P I_{SD1}(W/L)_1}}{I_{SD1}(\lambda_N + \lambda_P)}$$

$$(W/L)_1 = \frac{[A_{V1} I_{SD1}(\lambda_N + \lambda_P)]^2}{2K_P I_{SD1}} = \frac{[(100)(5E-6)(0.02+0.02)]^2}{2(15E-6)(5E-6)} = 2.666$$

7. The minimum size of M5 (=1) in step 5(b) can be adjusted to satisfy the positive input CMR of 3V.

$$V_{G1(max)} = V_{DD} - V_{SD5(SAT)} - V_{SG1}$$

$$V_{G1(max)} = V_{DD} - V_{SD5(SAT)} - \sqrt{\frac{2I_{SD1}}{K_P(W/L)_1}} - |V_{T1}|$$

$$V_{SD5(SAT)} = V_{DD} - V_{G1(max)} - \sqrt{\frac{2I_{SD1}}{K_P(W/L)_1}} - |V_{T1}|$$

$$= 5 - 3 - \sqrt{\frac{2(5E-6)}{(15E-6)(2.666)}} - 1 = 0.5$$

$$V_{SD5(SAT)} = \sqrt{\frac{2I_{SD5}}{K_P(W/L)_5}}$$

$$(W/L)_5 = \frac{2I_{SD5}}{K_P(V_{DS5(SAT)})^2} = \frac{2(10E-6)}{(15E-6)(0.5)^2} = 5.333$$

Select the larger of the two, $(W/L)_5$=5.333 and adjust the size of M7 for proper mirroring with M5.

$$(W/L)_7 = \frac{I_7}{I_5}(W/L)_5 = \frac{20}{10}(5.333) = 10.666$$

8. The minimum size of M3 or M4(=1) in step 5(a) can be adjusted to meet the negative input CMR of -3V.

$$V_{G1(min)} = V_{SS} + \sqrt{\frac{2I_{DS3}}{K_N(W/L)_3}} + V_{T3} - |V_{T1}|$$

$$(W/L)_3 = \frac{2I_{DS3}}{K_P(V_{G1(min)} - V_{SS} - V_{T3} + |V_{T1}|)^2} = \frac{2(5E-6)}{(40E-6)[-3-(-5)-1+|-1|]^2} = \frac{1}{16}$$

Select the larger of the two, $(W/L)_3$=1. No further adjustment needed.

9. Determine the size of M8 to provide as the main current mirror for the comparator.

For V_{SD5}=0.5V and V_{SD7}=0.5V, this voltage corresponds to the value of V_{G8}=3.5V or V_{SG8}=1.5V. Let I_{SD8}=20uA.

$$(W/L)_8 = \frac{2I_{SD8}}{K_P(V_{SG8} - V_{TP})^2} = \frac{2(20E-6)}{(15E-6)(5-3.5-1)^2} = 10.666$$

The external resistor Rb connected between V_{G8} and ground must be chosen to provide the required current for M8 of 20uA.

$$R_b = \frac{V_{G8} - 0}{I_{DS8}} = \frac{3.5 - 0}{20E-6} = 175K$$

10. Select the width of each transistor.

PAR	M1	M2	M3	M4	M5	M6	M7	M8
I(uA)	5	5	5	5	10	20	20	20
T	P	P	N	N	P	N	P	P
W/L	2.666	2.666	1	1	5.333	4	10.666	10.666
W(u)	14.93	14.93	5.6	5.6	29.86	22.4	59.73	59.73
L(u)	6.6	6.6	6.6	6.6	6.6	6.6	6.6	6.6
Leff(u)	5.6	5.6	5.6	5.6	5.6	5.6	5.6	5.6

Finding the W, L to the nearest multiple of λ=0.6.

PAR	M1	M2	M3	M4	M5	M6	M7	M8
I(uA)	5	5	5	5	10	20	20	20
T	P	P	N	N	P	N	P	P
W/L	2.666	2.666	1	1	5.333	4	10.666	10.666
W(u)	15	15	5.4	5.4	30	21.6	60	60
L(u)	6.6	6.6	6.6	6.6	6.6	6.6	6.6	6.6
Leff(u)	5.6	5.6	5.6	5.6	5.6	5.6	5.6	5.6

*Adjusted to satisfy the balance condition to minimize the input offset voltage, Vos:

$$\frac{(W/L)_6}{(W/L)_4} = 2\frac{(W/L)_7}{(W/L)_5}$$

$$\frac{W_6}{W_4} = 2\frac{W_7}{W_5}$$

$$\frac{21.6}{5.4} = 2\frac{60}{30}$$

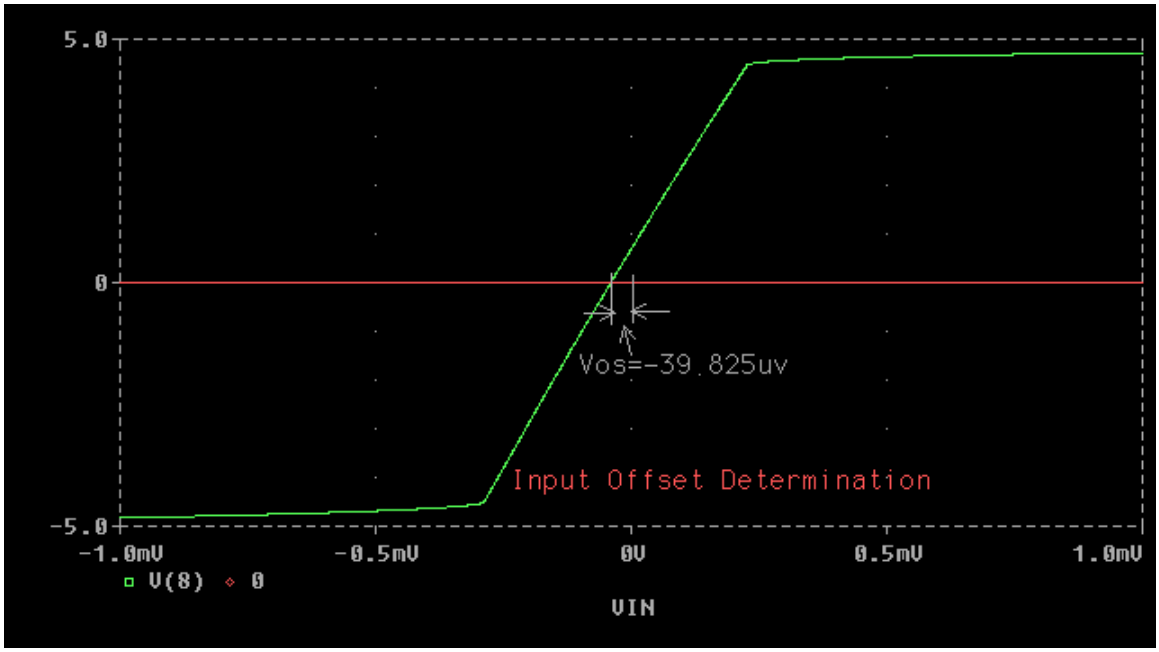
$$4 = 4$$

4. Comparator Simulation

4.1. CMOS Comparator Implementation with NMOS Input Drivers

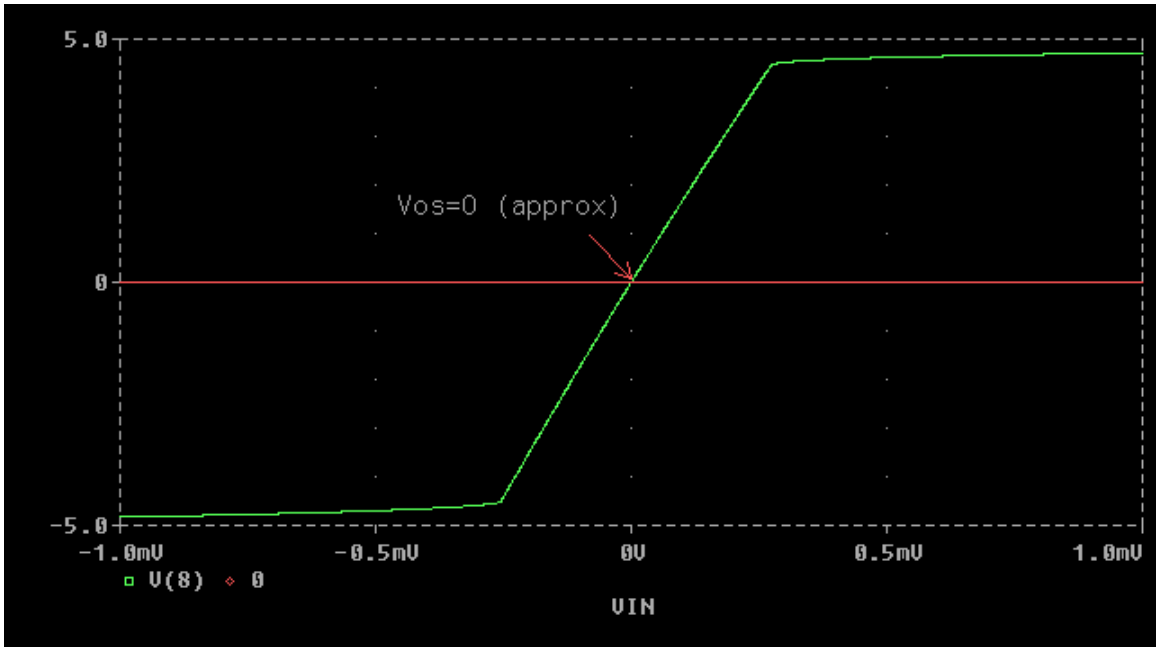
The PSpice netlist is given below:

```
* Filename="diffcmp.cir"
* MOS Diff Amp with NMOS Input Drivers and Current Mirror Load

* Input Signals
VIN 2 0 DC 0V
VOS 1 0 DC 0V

* Power Supplies
VDD 3 0 DC 5VOLT
VSS 4 0 DC -5VOLT

* Netlist for CMOS COMPARATOR in Pwell
M1  5  1 7 4    NMOS1  W=5.4U   L=6.6U
M2  6  2 7 4    NMOS1  W=5.4U   L=6.6U
M3  5  5 3 3    PMOS1  W=7.2U   L=6.6U
M4  6  5 3 3    PMOS1  W=7.2U   L=6.6U
M5  7  9 4 4    NMOS1  W=5.4U   L=6.6U
M6  8  6 3 3    PMOS1  W=59.4U  L=6.6U
M7  8  9 4 4    NMOS1  W=22.2U  L=6.6U
M8  9  9 4 4    NMOS1  W=22.2U  L=6.6U

* External Components
CL  8  0        2pF
RB 9 0          175K

* SPICE Parameters
.MODEL NMOS1 NMOS VTO=1 KP=40U
+ GAMMA=1.0 LAMBDA=0.02 PHI=0.6
+ TOX=0.05U LD=0.5U CJ=5E-4 CJSW=10E-10
+ U0=550 MJ=0.5 MJSW=0.5 CGSO=0.4E-9 CGDO=0.4E-9
.MODEL PMOS1 PMOS VTO=-1 KP=15U
+ GAMMA=0.6 LAMBDA=0.02 PHI=0.6
+ TOX=0.05U LD=0.5U CJ=5E-4 CJSW=10E-10
+ U0=200 MJ=0.5 MJSW=0.5 CGSO=0.4E-9 CGDO=0.4E-9

* Analysis
.DC VIN -1mv 1mV 1uV
.TF V(8) VIN
.PROBE
.END
```



To eliminate the input offset voltage, the negative of Vos is applied at the negative input of the comparator. That is, the PSpice entry for VOS is modified as follow:

```
VOS 1 0 DC 39.825uv
```



**** SMALL-SIGNAL CHARACTERISTICS

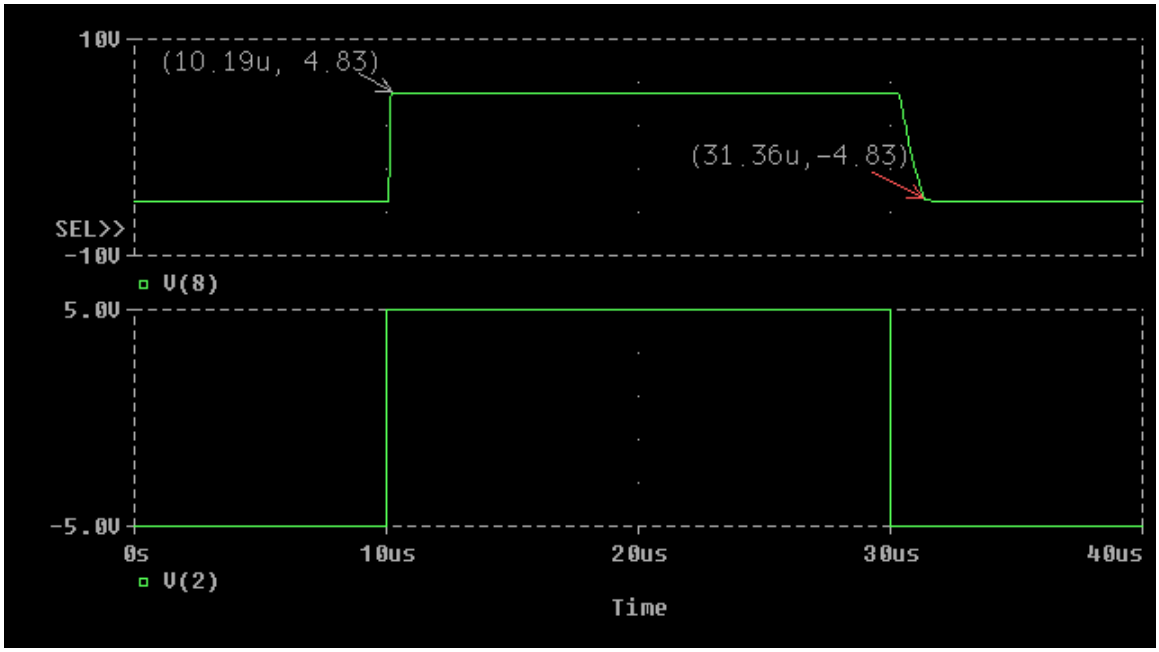
V(8)/VIN = 1.728E+04

INPUT RESISTANCE AT VIN = 1.000E+20

OUTPUT RESISTANCE AT V(8) = 1.269E+06

4.1.2 Comparator Transient Response Slew Rate Measurement

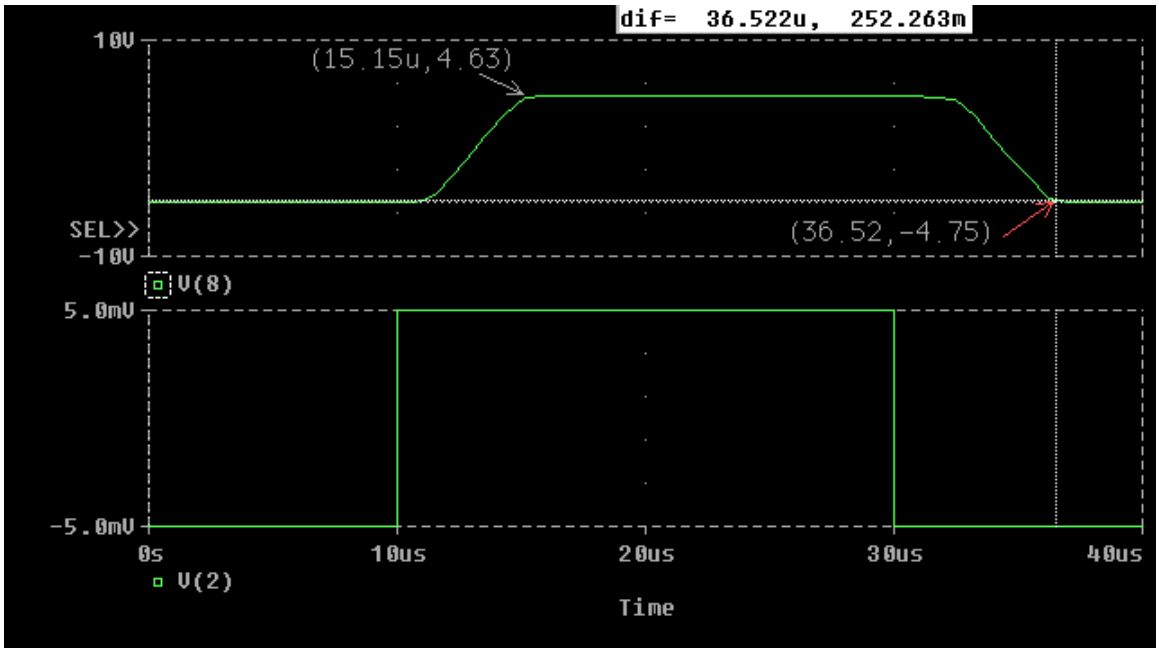
```
* Filename="diffcmp1.cir"
* MOS Diff Amp with NMOS Input and Current Mirror Load

* Input Signal
VIN 2 0 PWL(0,-5V 10us,-5V 10.01us,5V 30us, 5V 30.01us,-5V 1s, -5V)
VOS 1 0 DC -88.501uV

*Power Supplies
VDD 3 0 DC 5VOLT
VSS 4 0 DC -5VOLT

* Netlist for Slew Rate Measurement


* Netlist for CMOS COMPARATOR in Pwell
M1  5  1 7 4    NMOS1  W=5.4U   L=6.6U
M2  6  2 7 4    NMOS1  W=5.4U   L=6.6U
M3  5  5 3 3    PMOS1  W=7.2U   L=6.6U
M4  6  5 3 3    PMOS1  W=7.2U   L=6.6U
M5  7  9 4 4    NMOS1  W=5.4U   L=6.6U
M6  8  6 3 3    PMOS1  W=59.4U  L=6.6U
M7  8  9 4 4    NMOS1  W=22.2U  L=6.6U
M8  9  9 4 4    NMOS1  W=22.2U  L=6.6U

* External Components
CL  8  0        2pF
RB  9   0       175K


* SPICE Parameters
.MODEL NMOS1 NMOS VTO=1 KP=40U
+ GAMMA=1.0 LAMBDA=0.02 PHI=0.6
+ TOX=0.05U LD=0.5U CJ=5E-4 CJSW=10E-10
+ U0=550 MJ=0.5 MJSW=0.5 CGSO=0.4E-9 CGDO=0.4E-9
.MODEL PMOS1 PMOS VTO=-1 KP=15U
+ GAMMA=0.6 LAMBDA=0.02 PHI=0.6
+ TOX=0.05U LD=0.5U CJ=5E-4 CJSW=10E-10
+ U0=200 MJ=0.5 MJSW=0.5 CGSO=0.4E-9 CGDO=0.4E-9

*Analysis
.TRAN .1ns 40us
.PROBE
.END
```



4.1.3 Comparator Transient Response Settling Time Measurement

```
* Filename="diffcmp2.cir"
* MOS Diff Amp with NMOS Input and Current Mirror Load


* Input Signal
VIN 2 0 PWL(0,-5mV 10us,-5mV 10.01us,5mV 30us, 5mV 30.01us,-5mV 1s, -
5mV)
VOS 1 0 DC 0V

*Power Supplies
VDD 3 0 DC 5VOLT
VSS 4 0 DC -5VOLT

* Netlist for CMOS COMPARATOR in Pwell
M1  5  1 7 4    NMOS1  W=5.4U   L=6.6U
M2  6  2 7 4    NMOS1  W=5.4U   L=6.6U
M3  5  5 3 3    PMOS1  W=7.2U   L=6.6U
M4  6  5 3 3    PMOS1  W=7.2U   L=6.6U
M5  7  9 4 4    NMOS1  W=5.4U   L=6.6U
M6  8  6 3 3    PMOS1  W=59.4U  L=6.6U
M7  8  9 4 4    NMOS1  W=22.2U  L=6.6U
M8  9  9 4 4    NMOS1  W=22.2U  L=6.6U

* External Components
CL  8  0        2pF
RB  9   0       175K


* SPICE Parameters
.MODEL NMOS1 NMOS VTO=1 KP=40U
+ GAMMA=1.0 LAMBDA=0.02 PHI=0.6
+ TOX=0.05U LD=0.5U CJ=5E-4 CJSW=10E-10
+ U0=550 MJ=0.5 MJSW=0.5 CGSO=0.4E-9 CGDO=0.4E-9
.MODEL PMOS1 PMOS VTO=-1 KP=15U
```

```
+ GAMMA=0.6 LAMBDA=0.02 PHI=0.6
+ TOX=0.05U LD=0.5U CJ=5E-4 CJSW=10E-10
+ U0=200 MJ=0.5 MJSW=0.5 CGSO=0.4E-9 CGDO=0.4E-9

*Analysis
.TRAN .1ns 40us
.PROBE
.END
```

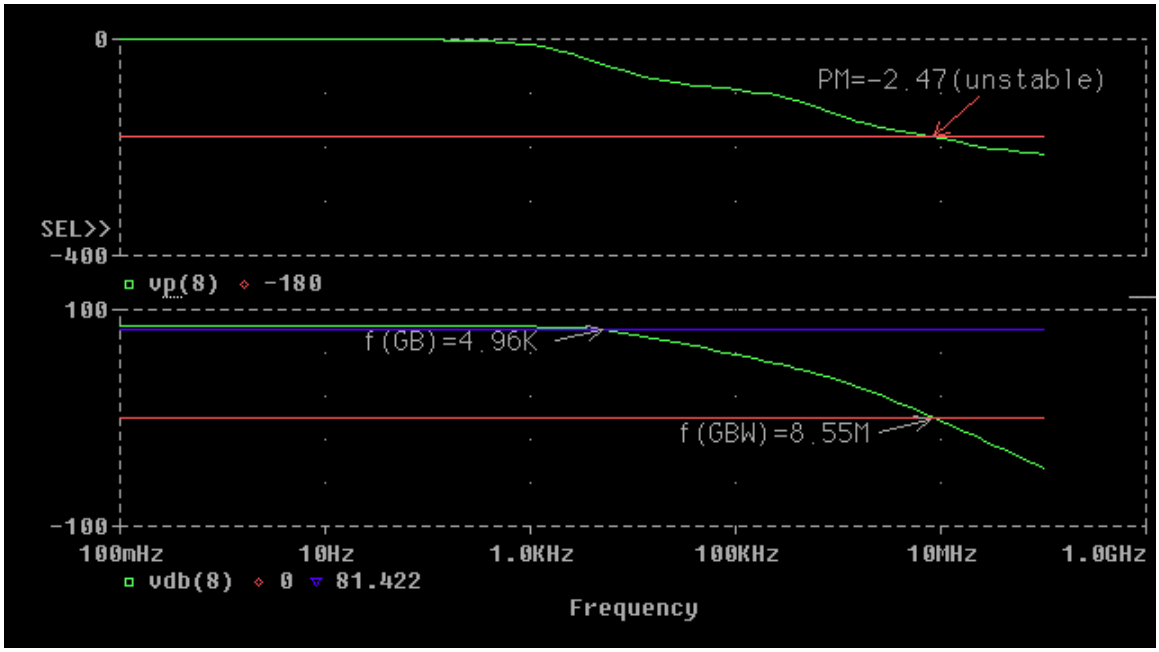


Upper output voltage for 5% settling time, 0.95(Vo(max))=0.95(4.85)=4.6
Lower output voltage for 5% settling time, 0.95(Vo(min))=0.95(-5)=4.75

4.1.4 Comparator Open-loop Transfer Function

```
* Filename="diffcmp4.cir"
* MOS Diff Amp with NMOS Input and Current Mirror Load

* Input Signal
VIN 2 0 AC 1V

*Power Supplies
VDD 3 0 DC 5VOLT
VSS 4 0 DC -5VOLT

* Netlist for CMOS COMPARATOR in Pwell
M1   5   0 7 7    NMOS1  W=5.4U   L=6.6U
M2   6   2 7 7    NMOS1  W=5.4U   L=6.6U
M3   5   5 3 3    PMOS1  W=7.2U   L=6.6U
M4   6   5 3 3    PMOS1  W=7.2U   L=6.6U
M5   7   9 4 4    NMOS1  W=5.4U   L=6.6U
M6   8   6 3 3    PMOS1  W=59.4U  L=6.6U
M7   8   9 4 4    NMOS1  W=22.2U  L=6.6U
```

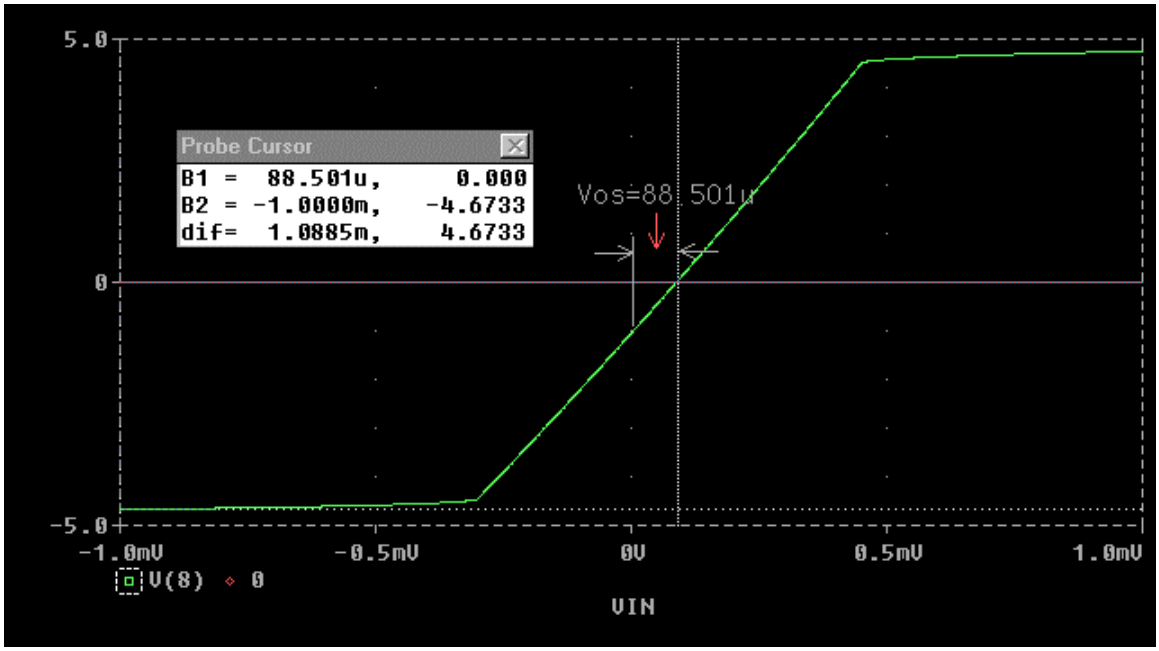
```
M8   9   9 4 4    NMOS1   W=22.2U   L=6.6U

* External Components
CL   8   0         2pF
RB   9   0         175K


* SPICE Parameters
.MODEL NMOS1 NMOS VTO=1 KP=40U
+ GAMMA=1.0 LAMBDA=0.02 PHI=0.6
+ TOX=0.05U LD=0.5U CJ=5E-4 CJSW=10E-10
+ U0=550 MJ=0.5 MJSW=0.5 CGSO=0.4E-9 CGDO=0.4E-9
.MODEL PMOS1 PMOS VTO=-1 KP=15U
+ GAMMA=0.6 LAMBDA=0.02 PHI=0.6
+ TOX=0.05U LD=0.5U CJ=5E-4 CJSW=10E-10
+ U0=200 MJ=0.5 MJSW=0.5 CGSO=0.4E-9 CGDO=0.4E-9

*Analysis
.AC DEC 10 0.1HZ 100MegHZ
.PROBE
.END
```



4.2. CMOS Comparator Implementation with PMOS Input Drivers

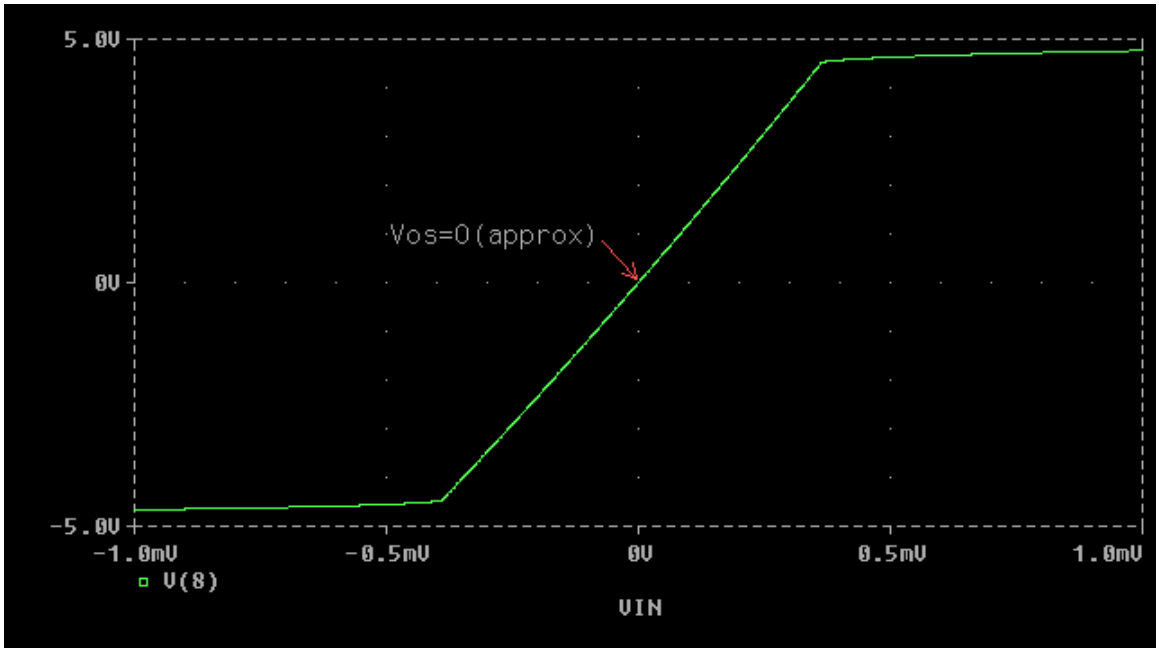
```
* Filename="diffcmpp.cir"
* CMOS Comparator with PMOS Input Drivers

* Input Signals
VIN 2 0 DC 0V
VOS 1 0 DC 0V

* Power Supplies
VDD 3 0 DC 5VOLT
VSS 4 0 DC -5VOLT

* Netlist for CMOS Comparator in Nwell
M1   5   1 7 7    PMOS1   W=15U    L=6.6U
```

```
M2   6   2 7 7     PMOS1   W=15U     L=6.6U
M3   5   5 4 4     NMOS1   W=5.4U    L=6.6U
M4   6   5 4 4     NMOS1   W=5.4U    L=6.6U
M5   7   9 3 3     PMOS1   W=30U     L=6.6U
M6   8   6 4 4     NMOS1   W=21.6U   L=6.6U
M7   8   9 3 3     PMOS1   W=60U     L=6.6U
M8   9   9 3 3     PMOS1   W=60U     L=6.6U

* External Components
CL   8   0         2pF
RB 9 0           175K

* SPICE Parameters
.MODEL NMOS1 NMOS VTO=1 KP=40U
+ GAMMA=1.0 LAMBDA=0.02 PHI=0.6
+ TOX=0.05U LD=0.5U CJ=5E-4 CJSW=10E-10
+ U0=550 MJ=0.5 MJSW=0.5 CGSO=0.4E-9 CGDO=0.4E-9
.MODEL PMOS1 PMOS VTO=-1 KP=15U
+ GAMMA=0.6 LAMBDA=0.02 PHI=0.6
+ TOX=0.05U LD=0.5U CJ=5E-4 CJSW=10E-10
+ U0=200 MJ=0.5 MJSW=0.5 CGSO=0.4E-9 CGDO=0.4E-9

* Analysis
.DC VIN -1mv 1mV 1uV
.TF V(8) VIN
.PROBE
.END
```



To eliminate the input offset voltage the negative of Vos is applied V- input.

VOS 1 0 DC –88.501uV



**** SMALL-SIGNAL CHARACTERISTICS

V(8)/VIN = 1.196E+04

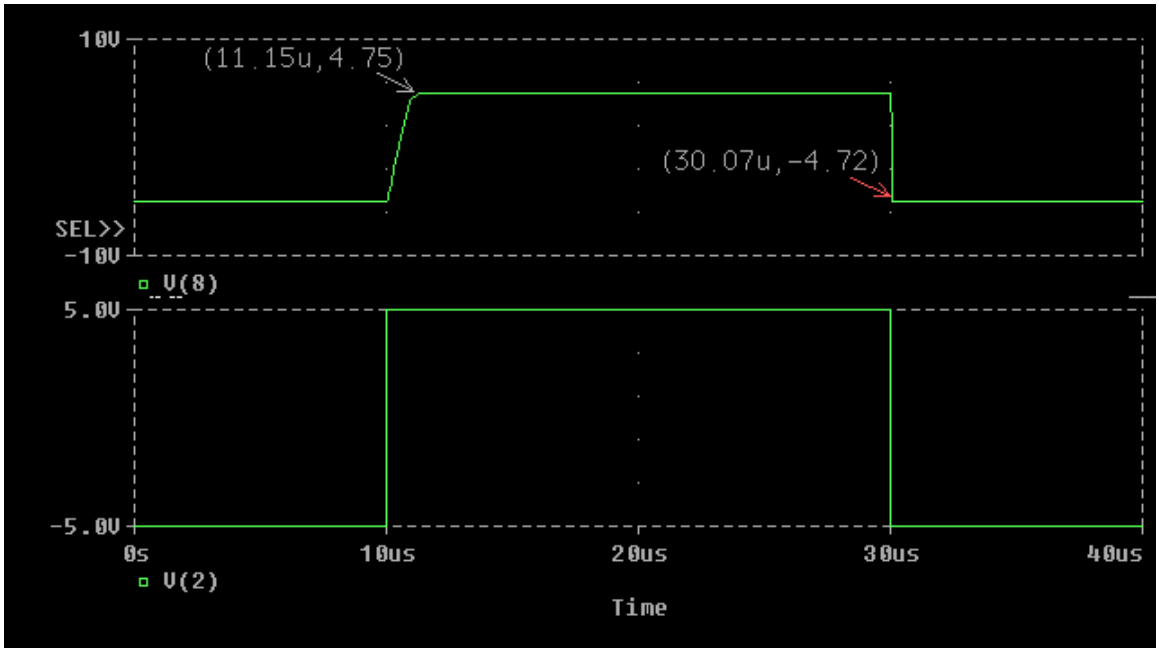
INPUT RESISTANCE AT VIN = 1.000E+20

OUTPUT RESISTANCE AT V(8) = 1.284E+06

4.2.1 Comparator Transient Response for Slew Rate Measuremnt

```
* Filename="diffcmpp1.cir"
* MOS Diff Amp with PMOS Input and Current Mirror Load

* Input Signal
VIN 2 0 PWL(0,-5V 10us,-5V 10.01us,5V 30us, 5V 30.01us,-5V 1s, -5V)
VOS 1 0 DC 0V

*Power Supplies
VDD 3 0 DC 5VOLT
VSS 4 0 DC -5VOLT

* Netlist for CMOS Comparator in Nwell
M1  5  1 7 7    PMOS1  W=15U    L=6.6U
M2  6  2 7 7    PMOS1  W=15U    L=6.6U
M3  5  5 4 4    NMOS1  W=5.4U   L=6.6U
M4  6  5 4 4    NMOS1  W=5.4U   L=6.6U
M5  7  9 3 3    PMOS1  W=30U    L=6.6U
M6  8  6 4 4    NMOS1  W=21.6U  L=6.6U
M7  8  9 3 3    PMOS1  W=60U    L=6.6U
M8  9  9 3 3    PMOS1  W=60U    L=6.6U

* External Components
CL  8  0        2pF
RB  9  0        175K
```

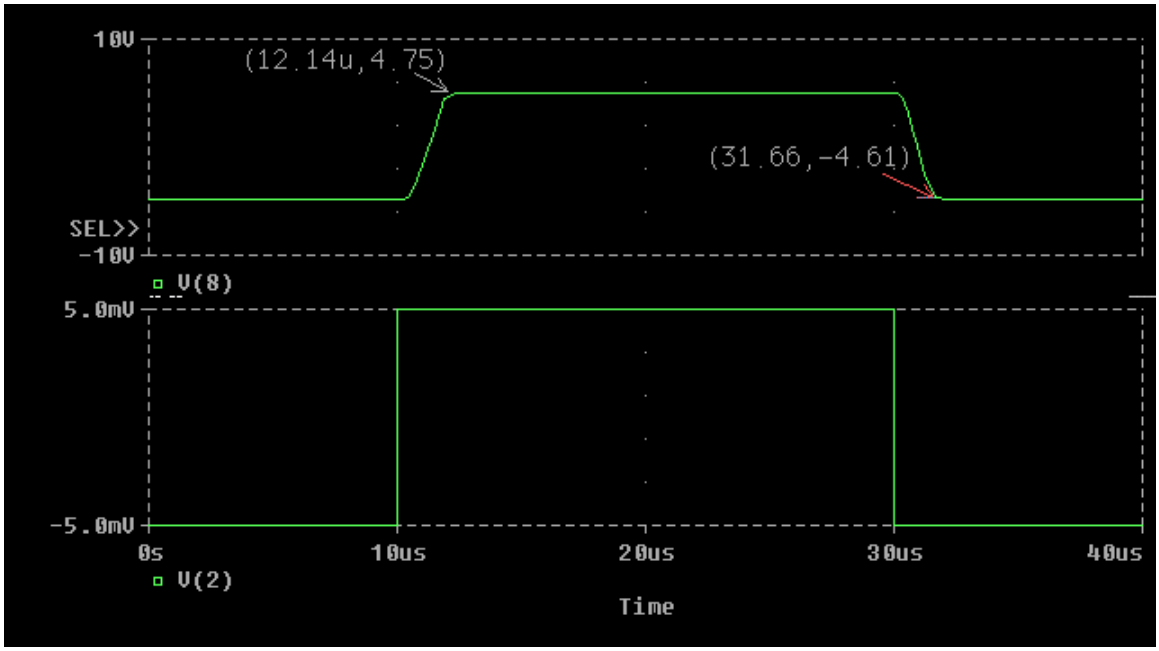
```
* SPICE Parameters
.MODEL NMOS1 NMOS VTO=1 KP=40U
+ GAMMA=1.0 LAMBDA=0.02 PHI=0.6
+ TOX=0.05U LD=0.5U CJ=5E-4 CJSW=10E-10
+ U0=550 MJ=0.5 MJSW=0.5 CGSO=0.4E-9 CGDO=0.4E-9
.MODEL PMOS1 PMOS VTO=-1 KP=15U
+ GAMMA=0.6 LAMBDA=0.02 PHI=0.6
+ TOX=0.05U LD=0.5U CJ=5E-4 CJSW=10E-10
+ U0=200 MJ=0.5 MJSW=0.5 CGSO=0.4E-9 CGDO=0.4E-9

*Analysis
.TRAN .1ns 40us
.PROBE
.END
```



4.2.2 Comparator Transient Response for Settling Time Measurement

```
* Filename="diffcmpp2.cir"
* MOS Diff Amp with PMOS Input and Current Mirror Load

* Input Signal
VIN 2 0 PWL(0,-5mV 10us,-5mV 10.01us,5mV 30us, 5mV 30.01us,-5mV 1s, -
5mV)
VOS 1 0 DC 0V

*Power Supplies
VDD 3 0 DC 5VOLT
VSS 4 0 DC -5VOLT

* Netlist for Slew Rate Measurement
* Netlist for CMOS Comparator in Nwell
M1   5   1 7 7    PMOS1  W=15U    L=6.6U
M2   6   2 7 7    PMOS1  W=15U    L=6.6U
M3   5   5 4 4    NMOS1  W=5.4U   L=6.6U
M4   6   5 4 4    NMOS1  W=5.4U   L=6.6U
M5   7   9 3 3    PMOS1  W=30U    L=6.6U
M6   8   6 4 4    NMOS1  W=21.6U  L=6.6U
```

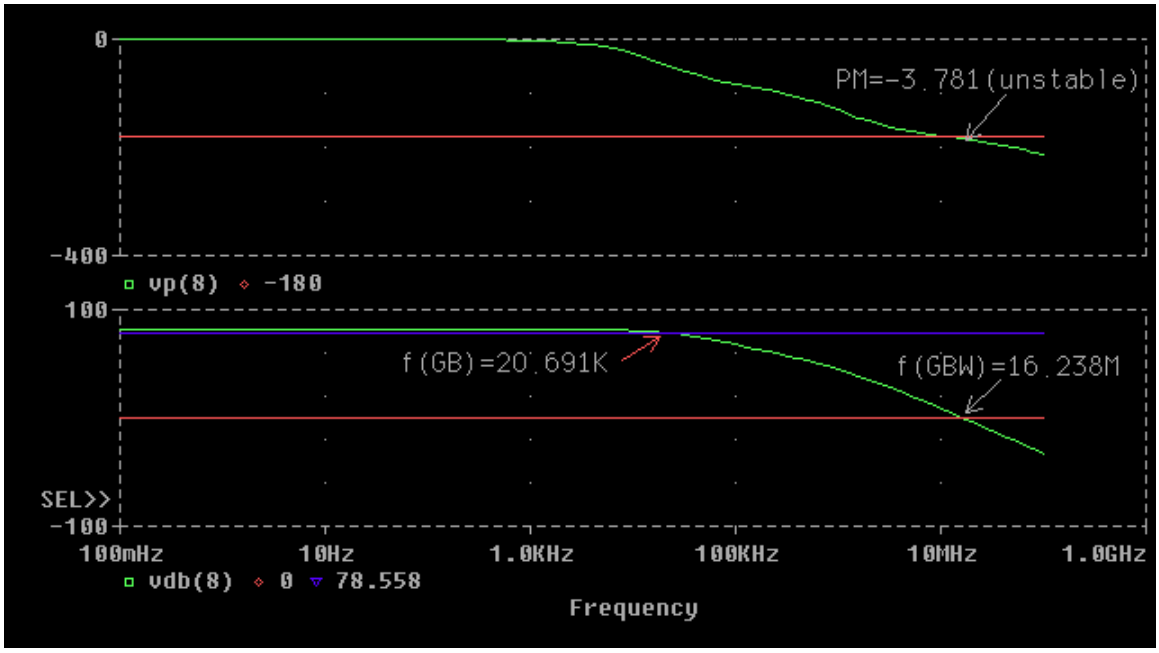
```
M7  8  9 3 3    PMOS1  W=60U    L=6.6U
M8  9  9 3 3    PMOS1  W=60U    L=6.6U

* External Components
CL  8  0        2pF
RB 9 0          175K

* SPICE Parameters
.MODEL NMOS1 NMOS VTO=1 KP=40U
+ GAMMA=1.0 LAMBDA=0.02 PHI=0.6
+ TOX=0.05U LD=0.5U CJ=5E-4 CJSW=10E-10
+ U0=550 MJ=0.5 MJSW=0.5 CGSO=0.4E-9 CGDO=0.4E-9
.MODEL PMOS1 PMOS VTO=-1 KP=15U
+ GAMMA=0.6 LAMBDA=0.02 PHI=0.6
+ TOX=0.05U LD=0.5U CJ=5E-4 CJSW=10E-10
+ U0=200 MJ=0.5 MJSW=0.5 CGSO=0.4E-9 CGDO=0.4E-9

*Analysis
.TRAN .1ns 40us
.PROBE
.END
```



4.2.3 Comparator Open-loop Transfer Function

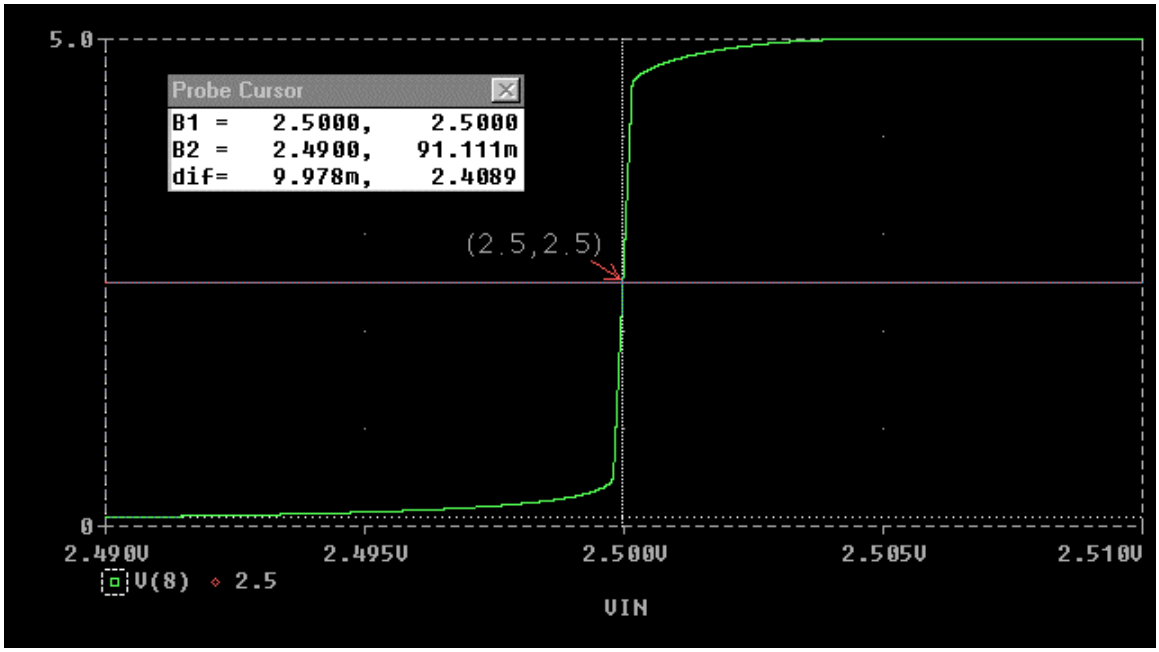
```
* Filename="diffcmpp3.cir"
* CMOS Comparator with PMOS Input Drivers

* Input Signals
VIN 2 0 AC 1V
VOS 1 0 DC -88.501uV

* Power Supplies
```

```
VDD 3 0 DC 5VOLT
VSS 4 0 DC -5VOLT

* Netlist for CMOS Comparator in Nwell
M1   5   1 7 7    PMOS1   W=15U    L=6.6U
M2   6   2 7 7    PMOS1   W=15U    L=6.6U
M3   5   5 4 4    NMOS1   W=5.4U   L=6.6U
M4   6   5 4 4    NMOS1   W=5.4U   L=6.6U
M5   7   9 3 3    PMOS1   W=30U    L=6.6U
M6   8   6 4 4    NMOS1   W=21.6U  L=6.6U
M7   8   9 3 3    PMOS1   W=60U    L=6.6U
M8   9   9 3 3    PMOS1   W=60U    L=6.6U

* External Components
CL   8   0         2pF
RB 9 0           175K

* SPICE Parameters
.MODEL NMOS1 NMOS VTO=1 KP=40U
+ GAMMA=1.0 LAMBDA=0.02 PHI=0.6
+ TOX=0.05U LD=0.5U CJ=5E-4 CJSW=10E-10
+ U0=550 MJ=0.5 MJSW=0.5 CGSO=0.4E-9 CGDO=0.4E-9
.MODEL PMOS1 PMOS VTO=-1 KP=15U
+ GAMMA=0.6 LAMBDA=0.02 PHI=0.6
+ TOX=0.05U LD=0.5U CJ=5E-4 CJSW=10E-10
+ U0=200 MJ=0.5 MJSW=0.5 CGSO=0.4E-9 CGDO=0.4E-9

* Analysis
.AC DEC 10 0.1HZ 100MegHZ
.PROBE
.END
```



4.2.4 Comparator Adjusted for 0-5V Operation

```
* Filename="diffcp5.cir"
* CMOS Comparator with PMOS Input Drivers

* Input Signals
VIN 2 0 DC 0V
VOS 1 0 DC 2.5V

* Power Supplies
VDD 3 0 DC 5VOLT
VSS 4 0 DC 0VOLT

* Netlist for CMOS Comparator in Nwell
M1  5  1 7 7    PMOS1  W=15U    L=6.6U
M2  6  2 7 7    PMOS1  W=15U    L=6.6U
M3  5  5 4 4    NMOS1  W=5.4U   L=6.6U
M4  6  5 4 4    NMOS1  W=5.4U   L=6.6U
M5  7  9 3 3    PMOS1  W=30U    L=6.6U
M6  8  6 4 4    NMOS1  W=21.6U  L=6.6U
M7  8  9 3 3    PMOS1  W=60U    L=6.6U
M8  9  9 3 3    PMOS1  W=60U    L=6.6U

* External Components
CL  8  0        2pF
RB 9 0          175K

* SPICE Parameters
.MODEL NMOS1 NMOS VTO=1 KP=40U
+ GAMMA=1.0 LAMBDA=0.02 PHI=0.6
+ TOX=0.05U LD=0.5U CJ=5E-4 CJSW=10E-10
+ U0=550 MJ=0.5 MJSW=0.5 CGSO=0.4E-9 CGDO=0.4E-9
.MODEL PMOS1 PMOS VTO=-1 KP=15U
+ GAMMA=0.6 LAMBDA=0.02 PHI=0.6
+ TOX=0.05U LD=0.5U CJ=5E-4 CJSW=10E-10
+ U0=200 MJ=0.5 MJSW=0.5 CGSO=0.4E-9 CGDO=0.4E-9

* Analysis
.DC VIN 2.49V 2.51V 1uV
.PROBE
.END
```



4.2.5 Comparator Transient Response for 0-5V Operation

```
* Filename="diffcp5t.cir"
* MOS Diff Amp with PMOS Input and Current Mirror Load

* Input Signal
VIN 2 0 PWL(0,2.495V 10us,2.495V 10.01us,2.505V 30us, 2.505V
30.01us,2.495V 1s, 2.495V)
VOS 1 0 DC 2.5V

*Power Supplies
VDD 3 0 DC 5VOLT
VSS 4 0 DC 0VOLT

* Netlist for CMOS Comparator in Nwell
M1  5  1 7 7    PMOS1  W=15U    L=6.6U
M2  6  2 7 7    PMOS1  W=15U    L=6.6U
M3  5  5 4 4    NMOS1  W=5.4U   L=6.6U
M4  6  5 4 4    NMOS1  W=5.4U   L=6.6U
M5  7  9 3 3    PMOS1  W=30U    L=6.6U
M6  8  6 4 4    NMOS1  W=21.6U  L=6.6U
M7  8  9 3 3    PMOS1  W=60U    L=6.6U
M8  9  9 3 3    PMOS1  W=60U    L=6.6U

* External Components
CL  8  0        2pF
RB 9 0          175K

* SPICE Parameters
.MODEL NMOS1 NMOS VTO=1 KP=40U
+ GAMMA=1.0 LAMBDA=0.02 PHI=0.6
+ TOX=0.05U LD=0.5U CJ=5E-4 CJSW=10E-10
+ U0=550 MJ=0.5 MJSW=0.5 CGSO=0.4E-9 CGDO=0.4E-9
.MODEL PMOS1 PMOS VTO=-1 KP=15U
+ GAMMA=0.6 LAMBDA=0.02 PHI=0.6
+ TOX=0.05U LD=0.5U CJ=5E-4 CJSW=10E-10
+ U0=200 MJ=0.5 MJSW=0.5 CGSO=0.4E-9 CGDO=0.4E-9

*Analysis
```

```
.TRAN .1ns 40us
.PROBE
.END
```