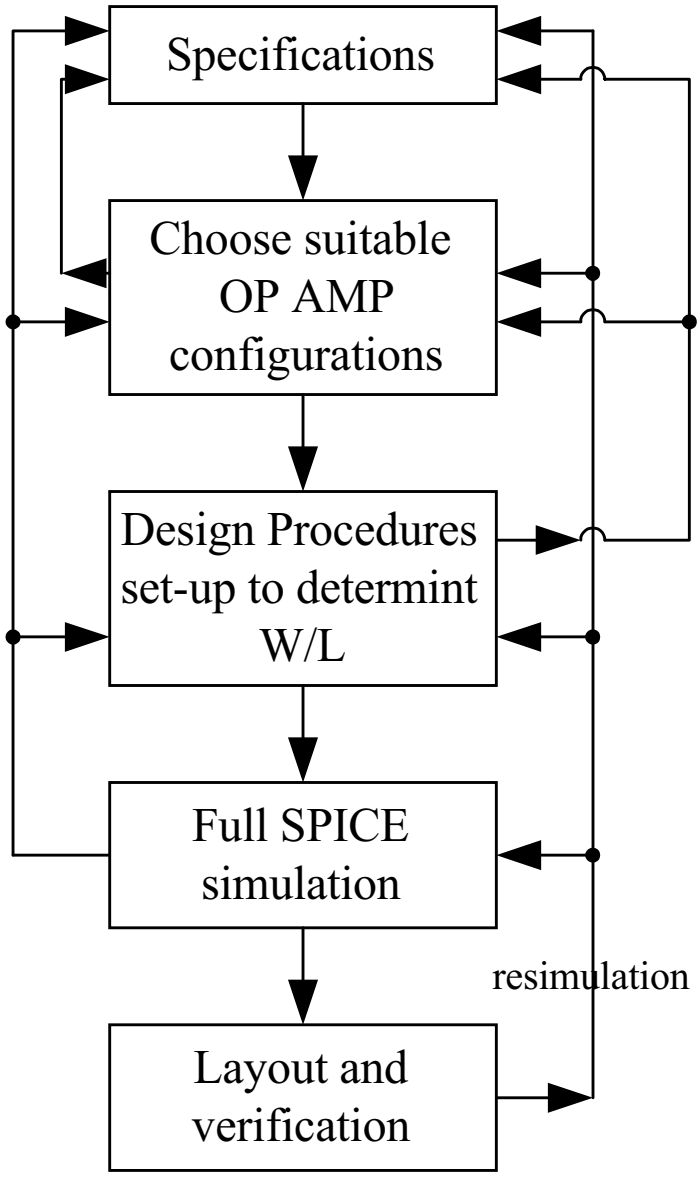
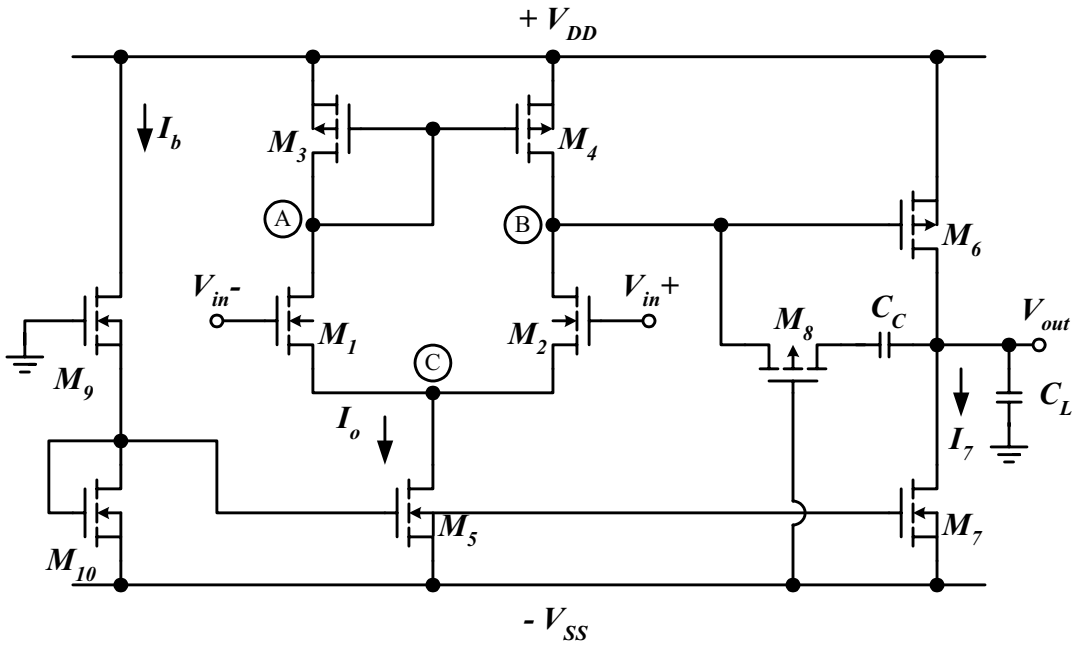
Chapter 7 Design Procedure of CMOS OP AMPs and Pratical Design Considerations on Noise and Offset

§ 7-1 Typical design procedure of two-stage CMOS OP AMPs

Synthesis or Design：Determine the circuit configuration and its MOS device dimensions from the specfications.

Flow Diagram：





Specfications

Low frequency gain	≧ 70dB	Phase margin	> 60°
Unity-gain frequency	≧ 2MHz	C_L	10pF
Slew rate	≧ 4V/μs	V_{DD}=V_{SS}	5V
CMRR	≧ 80dB		

Device parameters

$\mu C_{ox}/2$	$30\mu A/V^2$	$12\mu A/V^2$
	(NMOS)	(PMOS)
V_{TO}	1.2V	-1V

Procedures：

1. Choose a suitable C_c

   Example：choose C_c=C_L=10pF

2. According to the phase margin in the specifications, determine the second pole position.

Example：choose f_T= 2MHz

$$|S_{p2}| \cong +\frac{g_{m6}}{C_L} = 3\omega_u \cong 3g_{mi}/C_c$$

$$|S_{P2}| = 3\omega_u \Rightarrow \text{ Phase margin} > 60^o$$

3. Determine the transconductances of the first stage and the second stage.

   Example : $g_{m6} = 3g_{mi} = 3\omega_u C_L = 3\times 2\pi \times 2\times 10^6 \times 10^{-11}$

   $\Rightarrow g_{m6} = 377\mu$ mho

   $g_{mi} = 125.7\mu$ mho

4. From the slew rate specification, determine the bias currents in the first and the second stages.

   Example : $S = \frac{I_o}{C_C} \geq 4V/\mu s$

   Choose $S = 4V/\mu s, \Rightarrow I_o = 40\mu A$

   The negative-going slew rate is also limited by the Q_7 current source. To reduce or eliminate its effect, S_{ro} is set to 4S.

   $$S_{ro} = 2.5S = 10V/\mu s = \frac{I_7}{C_L}$$

   $$\Rightarrow I_7 = C_L S_{ro} = 100\mu A$$

5. Use the design rule for reducing the systematic offset voltage to design the transconductance of the load MOSFET's.

   Example : $\frac{(W/L)_3}{(W/L)_6} = \frac{(W/L)_4}{(W/L)_6} = \frac{I_o/2}{I_7} = \frac{1}{5}$

   $$g_{ml} = g_{m3} = g_{m4} = \sqrt{\frac{(W/L)_3 \cdot I_o/2}{(W/L)_6 \cdot I_7}}\, g_{m6}$$

   $$= \frac{I_o/2}{I_7} g_{m6} = \frac{1}{5} g_{m6} \cong 75.4\mu \text{ mho}$$

6. Calculate A_{dm} and *CMRR* to verify the design.

Example : $A_{dm} = \frac{g_{mi}g_{m6}}{(g_{dl}+g_{di})(g_{d6}+g_{d7})} \cong \frac{g_{mi}g_{m6}}{(\lambda I_o)(2\lambda I_7)}$

$\cong 6582 > 76dB \quad (\lambda = 0.03V^{-1} \text{ for } L \cong 10\mu m)$

$$CMRR = 2\frac{g_{mi}g_{ml}}{g_{d5}g_{di}} \approx \frac{2g_{mi}g_{ml}}{(\lambda I_o)(\lambda I_o/2)} \approx 26327 \approx 88dB$$

$g_{mi} = C_cW_u$, $I_o = C_cS$, $g_{m6}=3W_uC_L$, $I_7=S_{ro}C_L$

$g_{ml}=I_og_{m6}/2I_7=3C_cSW_u/2S_{ro}$

$$\Rightarrow \quad A_{dm} \approx \frac{3\omega_u^{\ 2}}{2\lambda^2 S_{ro}S} \quad ; \quad CMRR \approx \frac{6\omega_u^{\ 2}}{\lambda^2 S_{ro}S} \approx 4A_{dm}$$

If A_{dm} and *CMRR* could not satisfy the specifications, ω_o , S, and g_{mi} or g_{m6} can be readjusted .

7. Determine the nulling resistor R_c provoded by M_8.

Example: If $S_z \rightarrow S_{p2}$

$$R_c = \frac{1+(C_d+C_L)/C_c}{g_{m6}} \approx \frac{2}{g_{m6}} \approx 5.3K\Omega$$

If $S_z \rightarrow \infty$

$$R_c = \frac{1}{g_{m6}} = 2.65K\Omega$$

$$R_c = \frac{1}{\frac{\mu_p C_{ox}}{2}\frac{W_8}{L_8}\left[2\left(V_{SS}+V_B-|V_{TH8}|\right)\right]}$$

8. Dimension M_5 and M_7.

W/L can't be too small $\Rightarrow$ too large V_{GS}.

Can't be too large $\Rightarrow$ C_w too large $\Rightarrow$ *CMRR* $\downarrow$

$C_L \uparrow \Rightarrow$ phase margin $\downarrow$

Example: $\left(\frac{W}{L}\right)_5 = \frac{I_o}{\frac{\mu_n C_{ox}}{2}(V_{GS5} - V_{TH5})^2} \approx 5.33$ ($\frac{\mu_n C_{ox}}{2} \approx 30 \mu A/V^2$

$V_{GS5} - V_{TH5} \approx 0.5V$)

$$\left(\frac{W}{L}\right)_7 = \frac{I_7}{\frac{\mu_n C_{ox}}{2}(V_{GS7} - V_{TH7})^2} \approx 13.33$$

Choose $L_5=L_7=10\mu m \Rightarrow W_5=54\mu m$, $W_7=133\mu m$

9. Dimension M_1-M_4 and M_6

Example: $g_m \approx 2\sqrt{\frac{\mu C_{ox}}{2}\left(\frac{W}{L}\right) I_D}$ 0

$$\left(W/L\right)_1 = \left(W/L\right)_2 \approx \frac{8m_i^2}{4\frac{\mu_n C_{ox}}{2} I_o/2} \approx 6.58$$

$$(W/L)_3 = (W/L)_4 \approx \frac{g_{ml}^2}{4\frac{\mu_p C_{ox}}{2}\frac{I_o}{2}} \approx 5.92$$

$$(W/L)_6 = 5(W/L)_3 \approx 29.6$$

Choose $L=10\ \mu m$

$\Rightarrow\ W_1 = W_2 = 66\mu m$ ，$W_3 = W_4 = 60\mu m$ ，$W_6 = 300\mu m$

10. Estimate the dc bias voltage.

Example：$|V_{GS3}| = |V_{THP3}| + \sqrt{\frac{I_o/2}{\frac{\mu_p C_{ox}}{2}(W/L)_3}} = 1 + \sqrt{\frac{20}{12\times 6}} \approx 1.527$

$$\Rightarrow V_A = V_B = V_{DD} - |V_{GS3}| = 3.473V$$

$$\frac{I_O}{2} = \frac{\mu_n C_{ox}}{2}(W/L)_1(-V_C - V_{THn})^2$$

$$\Rightarrow V_C = -1.518V$$

11. Dimension M_8

Example： $2\frac{\mu_p C_{ox}}{2}(W/L)_8(5+3.473-1)=\frac{1}{R_C}$

$\Rightarrow (W/L)_8 \approx 1.052$

choose $W_8 = L_8 = 10\mu m$.

12. Determine V_{BIAS} and dimension M_9 and M_{10}

Example： $V_{GS} = V_{THn} + 0.5V = 1.7V$

$V_{BIAS} = -V_{SS} + V_{GSS} = -3.3V$

Choose $I_b = 20\mu A$

$\Rightarrow V_{GS9} = 0 - V_{BIAS} = 3.3V \Rightarrow V_{BIAS} = -3.3V$

$V_{GS10} = V_{BIAS} + V_{SS} = -1.7V$

$$(W/L)_9 = \frac{I_b}{\frac{\mu_n C_{ox}}{2}(V_{GS9} - V_{THn})^2} \approx 0.1512$$

$$(W/L)_{10} = \frac{I_b}{\frac{\mu_n C_{ox}}{2}(V_{GS10} - V_{THn})^2} \approx 0.2667$$

Choose $W_9 = 10\mu m$, $L_9 = 66\mu m$ and

$W_{10} = 27\mu m$, $L_{10} = 10\mu m$.

13. Use SPICE to simulate the overall OP AMP and make the necessary adjustment.

Reference : Reference Book No. 3, (Gregorian and Temes) pp. 222-241.

§7-2 Practical Design Consideration on Noise

§7-2.1 Noise of MOS devices

1) shot noise

* Due to the fluctuation in the number of carriers crossing a given surface in the conductor in any time interval.
* If the carrier density is low and the external electric field is high so that the interaction among the carriers are negligible, we have

$$\overline{i_{ns}^2} = 2qI(BW)$$

where i_{ns} is the random variation of the current.
I is the average current.
BW is the bandwidth in which the noise is measured.

* When an MOSFET is operated in the saturation region, inversion carrier density is high. => $\overline{i_{ns}^2}$ is much smaller than that predicted by the formula.

Shot noise is not important.

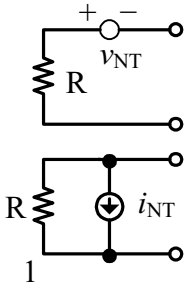
* In the subthreshold region, shot noise is higher.

2) Thermal noise

* Generated by the random thermal motion of the carriers in a resistor.
* The mean square of the noise voltage v_{nT} and the noise current i_{nT} are

$$\overline{v_{nT}^2} = 4KTR(BW)$$

$$\overline{i_{nT}^2} = 4KTG(BW)$$

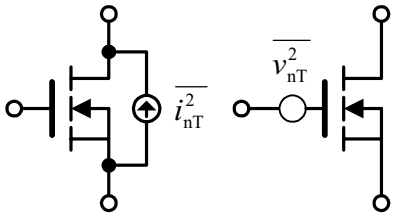


* In MOSFETs, R is the incremental channel resistance.

If the MOSFET is in the saturation region, $R = \frac{3}{2g_m} = \frac{1}{\frac{2}{3}g_m}$

$$\overline{v_{nT}^2} = \overline{(i_{nT}/g_m)^2} = \frac{8}{3}\frac{KT}{g_m}BW$$

* The spectral density $\overline{v_{nT}^2}/BW$ is independent of frequency $\Rightarrow$ White noise.
* Circuit models:



$\overline{v_{nT}^2}$:gate-referred noise voltage source.

* $\sqrt{\frac{\overline{v_{nT}^2}}{BW}} = \frac{nV}{\sqrt{H_z}}$

* When the MOSFET is turned off (R=∞, G=0), $\overline{i_{nT}^2}$ is very small.

  ⇒ Noiseless open circuit.

3) Flicker $(1/f)$ noise

* Generated by the trapping and releasing electrons from the channel caused by the interfacial states.
* Slow process ⇒ important at low frequencies

  ⇒ $1/f$ noise. Below ~ KH_z

* $\overline{v_{nf}^2} = \frac{K}{C_{ox}WL}\frac{BW}{f}$ $\qquad \overline{i_{nf}^2} = g_m{}^2\overline{v_{nf}^2}$

* (WL) ↑ , C_{ox} ↑ , Temperature ↓ , density of surface state ↓ ⇒ $\overline{v_{nf}^2}$ ↓

4) Combined noise

$$i_n = \sqrt{\overline{i_{nT}^2} + \overline{i_{nf}^2}} = \sqrt{(4KTG + Kg_m^2/(C_{ox}WLf)]BW}$$

∵independent noise sources.

$$v_n = \frac{i_n}{g_m}$$

§7-2.2 Noise Performance of NMOS Amplifiers

1) Enhancement-load amplifier

$$A_{V1} = -\alpha_2\sqrt{\frac{W_1L_2}{W_2L_1}} \quad \text{for} \quad e_{n1}$$

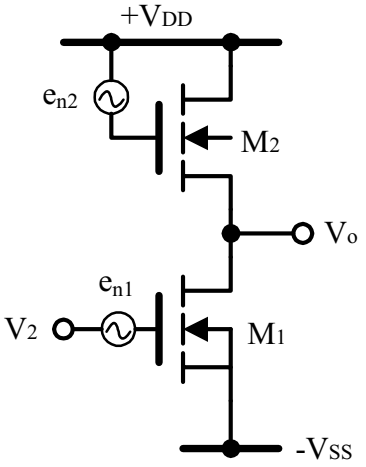
$$A_{V2} = \alpha_2 \quad \text{for} \quad e_{n2}$$

The equivalent input noise voltage

$$e_n(IN) = \frac{1}{A_{V1}}\sqrt{(A_{V1}e_{n1})^2 + (A_{V2}e_{n2})^2}$$

$$= e_{n1}\sqrt{1 + (\frac{A_{V2}e_{n2}}{A_{V1}e_{n1}})^2}$$

$$= \sqrt{\frac{a_n}{W_1L_1}(1 + \frac{L_1}{L_2})^2}$$



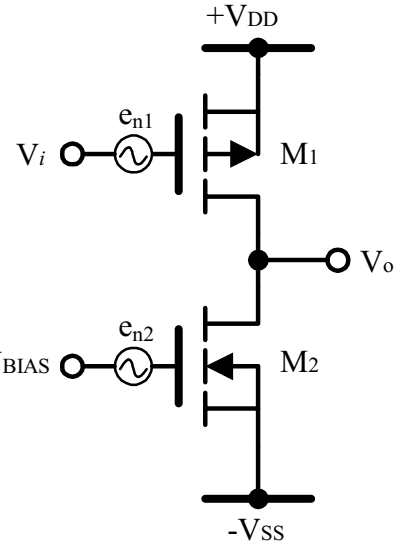
e_n : 1/f noise

$$e_n = \sqrt{\frac{a_n}{WL}}$$

* $W_1 \uparrow$, $L_2 \uparrow$ $\Rightarrow$ smaller $e_n(IN)$
* There exits an optimal $L_1 = L_2$ * Independent of W_2

§7-2.3 Noise Performance of CMOS Amplifiers

1) CMOS amplifier



$$A_{V1} = -g_{m1}(r_{ds1} \| r_{ds2})$$

$$A_{V2} = -g_{m2}(r_{ds1} \| r_{ds2})$$

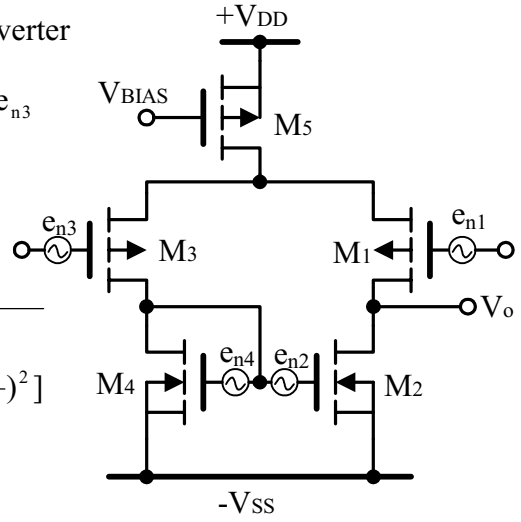
$$g_{m1} = 2\sqrt{(\frac{\mu_n C_{ox}}{2})_1 \frac{W_1}{L_1} I_D}$$

$$g_{m1} = 2\sqrt{(\frac{\mu_n C_{ox}}{2})_2 \frac{W_2}{L_2} I_D}$$

$$e_n(IN) = \sqrt{\frac{a_{n1}}{W_1 L_1}[1 + \frac{(\frac{\mu_p C_{ox}}{2})_2 a_{n2}}{(\frac{\mu_n C_{ox}}{2})_1 a_{n1}} (\frac{L_1}{L_2})^2]}$$

Design considerations for low noise can be found.

2) CMOS differential-input to single-ended converter



$$A_{V1} = \frac{1}{2}(g_{m1} + g_{m2})(r_{ds1} \| r_{ds2}) \quad \text{for } e_{n1},\ e_{n3}$$

$$A_{V2} = g_{m2}(r_{ds1} \| r_{ds2})$$

If $g_{m1} = g_{m3}$ and $g_{m2} = g_{m4}$

$$\Rightarrow e_n(IN) = \sqrt{2\frac{a_{n1}}{W_1 L_1}[1 + \frac{(\frac{\mu_n C_{ox}}{2})_2 a_{n2}}{(\frac{\mu_p C_{ox}}{2})_1 a_{n1}} (\frac{L_1}{L_2})^2]}$$

* $W_1 \uparrow$, $L_2 \uparrow$, $e_n(IN) \downarrow$

* Optimal $L_1 = \sqrt{\frac{(\frac{\mu_p C_{ox}}{2})_1 a_{n1}}{(\frac{\mu_n C_{ox}}{2})_2 a_{n2}}} L_2$

* The noise from M_2 and M_4 loads is very important!

Example : PMOS : $(\frac{\mu C_{ox}}{2})_p = 3\mu A / V^2$

$$a_{np} = 48 \times 10^3 (\mu V \cdot \mu m)^2 \quad \text{for } 20Hz \sim 20KHz$$

NMOS : $(\frac{\mu C_{ox}}{2})_N = 7\mu A / V^2$

$$a_{nn} = 380 \times 10^3 (\mu V \cdot \mu m)^2 \quad \text{for} \quad 20Hz \sim 20KHz$$

* NMOS is much more noisy than PMOS due to much larger $1/f$ noise

Why? 1.higher surface-state density

2.nonuniform trap center distribution (more centers near conduction band)

3.Efficient election trapping and releasing.

Bias current $I_D = 5\mu A$, Gain : $\approx 44dB$

Design Ⅰ: M_1, M_3 : $500\mu m / 5\mu m$ PMOS

M_2, M_4 : $100\mu m / 4\mu m$ NMOS

$\Rightarrow e_n(IN) = 38\mu V \quad 20Hz \sim 20KHz$

(33.9)

Design Ⅰ: M_1, M_3 : $500\mu m / 5\mu m$ PMOS

M_2, M_4 : $50\mu m / 44\mu m$ NMOS

$\Rightarrow e_n(IN) = 7.5\mu V \quad 20Hz \sim 20KHz$

(6.9)

3) CMOS inverter amplifier

$$A_V \equiv \frac{V_o}{V_i} = (g_{m1} + g_{m2})(r_{ds1} \| r_{ds2})$$

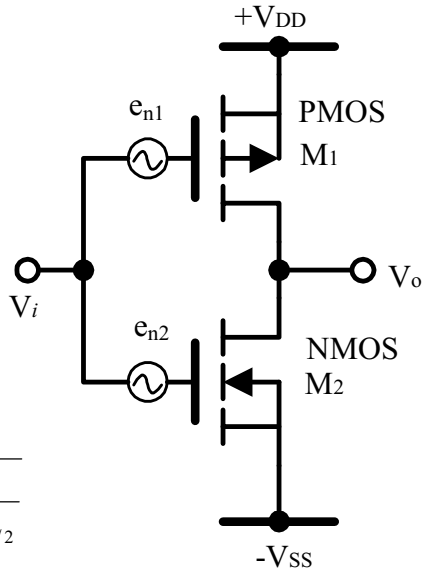
$$A_{V1} = -g_{m1}(r_{ds1} \| r_{ds2}) \quad \text{for} \quad e_{n1}$$

$$A_{V2} = -g_{m2}(r_{ds1} \| r_{ds2}) \quad \text{for} \quad e_{n2}$$

$$e_n(IN) = \frac{\sqrt{(g_{m1}e_{n1})^2 + (g_{m2}e_{n2})^2}}{g_{m1} + g_{m2}}$$

If $g_{m1} = g_{m2}$

$$\Rightarrow e_n(IN) = \frac{1}{2}\sqrt{e_{n1}^{\ 2} + e_{n2}^{\ 2}} = \frac{1}{2}\sqrt{\frac{a_{n1}}{W_1 L_1} + \frac{a_{n2}}{W_2 L_2}}$$



* Larger size WL $\Rightarrow$ smaller noise

If $g_{m1} \neq g_{m2}$

$$\Rightarrow e_n(IN) = \sqrt{\frac{a_{n1}}{W_1 L_1}\left(1+\frac{\left(\frac{\mu_n C_{ox}}{2}\right)_2}{\left(\frac{\mu_p C_{ox}}{2}\right)_1}\frac{a_{n2}}{a_{n1}}\frac{L_2^{\,2}}{L_1^{\,2}}\right)} \Big/ \left(1+\sqrt{\frac{\left(\frac{\mu_n C_{ox}}{2}\right)_2}{\left(\frac{\mu_p C_{ox}}{2}\right)_1}\frac{W_2}{W_1}\frac{L_1}{L_2}}\right)$$

* Increase the channel length of the transistor having the highest a_n parameter.

Example : Bias current 100μA

Design Ⅰ : $M_1 : {}^{1000\mu m}/_{5\mu m}$, $M2 : {}^{400\mu m}/_{4\mu m}$

$\Rightarrow e_n(IN) = 8.1\mu V(7.97\mu V)$ 20Hz ~ 20KHz

Design Ⅱ : $M_1 : {}^{1000\mu m}/_{5\mu m}$, $M2 : {}^{200\mu m}/_{8\mu m}$

$\Rightarrow e_n(IN) = 5.9\mu V(5.65\mu V)$ 20Hz ~ 20KHz

Design Ⅲ : $M_1 : {}^{500\mu m}/_{10\mu m}$, $M2 : {}^{400\mu m}/_{4\mu m}$

$\Rightarrow e_n(IN) = 10.5\mu V(10.36\mu V)$

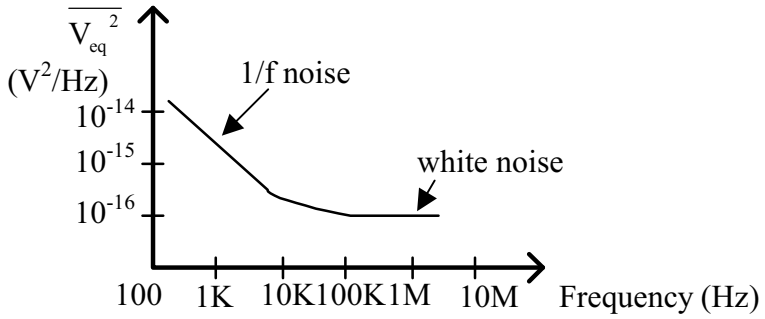
* Best noise figure $\Rightarrow$ highest ${}^{W}/_{L}$ in PMOS

lowest ${}^{W}/_{L}$ in NMOS

Note : WL for PMOS (NMOS) are the same.

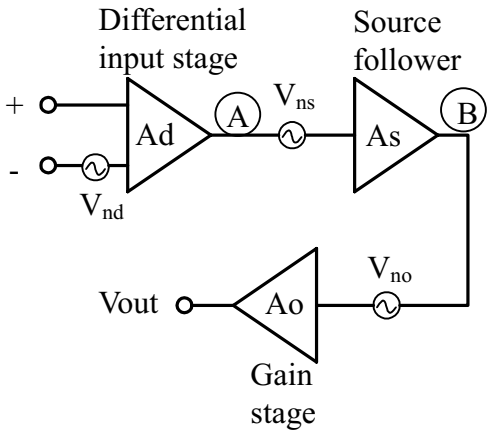
Reference : J.-C. Bertails, JSSC, vol.SC-14, pp.773-776, Aug.1979.

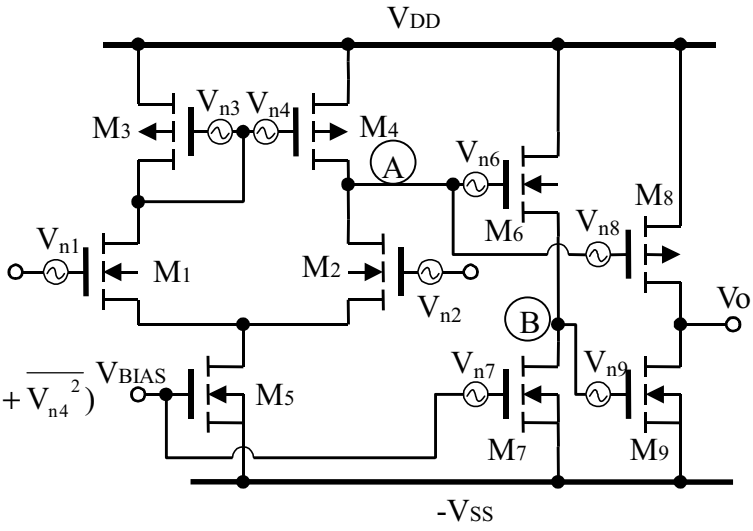
Noise spectrum of a typical MOSFET :



§7-2.4 Noise performance of CMOS OP AMPs

1.Midband Analysis





$$\overline{V_{nd}^2} = \overline{V_{n1}^2} + \overline{V_{n2}^2} + \left(\frac{g_{m4}}{g_{m1}}\right)\left(\overline{V_{n3}^2} + \overline{V_{n4}^2}\right)$$

$$\overline{V_{ns}^2} = \overline{V_{n6}^2} + (g_{m7}/g_{m6})^2\,\overline{V_{n7}^2}$$

$$\overline{V_n^2} \approx \overline{V_{nd}^2} + \overline{V_{ns}^2}\Big/A_d^2 = \overline{V_{n1}^2} + \overline{V_{n2}^2} + \left(g_{m4}\Big/g_{m1}\right)^2\left(\overline{V_{n3}^2} + \overline{V_{n4}^2}\right) + \left[\overline{V_{n6}^2} + \left(g_{m7}\Big/g_{m6}\right)^2\overline{V_{n7}^2}\right]\Big/A_d^2$$

* At low frequency (<1KHz) , $1/f$ noise dominates and $|A_d(w)| >> 1$

$\Rightarrow \overline{V_{ns}^2}$ has a negligible effect on the OP noise.

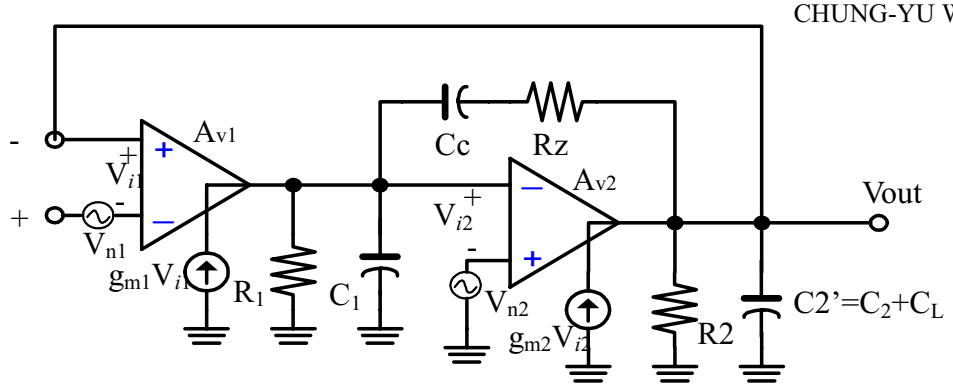
The input stage dominates the overall noise contribution.

* At high frequency where $|A_d(w)| \approx g_{m7}/g_{m6} >> 1$, ($\because M_6$, M_7 is a level shifter, g_{m6} is small to obtain a large $V_{Gs6} \Rightarrow g_{m7}/g_{m6} >> 1$), the effect of V_{n7} is comparable to that of V_{n1} and V_{n2}. Thus M_7 must be a low-noise device (like PMOS).

The effect of V_{no} is negligible on the total equivalent input noise voltage since the gain of the gain stage is very high.

§7-2.5 High frequency analysis (for white noise)

For CMOS 2-stage OP AMP (without level shifter), the small-signal equivalent circuit is



(under unity-gain feedback)

$$\frac{V_{out}}{V_{in1}}=\frac{A_V[1-sC_c(\frac{1}{g_{m2}}-R_z)]}{1+A_V+as+bs^2+cs^3}$$

$$\frac{V_{out}}{V_{in2}}=A_{V2}\frac{\{1+s[C_c(R_1+R_z)+C_1R_1]+s^2C_1C_cR_1R_z\}}{(1+A_V)+as+bs^2cs^3}$$

when $A_V=A_{V1}+A_{V2}$

$$a=C_c[A_V(\frac{1}{g_{m1}}-\frac{1}{g_{m2}}+R_z)+R_1+R_2+R_z]+C_1R_1+C_2'R_2$$

$$b=R_1R_2(C_1C_2'+C_1C_c+C_2'C_c)+R_zC_c(C_1R_1+C_2'R_2)$$

$$c=C_1C_2'C_cR_1R_2R_z$$

Usually, $|A_V|>>1$, $R_z<<R_1$, $R_z<<R_2$, $C_1<<C_c$, $C_1<<C_L$, and $C_2<<C_L$

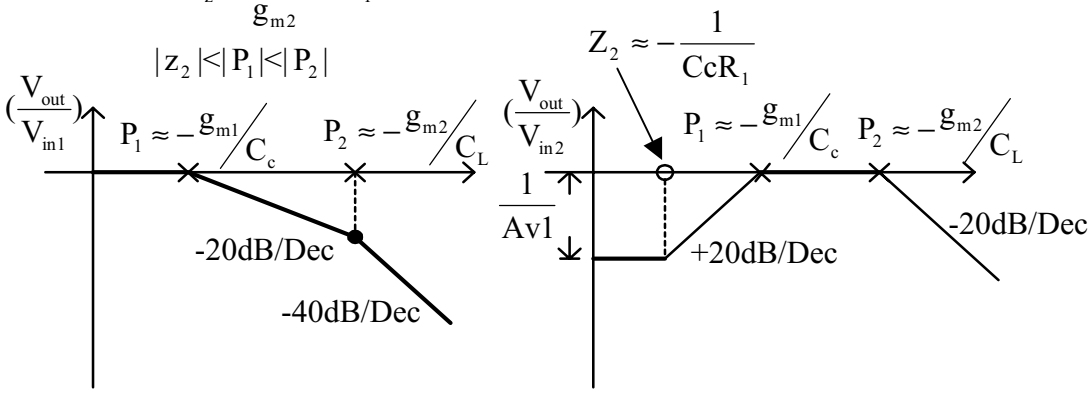
$\Rightarrow$ LHP Poleo : $P_1\approx-g_{m1}/C_c$; $P_2\approx-g_{m2}/C_L$, $P_3\approx-1/C_1R_z$

RHP zero $(\frac{V_{out1}}{V_{in1}})$: $z_1=[C_c(\frac{1}{g_{m2}}-R_z)]^{-1}$;

LHP zeros : $-\frac{1}{C_cR_1}=z_2$, $z_3\approx-\frac{1}{C_1R_z}$ $(z_3\rightarrow\infty)$

If $R_z=\frac{1}{g_{m2}}\Rightarrow z_1=\infty$

$|z_2|<|P_1|<|P_2|$



The equivalent noise bandwidths are

$$BW_1 = {g_{m1}}/{4C_c} \quad (= {|P_1|}/{4})$$

$$BW_2 = {g_{m2}}/{4C_L} - {g_{m1}}/{4C_c} \quad (= {|P_2|}/{4} - {|P_1|}/{4})$$

$$\approx {g_{m2}}/{4C_L} \quad (Cc >> C_L)$$

$$\overline{V_{ntot}}^2 = \sum 4KT\gamma_i \frac{1}{g_{mi}}(BW_i)A_i, \ \gamma_i = \text{constant}(\approx \frac{3}{2})$$

(Consider only thermal noise)

$$= \frac{A_V}{1+A_V} 4KT\gamma_1 \frac{1}{g_{m1}}({g_{m1}}/{4C_c}) + \frac{A_{V2}'}{1+A_V'} 4KT\gamma_2 \frac{1}{g_{m2}}({g_{m2}}/{4C_L})$$

$$= \frac{A_V}{1+A_V}\gamma_1 \frac{KT}{C_c} + \frac{A_{V2}'}{1+A_V'}\gamma_2 \frac{KT}{C_L}$$

where A_{V2}' and A_V' are average gains between P_1 and P_2.

* The total white noise of the OP AMP is inversely proportional to C_c and C_L.
* Due to the foldover effect in SCF, white noise (thermal noise) becomes important.
* 1) Clock feedthrough noise; 2) noises coupled from the power supplies, clock, and ground lines, and from the substrate; 3) white noise and flicker noise generated in the switches and OP AMPs are three major noise sources in the switched-capacitor circuits.

§7-2.6 Dynamic range of OP AMPs

$V_{in,max}$: the maximum input voltage which an OP AMP can handle without generating an excess amount of nonlinear distortion.

$V_{in,min}$: the minimum input signal voltage which still does not drown in noise and distortion.

$$\text{Dynamic range} \equiv 20\log_{10}({V_{in,max}}/{V_{in,min}})$$

For an open-loop OP AMP,

$$V_{in,max} \approx V_{cc} / A_d$$

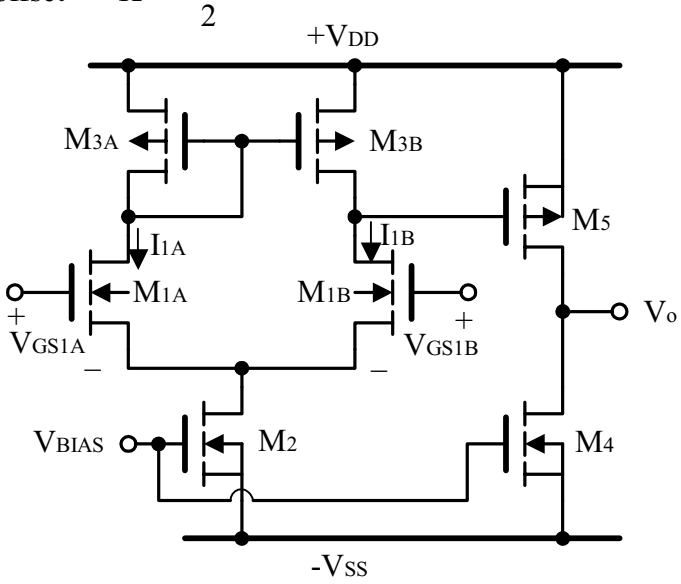
$$V_{in,min} \approx \sqrt{\overline{V_n^2}}$$

$$\Rightarrow \text{ Dynamic range } \approx 30-40\text{dB}.$$

§7-3 Practical Design Consideration on Offset

§7-3.1 Input offset voltage of a CMOS OP AMP

1). Random offset $\quad K \equiv \dfrac{C_{ox}\mu}{2}$



$V_o=V_{DD}-V_{GS3}$

$V_{GS3A}=V_{GS3B}-V_{GS3}$

$$V_{OS} \equiv V_{GSIA} - V_{GSIB} = \left[\frac{2}{K_{N1A}}\left(\frac{L}{W}\right)_{1A} I_{1A}\right]^{\frac{1}{2}} - \left[\frac{2}{K_{N1B}}\left(\frac{L}{W}\right)_{1B} I_{1B}\right]^{\frac{1}{2}} + V_{TH1A} - V_{TH1B}$$

$$= \Delta V_{TH1} + \left(\frac{2}{K_N} I_1\right)^{\frac{1}{2}} \left[\left(\frac{L_1 + \frac{\Delta L_1}{2}}{W_1 + \frac{\Delta W_1}{2}}\right)^{\frac{1}{2}} - \left[\frac{L_1 - \frac{\Delta L_1}{2}}{W_1 - \frac{\Delta W_1}{2}}\right]^{\frac{1}{2}}\right] + \cdots\cdots$$

$$\cong \Delta V_{TH1} + \left(\frac{2}{K_N} I_1 \frac{L_1}{W_1}\right)^{\frac{1}{2}} \left[\left(1 + \frac{1}{2}\frac{\Delta L}{2L_1}\right)\left(1 - \frac{1}{2}\frac{\Delta W}{2W_1}\right) - \left(1 - \frac{1}{2}\frac{\Delta L}{2L_1}\right)\left(1 + \frac{1}{2}\frac{\Delta W}{2W_1}\right)\right] + \cdots$$

$$\cong \Delta V_{TH1} + \left(\frac{2}{K_N} I_1 \frac{L_1}{W_1}\right)^{\frac{1}{2}} \left(\frac{\Delta L}{2L_1} - \frac{\Delta W}{2W_1}\right) - \left(\frac{2}{K_N} I_1 \frac{L_1}{W_1}\right)^{\frac{1}{2}} \left(\frac{\Delta K_N}{2K_N}\right) + \left(\frac{2}{K_N} I_1 \frac{L_1}{W_1}\right)^{\frac{1}{2}} \left(\frac{\Delta I}{2I_1}\right)$$

$$A \equiv \frac{A_1 + A_2}{2} \qquad \Delta A \equiv A_1 - A_2$$

$$\Delta I = I_{1A} - I_{1B} = \frac{K_{P3A}}{2}\left(\frac{W}{L}\right)_{3A}(V_{GS3} - V_{TH3A})^2 - \frac{K_{P3B}}{2}\left(\frac{W}{L}\right)_{3B}(V_{GS3} - V_{TH3B})^2$$

$$= \frac{K_P}{2}\frac{W_3}{L_3}(V_{GS3} - V_{TH3})^2\left(\frac{\Delta K_P}{K_P} + \frac{\Delta W_3}{W_3} - \frac{\Delta L_3}{L_3} - \frac{2\Delta V_{TH3}}{V_{GS3} - V_{TH3}}\right)$$

$$= I_1\left(\frac{\Delta K_P}{K_P} + \frac{\Delta W_3}{W_3} - \frac{\Delta L_3}{L_3} - \frac{2\Delta V_{TH3}}{V_{GS3} - V_{TH3}}\right)$$

$$\Rightarrow V_{OS} = \Delta V_{TH1} + \left(\frac{2}{K_N} I_1 \frac{L_1}{W_1}\right)^{\frac{1}{2}}\left[\frac{\Delta L_1}{2L_1} - \frac{\Delta W_1}{2W_1} - \frac{\Delta K_N}{2K_N} + \frac{\Delta K_P}{2K_P} + \frac{\Delta W_3}{2W_3} - \frac{\Delta L_3}{2L_3} - \frac{\Delta V_{TH3}}{V_{GS3} - V_{TH3}}\right]$$

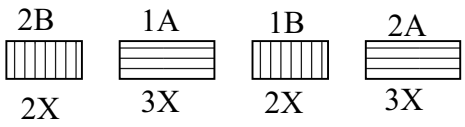
$$\cong \Delta V_{TH1} + (V_{GS1} - V_{TH1})\left(\frac{\Delta W_3}{2W_3} + \frac{\Delta L_1}{2L_1}\right) - \left(\frac{K_P}{K_N}\frac{W_3}{W_1}\right)^{\frac{1}{2}}\Delta V_{TH3} \quad (\text{If } \frac{\Delta L_3}{2L_3}, \frac{\Delta W_1}{2W_1} \to 0)$$

2).Systematic offset. $V_{OS} = \frac{V_{Odc}}{A_O}$ where $V_{Odc} \neq 0$ and A_O is the dc gain of the OP AMP.

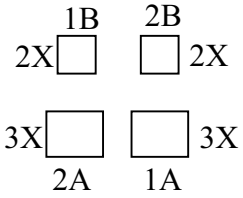
7-3.2 Low offset design techniques for CMOS OP AMPs

1. Layout techniques to reduce the random offset.

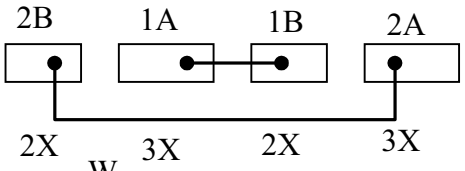
   a).linear varation of devices across a row of transistor or a matrix of transistors.

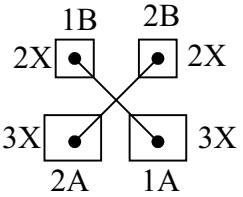


or



   b).cross-coupled connection





$I_{DS} \propto V_{gs}^{\ 2} \cdot \frac{W}{L}$ $L_{2B} = KL_{1B}, L_{2A} = KL_{1A}$, $\frac{L_{1B}}{L_{2A}} = \frac{L_{2B}}{L_{1A}} = N$, W's are the same

Cross-coupled: $I_{DS1A} + I_{DS1B} = I_{DS2A} + I_{DS2B}$

$$\frac{V_{GS1}^{\ 2}}{L_{1A}} + \frac{V_{GS1}^{\ 2}}{L_{1B}} = \frac{V_{GS2}^{\ 2}}{L_{2A}} + \frac{V_{GS2}^{\ 2}}{L_{2B}} \Rightarrow \frac{V_{GS1}}{V_{GS2}} \cong \sqrt{\frac{1+KN}{K+N}}$$

If K=1 => precision channel length control $\Rightarrow \frac{V_{GS1}}{V_{GS2}} \cong 1 \Rightarrow$ Ordered dimension error $\cong 0 \Rightarrow V_{OS} \cong 0$

If K=1.1, N=1.1 ➔ $\frac{V_{GS1}}{V_{GS2}} = 1.0023$

But for single-pair design (1B, 2B, or 1A, 2A)

$\frac{V_{GS1}}{V_{GS2}} = \sqrt{K} = \sqrt{1.1} = 1.049$ larger V_{GS} error ➔ larger V_{OS}

Ref: RCA Review, vol. 39, pp.250-277, June 1978.

c) Common-centroid structures to reduce ΔV_{TH}

Ref: IEEE JSSC, vol. SC-13, pp.791-798, Dec. 1978
IEEE JSSC, vol. SC-16, pp.661-668, Dec. 1981

2.General optimum matching rules to reduce the random offset

1. Same structure
2. Same temperature
3. Same shape, same size
4. Minimum distance
5. common-centroid geometries
6. Same orientation
7. Same surroundings
8. Non minimum size

Ref.: IEEE JSSC, vol. SC-20, pp.657-665, June 1985

3.Low $V_{GS} - V_{TH1}$ to reduce the dimensional random offset

4.Dimension design to eliminate the systematic offset

$\frac{(W/L)_{3A}}{(W/L)_5} = \frac{(W/L)_{3B}}{(W/L)_5} = \frac{1}{2}\frac{(W/L)_2}{(W/L)_4}$ ➔ $V_{odc} = 0$ ➔ systematic offset ≈ 0

To avoid the process-induced variations in channel lengths, we usually choose $L_5 = L_{3A} = L_{3B}$. But this design will enhance the noise contribution from the PMOS M_{3A}, M_{3B} (NMOS M_{3A}, M_{3B} for PMOS-input structure).

➔ A compromise is required.

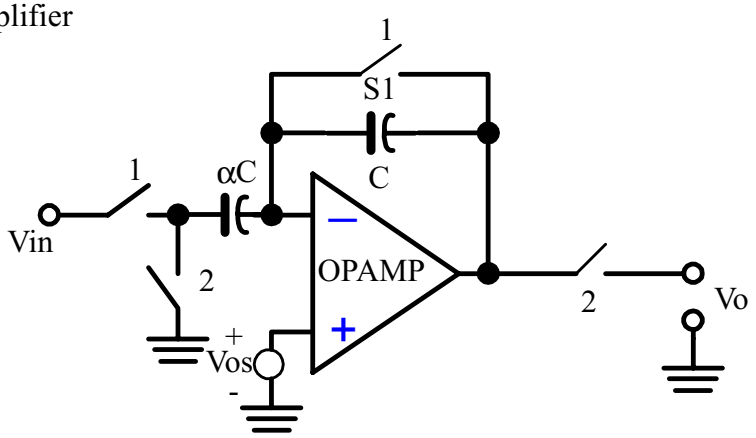
5.Sample-data techniques to eliminate the offset voltage.

Ref.: IEEE JSSC, p.499, Aug. 1978
IEEE JSSC, vol. SC-10, pp.371-379, Dec. 1975
IEEE JSSC, vol. SC-20, pp.805-807, June. 1985
IEEE JSSC, vol. SC-17, pp.1008-1013, Dec. 1986
IEEE JSSC, vol. SC-16, pp.745-748, Dec. 1981
IEEE JSSC, pp.837-844, Aug. 1985

Applications: Zero-offset OP AMPs, High-precision comparators, Instrumentation amplifiers, High-precision amplifiers, Switched-capacitor amplifier, Switched-capacitor network.

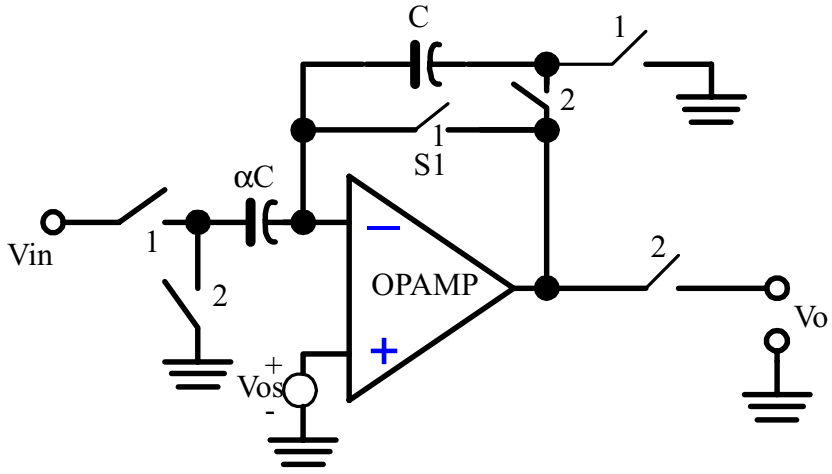
1) Offset cancellation in OP-AMP-based switched-capacitor(SC) amplifier

(1) SC amplifier

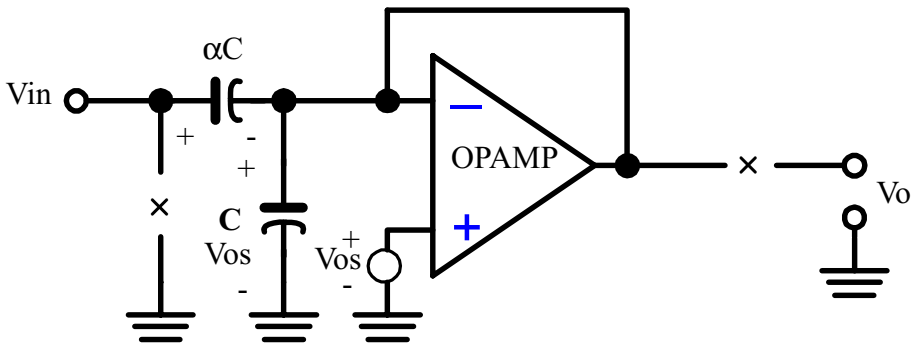


$$\frac{Vin\alpha C}{C}+V_{OS}=V_O \qquad \Rightarrow \frac{V_O}{V_{in}}=\alpha+\frac{V_{OS}}{V_{in}}$$

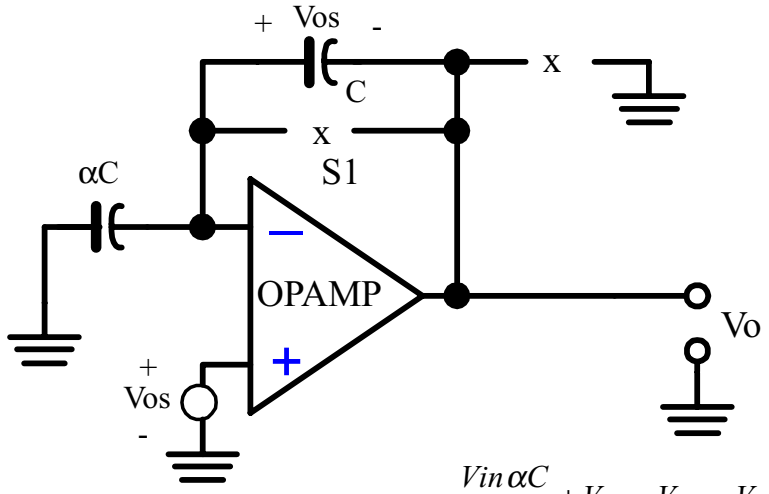
(2) Modified SC Amplifier



Step 1: Switch 1 ON, Switch 2 OFF:



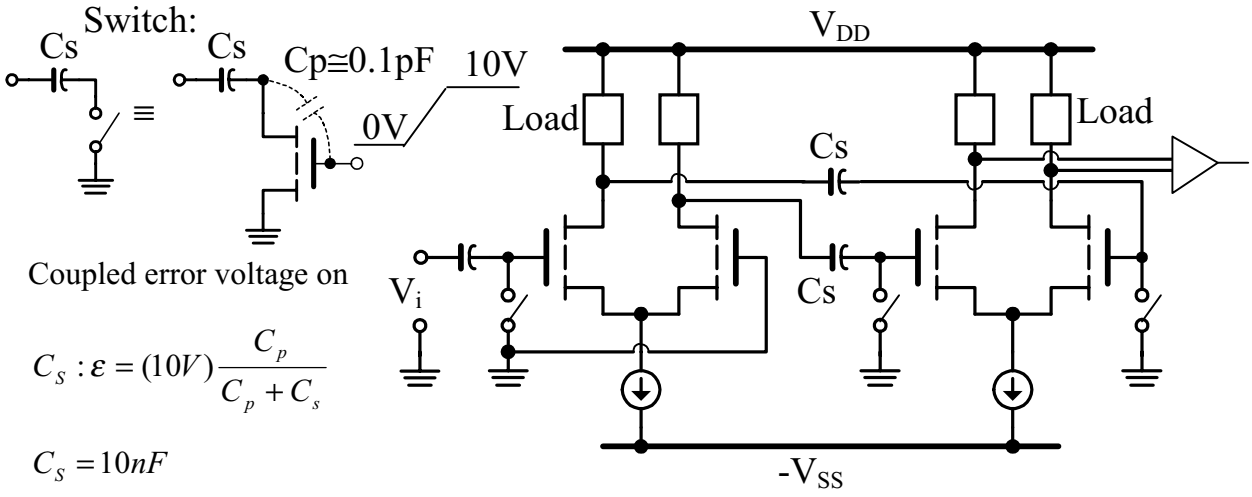
Step 2: Switch 2 ON, Switch 1 OFF:



$$\frac{Vin\,\alpha C}{C} + V_{OS} - V_{OS} = V_O$$

*The charge injection error of the switched S1 cannot be eliminated.

2) Offset cancellation in precision amplifier



Coupled error voltage on

$$C_S : \varepsilon = (10V)\frac{C_p}{C_p + C_s}$$

$$C_S = 10nF$$

$$\Rightarrow \varepsilon = 10V\,\frac{0.1pF}{0.1pF + 10000\,pF}$$

$$= 100\mu V$$

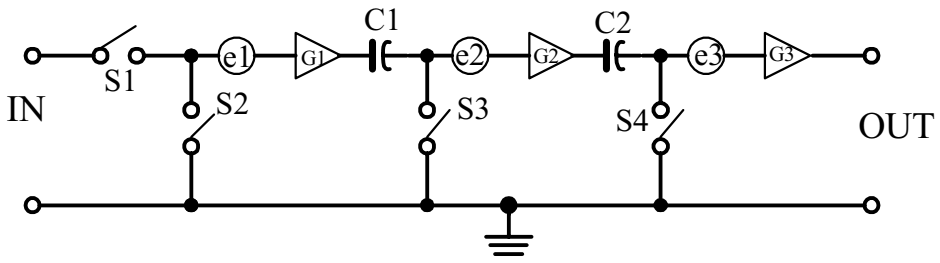
$$C_S \uparrow \varepsilon \downarrow$$

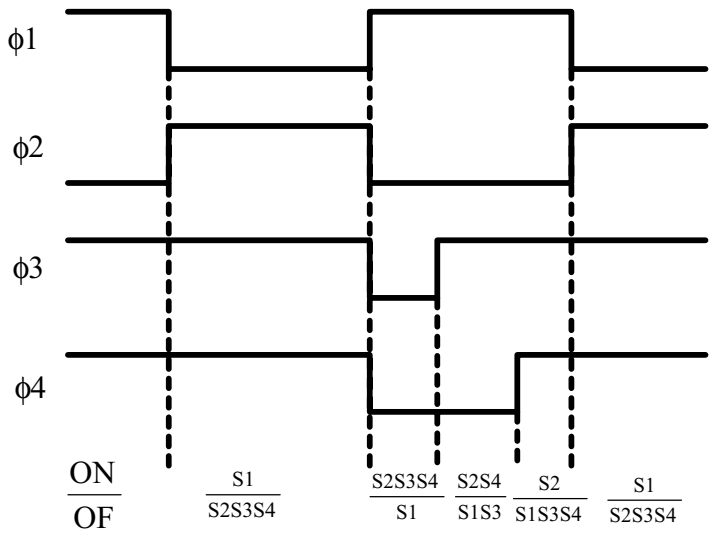
or using the differential outputs rather than the single output to eliminate the common mode voltage ε

* amplifier with offset voltage memorization
* residual voltage successive memorization (RSM) amplifier
* auto-zero design
* chopper-stablized design

※ capable of reducing the offset voltage by 1~4 order of magnitude

RSM amplifier(P-MOSFETs)





$V_{off} = (e_n + \varepsilon_n) / G_1 G_2 ... G_{n-1}$

e_n : input offset voltage

ε_n : parasitic clock error pulse of the nth stage