Design of Low Power Low Noise Operational Amplifier

A Thesis Submitted in partial fulfillment of the
Requirements for the award of degree of

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in
VLSI Design & CAD

Submitted by
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June - 2009.

CERTIFICATE

I hereby certify that the work which is being presented in the thesis entitled, **"Design of Low Power Low Noise Operational Amplifier"**, in partial fulfillment of the requirements for the award of degree of **Master of Technology in VLSI Design and CAD** at **Thapar University**, Patiala, is an authentic record of my own work carried out under the supervision of **Ms. Alpana Agarwal, Assistant Professor** and refers other researcher's work which are duly listed in the reference section.

The matter embodied in this thesis has not been submitted for the award of any other degree of this or any other university.

Date: 15/July/09

(ANILESH)

This is to certify that the above statement made by the candidate is correct and true to the best of my knowledge.

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Date: **ANILESH**

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ABSTRACT

The modern electronics industry is witnessing the dominance of miniaturization in every sphere of electronics and communications forming the backbone of medical electronics, mobile communications, computers, state-of-art processors etc. All efforts eventually converge on decreasing the power consumption entailed by ever shrinking size of the circuits enabling the portable gadgets. Designing high performance analog circuits is becoming increasingly challenging with the persistent trend towards reduced supply voltages .The main building block in an analog circuit is the operational amplifier. The main characteristics under consideration are high gain, high PSRR, low offset voltage, high output swing. At reduced supply voltages, in addition to output swing, noise and power are other two very important parameters.

Noise limits the minimum signal level that a circuit can process with acceptable quality. Today's analog designers constantly deal with the problem of noise because it trades with power dissipation, speed and linearity. Real circuits, of course, are never immune from small," random" fluctuations in voltage and current levels.

In digital circuits noise is defined as any deviation of a signal from its nominal value in those subintervals of time when it should otherwise be stable. In analog circuits noise is defined as fluctuations which may result from such causes as variations in the DC power supply, shifting values of parameters due to processing and temperature variation.

In the present work a **Low Power Low Noise Operational Amplifier** has been designed. PMOS input transistors and weak inversion topology is used for low power and low noise. PMOS transistors as an input stage driver transistor reduce the flicker noise and subthreshold operation reduces the power and noise both.
This opamp is designed using *TSMC 0.35* μm technology with a supply voltage of 3.3V. The value of the load capacitance is taken as 5 *pF*. The *power dissipation* of the op amp is 31.26 μW with *bandwidth* (f_{3dB}) of 1.32 *KHz* . Total Input Refereed Noise comes out to be 382.68 nV/$\sqrt{Hz}$ at 1 Hz, 123.68 nV/$\sqrt{Hz}$ at 10 Hz and 30.75 nV/$\sqrt{Hz}$ at 1 KHz.

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LIST OF SYMBOLS USED IN THIS THESIS

Symbol	Quantity	Units
μ	Charge carrier mobility	cm^2/V_S
A_o	DC open-loop gain	dB
A_v	Closed loop voltage gain	dB
B	Bandwidth	Hz
C_{gs}	Gate-source capacitance	f or F
CMRR	Common-mode rejection ratio	dB
C_L	Load capacitor	f
C_{OX}	Normalized oxide capacitance	f/m^2
F	Frequency	Hz
GBW	Unity gain bandwidth	Hz
g_m	Trans-conductance	Ω^{-1}
$g_{m,n}$	Trans-conductance of n-transistor	Ω^{-1}
$g_{m,p}$	Trans-conductance of p-transistor	Ω^{-1}
$g_{m,T}$	Total trans-conductance	Ω^{-1}
ICMR	Input common mode range	dB
I_d	Drains current	A
K	Boltzmann's constant	J/K
L	Channel length	m or μm
W	Channel width	m
LVS	Layout vs. Schematic	
PSRR	Power Supply Rejection Ratio	dB
SNR	Signal-to-Noise Ratio	dB
SR	Slew rate	V/μs
V_{CM}	Common-mode input voltage	V
V_{DD}	Positive supply	V
V_{DG}	Drain to gate voltage	V
V_{DS}	Drain-source voltage	V

$V_{d,sat}$	Saturation voltage	V
V_{GS}	Gate-source voltage	V
Vsb	Source-bulk voltage	V
GND	Ground	
V_T	Threshold voltage	V
MIFG	Multi Input Floating Gate	
IRN	Input Refereed Noise	

Chapter 1

INTRODUCTION

This chapter discusses the background and motivation behind the Low Power Low Noise Operational Amplifier. This chapter also discusses the need of low power low noise amplifier and its applications.

1.1 BACKGROUND

In concern of power, a low power design has made a revolutionary change in our life style. And still people are fighting for low power and better performance. The desire for portability of electronic equipment generated a need for low power systems in battery operated products like hearing aids, implantable cardiac pacemakers, cell phones, and hand held multimedia terminals. Low power dissipation is essential for these applications to have long battery life and less weight.

In concern of noise, *noise is a concern because it sets a fundamental limit on the normal operation of all electronic circuits and systems*. Traditionally, it is stated that noise is important whenever we are dealing with weak signals. That's true, but perhaps a more appropriate statement would be that noise is important whenever the amplitudes of the processed signals are similar to those of the existing noise. Clearly, if we refer exclusively to the intrinsic noise, only very weak signals risk loosing their information content in a noisy environment. The information carried by signals with high amplitudes is not corrupted.

A large demand of low power low noise amplifier has been seen in bio-medical instruments. Bio-medical instruments which are interfacing with the humans, animals and plants require low noise. Since these instruments deal with the small signals, noise becomes very important in this case. Low power is also required in these systems for the portability and long life, it means with a small battery it can work for a long time. Most of biopotential signals are of very low amplitude that is the amplitude of electrocardiography (ECG) signal is around tens of μV to several mV, and the electroencephalography (EEG) signal is at μV level [1]. Thus noise becomes very important for the systems which record these types of signals.

1.2 MOTIVATION

The design of analog circuits itself has evolved together with the technology and the performance requirements. As the device dimension shrink, the supply voltage of integrated circuits drops, and the analog and digital circuits are fabricated on one chip, many design issues arise that were unimportant only few decade ago. In design of analog circuits not only the gain and speed are important but also power dissipation, supply Voltage, linearity, noise and maximum voltage swing. Further the input and output impedances determine how the circuit interact with preceding and subsequent stages. In practice most of these parameters trade with each other, making the design multidimensional optimization problem.

Noise limits the minimum signal level that a circuit can process with acceptable quality. Today analog designers constantly deal with the problem of noise because it trades with power dissipation, speed, and linearity. Real circuits, of course, are never immune from small," random" fluctuations in voltage and current levels.

So in this thesis a two stage opamp is designed which provides both low power and low noise.

1.3 APPLICATIONS

The low power and low noise opamp is the most important device for applications in biomedical field.

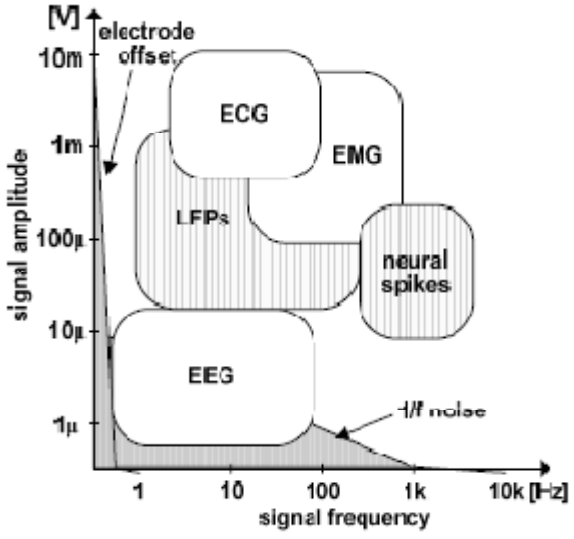


Figure 1.1 Amplitudes and frequencies of biopotential signals [1]

Amplitudes and frequencies of the bio-potential signals are shown in the figure 1.1. In all animals and some plants information about motion, perception, etc. are transmitted with electrical signals. Such signals are routinely recorded as an electroencephalogram (EEG), electrocardiogram (ECG) and electromyogram (EMG) waves. Also the activity of human brain and heart are recorded through the electrical signals. These signals have very low amplitude therefore instruments recording these types of signal uses low power low noise amplifier.

1.4 REQUIRED SPECIFICATIONS

Table 1.1 shows the required specifications according to the application [1] - [6].

Table 1.1 Required specifications for the Design

Parameters	Required Value
DC open loop gain	≥ 40 dB
Input refereed noise	≤ 5 μV
Power Dissipation	≤ 100 μV
f_{-3dB} frequency	≤ 1 KHz
CMRR	≥ 60 dB
PSRR	≥ 60 dB
Phase margin	≥50°

1.5 THESIS ORGANISATION

Following the introduction the chapter 2 provides an overview of opamp parameters and Noise in MOS.

Chapter 3 presents the various type of topology for low noise and low power dissipation.

Chapter 4 presents the design steps of low power low noise amplifier. It also contains the simulation results of design.

Chapter 5 presents Layout and Design match report. It also contains the post layout simulation results.

Chapter 6 is the concluding chapter in which design is analysed for further improvements.

Chapter 2

OP AMPS PARAMETERS AND NOISE IN MOS

Operational amplifiers (opamps) are an integral part of many analog and mixed signal systems. Opamps with vastly different levels of complexity are used to realize functions ranging from dc bias generation to high speed amplification or filtering.

This chapter discusses about ideal opamp, basic opamp structure and its parameters such as gain bandwidth product, common mode rejection ratio, power supply rejection ratio, noise *etc.* in detail.

2.1 IDEAL OPAMP

Ideally opamp is differential amplifier with two inputs and one output, infinite gain, infinite input resistance so that no loading effect can occur and zero output resistance.

The Thevenin amplifier model is shown in figure 2.1 below, showing standard opamp notation. It amplifies the voltage difference, $V_d = V_p - V_n$, on the input port and produces a voltage, V_o, on the output port that is referenced to ground.

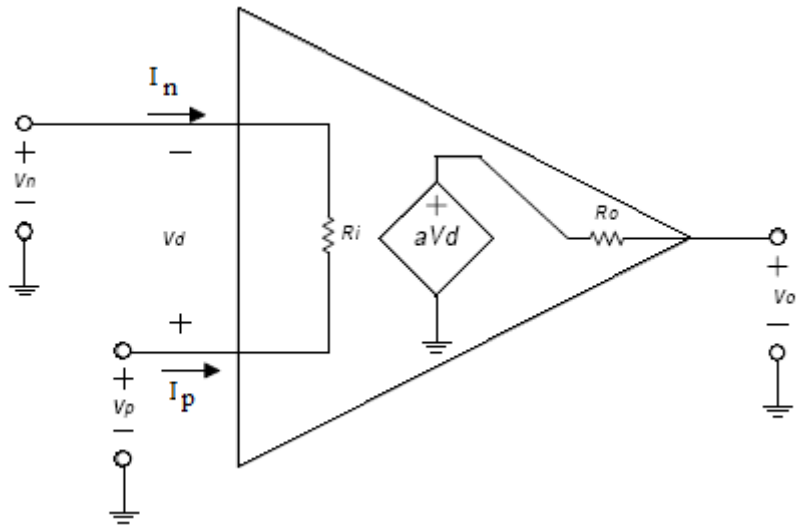


Figure 2.1 Standard opamp notation

The ideal opamp model was derived to simplify circuit calculations and is commonly used by engineers in first order approximation calculations. The ideal model makes three simplifying assumptions:

- Gain is infinite $A_v = \infty$
- Input Resistance is infinite $R_i = \infty$
- Output Resistance is zero $R_o = 0$

Applying these assumptions to the figure 2.1, results in the ideal opamp model shown in figure 2.2.

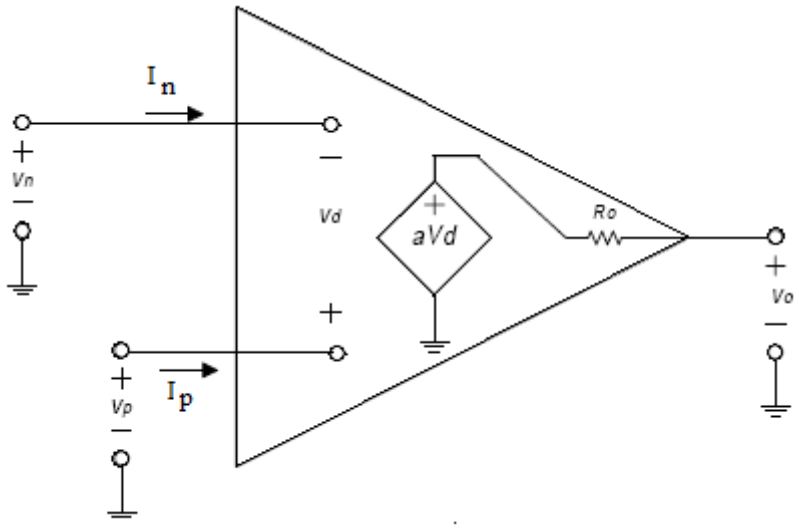


Figure 2.2 Ideal opamp model

Other simplifications can be derived using the ideal opamp model

- $In = Ip = 0$

Because $R_i = \infty$ we assume $I_n = I_p = 0$. There is no loading effect at the input.

- $V_o = A_v \times V_d$

Because $R_o = 0$ there is no loading effect at the output.

- $V_d = 0$

If the opamp is in linear operation, V_o must be a finite voltage. By definition $V_o = A_v \times V_d$. Rearranging, $V_d = V_0 / Av$. Since $A_v = \infty$, $V_d = V_o / \infty = 0$. This is the basis of the virtual short concept.

- Common mode gain = 0

The ideal voltage source driving the output port depends only on the voltage difference across its input port. It rejects any voltage common to V_n and V_p.

- Bandwidth = ∞
- Slew Rate = ∞

There are no changes in performance over time, temperature, humidity, power supply variations, etc.

2.2 BASIC OPERATIONAL AMPLIFIER

We can define operational amplifier as a "high-gain differential amplifier". By *high* we mean a value that is adequate for the application, typically in the range of 10^1 to 10^5. Since opamps are usually employed to implement feedback system, their open loop gain is chosen according to the precision required of the closed loop circuit.

Up to two decades ago, most opamps were designed to serve as "general-purpose" building blocks, satisfying the requirement of many different applications. In contrast, today's opamp design proceeds with the recognition that the trade-offs between the parameters eventually require a multi-dimensional compromise in the overall implementation, making it necessary to know the *adequate* value that must be achieved for each parameter [7].

Opamps can have one or more number of stages and thus can be classified according to stages in opamp. Simple single stage opamps are telescopic and folded cascade opamp.

Telescopic opamp is basically a differential amplifier with cascade load using PMOS and cascade NMOS driver transistors. It is also known as Cascode opamp. Figure 2.3 shows cascode opamp and figure 2.4 shows folded cascode opamp. The related details are discussed in opamp topologies.

In one stage opamps the small signal current produced by the input pair, directly flows through the output impedance therefore the gain of the topologies is limited to the product of the input pair transconductance and the output impedance. Cascading of such stages increases gain but at the cost of output voltage swing. To provide adequate gain and output swing two stage opamp are used in which the first stage provides the high gain and second stage provides large voltage swing. In two-stage opamp, figure 2.5, the second stage is typically configured as a simple common-source stage so as to allow maximum output swings.

To achieve higher gain first stage can incorporate cascode devices. Cascading of each stage adds one pole to open loop transfer function, making it difficult to guarantee stability in feedback system using such an opamp. Thus opamps having more than two stages are rarely used [7].

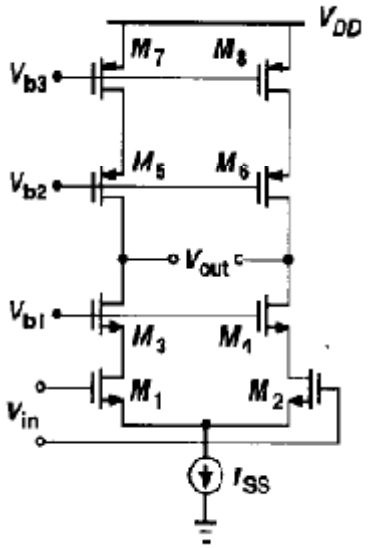


Figure 2.3 Cascode opamp

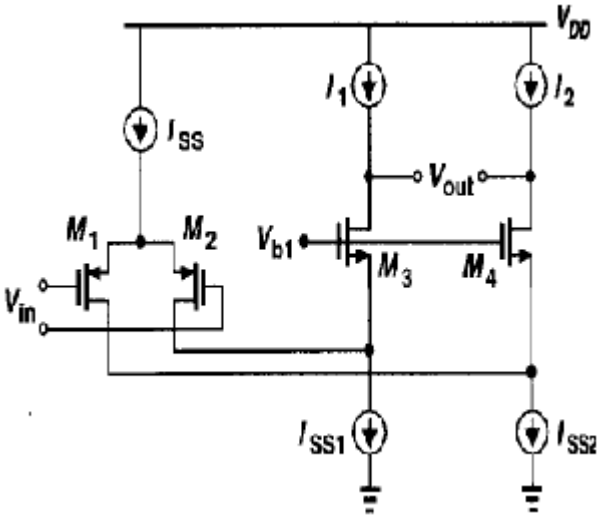


Fig 2.4 Folded Cascode opamp

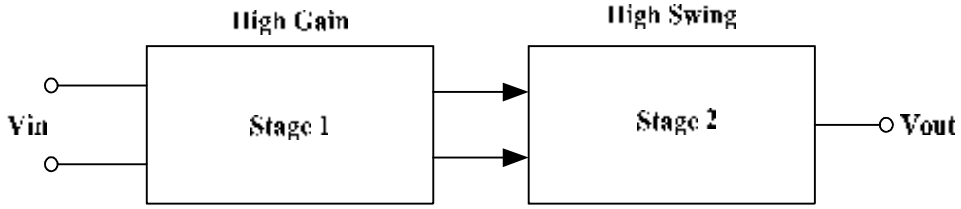


Figure 2.5 Two stage opamp

2.3 OPAMP PERFORMANCE PARAMETERS

Large signal voltage amplification, ***Av:*** The open loop gain of an opamp determines the precision of the feedback system employing the opamp. The required gain can be adjusted according to the application. Trading with the parameters such as speed and output voltage swings, the minimum required gain must therefore be known. A high open loop gain is also necessary to suppress nonlinearity.

Av is the ratio of the peak-to-peak output voltage swing to the change in input voltage required to drive the output.

$$A_v = \frac{V_{o(p-p)}}{V_{in}} \tag{2.1}$$

Differential voltage Amplification, A_{VD}: The ratio of the change in the output to the change in differential input voltage producing it with the common-mode input voltage held constant.

$$A_{vd} = \left.\frac{\Delta V_o}{\Delta V_{in}}\right|_{Vincm\ ,const} \tag{2.2}$$

Unity gain bandwidth, *UGB:* The range of frequencies within which the open-loop voltage amplification is greater that unity.UGB is shown in figure 2.6.

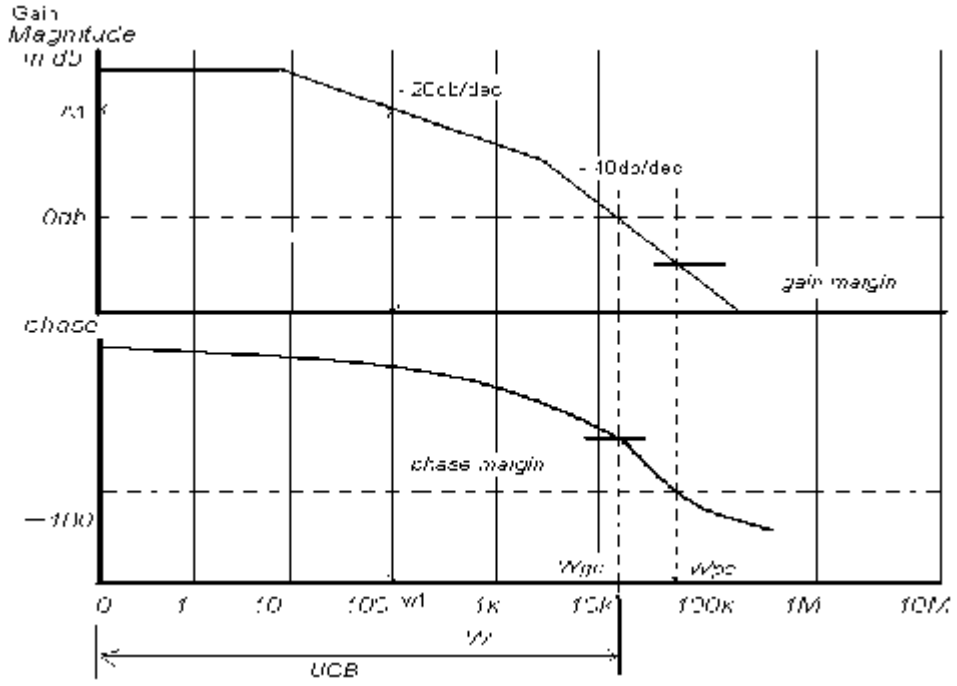


Figure 2.6 Showing Unity Gain Bandwidth (UGB), Gain Margin (GM), Phase Margin (PM)

Gain bandwidth product, *GBW*: The product of the open-loop voltage amplification and the frequency at which it is measured. From figure 2.6, Gain bandwidth product is

$$GBW = A_1 \times \omega_1 \tag{2.3}$$

Gain margin, *GM*: The reciprocal of the open-loop voltage amplification at the lowest frequency at which the open-loop phase shift is such that the output is in phase with the inverting input.

Phase margin, *PM*: The absolute value of the open-loop phase shift between the output and the inverting input at the frequency at which the modulus of the open-loopamplification is unity. Gain and phase margins are measures of stability for a feedback system, though often times only phase margin is used rather than both. Based the magnitude response of the loop gain, $|Av|$, gain margin is the difference between unity and $|Av\ (W_{180°})|$ where $W_{180°}$ is the frequency at which the loop gain phase, is -180°, called as Phase crossover frequency. Phase margin is the phase difference between phase of $Av\ (W_{0dB})$ and -180° where W_{0dB} is the frequency at which $|Av|$ is unity, called unity gain frequency. Gain and phase margins are illustrated in figure 2.6.

Maximum-output swing Bandwidth, *BOM*: The range of frequencies within which the maximum output voltage swing is above a specified value.

Common-mode rejection ratio, *CMRR:* The ratio of differential voltage amplification to common-mode voltage amplification. CMRR falls off as the frequency increases.

$$CMRR = A_{DIFF} / A_{COM} \tag{2.4}$$

Note: This is measured by determining the ratio of a change in input common-mode voltage to the resulting change in input offset voltage.

Supply voltage rejection ratio, *SVRR:* The absolute value of the ratio of the change in supply voltages to the change in input offset voltage.

$$SVRR = \Delta V_{cc} / \Delta V_{os} \tag{2.5}$$

Slew rate, *SR*: The average time rate of change of the closed-loop amplifier output voltage for a step-signal input.

$$SR = dv/dt \tag{2.6}$$

In opamps we trade power consumption for noise and speed. To increase slew rate, the bias currents within the opamp are increased.

Common-mode input voltage range, V_{ICR}: The range of common-mode input voltage that if exceeded may cause the operational amplifier to cease functioning properly.

Maximum peak output voltage swing, V_{OM}: The maximum positive or negative voltage that can be obtained without waveform clipping when quiescent dc output voltage is zero.

Maximum peak-to-peak output voltage swing, $V_{O(PP)}$: The maximum peak-to-peak voltage that can be obtained without waveform clipping when quiescent dc output voltage is zero.

Equivalent input noise voltage, V_n: The voltage of an ideal voltage source (having internal impedance equal to zero) in series with the input terminals of the device that represents the part of the internally generated noise that can properly be represented by a voltage source.

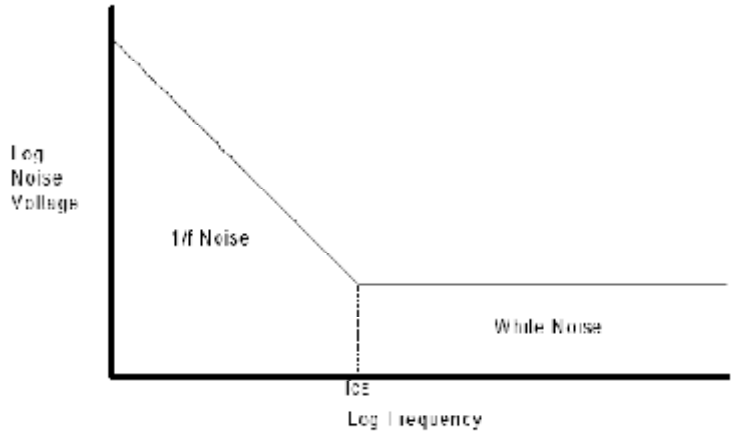


Figure 2.7 Typical Opamp Input Noise Spectrum

All opamps have associated parasitic noise sources. Noise is measured at the output of an opamp and referenced back to the input; thus, it is called equivalent input noise. The spectral density of noise in opamps has a 1/f and a white noise component. 1/f noise is inversely proportional to frequency and is usually only significant at low frequencies. White noise is spectrally flat [8].

Input resistance, R_i: The resistance between the input terminals with either input grounded.

Differential input resistance, R_{id}: The small-signal resistance between two ungrounded input terminals as shown in figure 2.8.

Output resistance, R_o: The resistance between an output terminal and ground.

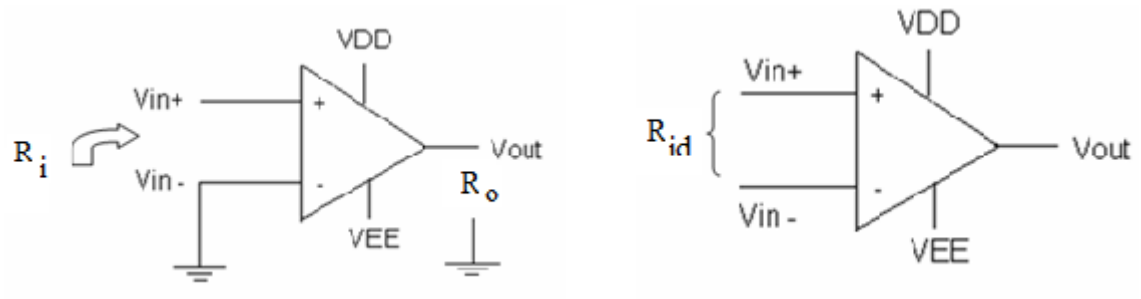


Figure 2.8 Showing R_i, R_{id} and R_o

Input offset voltage, V_{io}: The dc voltage that must be applied between the input terminals to force the quiescent dc output voltage to zero or other level, if specified.

Input offset current, I_{io}: The difference between the currents into the two input terminals with the output at the specified level. This is shown in figure 2.8.

Input bias current, I_B: The average of the currents into the two input terminals with the output at the specified level as shown in figure 2.9 [8].

$$I_B = (I_{b+} + I_{b-})/2$$
$$I_{io} = I_{b+} - I_{b-} \tag{2.7}$$

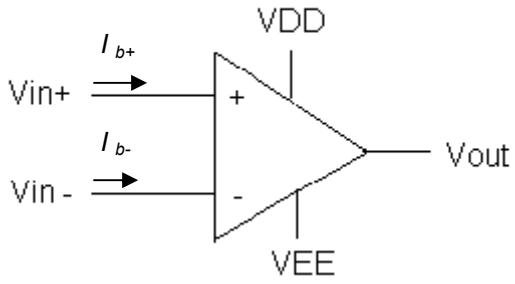


Figure 2.9 Opamp Input bias Current and Input offset Current

2.4 NOISE IN MOS

Noise is a random process that is the value of noise cannot be predicted at even if the past values are known. The phenomena which are relevant to noise generation are usually

investigated with statistical methods and/or thermodynamic concepts. To describe random processes, we use the concepts of probability, average, and correlation. Signals are either *deterministic* (if they can be modelled as specified functions of time) or *stochastic* (taking on random values in time).

A deterministic signal is normally described by its peak value, peak to peak value, mean value, and/or root-mean-square value. Since at each instant the amplitude of a random signal has a different (but non-repetitive) value, its evolution is not predictable.

Because of its very nature, the peak value is no longer a characteristic of the random signal, therefore we use the probability density function (PDF). This quantity offers a statistical description of the random signal in terms of its amplitude probability distribution over time.

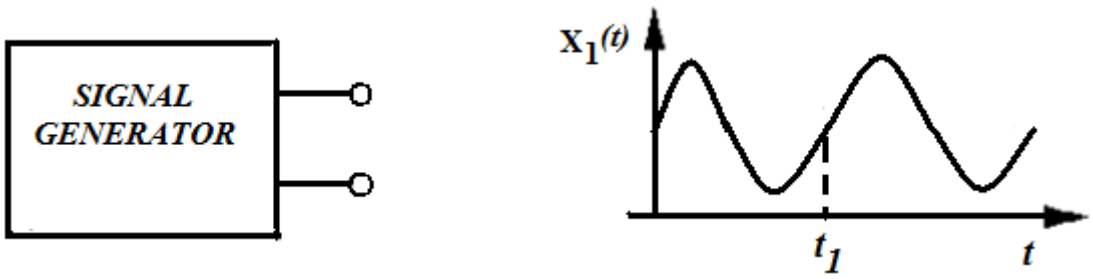


Figure 2.10 (a) Output of a signal generator [7]

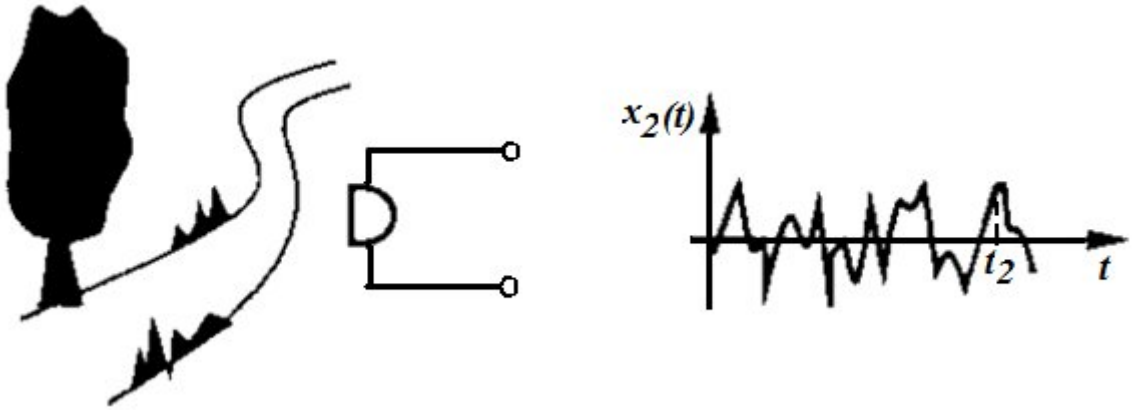


Figure 2.10 (b) Output of the sound of river [7]

Compare the output of a sine wave generator with a microphone picking up the sound of water flow in river as shown in figure 2.10. While the value of $x_1(t)$ at $t = t_1$ can be predicted from the observed waveform, the value of $x_2(t)$ at $t=t_2$ cannot. This is the

principal difference between deterministic and random process. If the instantaneous value of noise in the time domain cannot be predicted then how can we calculate noise in circuit analysis? This is done by observing the noise for a long time and using the measured results to construct a statistical model for the noise.

Therefore to calculate the noise we calculate the average power of noise which is predictable in most cases.

The average power delivered by the periodic voltage v(t) to a load resistance R_L is given by

$$P_{av} = \frac{1}{T}\int_{-T/2}^{+T/2} \frac{v^2(t)}{R_L} dt \tag{2.8}$$

where T denotes the periods.

Now for calculation of noise (random signal) the measurement is carried out for a long time since the signal is not periodic as

$$P_{av} = \lim_{T\to\infty} \frac{1}{T}\int_{-T/2}^{+T/2} \frac{v^2(t)}{R_L} dt \tag{2.9}$$

Figure 2.11 shows the operation on a signal, first signal is squared then the area under the resulting waveform is calculated for a long time T, and the average power is obtained by normalising the area to T.

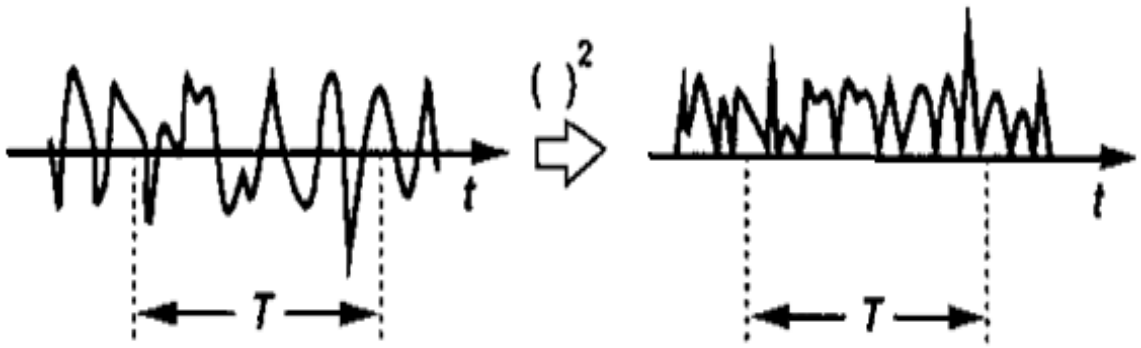


Figure 2.11 Average noise power [7]

To simplify the calculations, we write the definition of P_{av} as

$$P_{av} = \lim_{T\to\infty} \frac{1}{T}\int_{-T/2}^{+T/2} v^2(t) dt \tag{2.10}$$

where P_{av} is expressed in V^2.

Now if we know the actual power delivered to a load $R_{L,}$ then P_{av}/R_L can be calculated easily. We can also define the root-mean-square (rms) voltage for noise as $\sqrt{P_{av}}$.

2.4.1 NOISE SPECTRUM

The concept of average power becomes more versatile if defined with regard to the frequency content of noise. Therefore we define noise in term of "power spectral density" (PSD). The spectrum of PSD shows how much power the signal carries at each frequency.

The power spectral density is a real, even, nonnegative function S(f) which yields the total average power per ohm when integrated over the frequency domain. Therefore, the power spectral density is the relative distribution of signal power throughout the spectrum.

That is, as shown in figure 2.12 ,we apply x(t) to a bandpass filter with centre frequency f_1 and 1-Hz bandwidth, square the output , and calculate the average over a long time to obtain $S_x(f)$.

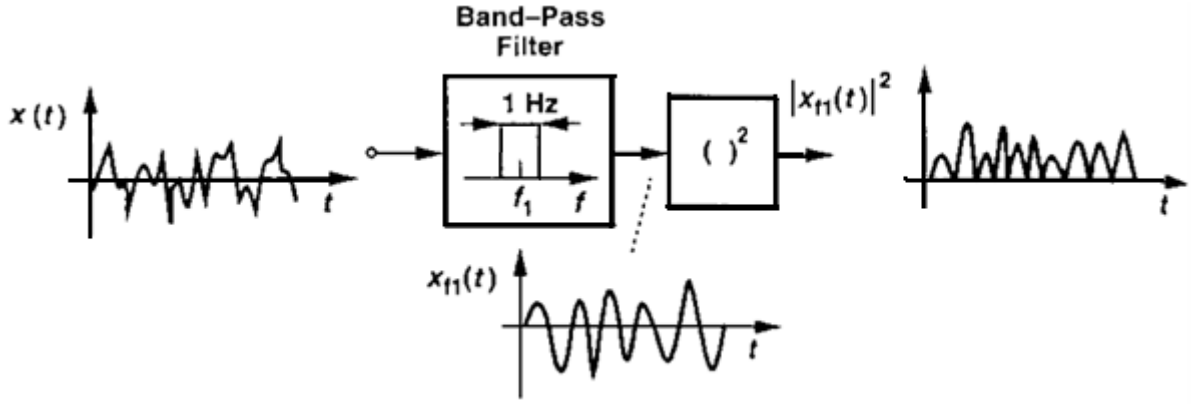


Figure 2.12 Calculation of noise spectrum [7]

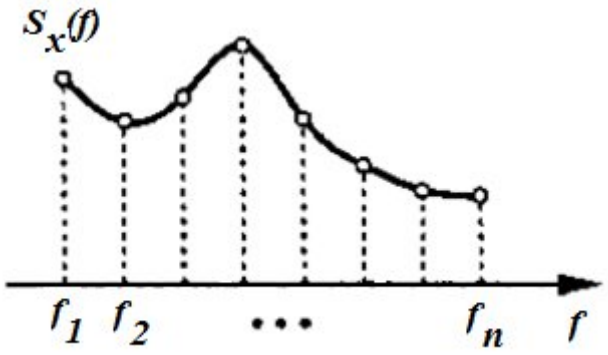


Figure 2.13 Noise spectrum [7]

Repeating the procedure with bandpass filters having different frequencies, we arrive at the overall shape of $S_x(f)$ as shown in figure 2.13. $S_x(f)$ is expressed in V^2/Hz.

An example of common type of noise is the "white spectrum" also called white noise. Shown in figure 2.14, such a PSD displays the same values at all frequencies (similar to white light).

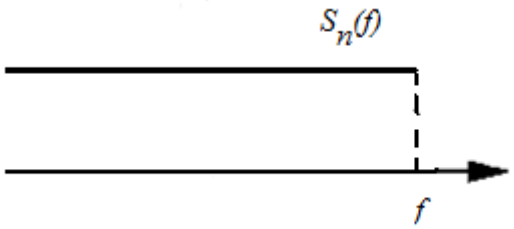


Figure 2.14 White noise spectrum [7]

We note that the white noise does not exist because the total area under the PSD is infinite. In practice, however, any noise spectrum that is flat in the band of interest is usually called white.

The PSD is a powerful tool in analysing the effect of noises in circuits, in conjunction with the following theorem.

Theorem: if a signal with spectrum $S_x(f)$ is applied to a linear time-invariant system with transfer function H(s), then the output spectrum is given by

$$S_y(f) = S_x(f)\left|H(f)\right|^2 \tag{2.11}$$

Where $H(f) = H(s = 2\pi if)$ [9]

This theorem tells that the spectrum of the signal should be shaped by the transfer function of the system as shown in the figure below.

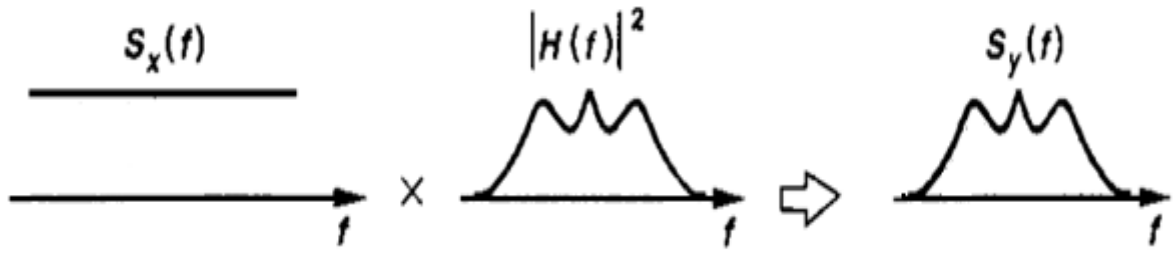
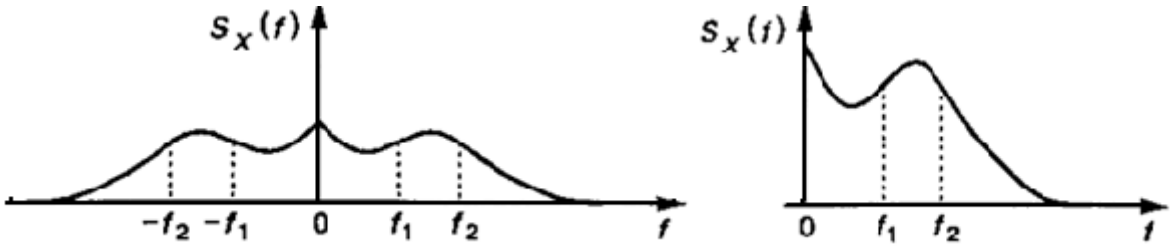


Figure 2.15 Noise shaping by a transfer function [7]

Since $S_x(f)$ is an even function of f for real x(t) [9] as shown in figure 2.16, the total power carried by x(t) in the frequency range[f1 f2] is equal to

$$P_{f1,f2} = \int_{-f2}^{-f1} S_x(f)df + \int_{+f1}^{+f2} S_x(f)df$$

$$= \int_{+f1}^{+f2} 2S_x(f)df \qquad (2.12)$$



(a) (b)

Figure 2.16 (a) Two sided spectrum (b) One sided spectrum [7]

In fact the integral in (2.12) is the quantity measured by a power meter sensing the output of a bandpass filter between f_1 and f_2. We call the representation of figure the "two sided" spectrum and that of figure the "one sided" spectrum.

In summary the spectrum shows the power carried in a small bandwidth at each frequency, revealing how fast the waveform is expected to vary in the time domain.

2.4.2 TYPES OF NOISE

In electrical circuits there are 5 common noise sources:

- Thermal noise
- Flicker noise
- Shot noise
- Burst noise
- Avalanche noise

In opamp circuits, most concern of noise is thermal and flicker noise since they affect the normal operation significantly.

(a) Thermal noise

A noise voltage called *thermal noise* is generated when thermal energy causes free electrons to move randomly in a resistive material [10]. The phenomenon was discovered by Schottky in 1928 and first measured and evaluated by Johnson in the same year. It is also referred to as *Johnson noise* [11]. Shortly after its discovery, Nyquist used a thermodynamic argument to show that the open-circuit rms thermal noise voltage across a resistor is given by

$$v(t) = \sqrt{4kTR\Delta f} \quad [10] \tag{2.13}$$

Where k is Boltzmann's constant, T is the absolute temperature, R is the resistance, and Δf is the bandwidth in hertz over which the noise is measured.

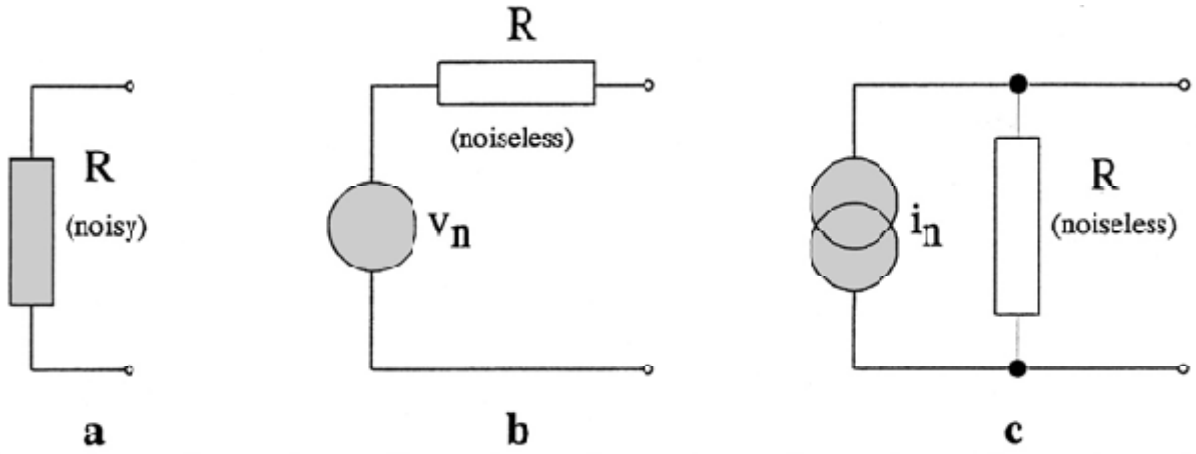


Figure 2.17 (a) Noisy resistor, (b) Thevenin equivalent circuit, (c) Norton equivalent circuit [12]

Equation (2.13) is the basis for two resistor noise models- the Thevenin model and the Norton model. These are shown in figure 2.17. The short-circuit rms thermal noise current in the Norton model of figure 2.17 (b) is given by

$$I(t) = \sqrt{\frac{4kT\Delta f}{R}} \quad [10] \tag{2.14}$$

Because noise is random, the source polarities in the figure are arbitrary. The total rms noise in a circuit is independent of the assumed polarities. Thermal noise is present in all circuit elements containing resistance. The noise is independent of the composition of the resistance. It is modeled the same way in discrete-circuit resistors and in integrated-circuit monolithic and thin-film resistors [13].

A carbon composition resistor generates the same amount of thermal noise as a metal film resistor of the same value. However, an additional noise component called flicker noise may be present in the carbon composition resistor. It results from the variable contact between the carbon particles of the resistive material. This noise is present only when a direct current flows in the resistor. Equation (2.13) shows that thermal noise voltage is proportional to the square root of the product of the absolute temperature, the resistance value, and (to the highest measurable frequencies) the bandwidth over which the noise is measured. For a fixed temperature, the thermal noise voltage in a circuit can be reduced by minimizing the resistance and the bandwidth. Further reduction can only be obtained by operating the circuit at lower temperatures.

The power in thermal noise is proportional to the square of V_t which is independent of frequency for a fixed bandwidth and is given by

$$P_{av} = 4kT\Delta f \tag{2.15}$$

The power between 100 and 200 Hz is the same as it is between 10100 and 10200 Hz. Such noise is said to have a *uniform or flat* power distribution and is called *white noise* up to100 THz**.** Its spectrum is shown in the figure (2.18). It is called this by analogy to white light which also has a flat power distribution in the optical band. Spectral power density for thermal voltage noise is given as

$$S_v(f) = 4kTR \qquad f \geq 0 \tag{2.16}$$

and for thermal current noise is given as

$$S_v(f) = 4kT / R \qquad f \geq 0 \tag{2.17}$$

MOSFET also exhibit thermal noise. The most significant source of thermal noise in MOS is the noise generated in the channel.

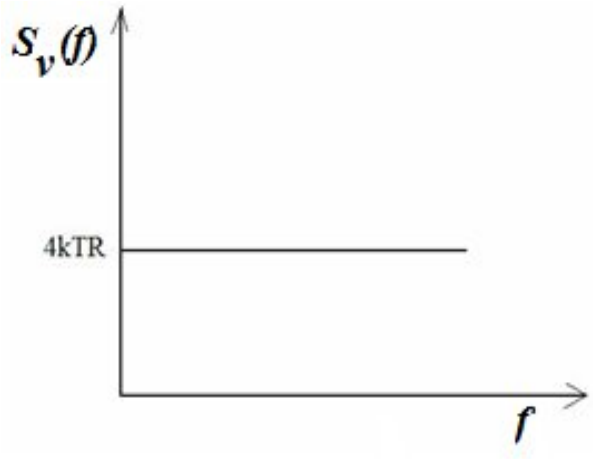


Figure 2.18 Thermal noise of a resistor [7]

It can be proved [13] that for long channel MOS devices operating in saturation region thermal noise is modeled by the current source connected between the drain and source terminal.

Its spectral density is given as

$$S_v(f) = 4kT\gamma g_m \tag{2.18}$$

where constant is equal to 2/3 for long channel transistor and have a larger value for submicron MOSFET.

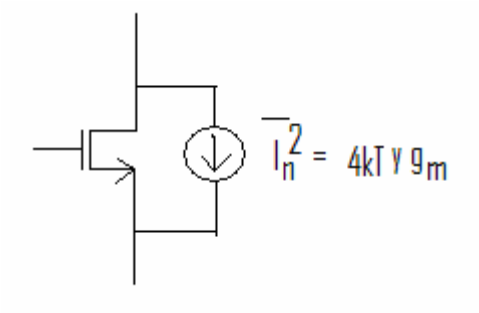


Figure 2.19 Thermal noise of a MOSFET [7]

The ohmic section of MOSFET also contributes thermal noise. The gate, source and drain material have resistivity so produces thermal noise. For a wide transistor source and drain resistance are negligible and only gate resistance exist. It can be proved that gate resistance is equal to Rg/3. [7]

Where Is This Noise Important? Thermal noise is generated only in *dissipative* systems (for instance a purely reactive device does not generate thermal noise). Therefore, it is associated with all resistors and lightly doped semiconductor layers.

(b) Flicker noise

The imperfect contact between two conducting materials causes the conductivity to fluctuate in the presence of a dc current. This phenomenon generates what is called *flicker noise* or *contact noise.* It occurs in any device where two conductors are joined together, that is, the contacts of switches, potentiometers, relays, etc. In resistors, it is caused by the variable contact between particles of the resistive material and is called *excess noise* [14]. Metal film resistors generate the least excess noise, carbon composition resistors generate the most, with carbon film resistors lying between the two. Flicker noise in BJT's occurs in the base bias current. In FET's, it occurs in the drain bias current. Flicker noise is modeled by a voltage source in series with the gate and spectral density is given by

$$S_v(f) = \frac{K}{C_{ox}WL}\frac{\Delta f}{f} \tag{2.19}$$

where K is a process dependent constant.

The noise spectral density is inversely proportional to the frequency as shown in the figure. Because of this, flicker noise is commonly referred to as l/f *noise***,** read *"one-over-f noise."* Because it increases at low frequencies, it is also referred to as *low-frequency noise***.** Another name that is sometimes used is *pink noise* [l0]. This name comes from the optical analog of pink light which has a power density that increases at the longer wavelengths, i.e., at the lower frequencies.

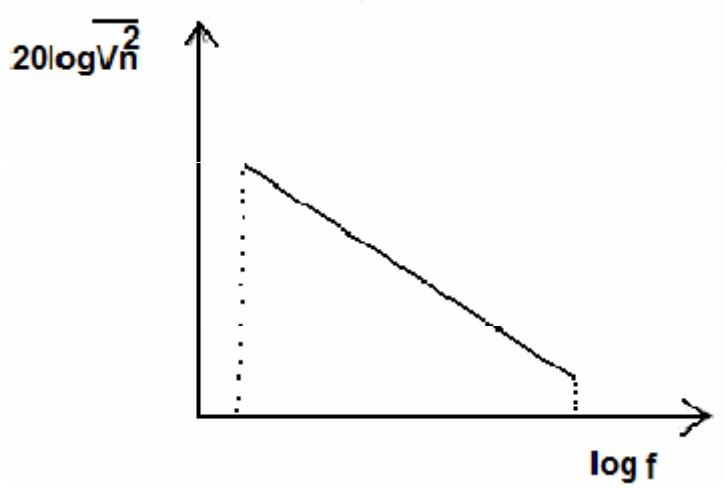


Figure 2.20 Flicker noise spectrum [10]

In order to quantify the significance of the 1/f noise with respect to thermal noise for a given device, we plot both spectral densities on the same axes. Called the 1/f noise corner frequency, the intersection point serves as a measure of what part of the band is mostly corrupted by flicker noise as shown in figure 2.21.

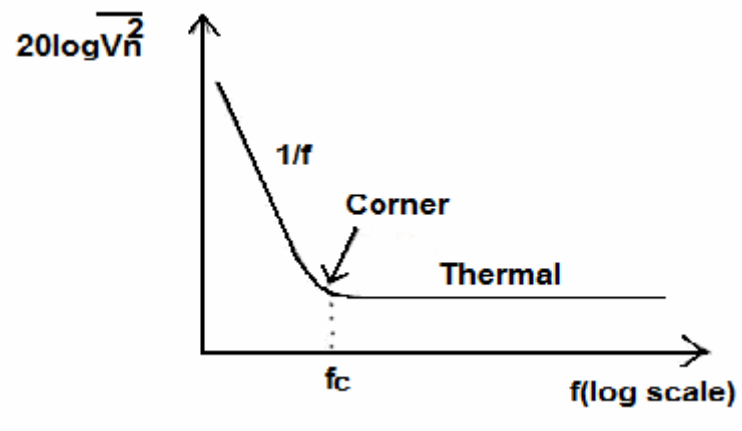


Figure 2.21 Flicker noise corner frequency [10]

The 1/f noise corner, f_c of the output current is determined as

$$4kT(\frac{2}{3}g_m) = \frac{K}{WLC_{ox}}\frac{1}{f}g_m^2$$

$$f_c = \frac{K}{WLC_{ox}}g_m\frac{3}{8kT} \tag{2.20}$$

This result implies that f_c generally depends on device dimension and bias current. Flicker noise is also found in carbon composition resistors where it is often referred to as excess noise because it appears in addition to the thermal noise.

In electronic devices, flicker noise is always conditioned by the existence of a DC current in a discontinuous medium. It is assumed to be due either to defects affecting the semiconductor lattice (including unwanted impurity atoms), or to interactions between charge carriers and the surface energy states of the semiconductor [15].

Imperfect contacts (such as those between granules of carbon in carbon resistors) can also generate 1/f noise. In this case the 1/f noise is equivalently called "excess noise," since it adds to the thermal noise of the resistor.

Flicker Noise in MOSFET. The low frequency noise is caused primarily by fluctuation of the number of inversion layer carriers as they are trapped and detrapped to and from traps located in the oxide. But these fluctuations can also induce fluctuations in the channel mobility of the remaining carriers in the channel since the traps act as Coulombic scattering sites when they capture a carrier. Recently, a new approach to carrier trapping-detrapping noise, which avoids the over simplified assumptions of the original McWhorter model, has been reported [16]. It can be concluded that the physical picture for the origin of noise in ordinary MOSFETs transistors, which accounts for both carrier number and mobility fluctuations. Typically, the drain current exhibits fluctuations with a 1/f spectrum. This is due to fluctuations in the population of charge carriers in the channel, a consequence of carrier trapping in the surface states situated at the SiO2–Si interface. Van der Ziel has established that for a MOSFET device the surface-state density at the Fermi level is the only parameter that influences 1/f noise. Hence, the only way to reduce flicker noise significantly is to lower the surface state density in the vicinity of the Fermi level.

He has shown that 1/f noise increases with decreasing temperature, since the density of surface states increases toward the conduction band. Thus, reduction of noise is achieved not only by channel length/area variation but also by optimized processing steps.

In saturation region oxide trap density is process dependent and lower for pmos transistor. Oxide trap density for nmos is weakly dependent on the gate bias while for pmos increases with the gate bias. Therefore working in saturation region it is advisable to have low gate bias for 1/f noise reduction. [17]

In subthreshold region the input refereed noise is lower because of the low gate bias therefore best noise performance it is good to bias the transistor in this region. [17]

Where Is This Noise Important? The more heterogeneous the structure of the device, higher the expected 1/f noise. Any inhomogeneity (in the lattice structure or materials) as well as contamination during processing, poor ohmic contacts, *etc*. can increase the flicker noise. Flicker noise is low in devices with homogeneous structure and a significant volume of material (for instance a 1-W resistor is less noisy than a 0.25-W resistor of the same value and type). In monolithic circuits, down-scaling of devices is favourable to increasing the 1/f noise. In recent CMOS processes the corner frequency of 1/f noise tends to increase up to 1MHz.

(c) Shot noise

The physical origin of shot noise is the discrete nature of charge carriers. It is generated when a current flows across a potential barrier [18]. It is caused by the random fluctuation of the current about its average value and occurs in vacuum tubes and in semiconductor devices. In vacuum tubes, it is generated by the random emission of electrons from the cathode. In semiconductors, it is generated by the random diffusion of holes and electrons through a p-n junction and by the random generation and recombination of hole-electron pairs.

The shot noise generated by a device is modeled by a parallel noise current source. The rms shot-noise current in the frequency band Δf is given by

$$I_{sh} = \sqrt{2qI\Delta f} \tag{2.21}$$

where ***q*** is the electronic charge and *I* is the dc current flowing through the device. This equation was derived by Shottky in 1928 and is known as the *Shottky formula***.**

For a fixed bandwidth, the noise current is independent of frequency so that shot noise has a flat power distribution, i.e., it is white noise.

Where Is This Noise Important? Shot noise is always generated in photomultipliers and all vacuum devices (where electrons move on ballistic trajectories), as well as in junction diodes. Shot noise effects are better perceived in reverse-biased diodes (or in forward-biased junctions operating at very low currents). Shot noise is always associated with

charge carriers crossing a potential barrier. In many situations (particularly in a forward-biased diode), shot noise is "smoothed" by the space charge and the transit time of carriers. Shot noise effects are stronger when the average current through the device is very low.

(d) Burst noise

Burst noise is caused by a metallic impurity in a p-n junction. Its onset is associated with contamination by heavy metallic atoms during processing, or to crystallographic damage of regions close to junctions. It seems that the appearance and disappearance of bursts is associated with single-trap activity in a region with few free carriers (like the depletion region of the emitter junction). Such devices usually have small dimensions and are subject to high fields and current densities. Because it is caused by a manufacturing defect, it is minimized by improved fabrication processes. When burst noise is amplified and reproduced by a loudspeaker, it sounds like corn popping. For this reason, it is also called *popcorn noise***.** Historically, Montgomery (1952) was the first to note that some germanium NPN transistors (all fabricated in the same run) exhibit popcorn noise, especially when previously subjected to high bias voltages.

Where Is This Noise Important? Progress in manufacturing technology has almost completely eliminated burst noise (in large devices). It is still present in submicron bipolar or MOS transistors with lattice structure damage in sensitive areas.

(e) Avalanche noise

The physical origin of this noise is the process of carrier multiplication due to impact ionization in a reverse-biased PN junction. Avalanche noise is created when a pn junction is operated in the reverse breakdown mode. Under the influence of a strong reverse electric field within the junction's depletion region, electrons have enough kinetic energy that, when they collide with the atoms of the crystal lattice, additional electron-hole pairs are formed. These collisions are purely random and produce random current pulses similar to shot noise, but much more intense. When electrons and holes in the depletion region of a reversed-biased junction acquire enough energy to cause the avalanche effect, a random series of large noise spikes will be generated. The magnitude of the noise is difficult to predict due to its dependence on the materials.

Because the zener breakdown in a pn junction causes avalanche noise, it is an issue with opamp designs that include zener diodes. The best way of eliminating avalanche noise is to redesign a circuit to use no zener diodes.

Where Is This Noise Important? Avalanche noise mainly affects reverse-biased diodes operating at more than 8 V.

2.4.3 REPRESENTATION OF NOISE IN A CIRCUIT

Consider a general circuit shown in the figure 2.22. Thereafter model the possible noise sources and see the overall effect of noise. A general approach to calculate the noise is, set all the input to zero and calculate the total noise at the output due to the noise sources present in the circuit.

This is the output referred noise. This noise does not provide a fair comparison of performance of different circuit because it depends upon the gain. Consider a common source stage followed by a noiseless amplifier having gain A_v. The output noise is the product of and output noise. For only output noise, if the gain increases the output noise also increases which is a wrong result since a higher gain also provides a higher signal to noise ratio.

To overcome this situation, consider the input referred noise of circuit. Figure 2.23 shows the idea to model the input referred noise by combining the all noise sources in the circuit by a single source $V^2_{n,\,in}$ at the input.

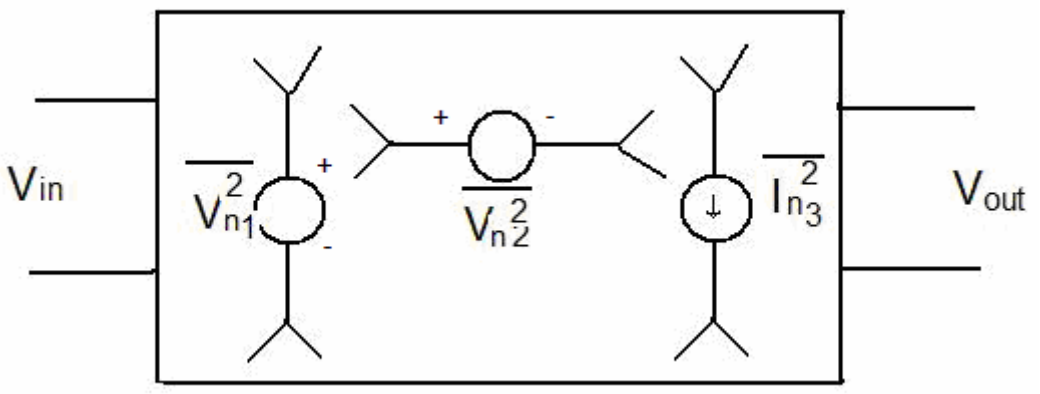


Figure 2.22 Noise sources in a circuit [7]

Now the input referred noise is given by the output noise voltage divided by the gain as

$$V^2_{n,\,in} = V^2_{n,\,out} / A_v^2 \qquad (2.22)$$

In this situation the input noise and signal both are multiplied by the gain when processed by the circuit. It represents how much the input signal is corrupted by the noise. Due to

this reason input referred noise provides a fair comparison of different circuit. The input referred noise is a fictitious quantity. it cannot be measured at the input of the circuit.

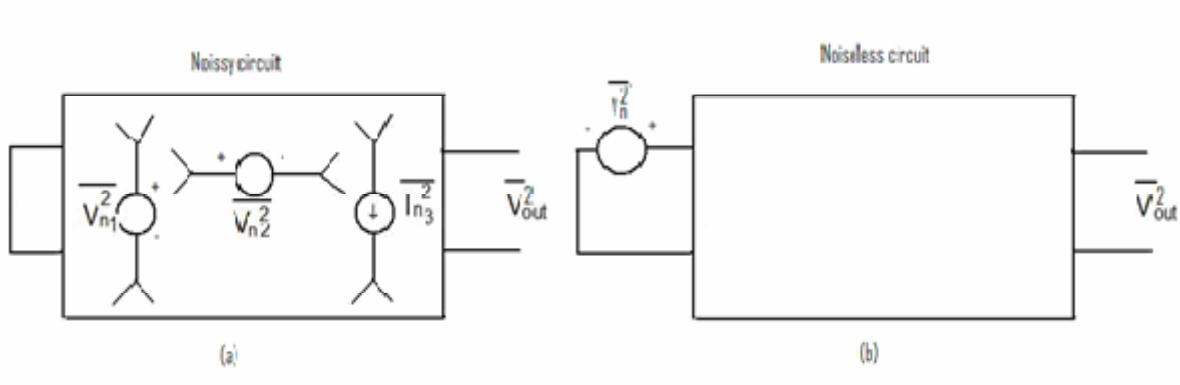


Figure 2.23 determination of input refereed noise voltage [7]

All the circuit cannot be modelled by a single voltage source in series with the input. To understand it considers the circuit shown in the figure 2.24 (a), which has finite input impedance and finite source impedance.

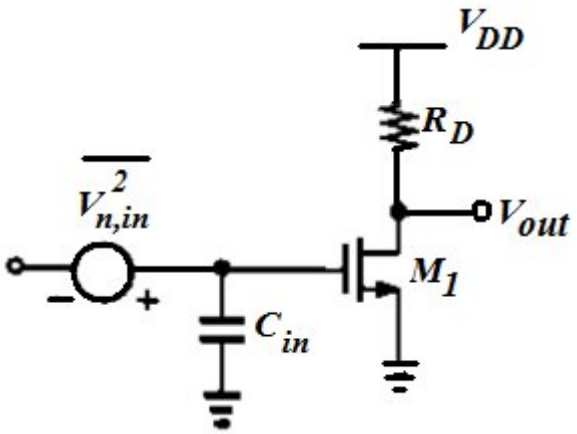


Figure 2.24 (a) CS stage with input capacitance [7]

The input referred noise voltage (due to thermal noise) for this circuit is given as

$$V_{n,in}^2 = \left(\frac{8}{3g_m} kT + \frac{4kT}{g_m^2 R_D} \right) \tag{2.23}$$

Now if the preceding stage is modelled by a Thevenin equivalent having an inductive output impedance as shown in the figure 2.24 (b).

If the L_1 increases, the voltage is divided between the L_1 and C_{in}. The effect of , is vanishes at the gate of M_1 and also at the output when L_1 approaches infinity, but this is incorrect because the output noise of the circuit is independent of L_1 and C_{in} and is equal to

$$V_{n,out}^2 = \left(\frac{8}{3}kTg_m + \frac{4kT}{R_D}\right)R_D^2 \tag{2.24}$$

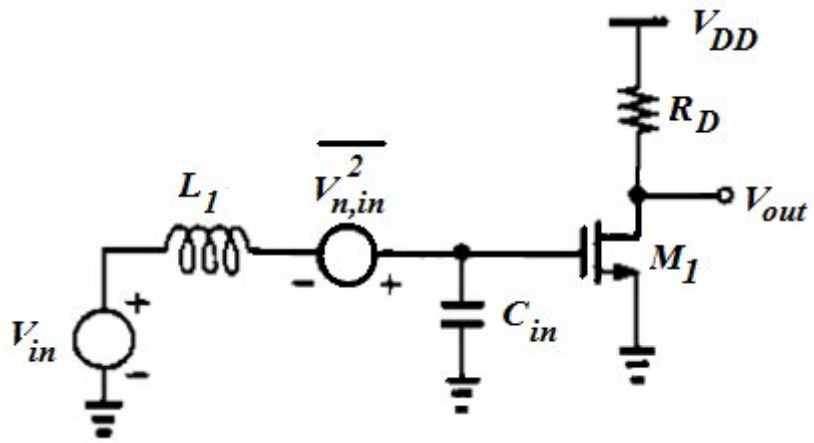


Figure 2.24 (b) CS stage stimulated by a finite source impedance [7]

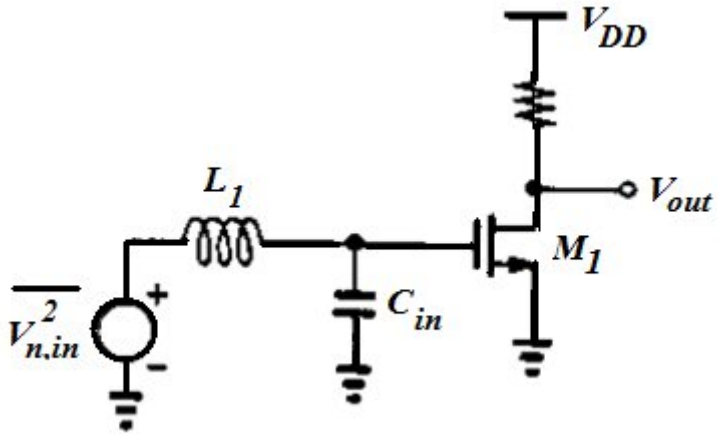


Figure 2.24 (c) Effect of single noise source [7]

To solve this problem we model the input referred noise by both a series voltage source and a parallel current source as shown in the figure 2.25.

Now if the output impedance of the preceding stage have large value it reduces the effect of but the noise current still flow through finite impedance producing the noise at the

input. Thus the both voltage and current sources are necessary to represent the noise of any linear two port circuit [19]. This model is valid for any source impedance.

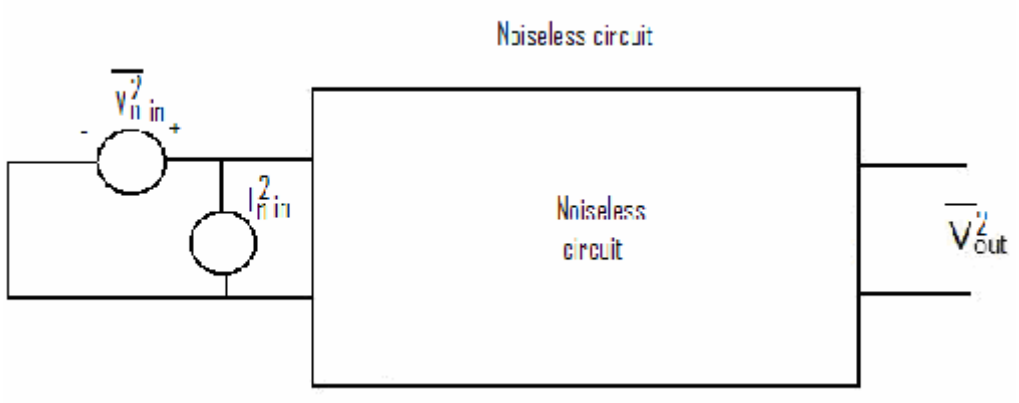


Figure 2.25 Representation of noise by voltage and current sources [7]

Now consider the two cases zero and infinite impedance as shown in the figure 2.26. When zero source impedance, noise current flow through noise voltage source and has no effect on the output and due to the noise voltage source only.

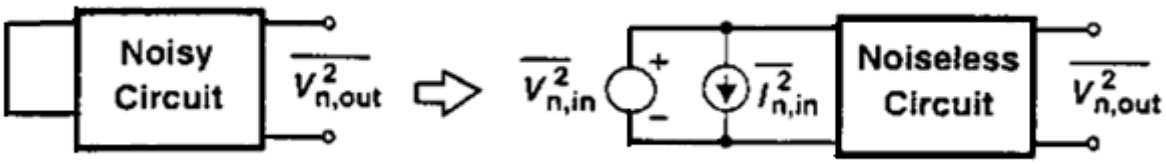


Figure 2.26 (a) Calculation of input referred noise voltage [7]

When infinite source impedance the input noise source has no effect and output noise is due to the current source only.

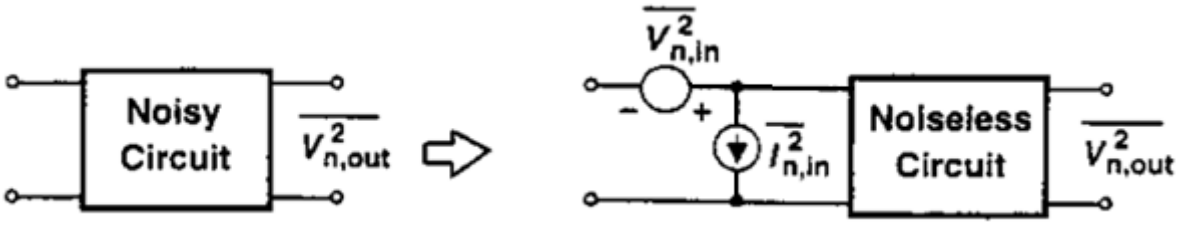


Figure 2.26 (b) Calculation of input referred noise current [7]

Chapter 3

LITERATURE SURVEY

3.1 LOW POWER OPAMP TOPOLOGIES

The operational amplifier, which is the most versatile and important building block in any analog circuits have several topologies. Among them one or combination of topologies are selected depending on the required specification.

Different topologies or techniques used to design a required opamp are listed below.

1. Cascode Opamp Topology
2. Folded Cascode Opamp Topology
3. Fully Differential Opamp Topology
4. Gain boosted Opamp Topology
5. Current feedback Opamp Topology
6. Rail to Rail Opamp Topology
7. Bulk Driven MOSFET Topology
8. Floating Gate MOSFET Topology
9. Charge Pump assisted Topology
10. Sub-threshold / Weak inversion Topology

Among these topologies some are used for low power, low voltage opamp design. Those topologies are

- Bulk Driven MOSFET Topology
- Floating Gate MOSFET Topology
- Sub-threshold / Weak inversion Topology

These topologies are discussed further one by one.

3.1.1 BULK DRIVEN MOSFET TOPOLOGY

- **Basics of Bulk Driven MOSFET**

Digital circuitry benefits from technology scaling and reduced supply voltages which result in increased speed and reduced power consumption, respectively. With analog circuits the situation is different because reducing the supply voltage reduces also the dynamic range and speed. To maintain the same performance, more power is consumed. Another problem with reduced supply voltage is that many of the conventional analog

circuit topologies will not operate anymore due to the fact that as the maximum allowable supply voltage scales down with the minimum feature size, the same amount of reduction doesn't happen with the threshold voltages of MOS-transistors because this would lead to increased leakage currents. To overcome the threshold voltage problem a bulk-driven MOSFET or a floating-gate MOSFET can be utilized [20].

Earlier designers have often taken granted that MOSFET is actually a three terminal device. The bulk terminal is usually ignored or simply connected to ground or V_{dd} or tied to the source terminal. Recently, however, it has been discovered that the bulk terminal may be used as a small signal input in completely novel family of amplifiers that are very well suited to an ultra-low supply environment [21].

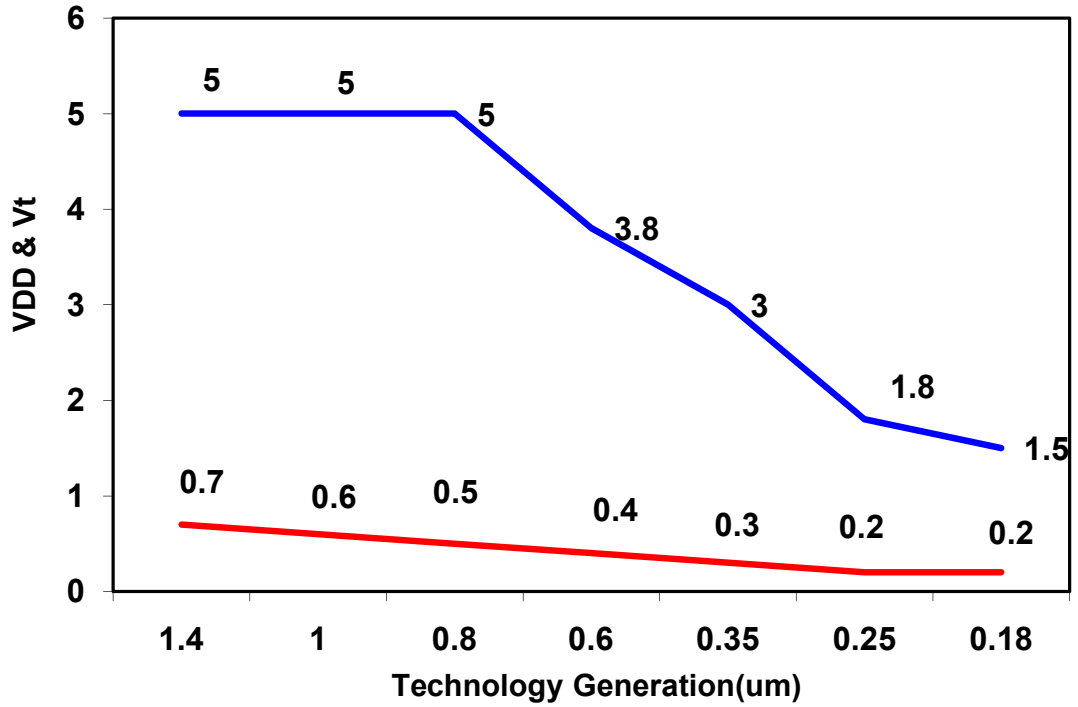


Figure 3.1 Plot of V_T Verses Technology [22]

By scaling supply voltage, V_T can be scaled to great extend, but with the scaling of supply voltage, threshold voltage should be scale down to obtain desired combination of speed and power. The fact is that V_T does not scale down with V_{DD} in new submicron technology. The plot of Supply voltage and V_T Vs Technology is shown in figure 3.1.

Bulk terminal has given extra degree of freedom to designers, by connecting voltage to the bulk terminal V_T can be controlled as per requirement. MOS transistor undergoes 'body effect' when bulk voltage is not equal to source voltage. V_b not equal to V_s, this is

considered as bad effect as it increases V_T and lowers voltage headroom. On the other hand effect of forward bias source to bulk potential is quite desirable which lowers V_T.
The relation of V_T and V_{bs} is given by following equation

$$V_T = V_{T0} \pm \gamma(\sqrt{2|\phi_F| - V_{BS}} - \sqrt{2|\phi_F|}) \quad (3.1)$$

Figure 3.2 shows Threshold Voltage adjustment with V_{BS}. As shown in graph Vt reduces for forward bias source-bulk potential and shows body effect for reverse connection.

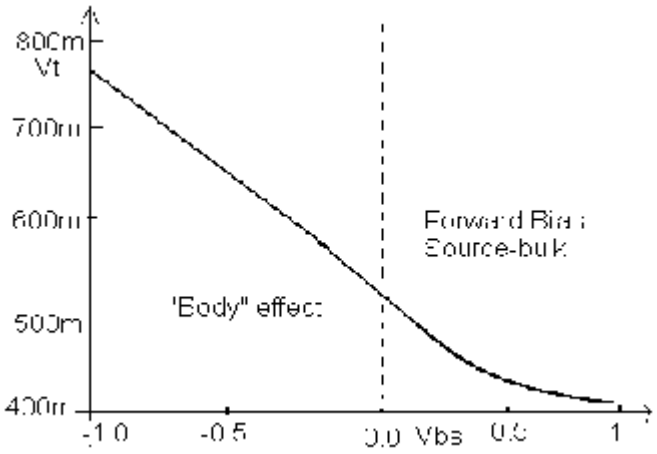


Figure 3.2 Threshold Voltage adjustment with V_{BS} [22]

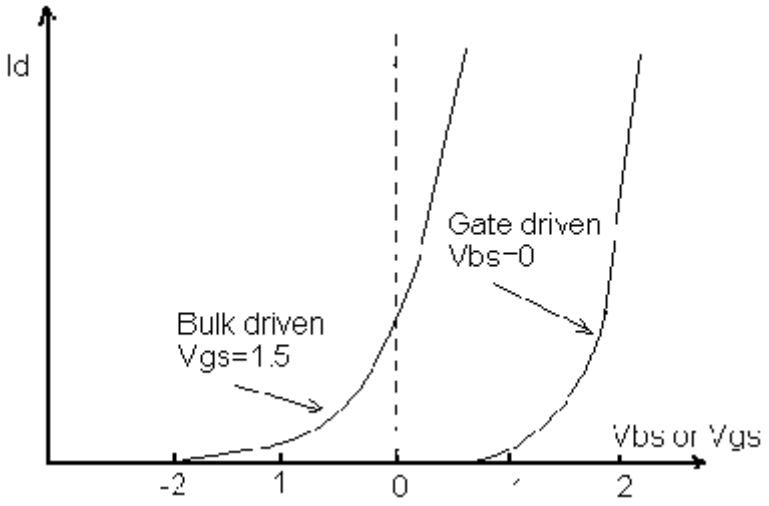


Figure 3.3 Drain Current of Bulk driven and Gate driven MOSFETS [23]

Figure 3.3 shows the drain current I_d for bulk-source driven transistor and gate-source driven transistor. From the grapg it can seen that bulk driven transistor is ON for negative, zero and positive bulk-source potential, which is same as in JFET. Thus a bulk driven transistor acts as JFET (Depletion) device.

- **Bulk Driven Circuit**

The operation of the bulk-driven MOSFET is of depletion type. The gate-source voltage is set to a value sufficient to turn on the transistor i.e. the transistor is ON even though the bulk voltage is zero (same as in JFET, JFET remains ON even if its gate potential is zero). Bulk terminal acts as 'gate' of JFET. The input voltage is then applied to the bulk-terminal (i.e. well) of the transistor to modulate the threshold voltage Vt of the device and thus the current flow through the transistor. The advantage of a bulk-driven device over a gate-driven device is that the threshold voltage limitation disappears and both positive and negative bias voltages (VBS) are possible. This is especially important in analog low voltage circuits where the dynamic range of the signal should be maximized with respect to the supply voltage in order to maximize the performance of the circuit [20].

In bulk driven circuits, as the MOSFET is driven by signal applied to bulk terminal, the drain current is function of transconductance, gmb and bulk-source voltage, V_{BS}. The transconductance gmb is given by [22]

$$g_{mb} = \frac{di_D}{dV_{BS}} = \frac{\gamma \times g_m}{2\sqrt{2\phi_F - V_{BS}}} \tag{3.2}$$

where $$g_{mb} = \eta g_m \tag{3.3}$$

and

$$\eta = \frac{\gamma}{2\sqrt{2\phi_F - V_{BS}}} \approx 0.2...0.4 \tag{3.4}$$

Thus as $gmb < gm$, the gain of the bulk driven amplifier is always less as compared to that off gate driven amplifier. From equation 3.4, it can be easily shown that gain of a bulk driven amplifier can exceed that of conventional gate driven common source amplifier when

$$V_{BS} \geq 2\phi_F - 0.25\gamma^2 \tag{3.5}$$

Following figure 3.4 shows a input differential stage using bulk driven MOSFETs. Gate of two NMOS are shorted and connected to supply voltage, V_{DD}. Input signal Vin1 and Vin2 are applied to the bulk inputs of NMOS M1 and M2 respectively. Note that for a n-type substrate only NMOS can be used as bulk driven MOS device, it is shown in figure 3.5.

From equation 3.4, g_{mb} is 0.2 to 0.4 times of g_m, thus effective g_m is nearly linear over common mode input range. Figure 3.6 shows gm variation for conventional differential

pair and bulk driven differential pair [9]. Bulk driven method reduces threshold voltage, the input common mode range increases in bulk driven circuits. The example of designed opamp with bulk-driven input transistors is shown in figure 3.7. Because an n-well CMOS-process has been used, the bulk-driven devices are of PMOS-type. By applying the input signal to the bulk-terminals instead of gate-terminals of the input transistors, the threshold voltage limitation disappears and a large input CMR of the opamp is achievable.

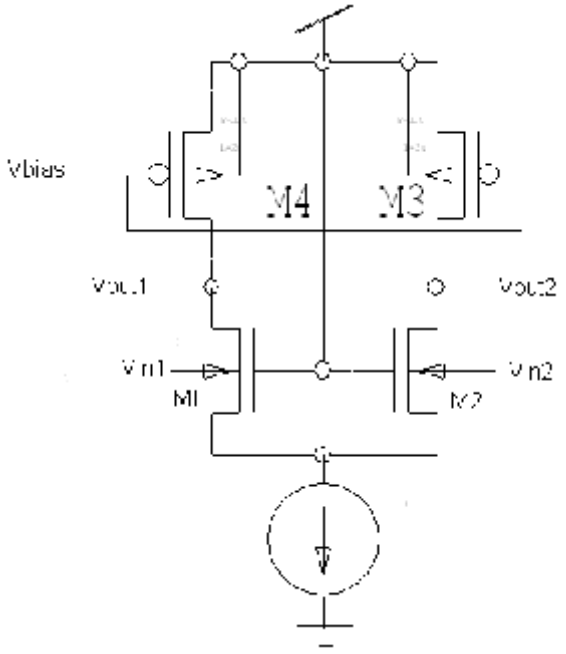


Figure 3.4 Differential input Stage using Bulk Driven NMOS transistors

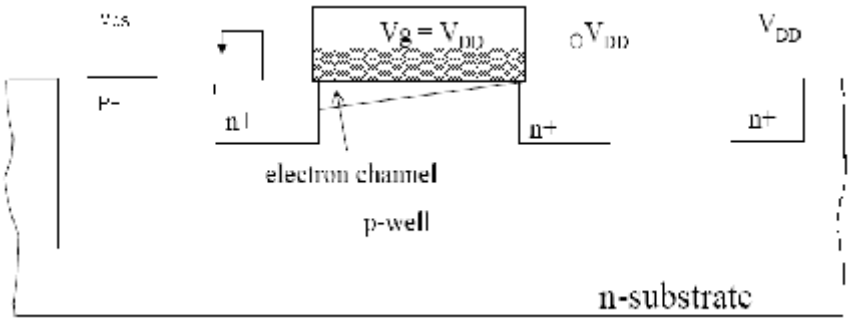


Figure 3.5 NMOS Bulk Driven MOSFETs

Another goal was to minimize current consumption and input referred noise. The noise at low frequencies is dominated by 1/ f-noise. This is minimized by choosing fairly large

values for channel width and length of the input transistors M4,5 and the channel length of the current mirror load transistors M6,7. The large channel lengths in the input stage result in a large output impedance of the input stage which increases the gain but decreases the bandwidth of the opamp.

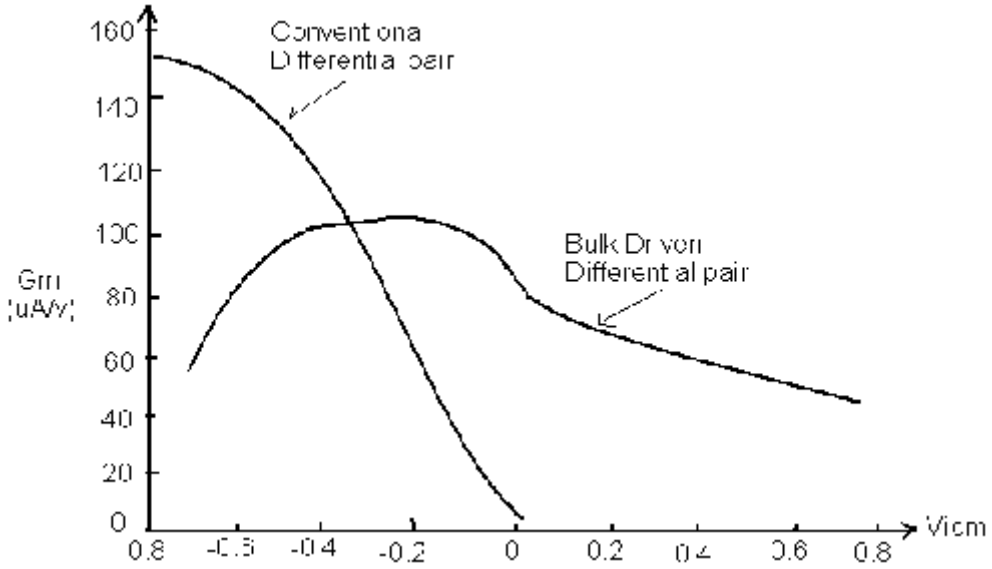


Figure 3.6 $g_m$variation for conventional differential pair and Bulk driven differential pair [22]

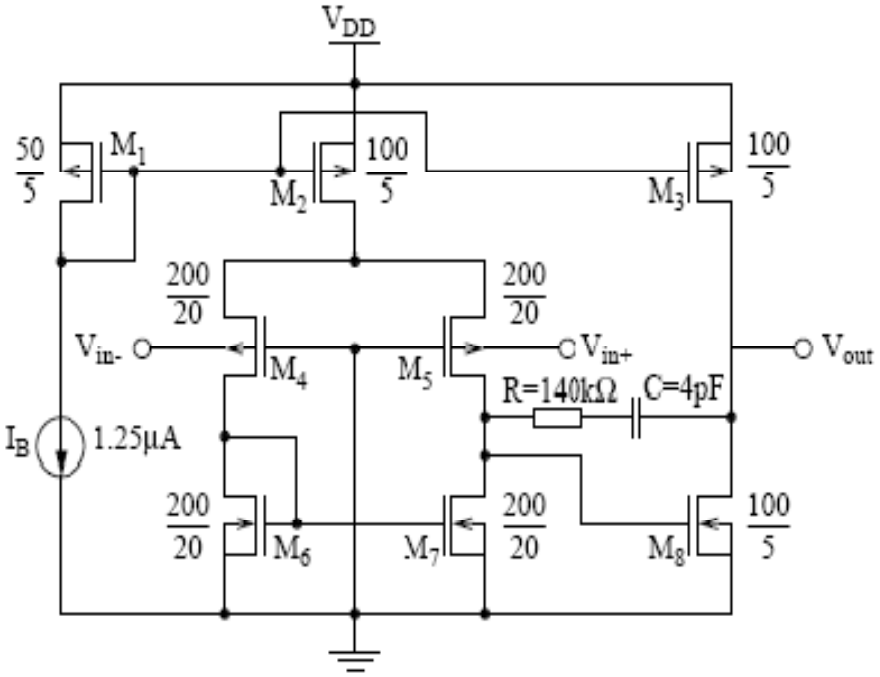


Figure 3.7 Bulk Driven Miller compensated Opamp.

Thermal noise is minimized by using an interdigitated structure in the input transistors with plenty of bulk-contacts. The aspect ratio W/L of the input transistors is designed sufficiently large to limit the maximum possible negative V_{SB} to avoid large leakage currents from source to bulk and from source to substrate (in the case where the input voltage V_B is close to negative supply rail) [20].

- **Advantages and disadvantages of Bulk driven circuits**

Advantages of Bulk Driven MOSFET circuit

- Removes the threshold voltage requirements and the device can be operated at low supply voltages. Due to depletion characteristics zero, negative, and even small positive values of bias voltage can be applied to get the desired dc currents.

- Bulk-driven MOSFETs can work even at 0.9 V (for $V_T \approx 0.8$) and we can use conventional gate to modulate the bulk-driven MOSFETs i.e. the on-off ratio of bulk driven MOSFET modulated by the gate is very large as the gate can totally shutoff the channel.
- the small-signal transconductance, g_{mb} can be larger than the MOSFET's transconductance, gm if $V_{BS} \geq .5V$. But there will be appreciable current flowing in bulk source junction under these conditions.
- Linear gm can be obtained, as g_{mb} is only 0.2 to 0.4 times of g_m
- No latch-up problem, as transistor does not conducts because of small V_{bs} voltage.

Disadvantages of Bulk Driven MOSFET

- All the MOSFETs require isolated bulk terminals.
- The capacitance of the bulk-driven MOSFET cause problems. The gate-driven MOSFET's frequency response capability is described by its transitional frequency, f_T

$$f_{Tgate\ -\ driven} \approx g_m / \left(2\pi C_{gs}\right) \tag{3.6}$$

where C_{gs} is the gate-to-source capacitance. At, frequencies beyond f_T, the device no longer provides signal gain. For the bulk-driven MOSFET

$$f_{Tbulk-driven} \approx g_{mb} /(2\pi(C_{bs} + C_{bsub})) = \eta g_m /(2\pi(C_{bs} + C_{bsub})) \tag{3.7}$$

Where η is the ratio of g_{mb} to gm and is in the range of 0.2 to 0.4, C_{bs} is the bulk-to-source capacitance, and C_{bsub} is the well-to substrate capacitance. For saturated strong inversion MOSFET operation and using some approximations the transitional frequency relation is given by

$$f_{T,bulk-driven} \approx (\eta / 3.8) f_{T,\ gate\ -\ driven} \tag{3.8}$$

- The polarity of the bulk-driven MOSFETs is process related. For P-well process, only N-channel bulk-driven MOSFETs are available, and for N-well process, only P-channel MOSFETs are available. Thus, bulk-driven MOSFETs cannot be used in CMOS structures where both N channel and P channel MOSFETs are required.
- Bulk-driven MOSFETs are fabricated in differential wells to have isolated bulk terminal and the matching between bulk-driven MOSFETs in differential wells suffers. Thus the analog circuit with tight matching between MOSFETs is difficult to fabricate [24].
- Higher noise figure (because of lower gm) [9]

$$Noise_{\ bulk\ -driven} = \frac{Noise_{\ gate\ -driven}}{\eta^2} \tag{3.9}$$

- Need separate wells, thus more expensive and bigger chip area [22]
- Another drawback of bulk driven is that as the bias voltage to the bulk changes, size of the depletion region between the bulk and substrate changes. This means that the input capacitance will now be dependent on the input bulk bias.[21]

3.1.2 FLOTING GATE TRANSISTOR OPAMP TOPOLOGY

- **Floating gate transistor**

The construction of floating gate transistor is shown in figure 3.8. Figure 3.8(a) shows the single input floating gate transistor and figure 3.8(b) shows a multi input floating gate transistor. Single input floating gate MOS transistors are widely used in digital memories as EPROMs (Erasable Programmable Read Only Memories) and EEPROMSs (Electrically Erasable Programmable Read Only Memories).Floating gate transistors are used in memories, because they can maintain charges for very long time, around 8 to 10 years. This is because of its structure. A floating gate is sandwiched between SiO2 layers. Thus the charge hold by the floating gate can not leak easily through high insulating SiO2 materials up and down. Another important application of floating gate found in Low Power Analog circuits.

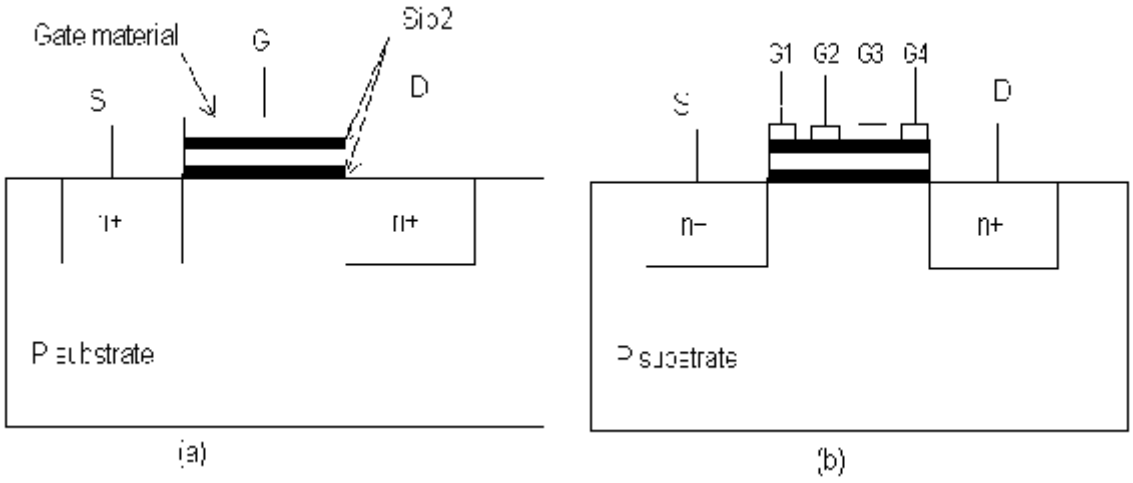


Figure 3.8 (a) Single Input Floating Gate Transistor, (b) Multi Input Floating Gate Transistor

Following figure 3.9 shows Floating Gate ideal device and practical device (in case of Analog circuits). As shown in figure 3.9 in low power analog circuits, floating gate with two input gates is used. One gate terminal is connected to V_{bias} to bias the transistor properly, whereas an input signal is applied at another one.

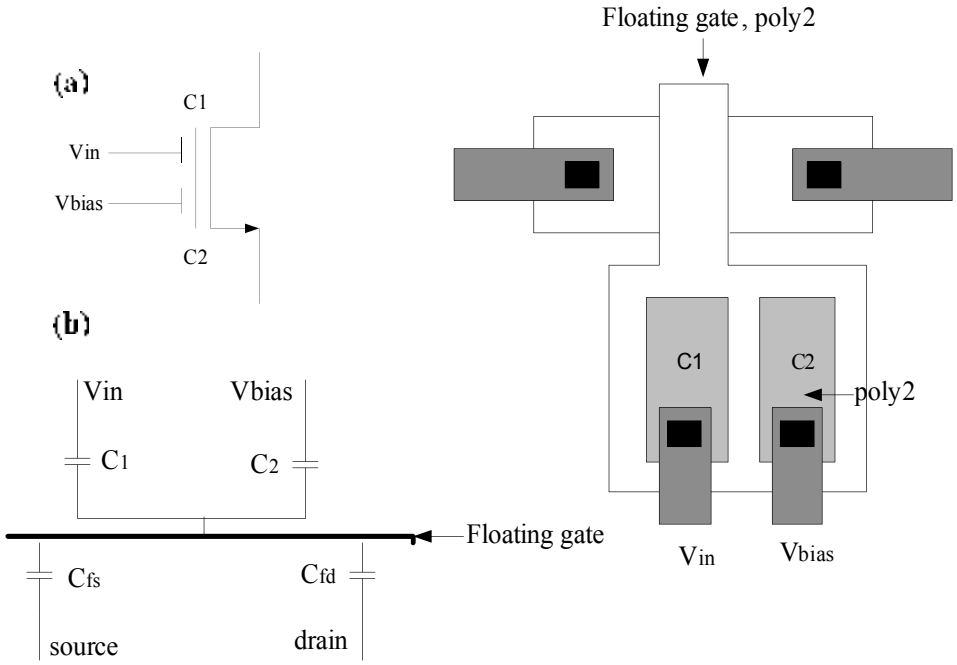


Figure 3.9 Floating Gate MOSFET, (a) Ideal Device, (b) Practical Device [25]

In a floating-gate transistor the charge on the gate of a MOSFET is controlled by two or more inputs through poly-poly capacitors between each input and the floating-gate By using one input for the signal and one for a bias voltage, the floating-gate potential can be partly set by the bias voltage. From figure 3.9 (a) the floating-gate potential V_{FGB} is

$$V_{FGB} = (C_1 V_{in} + C_2 V_{bias}) / C_1 + C_2 \tag{3.10}$$

In a floating-gate transistor the charge on the gate of a MOSFET is controlled by two or more inputs through poly-poly capacitors between each input and the floating-gate By using one input for the signal and one for a bias voltage, the floating-gate potential can be partly set by the bias voltage. From figure 3.9 (a) the floating-gate potential V_{FGB} is

$$V_{FGB} = (C_1 V_{in} + C_2 V_{bias}) / C_1 + C_2 \tag{3.10}$$

In practice floating gate MOS functioning not only depends on C1 and C2 but also on capacitors C_{fs}, C_{fd} and other parasitic node capacitances. To reduce the effect of these capacitors, value of C_1 and C_2 must be sufficiently high. The potential of the floating gate is also determined by a random charge component (Q_{FG})**.** During processing a random amount of charge accumulates on the floating-gate causing a change in its potential and in the case of a differential pair an offset since the amount of charge on the two floating-gates may be different. This charge can be removed by grounding the inputs and exposing the poly-poly capacitor edges to shortwave W-light. Shortwave W (< 290nm) photons have enough energy to enable charge transfer from the floating-gate poly layer to the other poly layer connected to one of the grounded inputs. Erasure time is proportional to the exposed edge length. The exposed area must be carefully controlled to avoid unintentional charge transfer from e.g. the substrate to the floating-gate. The area can be controlled by openings in passivation or by metal shields. In the process used for this work the strongly UV-attenuating passivation needs to be removed from the areas selected for W-exposure.

- **Multiple-Input Floating Gate MOS Transistors**

The n input control gates are capacitively coupled to the floating gate. Let's assume Q_{FG} is the net charge on the floating gate, V_{FG} is the voltage of the floating gate, and V_{Gi} is voltage of the i_{th} control gate, thus

$$V_{FG} = (Q_{FG} + C_{FGD} V_D + C_{FGS} V_S + C_{FGB} V_B + \sum_{i=1}^{n} C_{Gi} V_{Gi}) \Big/ C_{Total} \tag{3.11}$$

where $C_{Total} = C_{FGD} + C_{FGS} + C_{FGB} + \sum_{i=1}^{n} C_{Gi}$

If we do not considering the control gates, the physical structure of the floating-gate transistor is the same with conventional MOS transistor, so the I_D vs. V_{FGS} characteristics of a floating gate transistor is the same with that of a conventional MOS transistor.

Characteristics of MIFG MOS transistors

The equivalent threshold voltage seen from V_{Gi} is given by

$$V_{T,equ} = \frac{V_T - V_b k_1}{k_2} \tag{3.12}$$

which may less than V_T depending on the value of V_b, k_1 and k_2.

The effective transconductance is given by

$$g_{m,eff} = k_2 g_{m,FG} \tag{3.13}$$

where, $g_{m,FG}$ is the transconductance seen from the floating gate. Note that $g_{m,eff}$ is less than $g_{m,FG}$ by a factor of k_1.

As there is a DC and AC feedback from drain to floating gate through C_{GD}, the output impedance is less than that of an MOS transistor working in the same biasing condition. To get the output impedance of the floating gate MOS transistor, we connect all the inputs to AC ground, and apply a voltage source at the drain of the floating gate MOS transistor. We can get the following small signal circuit shown in figure 3.10.

We can easily get the output conductance is

$$g_{o,Eff} = \frac{C_{GD}}{C_{Total}} g_m + g_o \tag{3.14}$$

Thus the output resistance of floating gate transistor is low.

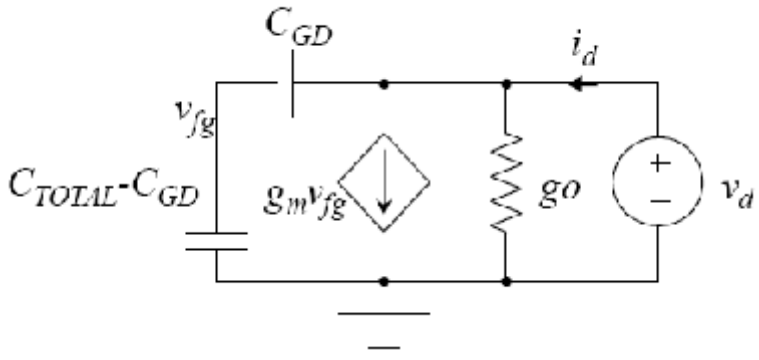


Figure 3.10 Multiple input Floating gate small signal for output conductance calculation.

- **Floating gate MOSFET Circuits**

Multiple input floating gate (MIFG) MOSFET differential pair is shown in figure 3.11 below. There are two types of MIFG differential pair, those are

1) Differential pair I (Biased by floating voltage source)
2) Differential pair II (Biased by non-floating voltage source)

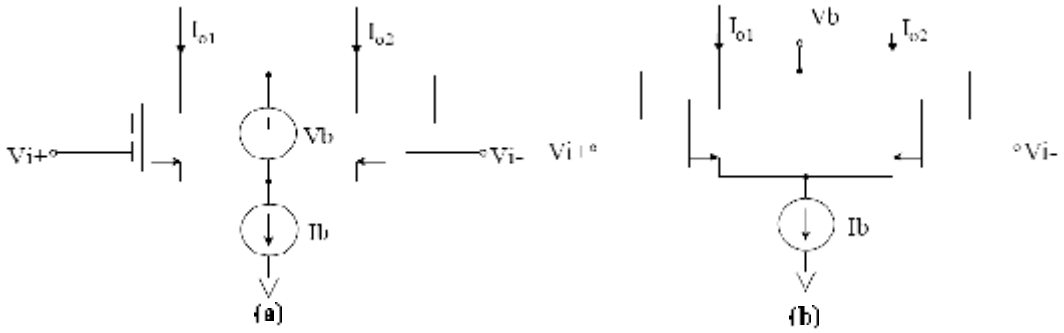


Figure 3.11 MIFG Differential pair (a) Differential pair I (Biased by floating voltage source) (b) Differential pair II (Biased by non-floating voltage source) [26].

MIFG differential pair I is equivalent to a differential pair with low VT transistors. It can not have a rail-to-rail range. And the floating voltage source may limit its common mode swing range if the floating voltage source cannot swing out of the supply rails.

The following graph in figure 3.12 is the transconductance vs. common mode input voltage of MIFG differential pair I and conventional differential pair.

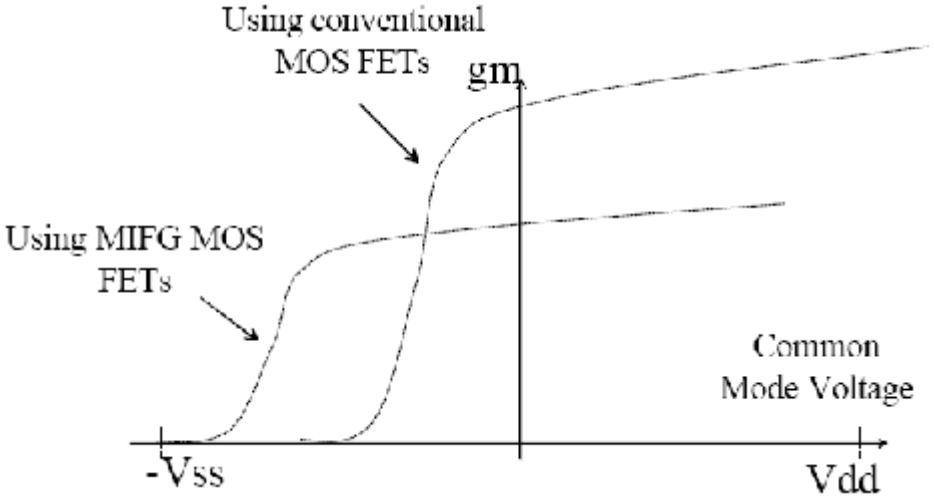


Figure 3.12 gm Vs Common mode input Voltage of MIFG differential pair and Conventional differential pair.

Because of the floating gate, gm is attenuated. The DC bias V_b introduces a DC shift in the curve below [26].Usually the floating voltage source is implemented as follows shown in figure 3.13. In (a) the floating voltage source is implemented by a diode connected MOS transistor using a biasing source I_{b2}. In (b) the floating voltage source is implemented by a common drain connected PMOS transistor biased by a current source I_{b2}.

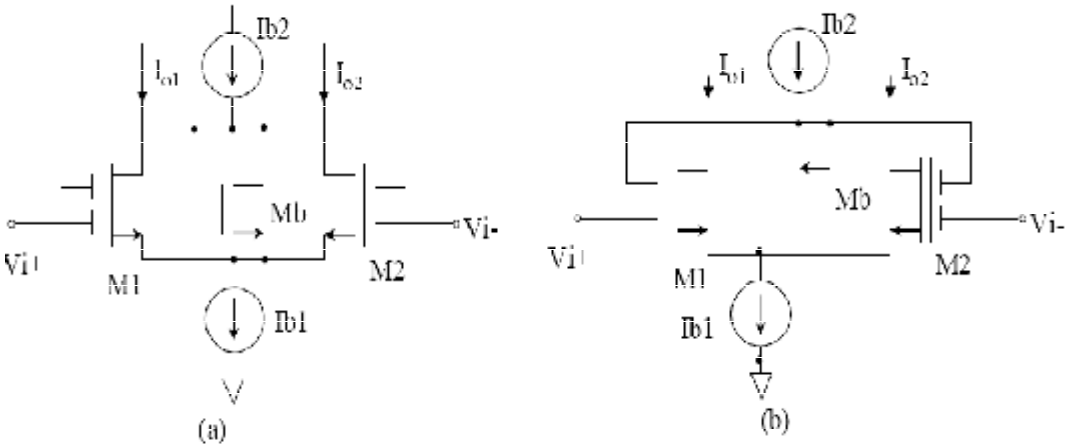


Figure 3.13 Floating Gate Differential pair with (a) Diode connected Voltage source, (b) Common drain Voltage source.

We may notice that, for both of these two circuits, when the input common mode voltage is approaching V_{DD}, I_{b2} can be driven out of saturation region, because the low resistance of diode connected Mb and current I_{b2} which is working ohmic region, the PSRR and CMRR may be degraded.

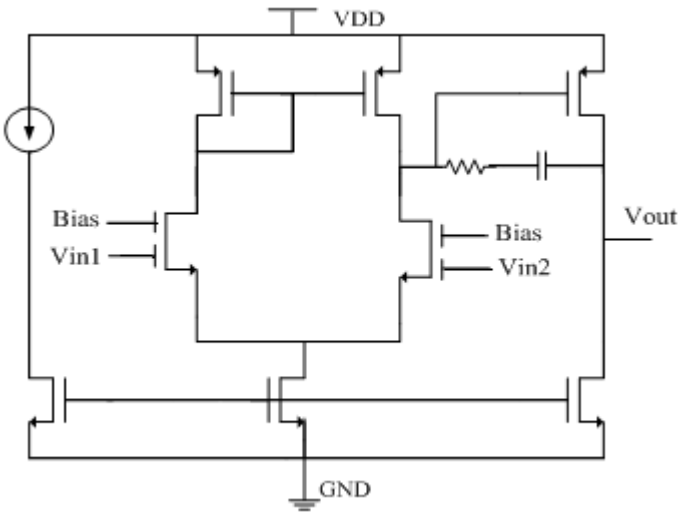


Figure 3.14 Opamp with floating gate input transistors [25]

Figure 3.14 shows a Floating gate transistor opamp. The input common mode range of an opamp can be increased with the floating-gate transistors but due to the capacitive division the input signal is attenuated which results in deterioration of gain, GBW and noise properties. Nevertheless, acceptable performance for the intended low-power biomedical applications can be achieved. The random charge on the floating-gates is a significant issue since for most analog applications it is unacceptably large. To erase this charge with UV illumination the passivation of the IC chip may need to be partially removed and the UV-exposed area must be carefully controlled to prevent unintentional charge transfers [25].

3.1.3 SUBTHRESHOLD/WEAK INVERSION OPAMP TOPOLOGY

Opamps operating in weak inversion region have become very useful because they operate not only at low power supply currents but also at low power supply voltages.

$$I_{DS} = 2KW/L[\eta kT/qe]2\exp[q(V_{GS} - V_T)/\eta kT] \tag{3.15}$$

where η lies between 1.2 and 2. Parameters q, k, V_{TN} and T represent the electronic charge, Boltzmann constant, threshold voltage of N channel MOSFET and temperature, respectively.

From this equation the transconductance can easily be derived as [27]

$$g_m = \frac{I_D}{\eta kT/q} \tag{3.16}$$

Equation 3.16 shows a linear relationship between transconductance and drain current. Furthermore, important one is transconductance is independent of device geometry [27].

Also in weak inversion the transconductance is proportional to current whereas in strong inversion the transconductance is proportional to square root of the current [28]. The relation between g_m and I_D is a square law one and gm independent of device geometry these two characteristics set the subthreshold region apart from the strong inversion region.

In equation 3.15 V_{ds} term is not included. As in strong inversion here also V_{ds} term comes with the factor λ. In weak inversion λ may not necessarily be the same as that extracted from strong inversion. The expression for output resistance in weak inversion is

$$r_o \cong \frac{1}{\lambda i_d} \tag{3.17}$$

Like the transconductance, the output resistance is also independent of device aspect ratio W/L. Since λ is a function of channel length, it is only the control parameter the designer has on the gain, $gm.r_0$, of a single stage operating in weak inversion [27].

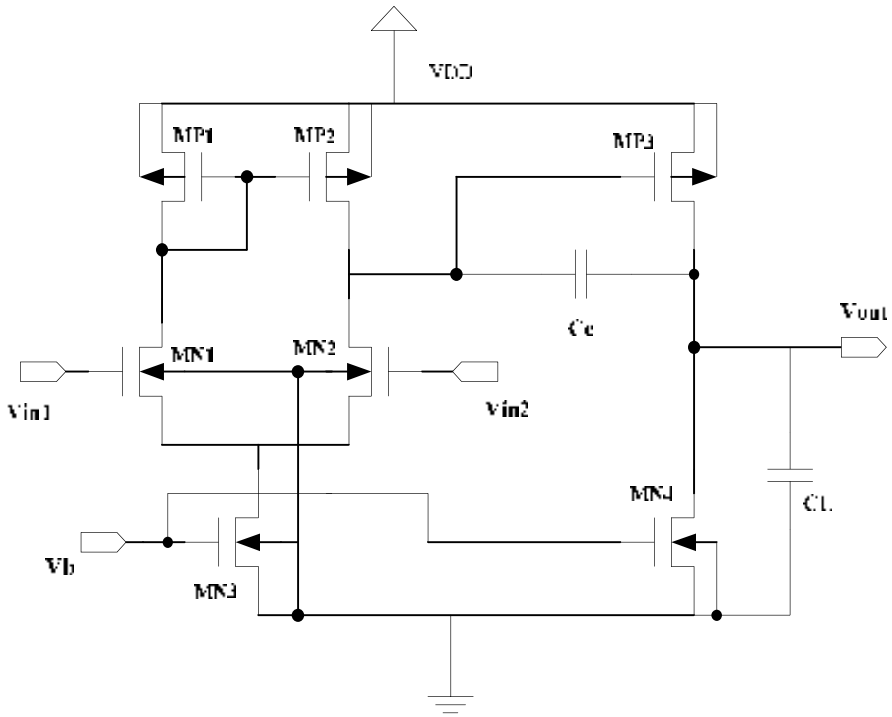


Figure 3.15 Two stage Miller Opamp operating in weak inversion

The gain bandwidth product is given by

$$GBW = \frac{I_{D1}}{\eta_1 kTC/q} \tag{3.18}$$

It is interesting to note that while the dc gain of the opamp is independent of I_D, the GB is not. This becomes a limiting factor in the dynamic performance of the opamp operating in weak inversion, because the dc current is small thus GB is small. The slew rate of this amplifier is also low.

There are several limitations of devices operating in sub-threshold region.

- Frequency response of devices is poor. As Gain bandwidth product is directly proportional to subthreshold current, which is very low and thus low GB.
- drain and source substrate currents associated with the reverse biased diffusion-substrate
- Junctions are not necessarily negligible compared to sub-threshold drain current.

- Linearity is quite poor for $V_{DS} < 3V_t$ ($V_t = kT/q$). This makes the low-voltage circuit design quite complicated.
- For obtaining higher gain conditions, the devices of larger width or low drain current are required and this limits the speed of the sub-threshold circuits [24].

In summary, the low power and low supply voltage is now prime need of portable gadgets.

Among them bulk driven topology allows rail to rail input common mode range and almost linear gm over V_{icm}. There is no latch up problem. The gain offered by this method is low also there is large leakage current for higher common mode input voltage. It takes large silicon area and thus cost is high. The input capacitance (bulk-source depletion) is input signal dependent.

The Floating Gate input topology also allows rail-to-rail input common mode voltage range, at the cost of limited low frequency capabilities, because of large input node parasitic capacitance. This gives low output resistance. Multiple input consumes more silicon area, but less as compared to that of bulk driven transistors. Extra fabrication stage is required to form floating gate structure. Thus it is costly.

Input Differential pair operating in weak inversion, is the most efficient way to achieve low power dissipation in opamp. Also the conventional MOS transistors are used in design. Thus not required any extra fabrication step and thus small area consumption and low cost as compared to other techniques. Frequency response of devices is poor. As Gain bandwidth product is directly proportional to subthreshold current, which is very low and thus low GB. For obtaining higher gain conditions, the devices of larger width or low drain current are required and this limits the speed of the sub-threshold circuits.

3.2 LOW NOISE OPAMP TOPOLOGIES

There are many methods of noise reduction used in different research papers based on different application. But here suggested techniques are the general methods of noise reduction which can be used in most applications

1. Autozero Technique
2. Chopper stabilization
3. Switched biasing
4. Subthreshold operation

3.2.1 AUTOZERO TECHNIQUE [29, 30, 31]

The basic idea of AZ is sampling the unwanted quantity (noise and offset) and then subtracting it from the instantaneous value of the contaminated signal either at the input or the output of the op-amp. This cancellation can also be done at some intermediate node between the input and the output of the op-amp, using an additional input port defined as the nulling input and identified with the letter *N* in the schematics of figure 3.16.

If the noise is constant over time (like a dc offset) it will be cancelled, as needed in a high-precision amplifier or high-resolution comparator. If the unwanted disturbance is low-frequency random noise (for example, l/f noise), it will be high-pass filtered and thus strongly reduced at low frequencies but at the cost of an increased noise floor due to aliasing of the wideband noise inherent to the sampling process. The general principle of the AZ process will first be described considering only the input referred dc offset voltage V_{OS}, and then it is extended to the input referred random noise voltage V_N.

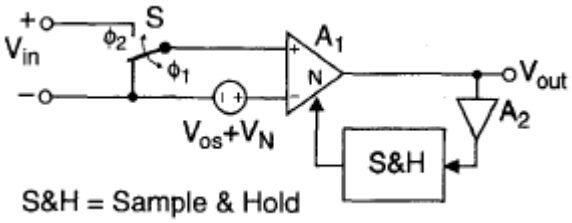


Figure 3.16 (a) Basic autozeroed stage –analog offset control stage [29]

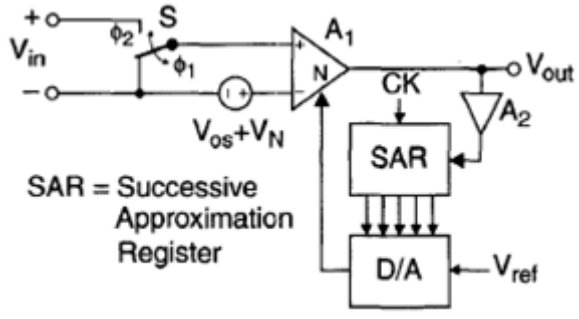


Figure 3.16 (b) Digital offset control stage [29]

The AZ process requires at least two phases: a sampling phase (Φ_1) during which the offset voltage V_{OS} and the noise voltage V_N sampled and stored, and a signal-processing

phase (Φ_2) during which the offset-free stage is available for operation. The two major categories of AZ are shown in figure 3.16. During the sampling phase (shown in figure 3.16a), the amplifier is disconnected from the signal path, its inputs are short-circuited and set to an appropriate common-mode voltage. The offset is nulled using an auxiliary nulling input port *N* by means of an appropriate feedback configuration and/or a dedicated algorithm. The control quantity x_c, is next sampled and stored, either in an analog form as a voltage using a S/H stage [figure 3.16a] or in a digital form, using for example a register [figure 3.16b]. The output V_{out} is forced to a small value in these particular configurations. The input terminals of the amplifier can afterwards be connected back to the signal source for amplification. If it is used under the same conditions as during sampling, the amplifier will ideally be free from any unwanted offset.

3.2.2 CHOPPER STABILIZATION TECHNIQUE [29, 31, 32]

Figure 3.17 describes the essential idea of the CHS technique, which combines the amplifier with two modulators at the input and output. The input signal is first frequency-shifted in the input modulator to higher frequencies, where the subsequent CMOS amplifier is free from 1/f noise, is then amplified and shifted back to its original frequency in the second modulator. In contrast to the signal, the offset and 1/f-noise of the amplifier between the modulators are only modulated once by the second modulator and translated to higher frequencies. Unlike the

CDS technique, the chopper stabilization technique does not introduce any aliasing of broadband noise, which for CHS technique causes the power spectral density in the baseband to increase proportionally to the ratio of the noise bandwidth and sampling frequency. This large energy arising from chopping frequency, which is restricting the usable signal bandwidth, requires high order filter to be removed. This is a major drawback of CHS technique and the use of it in operational amplifiers is unwilling. Apart from these, CHS and CDS are limited to use in bandwidth. These techniques make only use of the non-diminishing auto-correlation function of non-white noise to predict its actual value based on the previous one. They do not help to reduce the 1/f noise “itself”.

Basic Principle

The CHS technique was introduced about 50 years ago to realize high-precision dc gains with ac-coupled amplifiers. These were originally constructed using vacuum tubes and mechanical relay choppers. When solid-state components became available, they were

then made with modular and hybrid techniques. Now they can easily be realized on-chip by taking advantage of integrated switches. Unlike the AZ process, the CHS technique does not use sampling, but rather applies modulation to transpose the signal to a higher frequency where there is no l/f noise, and then demodulates it back to the baseband after amplification. The chopper amplification principle is illustrated in figure 3.17. Suppose that the input signal has a spectrum limited to half of the chopper frequency so no signal aliasing occurs, and that the amplifier is ideal, with no noise or offset. This input signal is multiplied by the square-wave carrier signal $m_1(t)$ with period $T = 1/f_{chop}$. After this modulation, the signal is transposed to the odd harmonic frequencies of the modulation signal. It is then amplified and demodulated back to the original band.

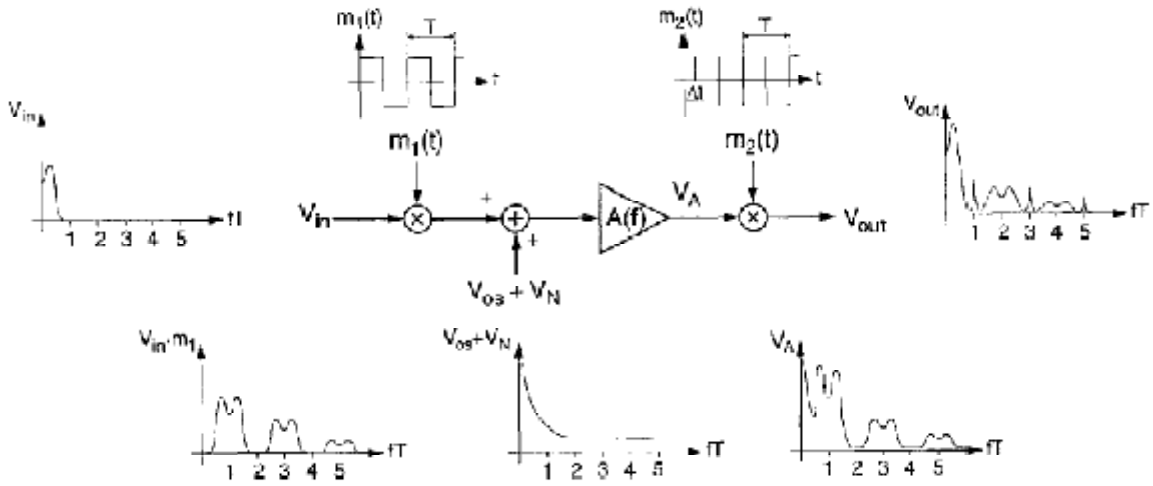


Figure 3.17 Chopper amplification principle [29]

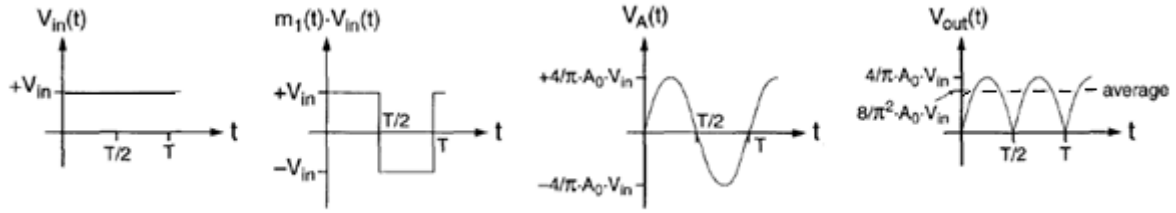


Figure 3.18 Waveform along the chopper amplifier [29]

Assuming that the input of the chopper amplifier is a dc signal V_{in}, the signal at the output of the first chopper modulator is a square wave of period T and amplitude V_{in} .If the amplifier has a gain A_o, an infinite bandwidth and does not introduce any delay, the signal

at its output is simply the same square wave with an amplitude A_0 $V_{in,}$ and the signal after demodulation is again a dc signal of value A_0 V_{in}.

To illustrate a less ideal solution, assume now that the amplifier has a constant gain A_0 up to twice the chopper frequency and is zero otherwise (ideal low-pass). As shown in figure 3.18, the amplifier output signal $V_A(t)$ is now a sinewave corresponding to the fundamental component of the chopped dc signal with an amplitude (4/) (A_o .V_{in}). The output of the second modulator is then a rectified sinewave containing even order harmonic frequencies components. The dc value after low-pass filtering is (4/) (A_o.V_{in}), corresponding to an equivalent dc gain of (8/ ^{2}). A_0 = 0.8. A_0.

This example shows that the finite bandwidth of the amplifier introduces some spectral components around the even harmonics of the chopper frequency which have to be low-pass filtered to recover the amplified signal. The gain of the chopper amplifier is also sensitive to the delay introduced by the main amplifier. Assume again that the input is a dc signal V_{in} and that the amplifier has an infinite bandwidth but introduces a constant delay, say of a quarter of a period T/4. If the input and output modulators are in phase, the output signal is a chopped cosine wave, without a dc component and containing only odd harmonics. This means that the dc gain of the overall chopper amplifier is zero. If the same constant delay is introduced between the input and the output modulators, the output signal is again a rectified sine wave. This shows that in order to maintain a maximum de gain, the phase shift between the input and the output modulators has to match precisely the phase shift introduced by the amplifier. Since the noise and offset are modulated only once, they are transposed to the odd harmonics of the output chopping square wave, leaving the amplifier ideally without any offset and low-frequency noise.

3.2.3 SWITCHED BIASING TECHNIQUE

Periodical on-off switching of a MOS transistor between strong inversion and accumulation leads to a reduction of the intrinsic l/f noise of the device [33, 34, 35].

This can he explained using the picture in figure 3.19. l/f current noise is caused by traps at the Si/SiO_2 interface. The carriers (electrons or holes) can fluctuate between trapped (no current Contribution) and free states (contribution to current), when both states have approximately equal free energy for the carriers. Under constant gate-to-source voltage this is the case for a few traps.

If the operating point of the MOSFET and respectively the gate-to-source voltage is changed strongly (e.g. from accumulation to depletion), the fluctuation probability between the two states is significantly reduced, resulting in a smaller noise current contribution from the corresponding trap states. However, there is an almost equal amount of traps (at different trap energy levels) which contribute to l/f noise at the other gate voltage. If the gate voltage is changed between these two gate voltages at a rate faster than the trapping / de-trapping time constant of the traps, the situation changes. Some occupied traps cannot be discharged as well as some non-occupied traps remain empty, thus reducing the 1/f noise current of the device.

This concept is used to reduce the noise in CMOS Miller op-amp and suitable for linear, time-continuous analog CMOS IC's. Using this concept compared to a reference circuit, a threefold reduction (5 dB) at l0 Hz in 1/f noise is achieved for an operational amplifier designed in a standard 0.12 m, 1.5V CMOS technology with 12% increase in power consumption [33]

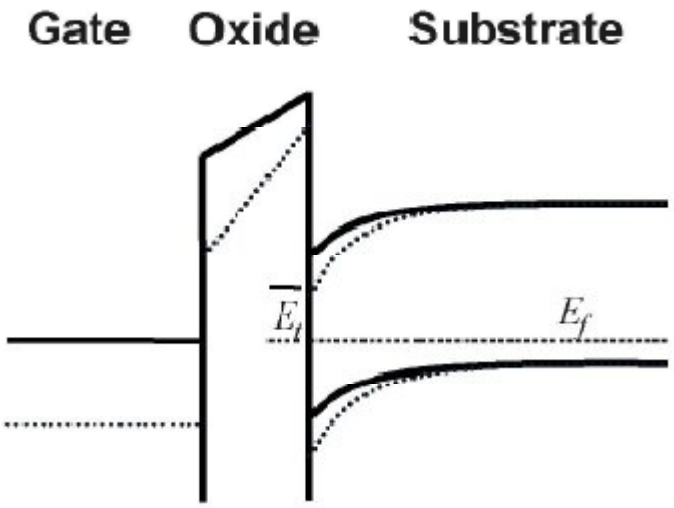


Figure 3.19 Energy band diagram for an n-MOSFET, with an active trap in the gate oxide. Solid lines show the transistors off-state (accumulation), and dashed lines the transistor on-state (inversion). [33]

This circuit architecture is further modified and achieved the 1/f noise reduction of 7 dB for a CMOS Miller operational amplifier implemented in a 0.13 μm 1.5 V standard CMOS technology. This architecture successfully reduces the 1/f noise and is applicable to a continuous signal processing analog IC's [35]. A careful design of the switches in the scheme is needed for the optimization of glitch which may occur in the circuit architecture.

The basis of the new circuit implementation is shown in figure 3.20. The transistor whose noise contribution shall he reduced is replaced by the circuit shown on the right side of figure 3.20. Using two complementary (full swing range) clock signals (Q1 and Q2) with 50 % duty cycle and two switches (SW' and SW"), the gates of Transistor Tland T2 are alternately connected to node ***G*** or VDD. One of the transistors (e.g. T') operates in inversion (on-state), the other (e.g. T") in accumulation (off-state) within the same period. In this configuration both transistors experience a switching between accumulation and inversion (which is necessary for intrinsic lif-noise reduction). Due to the alternate switching of two transistors a continuous operation of the transistor pair is assured. The principle is applicable to many time continuous analog circuits and topologies.

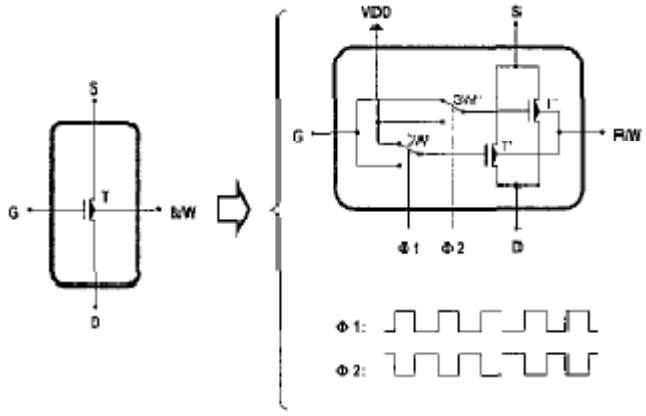


Figure 3.20 Implementation of switched biasing technique [33]

It is advantageous to choose a clock frequency which is high compared to the signal frequencies processed in the circuit. Artifacts arising from the switching can easily be filtered by an analog filter. In addition, in today's system on chip applications (which normally include A-to-D conversion), the clock frequency can also be filtered digitally and with high precision during signal processing (if chosen to be anywhere out of the signal hand(s)).

During design, care has to be taken to the resistance and capacitance of the switches (thermal noise, input capacitance) and to mixing of the clock frequency with signal frequencies due to the non-linearity of the circuit. However, low non-linearity is a design goal for most op-amps anyhow.

Finally, it has to he mentioned that the noise reduction technique can he combined with other noise reduction techniques like CHS or CHD to further suppress l/f noise.

3.2.4 SUB THREHOLD/WEAK INVERSION TECHNIQUE

MOSFETs generally generate much higher intrinsic noise than bipolar devices. This is due to the lower l/f noise of BJTs compared to MOSFETs of equivalent area, as well as their higher transconductance at a given device current. Lateral bipolar transistors have been constructed in bulk CMOS processes and have demonstrated excellent noise performance [37, 38], but large bipolar base currents (relative to MOSFET gate currents) and large parasitic vertical collector currents can limit their application in CMOS analog circuit design. However, a MOSFET operating in the subthreshold region exhibits similar characteristics to a bipolar transistor without requiring the relatively large base currents of BJTs to operate.

Unlike the square-root proportionality found in a saturation MOSFET, a subthreshold MOSFET has a linear relationship between the transconductance and the drain current [27], which is comparable to the relationship between transconductance and collector current in a BJT, as shown below (where n is process dependent).

Bipolar $$g_m = \frac{qI_c}{kT} \tag{3.19}$$

MOSFET subthreshold $$g_m = \frac{qI_D}{nkT} \quad (n \geq 1) \tag{3.20}$$

saturation $$g_m = \sqrt{2K\frac{W}{L}I_D} \tag{3.21}$$

Thus, the transconductance to drain current ratio for a MOSFET is maximized in subthreshold operation [39]. The flicker and white noise spectral densities of subthreshold MOSFETs should be less than saturation MOSFETs due to higher transconductance and different current mechanisms. The MOSFET noise equation [13] is

$$v_n^2 = \left(\frac{8}{3}kTg_m\Delta f + \frac{K}{C_{ox}WL}\frac{\Delta f}{f}\right) \tag{3.22}$$

As seen in (3.22), white noise (the first term) is inversely proportional to the transconductance g_m thus, increased transconductance will result in less white noise. Furthermore, current flow in MOSFET subthreshold operation is dominated by diffusion current rather than drift current [40], similar to the BJT. Since l/f noise has been linked to

surface effects in MOSFETs [38] and diffusion current occurs deeper into the substrate and away from the surface of the device, subthreshold devices should exhibit lower l/f noise levels than MOSFETs operating in saturation. The gain bandwidth product for a two-stage opamp is

$$\text{GBW Product} = \frac{g_{m,in}}{C_C} \tag{3.23}$$

(where C_C is the compensation capacitor), consequently, the transconductance of the differential input transistors**,** g_{mi}, should be maximized with respect to the drain current.

Similarly, the noise of an operational amplifier is generally dominated by the differential input pair [13]. Therefore, since the input transistors are the most critical devices in defining the performance of an opamp, the design requirements imply subthreshold operation of the input MOSFETs.

Typically MOSFETs operating in subthreshold have been biased at very small drain currents (< 10 nA). Although these circuits have performed well in low power applications they provide very limited gain-bandwidth. However, if a MOSFET is designed with very large width-to-length ratios then subthreshold operation at relatively high drain currents (> 1uA**)** becomes possible, and an opamp with lower equivalent input noise voltage and higher GBW product should result. PMOS transistors show low flicker noise in comparison to the NMOS transistors therefore we use the PMOS input transistor for lower flicker noise [10, 17].

From the discussion in this chapter, the designed topology of the Low Noise Low Power amplifier is shown in the figure 3.21.

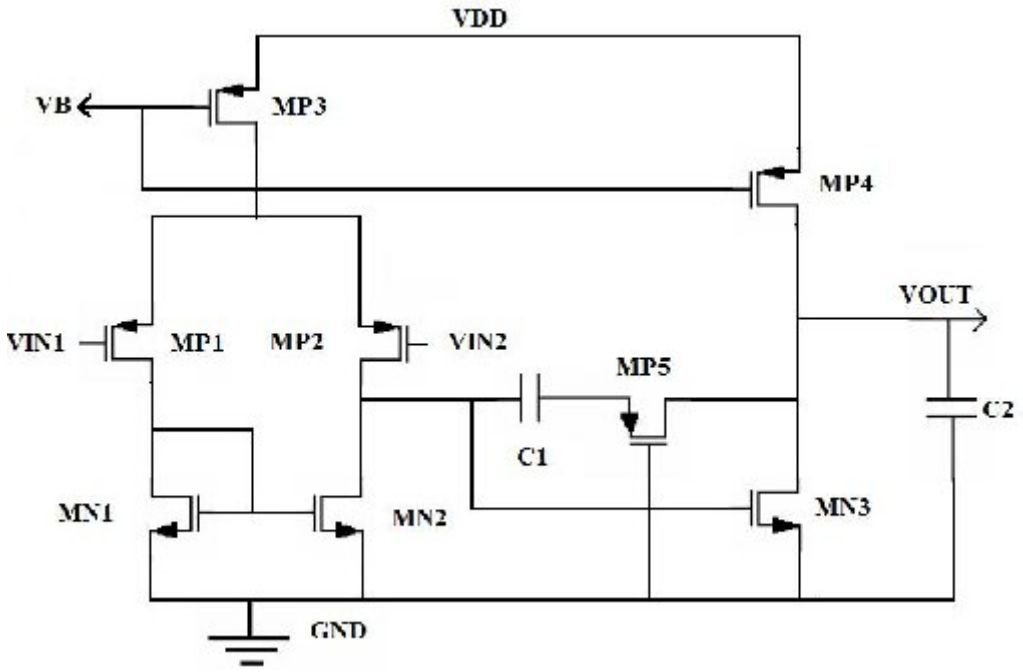


Figure 3.21 Topology of the Low Noise Low Power Amplifier

Table 3.1 shows comparison of different low power and low noise opamp design techniques. It is concluded from the above discussion that subthreshold/weak inversion technique suits best according to our requirement.

Table 3.1 Tabular comparison of low power low noise design topologies

Techniques	**Power Dissipation**	**Gain**	**Noise/ leakage current**	**Silicon area**	**Cost/ Complexicity**
Bulk Driven	Low	Low	Less noise, Large leakage	Small	High
Floating Gate	Low	Low	Low leakage	Large	High
Autozero	High	-	Low	Large	High
Chopper Stabilization	High	-	Low	Large	High
Switched Biasing	Low	High	Low	Moderate	High
Weak inversion	Ultra Low	High	Low	Moderate	Low

Chapter 4

DESIGN AND SIMULATION OF LOW POWER LOW NOISE OPERATIONAL AMPLIFIER

The main constraints in the design are the requirement of low input referred noise, low power consumption. Schematic of the two stage opamp with Miller Compensation scheme is shown in the figure 4.1.

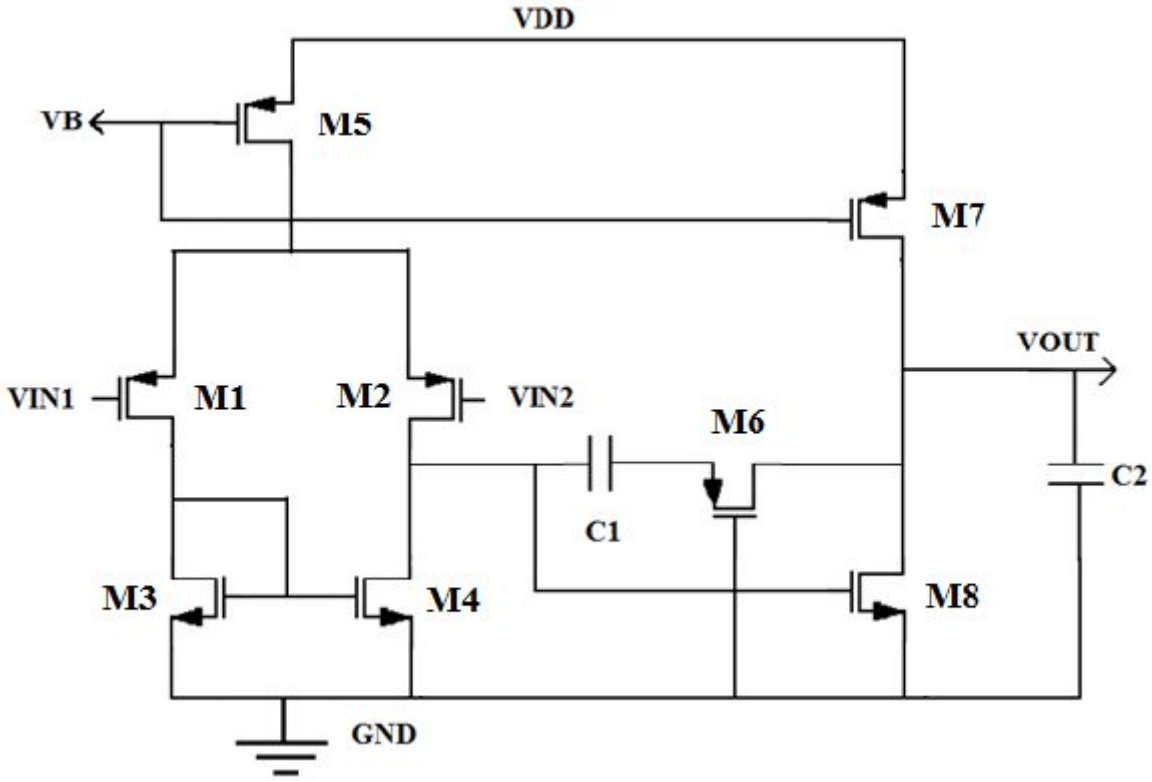


Figure 4.1 Schematic of Low Power Low Noise Opamp

4.1 DESIGN OF OPAMP

This opamp is designed using *TSMC 0.35 μm* technology with a supply voltage of 3.3*V*. The value of the load capacitance is taken as 5 *pF*

The technology parameters used in calculations are

$\mu_n C_{OX} = 132.5\times10^{-6}$ A/V^2 $\quad \lambda_n$=0.02 V^{-1} $\quad V_{tn} = 0.549V$

$\mu_p C_{OX} = 50.12\times10^{-6}$ A/V^2 $\quad \lambda_p$=|0.04| V^{-1} $\quad V_{tp} = -0.68V$

K_{Fn} = 1.000E-25 $\quad K_{Fp}$ = 1.000E-26

Where K_{Fn} is Flicker noise coefficient for NMOS and K_{Fp} is the flicker noise coefficient for PMOS.

Table 4.1 shows the target specifications of the design.

Table 4.1 Target Specifications of Design

Parameters	**Target Value**
Total input referred noise	≤ 1 μV
Power dissipation	30 μW
DC open loop gain	≥ 60 dB
Unity gain bandwidth	5 MHz
Phase margin	≥50°
f_{-3dB} frequency	≥ 1 KHz
CMRR	≥ 85 dB
PSRR	≥ 85 dB

According to requirement for low power and low noise, we start from the noise analysis of the op-amp and then set the current using power dissipation. Circuit for noise analysis is shown in the figure 4.2 on next page. Figure 4.2 (a) shows the contribution of noise by each transistor and figure 4.2 (b) shows the noise refereed to the input of transistor M1.

Total output noise current is

$$i_o^2 = g_{m1}^2 v_{eq1}^2 + g_{m2}^2 v_{eq2}^2 + g_{m2}^2 v_{eq2}^2 + g_{m3}^2 v_{eq3}^2 + g_{m4}^2 v_{eq4}^2 \tag{4.1}$$

If v_{eqT}^2 is the total input refereed noise at the input of transistor M1 therefore

$$i_o^2 = g_{m1}^2 v_{eqT}^2 \tag{4.2}$$

Now the total input referred noise is

$$v_{eqT}^2 = v_{eq1}^2 + v_{eq2}^2 + \left(\frac{g_{m3}^2}{g_{m1}^2}\right)\left(v_{eq3}^2 + v_{eq4}^2\right) \tag{4.3}$$

Where $g_{m1} = g_{m2}$ and $g_{m3} = g_{m4}$

Flicker noise of transistor is given as

$$v_{eq}^2 = \frac{K}{WKC_{ox}} \frac{\Delta f}{f} \tag{4.4}$$

where K is the flicker noise coefficient.

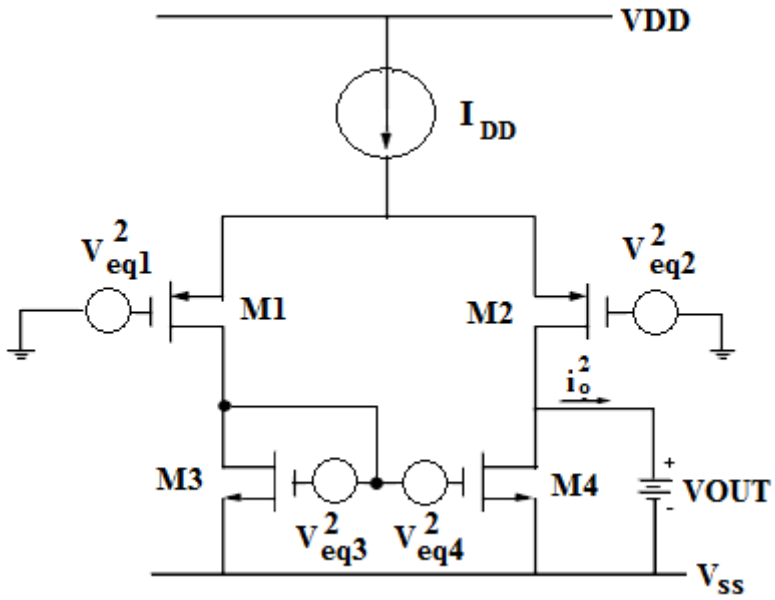


Figure 4.2 (a) Circuit for calculation of output noise [13]

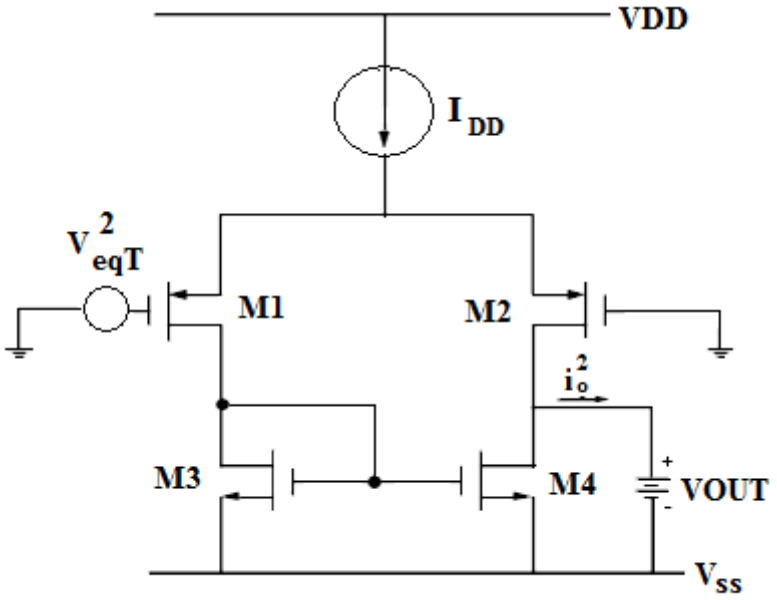


Figure 4.2 (b) Circuit for calculation of input refereed noise [13]

By putting value of flicker noise of transistors M1, M2, M3 and M4 in equation (4.3) we get flicker noise refereed at the input of transistor M1 [13]

$$v_{flic\,\mathrm{ker}}^2 = \frac{2K_p}{fW_1L_1C_{ox}}\left(1+\frac{K_n\mu_n}{K_p\mu_p}\frac{L_1^2}{L_3^2}\right)\Delta f \tag{4.5}$$

K_n and K_p are flicker noise coefficients for NMOS and PMOS respectively.

Thermal noise of the transistor is given as

$$v_{eq}^2 = \frac{8kT}{3g_m}\Delta f \tag{4.6}$$

where k is Boltzmann constant.

By putting value of thermal noise of transistors M1, M2, M3 and M4 in equation (4.3) we get thermal noise refereed at the input of transistor M1 [13]

$$v_{thermal}^2 = 4kT\frac{4}{3\sqrt{2\mu_pC_{ox}\left(\frac{W}{L}\right)_1 I_D}}\left(1+\sqrt{\frac{\mu_n\left(\frac{W}{L}\right)_3}{\mu_p\left(\frac{W}{L}\right)_1}}\right)\Delta f \tag{4.7}$$

From the above noise analysis it is concluded that for low noise

- Transconductance of the input transistor should be greater than load transistor. Sizing devices M1 and M2 with large W/L ratios forces them to operate in the weak inversion region, where their relative transconductances are maximized.
- Flicker noise in PMOS transistors is 1-2 orders of magnitude lower than in NMOS transistors [41, 42].
- Gate Area of transistors should be large.
- Length of load transistor should be greater than the input transistor.

From equation (4.7), if $g_{m1} >> g_{m3}$ then the tranconductance of the input transistor can be calculated.

Now, we are not able to determine the aspect ratio of M1 and M2, since their bias currents are not set, but the knowledge of , and the gain-bandwidth product requirement, allows us to draw the value of the compensation capacitor according to the following equation

$$C_1 = \frac{1}{2\pi}\frac{g_{m1,2}}{f_{UGB}} \tag{4.8}$$

For phase margin of 60^o Value of Cc can also be calculated according to $C_1 > 0.22C_2$ [27, 43].

Current can be calculated from the power requirement as given by the equation

$$P_d = V_{dd} \times I_B \tag{4.9}$$

Where $I_B = I_{D5} + I_{D7}, I_{D7}$ is 2-3 times greater than the I_{D5}.

The slew rate associated with C_1 is found to be

$$\text{Slew Rate}_{\text{INT}} = \frac{I_{D5}}{C_1} \tag{4.10}$$

The slew rate associated with C_2 is found to be

$$\text{Slew Rate}_{\text{EXT}} = \frac{I_{D7} - I_{D5}}{C_2} \tag{4.11}$$

Aspect ratio of the transistor M1 and M2 can be calculated from the equation

$$\left(\frac{W}{L}\right)_{1,2} = \frac{g_{m1,2}^2}{2\mu_n C_{ox} I_{D1,2}} \tag{4.12}$$

For a two stage amplifier in which the frequency behaviour can well be assumed with a single non-dominant pole (a single second pole), the phase margin is expressed by [44]

$$M_\phi = 90^o - \arctan\frac{f_{UGB}}{f_{SP}} \tag{4.13}$$

where, due to the pole-splitting effect, the frequency at which the second pole occurs is

$$f_{SP} = \frac{g_{m8}}{2\pi C_2} \tag{4.14}$$

Therefore, the tranconductance gain of M8 results [44]

$$g_{m8} = 2\pi f_{UGB} C_2 t_g\left(M_\phi\right) \tag{4.15}$$

since = , its aspect ratio is

$$\left(\frac{W}{L}\right)_8 = \frac{g_{m8}^2}{2\mu_n C_{ox} I_{D7}} \tag{4.16}$$

Since current I_{D7} is known, aspect ratio of transistor M7 can be calculated. Once the transconductance of transistor M8 is known, we also can find the value of resistance R_C that compensate for the right half plane zero caused by the forward path to the output. This resistance can be implemented by a PMOS (M6) transistor in triode region and is given by

$$R_C = \frac{1}{g_{m8}} \tag{4.17}$$

For two pole amplifier, the separation factor K, between the second pole and gain bandwith product is defined as

$$K = \frac{f_{SP}}{f_{UGB}} \tag{4.18}$$

Phase margin of 60^o means a K value of about 1.7 [44].

Using equations (4.8), (4.14) and (4.18) the compensation capacitor can also be expressed as

$$C_1 = K \frac{g_{m1,2}}{g_{m8}} C_2 \tag{4.19}$$

As for as transistors M3 and M4 is concerned, they contribute to the systematic offset and CMRR, besides affecting noise performance.

In order to improve both offset and CMRR, accurate matching must be guranted by both a proper layout design and symmetrical bias condition. This means the same drain source voltages, other than the same aspect ratio. Consequently, we must set

$$V_{GS3} = V_{DS4} = V_{GS8} \tag{4.20}$$

which gives

$$\left(\frac{W}{L}\right)_{3,4} = \frac{I_{D3.4}}{I_{D8}} \left(\frac{W}{L}\right)_8 \tag{4.21}$$

After employing above all equation (4.1) - (4.21) and using some iteration on tool, we design low power low noise amplifier with following aspect ratio, capacitor values and biasing voltages as shown in Table 4.2 and 4.3.

Table 4.2 Capacitor Value and Biasing Voltage

function	value
Load Capacitances	5 pf
Miller Capacitance	1.5 pf
Current Source Bias	2.5 V

Table 4.3 Low Power Low Noise Amplifier Device Sizes

Device	Width/Length in Microns	Function
M1/M2	140/1.4	Input Transistor
M3/M4	1.4/10.4	Input Stage Load
M5	10.5/0.7	Bias Current Source
M6	4.2/14	Miller Resistance
M7	15.4/0.7	Output Stage Load
M8	1.4/2.8	Output stage Driver

4.2 SIMULATION OF OPAMP

Prepared circuit of amplifier is simulated at mentor graphics ASIC design kit design architect IC tool at 0.35µm technology. The amplifier is to be powered from a 3.3 volts power supply. All values have been measured at load capacitance of 5pF.

The simulations include AC response, Transient analysis, Common Mode Rejection Ratio, Power Supply Rejection Ratio, Input Common Mode Range and Noise Analysis.

SIMULATION RESULTS

This design provided an overall gain of 68.80 dB with Power Dissipation 31.26 . Total Input refereed Noise is 382.68 nV/$\sqrt{Hz}$ at 1 Hz, 123.68 nV/$\sqrt{Hz}$ at 10 Hz and 30.75 nV/$\sqrt{Hz}$ at 1 KHz. Common Mode rejection is 109.4173 dB and Power Supply Rejection Ratio of 99.85 dB. Unity gain bandwidth is 4.5 MHz with 3dB frequency of 1.32 KHz. The phase margin comes out to be nearly 56.45º making design relatively stable.

4.2.1 AC RESPONSE

This response is used for observing open loop gain, Unity Gain Bandwidth (UGB), 3-dB bandwidth and the Phase Margin of the circuit. In the test setup a differential AC signal of 1V is applied to the inputs along with this the dc bias potential is also applied. The output was taken between single end and GND. In figure 4.3, one method of measuring the AC performance is presented. In this configuration, the amplifier is open loop, and the AC

small signal is applied at the input. In Figure 4.4, a Gain and phase plot for 3.3V, 27°C is shown. As can be seen, the open loop gain is 68.80dB, 3-dB frequency is 1.32 KHz and a phase margin is nearly 56.45º.

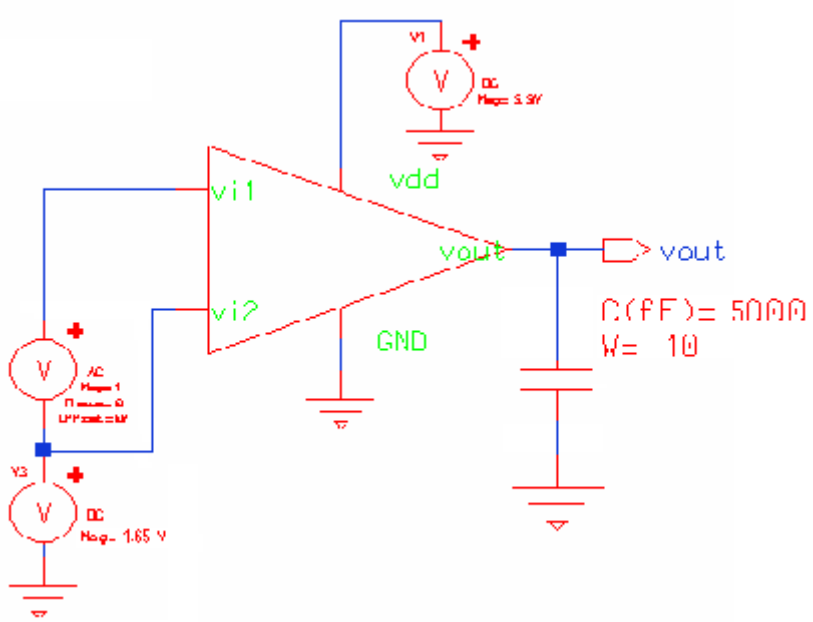


Figure 4.3 Configuration for simulating the open loop frequency response of op-amp

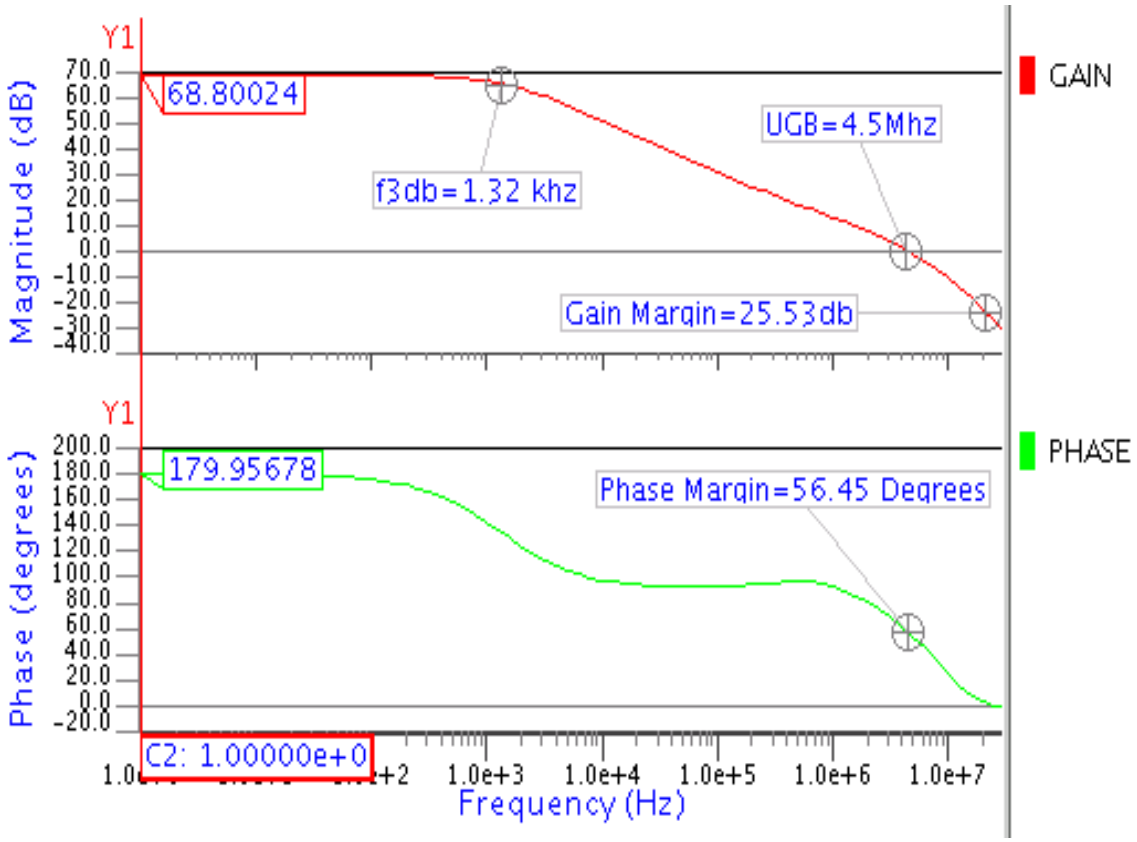


Figure 4.4 Frequency response of op-amp

4.2.2 TRANSIENT RESULTS

Schematic for the transient simulation of the amplifier in unity gain configuration is shown in the figure 4.5 and simulation result is shown in the figure 4.6. We get the output swing (peak to peak) 2.99 V.

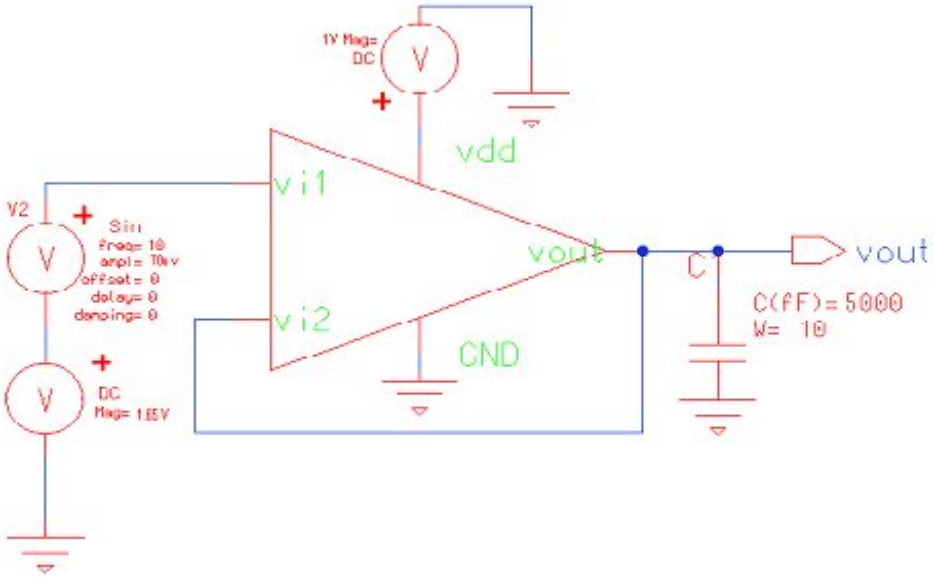


Figure 4.5 Schematic for the simulation of the transient Response with unity feed back

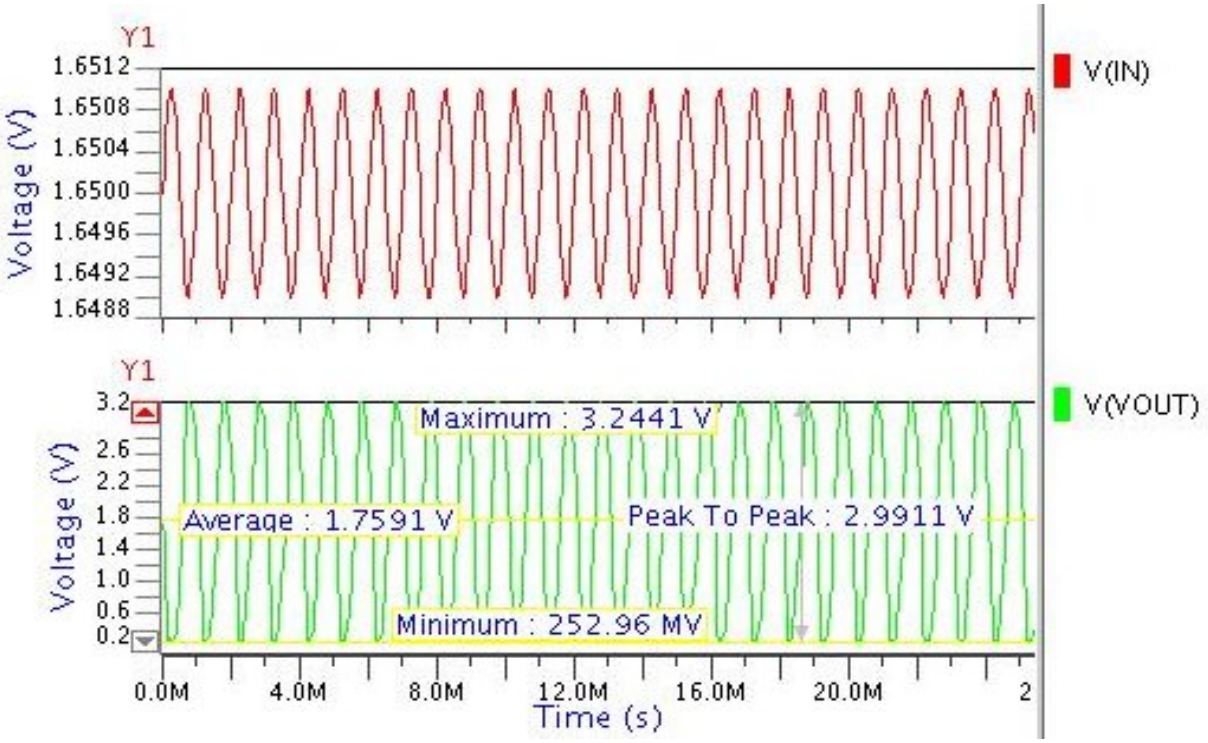


Figure 4.6 Input and Output signals for transient analysis

4.2.3 STEP RESPONSE – SLEW RATE MEASUREMENT

In figure 4.7, a step from ground to *VDD* is applied at the input with unity feedback configuration. The amplifier's slew rate is 806.21mV/µs for the rising edge and 2.6125V/µs for the falling edge.

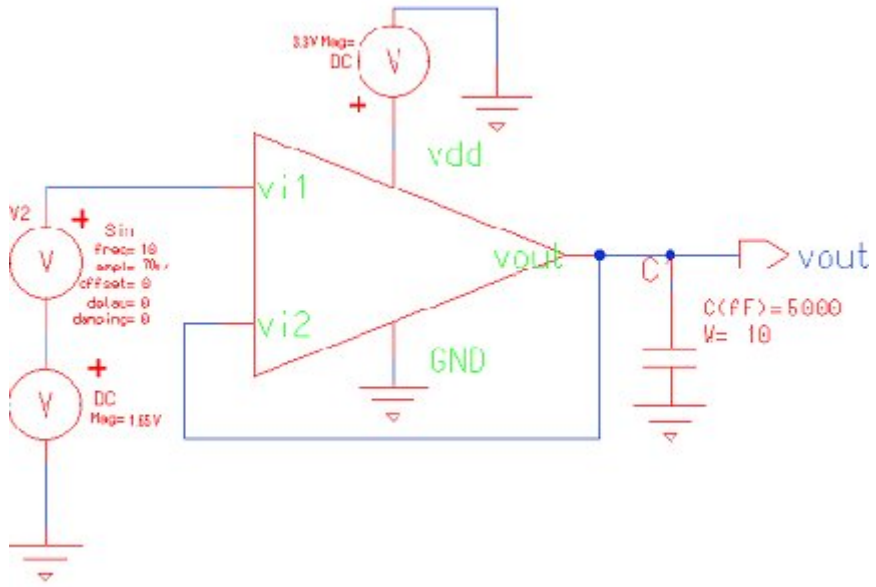


Figure 4.7 Schematic for the simulation and measurement of the slew rate

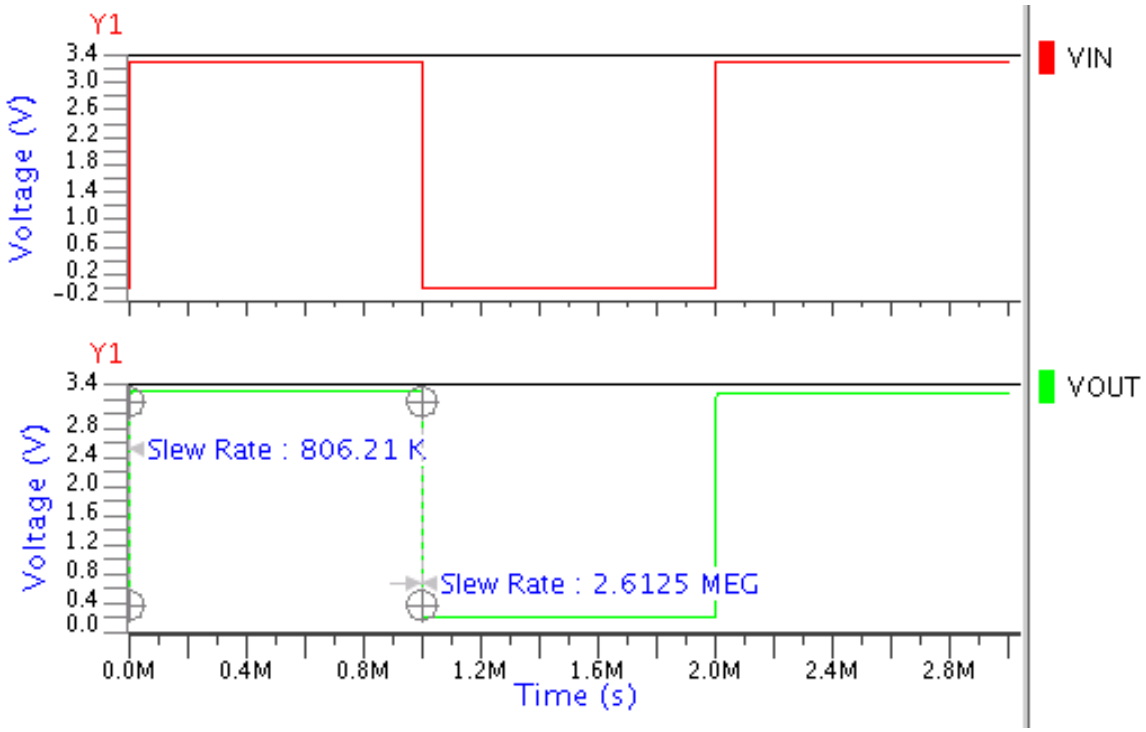


Figure 4.8 Slew rate for the rising and falling edge with opamp in unity gain configuration

4.2.4 SETTLING TIME

Settling time is the length of time for the output voltage of an operational amplifier to approach, and remains within, a certain tolerance of its final value. This is usually specified for a fast full-scale input step. In figure 4.2.10 shows the settling time of the input pulse of 1V magnitude in unity gain configuration for different tolerance values.

Table 4.4 Variation of Settling Time of opamp with different Tolerance values

Tolerance (%)	Settling Time (µs)
1	3.8200
5	3.5813
10	3.3782

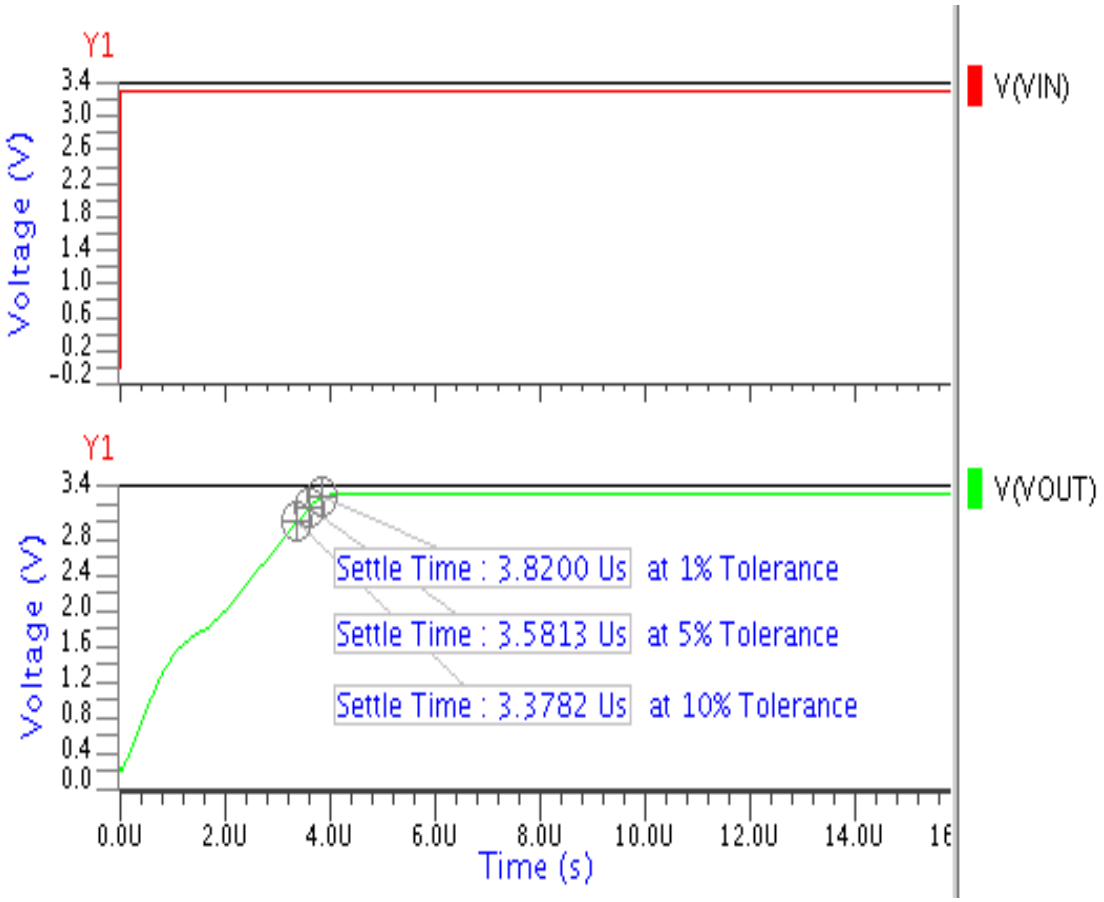


Figure 4.9 Settling time for the different tolerance values with unity gain configuration

4.2.5 COMMON MODE REJECTION RATIO

In order to simulate common mode rejection, differential gain as well as the common mode gain of the op-amp is required and the CMRR is obtained by A_{DG}(dB)-A_{CM}(dB). A 1V AC source is placed on the positive input as shown in figure 4.10.

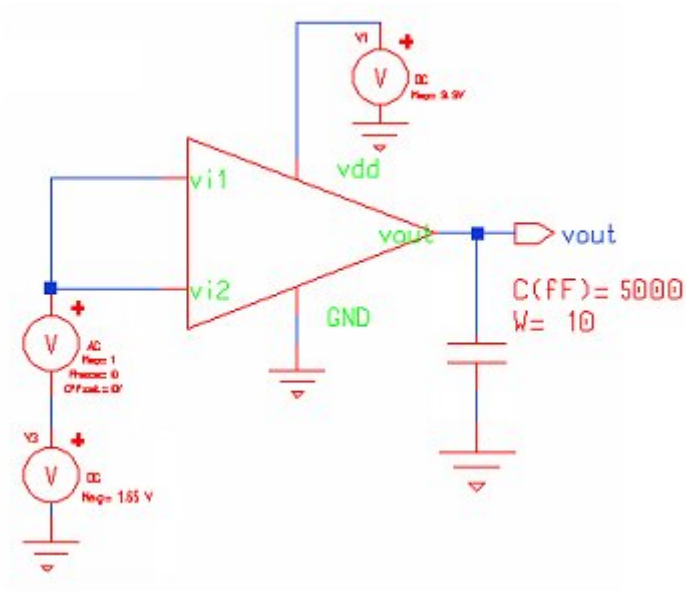


Figure 4.10 Schematic for the simulation of CMRR

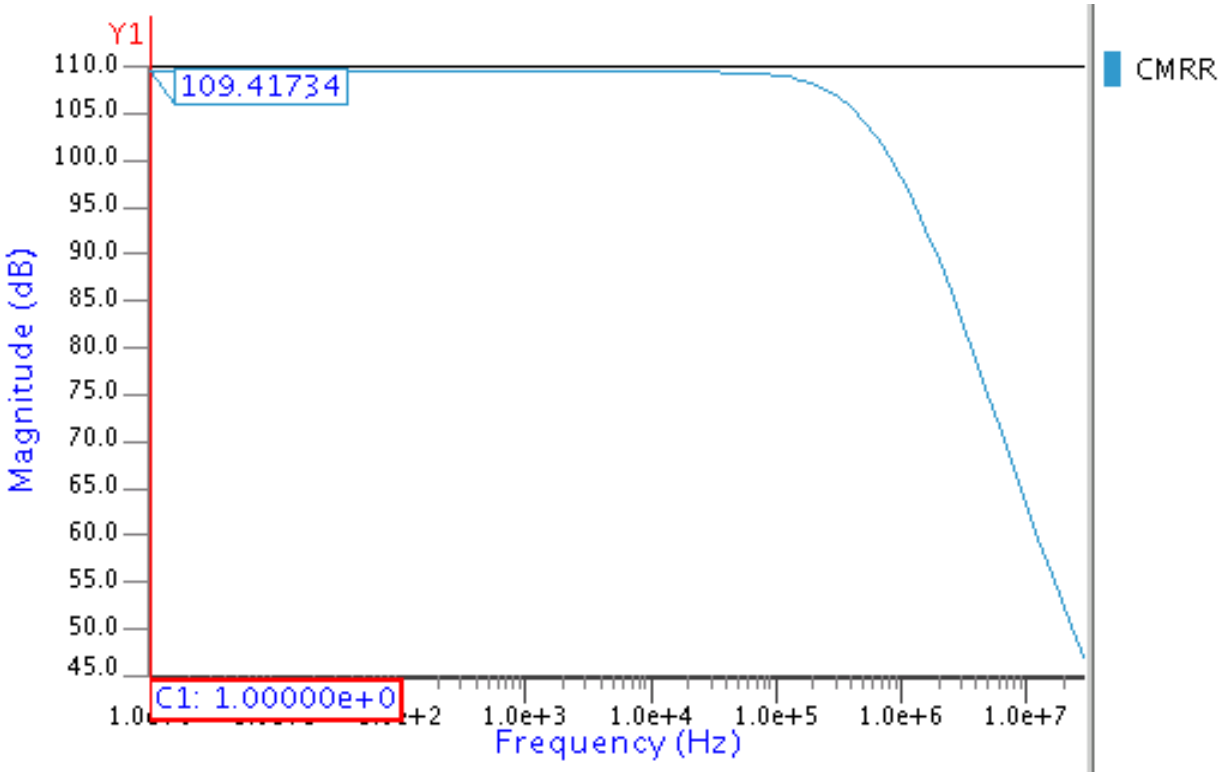


Figure 4.11 Simulation Result of Common Mode Rejection Ratio

When the simulator sweeps the frequency, there will be a 1V AC source on both the positive and negative inputs and hence the AC signal at the output will be the common mode gain [27]. The previously calculated gain can be divided by this gain to give the CMRR. The common mode rejection ratio was found the value 109.4173dB.

4.2.6 POWER SUPPLY REJECTION RATIO

PSRR or power supply Rejection Ratio shows the capability of the circuit to reject supply noise. There are two PSRR one for positive supply voltage and other of negative supply voltage. It is of two types:-

a) Positive PSRR

b) Negative PSRR

POSITIVE PSRR

The test setup shown below is for positive PSRR. In this method we apply only common mode dc potential to the input transistors and a 1V AC signal is inserted between VDD supply and VDD port of the circuit.

In order to simulate power supply rejection, differential gain as well as the PSRR+ gain of the op-amp is required and the CMRR is obtained by A_{DG}(dB)-A_{PSRR+}(dB).

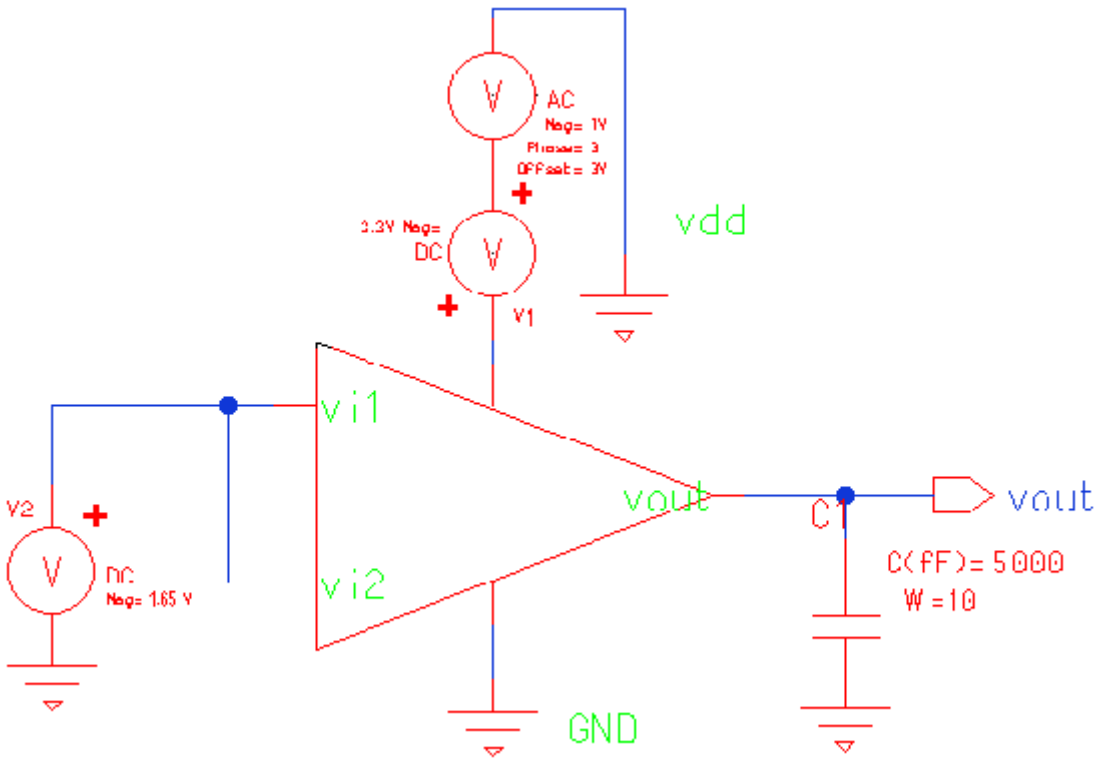


Figure 4.12 Schematic for the simulation of Positive PSRR

The value of positive PSRR is 99.85 dB at lower frequency and 96.84 dB at 3dB frequency.

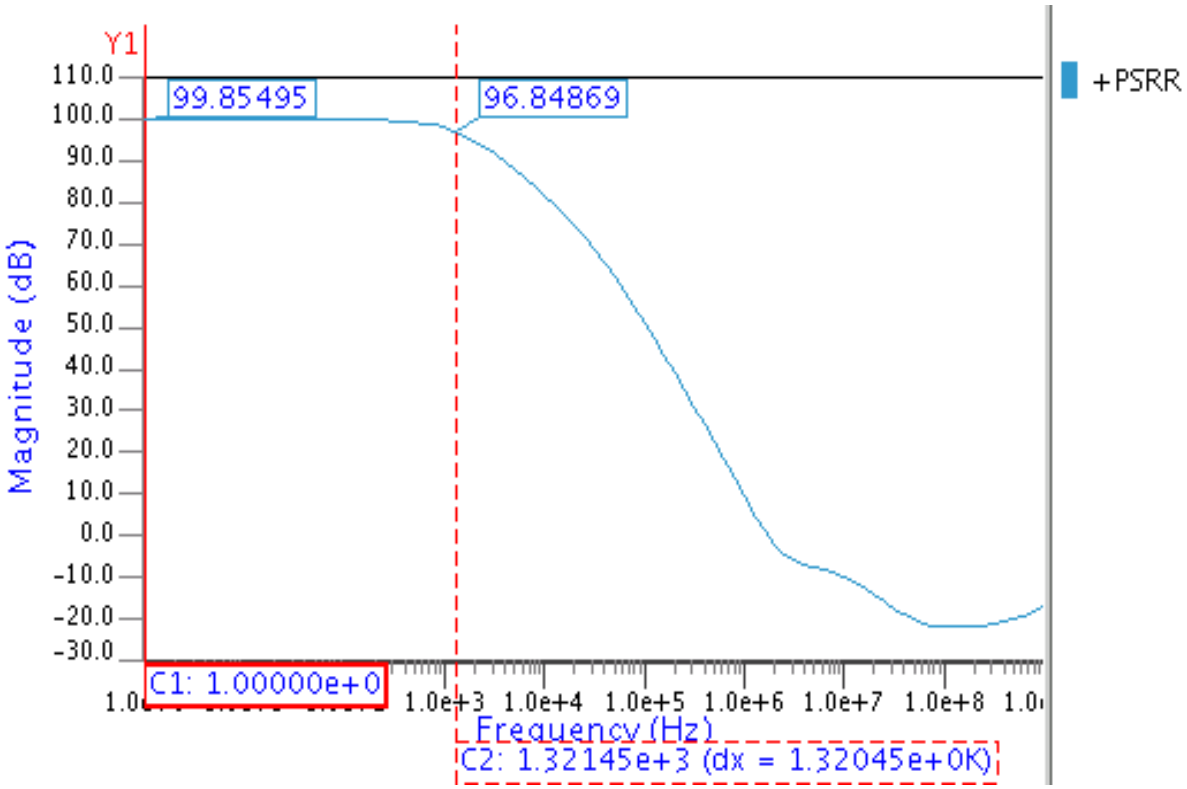


Figure 4.13 Simulation Result of Positive Power Supply Rejection Ratio

NEGATIVE PSRR

The test setup is shown in figure 4.14 for negative PSRR.

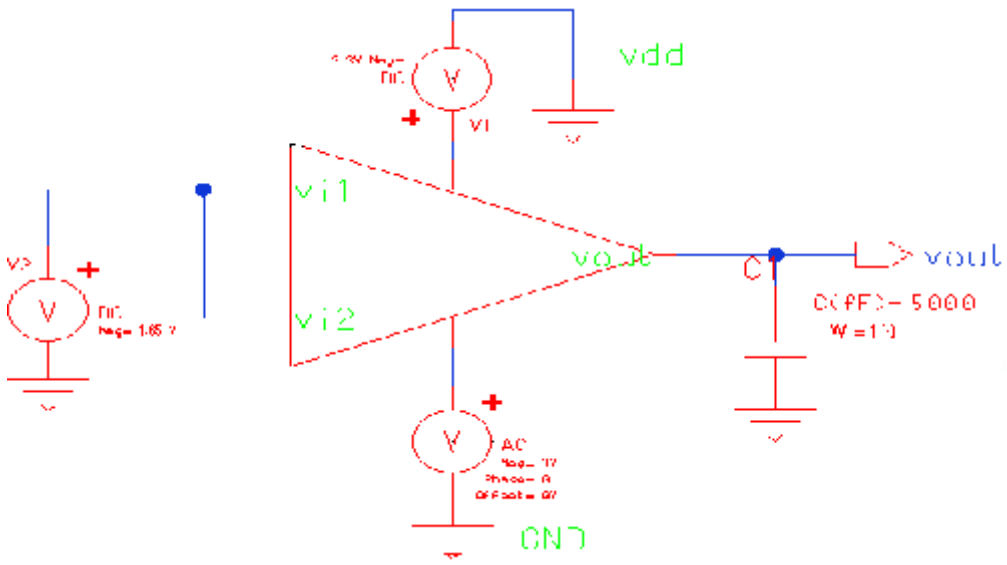


Figure 4.14 Schematic for the simulation of Negative PSRR

In this method we apply only common mode dc potential to the input transistors and a 1V AC signal is inserted at ground terminal, now the differential gain which we get at the output of the op-amp is noted.

This gain is subtracted from differential gain A_D(dB) then the pot we get is the PSRR plot.The value of negative PSRR is 111.249 dB at lower frequency and 108.23 dB at 3dB frequency.

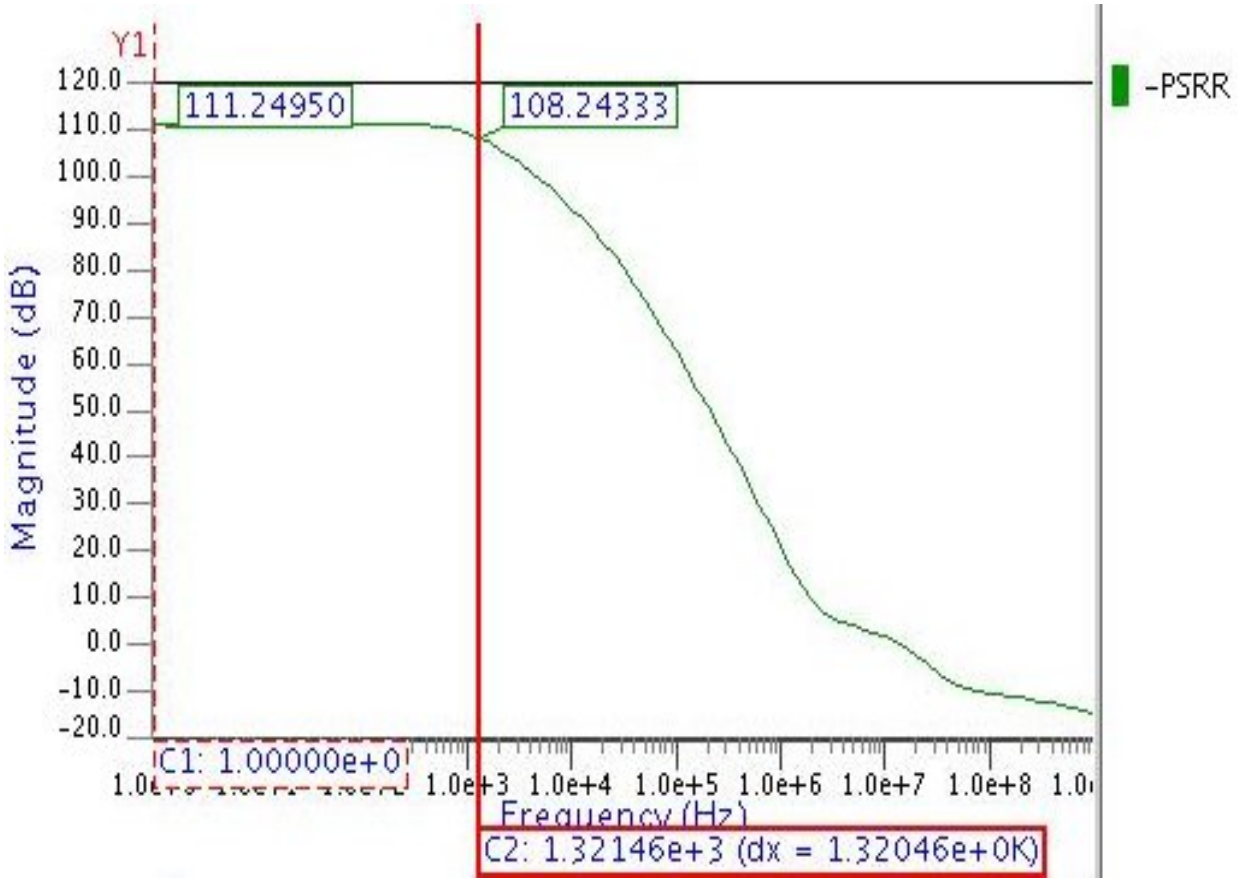


Figure 4.15 Simulation Result of Negative Power Supply Rejection Ratio

4.2.7 INPUT COMMON-MODE RANGE CHARACTERISTICS USING UNITY GAIN CONFIGURATION

DC analysis of the circuit provides the ICMR. This test is performed to test the offset voltage and the input common mode range of the op-amp that is the range of op-amp for which there is a linear relationship between input and the output.

Figure 4.16 shows the setup of simulating ICMR opamp is in unity gain configuration and at non-inverting terminal dc voltage sweep from 0 to 3.3 is applied. As shown in figure 4.17 at 0 V input voltage, output value is .2216 V.

This is the output offset voltage. Input offset can be obtained by dividing this value to the DC gain.

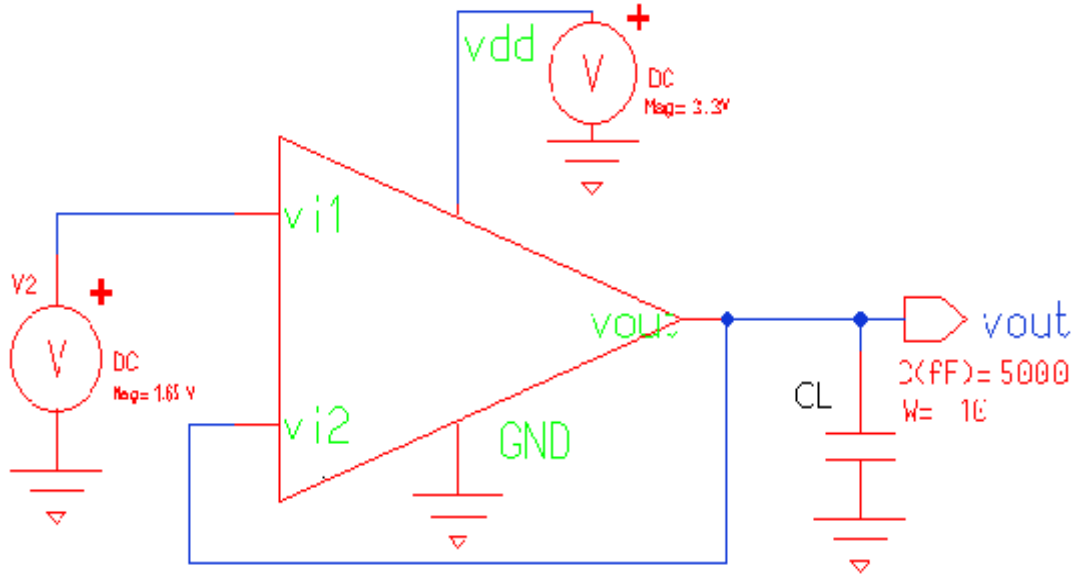


Figure 4.16 Schematic for the simulation of Input Common-Mode Range

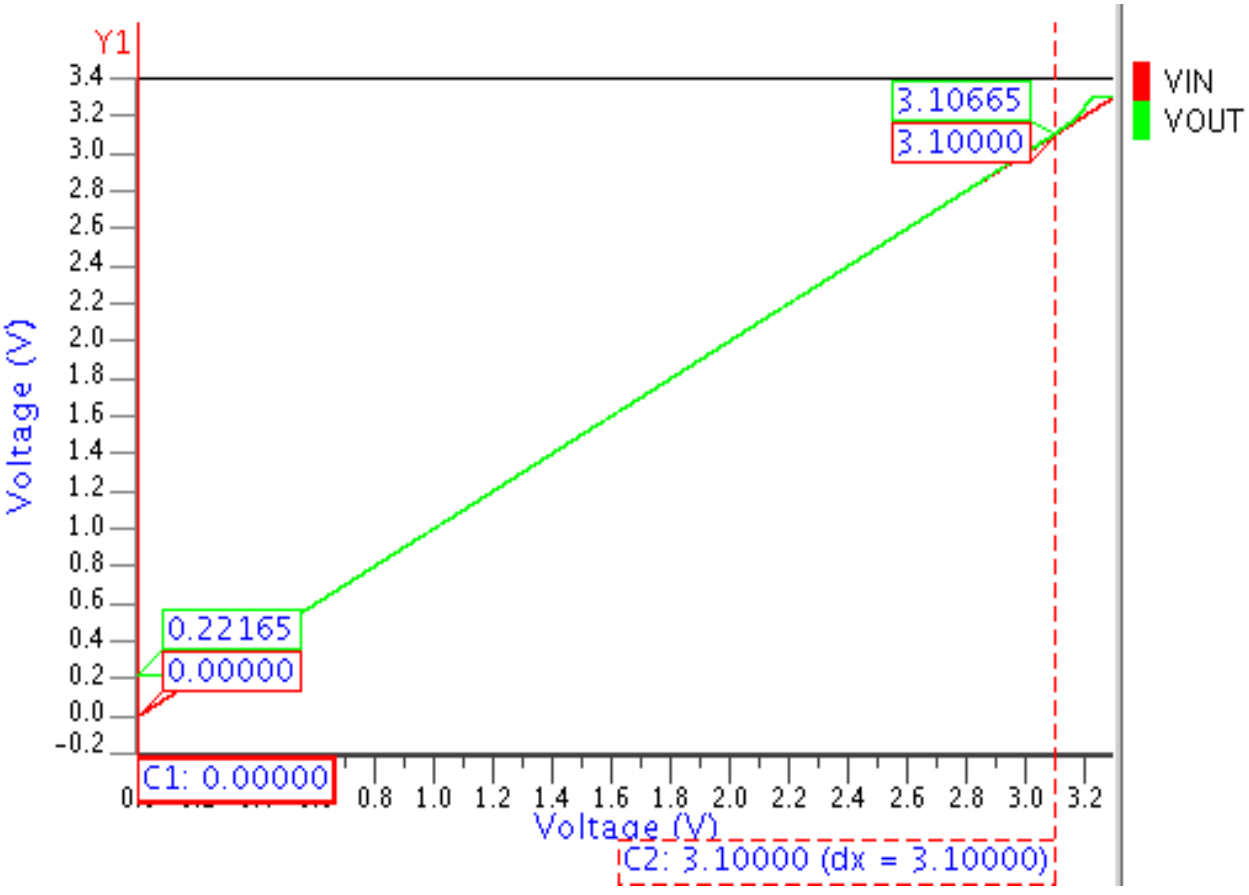


Figure 4.17 Simulation Result of Input Common-Mode Range

4.2.8 EFFECT OF VARIATION OF TEMPERATURE ON FREQUENCY RESPONCE

The frequency response is shown in figure 4.18 at different temperature. The temperature is varied from -20°C to 70°C and corresponding change in gain is from 68.85db to 68.75db. The gain will decrease with temperature because transconductance of opamp will decrease with temperature. The decrement in transconductance is due to the decrement in mobility.

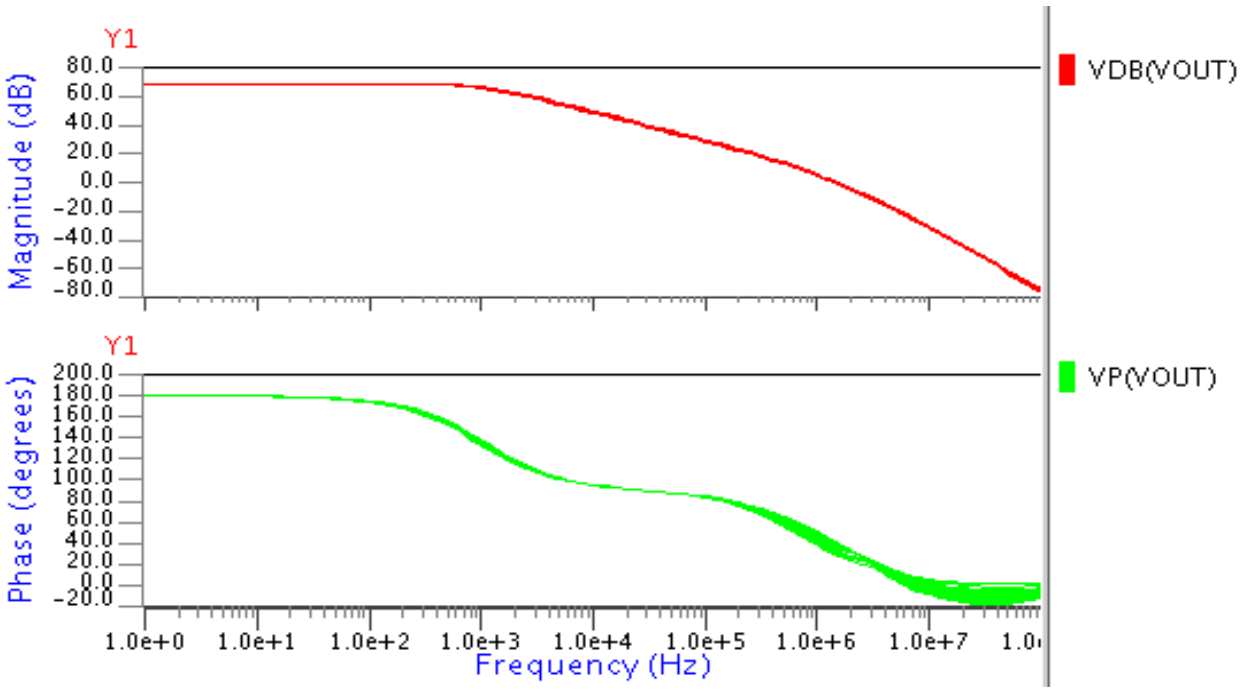


Figure 4.18 AC response with temperature variation

4.2.9 NOISE ANALYSIS

For noise analysis the opamp is as shown in figure 4.19. The terminals are connected to a common mode dc level without ac signal. And the output is measured at the output terminal. Now this output value is divided by dc gain of the opamp. The input referred noise is shown in figure 4.20. The Total Input Refereed Noise comes out 382.68 nV/$\sqrt{Hz}$ at 1 Hz, 123.68 nV/$\sqrt{Hz}$ at 10 Hz and 30.75 nV/$\sqrt{Hz}$ at 1 KHz.

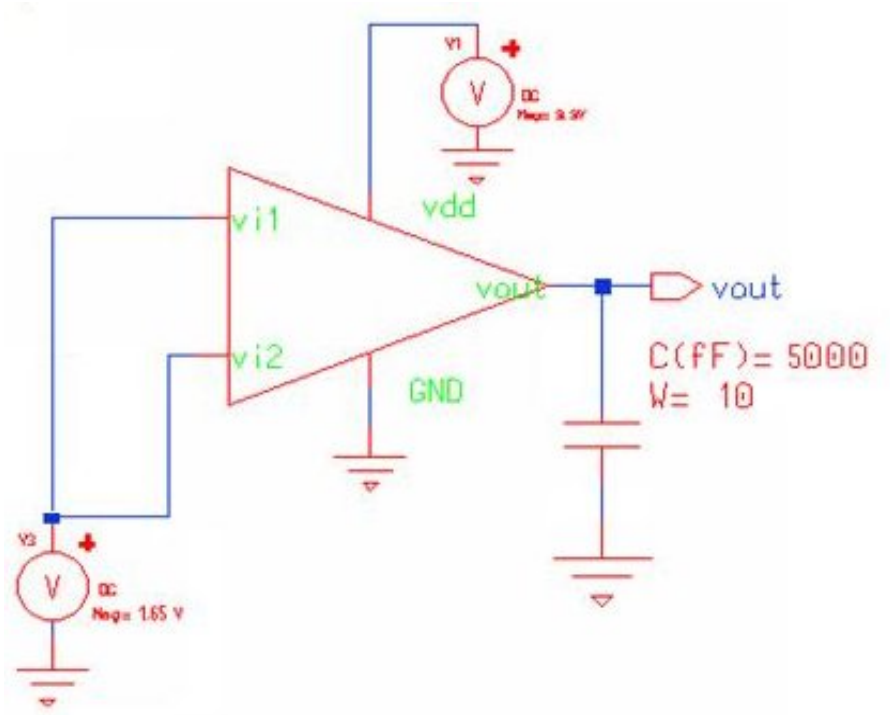


Figure 4.19 Schematic for the simulation of Noise Analysis

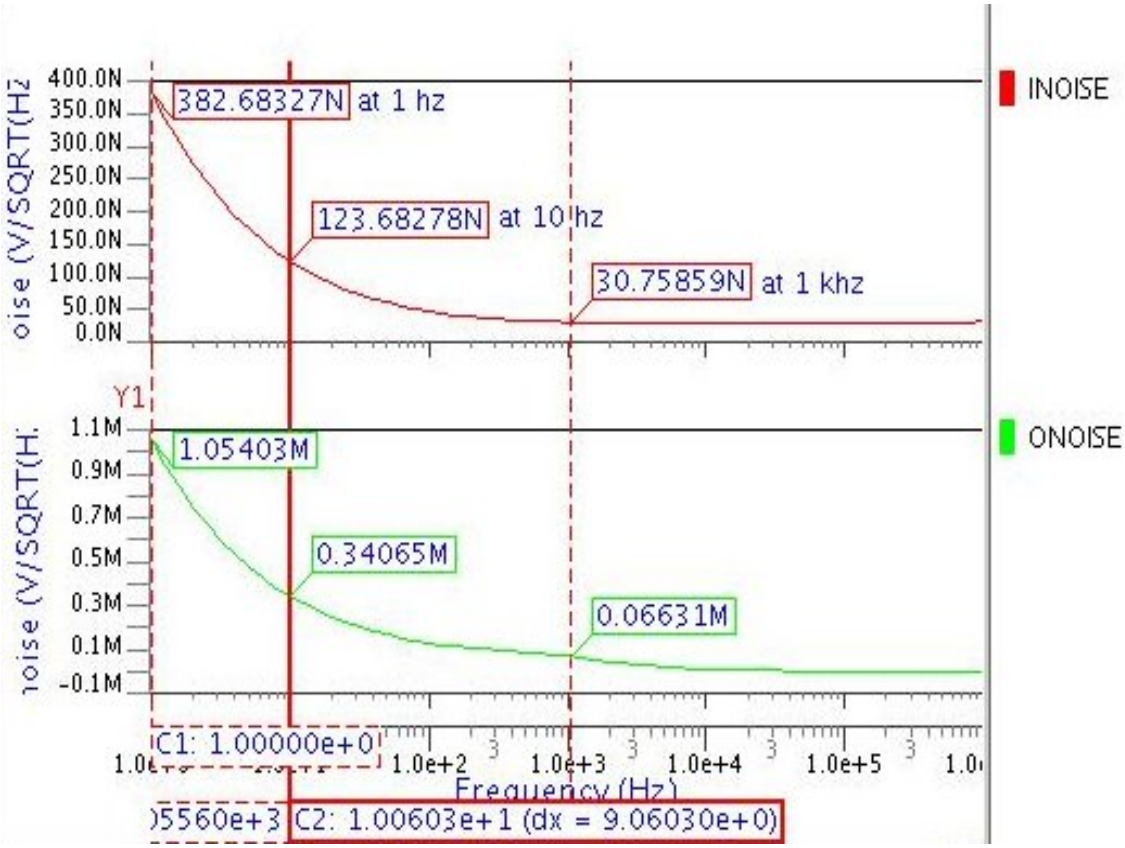


Figure 4.20 Simulation Results of Total Input Referred Noise

4.2.10 CORNER FREQUENCY

Corner frequency for the amplifier is shown in the figure 4.21. It is obtained 182.91 Hz.

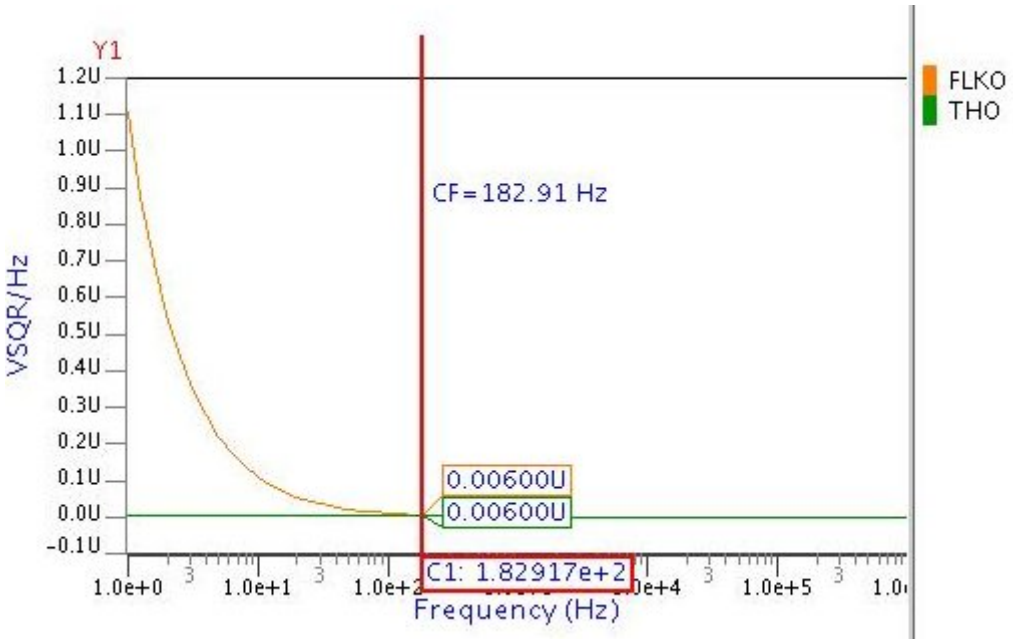


Figure 4.21 Corner frequency

4.2.11 EFFECT OF VARIATION OF TEMPERATURE ON NOISE

Effect of variation of temperature from -20^{o} to 70^{o} is shown in the figure 4.28. We see from the result, when the temperature increases noise is increases. It is due to the increase in carrier fluctuations. Due to the temperature variation, variation in noise occurs of 22 nV.

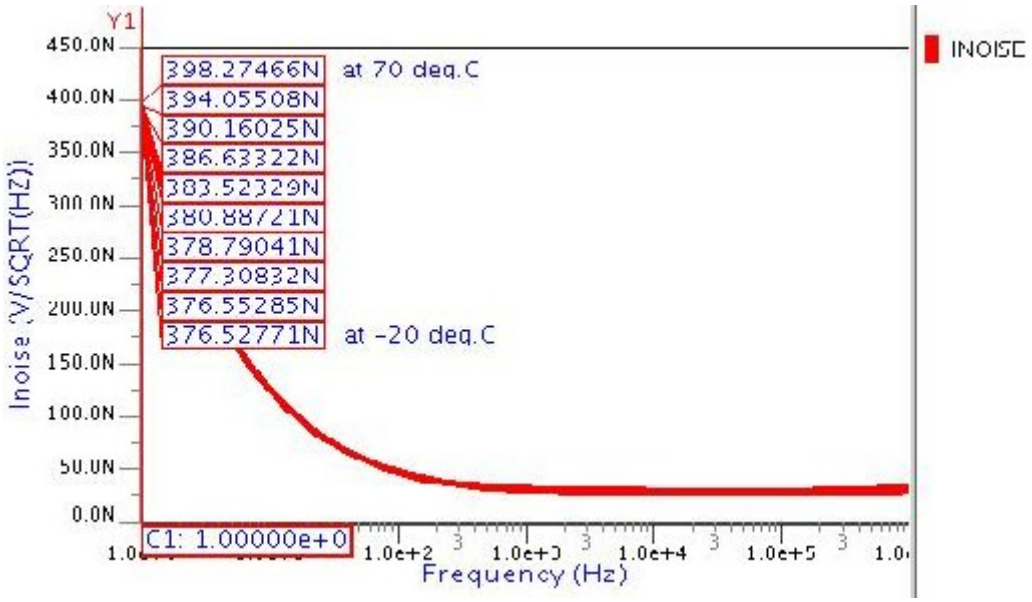


Figure 4.22 Temperature variation effect on total input noise

Table 4.5 shows the individual value of total input noise at different temperature.

Table 4.5 Input noise variation with temperature variation

Temperature (degree)	**Input Noise(nV/$\sqrt{Hz}$)**
-20º	376.527
0º	377.308
20º	380.887
40º	386.633
70º	398.274

Table 4.6 shows the simulation results obtained by design.

Table 4.6 Simulation Results of Low Power Low Noise Opamp

Specification parameters	**Simulation Results**
Unity Gain Bandwidth (UGB)	4.8 MHz
F_{3dB} Frequency	1.32 KHz
Low Frequency Gain	68.80 dB
Phase Margin	56.45 deg
Power Consumption	30.26 µW
Slew Rate	806.2 mV/µs, 2.61V/µs
ICMR	.22 V to 3.3 V
Output Offset Voltage	221 mV
Output Swing	2.99 V
Settling Time (10%)	3.37 µs
+PSRR / -PSRR	99.85 dB / 111.2495 dB
CMRR	109.4173 dB
Input Refereed Noise at 1 Hz at 10 Hz at 1 KHz	 382 .68 nV/$\sqrt{Hz}$ 123.68 nV/$\sqrt{Hz}$ 30.75 nV/$\sqrt{Hz}$
Corner Frequency	182.91 Hz

Chapter 5

LAYOUT AND POSTLAYOUT SIMULATION

5.1 ANALOG LAYOUT

When low-level or high-precision circuitry is being designed, a lot of care is usually given to the details of the circuit schematic and how the signal runs are routed. In doing layouts for digital circuits, the speed and the area are the two most important issues. In contrast, in doing layout for analog circuits, everything should be considered simultaneously.

In addition to the speed and the area, other equally critical considerations should be taken into account. In analog layout more care has to be taken as the circuit performance changes drastically due to noise, mismatches, crosstalk and shielding required to protect critical nodes from being disturbed. Without proper layout, the mismatches and the coupled noise would be quite large and would significantly degrade the performance of the amplifiers [7, 45, 46].

5.1.1 ANALOG LAYOUT ISSUES

(a) Matching of Devices

Device mismatch is too often treated as part of the black art of analog design. Random device mismatch plays an important role in the design of accurate analog circuits. The device mismatch is due to number factors like local process variation, global lithographic variations, local lithographic variations and process gradients. These factors affect all devices transistors, resistor, capacitors, and therefore similar techniques can be used to match all elements. During fabrication phase mismatch in physical parameters like doping concentration (Na), mobility (μ), oxide thickness (tox) and layout dimensions (W, L) gives origin to mismatch in electrical parameter like V_T and β and thus mismatch in I_D.

Matching of individual devices is of paramount concern in analog circuit design. Infect almost all of the 'analog layout techniques' are actually methods for improving matching between different devices on a chip. Matching is important because most analog circuit designs use a ratio based design technique. Some common techniques that help improve device matching are MULTI-GATE FINGER LAYOUT and COMMON-CENTROID LAYOUT [46, 47].

Use of transistor fingering for large and critical transistors is always beneficial. In fingering the transistor is “fingered” into multiple transistors that are connected in parallel. The folded transistors reduce the source/ Drain junction area and the gate resistance. The gate resistance can be reduced by decomposing the transistor into more parallel fingers.

Common-centroid layout refers to a layout style in which a set of devices has a common center point. This is used to minimize the effect of linear process gradients (e.g. oxide thickness) in a circuit [46].

Example: Consider that a transistor 'A' has 'M' fingers and can be represented by 'M' instances of the letter 'A'. For example 'AAAA' represents a transistor 'A' that has 4 fingers.

Now consider the layout of two transistors, 'A' and 'B'. One structure is:

AABB

The problem with this structure is that the transistor 'A' will have a different oxide capacitance (which affects transconductance, Ft) than 'B' because of oxide gradients. For instance, if the oxide thickness at the center of the structure is Tox, and there is an oxide gradient DEL, the average oxide thickness for 'A' and 'B' is

Tox (A, average) = [Tox - 2DEL]/2 + [Tox - DEL]/2 = Tox - 3DEL/2

Tox (B, average) = [Tox + 2DEL]/2 + [Tox + DEL]/2 = Tox + 3DEL/2

Now consider the following layout:

ABBA

The average oxide thickness will now be:

Tox (A, average) = [Tox - 2DEL]/2 + [Tox + 2DEL]/2 = Tox

Tox (B, average) = [Tox - DEL]/2 + [Tox + DEL]/2 = Tox.

(b) NOISE

Dynamic range is limited by noise and so it is an important parameter to be considered in all analog circuits. In general there are two types of noise, random noise and environmental noise. Random noise is consisting of a large number of transient disturbances with a statistically random time distribution. Thermal noise is an example of random noise. Random noise is dealt with at the circuit design level. However there are some layout techniques which can help to reduce random noise. The gate resistance of the

poly-silicon and the neutral body region, which are both random noise sources, is reduced by multi-gate finger layout [7].

Other noise considers is environmental noise. Environmental noise is also dealt with at the circuit level. One common design technique used to minimize the effects of environmental noise is to employ a 'fully-differential' circuit design, since environmental noise generally appears as a common-mode signal. However Substrate plugs is also very useful for reducing 'substrate noise', which is a particularly troublesome form of environmental noise encountered in highly integrated mixed-signal systems and Systems-On-a-Chip (SOC).

5.2 LAYOUT OF OPAMP

Due to huge aspect ratio MP1 and MP2 transistors are divided into multiple fingers. Aspect ratio of MP1 and MP2 is 140/1.4. Since 140 = 3 × 46.66 thus a single transistor is divided in to 3 fingers with width of 46.66µm.

Layout of the opamp without capacitive load is shown in the figure 5.1.

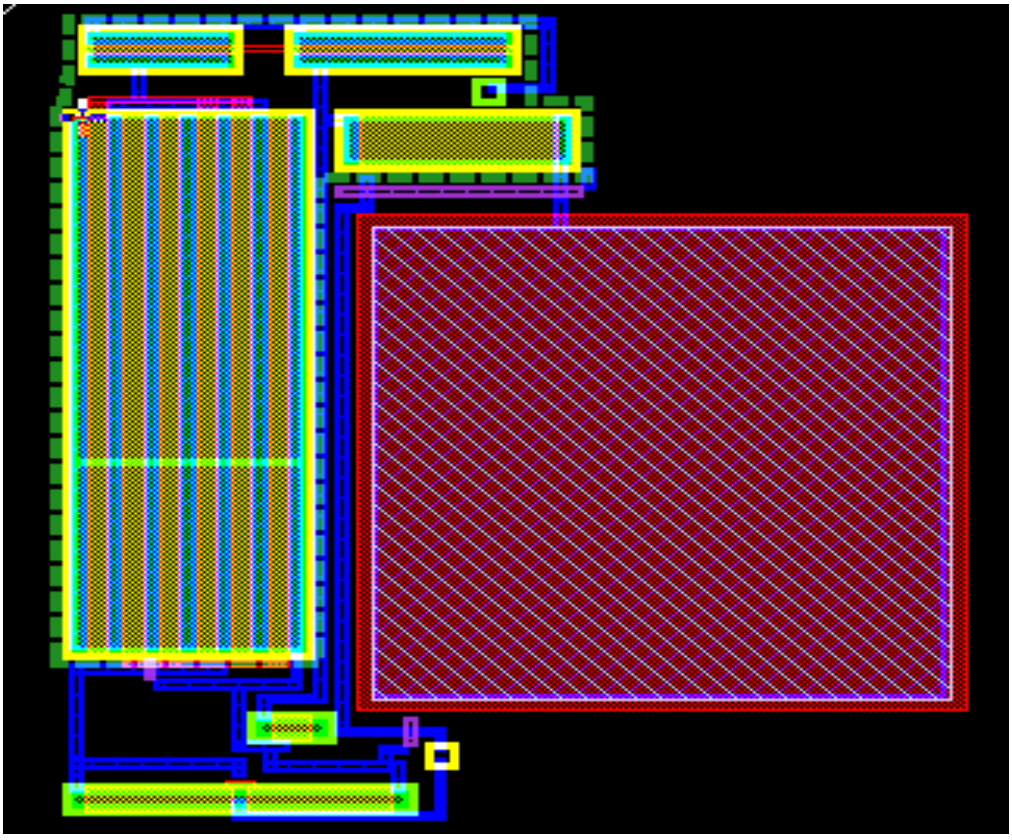


Figure 5.1 Layout of Low Power Low Noise Opamp without load

Layout of the opamp with capacitive load is shown is the figure 5.2.

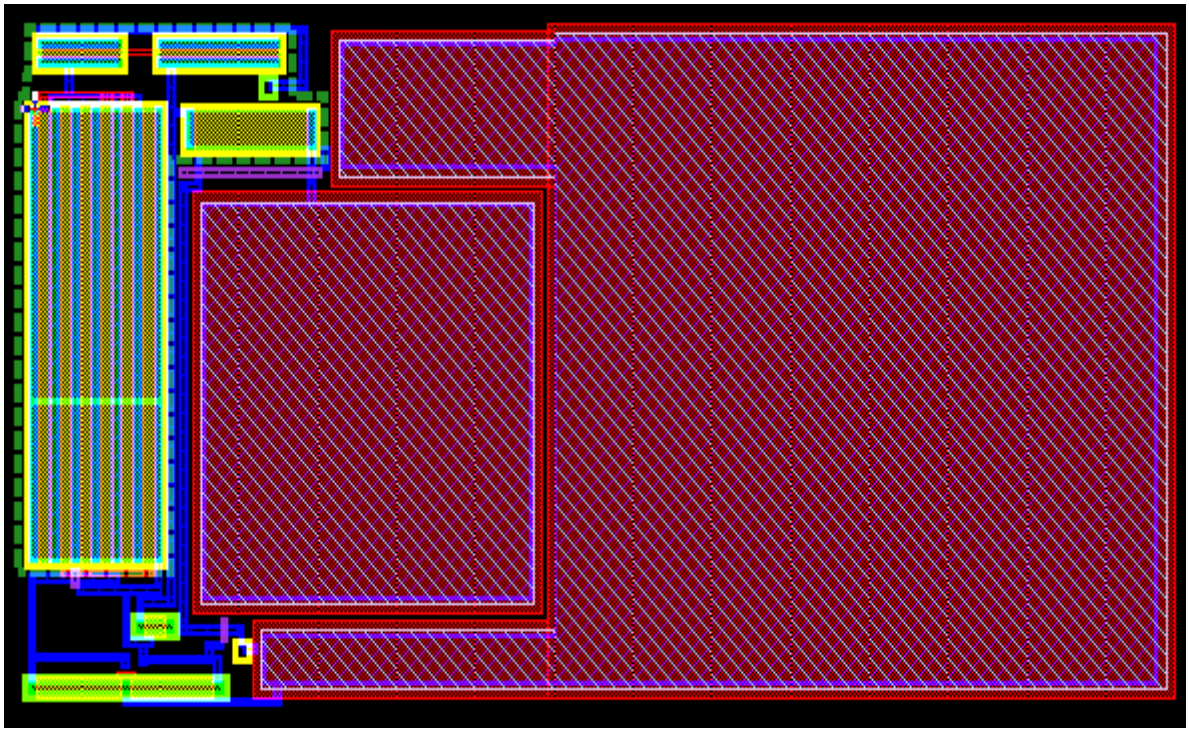
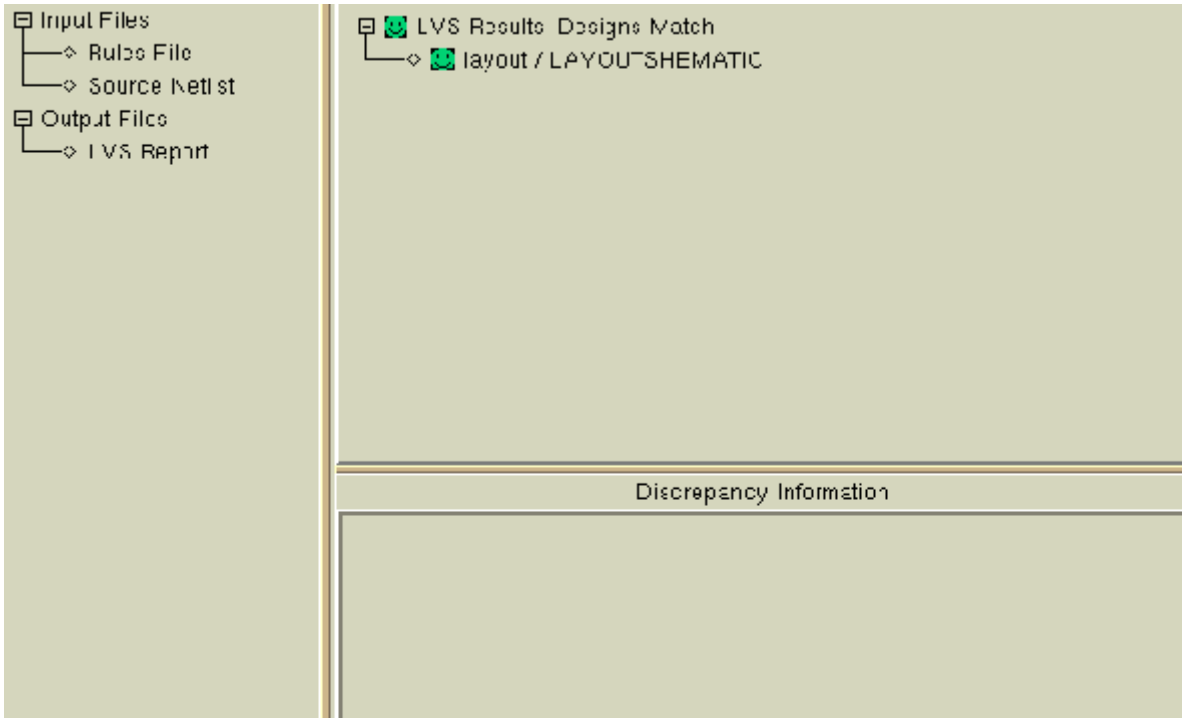


Figure 5.2 Layout of Low Power Low Noise Opamp with load

5.3 DESIGN MATCH REPORT

After completing the layout, layout is compared with the schematic. For this comparison



a source netlist generated by the schematic is matched with the layout and provides the design match report and LVS report. This checks all the connections in schematic with layout.

A smiling face in the design match report and in LVS report shows the successfully matching of layout and schematic. Source netlist and LVS report is given in appendix A.1 and A.2.

5.4 PEX REPORT

After matching of layout and schematic PEX has to be check, which verifies all the components values in schematic with layout and give information about parasitic if they come in to picture. The PEX report is given in appendix A.3.

5.5 POST LAYOUT SIMULATION

After completing the PEX, Post layout simulations have been done on extracted netlist. The simulation results of post layout simulation are given below.

5.5.1 AC RESPONSE

Post layout frequency response curve is shown below.

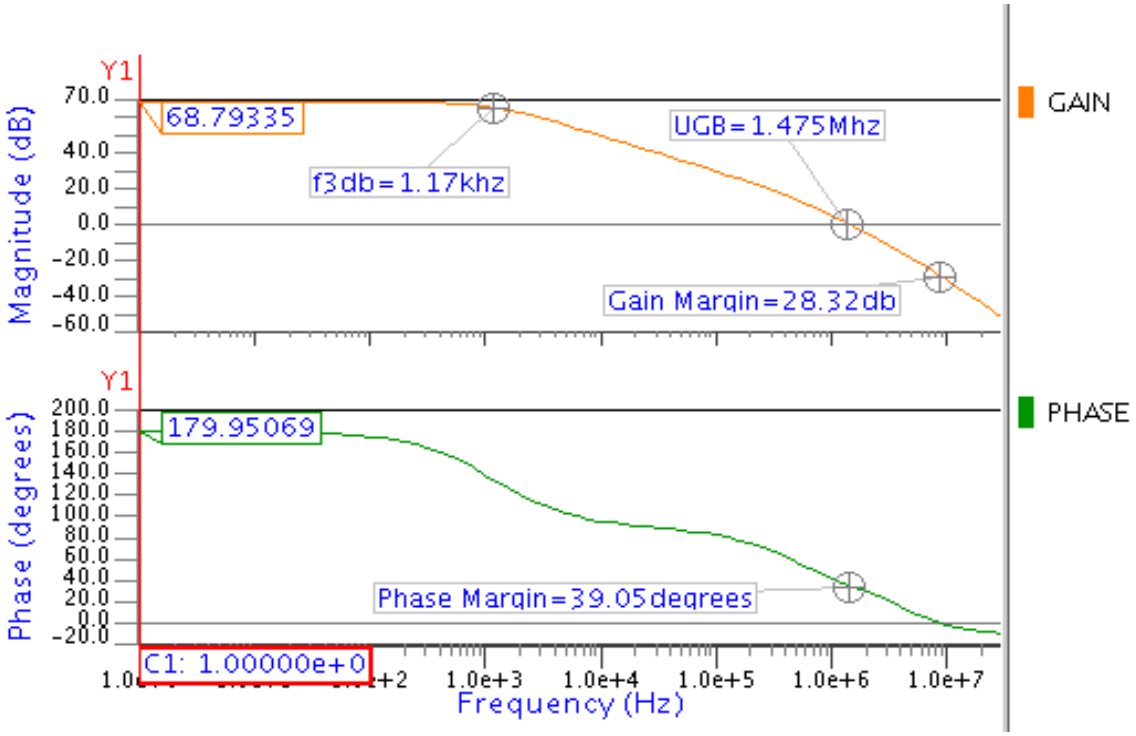


Figure 5.3 Post layout simulation - AC analysis

The post layout results of frequency response shows that there is a very small negligible variation in gain of op-amp but phase margin changes due to the addition of parasitic capacitances.

5.5.2 AC RESPONSE WITH TEMPERATURE VARIATION

Gain and phase variation with temperature is negligible. So circuit is suitable for wide range of temperature.

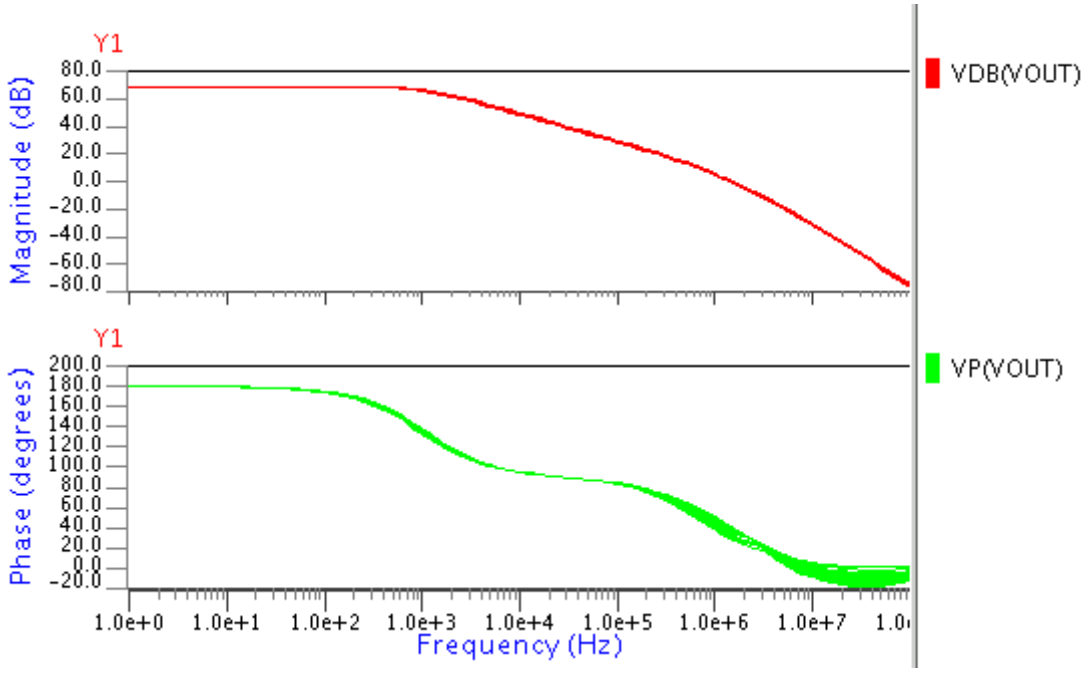


Figure 5.4 Post layout simulation –AC response with temperature variation

5.5.3 STEP RESPONSE – SLEW RATE MEASUREMENT

A small change occurs in slew rate of rising edge but falling edge slew rate changes more due to the parasitices.

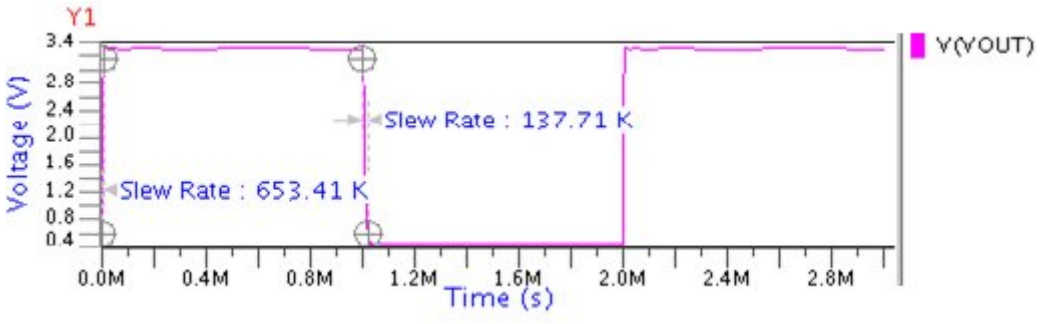


Figure 5.5 Post layout simulation – slew rate

5.5.4 SETTLING TIME

Settling time with layout, simulation comes with some slightly high value then schematic simulation. This is due to parasitic addition in circuit.

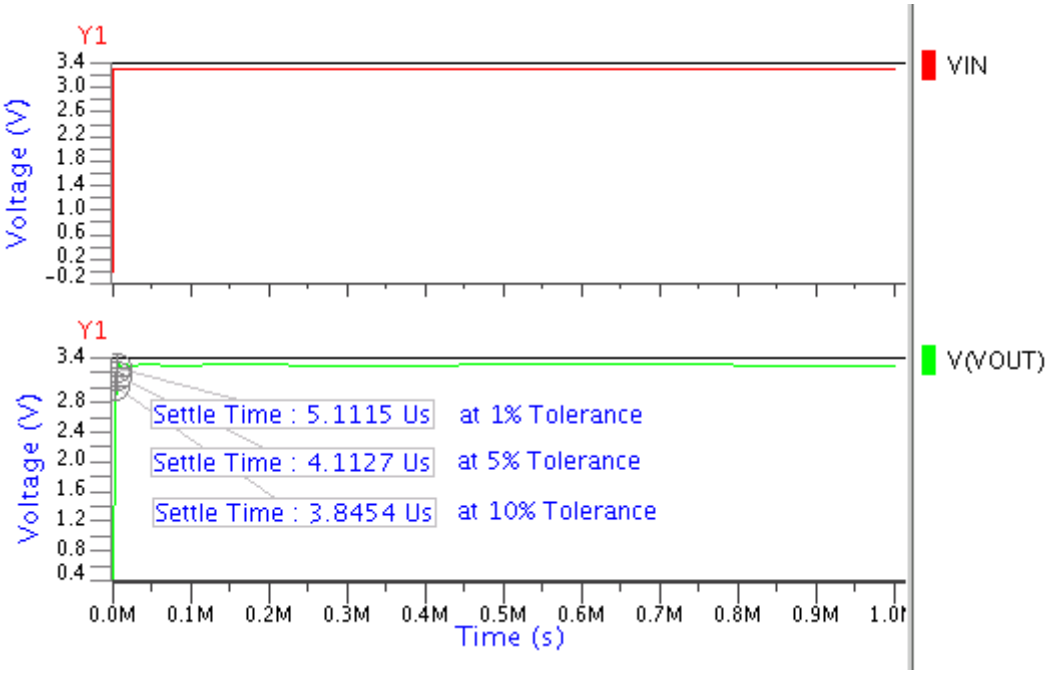


Figure 5.6 Post layout simulation – Settling time for the different tolerance values

5.5.5 COMMON MODE REJECTION RATIO

CMRR comes out as 109.4191dB which is similar to the schematic simulation.

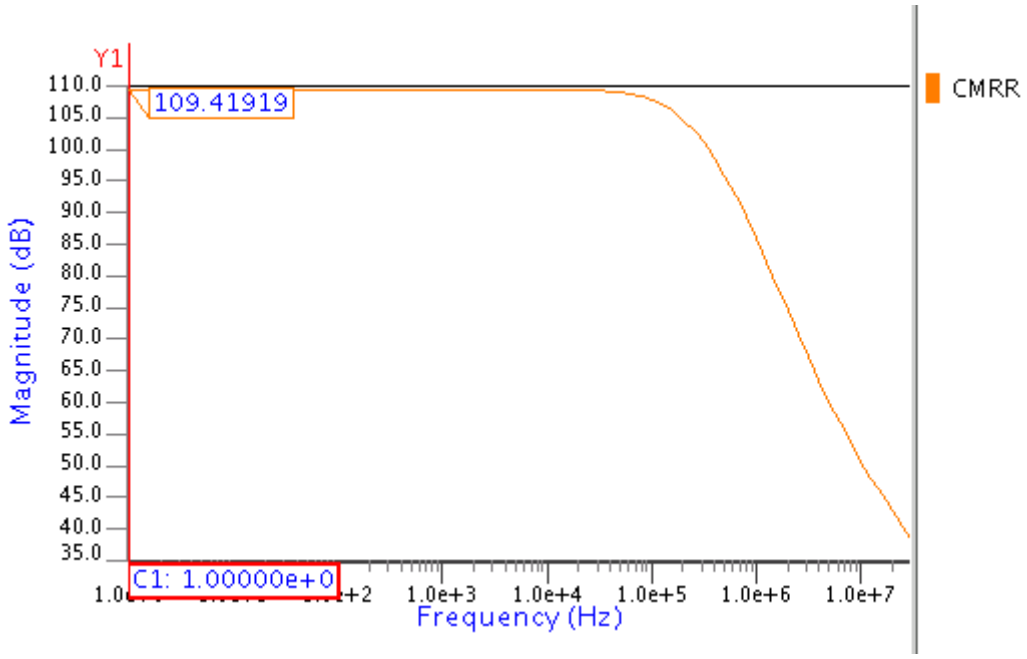


Figure 5.7 Post layout simulation – Common Mode Rejection Ratio

5.5.6 POWER SUPPLY REJECTION RATIO

POSITIVE PSRR

It comes out as 97.3452dB which is slightly less than the schematic simulation.

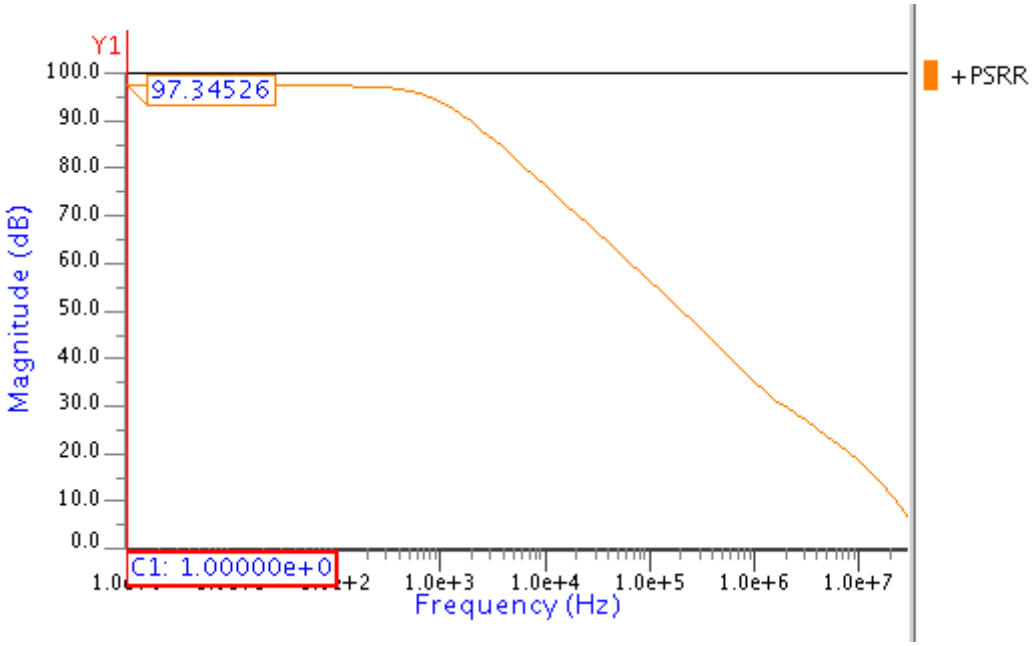


Figure 5.8 Post layout simulation – Positive PSRR

NEGATIVE PSRR

It comes out as 109.4191dB which is slightly less than the schematic simulation.

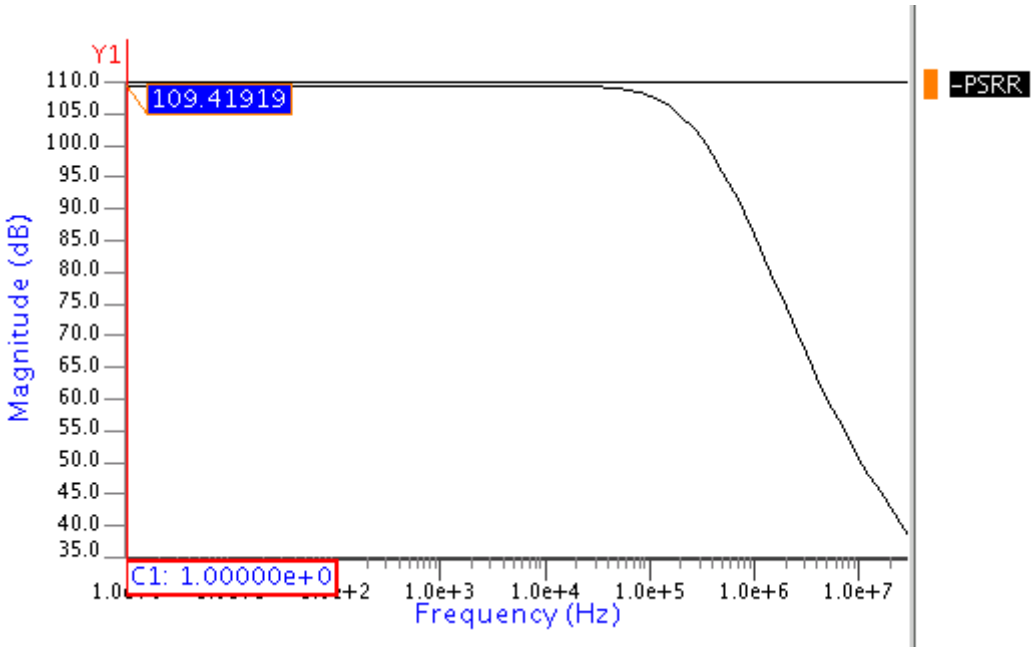


Figure 5.9 Post layout simulation – Negative PSRR

5.5.7 NOISE ANALYSIS

The Input Refereed Noise comes out to be 382.79 nV/$\sqrt{Hz}$ at 1 Hz, 123.44 nV/$\sqrt{Hz}$ at 10 Hz and 30.89 nV/$\sqrt{Hz}$ at 1 KHz which is similar to the schematic simulation.

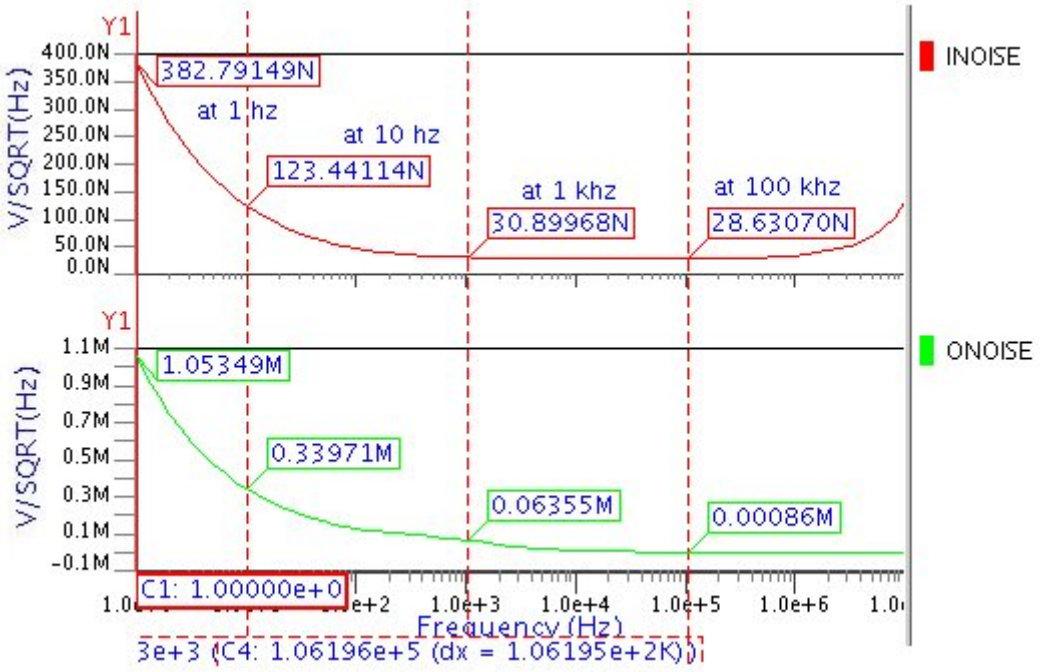


Figure 5.10 Post layout simulation – Noise analysis

5.5.8 EFFECT OF TEMPERATURE VARIATION ON NOISE

These results are also similar to the schematic simulation. For temperature variation of range -20^{o} C to 70^{o} C, overall variations in noise is 22 nV at frequency 1 Hz.

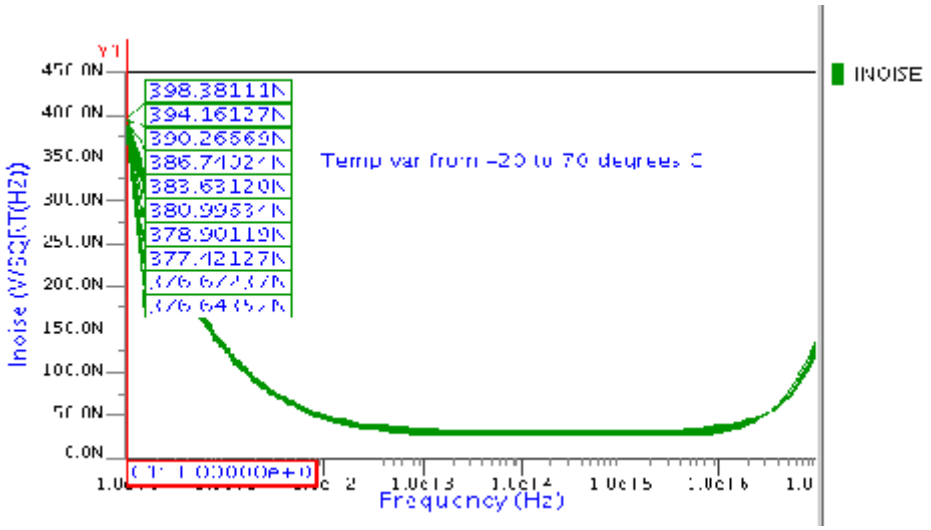


Figure 5.11 Post layout simulation – Noise with temperature variation

5.5.9 COMPARISON OF SCHEMATIC AND POSTLAYOUT RESULTS

These results are compared in the Table 5.1 shown below. It can be concluded from the comparison of results, designed circuit meets the required specifications of the application.

Table 5.1 Schematic and post layout result comparison

Specification parameters	**Schematic Results**	**Post layout Results**
Unity Gain Bandwidth (UGB)	4.8 MHz	1.475 MHz
F_{3dB} Frequency	1.32 KHz	1.17 KHz
Low Frequency Gain	68.80 dB	68.79 dB
Phase Margin	56.45 deg	39.05 deg
Power Consumption	31.26 µW	31.17 µW
Slew Rate	806.2 mV/µs, 2.61V/µs	653.4 mV/µs, 137.7 mV/µs
Settling Time (10%)	3.378 µs	3.845 µs
+PSRR / -PSRR	99.85 dB / 111.2495 dB	97.345 dB / 109.41 dB
CMRR	109.4173 dB	109.4191 dB
Total Input Refereed Noise at 1 Hz at 10 Hz at 1 KHz	 382 .68 nV/√Hz 123.68 nV/√Hz 30.75 nV/√Hz	 382 .79 nV/√Hz 123.44 nV/√Hz 30.89 nV/√Hz

Chapter 6

CONCLUSION AND FUTURE SCOPE

6.1 CONCLUSION

In the present thesis work a two stage Low Power Low Noise Amplifier has been designed and simulated. Simulation and post layout simulation results have been verified the design for the targeted applications. It shows this design is efficient for use in biomedical instruments like EEG and ECG systems.

As the noise and power are the two main constraints in analog / mixed signal circuits. PMOS input transistors and weak inversion topology is used for low power and low noise. PMOS transistors as an input stage driver transistor reduce the flicker noise and subthreshold operation reduces the power and noise both.

It can be used for the recording of biopotential signals having frequency up to 1.17 KHz. Circuit gain is 68.79 dB therefore it is efficient to amplify the low biopotencial signals (≈ μV range). Common Mode Rejection Ratio of this design is 109.41 dB. Total Input Refereed Noise obtained by this design is 382.79 nV/$\sqrt{Hz}$ at 1 Hz, 123.44 nV/$\sqrt{Hz}$ at 10 Hz and 30.85 nV/$\sqrt{Hz}$ at 1 KHz which is less in comparison of previous work done [1]-[6], [36]. Thus low noise makes it more efficient for recording the low amplitude signals. Power dissipation of circuit is 31.17 μW. This makes the design portable that is a small battery can carry on work for the long time.

6.2 FUTURE SCOPE

Due to the nature of the wide research topic, there are still several Areas of improvement for future work in this opamp. A filter circuit can be implemented at the input for flexibility of the design to reject the large dc potential produced by the electrode (which detects the signals). Bandwidth, Slew Rate and Settling Time can be improved further.

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APPENDIX

A.1 SOURCE NETLIST

```
* LVS netlist generated with ICnet by 'anilesh' on Wed Jun 17 2009 at 10
*
* Component pathname : /home/anilesh/anilesh/LAYOUTSHEMATIC
*
.subckt LAYOUTSHEMATIC  VOUT GND VB VDD VIN1 VIN2

        MN2 N$1 N$1 GND GND n L=10.4u W=1.4u
        MP3 x VB VDD VDD p L=0.7u W=10.5u
        C1 N$5 N$2 notchedrow 1500f
        MN3 VOUT N$5 GND GND n L=2.8u W=1.4u
        C2 VOUT GND notchedrow 5000f
        MP4 VOUT VB VDD VDD p L=0.7u W=15.4u
        MN1 N$5 N$1 GND GND n L=10.4u W=1.4u
        MP1 N$1 VIN1 x VDD p L=1.4u W=140u
        MP5 VOUT GND N$2 VDD p L=14u W=4.2u
        MP2 N$5 VIN2 x VDD p L=1.4u W=140u
.ends LAYOUTSHEMATIC
```

A.2 LVS REPORT

```
        ##################################################
        ##                                              ##
        ##         C A L I B R E    S Y S T E M         ##
        ##                                              ##
        ##             L V S   R E P O R T              ##
        ##                                              ##
        ##################################################


REPORT FILE NAME:          layout.lvs.report
LAYOUT NAME:               layout.calibre.gds
SOURCE NAME:
/home/anilesh/anilesh/LAYOUTSHEMATIC/LAYOUTSHEMATIC.src.net
('LAYOUTSHEMATIC')
```

```
RULE FILE:                /home/anilesh/anilesh/_tsmc035.rules_
LVS MODE:                 Mask
RULE FILE NAME:           /home/anilesh/anilesh/_tsmc035.rules_
CREATION TIME:            Fri Jun 12 11:57:41 2009
CURRENT DIRECTORY:        /home/anilesh/anilesh
USER NAME:                anilesh
CALIBRE VERSION:        v2006.2_30.26    Fri Jul 7 22:37:10 PDT 2006

****************************************************************
                    OVERALL COMPARISON RESULTS
****************************************************************


                        #       ###################       _   _
                      #         #                 #       *   *
                    #   #       #     CORRECT     #         |
                     # #        #                 #       \___/
                      #         ###################

----------------------------------------------------------------

INITIAL NUMBERS OF OBJECTS
--------------------------

                Layout    Source          Component Type
                ------    ------          --------------
 Ports:              6         6
 Nets:              22        10    *
 Instances:          3         3          MN (4 pins)
                     9         5    *     MP (4 pins)
                     2         2          C (2 pins)
                ------    ------
 Total Inst:        14        10

NUMBERS OF OBJECTS AFTER TRANSFORMATION
---------------------------------------
                Layout    Source          Component Type
                ------    ------          --------------
 Ports:              6         6
 Nets:              10        10
 Instances:          3         3          MN (4 pins)
                     5         5          MP (4 pins)
                     2         2          C (2 pins)
                ------    ------
 Total Inst:        10        10


****************************************************************
                    INFORMATION AND WARNINGS
****************************************************************


                  Matched    Matched     Unmatched    Unmatched
Component
                   Layout    Source       Layout       Source    Type
                  -------    -------    ---------    --------    ---
 Ports:              6          6           0           0
 Nets:              10         10           0           0
```

```
 Instances:          3          3          0          0    MN(N)
                     5          5          0          0    MP(P)
                     2          2          0          0
C(NOTCHEDROW)
                  -------    -------    ---------    ---------
 Total Inst:         10         10          0          0

o Statistics:

   12 isolated layout nets were deleted.
   6 layout mos transistors were reduced to 2.
   4 mos transistors were deleted by parallel reduction.

o Isolated Layout Nets:

 (Layout nets which are not connected to any instances or ports).

11(0.500,28.500)  12(2.500,-235.500)  13(15.500,-235.500)  14(28.500,-
235.500)
15(41.500,-235.500)      16(54.500,-235.500)      17(67.500,-235.500)
18(75.000, 28.500)
19(100.500,-22.000)       20(2.000,-304.500)       21(60.000,-304.500)
22(68.500,-272.500)

o Initial Correspondence Points:

   Ports:        VDD VOUT GND VIN2 VIN1 VB

*********************************************************************
                              SUMMARY
*********************************************************************

Total CPU Time:      0 sec
Total Elapsed Time:  0 sec
```

A.3 PEX REPORT

```
* File: layout.pex.netlist
* Created: Fri Jun 12 12:02:07 2009
* Program "Calibre xRC"
* Version "v2006.2_30.26"
*
.include "layout.pex.netlist.pex"
.subckt LAYOUTSHEMATIC GND VOUT VIN1 VIN2 VB VDD
*
* GND GND
* VDD VDD
* VB  VB
* VIN2      VIN2
* VIN1      VIN1
* VOUT      VOUT
```

```
MN2  N_N$1_MN2_d  N_N$1_MN2_g  N_GND_MN2_s  N_GND_MN2_b  n  L=1.04e-05
W=1.4e-06
+ AD=1.54e-12 AS=1.68e-12
MN1  N_N$5_MN1_d  N_N$1_MN1_g  N_GND_MN1_s  N_GND_MN2_b  n  L=1.04e-05
W=1.4e-06
+ AD=1.54e-12 AS=1.68e-12
MN3  N_VOUT_MN3_d  N_N$5_MN3_g  N_GND_MN3_s  N_GND_MN2_b  n  L=2.8e-06
W=1.4e-06
+ AD=1.54e-12 AS=1.54e-12
MP1__1 N_N$1_MP1__1_d N_VIN1_MP1__1_g N_x_MP1__1_s N_VDD_MP1__1_b p
L=1.4e-06
+ W=4.7e-05 AD=5.17e-11 AS=5.64e-11
MP3  N_x_MP3_d  N_VB_MP3_g  N_VDD_MP3_s  N_VDD_MP1__1_b  p  L=7e-07
W=1.05e-05
+ AD=1.155e-11 AS=1.155e-11
MP2__1 N_N$5_MP2__1_d N_VIN2_MP2__1_g N_x_MP2__1_s N_VDD_MP1__1_b p
L=1.4e-06
+ W=4.7e-05 AD=5.64e-11 AS=5.64e-11
MP2__2 N_N$5_MP2__2_d N_VIN2_MP2__2_g N_x_MP2__2_s N_VDD_MP1__1_b p
L=1.4e-06
+ W=4.7e-05 AD=5.64e-11 AS=5.64e-11
MP1__2 N_N$1_MP1__2_d N_VIN1_MP1__2_g N_x_MP1__2_s N_VDD_MP1__1_b p
L=1.4e-06
+ W=4.7e-05 AD=5.64e-11 AS=5.64e-11
MP1__3 N_N$1_MP1__3_d N_VIN1_MP1__3_g N_x_MP1__3_s N_VDD_MP1__1_b p
L=1.4e-06
+ W=4.7e-05 AD=5.64e-11 AS=5.64e-11
MP2__3 N_N$5_MP2__3_d N_VIN2_MP2__3_g N_x_MP2__3_s N_VDD_MP1__1_b p
L=1.4e-06
+ W=4.7e-05 AD=5.17e-11 AS=5.64e-11
MP4  N_VOUT_MP4_d  N_VB_MP4_g  N_VDD_MP4_s  N_VDD_MP1__1_b  p  L=7e-07
W=1.54e-05
+ AD=1.694e-11 AS=1.694e-11
MP5 N_VOUT_MP5_d N_GND_MP5_g N_N$2_MP5_s N_VDD_MP1__1_b p L=1.4e-05
W=4.2e-06
+ AD=4.62e-12 AS=4.62e-12
C1 N_N$5_C1_pos N_N$2_C1_neg 1.4952p
C2 N_VOUT_C2_pos N_GND_C2_neg 5.00964p
*
.include "layout.pex.netlist.LAYOUT.pxi"
*
.ends
*
*
```

A.4 DC ANALYSIS RESULTS

NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE
N$16	1.7269	N$8	1.0084	VB	2.5000
VDD	3.3000	VIN1	1.6500	VIN2	1.6500
VO	1.0084	VOUT	1.7269	X	2.4390

VOLTAGE SOURCE CURRENT

NAME	CURRENT	VOLTAGE	POWER
V3	0.0000	0.0000	0.0000
V4	0.0000	2.5000	0.0000
V2	-9.4737U	3.3000	-31.2631U
V1	0.0000	1.6500	0.0000

TOTAL POWER DISSIPATION: 31.2631U WATTS

OPERATING POINT INFORMATION TEMPERATURE = 27.000 DEG C

	M3	**M8**	**M4**
MODEL	N	N	N
ID	1.6548U	6.1640U	1.6548U
VGS	1.0084	1.0084	1.0084
VDS	1.0084	1.7269	1.0084
VBS	0.0000	0.0000	0.0000
VTH	571.5816M	578.2064M	571.5816M
VDSAT	346.2003M	335.4970M	346.2003M
GM	7.1558U	26.5632U	7.1558U
GDS	24.8378N	110.3060N	24.8378N
RON	40.2613MEG	9.0657MEG	40.2613MEG
GMB	2.1384U	7.9556U	2.1384U
Cdd	377.7878A	363.1731A	377.7878A

Cdg	-19.4088F	-5.4103F	-19.4088F
Cds	25.2740F	6.7038F	25.2740F
Cdb	-6.2431F	-1.6566F	-6.2431F
Cgd	-382.6455A	-363.3021A	-382.6455A
Cgg	45.4774F	12.7759F	45.4774F
Cgs	-42.7469F	-11.8343F	-42.7469F
Cgb	-2.3479F	-578.2911A	-2.3479F
Csd	15.1362A	0.5215A	15.1362A
Csg	-19.4088F	-5.4103F	-19.4088F
Css	25.6367F	7.0664F	25.6367F
Csb	-6.2431F	-1.6566F	-6.2431F
Cbd	-10.2784A	-0.3924A	-10.2784A
Cbg	-6.6599F	-1.9554F	-6.6599F
Cbs	-8.1638F	-1.9358F	-8.1638F
Cbb	14.8340F	3.8916F	14.8340F
PHI	855.3281M	855.3281M	855.3281M
VBI	1.0136	1.0136	1.0136
Region	saturation	saturation	saturation
VTH_D	436.7777M	430.1529M	436.7777M

	M5	**M2**	**M7**	**M6**	**M1**
MODEL	P	P	P	P	P
ID	-3.3097U	-1.6548U	-6.1640U	-3.2095P	-1.6548U
VGS	-800.0000M	-788.9950M	-800.0000M	-1.7269	-788.9950M
VDS	-861.0050M	-1.4306	-1.5731	-144.8170N	-1.4306
VBS	0.0000	861.0050M	0.0000	1.5731	861.0050M
VTH	-756.1560M	-871.8490M	-747.9646M	-988.3124M	-871.8490M
VDSAT	-89.4777M	-52.1063M	-94.6554M	-688.1284M	-52.1063M
GM	54.8532U	38.5463U	97.4155U	1.9831P	38.5463U
GDS	759.2531N	264.1594N	1.1736U	11.2313U	264.1594N
RON	1.3171MEG	3.7856MEG	852.0667K	89.0368K	3.7856MEG
GMB	11.6867U	6.0641U	20.7157U	334.3277F	6.0641U
Cdd	2.5398F	34.7363F	3.7399F	76.0086F	34.7363F
Cdg	-10.1843F	-56.4505F	-15.5515F	-125.8027F	-56.4505F

Cds	9.3815F	25.2747F	14.4846F	66.2995F	25.2747F
Cdb	-1.7371F	-3.5605F	-2.6731F	-16.5054F	-3.5605F
Cgd	-2.4847F	-34.2010F	-3.6567F	-121.5986F	-34.2010F
Cgg	24.8617F	234.8869F	37.5634F	251.7681F	234.8869F
Cgs	-19.4338F	-80.1379F	-29.7714F	-127.4192F	-80.1379F
Cgb	-2.9432F	-120.5480F	-4.1353F	-2.7503F	-120.5480F
Csd	-35.1785A	-84.2653A	-55.2044A	75.0023F	-84.2653A
Csg	-10.1843F	-56.4505F	-15.5515F	-125.8027F	-56.4505F
Css	11.9565F	60.0952F	18.2797F	67.3058F	60.0952F
Csb	-1.7371F	-3.5605F	-2.6731F	-16.5054F	-3.5605F
Cbd	-19.9343A	-450.9562A	-27.9990A	-29.4123F	-450.9562A
Cbg	-4.4932F	-121.9860F	-6.4605F	-162.7106A	-121.9860F
Cbs	-1.9042F	-5.2321F	-2.9930F	-6.1861F	-5.2321F
Cbb	6.4173F	127.6690F	9.4814F	35.7611F	127.6690F
PHI	806.2572M	806.2572M	806.2572M	806.2572M	806.2572M
VBI	989.0633M	989.0633M	989.0633M	989.0633M	989.0633M
Region	saturation	subthreshold	saturation	linear	subthreshold
VTH_D	43.8440M	-82.8540M	52.0354M	738.5401M	-82.8540M

	C2	C1
V+	1.7269	1.0084
V-	0.0000	1.7269
ID	0.0000	0.0000