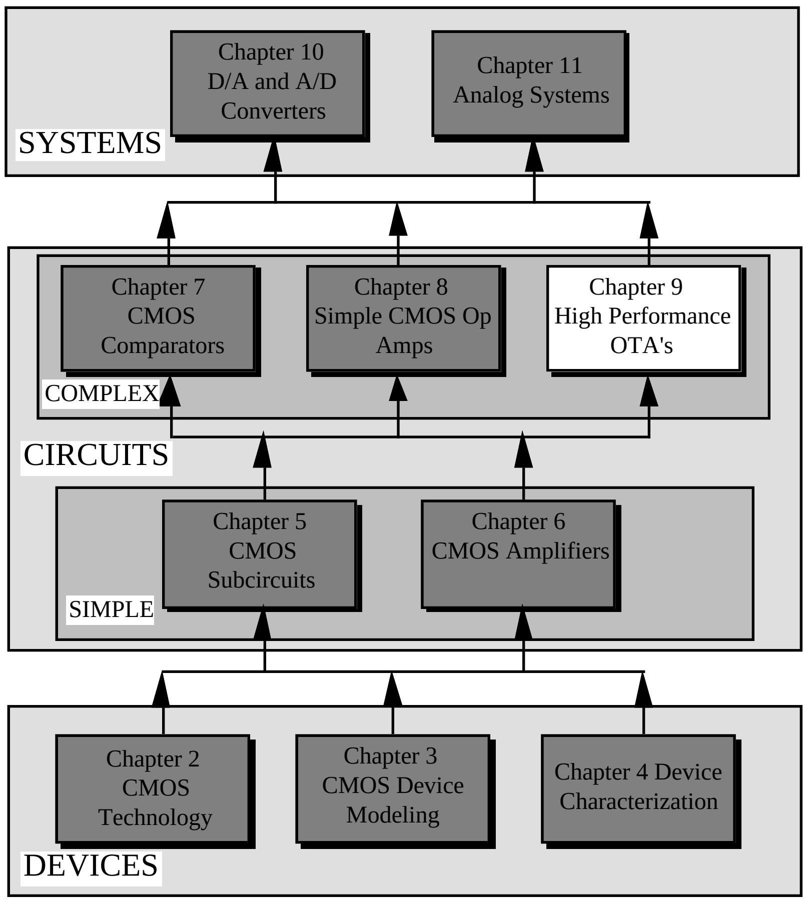
IX. HIGH PERFORMANCE CMOS AMPLIFIERS

Contents

Organization

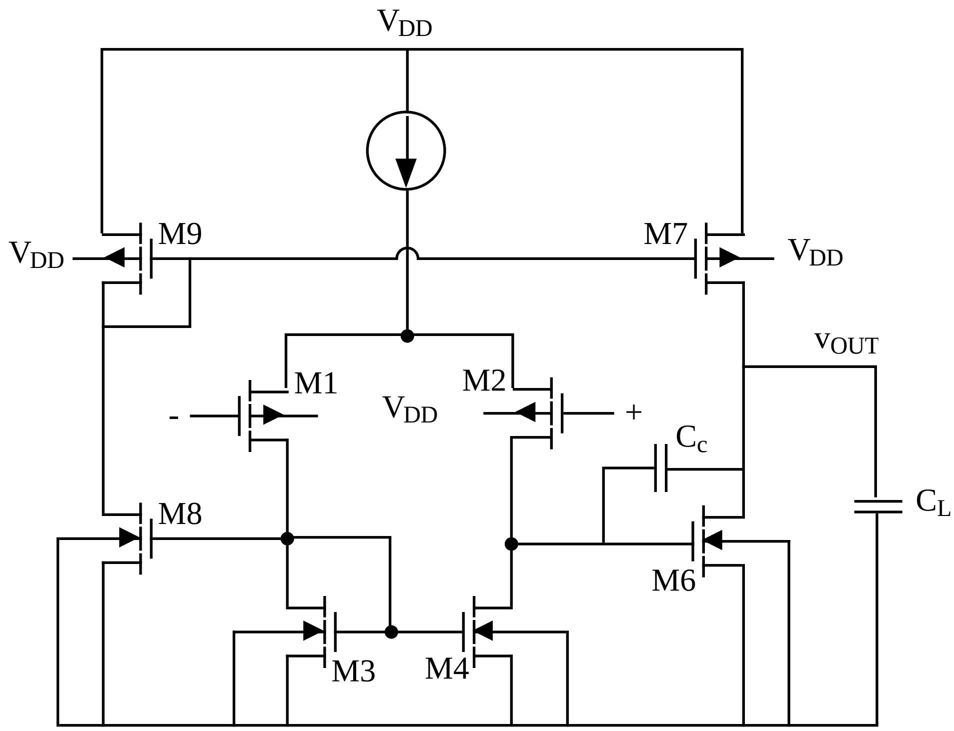


IX.1 IMPROVING THE TWO-STAGE ARCHITECTURE

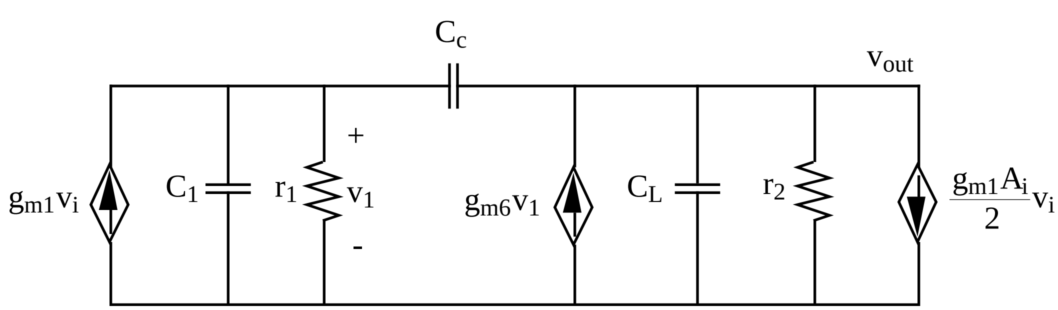
Amplifiers Using an MOS Output Stage

PUSH-PULL CMOS OTA

This amplifier is a simple extension of the seven-transistor OTA studied in Section 8.



small-signal equivalent circuit:



where $g_{m1} = g_{m2}$, $r_1 = \dfrac{1}{g_{ds2} + g_{ds4}}$, $r_2 = \dfrac{1}{g_{ds6} + g_{ds7}}$

Amplifiers Using an MOS Output Stage - Continued

Network equations:

$$[g_1 + s(C_1 + C_L)]v_1 - sC_c v_2 = g_{m1}v_i$$

$$[g_5 + sC_c]v_1 + [g_2 + s(C_c + C_L)]v_2 = \frac{g_{m1}A_I v_i}{2}$$

A_I is the current gain from M1 to M7: $A_I = \frac{i_7}{i_1}$

$$z = \frac{-g_{m6}}{\left(\frac{A_I}{2} - 1\right)C_c}$$

$$p_1 \approx \frac{-g_1 g_2}{g_{m6}C_c}$$

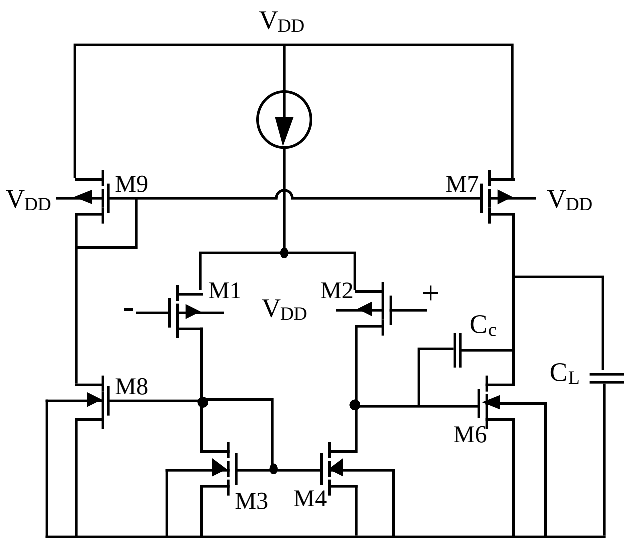
$$p_2 \approx \frac{-g_{m6}}{C_L}$$

$$A_V \approx \frac{g_{m1}g_{m6}}{g_1 g_2}$$

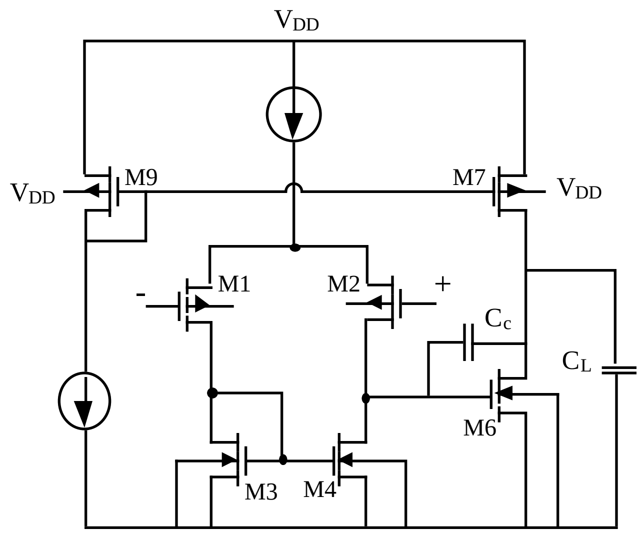
To guarantee that the zero stays in the left-half plane, $A_I > 2$

Amplifiers Using an MOS Output Stage - Continued

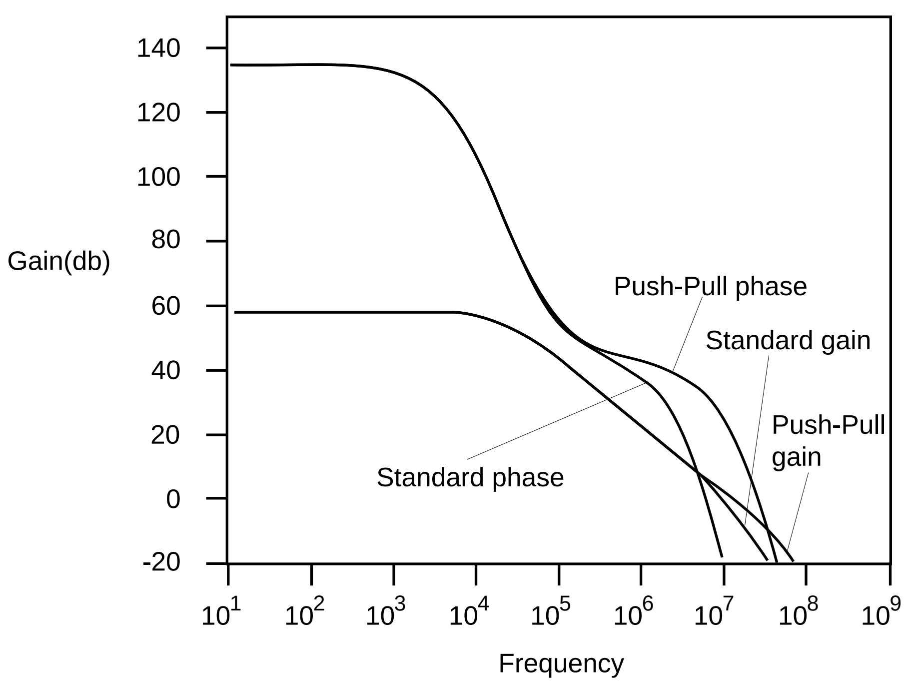
Example:



Push-Pull ($A_I \approx 3$)



Standard ($A_I = 0$)



IX.2 Two-Stage Cascode Architecture

Why Cascode Op Amps?

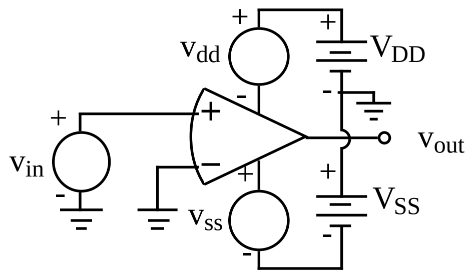
- Control the frequency behavior
- Increase PSRR
- Simplifies design

Where is the Cascode Technique Applied?

- First stage -
  - Good noise performance
  - Requires level translation to second stage
  - Requires Miller compensation
- Second stage -
  - Self compensating
  - Reduces the efficiency of the Miller compensation
  - Increases PSRR

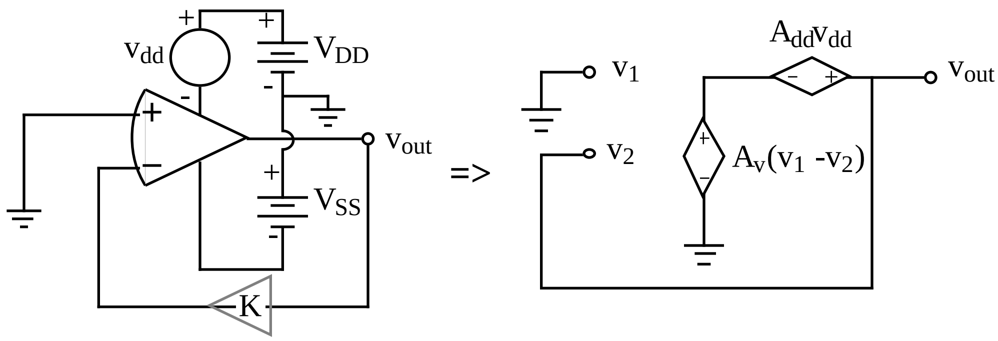
Power Supply Rejection Ratio (PSRR)

Definition:



$$PSRR^+ = \frac{A_v(v_{dd}=0)}{A_{dd}(v_{in}=0)} = \frac{\frac{v_{out}}{v_{in}}(v_{dd}=0)}{\frac{v_{out}}{v_{dd}}(v_{in}=0)}$$

Calculation of PSRR:



$$v_{out} = A_{dd}v_{dd} + A_v(v_1 - v_2) = A_{dd}v_{dd} - A_v v_{out}$$

$$v_{out}(1 + A_v) = A_{dd}v_{dd}$$

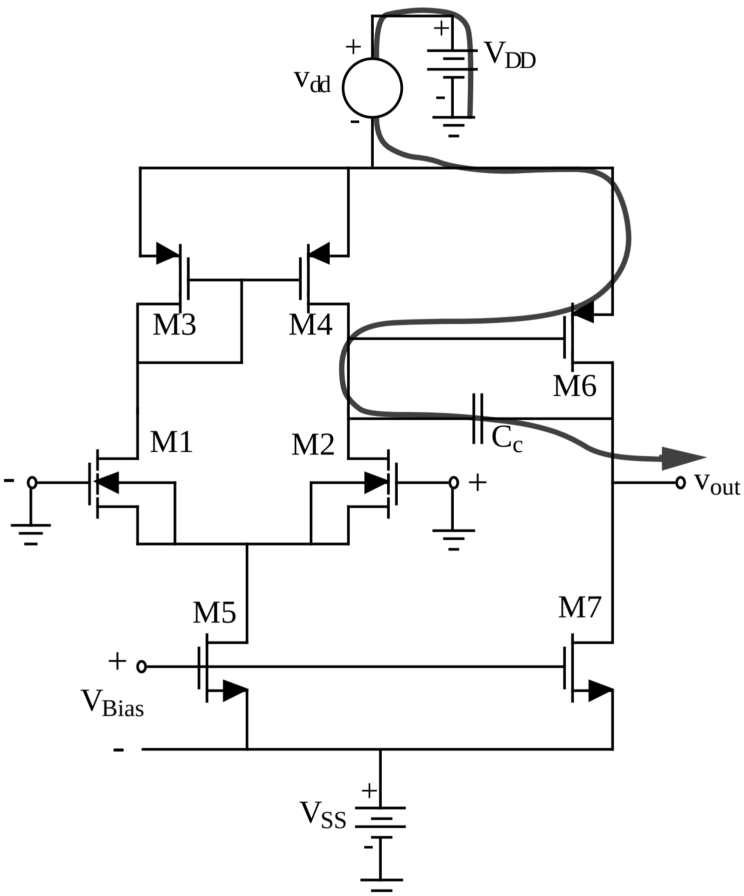
$$\frac{v_{out}}{v_{dd}} = \frac{A_{dd}}{1 + A_v} \approx \frac{A_{dd}}{A_v} = \frac{1}{PSRR^+}$$

Extends bandwidth beyond GB

↓

$$\frac{v_{out}}{v_{dd}} = \frac{KA_{dd}}{1+KA_v} \approx \frac{A_{dd}}{A_v}$$

Intuitive Interpretation of Positive PSRR for the Two-Stage OTA

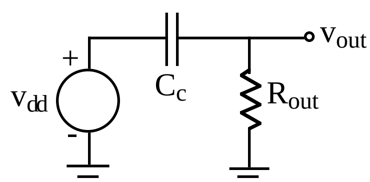


1.) The M7 current sink causes V_{GS6} to act like a battery.

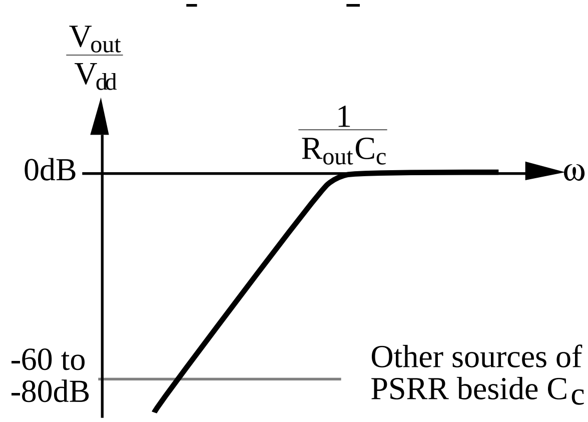
2.) Therefore, v_{dd} couples from the source to gate of M6.

3.) The path to the output is through any capacitance from gate to drain of M6.

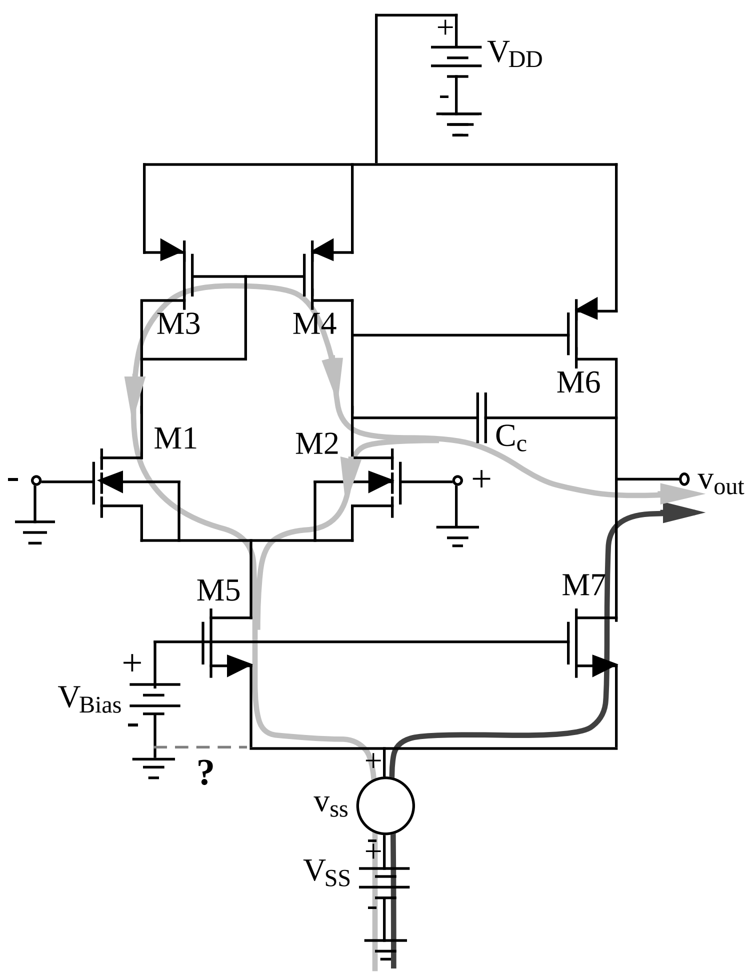
4.) Resultant circuit model-



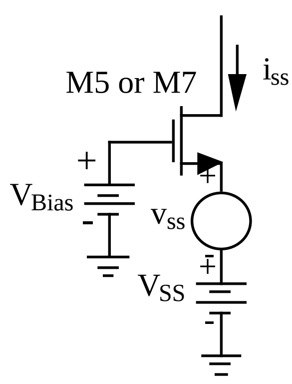
$\boxed{\text{Must reduce } C_c\text{!}}$

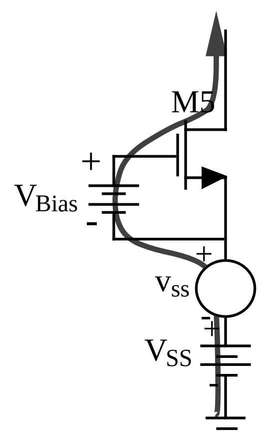


Intuitive Interpretation of the Negative PSRR for the Two-Stage OTA



Two mechanisms of v_{SS} injection:





Transconductance injection

Capacitance injection

Intuitive Interpretation of the Negative PSRR for the Two-Stage OTA - Continued

Transconductance injection:

Path through the input stage:

Not important as long as CMRR is high.

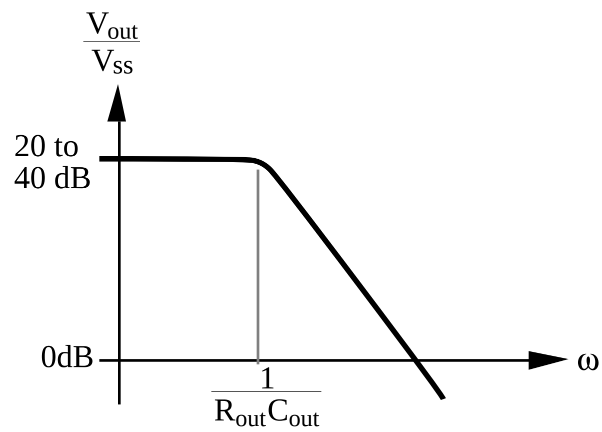
Path through the output stage:

$$v_{out} \approx i_{ss}R_{out} = g_{m7}v_{ss}R_{out}$$

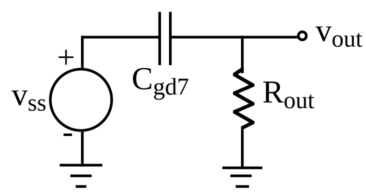
$$\frac{v_{out}}{v_{ss}} = g_{m7}R_{out}$$

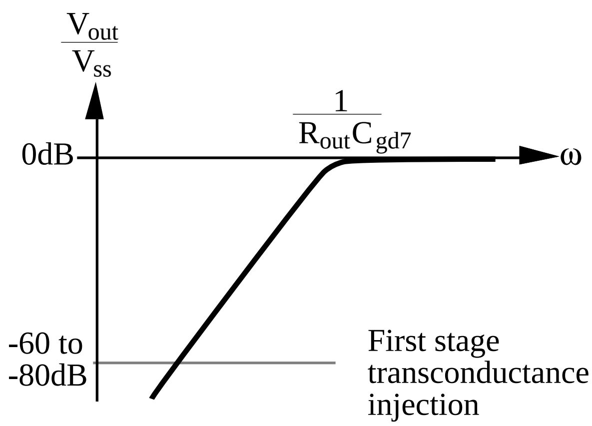
Frequency dependence -

$$R_{out} \to R_{out}\|\left(\frac{1}{sC_{out}}\right)$$



Capacitance injection:





Reduce C_{gd7}!

Problems with the two-stage OTA:

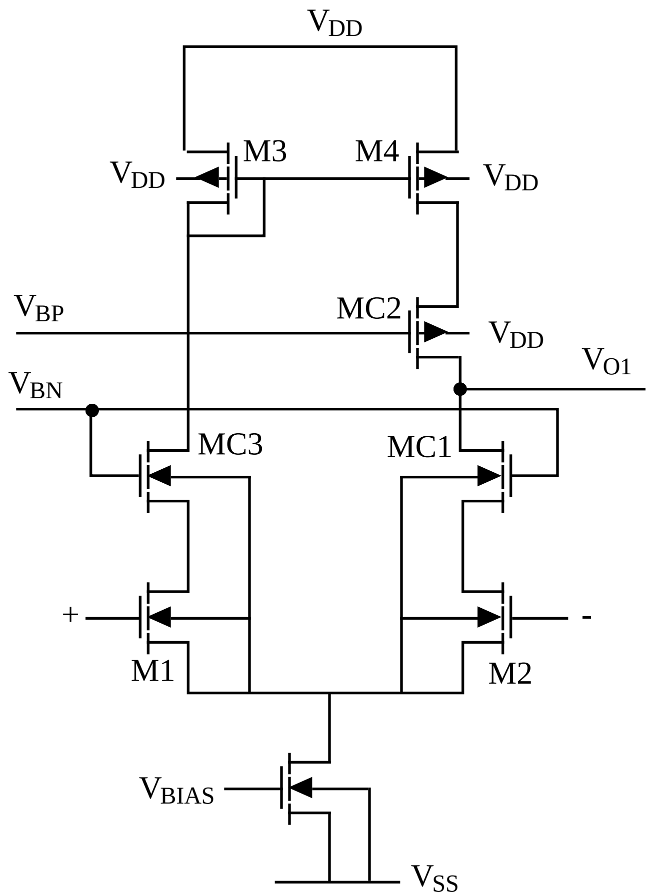
- Insufficient gain
- Poor stability for large load capacitance
- Poor PSRR

These problems can be addressed using various cascode structures.

We will consider several approaches:

- Cascoding the first stage
- Cascoding the second stage
- Folded cascode

First Stage Cascode



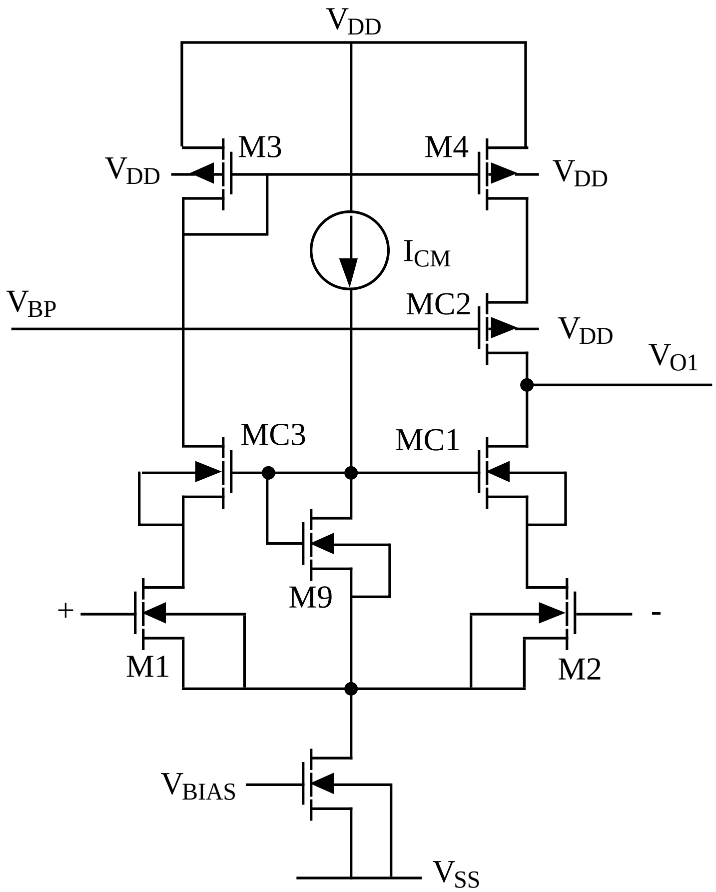
$r_{o1} \approx (g_{mc2} r_{dsc2}) r_{ds4} \parallel (g_{mc1} r_{dsc1}) r_{ds2}$

$\text{Gain} \approx g_{m2} r_{o1}$

- Overall gain increased by $\approx \dfrac{g_{mc} r_{dsc}}{2}$
- Requires voltage translation to drive next stage
- Requires additional biasing for cascode devices
- Common-mode problem at drains of M1 and M2

First Stage Cascode - Continued

Common-mode improvement:



Common-mode circuitry (M9) maintains V_{ds} of M1 and M2

$$A_V = g_{m1} r_{o1}$$

$$r_{o1} \approx (g_{mc2} r_{dsc2}) r_{ds4} \,||\, (g_{mc1} r_{dsc1}) r_{ds2}$$

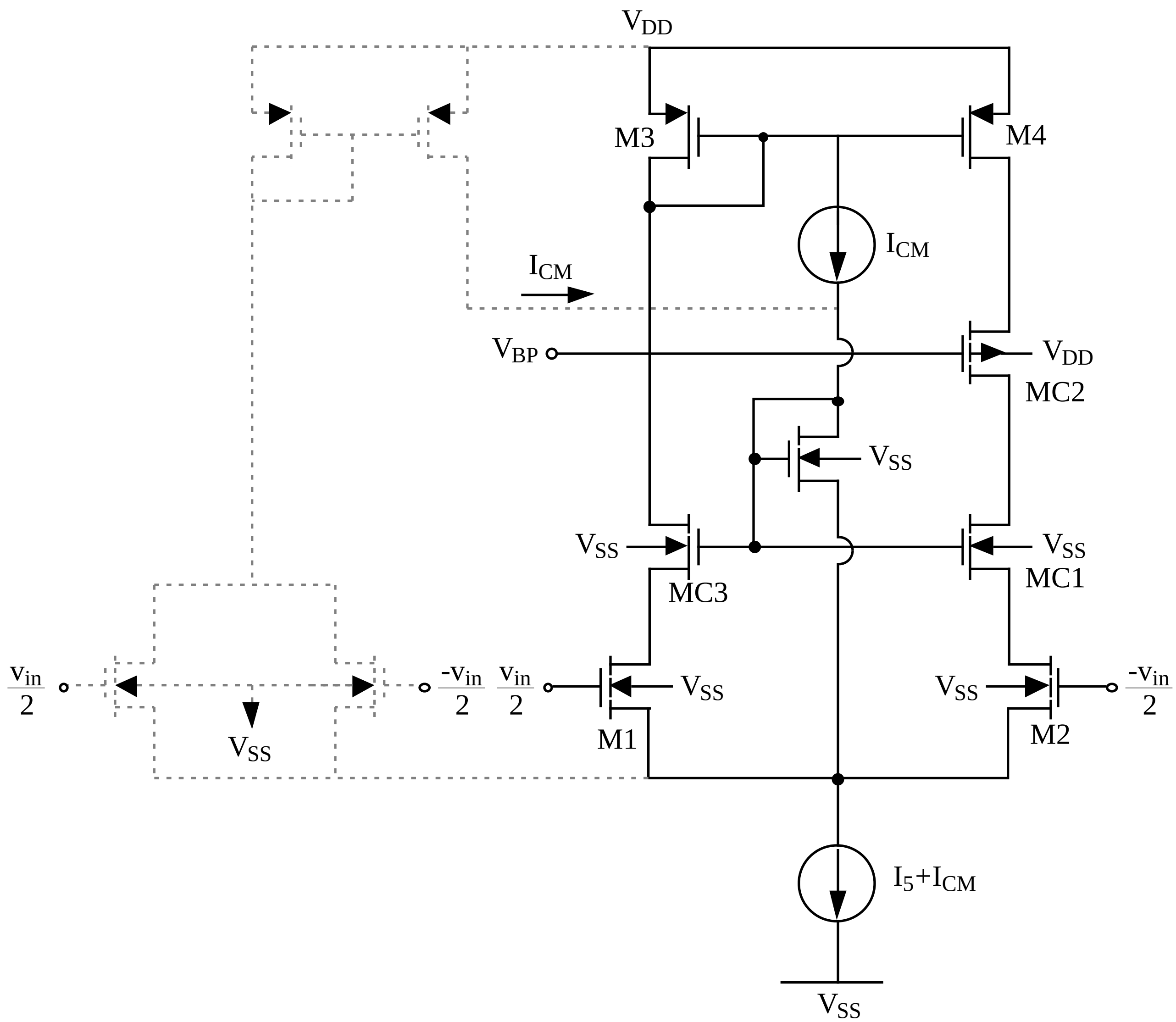
$$p_1 \approx \frac{-1}{C_L r_{o1}}$$

$$GB \approx A_V |p_1| \approx \frac{g_{m1}}{C_L}$$

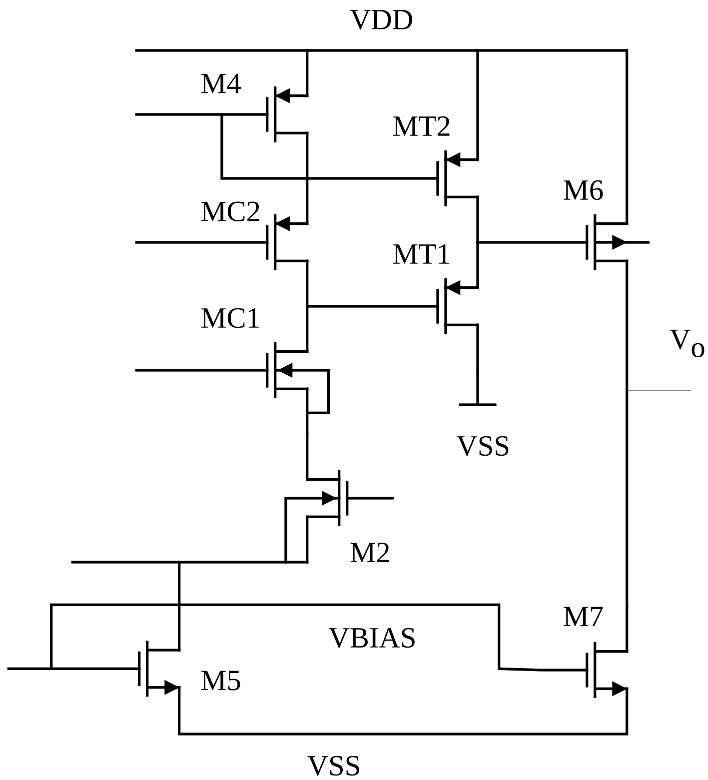
Output range of this amplifier is poor when used by itself. It needs an output stage to be practical.

First Stage Cascode - Continued

Implementation of I_{CM}

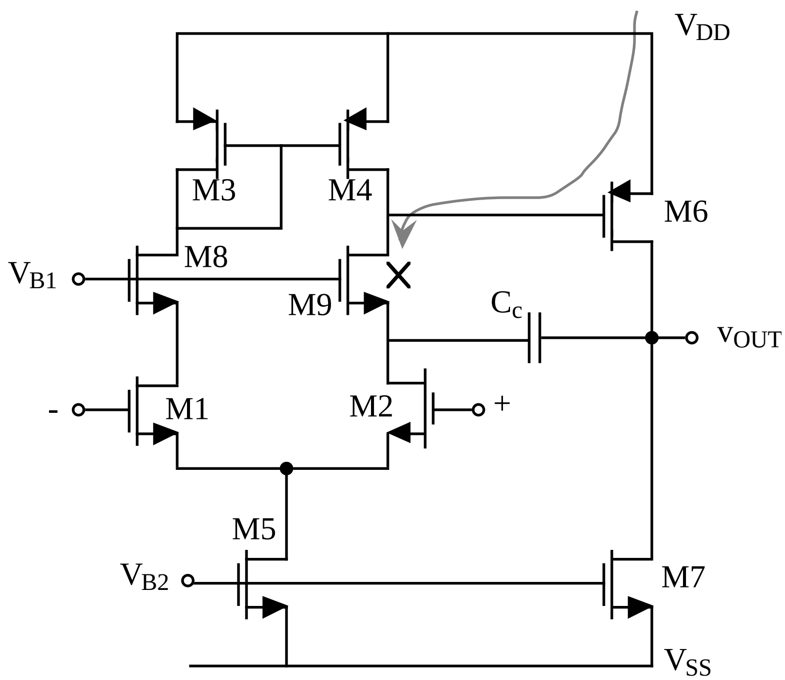


Level Translator for First Stage Cascode



Improved PSRR For Two-Stage OTA

Use cascode to reject C_c feedforward



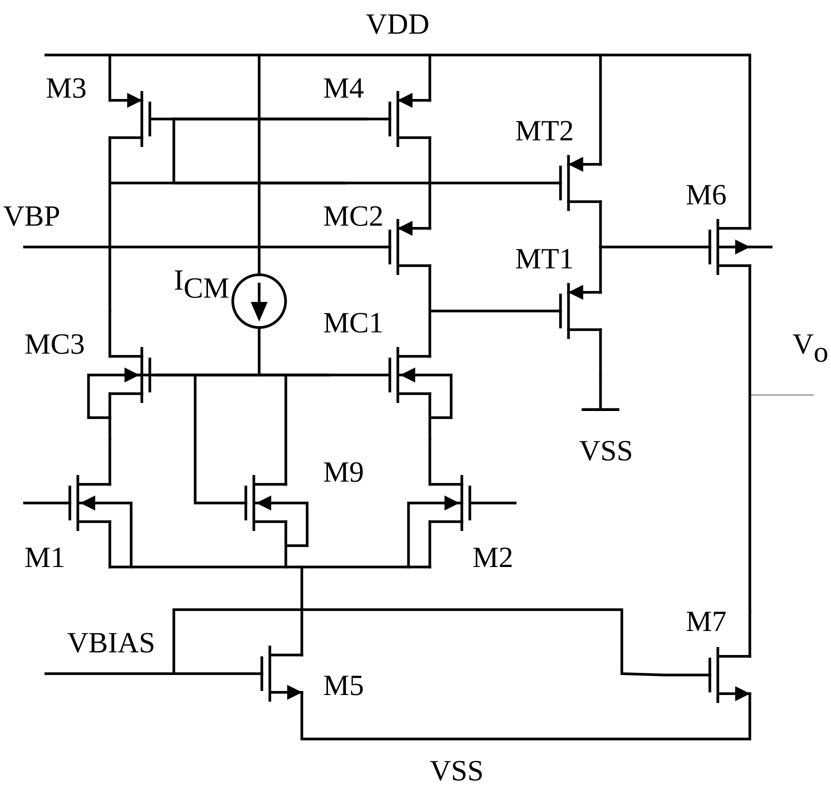
+PSRR is reduced by M9

Disadvantage -

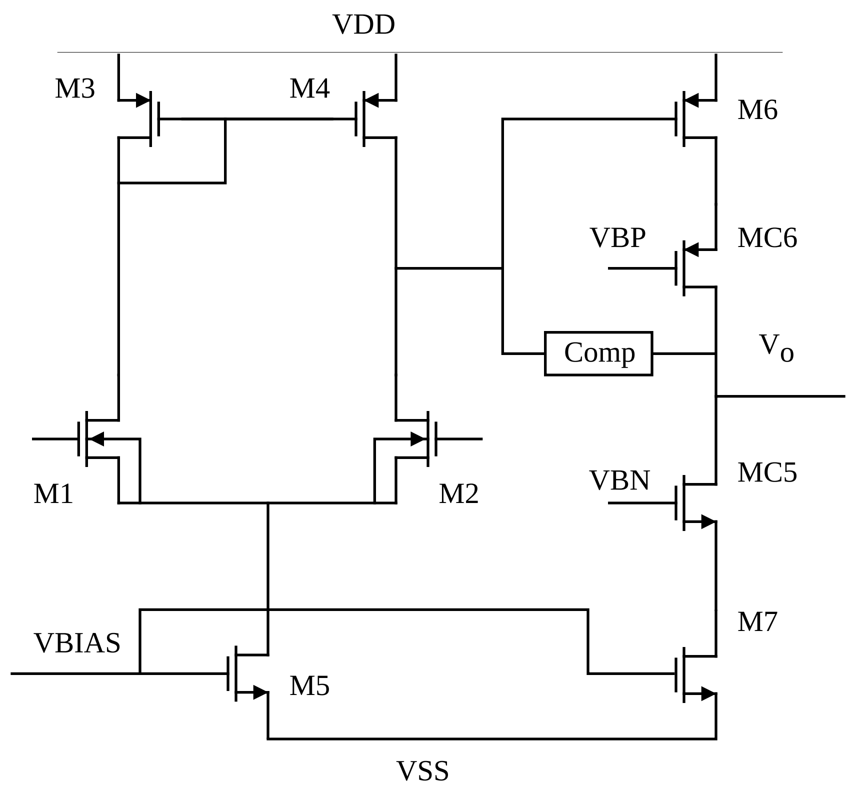
Miller pole is larger because $R_1 \approx \dfrac{1}{g_{m9}}$

positive input common mode range is restricted

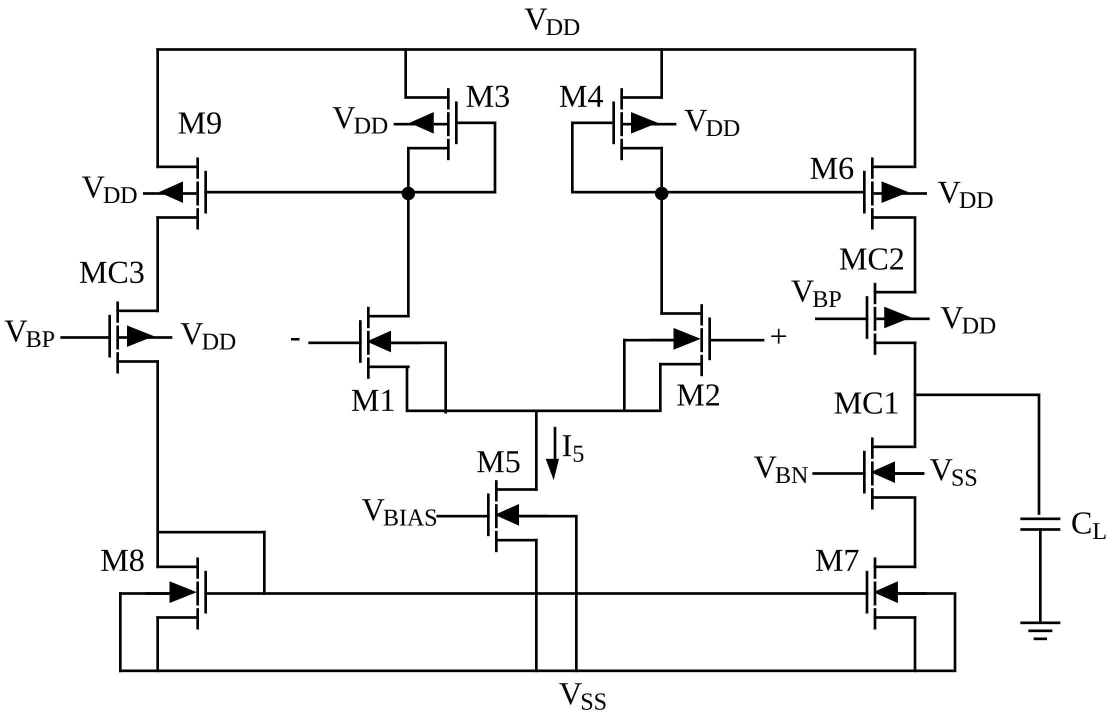
Complete Two Stage Cascode



Second Stage Cascode



LOAD COMPENSATED CASCODE AMPLIFIER



$$\left.\begin{aligned} A_{V1} &= \frac{g_{m2}}{g_{m4}} \\ A_{V2} &= \frac{1}{2}(g_{m6} + g_{m9})R_o \end{aligned}\right\} \quad A_V = \frac{g_{m2}}{2(g_{m4})}(g_{m6} + g_{m9})\, R_o$$

where

$$R_o \approx (g_{mc2}r_{dsc2})r_{ds6} \parallel (g_{mc1}r_{dsc1})r_{ds7} \text{ and } M7 = M8$$

Or,

$$A_V = \left(\frac{g_{m1}+g_{m2}}{2}\right) KR_o$$

where

$$K = \frac{W_6/L_6}{W_4/L_4} = \frac{W_9/L_9}{W_3/L_3}$$

Design Example

Pertinent design equations:

$$SR = \frac{i_{OUT}}{C_L}$$

$$A_V = \frac{g_{m2}}{2(g_{m4})}(g_{m6} + g_{m7})\, r_o$$

$$GB = \frac{g_{m2}(g_{m6} + g_{m7})}{2(g_{m4})C_L}$$

$$V_{in(max)} = V_{DD} - \sqrt{\frac{I_5}{ß_3}} - |V_{T3}|_{(max)} + V_{T1(min)}$$

$$V_{in(min)} = V_{SS} + V_{DS5} + \sqrt{\frac{I_5}{ß_1}} + V_{T1(max)}$$

Specifications:

$V_{DD} = -V_{SS} = 5V$

$SR = 5V/\mu s$ into $C_L = 50pf$

$GB = 5$ MHz

$A_V > 5000$

$CMR = \pm 3V$

Output swing = $\pm 3V$

Design Procedure

1.) Design for maximum source/sink current

$I_{source/sink} = C_L(SR) = 50pf(5V/\mu s) = 250\ \mu A$

2.) Note that -

Max. I_{OUT} (source) $= \frac{S_6}{S_4}\ I_5$

Max. I_{OUT} (Sink) = Max. I_{OUT} (source) if $S_3 = S_4$,

$S_9 = S_6$ and $S_7 = S_8$

3.) Choose $\underline{I_5 = 100\ \mu A}$

$\therefore\ \underline{S_9 = S_6 = 2.5\ S_4 = 2.5\ S_3}$

4.) Design for $\pm$ 3V output capability

a.) Negative peak

Let V_{DSC1}(sat.) = V_{DS7}(sat.) = 1V

under negative peak conditions, $I_{C1} = I_7 = 250\ \mu A$

Divide 2V equally,

$$\therefore\ 2V = \sqrt{\frac{2I_7}{K_N'S_7}} + \sqrt{\frac{2I_{C1}}{K_N'S_{C1}}} = 2\sqrt{\frac{2I_7}{K_N'S_7}} = 2\sqrt{\frac{500\ \mu A}{17\ \mu A/V^2\ S_7}}$$

$\therefore\ \underline{S_7 = S_{C1} = 29.4}$ -> $\underline{S_8 = S_7 = 29.4}$

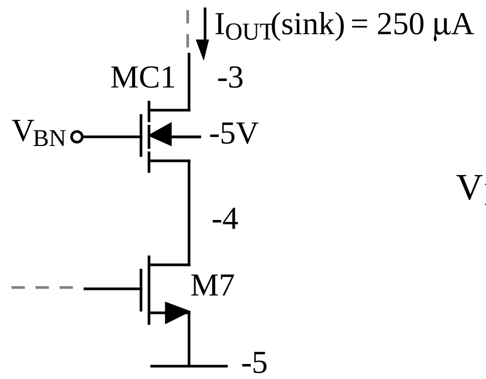
b.) Positive peak, divide voltage equally,

$$V_{SD6} = V_{SDC2} = 1V, \;\text{-->}\; 2V = \sqrt{\frac{2I_6}{K_P'S_6}} + \sqrt{\frac{2I_{C2}}{K_P'S_{C2}}} = 2\sqrt{\frac{2I_6}{K_P'S_6}}$$

$$\therefore \; \underline{S_6 = S_{C2} = 62.5} \quad \text{-->} \quad \underline{S_3 = S_4 = 25}$$

5.) Design of V_{BP} and V_{BN}

a.) V_{BN} (Assume max. I_{OUT} (sink) conditions)

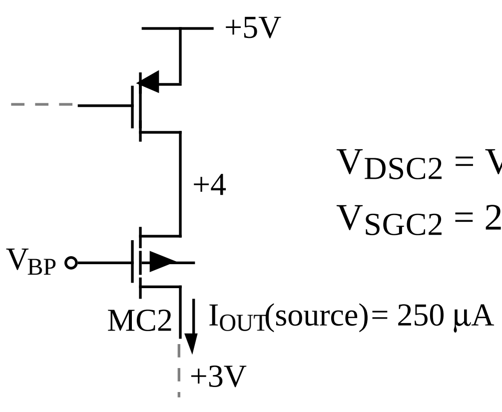


$$V_{DSC1} = V_{GSC1} - V_{TC1} \text{ (ignoring bulk effects)}$$

$$1 = V_{GSC1} - 1 \;\text{-->}\; V_{GSC1} = 2V$$

$$\therefore \; \underline{V_{BN} = -2V}$$

b.) V_{BP} (Assume max. I_{OUT} (source) conditions)



$$V_{DSC2} = V_{GSC2} - |V_{TC2}| \text{ (ignoring bulk effects)}$$

$$V_{SGC2} = 2V \qquad \therefore \; \underline{V_{BP} = +2V}$$

6.) Check max. V_{in} influence on S_3 (S_4)

$$V_{in}\,(\max) = V_{DD} - \sqrt{\frac{I_5}{ß_3}} - |V_{T03}|_{max} + V_{T1}(\min)$$

$$+3 = +5 - \sqrt{\frac{100\ \mu A}{K_P' S_3}} - 1.2 + 0.8$$

$$S_3 = \frac{100\ \mu A}{8\ \frac{\mu A}{V^2}\,(1.6V)^2} = 4.88 \quad (\text{Use } S_3 = S_4 = 25)$$

With $S_3 = 25$, V_{in} (max) = 3.89V which exceeds the specification.

7.) Find g_{m1} (g_{m2})

a.) A_V specification

$$A_V = \frac{g_{m1}}{g_{m4}}\left(\frac{g_{m6} + g_{m7}}{2}\right) R_{II}$$

$$g_{m4} = \sqrt{2I_4K_p'S_4} = 141.1\ \mu s$$

$$g_{m6} = \sqrt{2I_6K_P'S_6} = 353.5\ \mu s$$

$$g_{m7} = \sqrt{2I_7K_N'S_7} = 353.5\ \mu s$$

$$g_{mc1} = g_{m7}$$

$$g_{mc2} = g_{m6}$$

$$r_{ds6} = r_{dsc2} = \frac{1}{I_6\lambda_P} = 0.4\ M\Omega$$

$$r_{ds7} = r_{dsc1} = \frac{1}{I_7\lambda_N} = 0.8\ M\Omega$$

$$R_{II} \approx (g_{mc1}r_{dsc1}r_{ds7})\ ||\ (g_{mc2}r_{dsc2}r_{ds6}) = 45.25\ M\Omega$$

$$\therefore \left(\frac{g_{m1}}{141.1}\right)\left(\frac{707\ \mu s}{2}\right)(226.24\ M\Omega\ ||\ 56.56\ M\Omega) > 5000\ V/V$$

$$\therefore \quad g_{m1} > 44\ \mu s$$

b.) GB specification

$$GB = \frac{g_{m1}(g_{m6} + g_{m7})}{2g_{m4}}(50pF) = 10\pi\cdot 10^6 \text{ rps}$$

$$g_{m1} = \frac{(10\pi\cdot 10^6)(141.1\cdot 10^{-6})(50\cdot 10^{-12})}{707\cdot 10^{-6}/2} = 627\ \mu S$$

$$\therefore\ \underline{S_1 = S_2 = \frac{g_m{}^2}{I_5 K_N'} = 231}$$

$$A_V = \frac{g_{m1}}{g_{m4}}\left(\frac{g_{m6}+g_{m7}}{2}\right)R_{II} = \frac{627}{141.1}\left(\frac{707\mu S}{2}\right)(45.25M\Omega) = 71{,}080$$

8.) Find S_5 from V_{in} (min)

$$V_{in}\ (\min) = V_{SS} + V_{DS5} + \sqrt{\frac{I_5}{\beta_1}} + V_{T1}(\max)$$

$$-3 = -5 + V_{DS5} + \sqrt{\frac{100\ \mu A}{17\ \frac{\mu A}{V^2}\ S_1}} + 1.2$$

$$V_{DS5} = 0.8 - \sqrt{\frac{100}{(17)(231)}} = 0.8 - 0.1596 = 0.641$$

$$V_{DS5\ (sat)} = 0.641 = \sqrt{\frac{2(100\ \mu A)}{(17\ \frac{\mu A}{V^2})S_5}}$$

$$S_5 = \frac{2(100\mu A)}{17\mu A/V^2(0.641)^2} = 28.6$$

9.) V_{BIAS} -

$$I_5 = \frac{K_N'\cdot 28.6}{2}(V_{BIAS} + 5 - 1)^2 = 100\ \mu A$$

$$V_{BIAS} = 0.411 - 4 = -3.359V$$

10.) Summary of design -

$S_1 = S_2 = 231$

$S_3 = S_4 = 25$

$S_5 = 28.6$

$S_6 = S_9 = S_{C2} = S_{C3} = 62.5$

$S_7 = S_8 = S_{C1} = 29.4$

$V_{BP} = 2V$

$V_{BN} = -2V$

$V_{BIAS} = -3.359V$

11.) Check on power dissipation

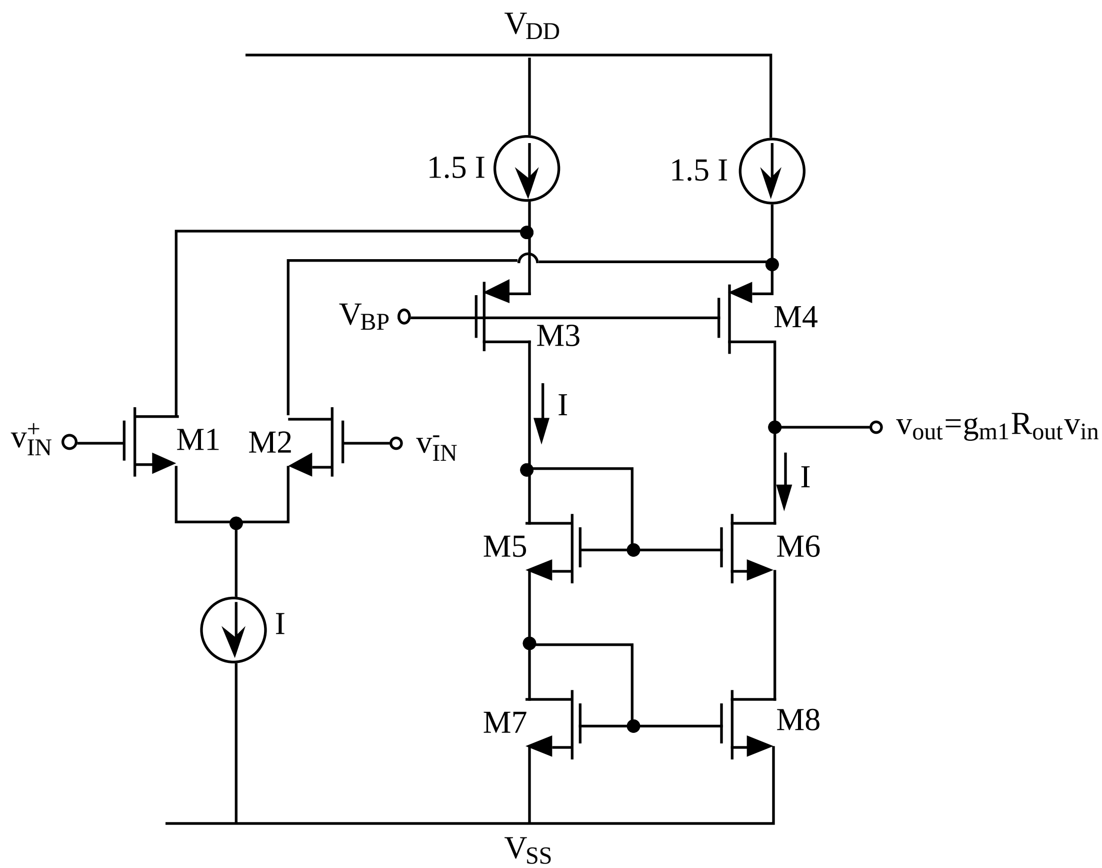
$$P_{diss} = 10(I_8 + I_5 + I_7) = 10(125\mu A + 100\mu A + 125\mu A)$$

$$= 3.5mW$$

12.) Design W's for lateral diffusion and simulate

X.3 FOLDED CASCODE ARCHITECTURE

Principle



Currents in upper current sinks must be greater than I to avoid zero current in the cascode mirror (M5-M8).

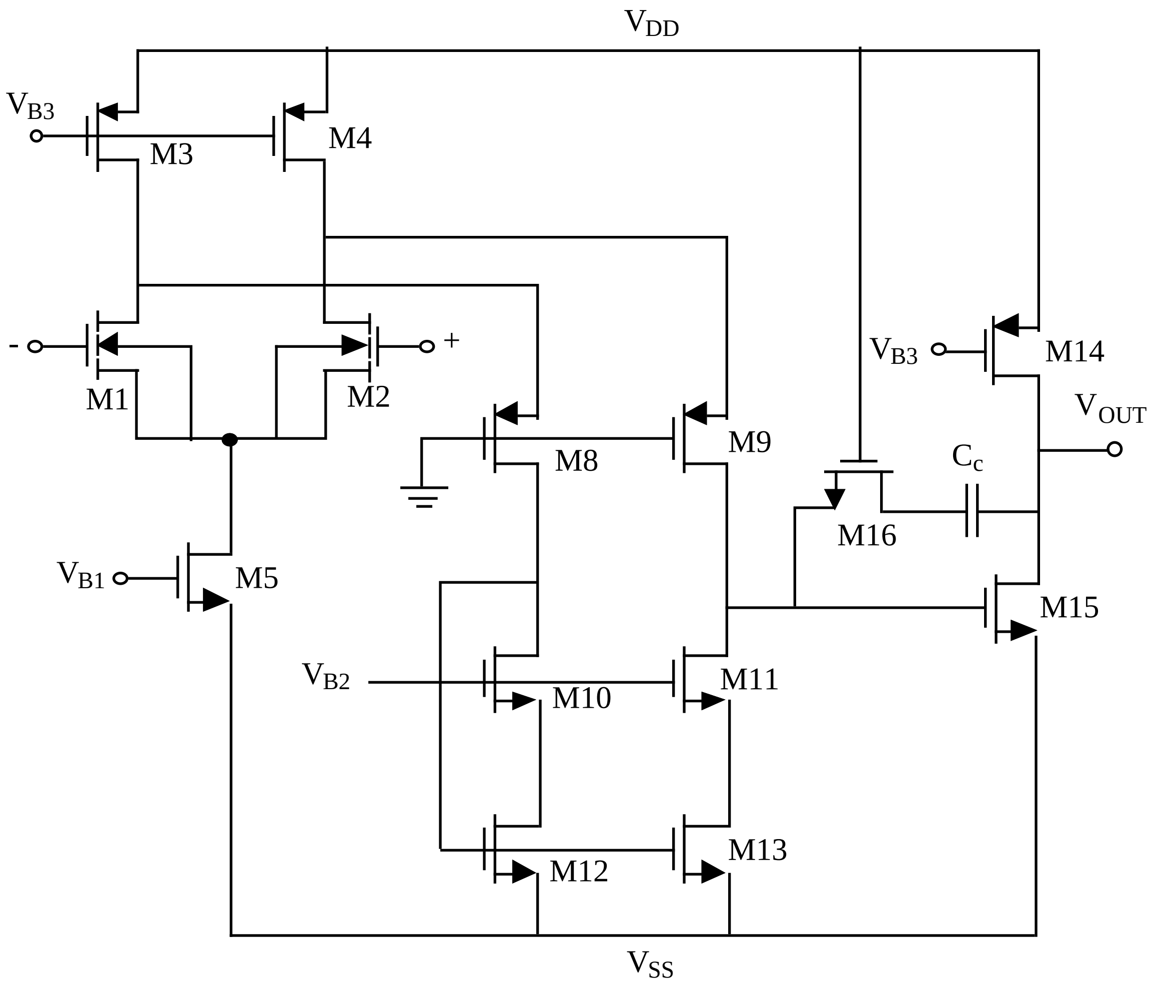
Advantages

Good input CMR.

Good frequency response.

Self compensating.

Folded Cascode OP Amp

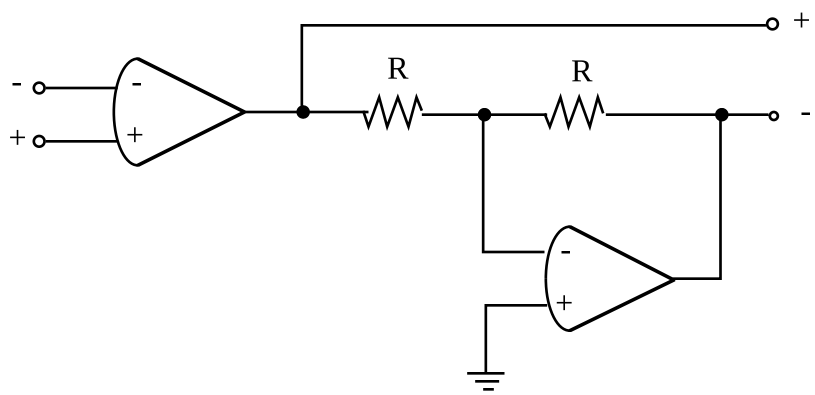


High gain, High speed, cascode amp

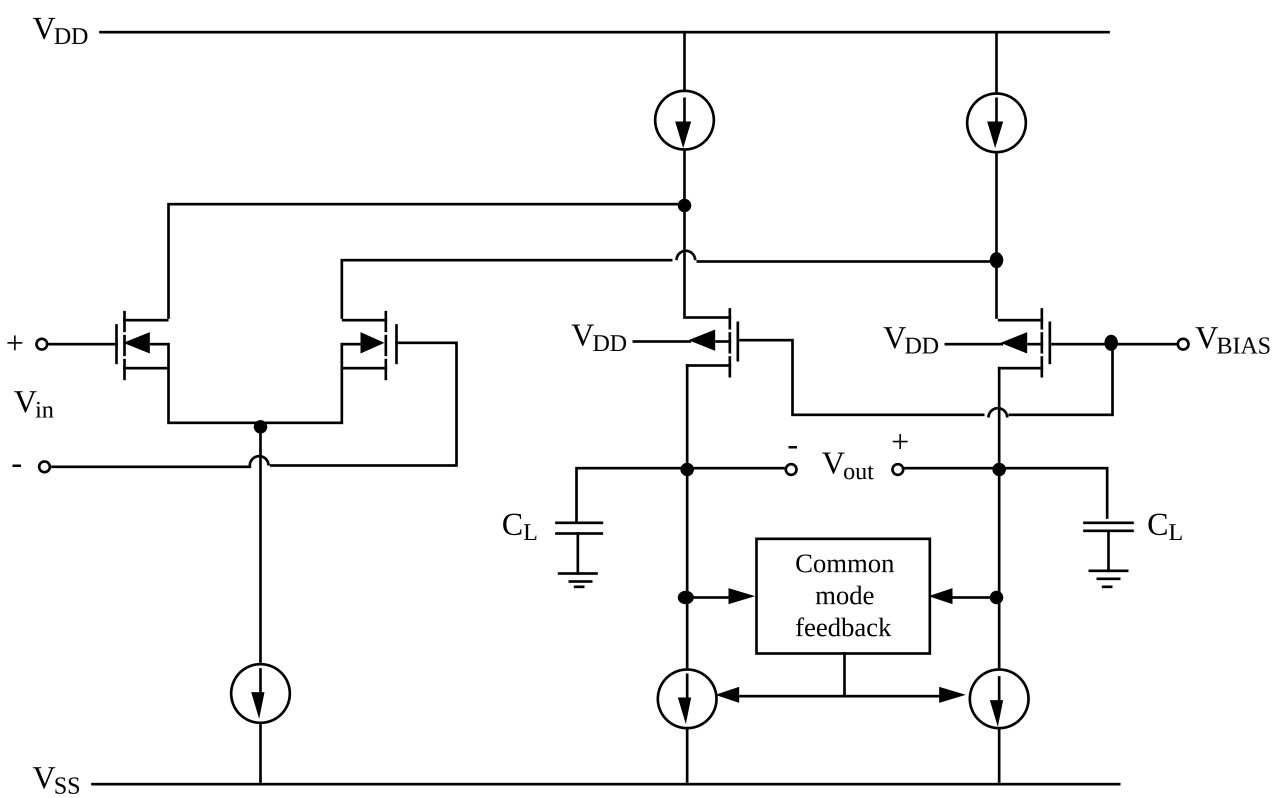
GB ≈ 10 MHz, A_{VDC} ≈ 100 dB

XI. 4 DIFFERENTIAL OUTPUT OTA'S

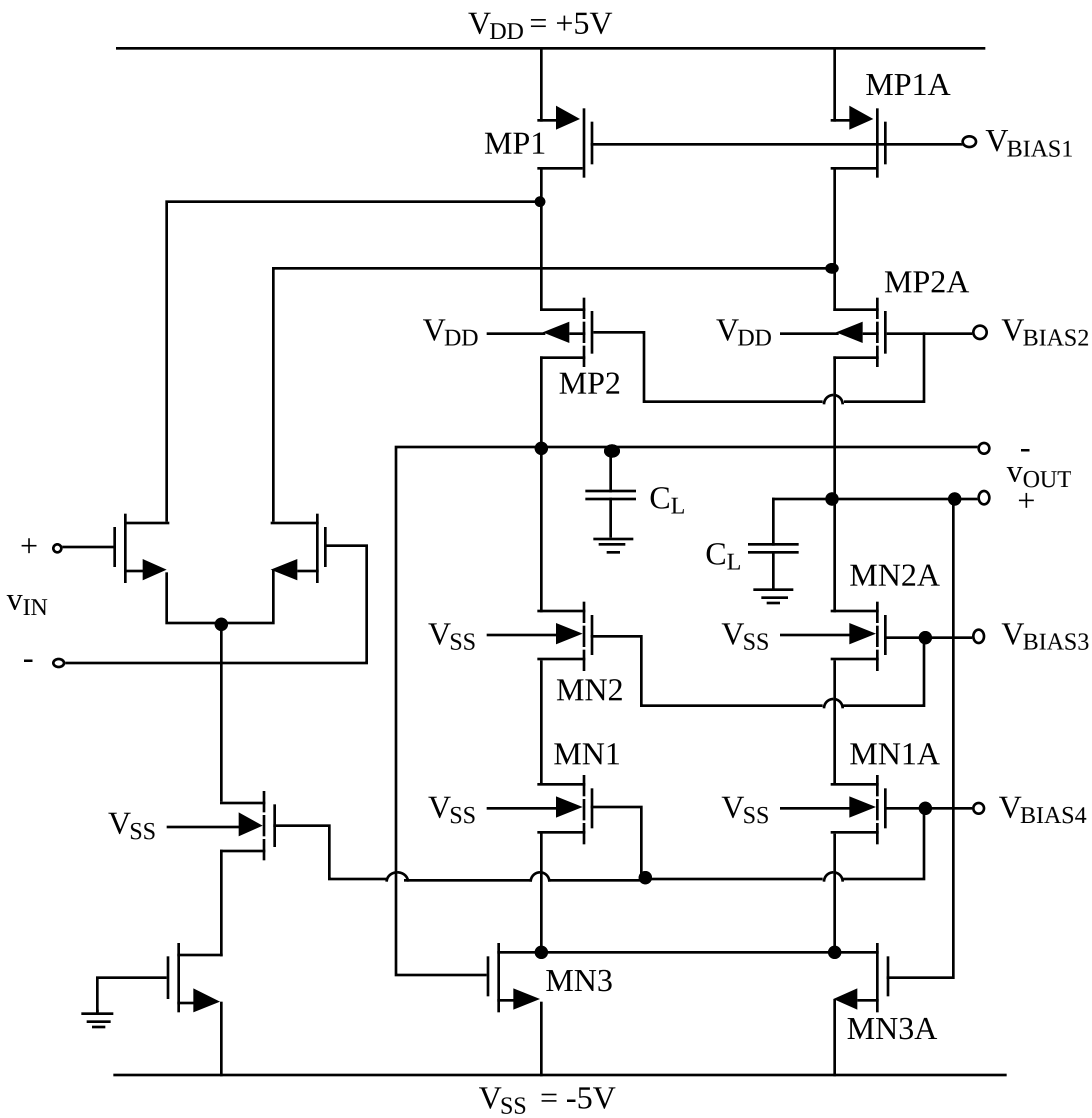
Implementation Using Two Differential-In, Singled-Ended Op Amps



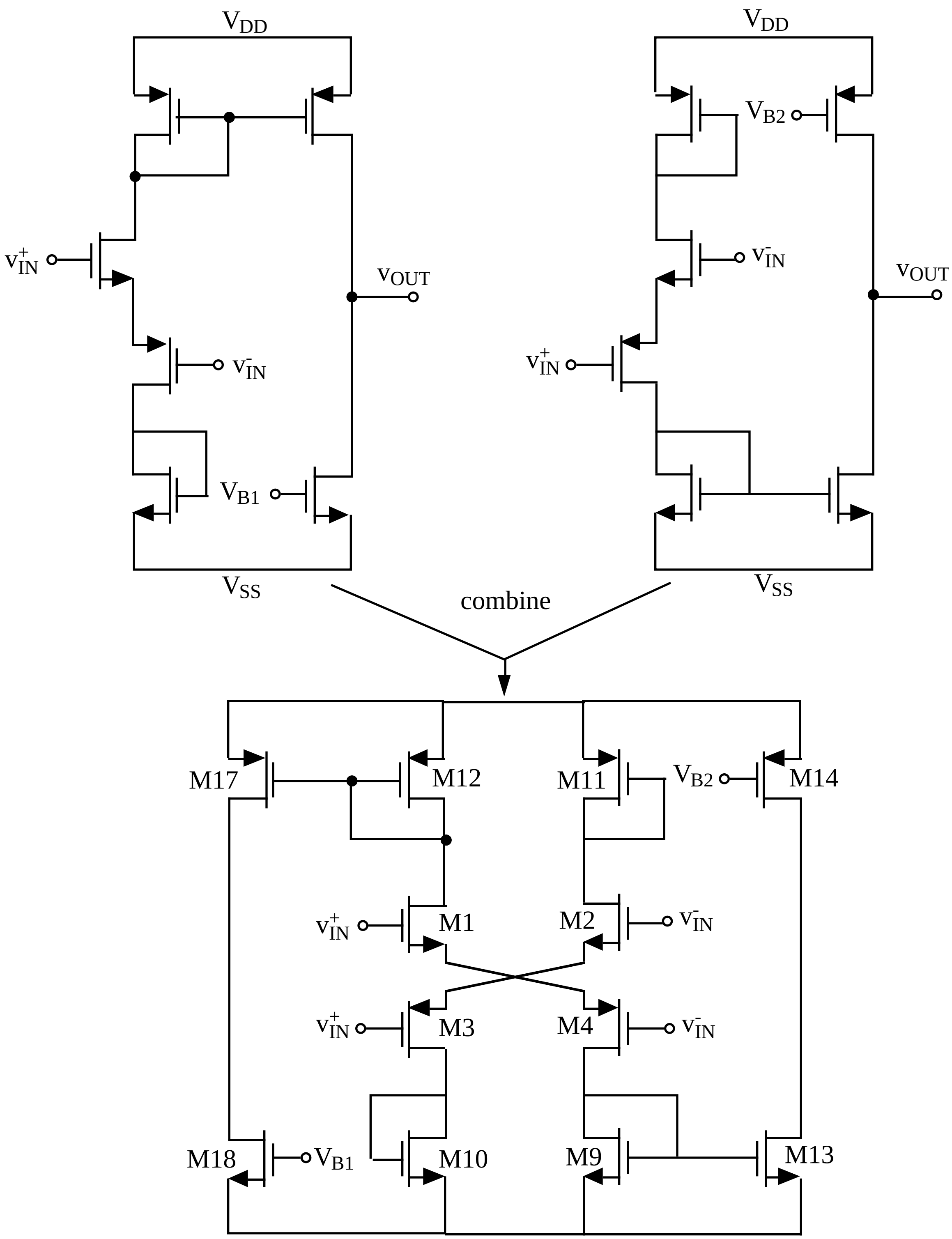
Conceptual Implementation of Differential In-Out OP Amp



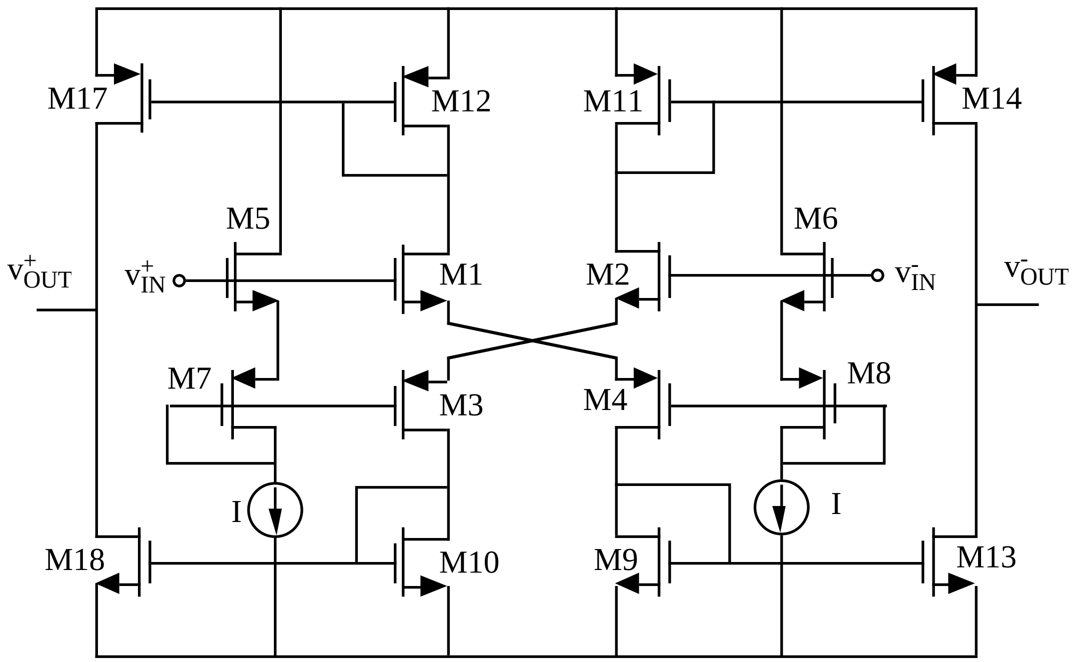
Schematic of a Fully Differential In-Out, FoldedCascode Op Amp



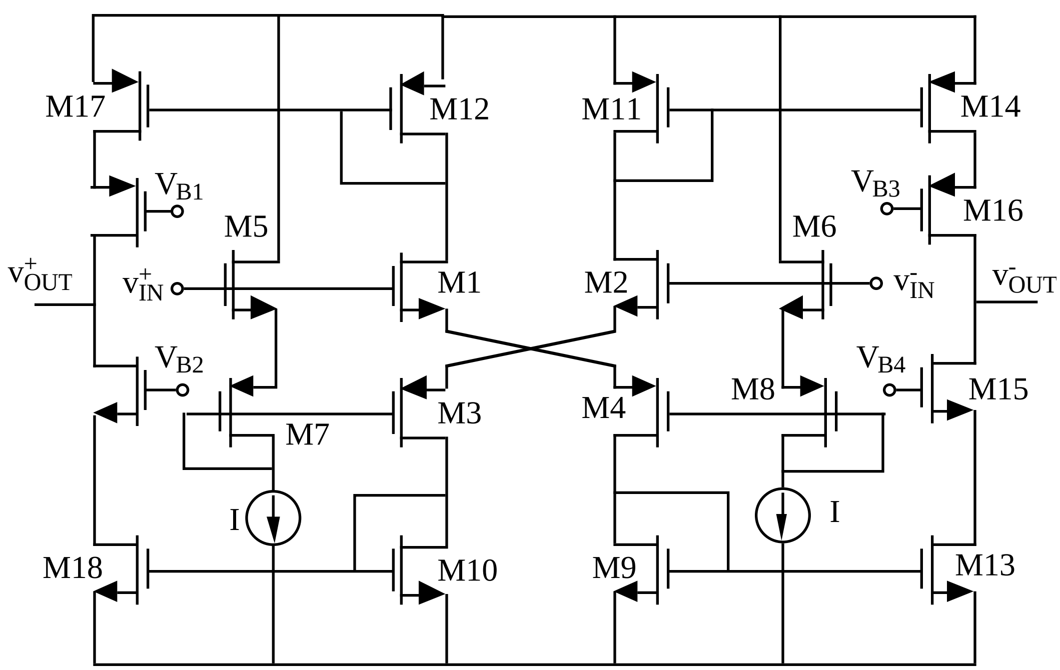
Evolution of Class AB Amplifier



Problem: DC levels of input voltages incompatible



DC problem solved, but amplifier has low gain and requires CM feedback



Gain improved using cascode

IX.5 LOW POWER AMPLIFIERS

General

Objective is to minimize the dc power dissipation.

Typical applications are:

1. Battery powered circuits.
2. Biomedical instrumentation.
3. Low power analog "VLSI."

Weak Inversion or Subthreshold Operation

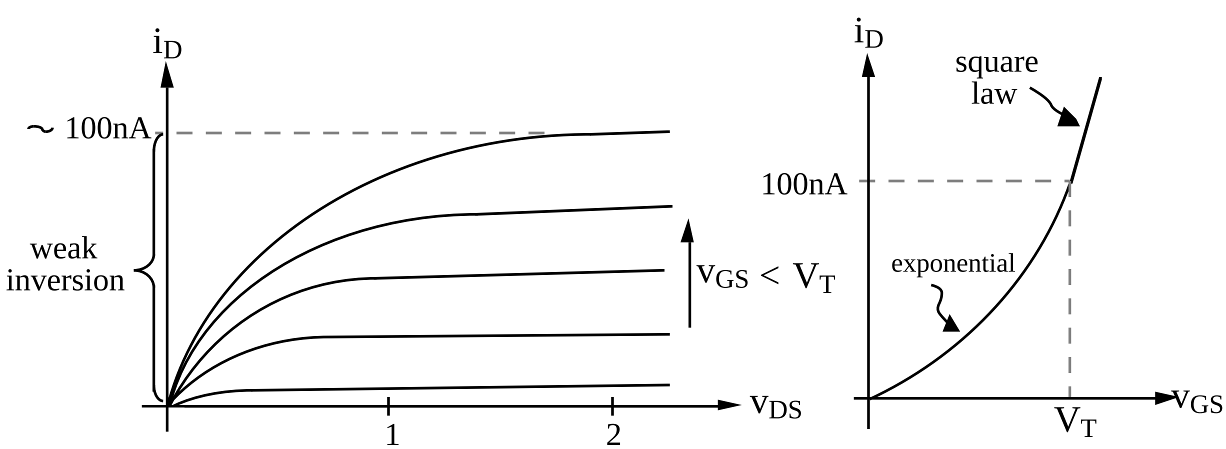
Drain current -

$$i_D = \left(\frac{W}{L}\right) I_D \exp\left(\frac{qv_{GS}}{nkT}\right)(1 + l v_{DS})$$

Small signal parameters -

$$g_m = \frac{qi_D}{nkT}\ , \qquad r_{ds} \approx (\lambda i_D)^{-1}$$

Device characteristics -



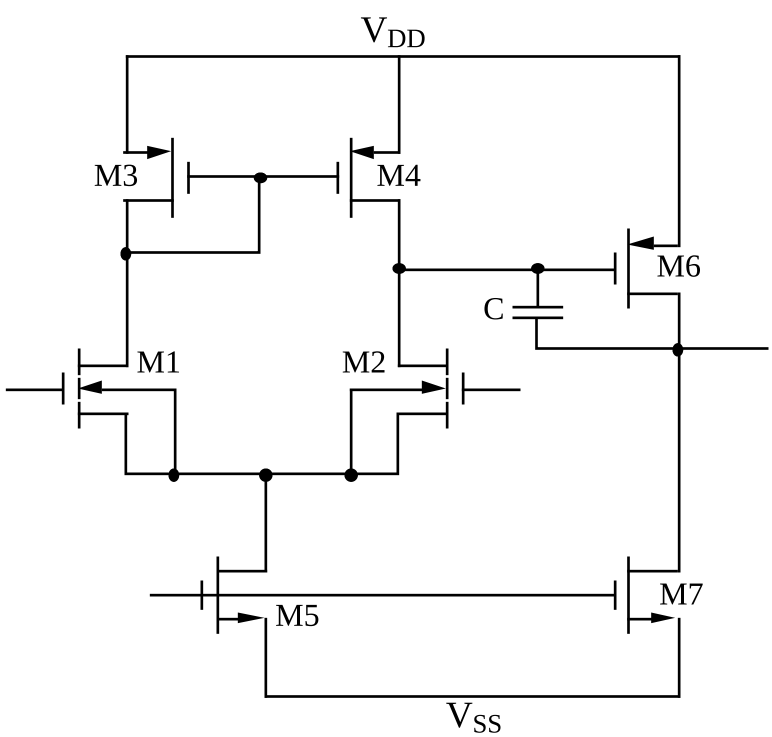
Op Amp Operating in Weak Inversion

Consider the two-stage op amp with reduced currents and power supplieds,

$$A_V = \frac{g_{m2}g_{m6}}{(g_{ds2}+g_{ds4})(g_{ds6}+g_{ds7})} = \frac{1}{n_2 n_6 (kT/q)^2 (l_2+l_4)(l_6+l_7)}$$

where,

$$GB = \frac{g_{m1}}{C} = \frac{I_{D1}}{(n_1 kT/q)C} \quad \text{and} \quad SR = \frac{2I_{D1}}{C} = 2GB\left(\frac{n_1 kT}{q}\right)$$



Design Example

Calculate the gain, unity-gain bandwidth, and slew rate of the previous two-stage op amp used in weak inversion if:

I_{D5} = 200nA	n_P = 1.5	$\lambda_P = 0.02\text{V}^{-1}$
L = 10 µm	n_N = 2.5	$\lambda_N = 0.01\text{V}^{-1}$
C = 5pF	T = 27˚C	

$$A_V = \frac{1}{(1.5)(2.5)(0.026)(2)(0.1+0.02)(0.01+0.02)} = 5698$$

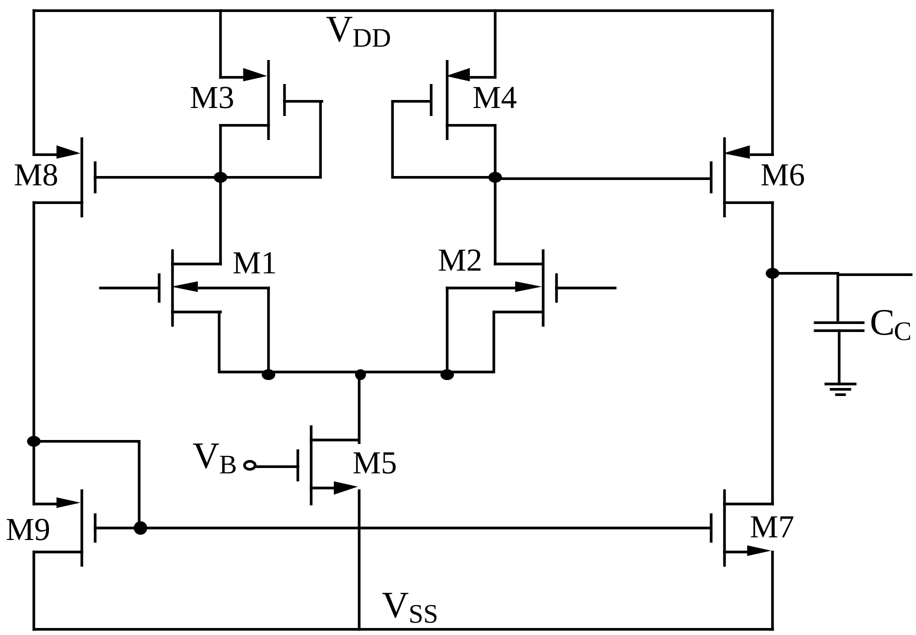
$$GB = \frac{100\cdot10^{-9}}{(2.5)(0.026)(5\cdot10^{-12})} = 307.69\text{Krps or } 48.97\text{KHz}$$

$$SR = 2(153.85\cdot10^{3})(2.5)(0.026) = 0.04\text{V}/\mu\text{s}$$

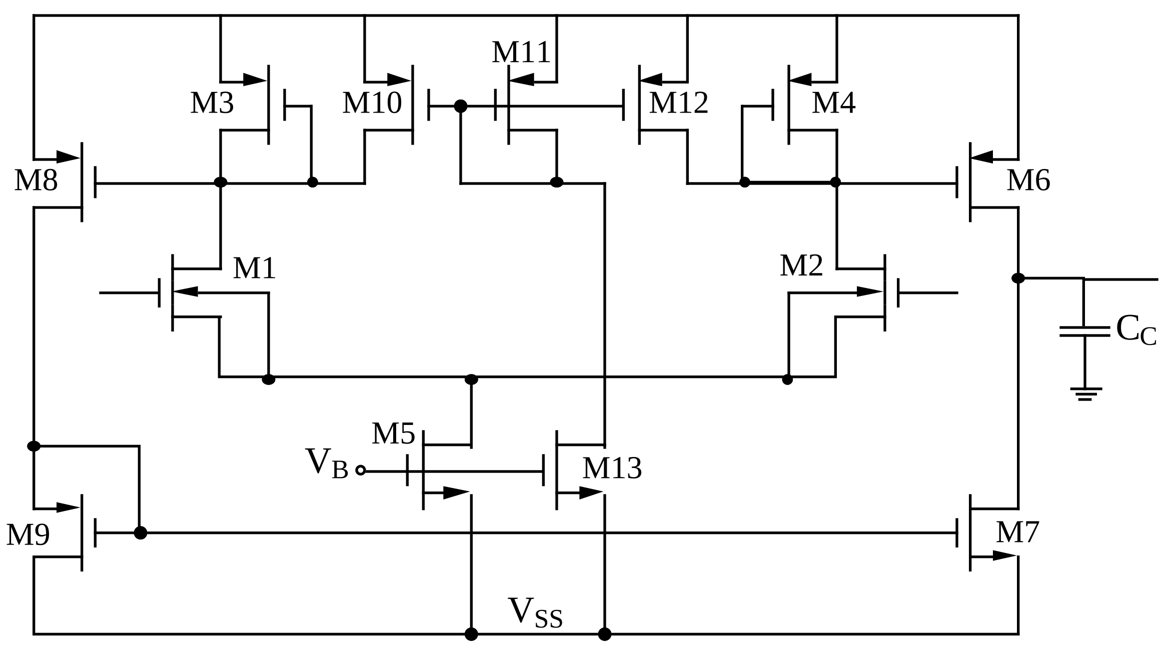
If $V_{DD} = -V_{SS} = 2.5$, the power dissipation is 0.2µW assuming $I_{D7} = I_{D5}$.

Push-Pull Micropower Op Amp

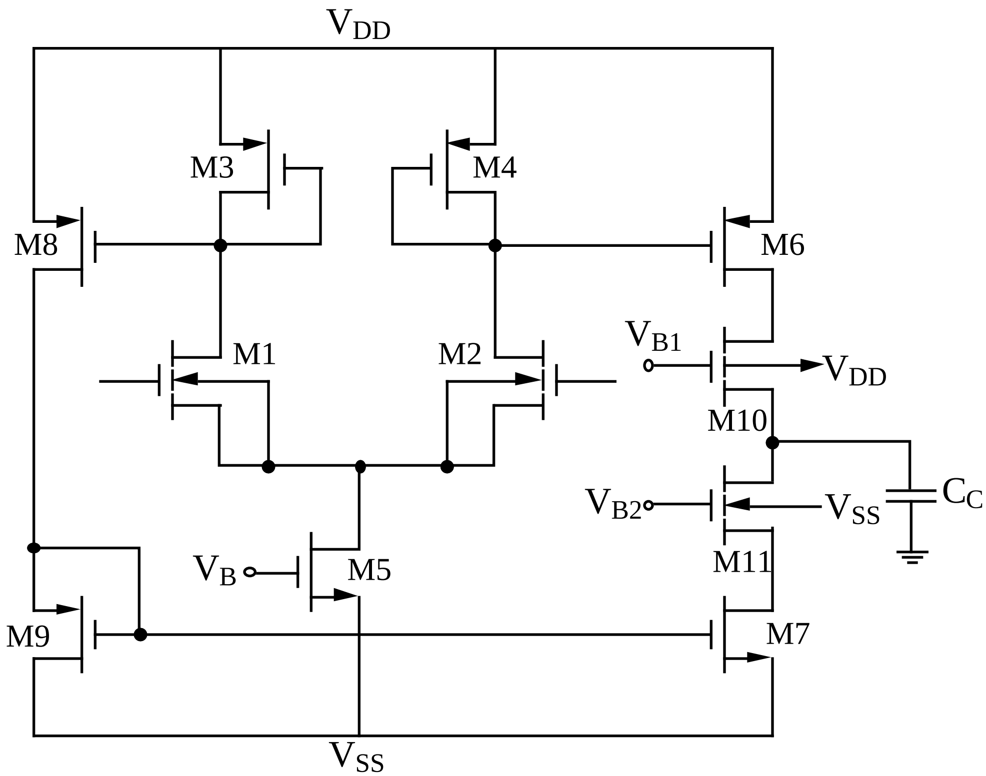
First stage clamped (low gain, low bias current)-



Gain enhancement for Push-Pull Micropower Op Amp



Push-Pull Cascode Micropower Op Amp

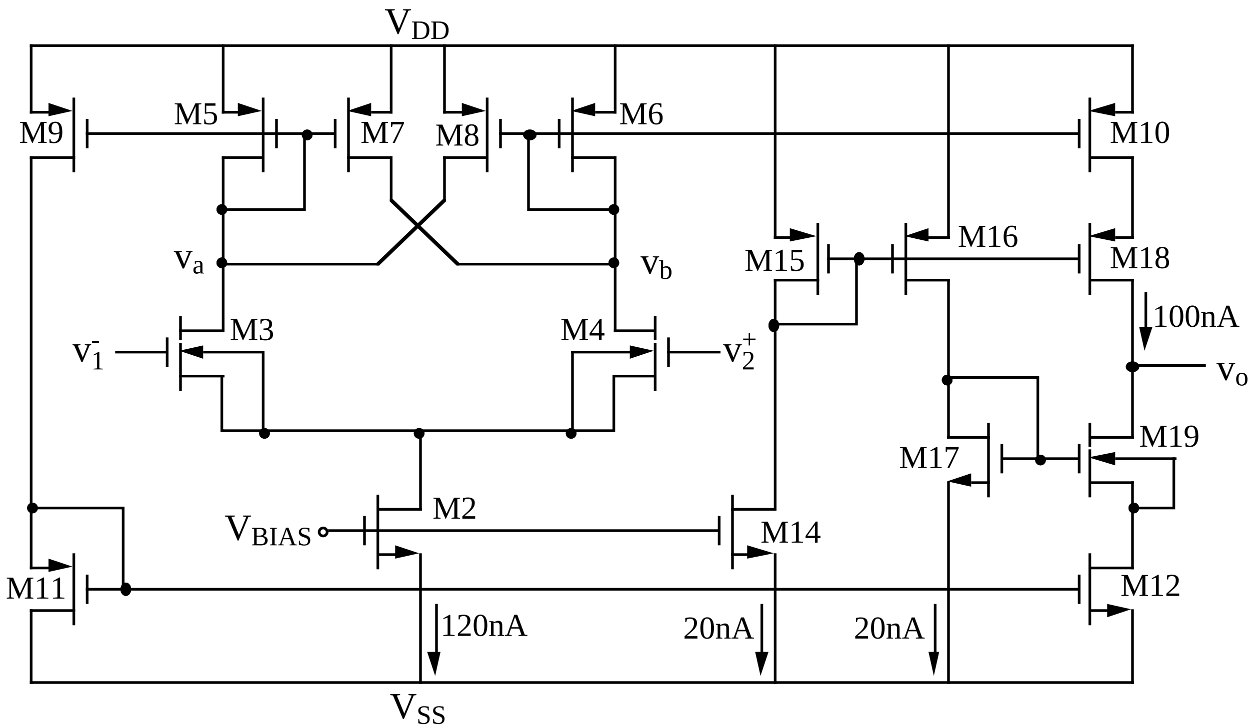


$$A_V = \frac{\frac{1}{n_N} + \frac{1}{n_P}}{V_t^2(\lambda_P^2 n_P + \lambda_N^2 n_N^2)} \approx 10{,}000$$

self-compensating

Low power << 1 μW

Micropower Op Amp



$P_{diss} = |V_{DD}-V_{SS}|(260\text{nA})$

$v_o = v_a g_{m9} r_o - v_b g_{m10} r_o \approx g_{m9} r_o (v_a - v_b)$; $g_{m9} = g_{m10}$

where

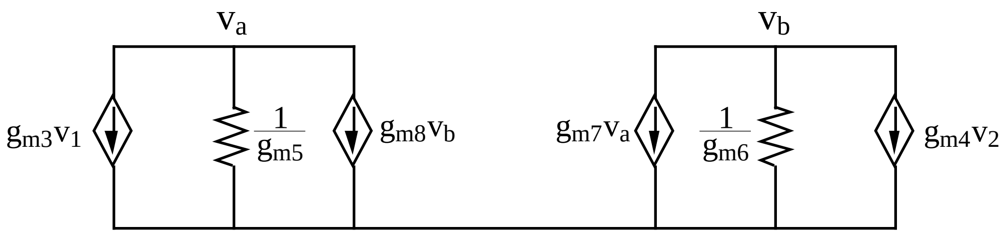
$$r_o \approx (r_{ds10} g_{m18} r_{ds18}) || (r_{ds12} g_{m19} r_{ds19})$$

and

$$(v_a - v_b) = \quad v_a - v_b = \frac{n_P}{n_N}\left(\frac{1 + k}{1 - k}\right)(v_2 - v_1)$$

(See following pages)

Small-Signal Analysis



$$v_a = -v_1\frac{g_{m3}}{g_{m5}} - v_b\frac{g_{m8}}{g_{m5}}$$

$$v_b = -v_2\frac{g_{m4}}{g_{m6}} - v_a\frac{g_{m7}}{g_{m6}}$$

$$\begin{bmatrix} v_1\frac{g_{m3}}{g_{m5}} \\ v_2\frac{g_{m4}}{g_{m6}} \end{bmatrix} = \begin{bmatrix} -1 & -\frac{g_{m8}}{g_{m5}} \\ -\frac{g_{m7}}{g_{m4}} & -1 \end{bmatrix} \begin{bmatrix} v_a \\ v_b \end{bmatrix}$$

$$v_a = \frac{\begin{vmatrix} v_1\frac{g_{m3}}{g_{m5}} & -\frac{g_{m8}}{g_{m5}} \\ v_2\frac{g_{m4}}{g_{m6}} & -1 \end{vmatrix}}{\begin{vmatrix} -1 & -\frac{g_{m8}}{g_{m5}} \\ -\frac{g_{m7}}{g_{m4}} & -1 \end{vmatrix}} = \frac{-v_1\frac{g_{m3}}{g_{m5}} + v_2\frac{g_{m4}g_{m8}}{g_{m5}g_{m6}}}{1 - \frac{g_{m7}g_{m8}}{g_{m5}g_{m6}}}$$

$$v_b = \frac{\begin{vmatrix} -1 & v_1\dfrac{g_{m3}}{g_{m5}} \\ -\dfrac{g_{m7}}{g_{m6}} & v_2\dfrac{g_{m4}}{g_{m6}} \end{vmatrix}}{\begin{vmatrix} -1 & -\dfrac{g_{m8}}{g_{m5}} \\ -\dfrac{g_{m7}}{g_{m4}} & -1 \end{vmatrix}} = \frac{-v_2\dfrac{g_{m4}}{g_{m6}} + v_1\dfrac{g_{m3}g_{m7}}{g_{m5}g_{m6}}}{1 - \dfrac{g_{m7}g_{m8}}{g_{m5}g_{m6}}}$$

$$v_a - v_b = \frac{\left(-v_1\dfrac{g_{m3}}{g_{m5}} + v_2\dfrac{g_{m4}g_{m8}}{g_{m5}g_{m6}}\right) - \left(-v_2\dfrac{g_{m4}}{g_{m6}} + v_1\dfrac{g_{m3}g_{m7}}{g_{m5}g_{m6}}\right)}{1 - \dfrac{g_{m7}g_{m8}}{g_{m5}g_{m4}}}$$

$g_{m3} = g_{m4} = g_{mI}$; $g_{m5} = g_{m6} = g_{mII}$; $g_{m7} = g_{m8} = g_{mIII}$

Then

$$v_a - v_b = \frac{\left(-v_1\dfrac{g_{mI}}{g_{mII}} + v_2\dfrac{g_{mI}g_{mIII}}{g_{mII}^2}\right) - \left(-v_2\dfrac{g_{mI}}{g_{mII}} + v_1\dfrac{g_{mI}g_{mIII}}{g_{mII}^2}\right)}{1 - \dfrac{g_{mIII}^2}{g_{mII}^2}}$$

Define: $\dfrac{g_{mIII}}{g_{mII}} = k$

$$v_a - v_b = \frac{(v_2 - v_1)\dfrac{g_{mI}}{g_{mII}}(1 + k)}{1 - k^2} = (v_2 - v_1)\frac{\left(\dfrac{g_{mI}}{g_{mII}}\right)}{1 - k}$$

$$v_a - v_b = \frac{g_{mI}}{g_{mII}}\left(\frac{1}{1 - k}\right)(v_2 - v_1)$$

Consider dc currents under balanced condititions:

$$I_4 = I_6 + I_7$$

$$I_3 = I_5 + I_8$$

$$I_8 = I_6\left(\frac{S_8}{S_6}\right)\ ;\quad I_7 = I_5\left(\frac{S_7}{S_5}\right)$$

$$\frac{I_8}{I_6} = \frac{S_8}{S_6} \ \Rightarrow \ \text{in W.I. } g_m \text{ is proportional to I}$$

$$\frac{I_8}{I_6} = \frac{S_8}{S_6} = k;\quad \frac{I_7}{I_5} = \frac{S_7}{S_5} = k$$

Since under balanced conditions

$$I_3 = I_4\ ;\ \ I_4 = I_5$$

$$I_4 = I_6\,(1 + k)$$

$$I_3 = I_5\,(1 + k)$$

Again, since $g_m \propto I$ in weak inversion, then

$$g_{m4} \propto I_6(1 + k) \ \text{ or } \ g_{m4} = \frac{I_6}{n_N \dfrac{kT}{q}}(1 + k)$$

and

$$g_{m3} \propto I_5(1 + k)$$

since

$$g_{m3} = g_{m4} = g_{mI} \ \Rightarrow \ g_{mI} = \frac{I_6}{n_N \dfrac{kT}{q}}(1 + k)$$

Also

$$g_{m4} = g_{mII} = \frac{I_6}{n_N \dfrac{kT}{q}}$$

then

$$\frac{g_{mI}}{g_{mII}} = \left(\frac{n_P}{n_N}\right)(1 + k)$$

finally:

$$v_a - v_b = \frac{n_P}{n_N}\left(\frac{1 + k}{1 - k}\right)(v_2 - v_1)$$

$$\approx \frac{1 + k}{1 - k}(v_2 - v_1)$$

Therefore,

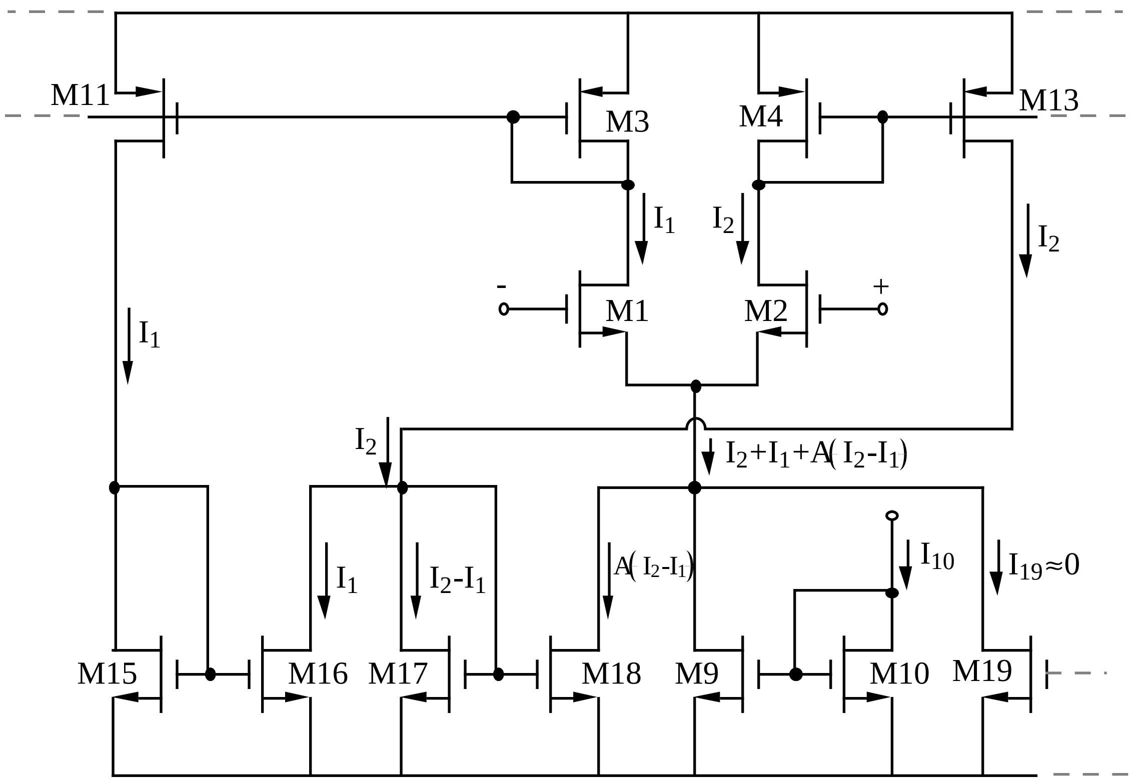
$$v_o = g_{m9}\, r_o\left(\frac{1+k}{1-k}\right)v_{id}$$

OTA CURRENT OVERDRIVE

Need large sinking and source currents without having to have large quiescent currents.

One possible solution uses "tail current boosting" -

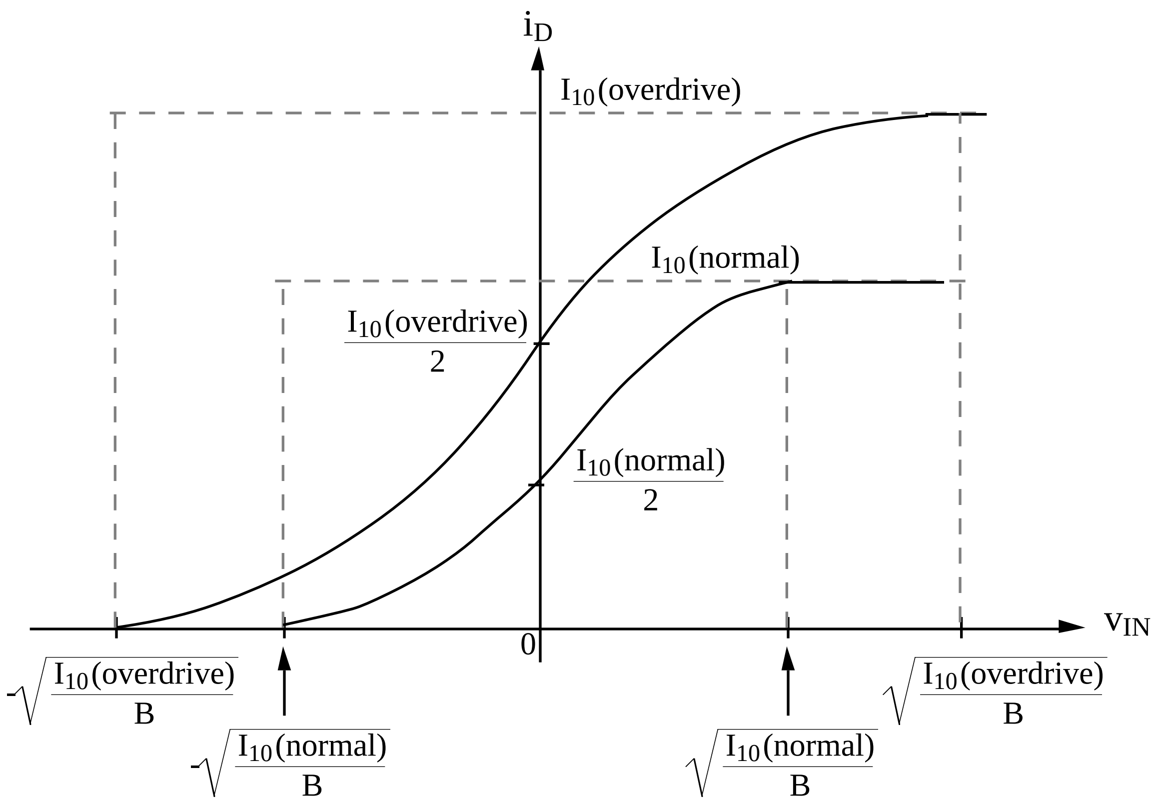
Assume that $S_3 = S_4 = S_{11} = S_{13}$, $S_{18} = AS_{17}$, $S_{15} = S_{16} = S_{17}$ = ..



$$\frac{W_{18}}{L_{18}} = A\frac{W_{17}}{L_{17}}$$

Principle in Achieving Current Overdrive

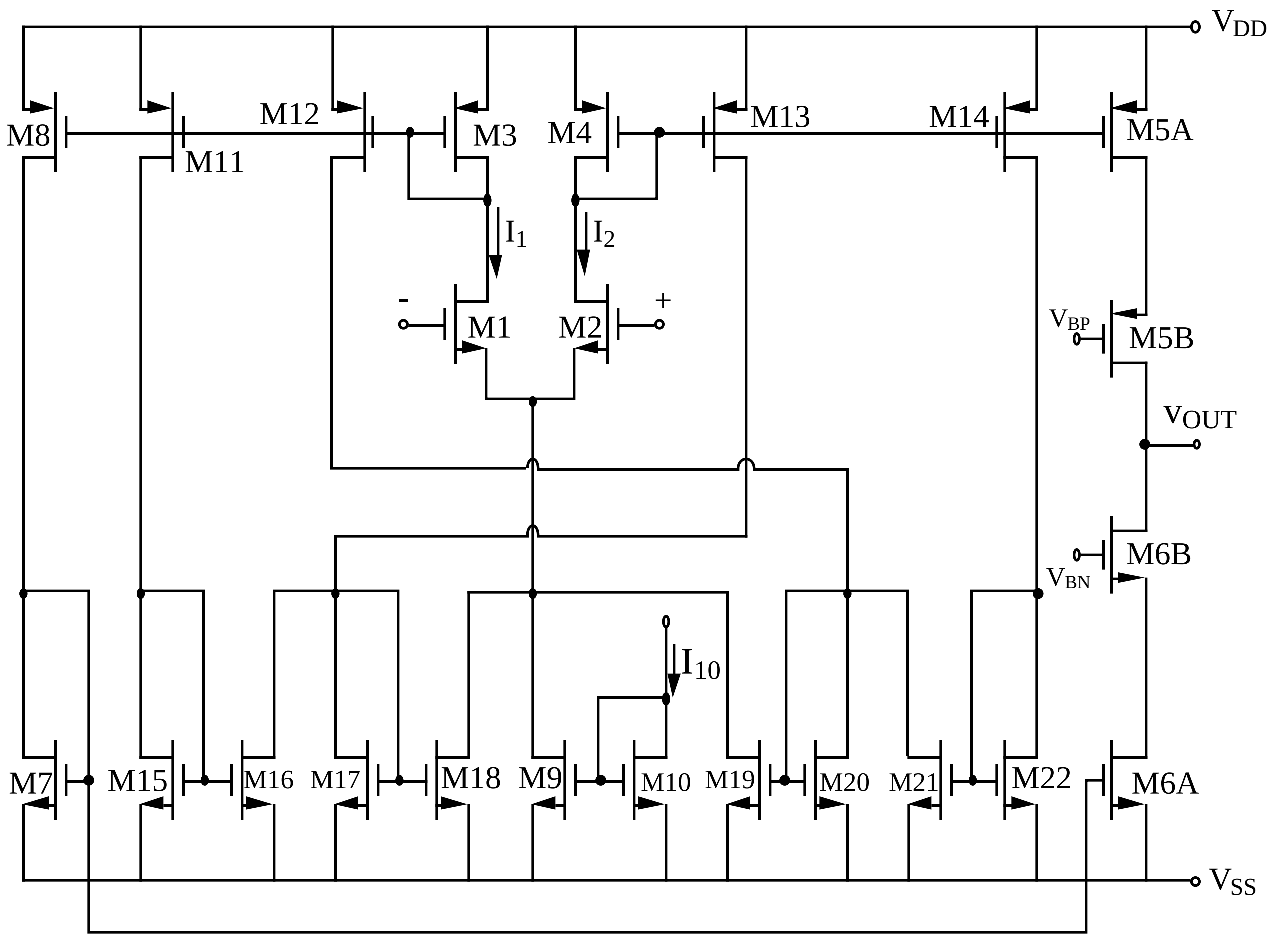
Differential amplifier transconductance characteristics -



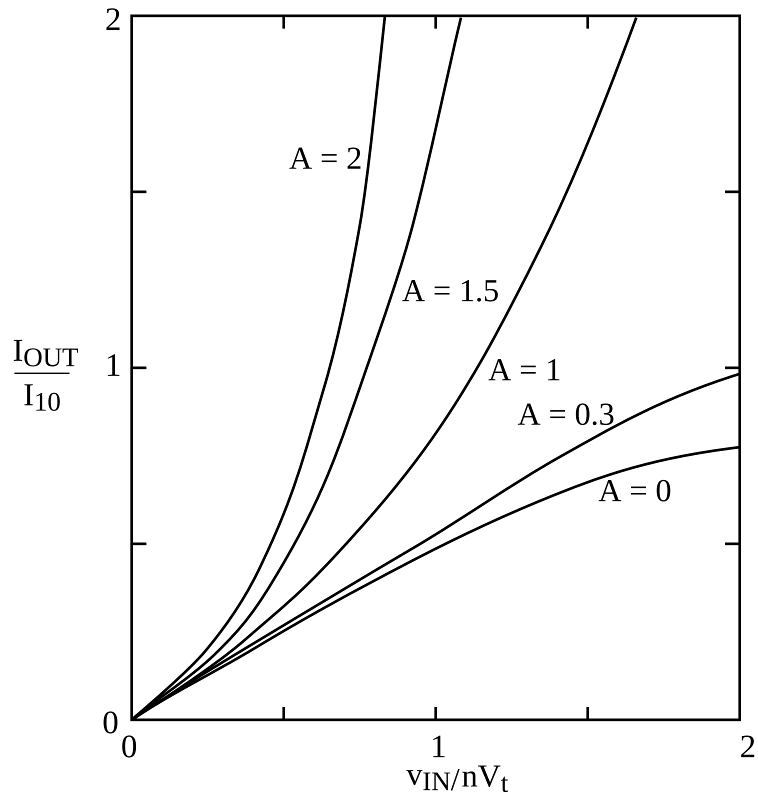
Positive feedback -

$$i_{OUT}\ (\text{max/min}) \approx \frac{I_{10}}{1 - \text{Loop gain}} = \frac{I_{10}}{1 - \frac{g_{m18}}{g_{m17}}\frac{g_{m13}}{g_{m14}}} = \frac{I_{10}}{1 - \frac{g_{m13}}{g_{m9}}A}$$

A Dynamically Biased Micropower Op Amp



Parametric Overdrive Curves for Dynamically Biased Op Amp



IX.7 - DYNAMICALLY BIASED AMPLIFIERS

Dynamic circuits take advantage of the fact that many applications are synchronously clocked resulting in periods of time where the circuits is not functioning.

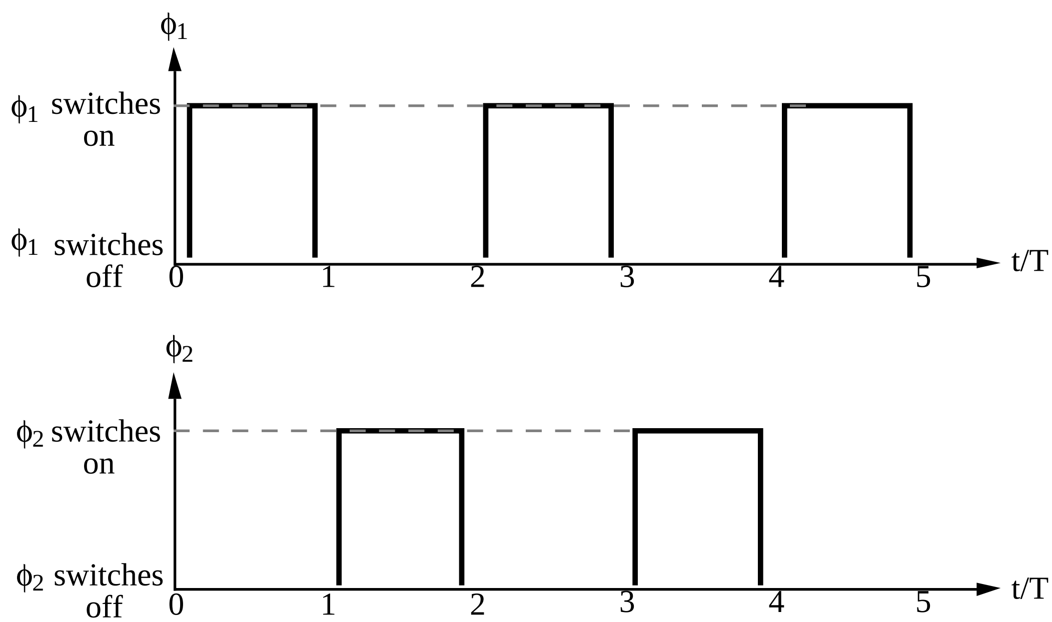
Will examine:

- Dynamic or switched resistors

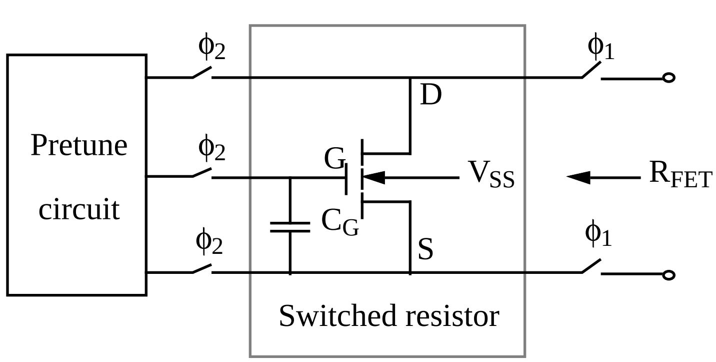
- Dynamically biased amplifiers

- Dynamically biased, push-pull, cascode op amp

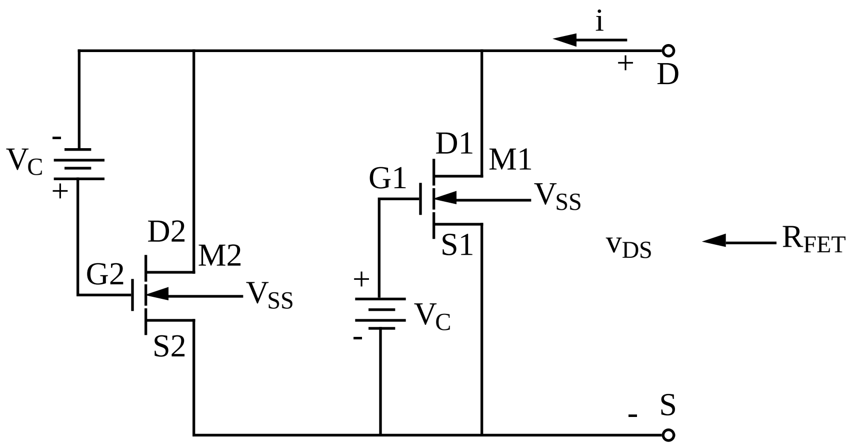
<u>Two Phase Clock</u>



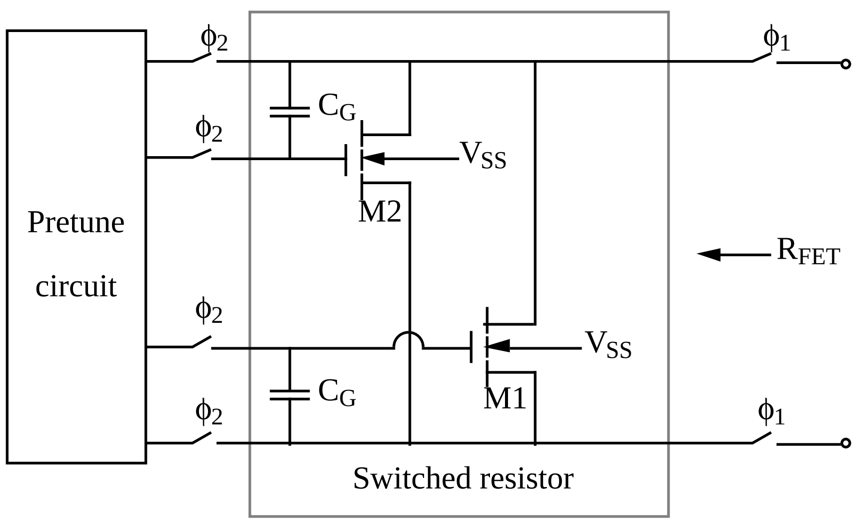
<u>A Switched Resistance Realization</u>



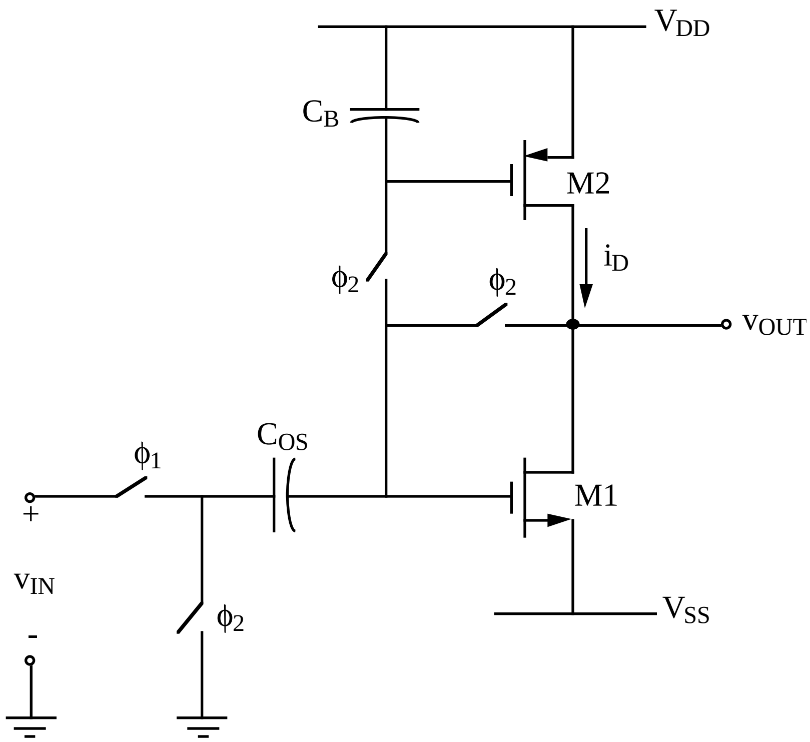
A Continuous Time Resistor Realization with Increased Signal Swing



Implementation of the Continuous Time Switched Resistor Realization using Dynamic Techniques



Dynamically Biased Inverter

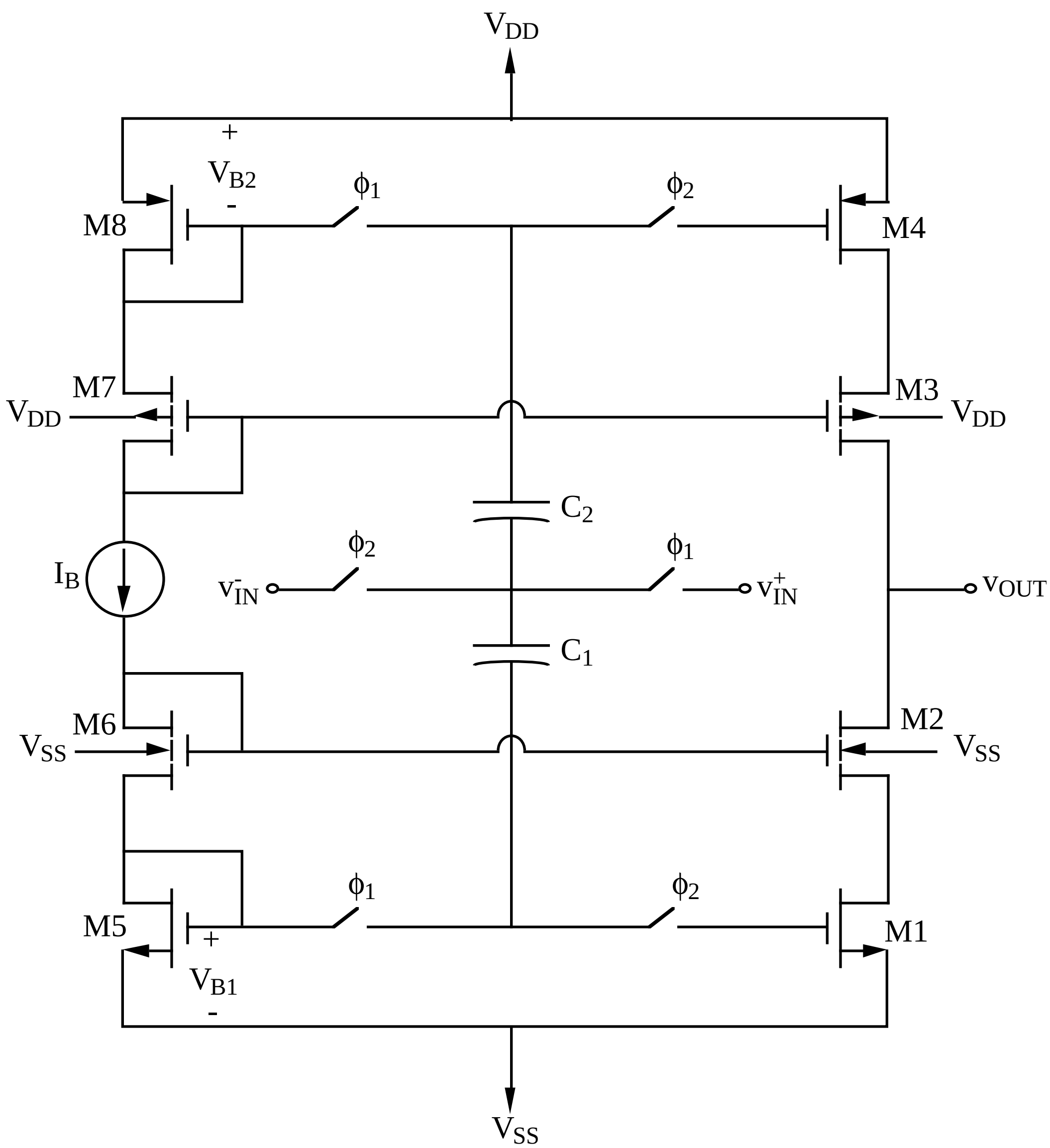


During phase 2 the offset and bias of the inverter is sampled and applied to C_{OS} and C_B.

During phase 1 C_{OS} is connected in series with the input and provides offset cancelling plus bias for M1. C_B provides the bias for M2.

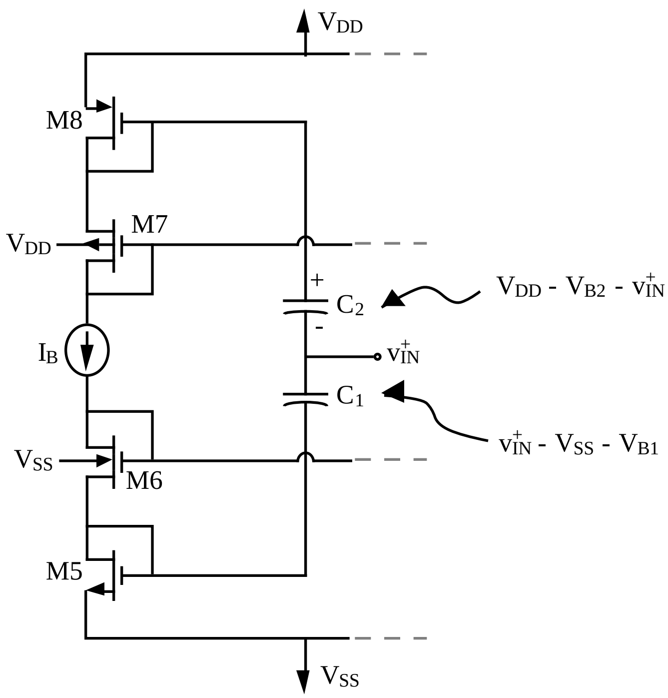
Dynamic, Push-pull, Cascode Op Amp

Simplified schematic -

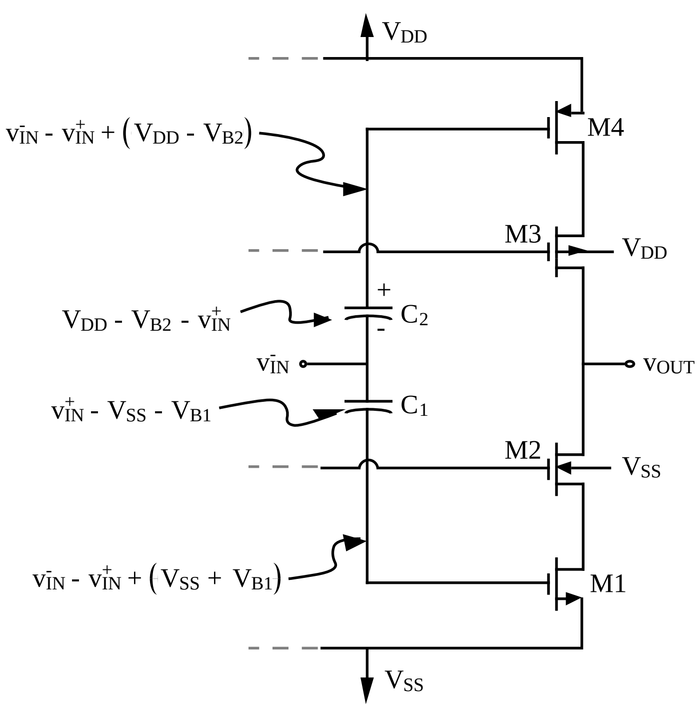


Dynamic, Push-pull, Cascode Op Amp - Cont'd

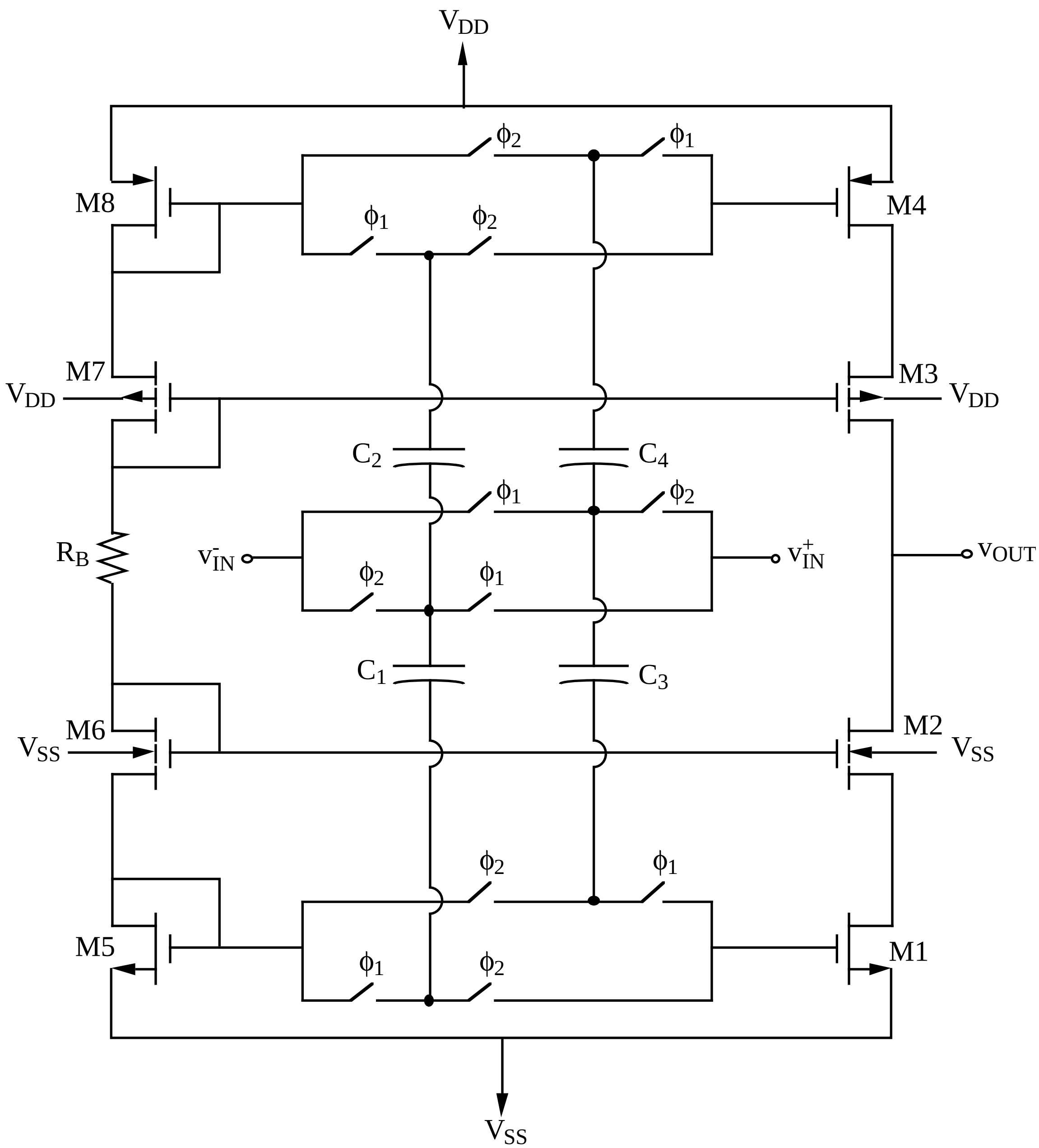
Phase 1 Clock Period



Phase 2 Clock Period



A Dynamic Op Amp which Operates on Both Clock Phases



1.6 mW dissipation Settling time = 10 ns into 5 pF

GB ≈ 130 MHz with C_L = 2.2 pF 1.5 μm technology

Used with a 28.6 MHz clock to realize a 5th order switched capacitor filter with a cutoff frequency of 3.5 MHz.