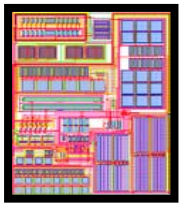
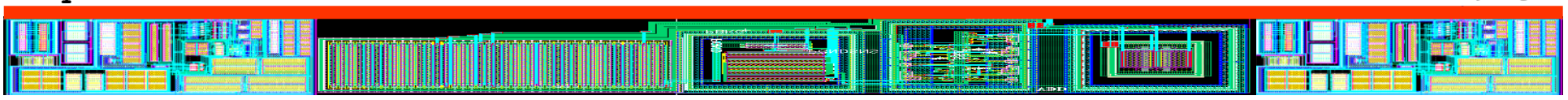
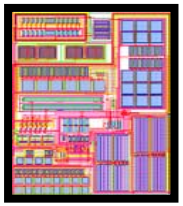


EE6326 Analog IC Design – Fall 2008

HW#3 Design Guide

Wenliang Chen, Ph. D.
Instructor

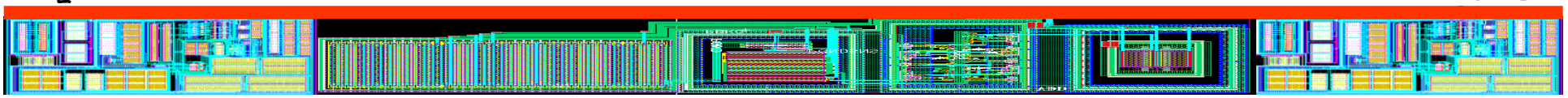


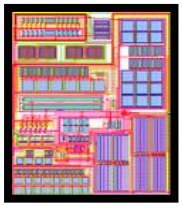


Outlines

- This design guide and class-note-05 are needed as references to complete HW#3.

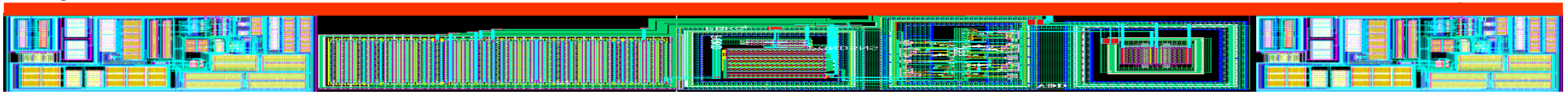
- Design Blocks
  - Brokaw Bandgap
    (architecture can be different.)
  - Constant current references & mirrors
  - IPTAT current references & mirrors
  - Constant Gm current references & mirrors
  - Thermal shut down circuit

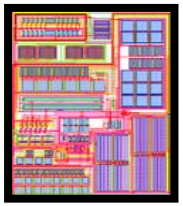




Design Steps

- **Design a bandgap circuit containing IPTATxR and VBE parts**
  - The IPTAT part will be re-used as current reference
  - A start-up circuit is needed
- **Design a constant current reference and mirror**
  - An ideal OPAMP is approximated with a "vcvs" ideal voltage source in cadence.
  - VBG and an external zero T.C. R are used to generate constant currents
  - Both current sources and current sinks are required.
- **Design an IPTAT current reference and mirror**
  - Re-use it from BG circuit
  - Only current sources are needed
- **Design a constant Gm current reference and mirrors**
  - An ideal OPAMP and VBG are used to increase Rout
  - Only current sinks are needed.
- **Design a thermal shut down circuit**
  - Tz,h=150C & Tz,l=130C
  - Thermal hysteresis of 20C is achieved by changing sensing-R values.

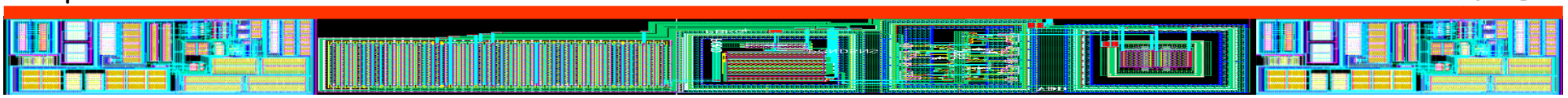




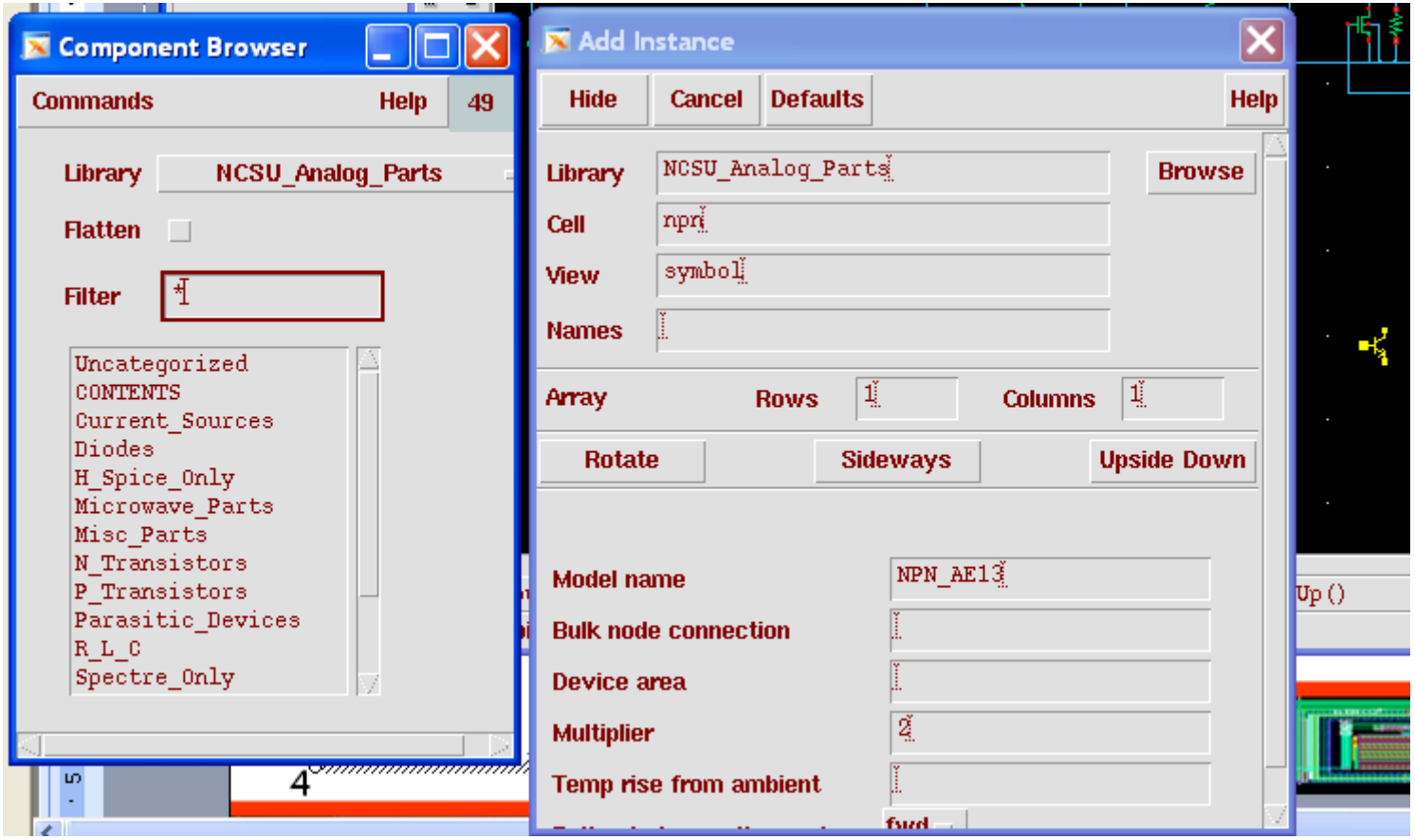
BJT model setup

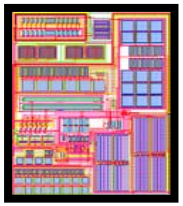
- In your UNIX home directory, please make a directory called "models".
- Copy "NPN_AE13" into the "models" directory
- To add a BJT symbol into your schematic
  - "i" → "NCSU_Analog_parts"→"N_Transistors"→"npn"→ drag it to a desired spot in your schematic then left click → key in "NPN_AE13" in the Model name and Multiplier number
  - In case changes of NPN_AE13 BJTs are needed, please "Q" the BJT symbol and type in "numbers of BJTs" in the "Multiplier" cell.

- When you are ready to run simulations, please include this model in ADE's model libraries path:
  - In "ADE" simulation window → setup → Model Libraries → key in "~/models/NPN_AE13" → Hit "O.K."



Adding a BJT into your schematic





Adding NPN_AE13 into Model Libraries Path!

Cadence® Analog Design Environment (1)

Status: Ready T=27.0 C Simulator: spectre 4

Session | Setup | Analyses | Variables | Outputs | Simulation | Results | Tools | Help

Design ...
Simulator/Directory/Host ...
Model Libraries ...
Temperature ...
Stimuli ...
Simulation Files ...
Environment ...

Analyses

	Arguments	Enable
	t	yes
	0 10m	yes

Design Variables

#	Name	Value
1	VG	2.38
2	VDP	2.8
3	VDN	1.5
4	fclk	3K
5	VOUT	1

Outputs

#	Name/Signal/Expr	Value	Plot	Save	March
44	net0367		no	allv	no
45	P39/D		no	yes	no
46	N25/D		no	yes	no
47	N26/D		no	yes	no
48	N24/D		no	yes	no
49	N27/D		no	yes	no

New Slide

e make a directory calle

directory

When you are ready to run simulations, please include this m

in ADE

- In "

spectre0: Model Library Setup

OK | Cancel | Defaults | Apply | Help

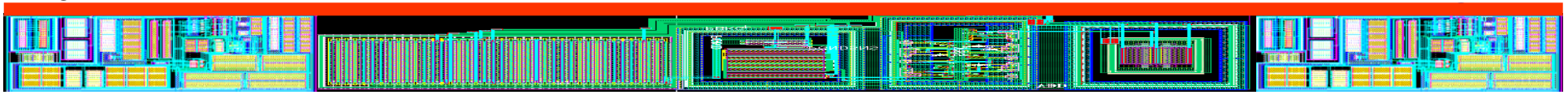
#Disable	Model Library File	Section
	...cad/ee6326/ncsu1.3/local/models/spectre/nom/tsmc35N.m.n88y	
	...cad/ee6326/ncsu1.3/local/models/spectre/nom/tsmc35P.m.n88y	

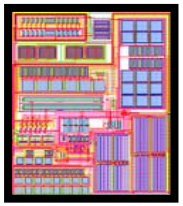
Enable | Disable | Up | Down

Model Library File: ~/models//NPN_AE13

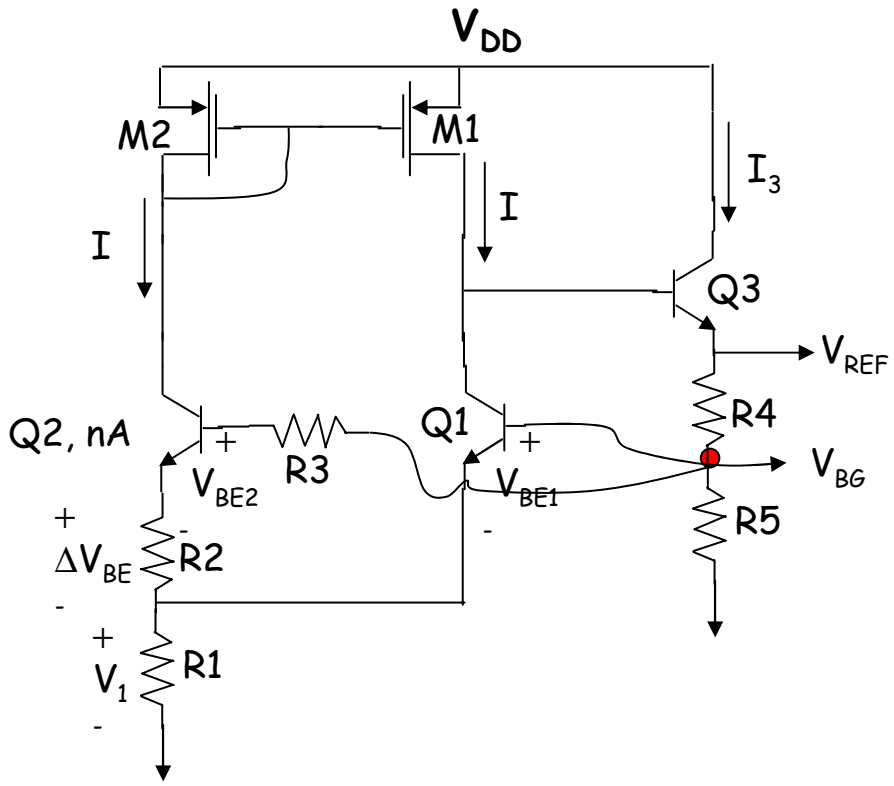
Section (opt.):

Add | Delete | Change | Edit File | Browse...





Brokaw Bandgap

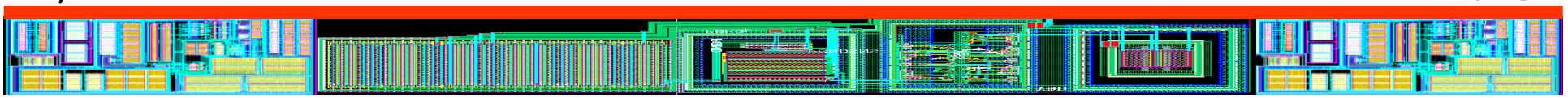


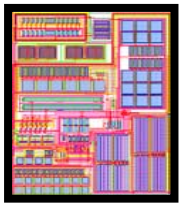
$$V_{BG} = V_1 + V_{BE1}$$
$$= 2 \times I \times R_1 + V_{BE1}$$
$$I = \frac{\Delta V_{BE}}{R_2} = \frac{V_T \ln(n)}{R_2}$$
$$V_{BG} = \frac{2 \times R_1}{R_2} V_T \ln(n) + V_{BE1}$$
$$= k_b \times V_T + V_{BE1}$$

$$V_{ref} = V_{BG}(1 + \frac{R_4}{R_5})$$

R_3 is to keep $V_{BE1} = V_{BE2}$

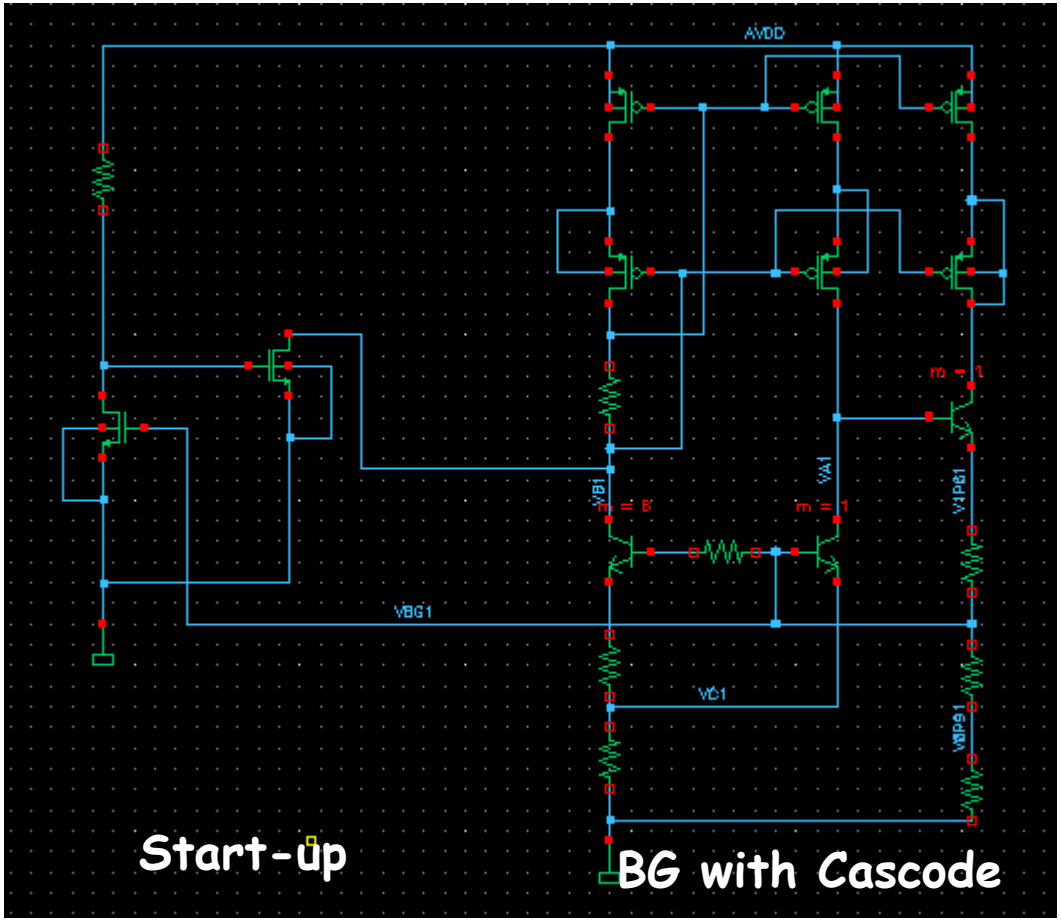
$$R_3 \sim \frac{R_2}{R_1}(\frac{R_4 R_5}{R_4 + R_5})$$

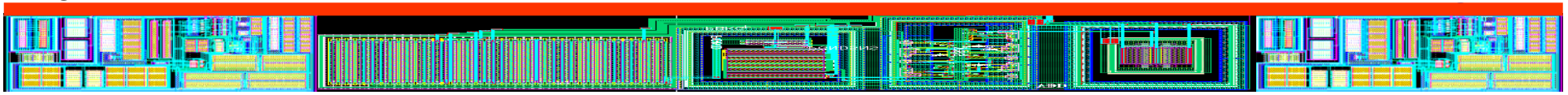


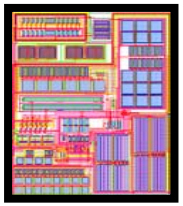


Brokaw Bandgap

UTD models

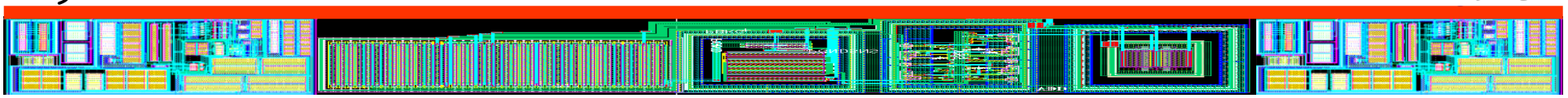


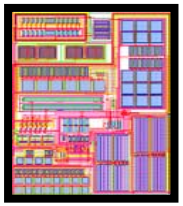




Design Procedure of Brokaw BG for VBG

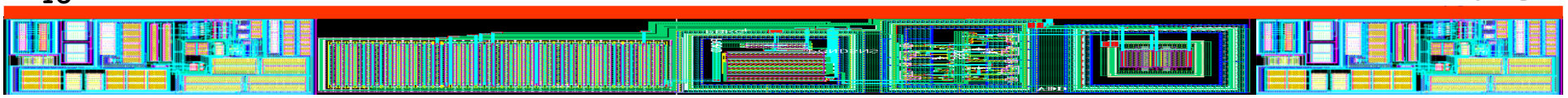
- Specification:VBG=1.2V, Vref=1.6V, I=10uA, I3=10uA
- Let's assume a n first & room temp = 300K
- I = VTln(n)/R2→ R2= VTln(n)/I
- Since VBG=1.2V, VBG = 2IR1+VBE1=20e-6xR1+VBE1=1.2
- Let's assume VBE=0.7V, → R1=(1.2-0.70.5)/2I
- I3=VBG/R5, → R5=1.2/I3
- Vref=VBG(1+R4/R5), R4=(Vref/VBG-1)xR5
- R3=(R2/R1)[R4R5/(R4+R5)]
- Make sure that the choice of PMOS are in saturation region & BJT are in active region
- If hand-calculation does not match sim. results, please adjust R1, R2 & R3 and iterations.
- For DC accuracy, adjusting R1 & R2 are crucial.

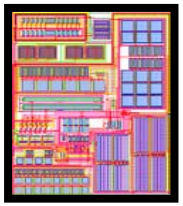




Design procedure of Brokaw BG for PSRR

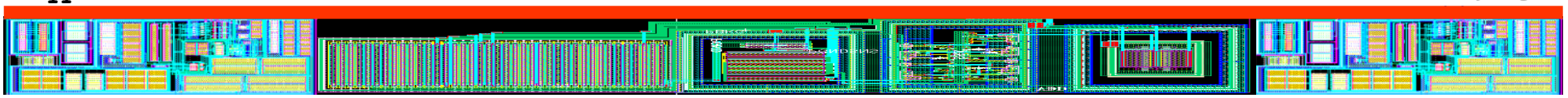
- Target PSRR=40dB, I=10uA, I3=10uA
- PSRR=20log(ΔVBG/ΔVnoise@supply)
- Let's plan to use PMOS $2\Delta V_{OD}$ wide-swing cascode on top Brokaw BG to provide the 40dB PSRR. The question is how does PSRR spec. translates to the required output impedance?
- If Rout is larger, ΔI is smaller.
- VBG=2xIxR1+VBE1; ΔVBG=2ΔIxR1, assuming VBE1 remains unchanged.
- Reasonable ΔVnoise@supply~ 100mV thus ΔVBG=1mV.
- R1~25 KΩ, thus ΔI=ΔVBG/2R1=1mV/50 KΩ =20nA
- Rout_min > ΔVnoise@supply/20nA = 100mV/20nA = 5MΩ !

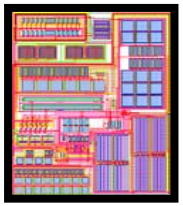




Design procedure for Rout of Wide-swing Cascode current mirror

- Rout~gm2 x rds2 x rds1; gm2=$2I_D/V_{GST}$
  Thus Rout~ $(2I_D/V_{GST})$ rds^2
- Assume V_{GST}~200mV; I_D=10uA; gm2~2e-5/0.1=2e-4=100uS
- Rout=5e6=1e-4xrds^2 → rds > 224kΩ
- We also know the potential of base of Q3 ~ 1.6V + 0.7V=2.3V
- Thus the Vout of the PMOS $2\Delta V_{OD}$ wide-swing cascode is 2.3V
- The $2\Delta V_{OD}$~1V, assume equal split ΔV_{OD}~0.5V.
- Thus the design spec. of output stage of PMOS $2\Delta V_{OD}$ wide-swing cascode is as following:
  - I_D~ 10uA; One ΔV_{OD}~ 0.5V, AVDD=3.3V & Vout~2.3V.
  - rds > 224kΩ; V_{GST}~200mV; g_{m2}~100uS
- Choose PMOS's size
  - dc OP sim. to get |Vth,p| ~ 740mV
  - Sweep I-V curve of PMOS such that
    - I_D~ 10uA, ΔV_{OD}~ 0.5V, rds > 224kΩ, $|V_{GST}|$~200mV & g_{m2}~100uS
    - Rough estimate size ~4(2.5/1)

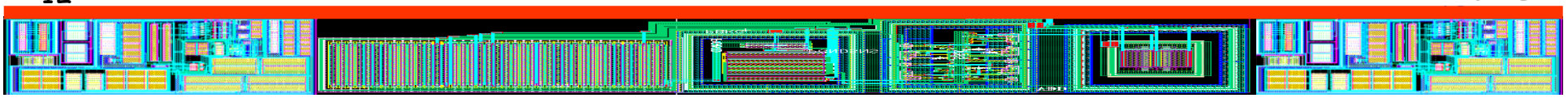


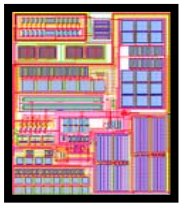


Testing of Brokaw BG

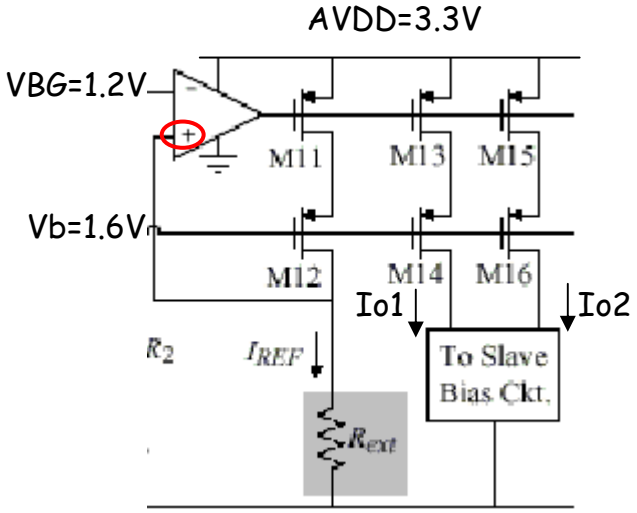
- T.C.:
  - Use dc analysis, sweep temp. from -40C to 125C
  - Use calculator function VS(VBG) to get VBG vs temp plot
  - T.C. = ΔVBG/1.2V/165C x 1e6 (ppm/^{o}C)

- PSRR:
  - Use "vsin" source to add noise with 0.1V amplitude
    - Offset voltage=0V
    - Amplitude=100mV
    - Frequency=1KHz
    - DC voltage=0V
  - Run transient analysis for 10ms
    - Plot VBG vs time
    - Measure the amplitude of $VBG_{pk\text{-}pk}$
    - PSRR = 20 x log ($\Delta VBG_{pk\text{-}pk}$/0.2) in dB

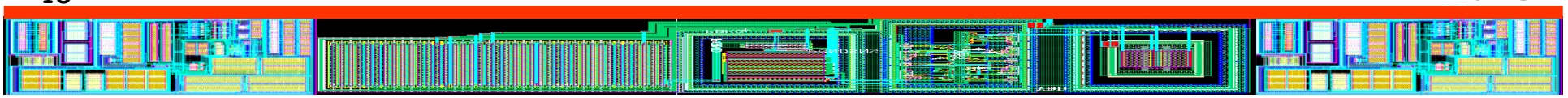


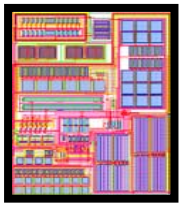


Constant Current Reference & Mirror



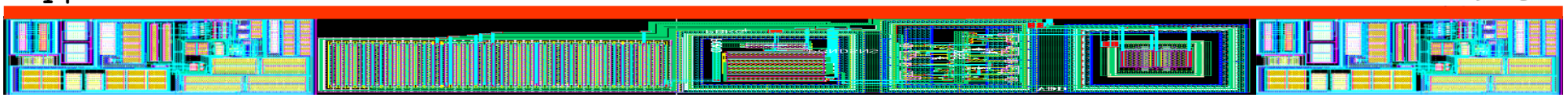
1) Use VBG to generate constant current reference
2) Iref=1uA, Rext=VBG/Iref
   (this Rext is too big for good noise performance,
   we will discuss noise and current trade off later.)
3) If $(W/L)_{14}=(W/L)_{12}$ & $(W/L)_{13}=(W/L)_{11}$ then I_{O1}=1uA
4) If $(W/L)_{16}=10(W/L)_{12}$ &
   $(W/L)_{15}=10(W/L)_{11}$ then I_{O2}=10uA
5) Use wide-swing cascode to generate current sinks
   of 5uA & 500nA
6) Rout measurements:
   a. Connect a dc voltage source at the output of current sinks or current sources.
   b. Set the dc voltage to 1V, measure Iout1
   c. Set the dc voltage to 2V, measure Iout2
   d. Rout ~ 1/|Iout1-Iout2|

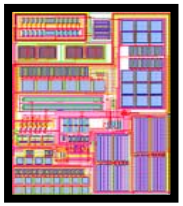




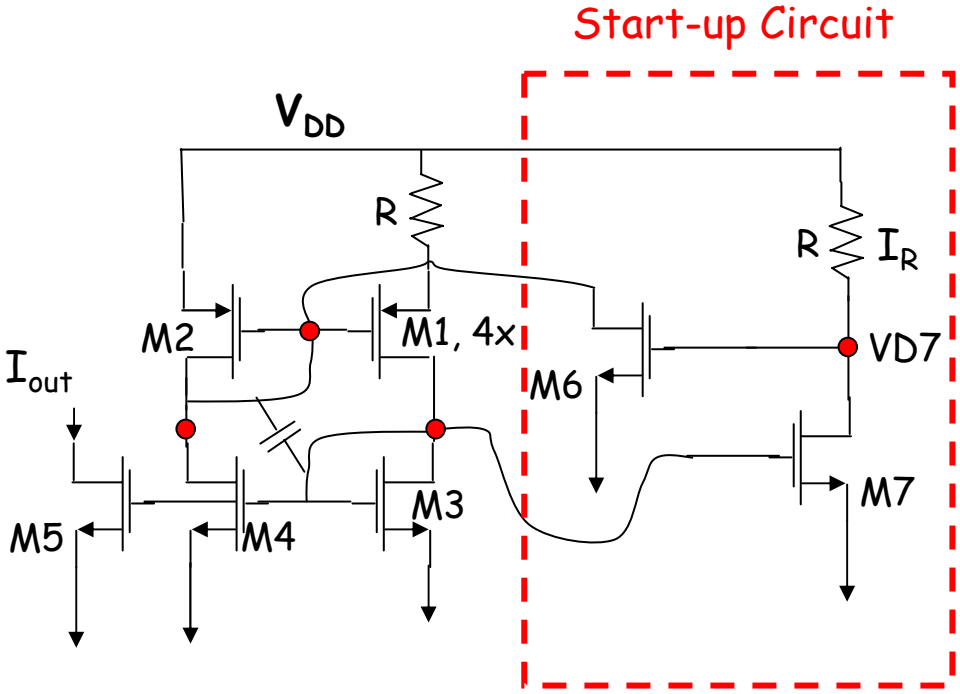
IPTAT reference and mirrors

- The IPTAT current in Brokaw bandgap cell will be re-used
- The 10uA IPTAT is mirrored out to generate 10uA & 2.5uA current sinks.
- The critical point to watch is the slope of IPTAT and its T.C.
- For real applications, we want to match these numbers with those which need compensations.





Constant Gm current reference



Adding a start-up circuit to make sure ID2 ≠ 0

$$I_{D2} = [\frac{(W/L)_4}{(W/L)_3}]^2 \frac{(1 - \sqrt{\frac{(W/L)_2}{(W/L)_1}\frac{(W/L)_3}{(W/L)_4}})^2}{\beta_2 R^2}$$ 2nd solution

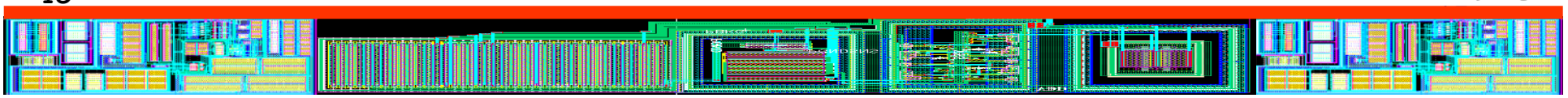
Choose $(W/L)_1 = 4x(W/L)_2; (W/L)_3 = (W/L)_4$

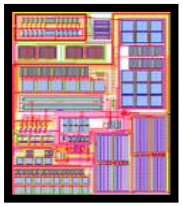
Thus $I_{D2} = \frac{1}{2\beta_2 R^2} = 10uA; R = \sqrt{\frac{1}{2\beta_2 x 10uA}}$

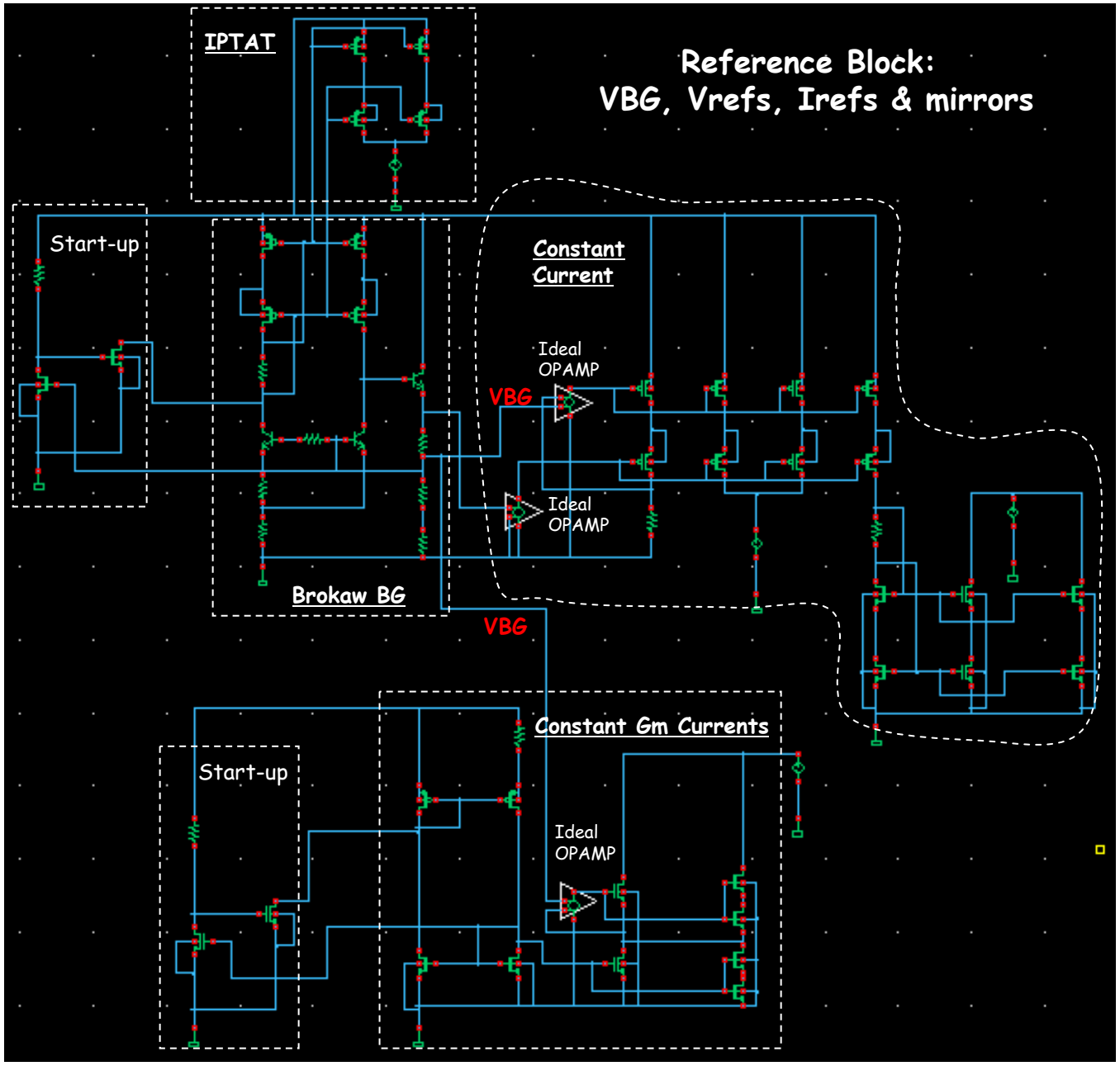
Use dc sweep to estimate $\beta = \frac{1}{2} uC_{ox} \frac{W}{L}$ from $I_D = \beta V_{GST}^2$

If M2's size is chosen first
β is estimated. Then R can be estimated.

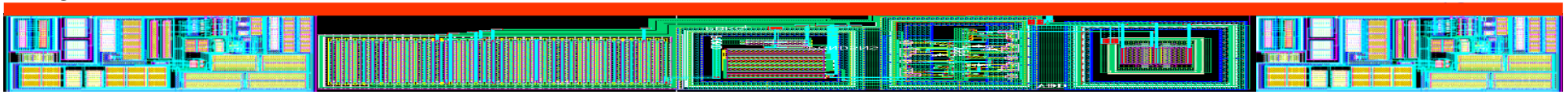
Let's try to construct the constant Gm cell with the estimate sizes.

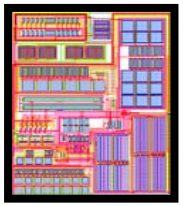





IPTAT
Reference Block:
VBG, Vrefs, Irefs & mirrors
Start-up
Constant
Current
Ideal
OPAMP
VBG
Ideal
OPAMP
Brokaw BG
VBG
Constant Gm Currents
Start-up
Ideal
OPAMP

UTD Models





Thermal Shut-Down Circuit

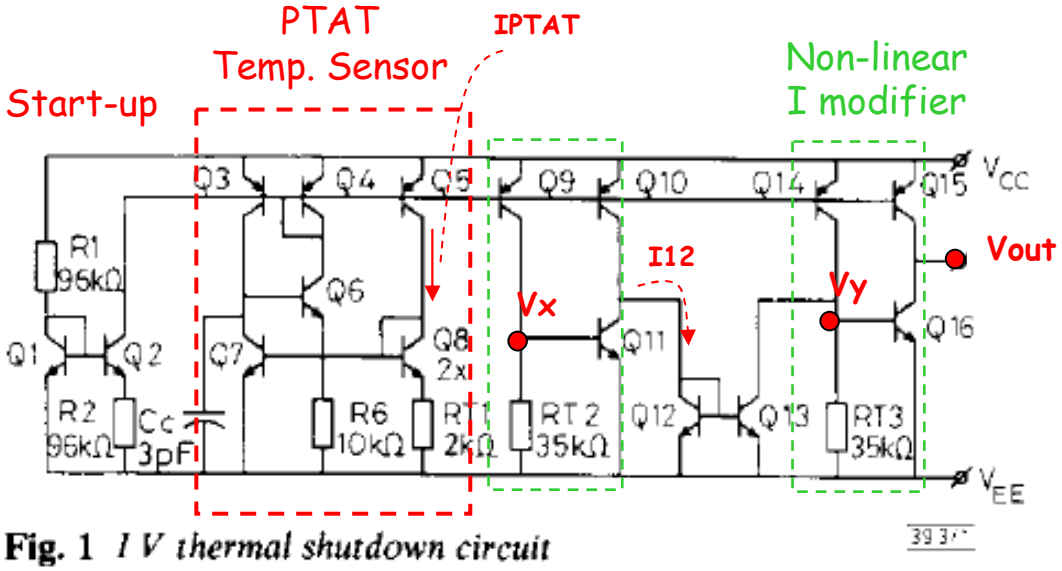
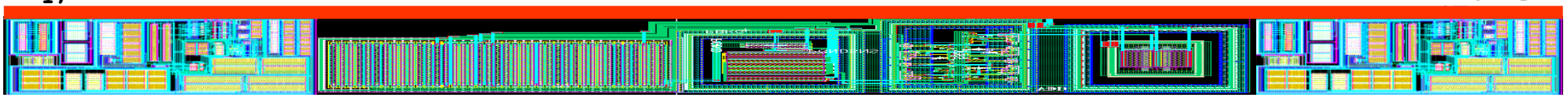
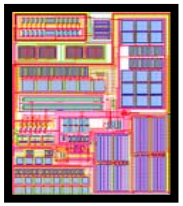


Fig. 1 *1 V thermal shutdown circuit*

"Integrated 1V Thermal Shutdown Circuit", M.H. Nagel et al.,
IEEE Electronics Letters,
7th Mat 1992, Vol.28, No. 10, p.969.





Design procedure of Thermal Shut-Down Circuit

1) $I_{PTAT} = \frac{kT\ln(n)}{qR_{T1}}$,

If set $n = 2$, $I_{PTAT} = 10uA$, get R_{T1} value

2) $T_Z(K) \sim \frac{qV_{g0}}{k} \frac{1}{\frac{R_{T2}}{R_{T1}} - \ln\frac{I_{PTAT}}{2c_1}}$,

Where $V_{g0} = 1.176V$ is bandgap voltage of Silicon

at 0^oK &

c_1 is saturation current coefficient.

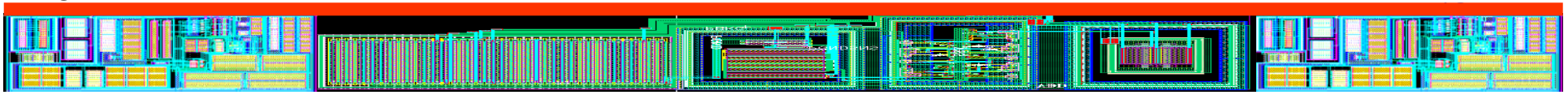
c_1 ~ IPTAT/2e-6 (reverse engineering formula!)

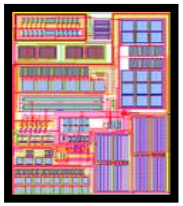
$T_{Z,H} = 150^oC$, from the above equation, get $R_{T2,H}$ value.

$T_{Z,L} = 130^oC$, get $R_{T2,L}$ value.

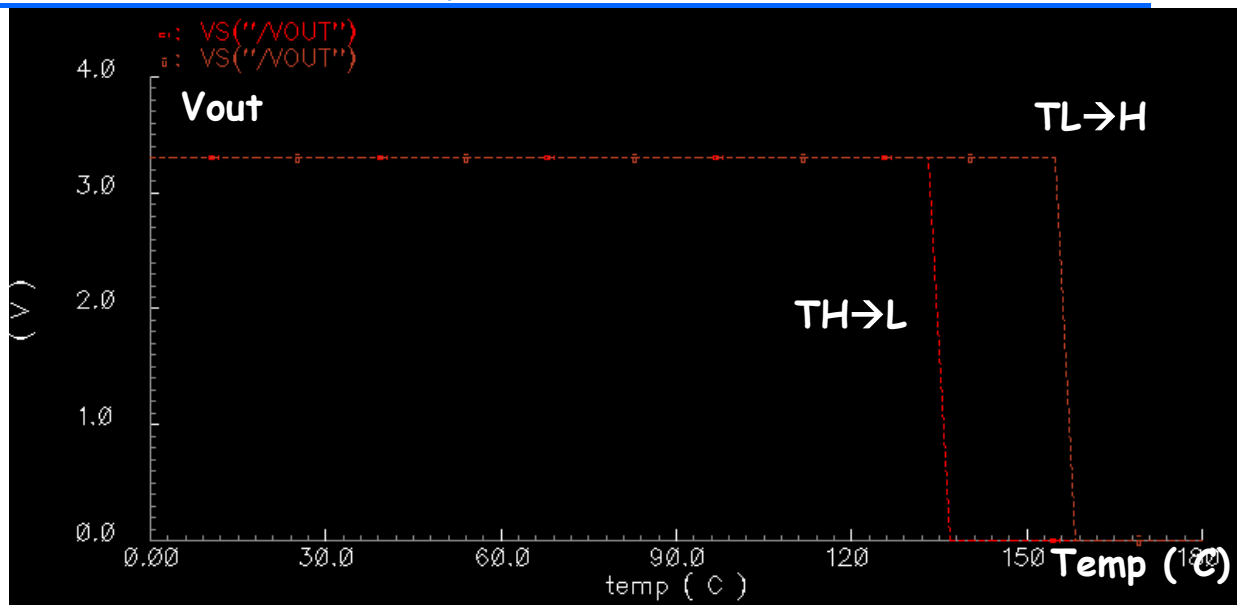
3) Please use a NMOS SW to change between $R_{T2,L}$ and $R_{T2,H}$ to get temp. hysteresis.

You will need to adjust $R_{T2,L}$ to get the right temp.

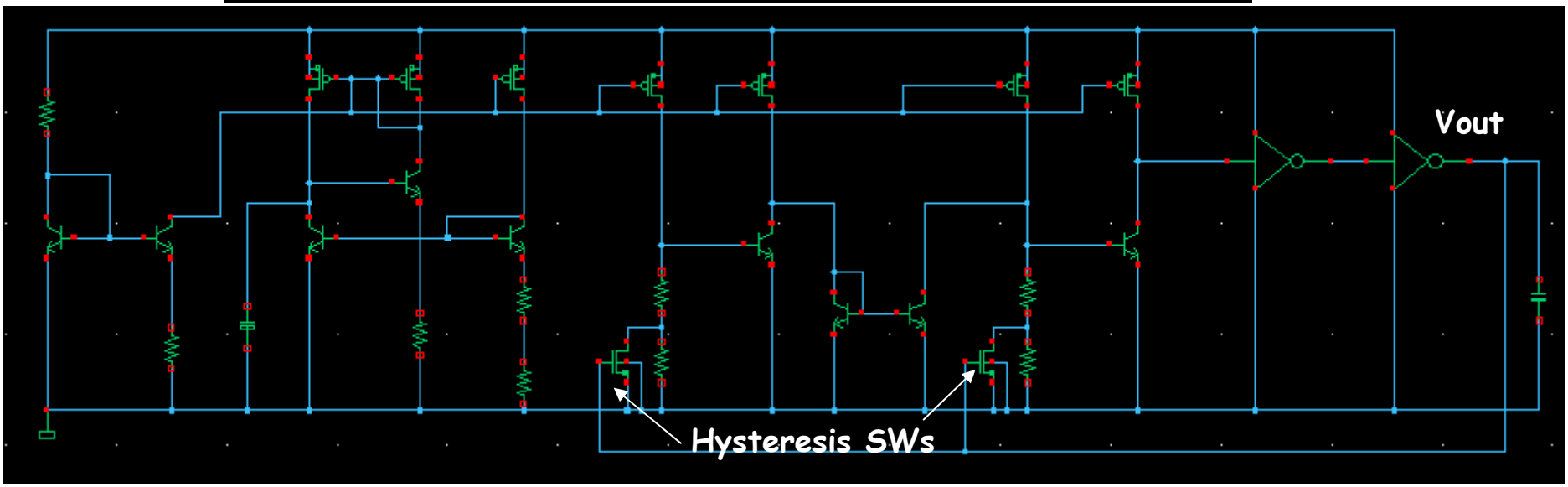


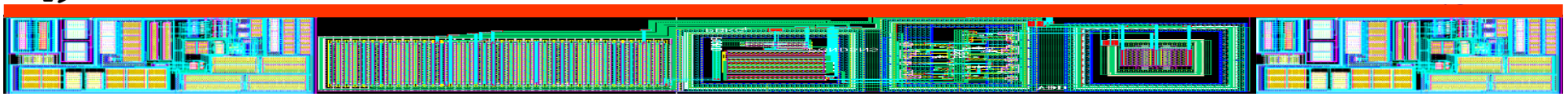


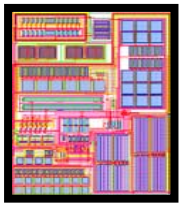
BiCMOS version of thermal shut down circuit



UTD Models







Summary

- The final design values should be reported based on simulation results. The values in this design guide is a good starting point.
- Good Luck!
- No late homework!
- Any HW related questions should be asked before the due date. Students are also encouraged to attend announced tutorial sessions and office hours. Any special request for additional meeting and questions raised after HW due date will be answered or arranged based on the availability of schedule.