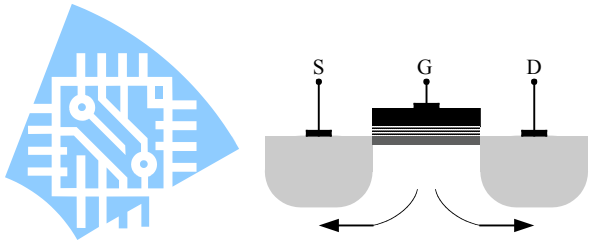

ELE6308

Microélectronique analogique et mixte

--- Amplificateur opérationnel ---

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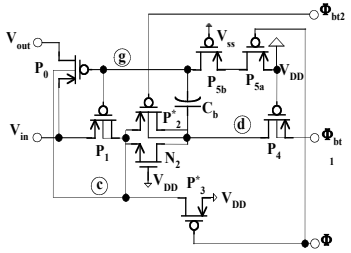


Amplificateur opérationnel

Plan

I. Vue globale

II. Conception DC (gain, polarisation, «offset»)

III. Conception AC: faibles signaux (compensation)

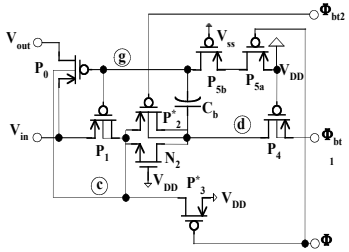
IV. Conception AC: forts signaux (Slew Rate)

V. Critères de performance et guide de design (Paramètres DC & AC).

VI. Generality (CMRR, PSRR, …)

VII. Input Common Mode Range

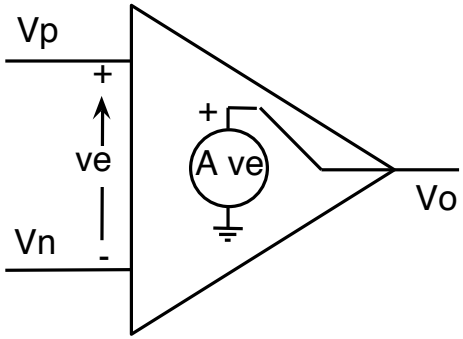
VIII. Noise in CMOS Opamps



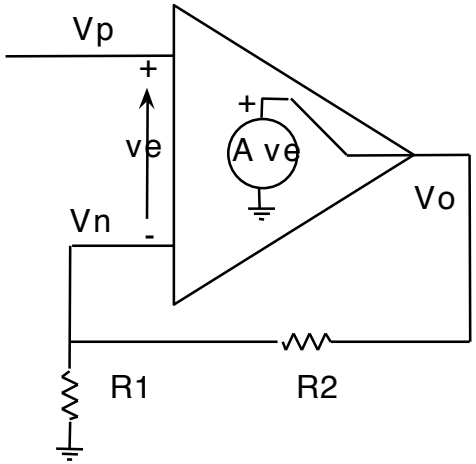
Amplificateur opérationnel

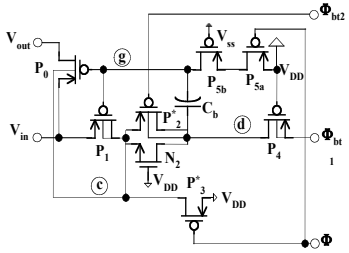
Vue globale

- **Catégories d'ampop idéal**
  - En boucle ouverte



  - En boucle fermée

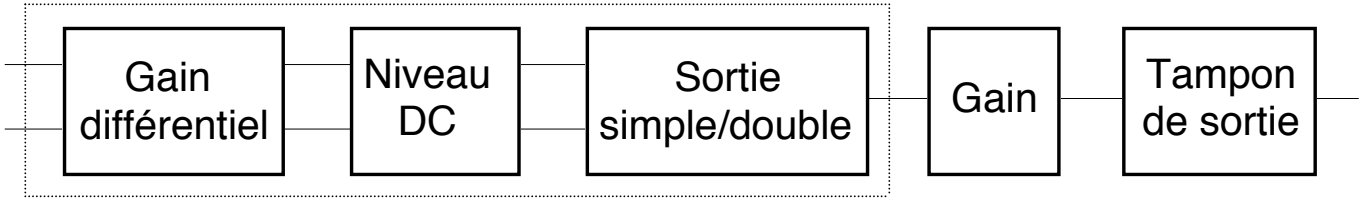




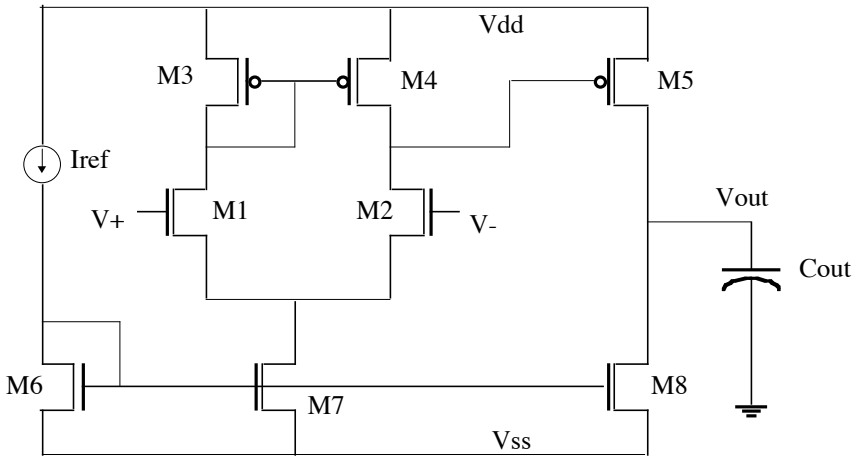
Amplificateur opérationnel

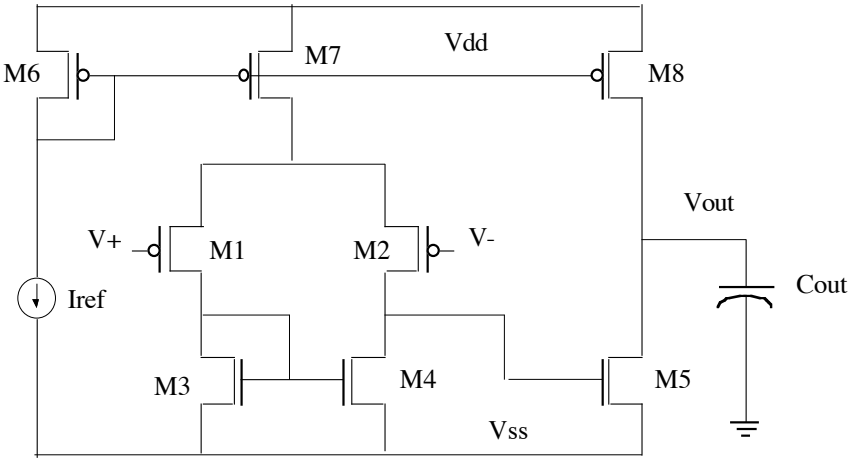
Vue globale (suite)

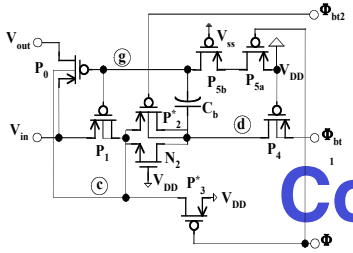
- **Fonctions internes d'un ampop**



- **Configuration de base d'un ampop en CMOS**



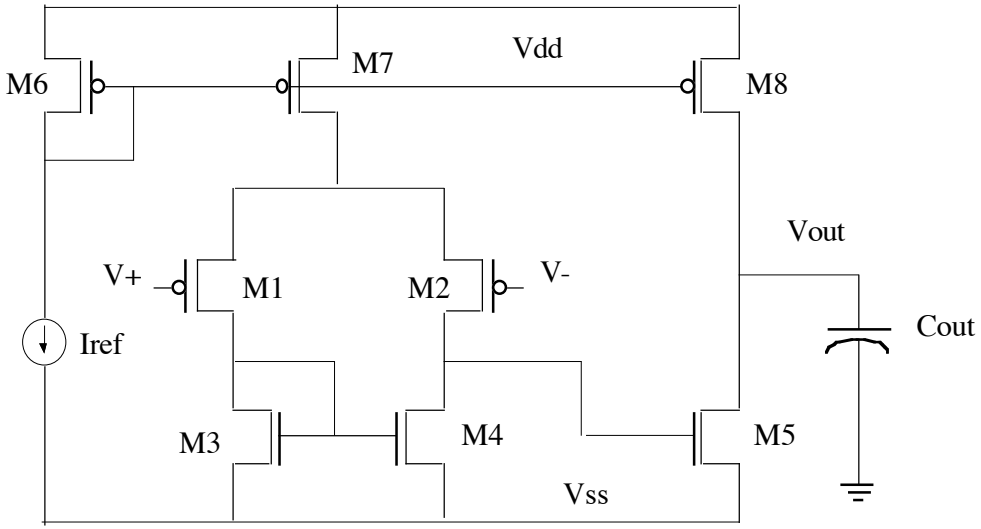


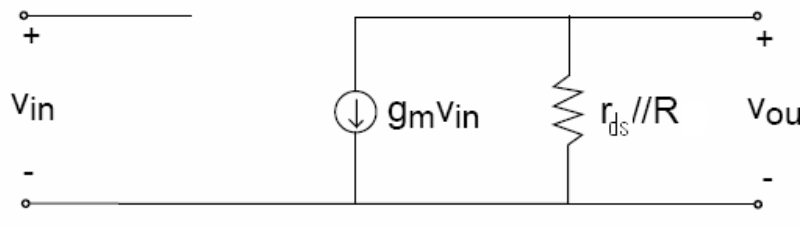


Amplificateur opérationnel

Conception DC (gain, polarisation, etc)

- **Gain en boucle ouverte - faibles signaux**



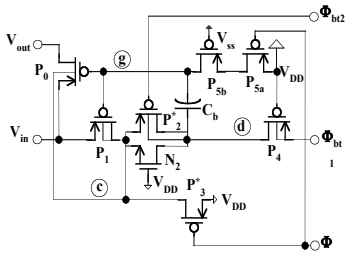


$$A_v = \frac{v_{out}}{v_{in}} = -g_m\left(r_{ds} \parallel R\right) \cong -g_m R$$

G_{oA} = gm ro = gm1 (ro2 ll ro4) gm5 (ro5 ll ro8)

- **Polarisation DC**
  - **Valeurs de courant**

⇒ Dissipation de puissance, «Slew rate» et gain en boucle ouverte



Amplificateur opérationnel

Conception DC (suite)

- **Tension de décalage (Offset)**
  - **Systématique**

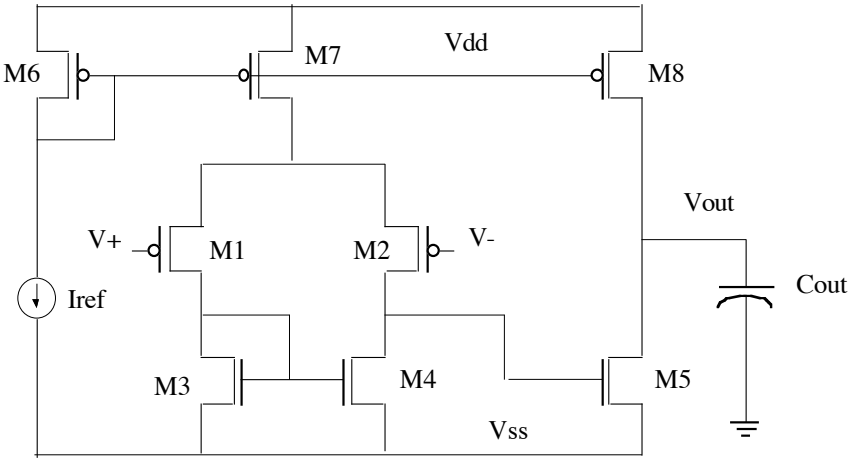
Résulte de la tension de sortie du premier étage. Il ne fournit donc pas la valeur désirée à l'entrée du second étage pour forcer la tension de sortie à zéro. Les valeurs appropriées pour obtenir Vout = 0 sont:

$$V_{DS3} = V_{DS4} = V_{GS4} = V_{GS5}$$

$$V_{GS4} = V_{TH} + \sqrt{\frac{2I_{D4}}{\mu C(W/L)_4}}$$

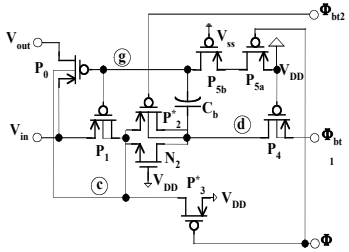
$$V_{GS5} = V_{TH} + \sqrt{\frac{2I_{D5}}{\mu C(W/L)_5}}$$

$$\frac{I_{D4}}{(W/L)_4} = \frac{I_{D5}}{(W/L)_5} = \frac{I_{D8}}{(W/L)_8}$$



$$I_{D4} = \frac{I_{D7}}{2} \qquad \frac{(W/L)_5}{(W/L)_4} = 2\frac{(W/L)_8}{(W/L)_7}$$

Pour L identiques, et
W4 = W5 ➡ W8 = W7/2.



Amplificateur opérationnel

Conception DC (suite)

- **Tension de décalage (suite)**
  - **«Offset» aléatoire**

$$I_D = \frac{\mu C_{ox}}{2}\frac{W}{L}\left(V_{GS}-V_{th}\right)^2 \Rightarrow V_{OS} \equiv \Delta V_{GS}\big|_{\Delta V_O=0} = -\underbrace{\frac{1}{2}\sqrt{\frac{2I_D}{\mu C_{ox}\left(W/L\right)}}}_{V_{GS}-V_{th}}\left[\frac{\Delta I_D}{I_D}-\frac{\Delta\left(W/L\right)}{W/L}\right]-\Delta V_{th}$$

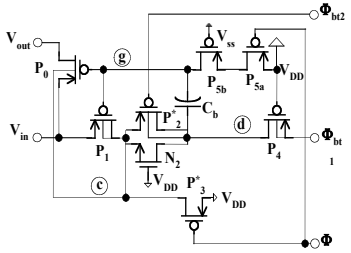
Étage différentielle: $V_{OS} = \frac{V_{GS}-V_{th}}{2}\left(\frac{\Delta R}{R}+\frac{\Delta\left(W/L\right)}{W/L}\right)+\Delta V_{th}$ $\qquad \frac{\Delta I_D}{I_D} = -\frac{\Delta R}{R}$

$$V_{OS} = \Delta V_{T(1-2)} + \Delta V_{T(3-4)}\,\frac{g_{m3}}{g_{m1}} + \frac{(V_{GS}-V_T)_{(1-2)}}{2}\left[\frac{-\left(\frac{\Delta W}{L}\right)_{(1-2)}}{\left(\frac{W}{L}\right)_{(1-2)}} - \frac{\left(\frac{\Delta W}{L}\right)_{(3-4)}}{\left(\frac{W}{L}\right)_{(3-4)}}\right]$$

Dû à la différence entre transistors d'entrée.

Dû à la différence entre les charges après un facteur de réduction par les transconductances.

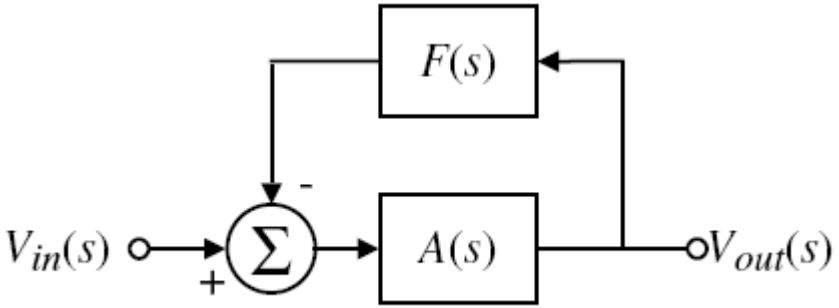
Dû à la différence de W/L des entrées et des charges lors de l'opération à faible polarisation.

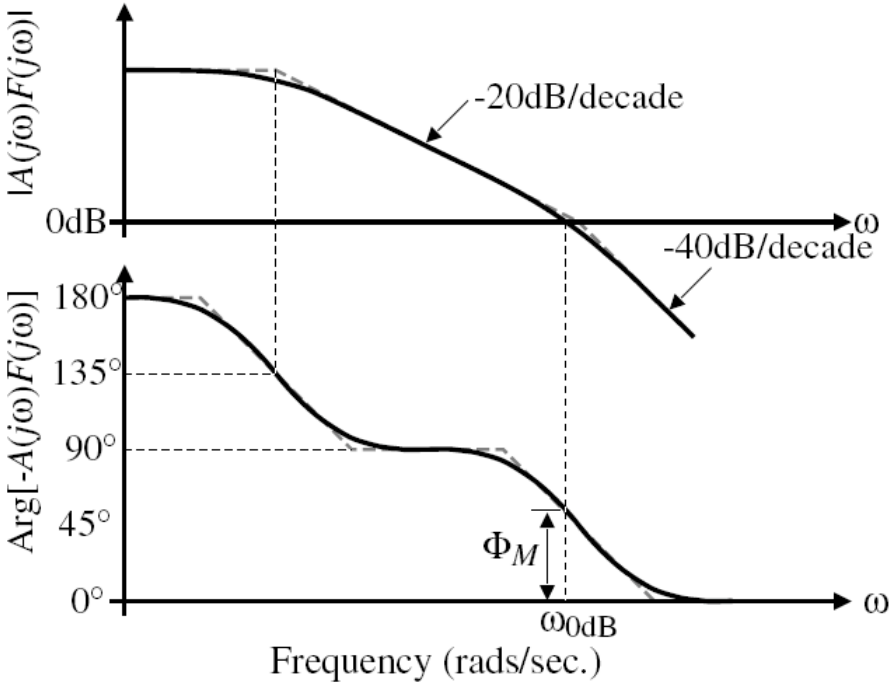


Amplificateur opérationnel

Conception AC: faibles signaux

- **À quoi sert la compensation ?**



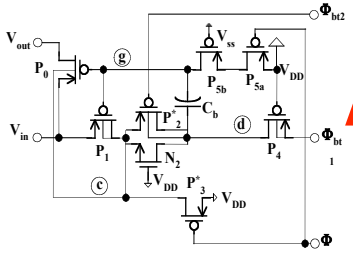


$$\text{Open-loop gain} = L(s) = -A(s)F(s)$$

$$\text{Closed-loop gain} = \frac{V_{out}(s)}{V_{in}(s)} = \frac{A(s)}{1+A(s)F(s)}$$

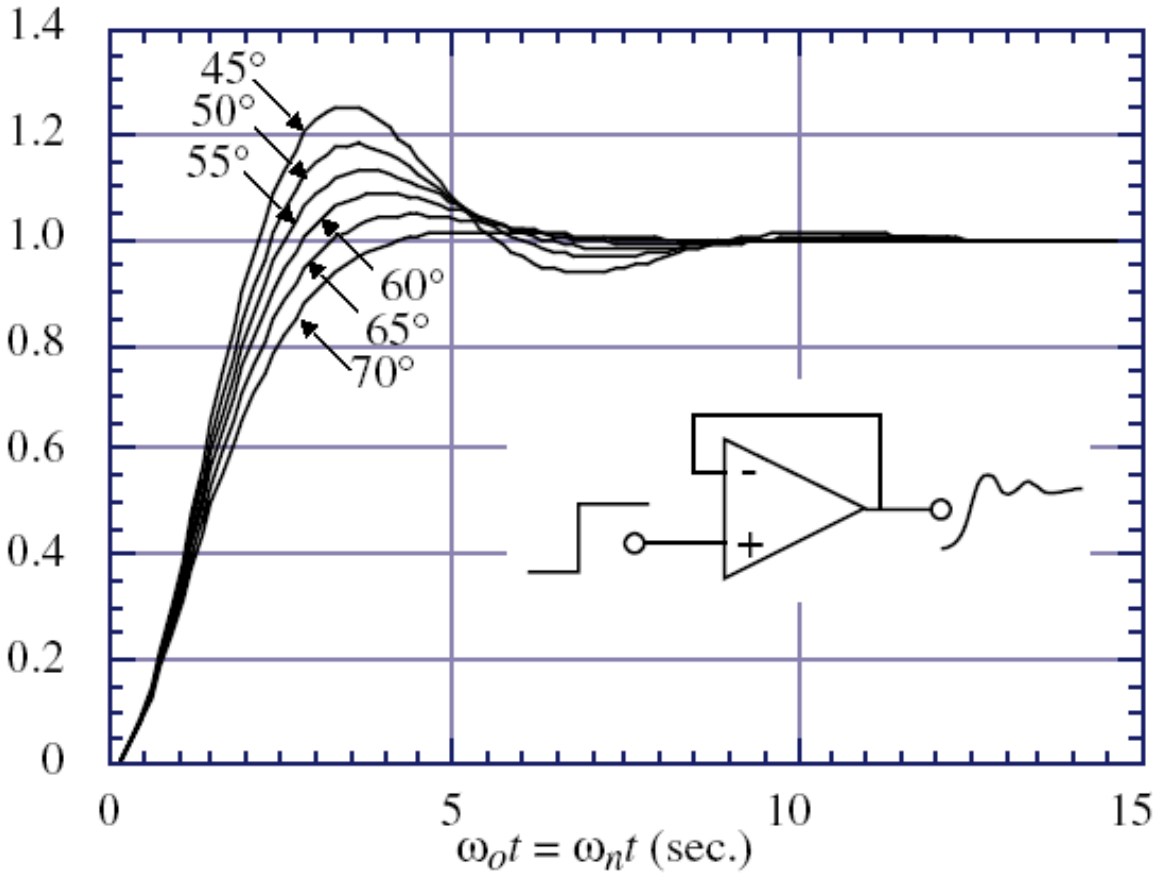
$$\text{Phase margin} = \Phi_M = \text{Arg}[-A(j\omega_{0\text{dB}})F(j\omega_{0\text{dB}})] = \text{Arg}[L(j\omega_{0\text{dB}})]$$

Pour un gain unitaire, la sortie est déphasée de 180° (interne) + un déphasage de 180° causé par l'entrée négative. Ceci consiste en un «feedback» positif qu'il faut éviter.

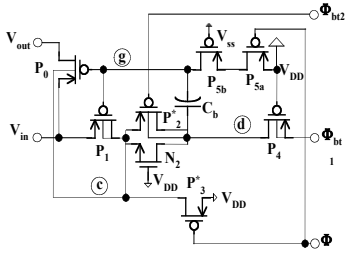


Amplificateur opérationnel

Conception AC: faibles signaux

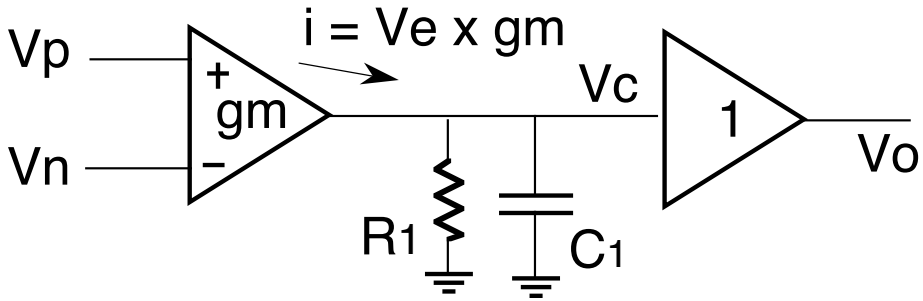


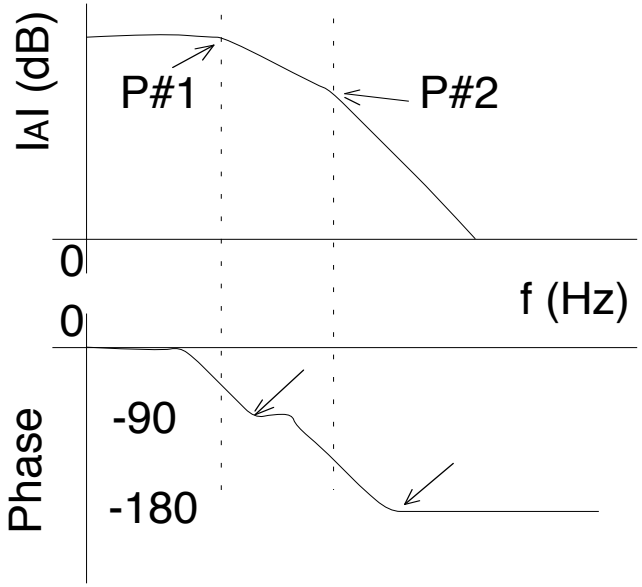
Marge de phase ≥ 45°



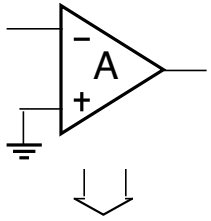
Amplificateur opérationnel

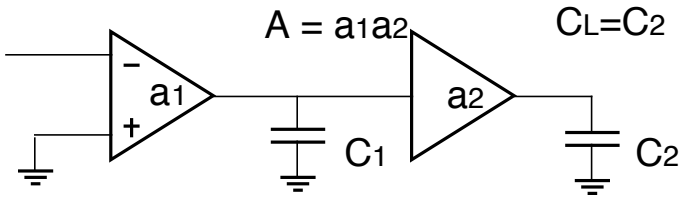
Conception AC: faibles signaux



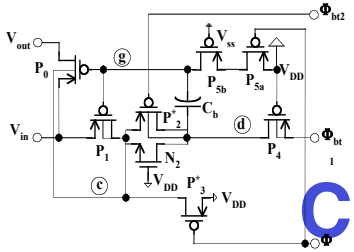


Gain et phase vs fréquence





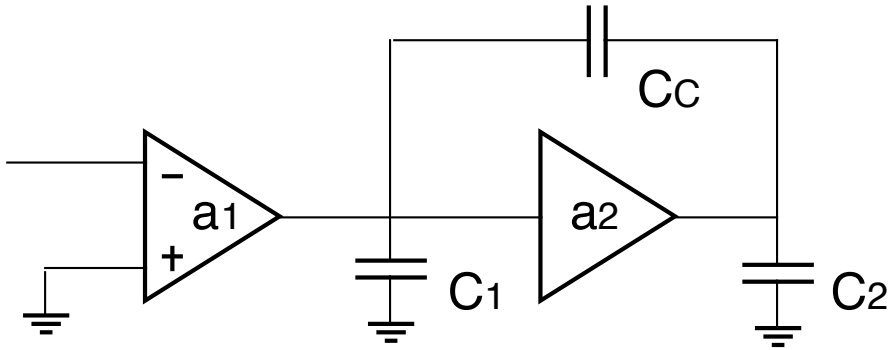
C1 et C2 sont des capacités parasites

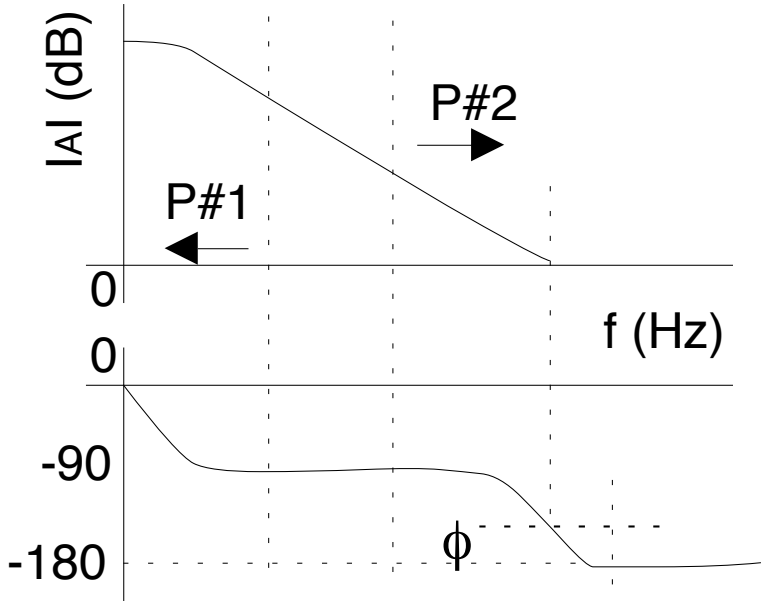


Amplificateur opérationnel

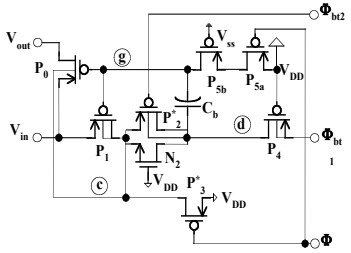
Conception AC: faibles signaux (suite)

- **Compensation par déplacement de pôle**
  - **Description qualitative**





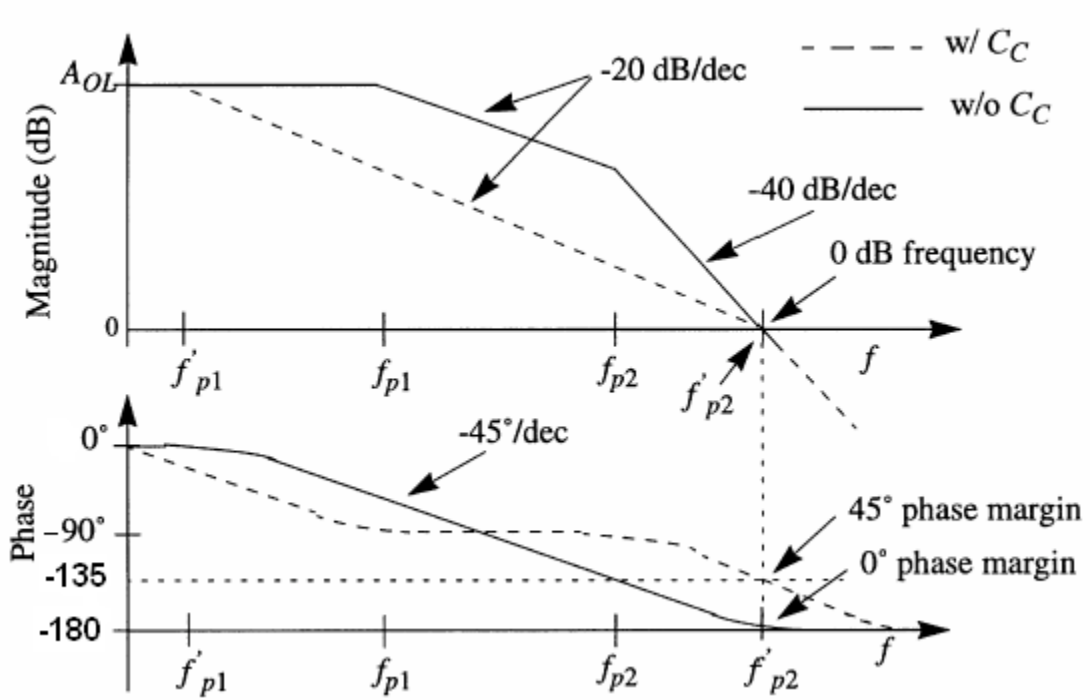
Cc déplace le pôle #1 vers la basse fréquence et le pôle #2 vers la haute fréquence.



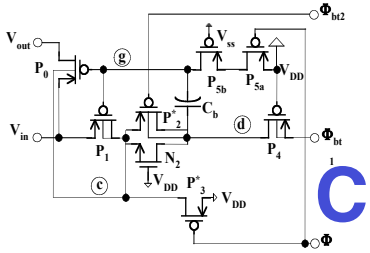
Amplificateur opérationnel

III. Conception AC: faibles signaux (suite)

- **Compensation par déplacement de pôle**
  - **Description qualitative**



À $|A| = 1$, $f = -135°$, et la marge est de 45°.

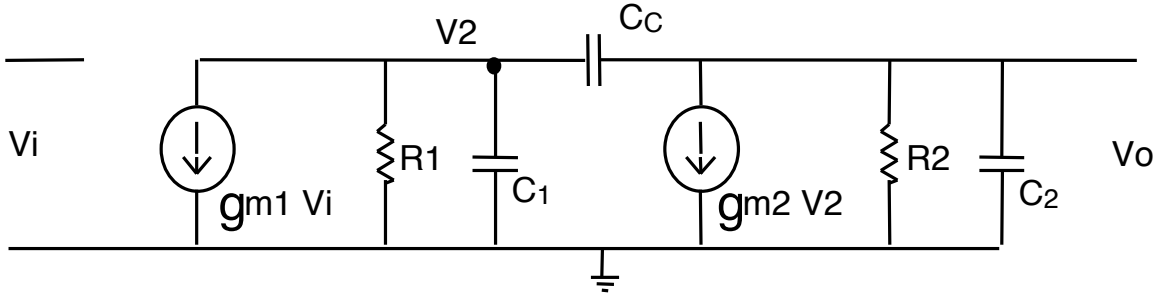


Amplificateur opérationnel

Conception AC: faibles signaux (suite)

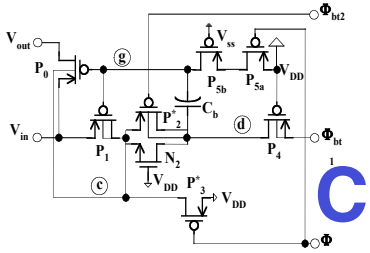
- **Compensation par déplacement de pôle (suite)**
  - **Description quantitative**

→ Modèle AC simplifié de l'ampop



$$\frac{V_o}{V_i} = \frac{g_{m1}g_{m2}R_1R_2\left(1-C_c\frac{s}{g_{m2}}\right)}{1 + s\left[(C_2 + C_c)R_2 + (C_1 + C_c)R_1 + g_{m2}R_1R_2C_c\right] + s^2 R_1R_2\left(C_1C_2 + C_CC_1 + C_CC_2\right)}$$

$$\text{Si } P_1 \ll P_2,\ D(s) = 1 - s\left(\frac{1}{P_1} + \frac{1}{P_2}\right) + \frac{s^2}{P_1P_2)} = 1 - \frac{s}{P_1} + \frac{s^2}{P_1P_2)}$$



Amplificateur opérationnel

Conception AC: faibles signaux (suite)

- Compensation par déplacement de pôle (suite)
  - **Description quantitative (suite)**

→ Les pôles

$$P1 = \frac{-1}{(C_1 + C_C)R_1 + (C_2 + C_C)R_2 + g_{m2}R_1R_2C_c} = \frac{-1}{g_{m2}R_2C_cR_1}$$

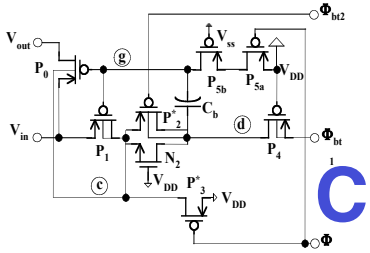
$$P_1P_2 = \frac{1}{R_1R_2(C_1C_2 + C_CC_1 + C_CC_2)}$$

$$P2 = \frac{-(g_{m2}R_2)C_cR_1}{R_1R_2(C_2C_1 + C_cC_1 + C_cC_2)} = \frac{-g_{m2}C_c}{C_2C_1 + C_cC_1 + C_cC_2}$$

☞ Pôle P1 a été poussé vers les basses fréquences par Cc (multiplicateur Miller).

☞ Pôle P2 a été déplacé vers les hautes fréquences en raison de la boucle (R2 ll 1/gm2).

$$P2 = \frac{-g_{m2}}{C_1 + C_2}$$



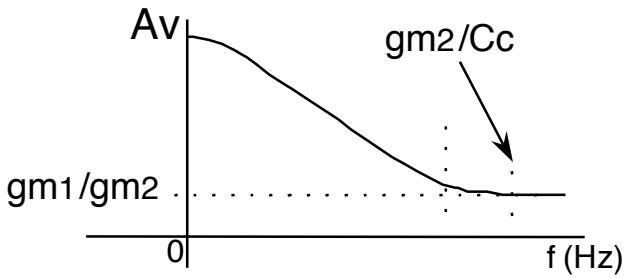
Amplificateur opérationnel

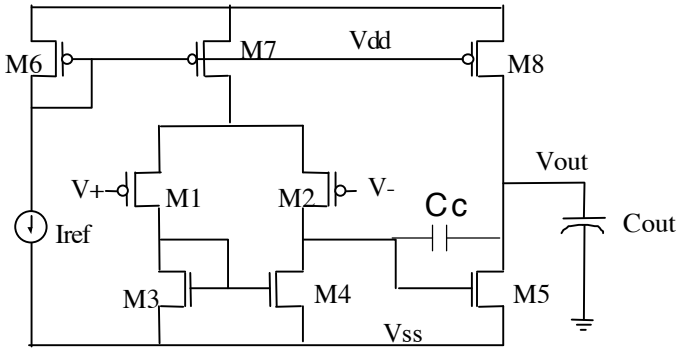
Conception AC: faibles signaux (suite)

- Compensation par déplacement de pôle (suite)
  - **Description quantitative (suite)**

→ Le zéro (z = gm2/Cc)

- ☞ À haute fréquence Cc se comporte comme un court-circuit;
- ☞ M5 se comporte comme une résistance de valeur 1/gm2 (une diode);
- ☞ Le gain Av devient = - gm1 (R1 ll 1/gm2) @ - gm1/gm2.

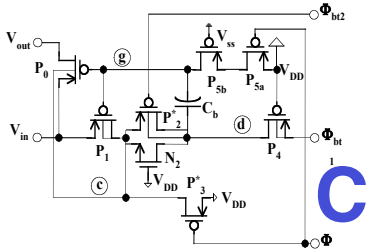




→ Annulation du zéro

- ☞ Pour le MOS, le zéro est proche de la fréquence donnant un gain unitaire.

$$\text{Gain DC} \times P1 \ @ \ \frac{gm1\ R1\ gm2\ R2}{gm2\ R2\ R1\ Cc} \ @ \ gm1 / Cc$$



Amplificateur opérationnel
Conception AC: faibles signaux (suite)

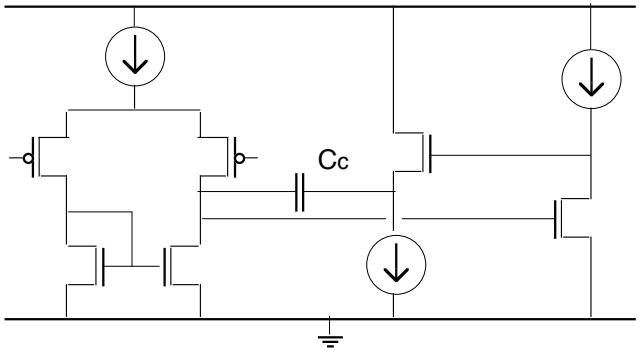
- Compensation par déplacement de pôle (suite)
  - **Description quantitative (suite)**

→ Annulation du zéro (suite)

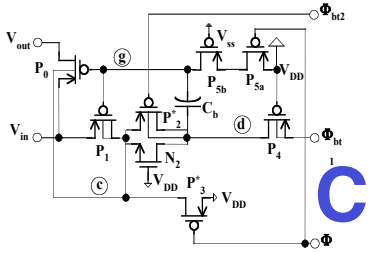
Le rapport: $\frac{\text{Gain unitaire}}{\text{zéro}}$ donne gm1/gm2

Si gm2 >> gm1 Þ zéro est peu important

→ Annulation à l'aide d'un suiveur



Le suiveur prévient le «feedforward», mais surface et puissance sont dégradées.

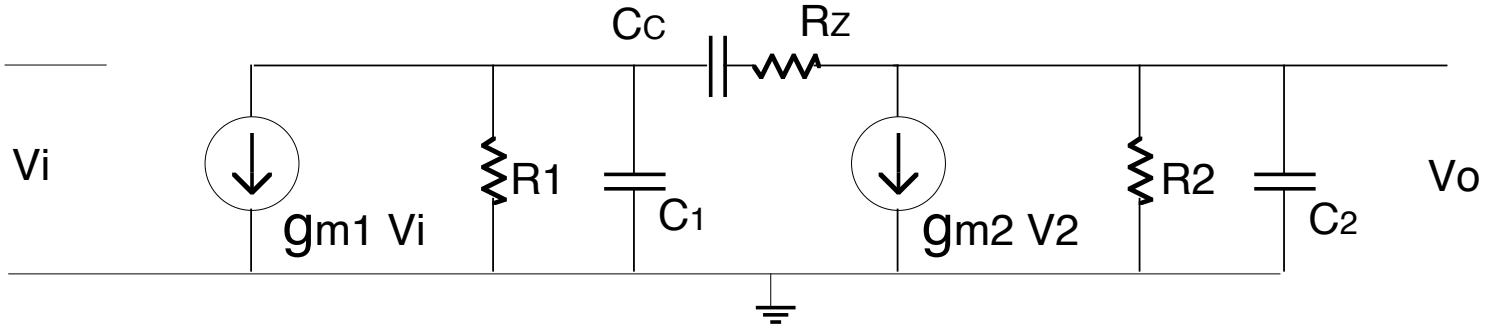


Amplificateur opérationnel

Conception AC: faibles signaux (suite)

- Compensation par déplacement de pôle (suite)
  - **Description quantitative (suite)**

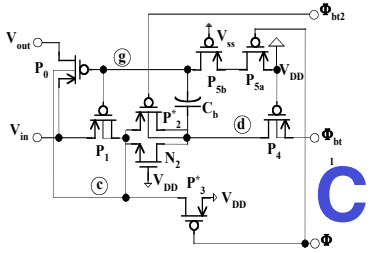
→ Annulation du zéro à l'aide d'une résistance (Rz)



$$z = \frac{1}{C_C\left(\frac{1}{g_{m2}} - R_Z\right)}$$

Si Rz = 1/gm2 Þ le zéro est annulé.

Si Rz > 1/gm2 Þ le zéro se déplace vers la partie gauche et par le fait même la marge de phase est améliorée.



Amplificateur opérationnel

Conception AC: faibles signaux (suite)

- Compensation par déplacement de pôle (suite)
  - **Description quantitative (suite)**

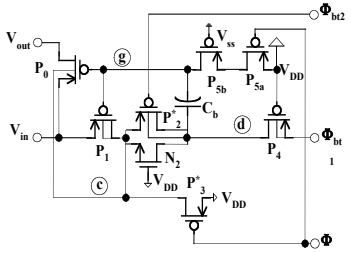
→ Effets de la charge capacitive (C2)

$$P_2 = -\frac{g_{m2}C_c}{C_1C_2 + C_CC_1 + C_CC_2} \approx -\frac{g_{m2}C_c}{C_CC_2} = \frac{g_{m2}}{C_2} \qquad C_C, C_2 >> C_1$$

☞ Le gain unitaire est gm1/Cc. On veut placer P2 au point du gain unitaire avec une marge de phase ≥ 45°.

☞ gm1/Cc £ gm2/C2;
gm2 est de même ordre de grandeur que gm1 Þ C2 £ Cc.

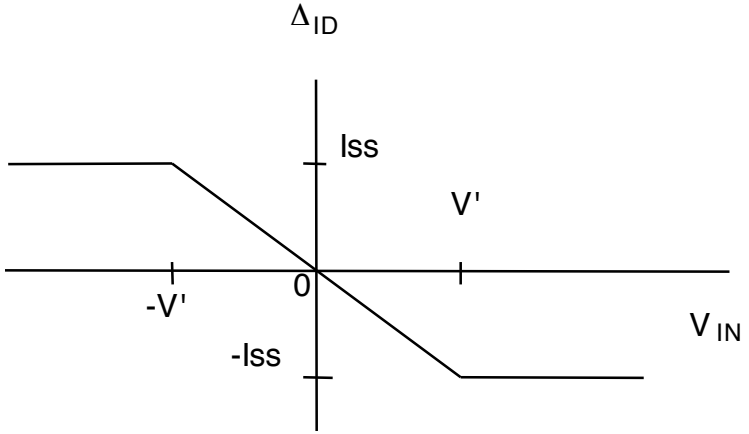
La charge maximale qu'on peut alimenter est donc C2 = Cc.



Amplificateur opérationnel

Conception AC: forts signaux

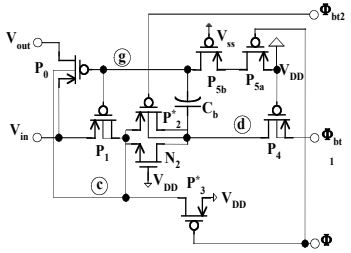
- **Réaction de la sortie «Slew Rate»**
  - **Les causes**



Si $V_{IN} > V'$ Þ le courant maximum de sortie est Iss:

$$V_O = \frac{1}{C_C}\int I_{SS}\,dt \;; \quad \frac{dV_O}{dt} = \frac{I_{SS}}{C_c}$$

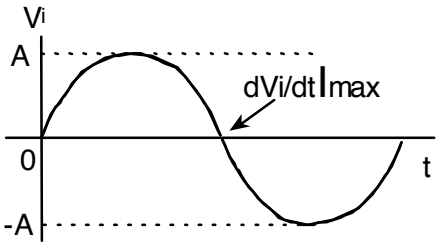
Le changement (augmentation) du voltage de sortie Vo en fonction du temps est linéaire.

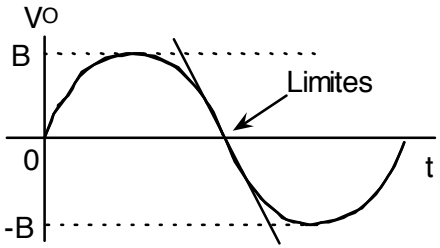


Amplificateur opérationnel

Conception AC: forts signaux (suite)

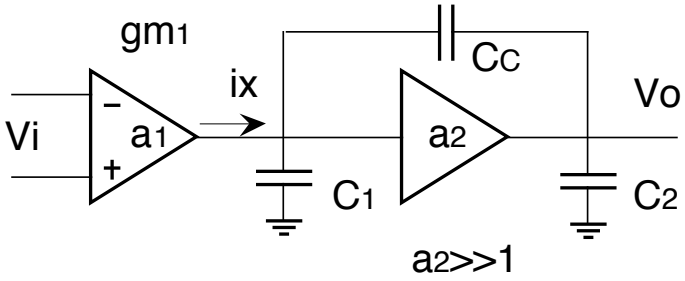
- **Réaction de la sortie «Slew Rate» (suite)**
  - **Effets du «Slew rate» sur les signaux de forte amplitude**





$V_i = A \sin \omega t \Rightarrow \left.\frac{dVi}{dt}\right|_{MAX} = \omega A \Rightarrow$ Slew rate $< \omega A$

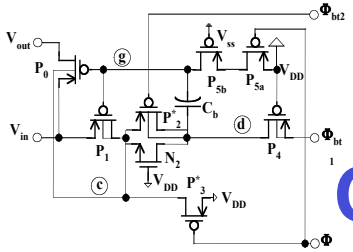
  - **Evaluation du «slew rate»**



→ Limites du «Slew rate»

$$\frac{dV_O}{dt} = \frac{I_{XM}}{Cc} \qquad \frac{\Delta I_X}{\Delta V_i} = g_{m1}$$

$$\frac{\Delta V_O}{\Delta I_X} = \frac{1}{sC} = \frac{1}{j\omega C} \qquad \frac{\Delta V_O}{\Delta V_i} = \frac{g_{m1}}{j\omega C}$$



Amplificateur opérationnel

Conception AC: forts signaux (suite)

- **Réaction de la sortie «Slew rate» (suite)**
  - **Evaluation du «Slew rate» (suite)**

De la théorie de compensation, nous savons que le gain unitaire doit se produire au pôle #2 le plus dominant .

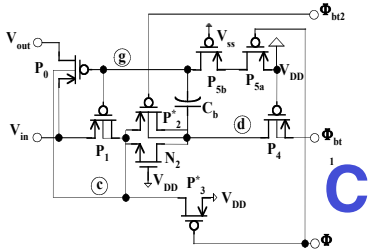
$$\frac{\Delta V_O}{\Delta V_i} = |1| = \frac{g_{m1}}{\omega_2 C} \qquad \therefore \frac{1}{C} = \frac{\omega_2}{g_{m1}}$$

$$\text{Slew Rate} = \frac{dV_O}{dt} = \frac{I_{XM}\omega_2}{g_{m1}} \qquad \left(\frac{dV_O}{dt} = \frac{I_{XM}}{Cc}\right)$$

$$SR = \frac{2I_{D1}\omega_2}{g_{m1}}$$

$$SR = \left(V_{GS} - V_{th}\right)_1 \omega_2$$

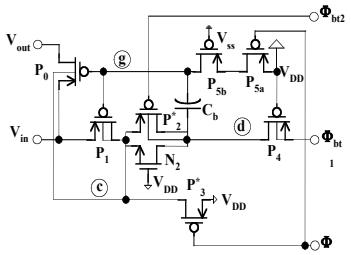
Pour améliorer le SR, augmenter V_{GS} - V_T



Amplificateur opérationnel

Critères de performance et guide de design

- **Paramètres DC**
  - **Gain intrinsèque**
    - → Composants longs pour obtenir impédance de sortie élevée
    - → Composants larges pour obtenir transconductance élevée
    - → Circuits cascodes.
    - → Courant de polarisation faible.
  - **Gamme de variation de sortie**
    - → Pas de circuits cascodes.
  - **Voltage d'«offset» (CMR)**
    - → Gros composants
    - → Courant de polarisation faible.
  - **Dissipation d'énergie**
    - → Courant de polarisation faible.



Amplificateur opérationnel

Critères de performance (suite)

- **Paramètres AC**
  - **Fréquence de gain unitaire gm1/Cc**
    - → Courant de polarisation élevé
    - → Composants à canaux courts
  - **«Slew rate»**
    - → Courant de polarisation élevé
- **Autres paramètres de design**
  - **Bruit d'entrée équivalent**
  - **Réjection de l'alimentation**
- **Contraintes de design des circuits intégrés**
  - **Tension d'alimentation**
  - **Surface**

Advanced Opamps

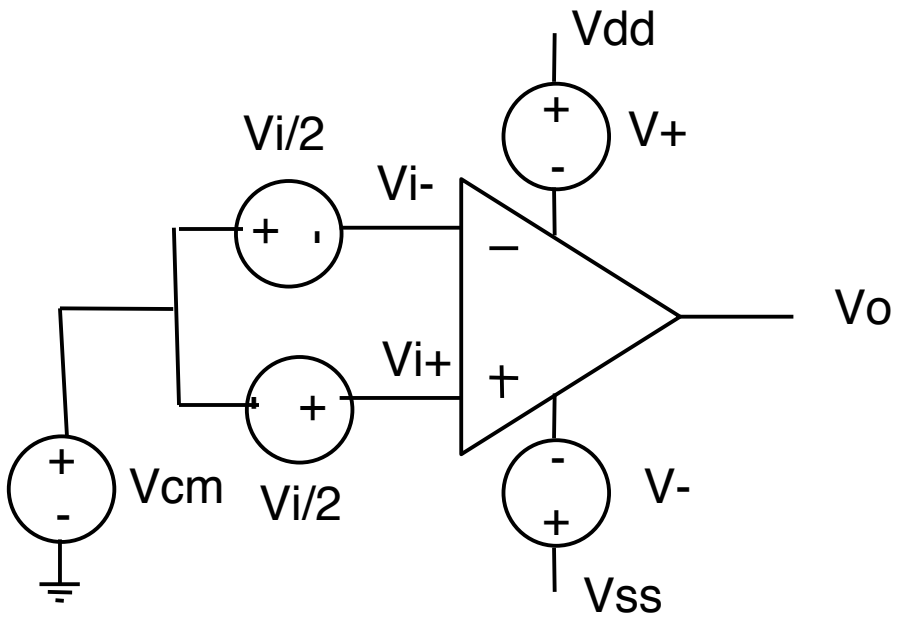
- **Generality**

$$v_i = v_i^+ - v_i^-$$

$$v_{cm} = \frac{v_i^+ + v_i^-}{2}$$

$$v_i^+ = v_{cm} + \frac{v_i}{2}$$

$$v_i^- = v_{cm} - \frac{v_i}{2}$$

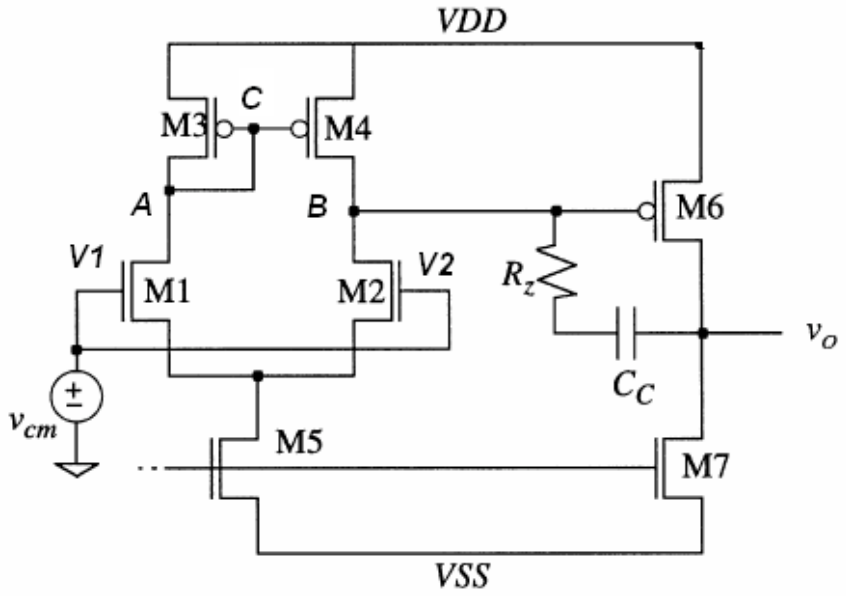


$$v_O = A_{dm} v_i + A_{cm} v_{cm} + A^+ v^+ + A^- v^-$$

CMRR

- The common-mode rejection ratio (CMRR) measures how well the amplifier can reject signals common to both inputs

$$\text{CMRR} = 20\log\left|\frac{A_{dm}}{A_{cm}}\right| = 20\log\left|\frac{v_o/v_i}{v_o/v_{cm}}\right|$$



- The differential stage determines how well the entire opamp rejects common mode signals.

$$\text{CMRR}_{\text{Op Amp}} = \text{CMRR}_{\text{ Input Stage}}$$

CMRR (Cont'd)

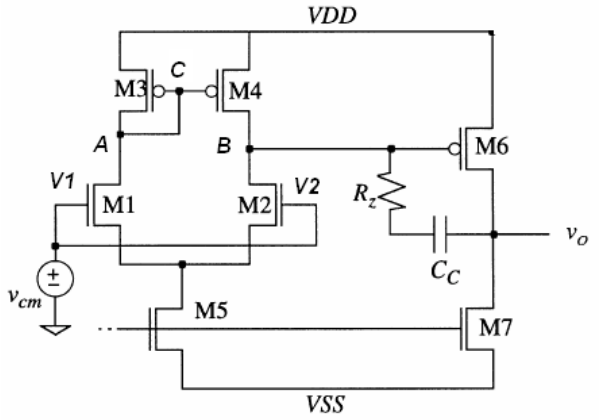
• The common-mode signal appearing on the drains of M3 and M4 will be identical

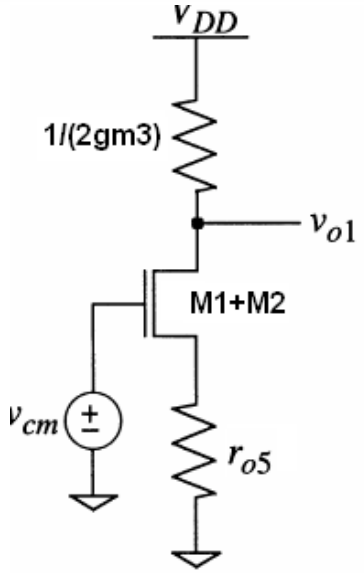
$$\frac{v_{o1}}{v_{cm}} = -\frac{1/g_{m3,4}}{2r_{o5}}$$

$$\text{CMRR} = 20\log\left|\frac{A_{dm}}{A_{cm}}\right| = 20\log\left|\frac{v_o/v_i}{v_o/v_{cm}}\right|$$

$$\text{CMRR} = 20\log(2g_{m1,2}g_{m3,4}(r_{o2}||r_{o4})r_{o5})$$

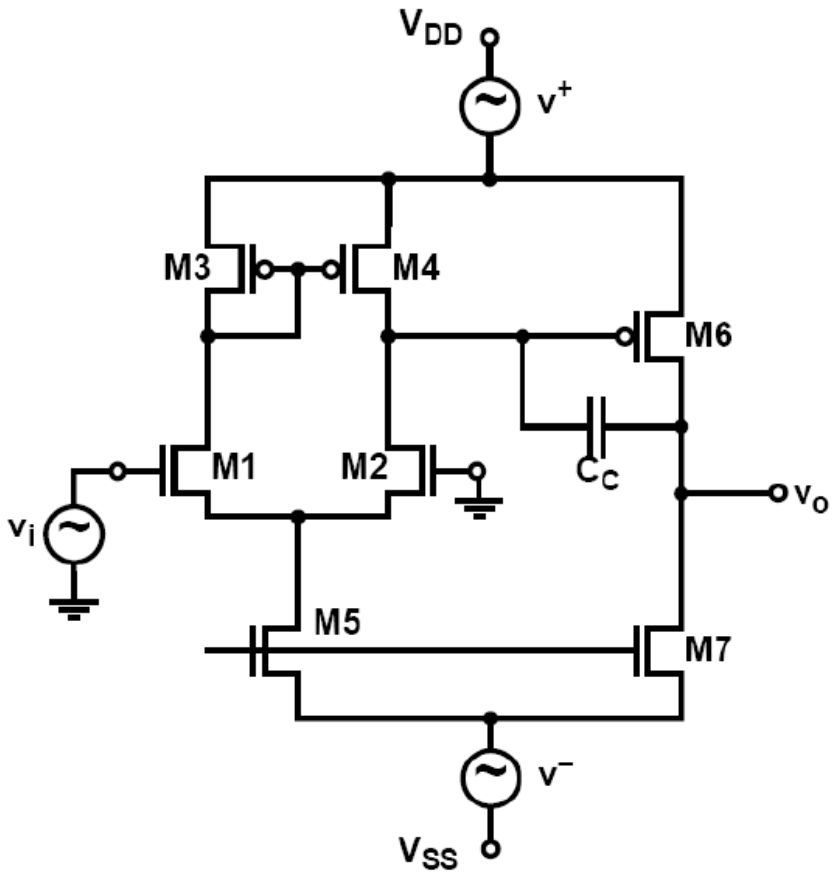
• The most efficient manner in which to increase the CMRR of this amplifier is to increase the resistance r_{o5}



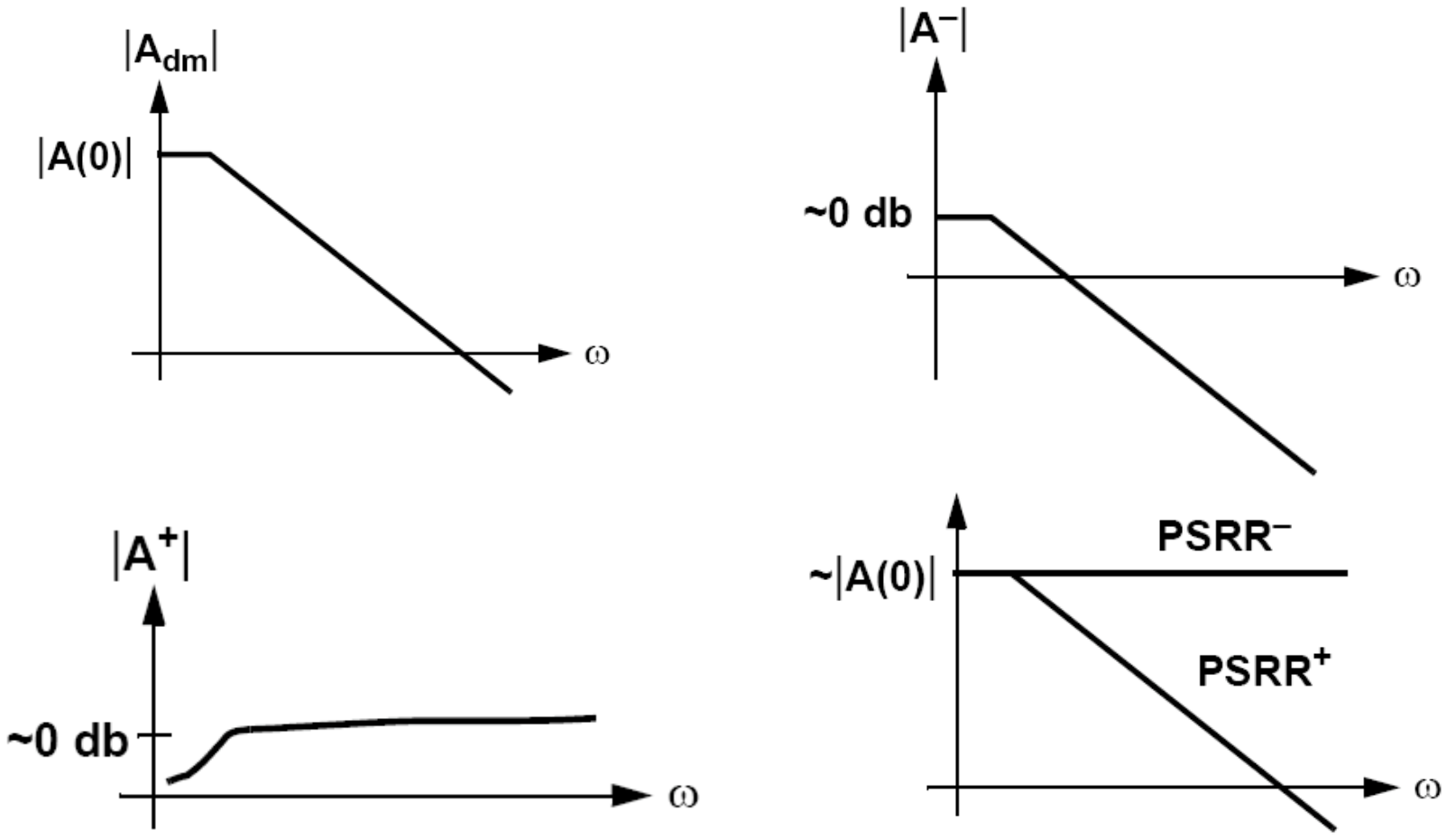


PSRR of 2-Stage Opamp (cont'd)

- A^- is largely determined by go5 & go7. It is typically ≤ unity at low frequencies and, more importantly, it rolls off with frequency in the same fashion as the open loop gain.
- PSRR– remains approximately constant with frequency.
- $A^+ \approx 1$ except at very low frequencies
- PSRR+ falls with frequency along with the open loop gain (Adm).
- At frequencies above the dominant pole (which is determined by C_C), C_C "shorts" the gate and drain of M6.



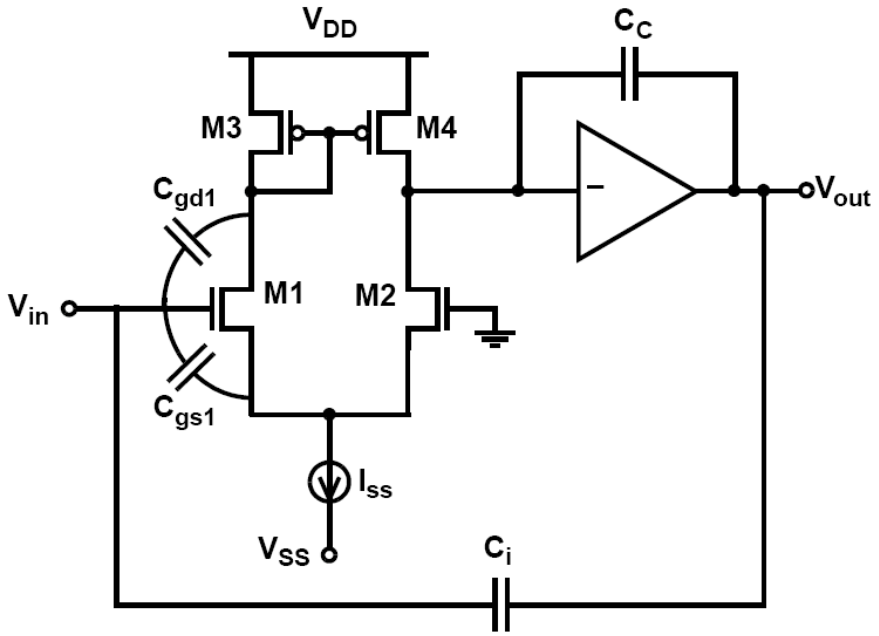
PSRR of 2-Stage Opamp (cont'd)



PSRR of 2-Stage Opamp (cont'd)

• Another significant source of coupling between the supply rails and the output is commonly referred to as "supply" capacitance. This term refers to the coupling from one, or both, of the supply rails into the input nodes of an op amp. It is primarily in circuits such as single-ended sampled-data integrators

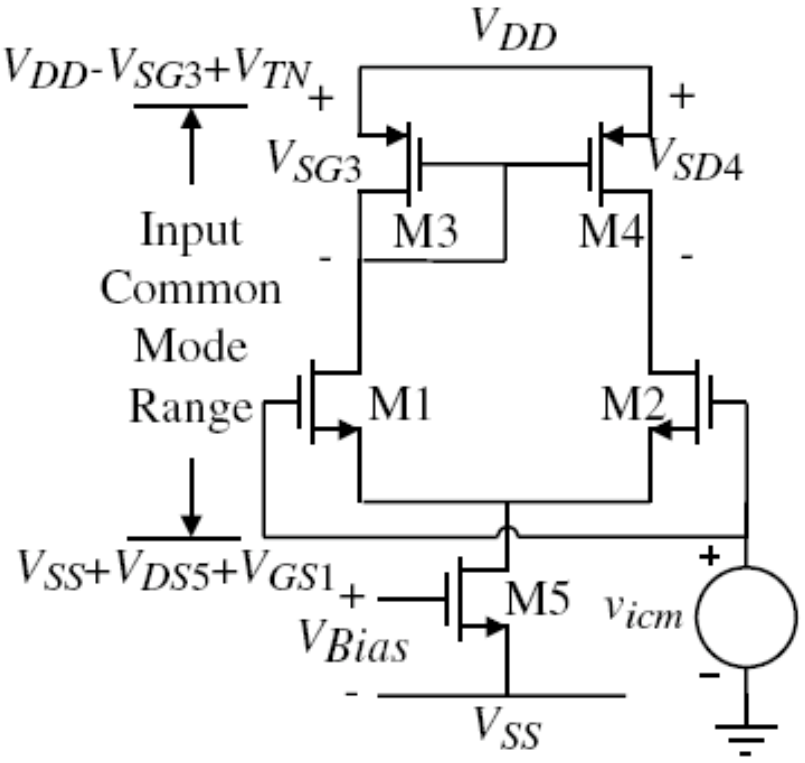
• The most important contributors to this type of coupling are displacement currents in the capacitances Cgs1 and Cgd1. These currents flow into the summing node and the resulting charge is accumulated on the integration capacitor, Ci.



• Interconnect crossovers may also couple supply variations into the summing node.

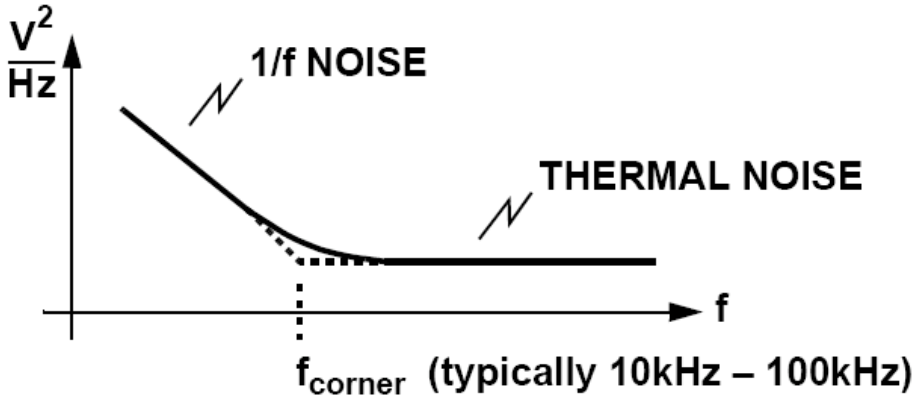
• Fully differential circuits are an obvious means of avoiding the most severe supply capacitance problems.

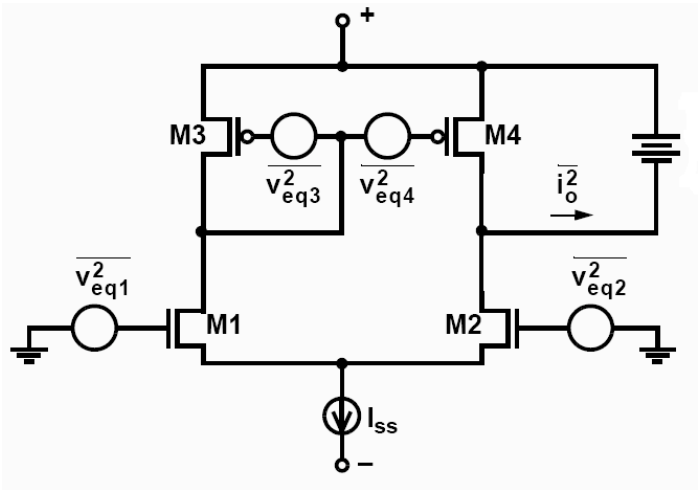
Input Common Mode Range



Differential amplifier with a current mirror load.

Noise in CMOS Opamps

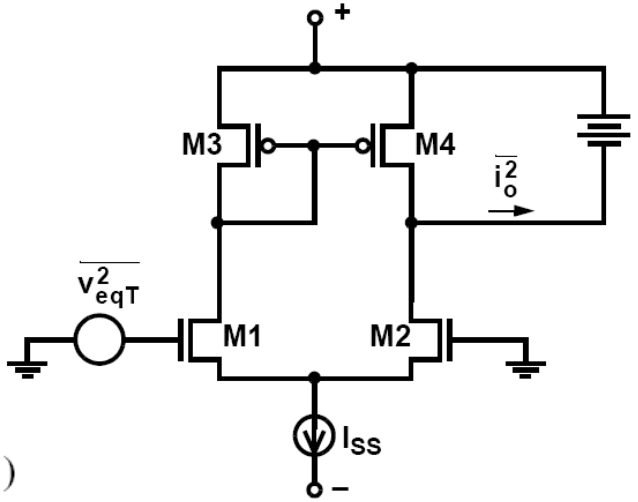




The gain of the input stage in a MOS op amp is usually large enough so that the input-referred noise of the overall amplifier is dominated by the noise contributions from the input-stage transistors.

$$\overline{i_O^2} = g_{m1-2}^2\left(\overline{v_{eq1}^2} + \overline{v_{eq2}^2}\right) + g_{m3-4}^2\left(\overline{v_{eq3}^2} + \overline{v_{eq4}^2}\right)$$

$$\overline{i_O^2} = \overline{g_{m1-2}^2}\,\overline{v_{IT}^2}$$



$$\overline{v_{eqT}^2} = \overline{v_{eq1}^2} + \overline{v_{eq2}^2} + \left(\frac{g_{m3}}{g_{m1}}\right)^2\left(\overline{v_{eq3}^2} + \overline{v_{eq4}^2}\right)$$

Noise in CMOS Op Amps (cont'd)

1/f NOISE

For an MOS transistor the input-referred 1/f noise can be modeled as:

$$\frac{\overline{v_{1/f}^2}}{\Delta f} = \frac{K_f}{fWLC_{ox}}$$

where Kf is the FLICKER NOISE COEFFICIENT

Using this model for each transistor in the input stage, the input-referred 1/f noise for the entire stage is

$$\frac{\overline{v_{1/fT}^2}}{\Delta f} = \frac{2K_{fN}}{fW_1L_1C_{ox}} + \left(\frac{g_{m3}}{g_{m1}}\right)^2\left(\frac{2K_{fP}}{fW_3L_3C_{ox}}\right)$$

Assuming that L2 = L1, W2 = W1, L4 = L3 and W4 = W3

$$\frac{\overline{v_{1/fT}^2}}{\Delta f} = \frac{2K_{fN}}{fW_1L_1C_{ox}} + \frac{\mu_P(W_3/L_3)}{\mu_N(W_1/L_1)}\left(\frac{2K_{fP}}{fW_3L_3C_{ox}}\right)$$

$$= \frac{2K_{fN}}{fW_1L_1C_{ox}}\left[1 + \frac{K_{fP}\mu_P L_1^2}{K_{fN}\mu_N L_3^2}\right]$$

Noise in CMOS Op Amps (cont'd)

Thermal NOISE

The input-referred thermal noise for an NMOS transistor is:

$$\frac{\overline{v_{eq}^2}}{\Delta f} = 4kT\left(\frac{2}{3g_m}\right)$$

$$\frac{\overline{v_{eqT}^2}}{\Delta f} = 4kT\left(\frac{4}{3g_{m1}}\right) + \left(\frac{g_{m3}}{g_{m1}}\right)^2\left[4kT\left(\frac{4}{3g_{m3}}\right)\right]$$

$$= 4kT\left(\frac{4}{3g_{m1}}\right)\left[1 + \frac{g_{m3}}{g_{m1}}\right]$$

$$= 4kT\left(\frac{4}{3g_{m1}}\right)\left[1 + \sqrt{\frac{\mu_P(W_3/L_3)}{\mu_N(W_1/L_1)}}\right]$$

$$= 4kT\left(\frac{4}{3\sqrt{2\mu_N C_{ox}(W_1/L_1)I_{d1}}}\right)\left[1 + \sqrt{\frac{\mu_P(W_3/L_3)}{\mu_N(W_1/L_1)}}\right]$$