REPORT

PROJECT # 2

Design of a

Switched Capacitor Integrator

Course No. :- 0301-610-01

Name: Analog Electronic Design

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<u>SWITCH CAPACITOR CIRCUITs (*An overview*) :</u>

A switched capacitor circuit is realized using op-amps, capacitors, switches and nonoverlapping clocks. The capacitor is taken as linear capacitance.

Op-amps:

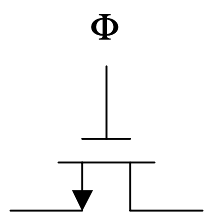
Here in the project we used the op-amp designed by us in the first project

Switches:

The requirement for switches used in the circuit is that they have a very high off resistance and a relatively low on resistance and introduce no offset when turned on. MOSFET transistors used as switch satisfies these requirements.

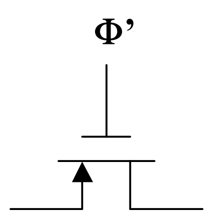
MOSFET circuits used as switches are as shown:

1)



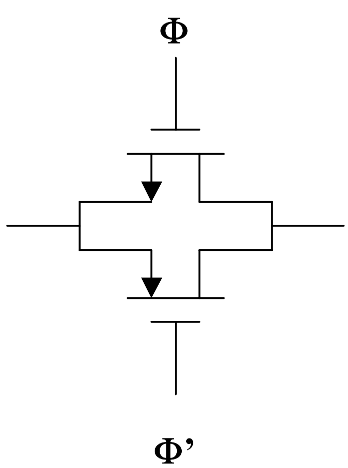
n-channel switch

2)



p-channel switch

3)



transmission gate

Φ' is complement of **Φ**

Φ is the clock signal which corresponds to one of the two logic levels corresponding to maximum and minimum power supply levels. We assume that when the input to the gate of the transistor is high the switch is on.

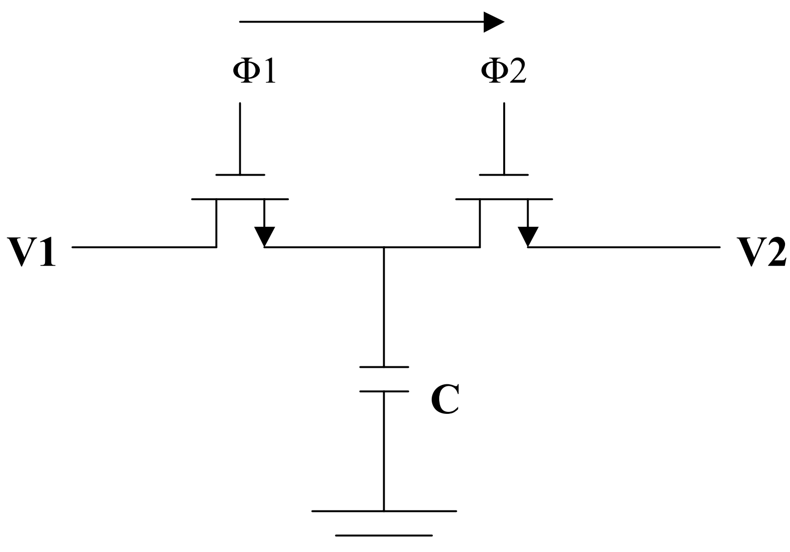
Nonoverlapping clocks:

At least one pair of non overlapping clock is required in switched capacitor circuits. These clock signals determine when charge transfer occur and they must be overlapping to ensure that the charge is not lost.

Nonoverlapping clocks refer to two logic signals running at the same frequency and arranged in such a way that at no time are both signals high.

BASIC OPERATION AND ANALYSIS

Resistor equivalence of a switched capacitor



Here V1 and V2 are two dc voltage sources. The charge on a capacitor Q is equal to C times the voltage V

$Q = C*V$

Now here $\Phi 1$ and $\Phi 2$ are a pair of nonoverlapping clocks. So C is charged to V1 and V2 during each clock period. Hence the change in the charge over one clock period that is transferred from node V1 to V2 is

$$Q = C * (V1 - V2)$$

Tis charge transferred every cycle. So we find an equivalent current due to this charge transfer. This current is

$$I = Q/T$$

T = clock period

Relating this to a equivalent resistor we get $I = (V1 – V2)/R$

Thus we get

$$\mathbf{R = T / C}$$
$$\mathbf{= 1 / f\,C}$$

Thus we can design a resistor using switched capacitor circuit.

But this circuit is sensitive to the parasitic capacitances of the capacitor C and the the transistor capacitances. So we have used another design in our project which is insensitive to the parasitic capacitances.

WORKING AND ANALYSIS OF THE CIRCUIT USED IN THE PROJECT

Design Considerations

Given that Gain = -100 (i.e. 100 for inverting configuration)

Now
Gain of an integrator = $1/RC_f$ --(1)
$1/RC_f = 100$

We assume C_f to be 10 pF (the value of load capacitance for the op-amp

Using this value of C_f we get R = 1 G

So we have to design the switch capacitor circuit in such a way and at such a sampling frequency that we get a resitance of 1 G from the circuit.

Uisng the formula

$f_s = 1/RC_1$ --(2)

we get

To get proper sampling og the signal as per the Nyquist Criteria The sampling frequency should be atleast twice the maximum frequency of the signal to be sampled.
So we take sampling frequency to 5 K.
For sampling frequency of 5 KHz

C_1 = 0.2 pF
= 200 f F

This value of C_1 could be consistent with the design.

It is important that we don't make C_1 less than around 100 f F because then the parasitic capacitances of the circuit become prominent and affect the performance of the circuit.

From the equations 1 and 2 we also get

Gain = $f_s C_1/ C_f$

Therefore for f_s = 5K we get

$C_1/ C_f = 0.02$

Thus we can change the values of the capacitors to improve the performance of the circuit keeping the ratio to be constant.

For sampling frequency of 10 KHz

$C_1 = 0.1$ pF
$= 100$ f F

Thus we can try out different combinations for sampling frequencies and the capacitors until we get the desired results.

The W/L ratio for all the CMOS transistors is taken as 1.

SIMULATION AND RESULTS

Here we used Cadence to simulate our design. Initially we simulated the circuit using sampling frequency to be 10 KHz and taking $C_f = 5$ pF and $C_1 = 0.5$ pF

To generate nonoverlapping clocks we provided a delay of 0.1 µs between two clocks. Also the peak amplitudes of the clock signals where kept –5 V to 5 V to ensure that the transistor turn on and off properly.

But for this case we did not get the desired response and we obtained the output which had lots of spikes due to improper charging – discharging of the capacitor.
Also clock feed through started appearing at the output although it was negligible.

So then we reduced the sampling frequency to 5 KHz and the feedback capacitance was increased to 10pF which reduced the switch capacitor to 200 fF.

The advantage that we got from making this change was that as the value of capacitor was reduced so that it can charge fast as compared fast as compared to first case. This helped in eliminating the clock feed through and also the irregularities in the output of the integrator.

On increasing the frequency keeping all other parameters constant it was found out that clock feed through started appearing at sampling frequency of around 8-9 KHz.
Also from the graph we get Gain = 120.

Simulation Results:

1) Gain = 120
2) The output of the circuit is similar to what the integration of a triangular waveform should be which proves that our design is correct as per the given specifications.