4. Current and Voltage Sources

Analog Design for CMOS VLSI Systems

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Current mirrors

A current mirror gives a replica (attenuated or amplified, if necessary) of a bias or signal current.

The most used current mirrors are:

- simple current mirror
- Wilson current mirror
- improved Wilson current mirror
- cascode current mirror
- modified cascode current mirror
- high compliance current mirror
- regulated cascode current mirror

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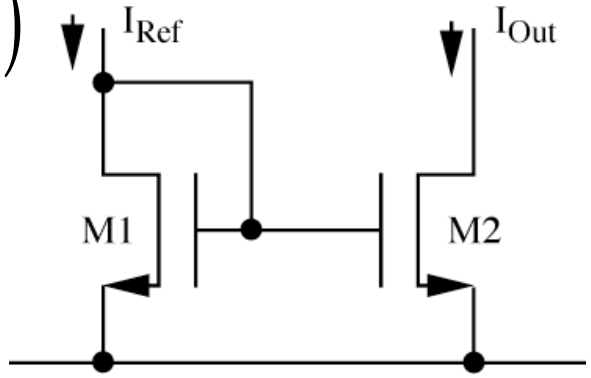
Simple current mirror

$$I_{Ref} = I_1 = \frac{\mu C_{ox}}{2}\left(\frac{W}{L}\right)_1 \left(V_{GS1} - V_{Th}\right)^2 \left(1 + \lambda V_{DS1}\right)$$

$$I_{Out} = I_2 = \frac{\mu C_{ox}}{2}\left(\frac{W}{L}\right)_2 \left(V_{GS1} - V_{Th}\right)^2 \left(1 + \lambda V_{DS2}\right)$$



$$V_{DS1} = V_{GS1} = V_{GS2}$$

to simplify the calculations let $\lambda V_{DS1} = 0$

$$I_{Out} = I_{Ref} \frac{\left(\frac{W}{L}\right)_2}{\left(\frac{W}{L}\right)_1}\left(1 + \lambda V_{DS2}\right)$$

$$r_{out} = r_{ds2} = \frac{1}{\lambda I_{Out}}$$

$$\frac{I_{Out}}{I_{Ref}} = \frac{\left(\mu C_{ox}\right)_2 \left(\frac{W}{L}\right)_2 \left(V_{GS} - V_{Th2}\right)^2 \left(1 + \lambda V_{DS2}\right)}{\left(\mu C_{ox}\right)_1 \left(\frac{W}{L}\right)_1 \left(V_{GS} - V_{Th1}\right)^2 \left(1 + \lambda V_{DS1}\right)}$$

Factors affecting the mirror accuracy:

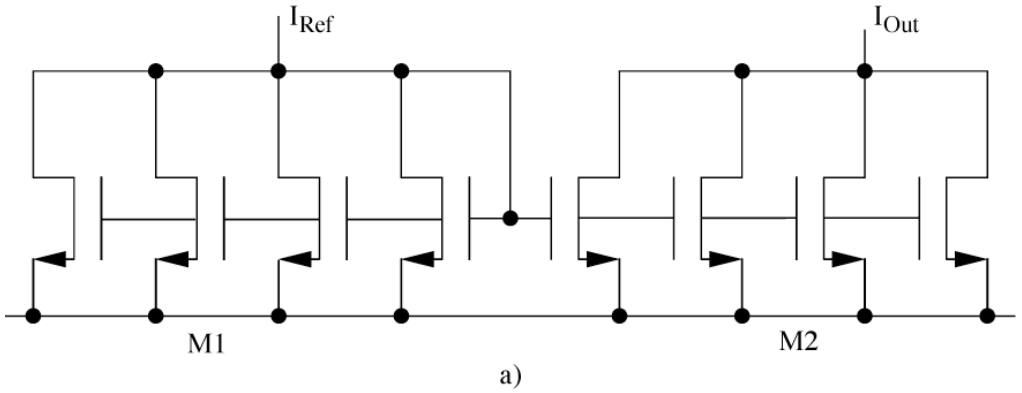
- channel length modulation $\frac{\left(1 + \lambda V_{DS2}\right)}{\left(1 + \lambda V_{DS1}\right)}$
- offset between the threshold voltages $\frac{\left(V_{GS} - V_{Th2}\right)^2}{\left(V_{GS} - V_{Th1}\right)^2}$
- imperfect geometrical matching $\left(\frac{W}{L}\right)_2 \Big/ \left(\frac{W}{L}\right)_1$
- technological parameter mismatch $\frac{\left(\mu C_{ox}\right)_2}{\left(\mu C_{ox}\right)_1}$
- parasitic resistances

Accuracy:

$$\left(\frac{\delta I_{Out}}{I_{Out}}\right)^2 = \left(\frac{\delta W}{W}\right)^2 + \left(\frac{\delta L}{L}\right)^2 + \left(\frac{\delta C_{ox}}{C_{ox}}\right)^2 + \left(\frac{\delta \mu}{\mu}\right)^2 + 2\left(\frac{\delta V_{Th}}{V_{GS} - V_{Th}}\right)^2 + 2\left(\frac{\delta V_{GS}}{V_{GS} - V_{Th}}\right)^2$$

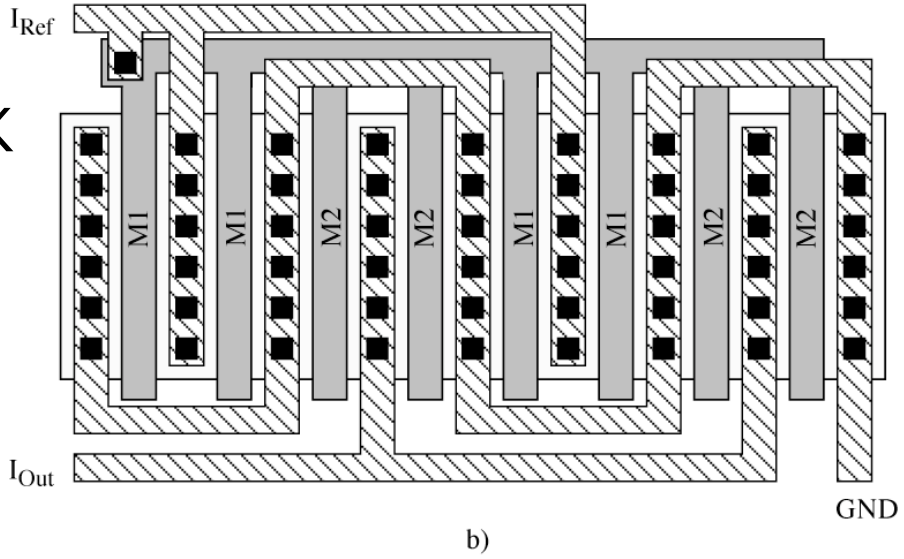
- The threshold mismatch is inversely proportional to the overdrive
- The threshold of the MOS transistors placed in close proximity are matches within few mV. By contrast, for MOS transistors which are hundred of microns apart have threshold voltages that can differ by few tens of mV.
- The last term refers to a mismatch in V_{GS}. It can derive from resistive voltage drop, due to a parasitic resistance in series with the source.
- The metal resistance is in the order of 20-50 mΩ/□, with 10 squares it result 0.2-0.5 Ω. If the current is 10 mA results an equivalent offset of 2-5 mV.
- $(\delta\mu/\mu)$ and $(\delta C_{ox}/C_{ox})$ are minimized with closed and centroid common structures.
- $(\delta W/W)$ and $(\delta L/L)$ depends on the lithographic process.

- For large *W* a good strategy is splitting the transistors into *n* equal parts connected in parallel.

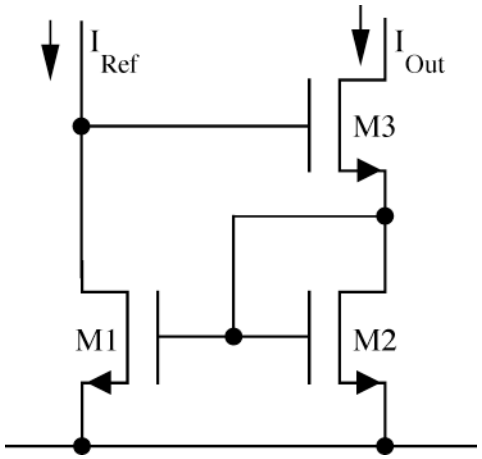


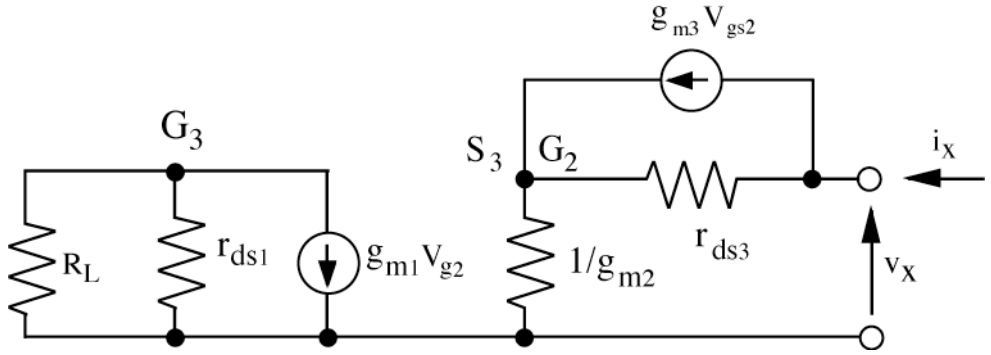
$$\left(\frac{\delta I_{Out}}{I_{Out}}\right)^2 = \frac{1}{n}\left[\left(\frac{\delta W}{W}\right)^2 + \left(\frac{\delta L}{L}\right)^2\right] + K$$

- Inter-digitized structures reduce parasitic capacitances.



Wilson current mirror





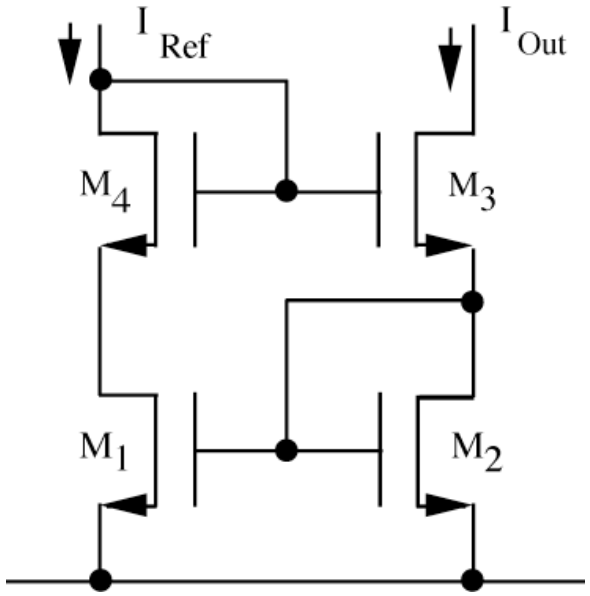
Increases the output resistance.

$v_{g2} = v_{s3} = i_x / g_{m2}$ $\quad v_{g3} = -g_{m1} v_{g2} r_T$ $\quad r_T = r_{ds1} // R_L$

$$v_x = \frac{i_x}{g_{m2}} + \left(i_x - g_{m3} v_{gs3}\right) r_{ds3} \qquad r_{out} = \frac{1}{g_{m2}} + \left[1 + \frac{g_{m3}}{g_{m2}}\left(1 + g_{m1} r_T\right)\right] r_{ds3}$$

- R_L must be large
- there is a systematic error because $V_{DS1} = V_{GS3} + V_{DS2}$

Improved Wilson current mirror



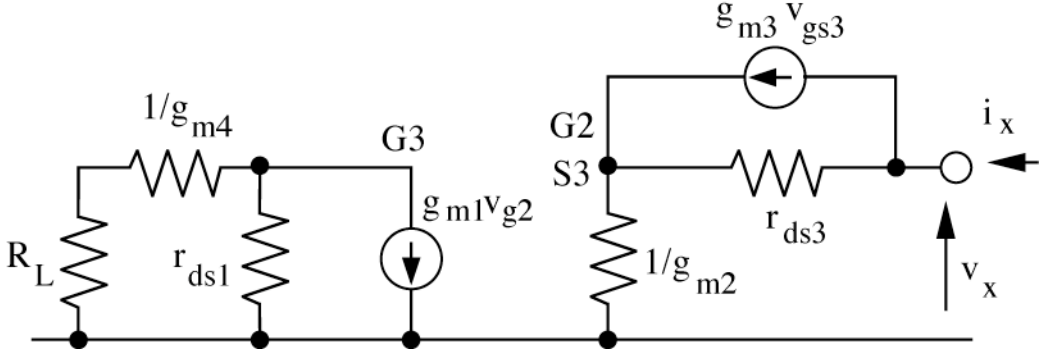
$$V_{DS1} = V_{GS3} + V_{DS2} - V_{GS4}$$

$$V_{DS1} = V_{DS2} \quad \text{if} \quad V_{GS3} = V_{GS4}$$

small signal analysis

$$v_{g3} = -g_{m1} v_{g2} r_T' \frac{R_L g_{m4}}{1 + R_L g_{m4}}$$

$$r_T' = r_{ds1} // \left(R_L + 1/g_{m4} \right)$$

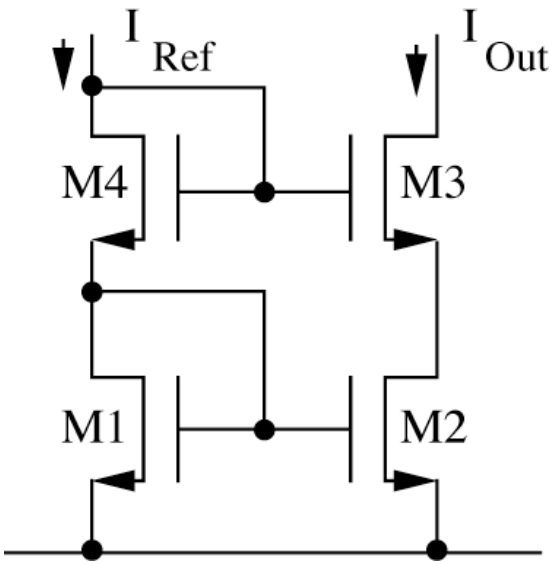


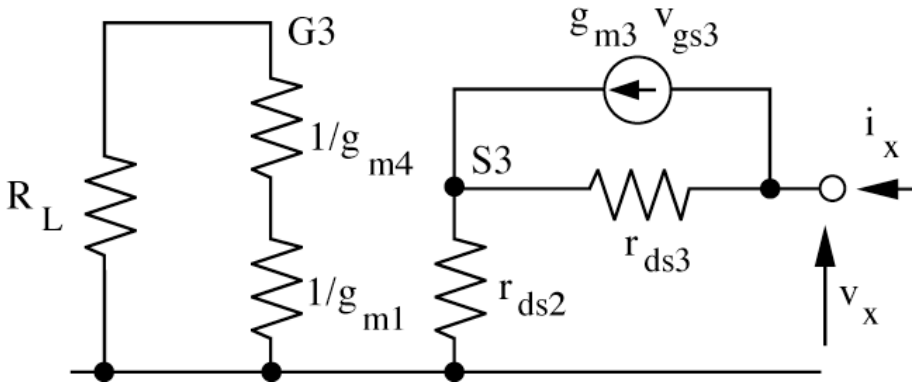
$$r_{out} \approx r_{ds3} \frac{g_{m3}}{g_{m2}} g_{m1} v_{g2} r_T' \frac{R_L g_{m4}}{1 + R_L g_{m4}}$$

The output swing in the Wilson and improved Wilson schemes is limited to

$$V_{out,min} = V_{GS1} + V_{sat,3} = V_{Th,n} + V_{sat,1} + V_{sat,3}$$

Cascode current mirror





It increases the output resistance without feedback loop. It has the same resistance of the cascode load.

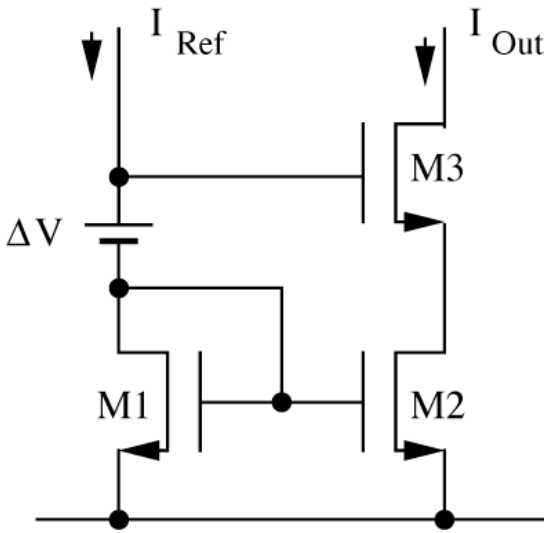
$v_x = r_{ds2} i_x + r_{ds3} (1 + g_{m3} r_{ds2}) i_x \qquad r_{out} \approx r_{ds3} g_{m3} r_{ds2}$

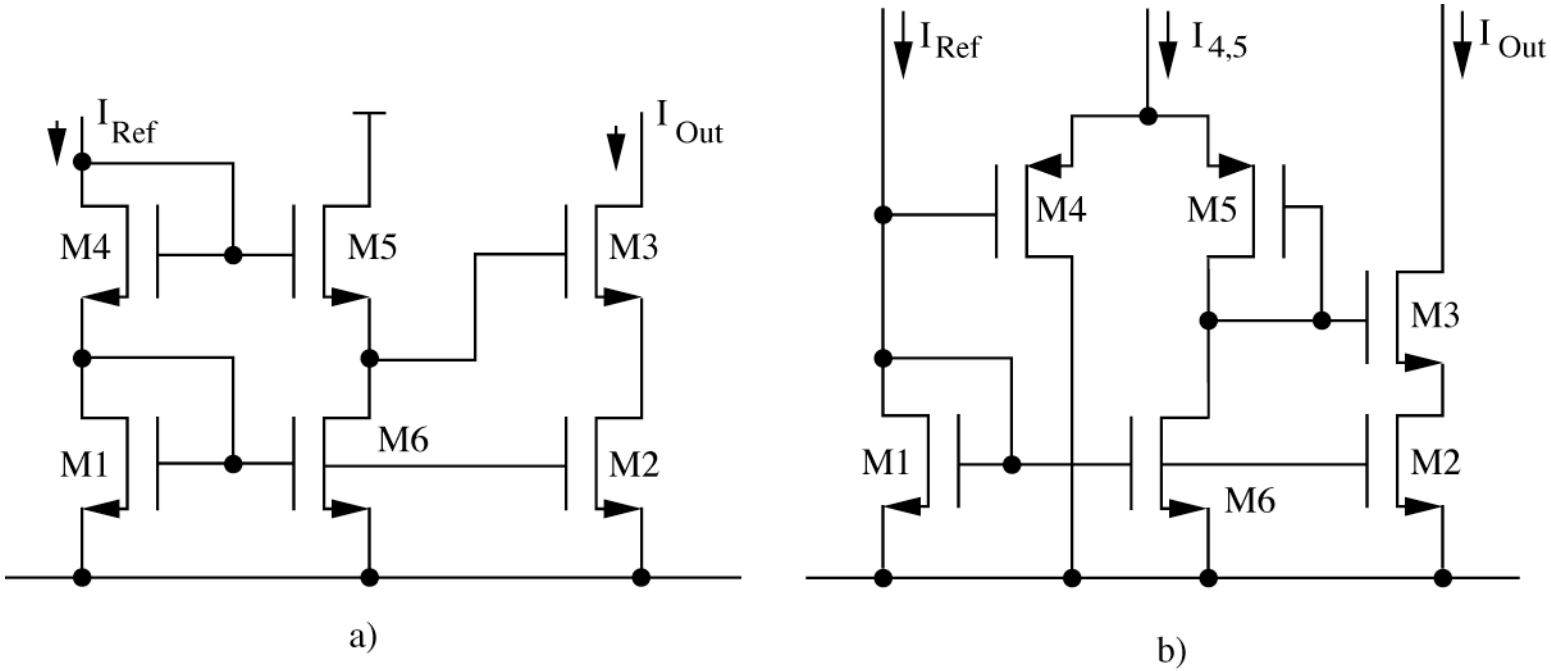
The output swing is limited to

$V_{G3} = V_{GS1} + V_{GS4} - V_{GS3} \quad V_{out,min} = V_{S3} + V_{sat,3} \approx V_{Th} + 2V_{sat}$

Modified cascode current mirror

- The function of the transistor M4 is to shift the voltage V_{DS1} of the amount enough to bias the gate of M3 without bringing M2 out of saturation.
- The use of M4 (matched with M3) allows to get $V_{DS1} = V_{DS2}$ (this is paid with the output swing limitation).
- The output swing is improved by the use of a level shift $V_{sat} < \Delta V < V_{Th}$.

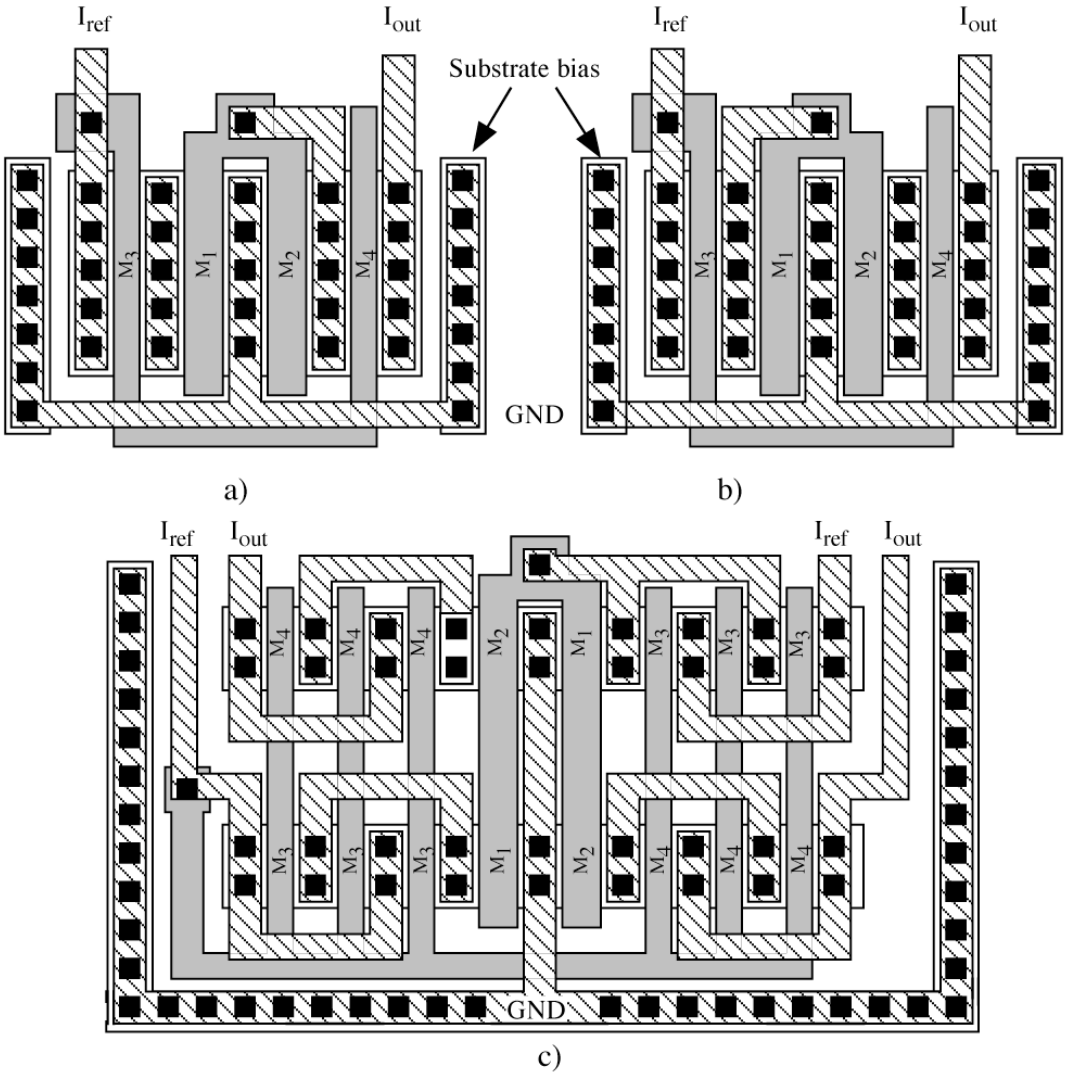




The geometrical dimensions of M1, M6, M4, M5 determine, with $V_{ov,4}$, ΔV.

$$\Delta V = V_{GS4} - V_{GS5} = \sqrt{\frac{2I_4 L_4}{\mu C_{ox} W_4}} - \sqrt{\frac{2I_5 L_5}{\mu C_{ox} W_5}}$$

Layout



Separate biasing in the cascode

All transistors operate in saturation

$I = I_1 = I_2 = I_3 = I_4$ (current scaling is possible)

$\beta_1 = \beta_2 = \beta_3 = \beta$

$V_{ov1} = V_{ov2} = V_{ov3} = V_{ov}$

$I_4 = \beta_4 (V_{ov4})^2$; $I_2 = \beta (V_{ov})^2$; $I_3 = \beta (V_{ov})^2$

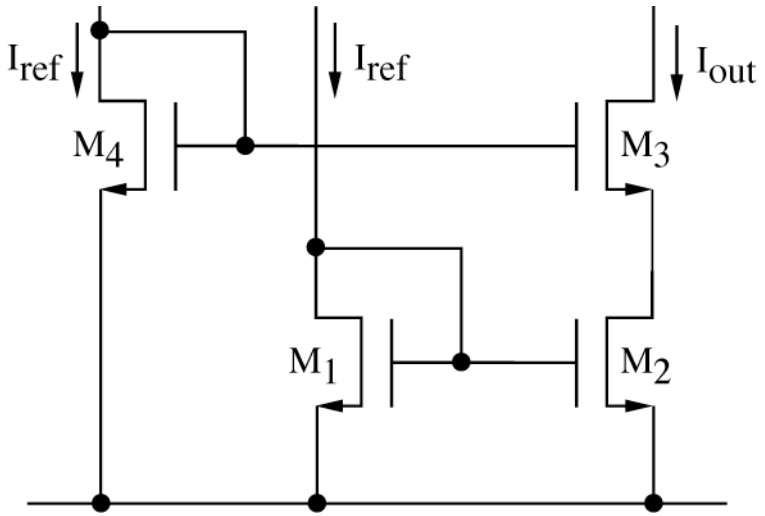
$V_{DS2} = V_{ov}$

$V_{GS3} = V_{TH} + V_{ov}$

$V_{GS4} = V_{TH} + 2\,V_{ov}$ $\quad V_{ov4} = 2\,V_{ov}$

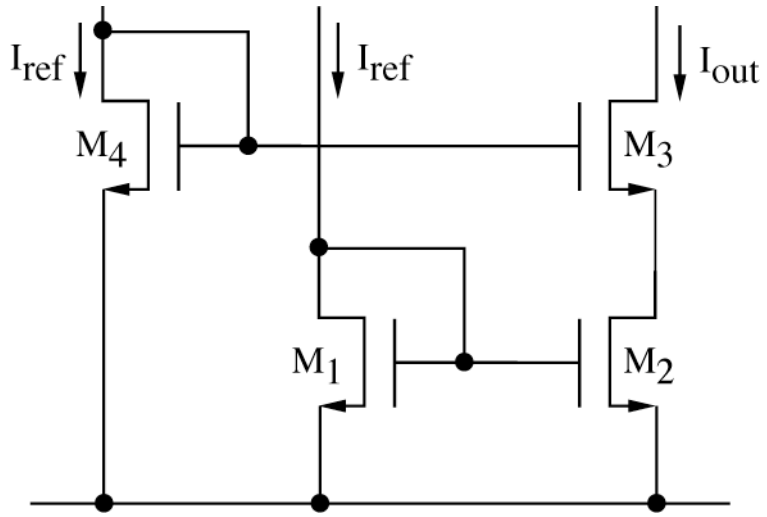
therefore $\beta = 4\,\beta_4$

$$\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2 = \left(\frac{W}{L}\right)_3 = 4\left(\frac{W}{L}\right)_4$$

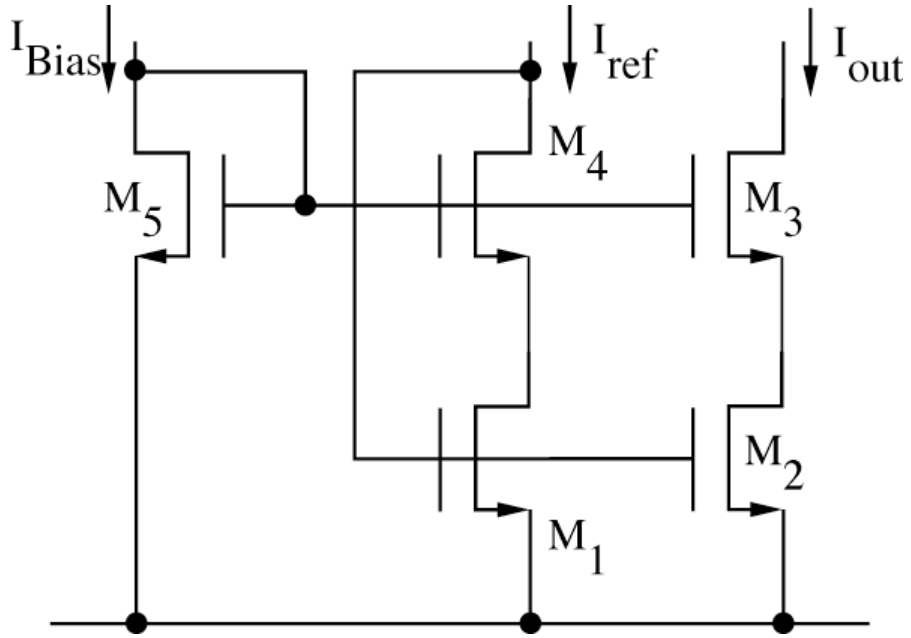


Current gain:

- systematic error due to $V_{DS1} \neq V_{DS2}$
- systematic error due to body effect on M3
- output swing $V_{out,\,min} = 2\,V_{DSsat}$
- output impedance: $r_{out} = r_{out4}\,g_{m2}\,r_{out2}$



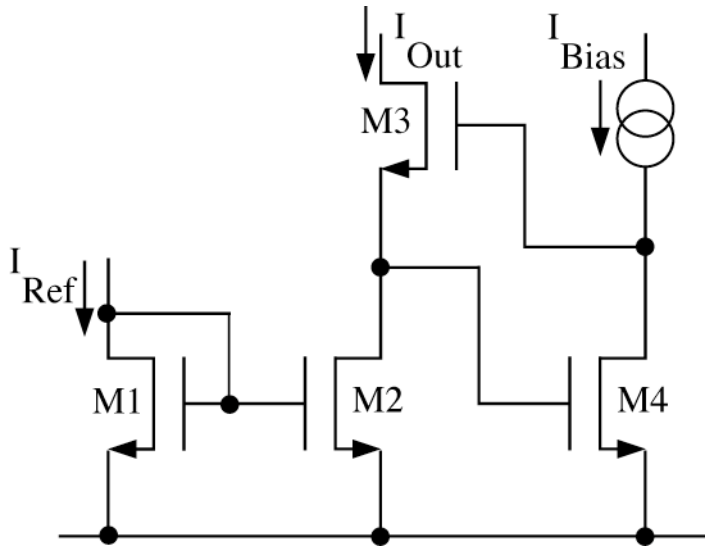
High-compliance current mirror



M1 = M2; M3 = M4 therefore $I_{out} = I_{ref}$

To properly work, we must impose $V_{DSsat\mathrm{M4}} < V_{Th1}$

Regulated-cascode current mirror



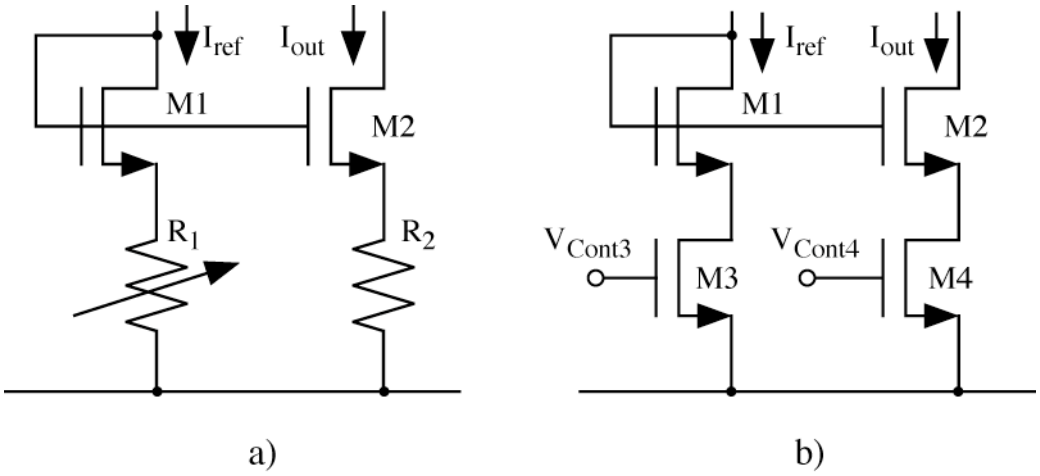
- Output impedance:

$$R_{out} = (g_{m3}r_{out3})r_{out2}(g_{m4}r_{out4})$$

- Output swing:

$$V_{outmin} = V_{GS4} + V_{DSsat3} \approx V_{Th} + 2\,V_{sat}$$

Adjustable current mirror

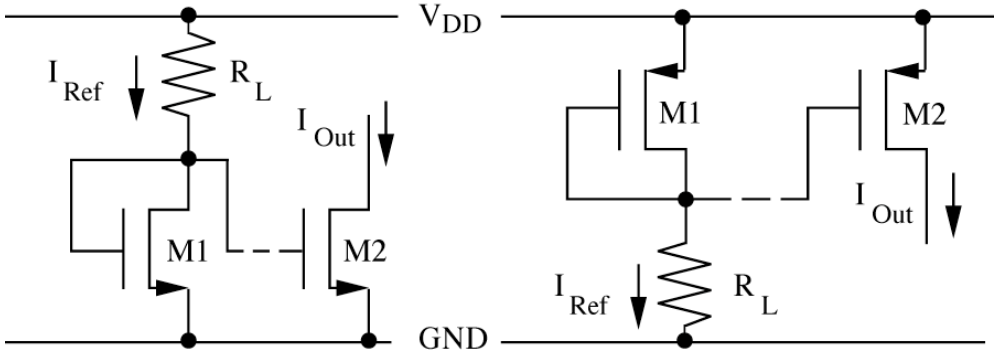


- Degeneration resistances achieved with MOS transistors in the triode region.
- The voltages at the gates of M3 and M4 control the mirror factor.

Current references

Most of the analog blocks require a reference current.
These simple current references depend on supply.

$$I_{Ref} = \frac{V_{DD} - V_{GS1}}{R_L}$$



The current accuracy is:

$$\left(\frac{\delta I_{Ref}}{I_{Ref}}\right)^2 = \left(\frac{\delta\left(V_{DD} - V_{GS1}\right)}{V_{DD} - V_{GS1}}\right)^2 + \left(\frac{\delta R_L}{R_L}\right)^2$$

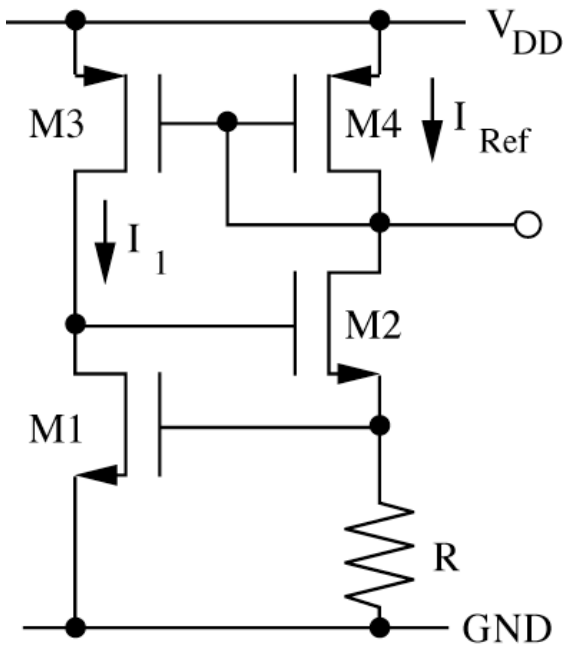
The global inaccuracy is around ±32%.

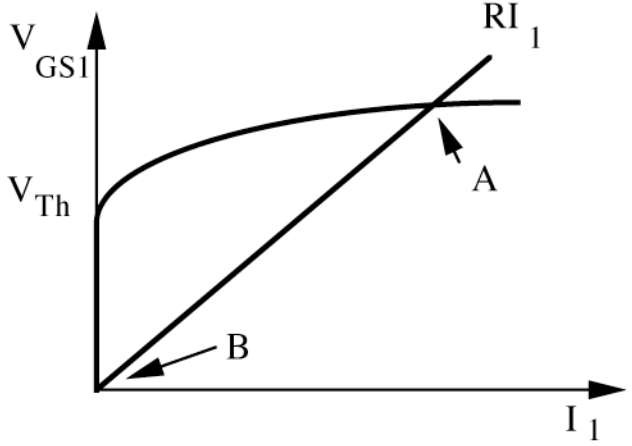
The dependence on supply is critical when supply lines are affected by spur signals.

Self biased (or bootstrapped) current reference

$$\left(\frac{W}{L}\right)_4 = \left(\frac{W}{L}\right)_3$$

$$\begin{cases} V_{GS1} = RI_1 \\ V_{GS1} = V_{Th} + \sqrt{\dfrac{I_1}{\frac{\mu C_{ox}}{2}\left(\frac{W}{L}\right)_1}} \end{cases} \quad \text{for } V_{GS1} > V_{Th}$$

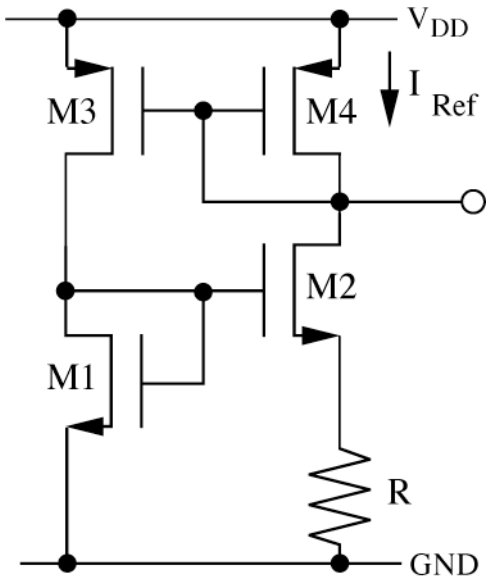




Two operating points: It is necessary to use a start-up circuit.

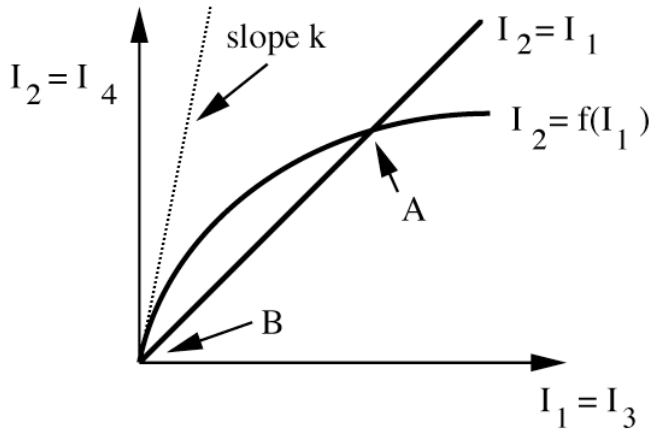
Self biased micro-current generator

$$\left(\frac{W}{L}\right)_4 = \left(\frac{W}{L}\right)_3 \qquad \left(\frac{W}{L}\right)_2 = k\left(\frac{W}{L}\right)_1 \qquad k > 1$$



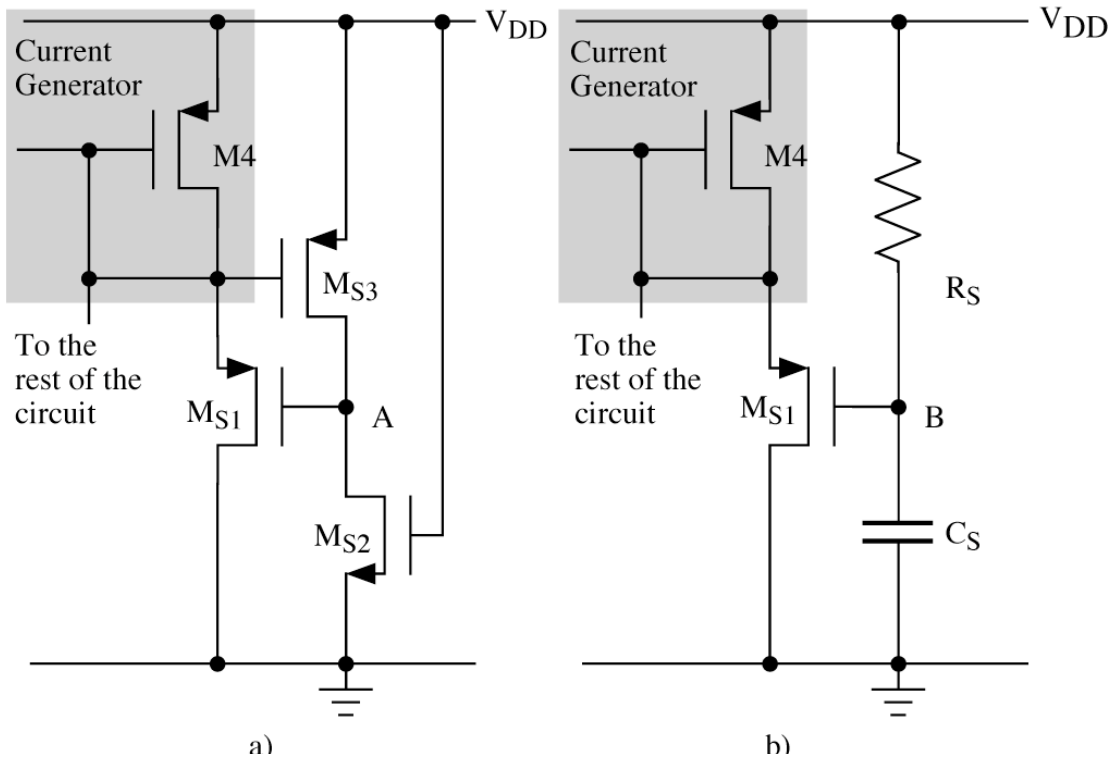
- Assume M3 = M4 ideal mirror $I_3 = I_4$
- Assume $V_{Th1} = V_{Th2}$

$$\sqrt{\frac{I_1}{\frac{\mu C_{ox}}{2}\left(\frac{W}{L}\right)_1}} = \sqrt{\frac{I_2}{\frac{\mu C_{ox}}{2}\left(\frac{W}{L}\right)_2}} + RI_2$$



For $k = 10$, $V_R \approx 60$ mV,
so $R = 60$ kΩ for $I = 1$ μA.

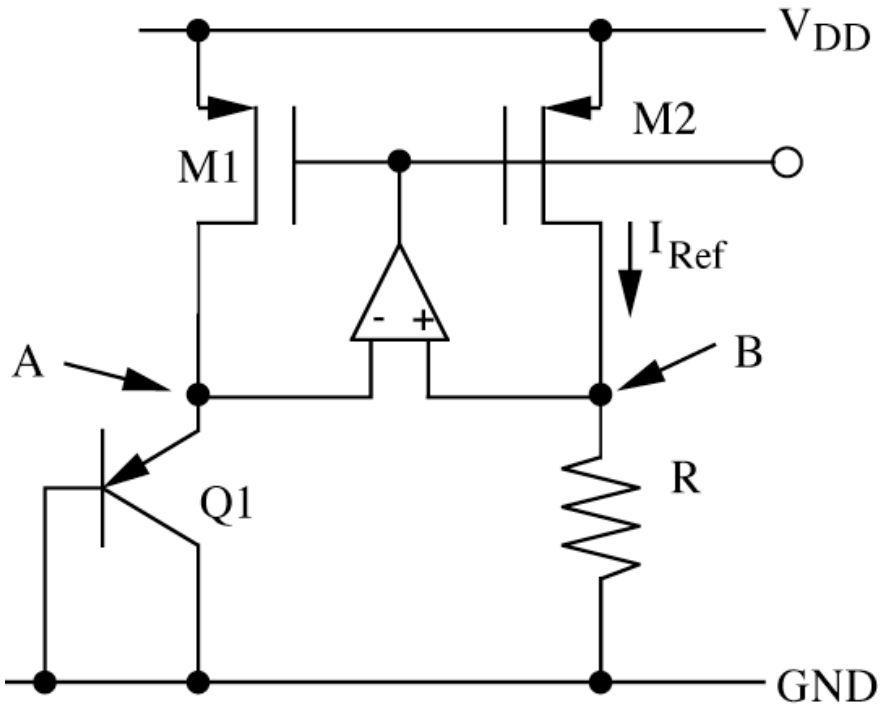
Start-up circuit



static dynamic

Monitor if the current is zero and inject a current that starts the circuit.

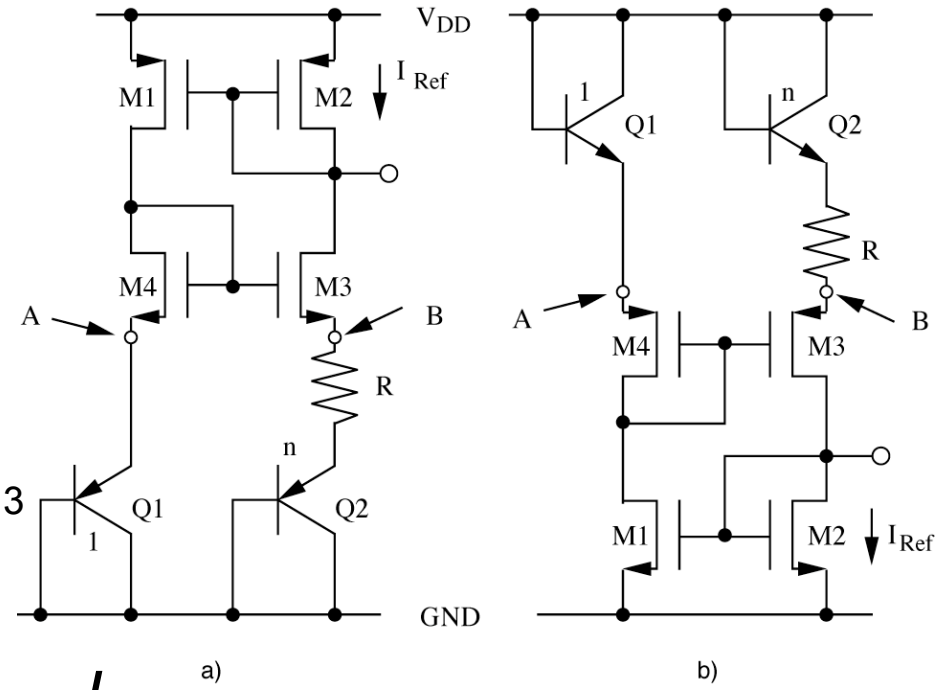
V_{BE}-based current generator



The voltage across the resistance and the diode voltage are made equal by the feedback loop action.

V_T-based current generator

For a p-well a vertical npn transistor with the collector tied to V_{DD} is available (the complementary for n-well).



$$\left(\frac{W}{L}\right)_2 = \left(\frac{W}{L}\right)_1 \quad \left(\frac{W}{L}\right)_4 = \left(\frac{W}{L}\right)_3$$

$$I_1 = I_2 \qquad V_A = V_B$$

$$V_{BE1} = V_T \ln\frac{I_1}{AI_{SS}} \qquad V_{BE2} = V_T \ln\frac{I_1}{nAI_{SS}}$$

$$I_1 = \frac{V_T}{R}\ln n$$

$$RI_1 = V_{BE1} - V_{BE2} = V_T \ln\left(\frac{I_1}{AI_{SS}}\frac{nAI_{SS}}{I_1}\right)$$

Both V_T and R have positive temperature coefficient.

Voltage references

- V_{BE} multiplier
- V_T multiplier
- Threshold voltage difference
- Band-gap

V_{BE} multiplier

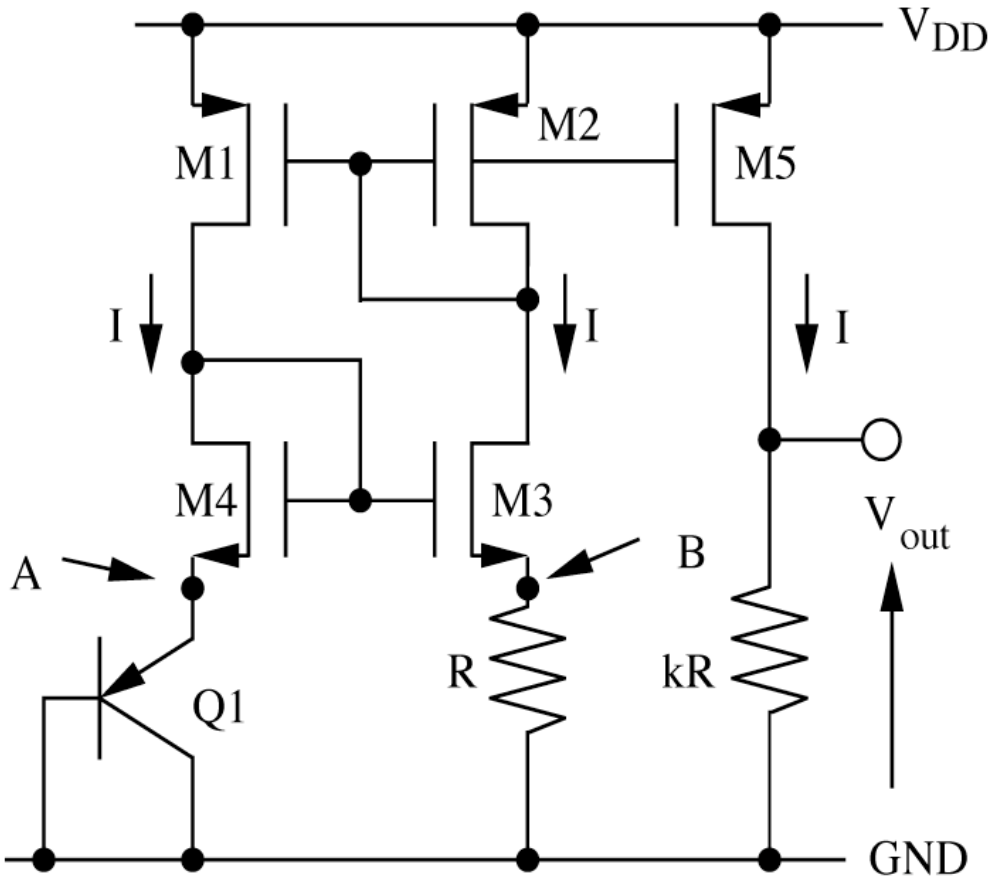
$$\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2 = \left(\frac{W}{L}\right)_5$$

$$\left(\frac{W}{L}\right)_3 = \left(\frac{W}{L}\right)_4$$

$$V_A = V_B$$

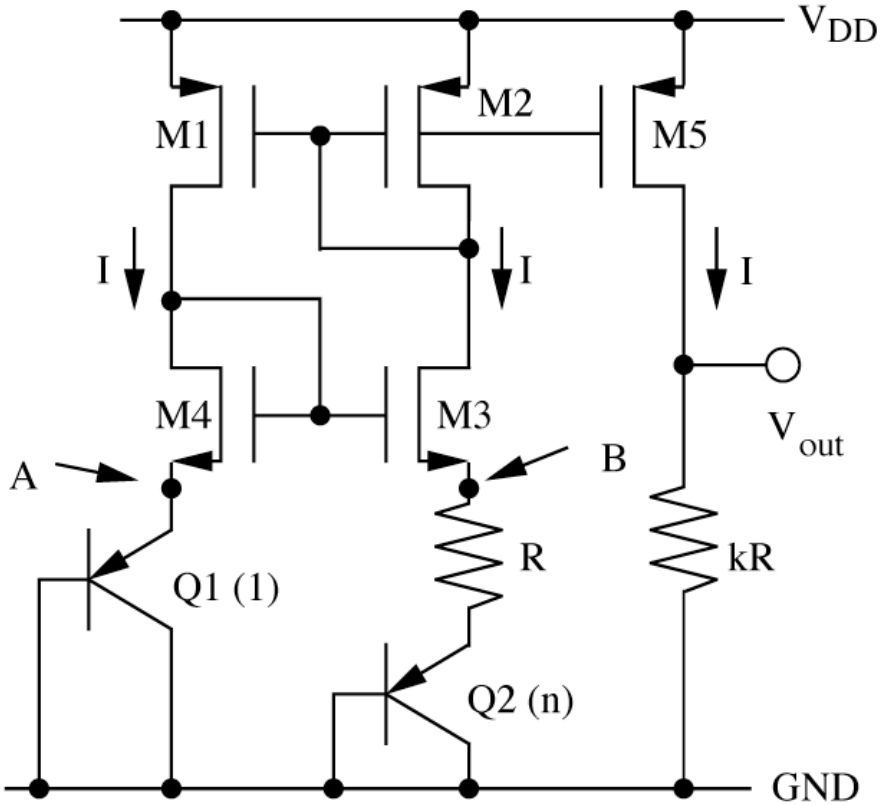
$$I = \frac{V_{BE}}{R}$$

$$V_{OUT} = k\,R\,I = k\,V_{BE}$$



V_{OUT} has a negative temperature coefficient

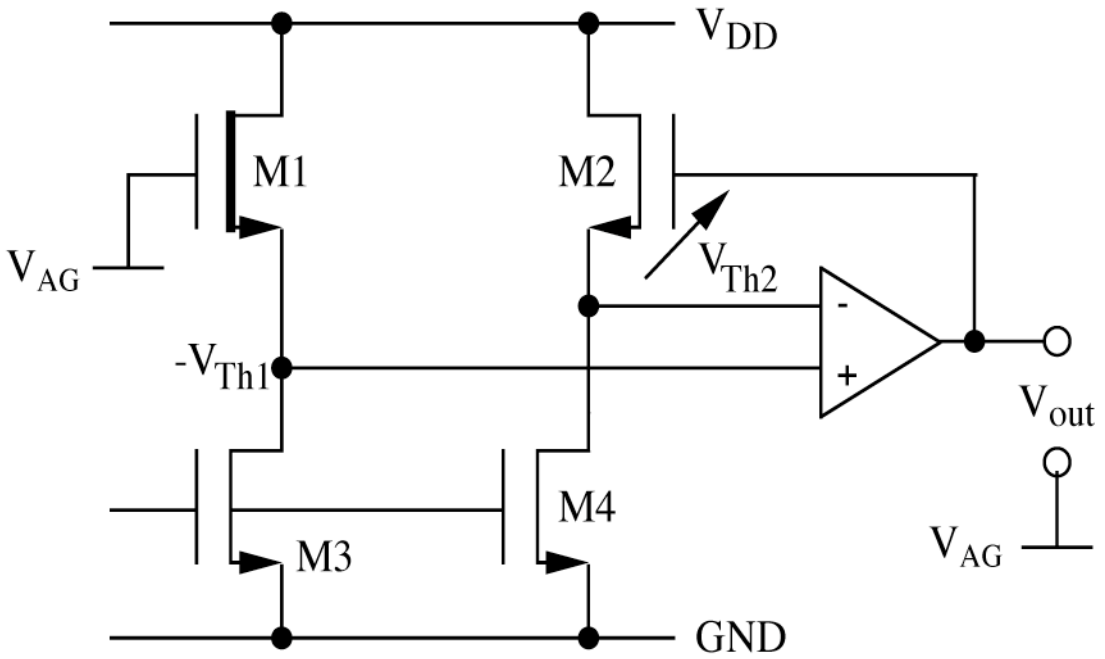
V_T multiplier



$$I = V_T / R \ln n$$

$$V_{OUT} = k V_T \ln n$$

Threshold voltage difference



M1 and M2 have different threshold (enhancement and depletion or enhancement and enhancement)

$$V_{OUT} = -V_{Th1} + V_{Th2}$$

Band-gap reference voltage

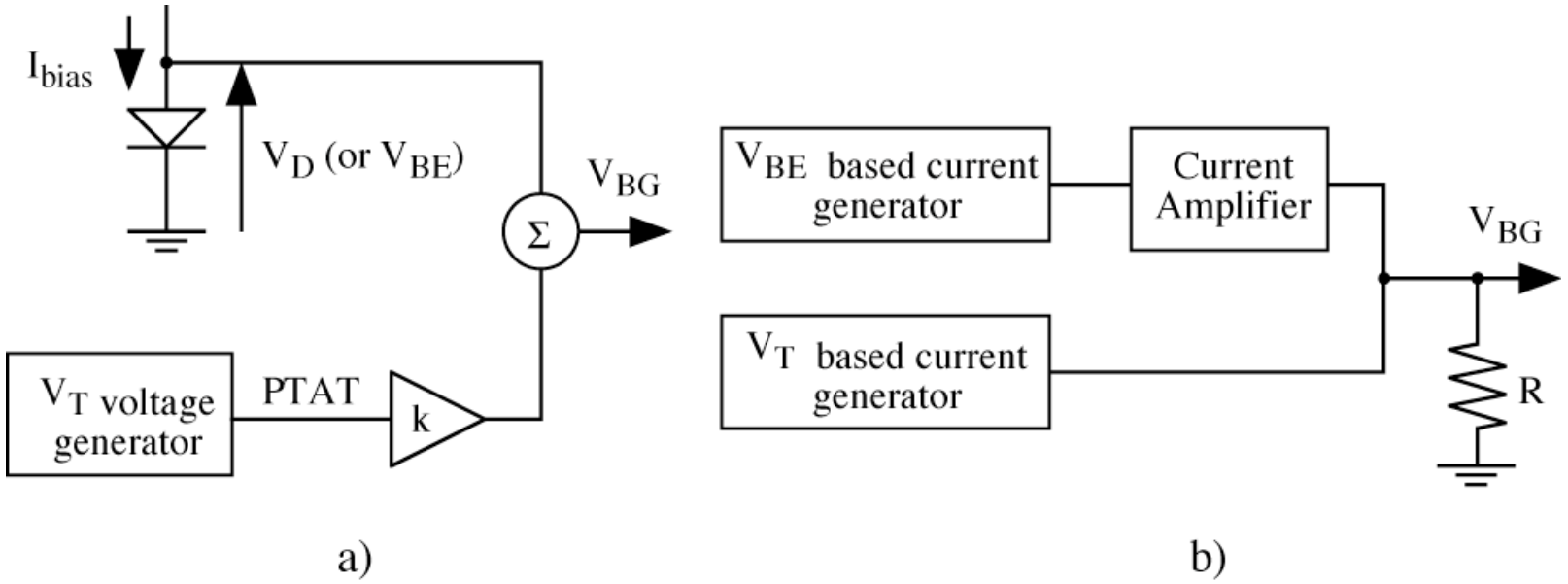
To obtain a reference voltage with zero temperature coefficient (in a defined temperature range) it is necessary to have:

$$V_{BG} = V_{BE} + m\, V_T$$

- V_{BE} has negative temperature coefficient (- 2.2 mV/°C at 300 K)
- V_T has positive temperature coefficient (+ 0.086 mV/°C at 300 K)

$$m \approx 25.6$$

Band-gap idea



a) implementation adding voltages

b) implementation adding currents and transforming current into voltage

Band-gap based on voltage processing

p-well process

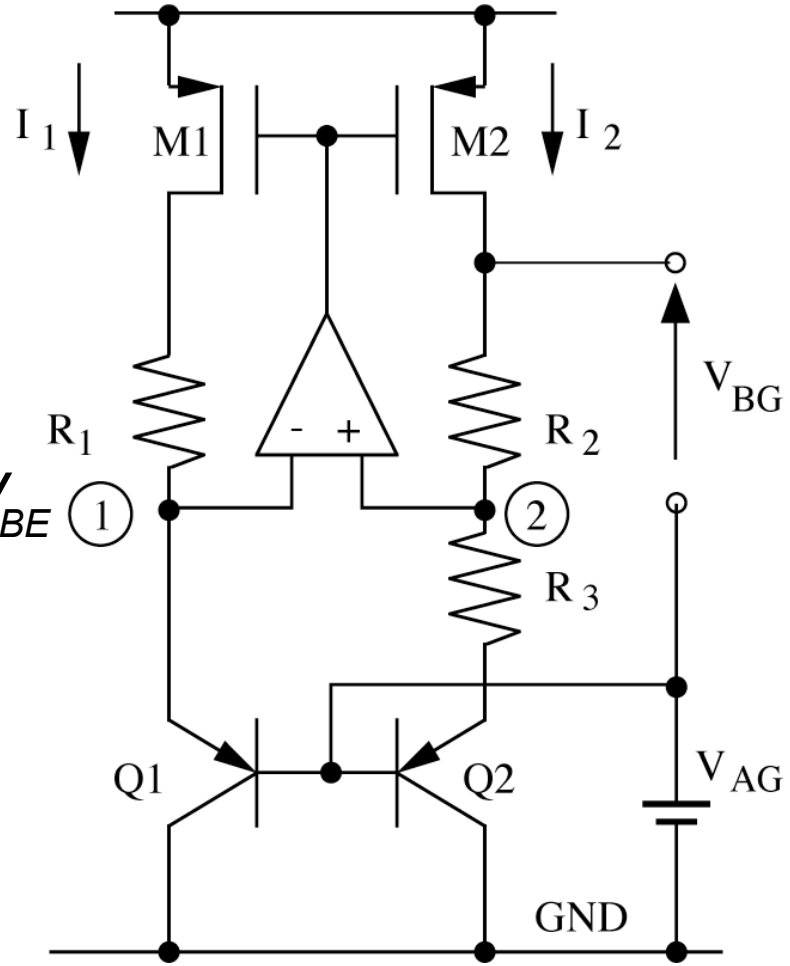
$$\Delta V_{BE} = V_T \ln\left(\frac{I_1}{A_1 I_{SS}} \frac{A_2 I_{SS}}{I_2}\right) = R_3 I_2$$

$$\frac{I_1}{I_2} = \left(\frac{W}{L}\right)_1 \Big/ \left(\frac{W}{L}\right)_2$$

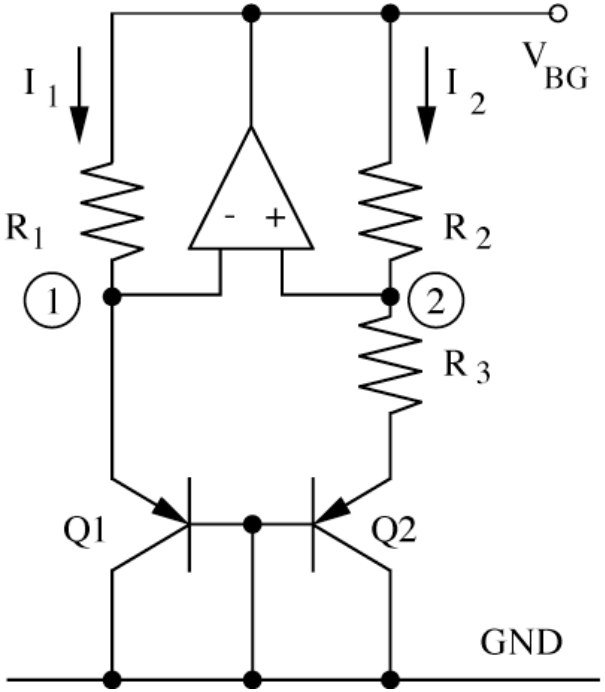
$$V_{BG} = V_2 - V_{AG} + R_2 I_2 = V_{BE1} + \frac{R_2}{R_3} \Delta V_{BE}$$

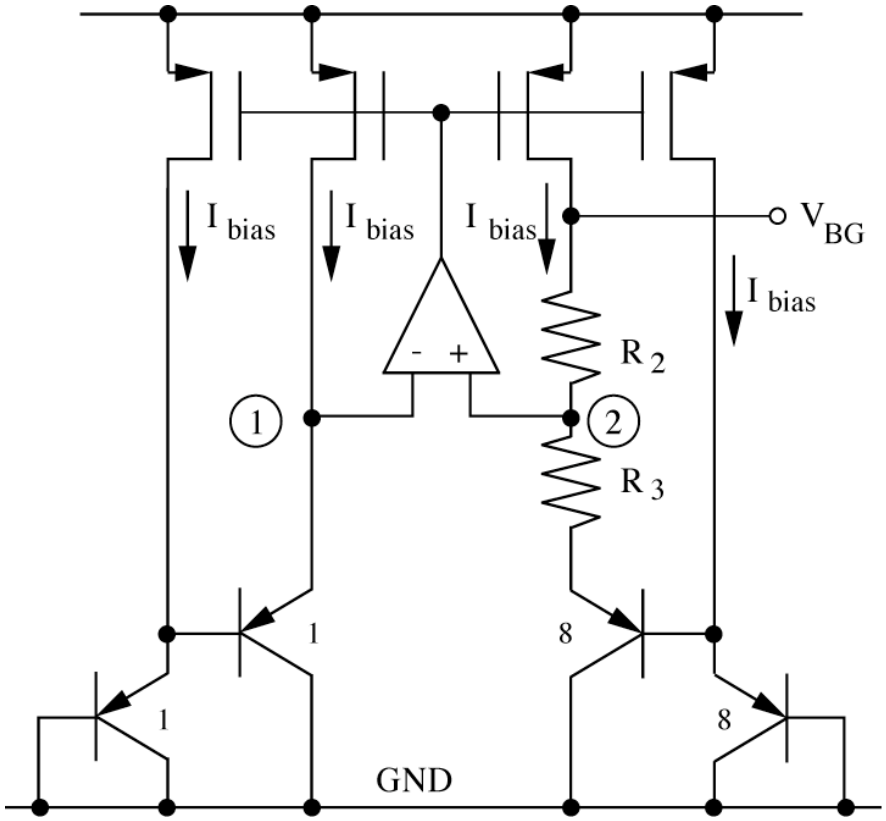
$$V_{BG} = V_{BE1} + V_T \frac{R_2}{R_3} \ln\left(\frac{(W/L)_1 A_2}{(W/L)_2 A_1}\right)$$

$$m = \frac{R_2}{R_3} \ln\left(\frac{(W/L)_1 A_2}{(W/L)_2 A_1}\right)$$



Other solutions



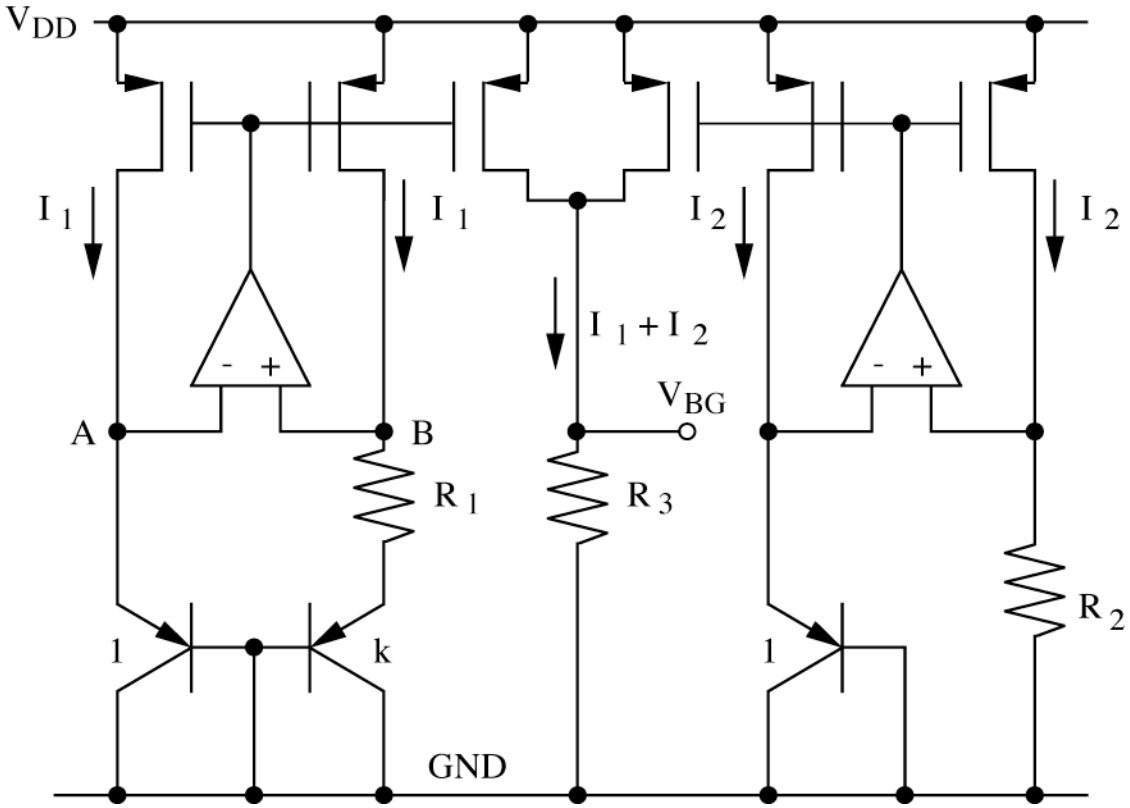


current provided by the op-amp

double band-gap

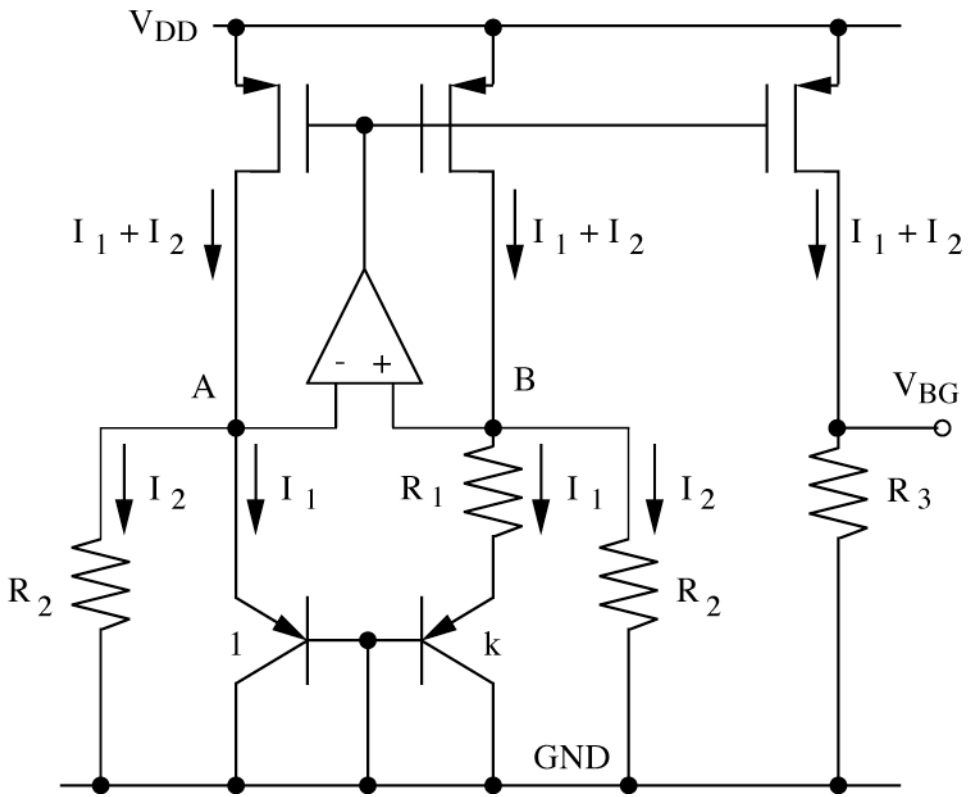
Band-gap based on current processing

p-well process



$$V_{BG} = V_{BE}\frac{R_3}{R_2} + V_T\frac{R_3}{R_1}\ln(k)$$

Combining the two op-amps

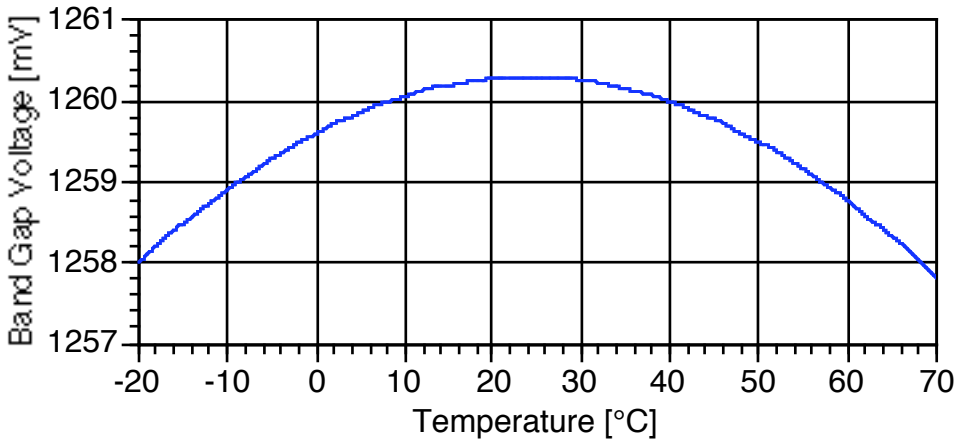


Curvature error

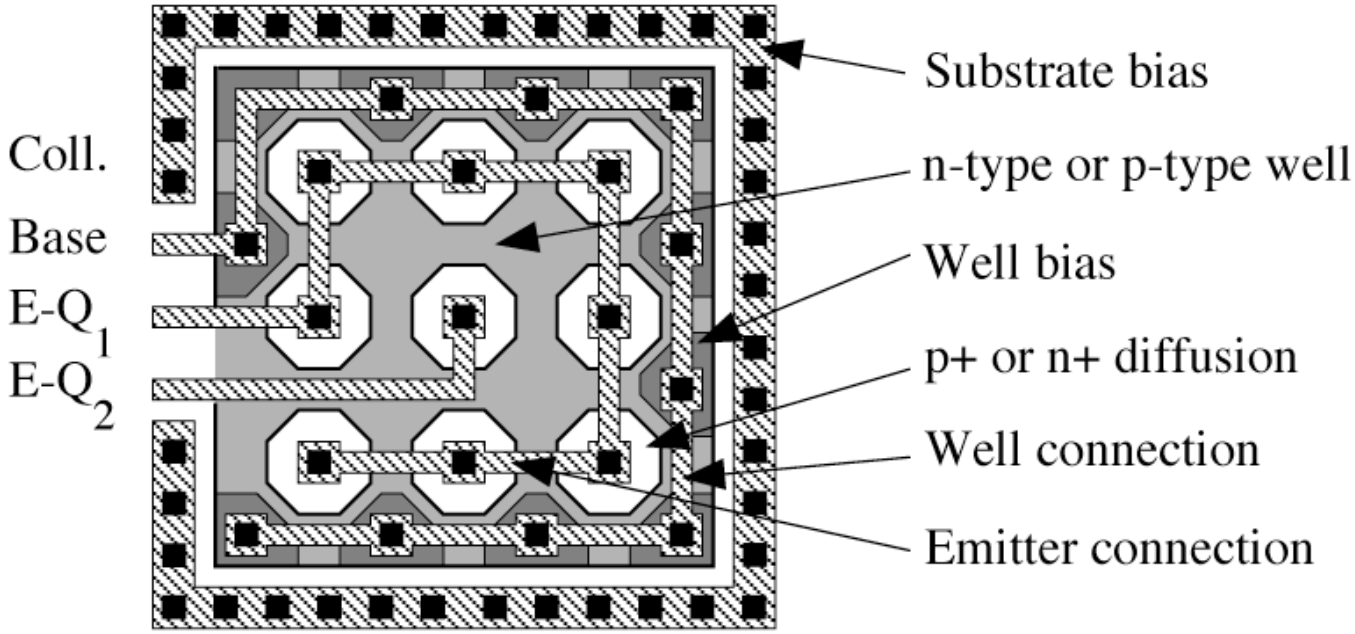
$$V_{BG} = V_G(T) - \left[V_G(T_0) - V_{BE}(T_0)\right]\frac{T}{T_0} - (\eta - \alpha)V_T \ln\frac{T}{T_0}$$

η is a process dependent parameter whose value ranges from 3 to 4

$$I_E = I_{E0}\left(\frac{T}{T_0}\right)^{\alpha}$$



Layout of a 8+1 BJT



- common centroid arrangement
- common well (same base voltage)