A PTAT Current Reference for CMOS

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Introduction

In the IC design course I attended in June at Portland State (thanks for not making it here on Monday, Duy!), Daniel Senderowicz made a provocative statement. Essentially, he said that there is never a valid excuse for biasing an analog cell with a resistor to VDD. You may get away with it, and it may seem quicker at the time, but the cost of a "proper" bias generator is not great in terms of die area, or even design time, if we are just a bit disciplined. When we bias our cells with simple resistor/diode bias networks, we knowingly introduce VDD sensitivity into our designs, which Senderowicz views as being hopelessly optimistic, if not plain stupid.

After thinking about it, I would say that I have to agree. Therefore I propose that we take more care in biasing the few analog cells that we use nowadays. This is not to say that one cannot get away with resistor biasing (as we obviously have many times), but if we can make our circuits less variable with temperature, without incurring excessive cost, then we should do so. It could be argued, also, that this is more critical as we move to lower supply voltages. In the typical resistor bias network (see Figure 1), where a resistor 'R' from VDD connects to an n-channel diode-connected MOSFET, the current that is established varies with the difference between VDD and the diode voltage VB. This difference becomes more variable when the diode takes up more of the supply range, as is the case with a lower VDD supply voltage (VB tends to stay approximately 1.0 V, even as process geometry is scaled down). Obviously the current also varies with the NMOS threshold voltage and the resistance.

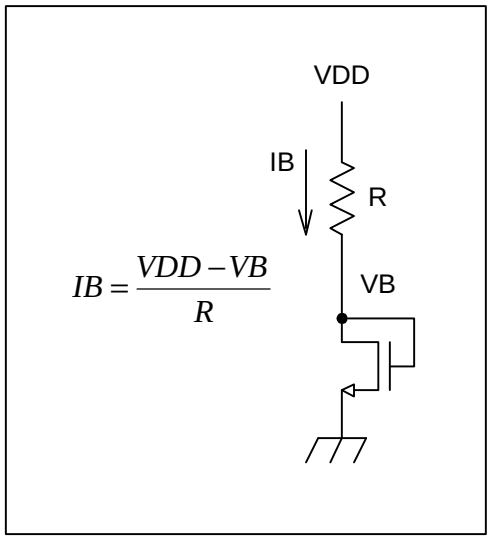

Figure 1

A sensitivity analysis of this circuit, relative to VDD, is not difficult, if we assume a voltage for VB.

$$S_{VDD}^{IB} = \frac{\partial IB}{\partial VDD} \cdot \frac{VDD}{IB} = \frac{1}{R}\left(\frac{VDD}{IB}\right) = \frac{VDD}{R\left(\frac{VDD - VB}{R}\right)} = \frac{VDD}{VDD - VB}$$

This result is perhaps worse than it appears at the start: the sensitivity can never be less than unity for real-world values of VDD and VB, and in practice is always more than unity. As VDD VB (decreasing from higher values),

the sensitivity tends toward infinity (the denominator tends toward zero with a finite numerator). Taking a typical example, if VDD = 5.0 V, and VB = 1.0 V, the sensitivity is 1.25. Now, if we scale to 3.3 V, and (generously) allow VB to go down to 0.8 V, the sensitivity degrades to 1.32. If VB had stayed at 1.0 V, as is probably more typical, sensitivity is even further degraded, to about 1.44.

Now, instead, imagine a bias generator that did not depend on VDD or threshold voltage, and which had a controlled dependence on temperature. Unfortunately, we cannot make an absolute current reference, but we can exploit the bipolar transistor available to us in a CMOS process to make a current reference that is dependent, to a large degree, only on resistance and temperature (This temperature dependence turns out to be desirable; see below. Obviously, we could make a relatively temperature independent current reference with a bandgap voltage reference and a resistor). As long as we use processes that give us tightly controlled resistance (e.g. ±15%), this gives us a pretty nice current reference, and in any case a reference that is better controlled than the resistance/diode based bias network of Figure 1.

This document describes a PTAT (proportional to absolute temperature) current reference that was suggested by Senderowicz. He recommends PTAT because it provides a first order correction to the transconductance variability of a MOSFET with temperature. Transconductance is a reasonably well-controlled parameter that should be a key design parameter goal in our circuits (as opposed to, for instance, output conductance, which is typically not well controlled or modeled). If we build our designs around transconductance, and aim to maintain transconductance constant over temperature, it will tend to make our designs more robust against temperature variation.

There is one caveat I can think of when it comes to using this PTAT bias generator. It is probably not a good idea for a physically large power output stage, because as the temperature increases, current increases. If the cell is large enough to influence the die temperature, it seems like this could cause a sort of “thermal runaway” wherein higher temperatures cause higher currents, causing higher power dissipation, causing even higher temperatures, and so on, ad nauseam.

Proposed PTAT current reference

The schematic for the proposed PTAT current reference is Figure 2. The circuit is relatively easy to analyze once the characteristics of the vertical PNP transistors are known. The circuit appears similar to a CMOS bandgap reference, and is in fact a subset of that familiar circuit. The bandgap must generate a PTAT voltage, and sum it with a VBE to end up with a low temperature coefficient voltage reference. But since we want PTAT to begin with, it is not necessary to worry about adding in the VBE.

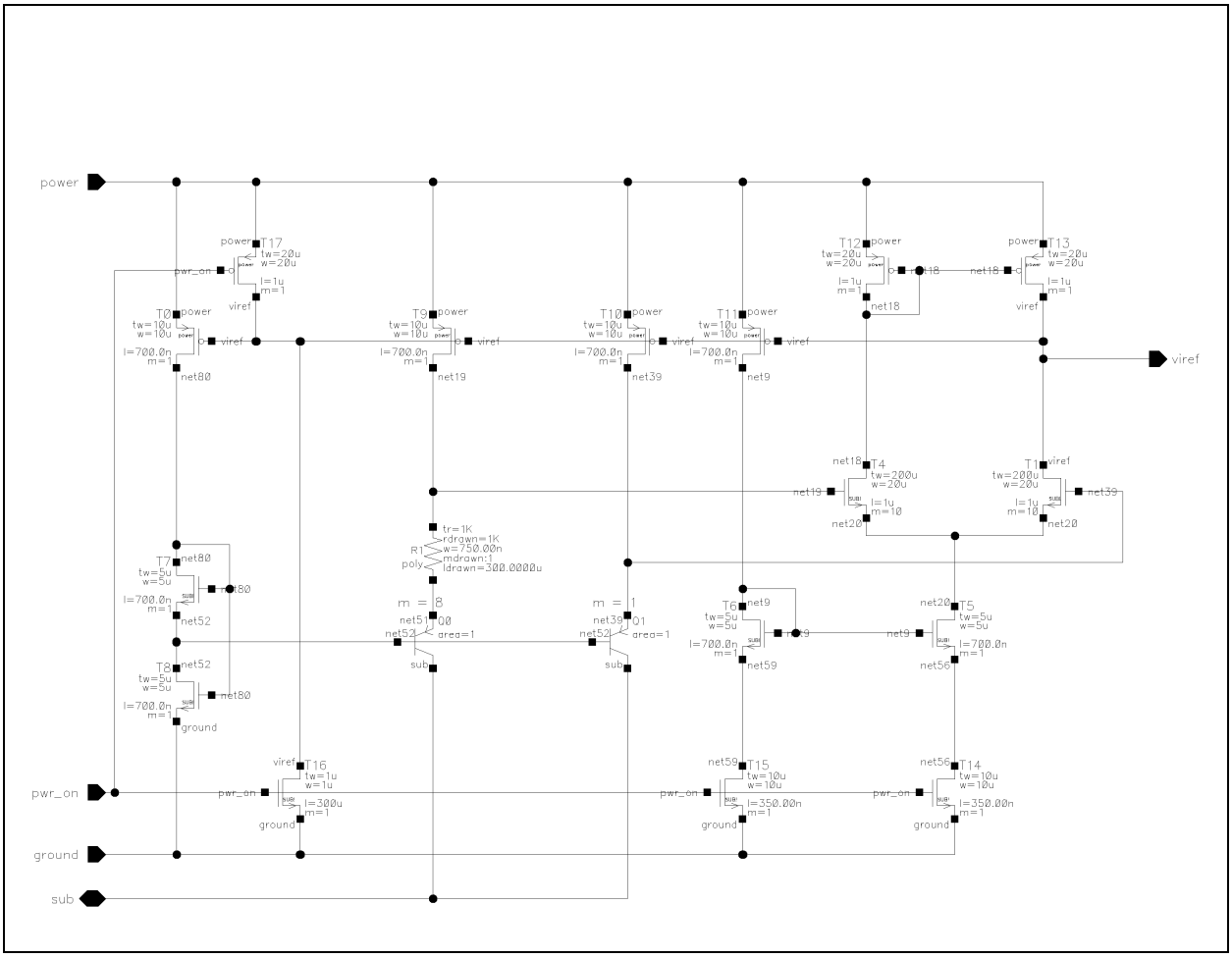

Figure 2 – schematic of cell 'pcbvg'

Referring to Figure 2, Q0 and Q1 are the vertical PNP transistors that generate the PTAT voltage, which is applied across resistor R1. First, recall that the difference in VBE between 2 transistors that have identical collector currents is as below:

$$\Delta VBE = VBE2 - VBE1 = VT \ln\left(\frac{IS1}{IS2}\right)$$

$$VT = \frac{kT}{q}$$

Note the remarkable fact that this voltage, ΔVBE, is dependent only on the saturation current ratio, constants k (Boltzmann's Constant) and q (charge on an electron), and T, the absolute temperature. The circuit above is

specified such that the ratio of saturation current of Q0 to that of Q1 is 8; this implies that the difference between the 2 VBE's, at room temperature, will be about 54 mV (VT = 26 mV, ln 8 = 2.1). Q0, being larger in area, will have the lower VBE. Incidentally, the condition that Q0 and Q1 have identical collector currents is enforced by T9 and T10, matched current sources that have identical terminal voltages and force the collector currents of Q0 and Q1, respectively.

Next notice that T1 and T4 make up an error amplifier that acts to force the voltages at the top of R1 and at the emitter of Q1 to be equal. But for this to be true, the difference in VBE's between Q0 and Q1 must appear across R1. For that to be the case T9 must source the current ΔVBE /R1 (about 54 μA at room temperature). So we have T9 supplying the current ΔVBE/R1, which is dependent only on the area ratio between Q0 and Q1, VT, and R1. VT is directly proportional to absolute temperature, scaled by a constant; the area ratio between Q0 and Q1 is set by design to 8, and R1 is a reasonably stable and accurate poly resistor (the temperature coefficient of poly resistors in the processes we use is on the order of 0.1%/ C). Since the loop acts to drive voltage 'viref' such that T9 sources this current, if we connect another p-channel transistor, matched to T9, with source to the 'power' net and gate to the 'viref' net, it will be a current source nominally matched to T9. In fact this idea is used within the cell to bias the differential amplifier tail (T5) and the bias voltage-generating network T7 and T8.

This brings up the issue of startup, since the circuit is bootstrapped; the internal circuitry expects the reference current to be there in order to work. The circuit does have a trivial solution wherein all the currents are zero, which means that it might not start up, except for T16. When 'pwr_on' is high, T16 weakly pulls down on the 'viref' node, turning on T9 and T10 such that the circuit is not allowed to stabilize at the zero-current state. T16 draws only about 1 μA when on, and therefore does not significantly disturb the normal operation of the circuit.

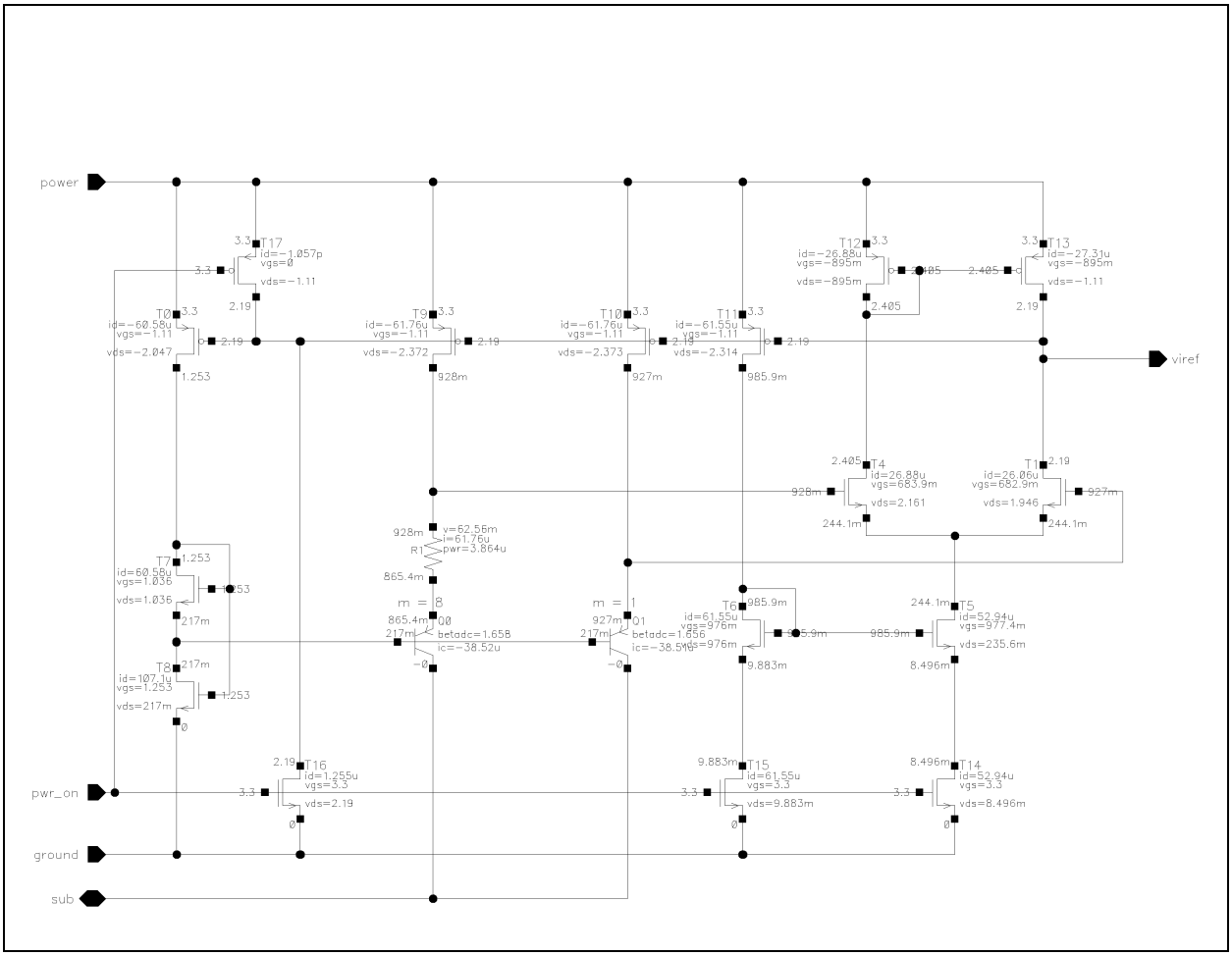

Figure 3 – 'pcbvg' cell schematic with operating points annotated

Performance of the circuit

A simulation test fixture was constructed for the cell ‘pcbvg’ (PTAT Current Bias Voltage Generator) and simulations were done in HSpice to prove the cell’s performance. Figure 4 is a schematic of the test fixture.

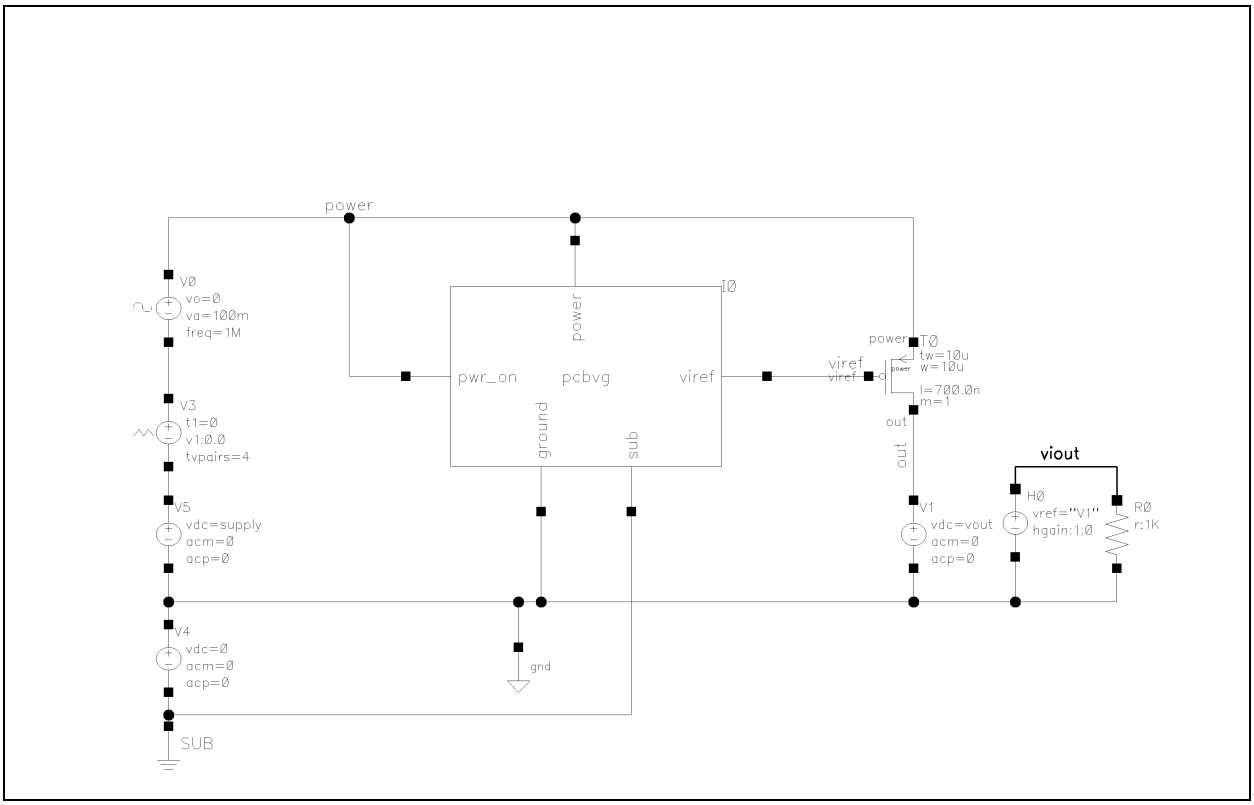

Figure 4 - Simulation Test Fixture

P-channel device T0 is connected to the ‘viref’ output of the reference generator to make a current source that mirrors the internal reference current. Current controlled current source H0 converts the current through V1 to a voltage at node ‘viout’, with a transresistance gain of 1.0 Ohm. This provides a convenient way to plot output current.

Figure 5 shows the performance of the current source T0 when biased by the PTAT generator. Remember that high output impedance is not a prime consideration in this case. At a temperature of 50 C, for instance, the output current is about 64 µA when the drain of T0 is grounded. The uniform spacing between the curves shows the reasonably linear relationship between temperature and output current that this circuit provides.

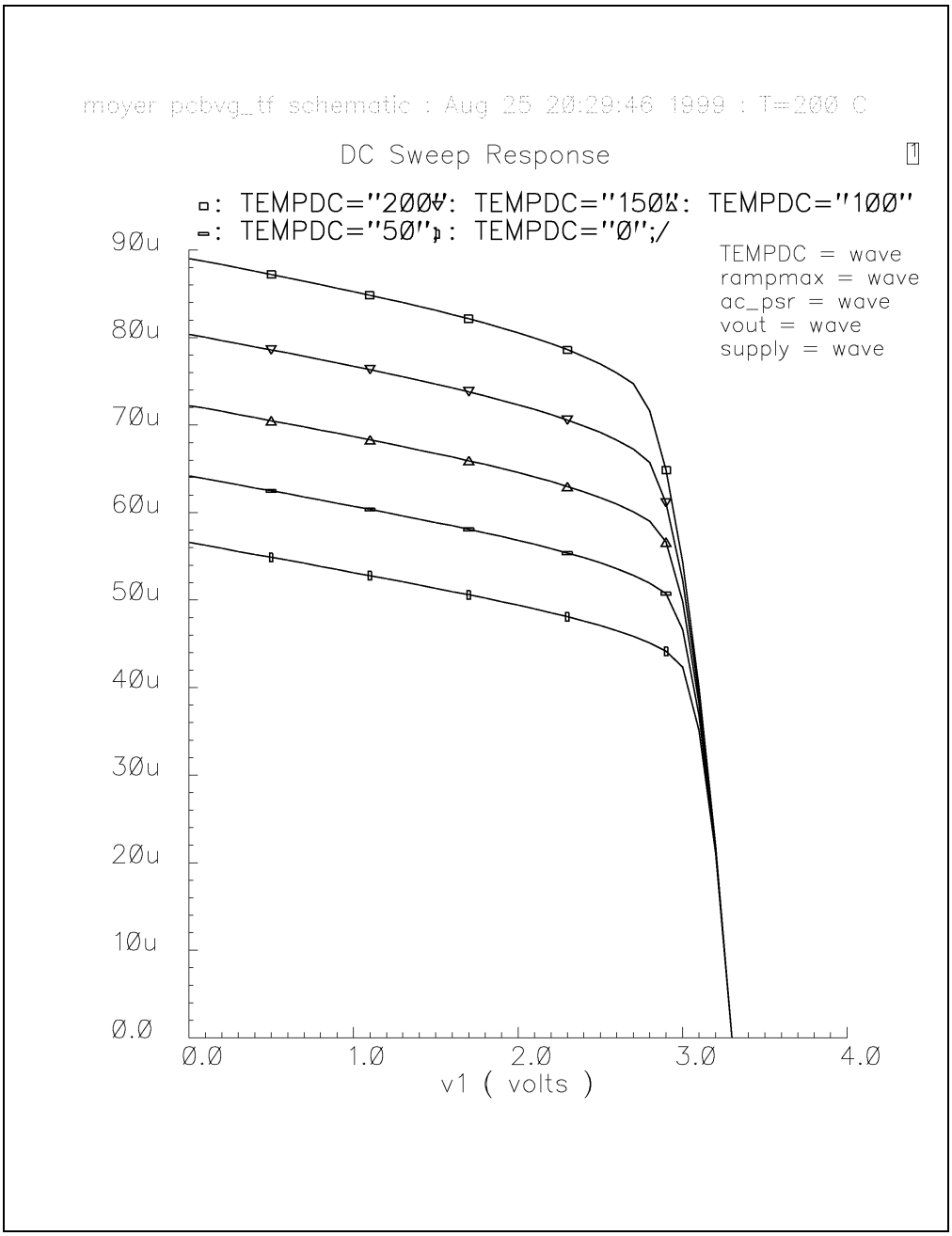

Figure 5 - Output Characteristic for Different Temperatures

Figure 6 shows more clearly how output current varies with temperature, for a fixed Vds of –3.3 V (V1 = 0 V). Over the simulated range of 0 – 200 C the dependence is again shown to be quite linear. A theoretical point at (-273,0) was placed on this graph to show how well the circuit extrapolates to an ideal PTAT source (at –273 C, absolute zero on the Kelvin scale, the output current would theoretically be zero for an ideal PTAT source). A small difference in slope is noted at the junction between simulated performance and extrapolated ideal performance.

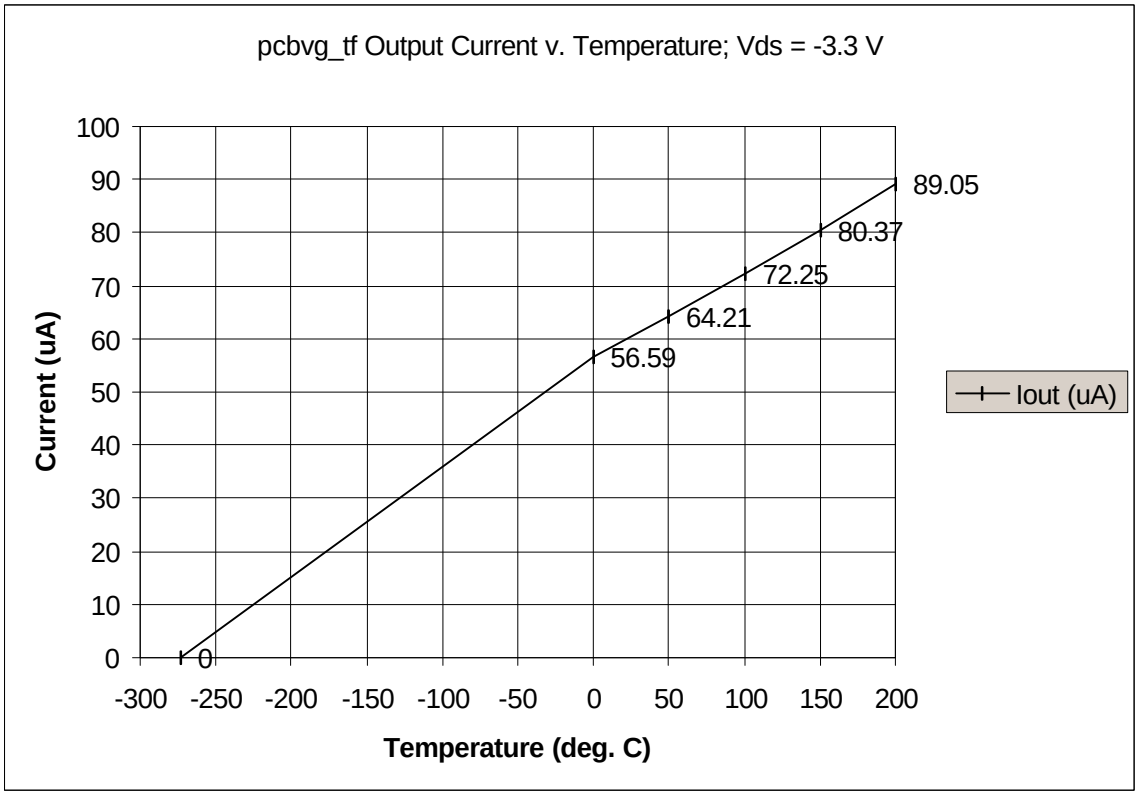

Figure 6 - Output Current v. Temperature

Ideally this current source should have no dependence on VDD; Figure 7 shows how dependent the circuit is on the supply voltage. The sensitivity is about 1.2 µA/V at low frequencies. This would imply that a 5 % change in VDD (nominal 3.3 V) would change the output current by about 200 nA. Relative to 64 µA this is a 0.3 % change in output current. Therefore the sensitivity is about 0.3/5 = 0.06, significantly better than the VDD-based current reference (sensitivities on the order of 1.0). Most of the sensitivity that the circuit does exhibit can be traced to T16, the startup device. Since it connects from 'viref' to ground, as power supply variations couple to 'viref' (desirable, since the output mirror is referred to VDD) the current through T16 is modulated. This means that the error amplifier (T1, T4, T12, T13) has to supply a VDD-dependent current (out of T13's drain, into T16's drain), and that the input differential voltage must therefore change with VDD somewhat. This effect can be reduced by increasing the resistance of T16 (at the expense of larger area), or by perhaps using another method for startup. Also, it might be possible to increase the gain of the error amplifier, so that the change input differential voltage would be less.

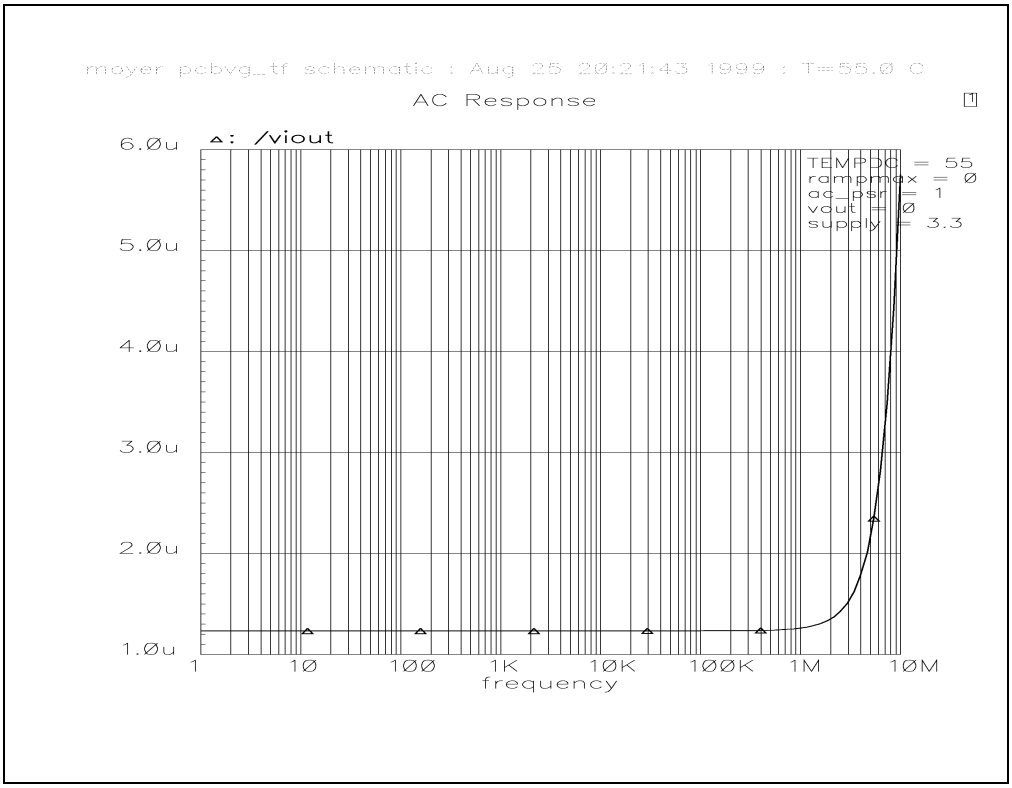

Figure 7 - Power Supply Sensitivity v. Frequency (uA/V)

It's also noted from Figure 7 that the power supply rejection gets worse as the frequency starts to increase past 1 MHz. If this is a problem, it can be addressed by bypassing the 'viref' node to VDD, or by directly bypassing VDD. It would also be possible to filter the 'viref' output voltage before applying it to the gate of the output mirror device with an RC network (remember to connect the capacitor to VDD, not ground) for even more effective high frequency supply rejection.