

Design of analog integrated circuits part 2: Operational Amplifiers

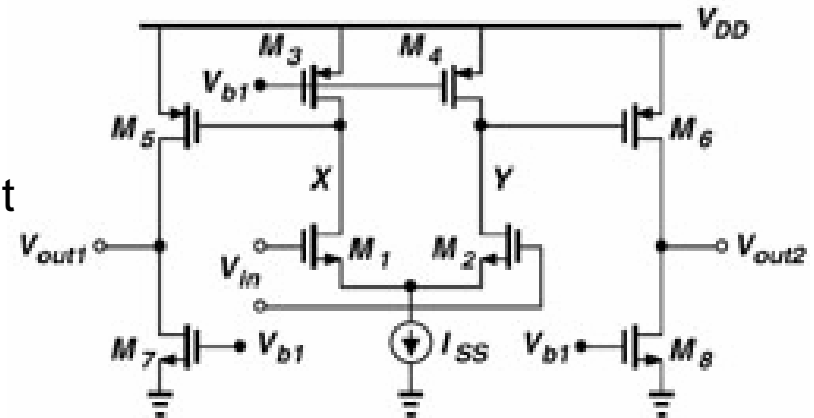
Note: some figures were taken from references:

1.- *B. Razavi, Design of Analog CMOS Integrated Circuits, Mc Graw-Hill, 2001*

2.- *R. J. Baker et al., CMOS Circuit Design, Layout and Simulation, Wiley Interscience, 1st Edition, 1998.*

Example of CMOS OPAMP design 6

Exercise 2: in the two stage Opamp of Fig. shown below, $W/L = 50/0.5$ for all transistors except for M5,6, for which $W/L = 60/0.5$. Also $I_{SS} = 0.25mA$ and the each output branch is biased at $1mA$. Assume $V_{DD} = 3V$, $V_{b1} = 1.09V$, Determine:



- The common level at nodes X and Y.
- The maximum output voltage swing.
- If each output node is loaded by a 1pF capacitor, compensate the Opamp by Miller multiplication for a phase margin of 60° in unity-gain feedback. Calculate the pole and zero before and after compensation.
- The slew rate.

Parámetros de transistores:

$$\begin{aligned} \mu_n C_{ox} &= 134 \mu A/V^2, \quad \mu_p C_{ox} = 38.3 \mu A/V^2, \\ \lambda_n &= 0.1 V^{-1}, \quad \lambda_p = 0.2 V^{-1}, \\ \gamma &= 0, \quad V_{THN} = 0.7V, \quad V_{THP} = -0.8V, \\ C_{gd6} &= 0.18 fF, \quad C_{db6} = 52.1 fF, \quad C_{gd8} = 0.2 fF, \\ C_{db8} &= 23.4 fF, \end{aligned}$$

To be solved in the classroom

Example of CMOS OPAMP design 7

Solución:

(a) CM level $V_X = V_Y = V_{DD} - V_{GS5} = V_{DD} - V_{GS6}$

de: $I = 1mA = \frac{1}{2} \mu_p C_{ox} (60/0.5)(|V_{GS6}| - |V_{THP}|)$ $\Rightarrow V_{GS6} = 1.46V$

así: $V_X = V_Y = 3 - 1.46 = 1.54V$

(b) Output swing $V_{O_max} = V_{DD} - V_{OD6} = 3 - (1.46 - 0.8) = 2.34V$

de: $I = 1mA = \frac{1}{2} \mu_p C_{ox} (50/0.5)(V_{b1} - V_{THN})$ $\Rightarrow V_{b1} = 1.09V$

así: $V_{O_min} = V_{OD8} = V_{b1} - V_{THN} = 1.09 - 0.7 = 0.39V$

El máximo output swing = $2.34 - 0.39 = 1.95V$

Example of CMOS OPAMP design 8

Solución (cont.):

(c) Compensación del opamp

Antes de compensar

$$\text{donde } R_y = r_{ON2} // r_{OP4}$$

$$R_O = r_{ON8} // r_{OP6}$$

Polo dominante $\omega_y = 1/C_y R_y$

2do polo $\omega_o = 1/C_o R_o$

$$C_y = C_{gd4} + C_{db4} + C_{gd2} + C_{db2} + C_{gs6} + C_{gd6}(1 + |A_{v2}|)$$

$$C_o = C_L + [C_{db6} + C_{gd6}(1 + 1/|A_{v2}|)] + C_{db8} + C_{gd8}$$

$$r_{ON2} = 1/(0.1 \times 0.125 \text{mA}) = 80 \text{k}\Omega$$

$$r_{OP4} = 1/(0.2 \times 0.125 \text{mA}) = 40 \text{k}\Omega$$

$$r_{ON8} = 1/(0.1 \times 1 \text{mA}) = 10 \text{k}\Omega$$

$$r_{OP6} = 1/(0.2 \times 1 \text{mA}) = 5 \text{k}\Omega$$

$$R_y = r_{ON2} // r_{OP4} = 26.67 \text{k}\Omega,$$

$$R_o = r_{ON8} // r_{OP6} = 3.33 \text{k}\Omega$$

Example of CMOS OPAMP design 9

Solución (cont.):

$$g_{m2} = (2 \times 1.34 \times 10^{-4} \times 100 \times 0.125 \times 10^{-3})^{1/2}$$
$$= 1.83 \text{ mA/V}$$

$$g_{m6} = (3.83)(60/0.5)(1.46 - 0.8)$$
$$= 3.03 \text{ mA/V}$$

$$A_{v1} = -g_{m2}R_y = -48.8 \text{ V/V}$$

$$A_{v2} = -g_{m6}R_O = -10.1 \text{ V/V}$$

$$A = A_{v1} A_{v2} = (-48.8)(-10.1) = 492.4 \text{ V/V}$$

$$C_O = 1 \text{ pF} + 52.1 \text{ fF} + 0.18 \text{ fF}(1 + 1/10.1) + 23.4 \text{ fF} + 0.2 \text{ fF} = 1.076 \text{ pF}$$

$$C_y = [0.15 + 43.8 + 0.2 + 23.4 + 76.6 + 0.18(1 + 1/10.1)] \text{ fF} = 146.1 \text{ fF}$$

Antes de compensar

Polo dominante $w_y = 1/C_y R_y = 1/(146.1 \text{ pF})(26.67 \text{ k}\Omega) = 2.57 \times 10^8 \text{ rad/s}$

2do polo $w_o = 1/C_O R_O = 1/(1.076 \text{ pF})(3.33 \text{ k}\Omega) = 2.79 \times 10^8 \text{ rad/s}$

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Solución (cont.):

Despues de compensar

$$\text{2do polo } w'_o = g_{m6}/(C_y + C_o) = 3.03mA/V/(1.076pF + 146.1fF) = 2.48x10^9 \text{ rad/s}$$

$$\text{Polo dominante } w'_y = 1/[C_y + C_C(1 + |A_{v2}|)R_y]$$

Para un margen de fase de 60°, tenemos:

$$90^\circ + \tan^{-1}(w'_1/w'_o) = 120^\circ \quad \Rightarrow \quad w'_1 = w'_o \tan^{-1}(30^\circ) = 1.43x10^9 \text{ rad/s}$$

$$\log(w'_1/w'_y) = 53dB/20dB/dec \quad \Rightarrow \quad w'_y = w'_1/10^{53.8/20} = 2.91x10^6 \text{ rad/s}$$

$$C_C = \{[(2.91x10^6)(26.67x10^3) - 146.1fF] / (1 + 10.08)\} = 1.15pF$$

Nótese que: $C_C \gg C_y$

$$\text{The zero: } w_Z = g_{m6}/(C_C + C_{gd6}) = 3.03x10^{-3}/(1.015pF + 0.18fF) = 2.63x10^9 \text{ rad/s}$$

Nótese que: $w_Z > w'_y, w'_o$

Example of CMOS OPAMP design 11

Solución (cont.):

(d) Determinando el valor de R_Z :

$$\text{de: } w_Z = 1/[C_C(1/g_{m6} - R_Z)] = -|w'_o|$$

$$R_Z = 1/g_{m6} + 1/(|w'_o| C_C) = 680.7\Omega$$

(e) Determinando el Slew Rate

$$\text{SR en } V_{O2} = -I_{D4}/C_C = -0.125\text{mA}/1.15\text{pF} = -1.09 \times 10^8 \text{ V/s}$$

$$\text{SR en } V_{O1} = -\text{SR en } V_{O2} = 1.09 \times 10^8 \text{ V/s}$$

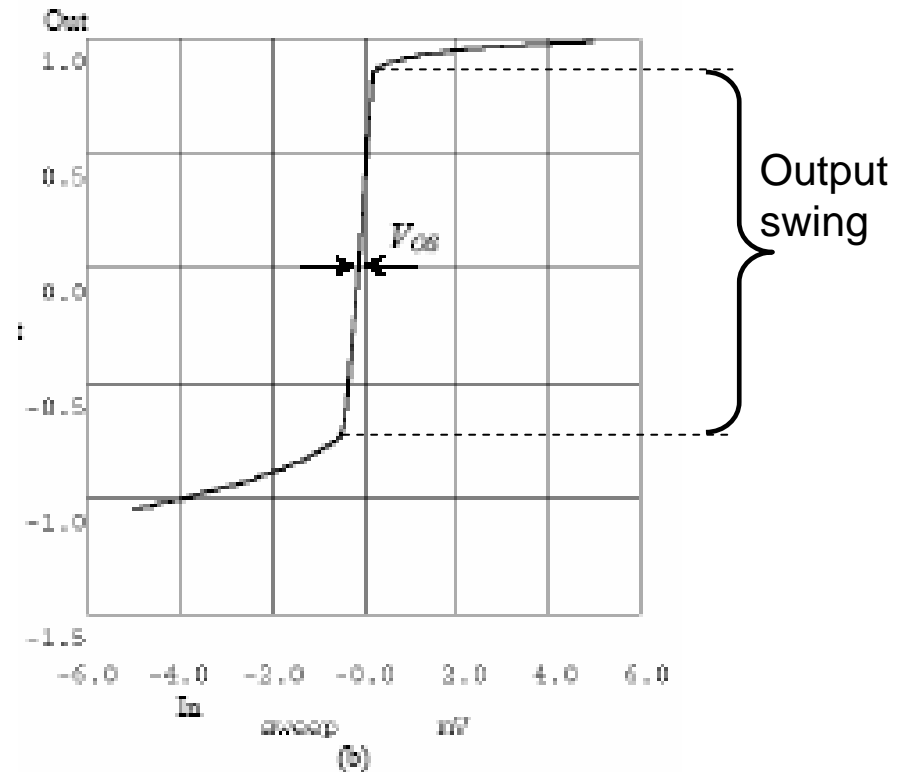
Characterizing the opamp

(b) The output swing:

This parameter is determined from the output stage of the Opamp.

From the example shown below, the output swing is the range where the output voltage is linearly related to the input, i.e. $\pm 0.8V$.

Notice from the same curve, the corresponding input voltage is $\sim \pm 5mV$ for such a value of output swing.

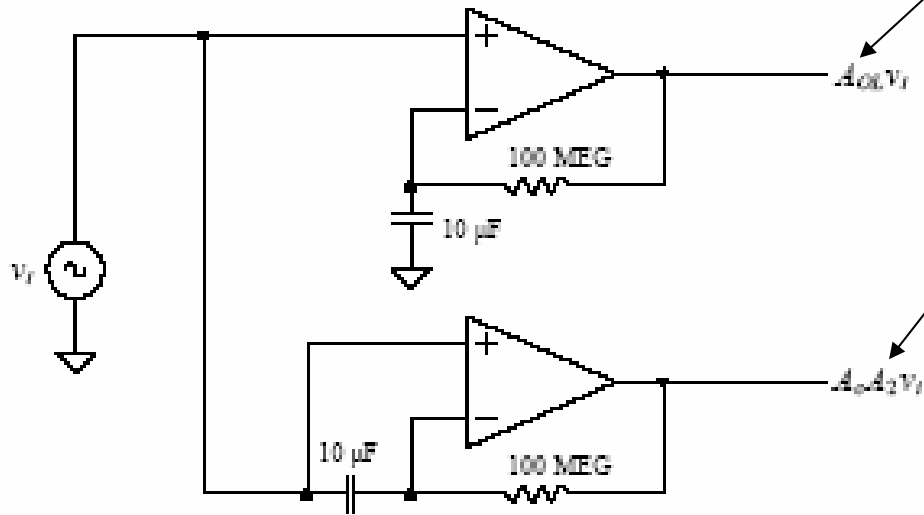


Characterizing the opamp

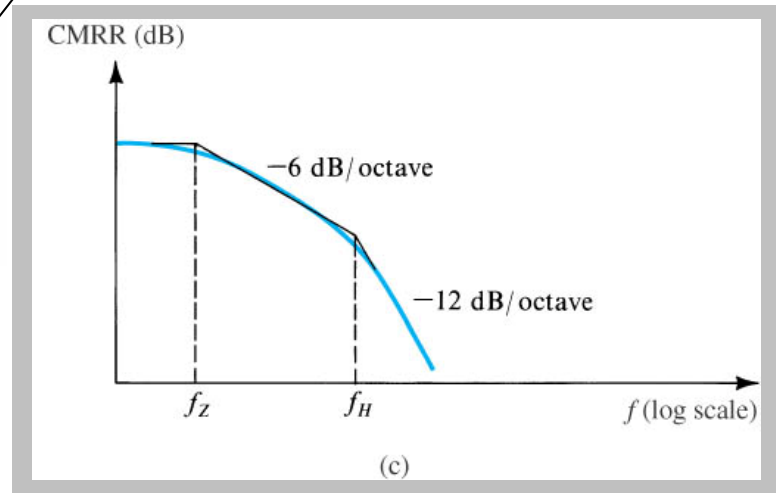
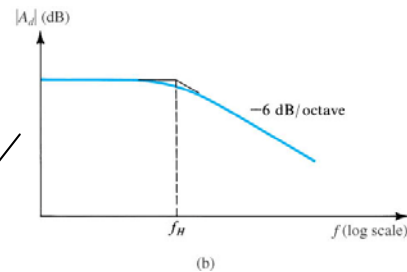
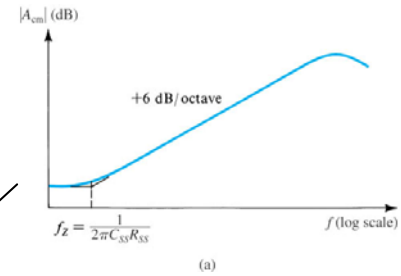
(c) The CMRR:

The CMRR of the Opamp is defined as:

$$CMRR = 20 \log \left(\frac{A_{OL}}{A_C A_2} \right) = 20 \log \left(\frac{A_1}{A_C} \right)$$



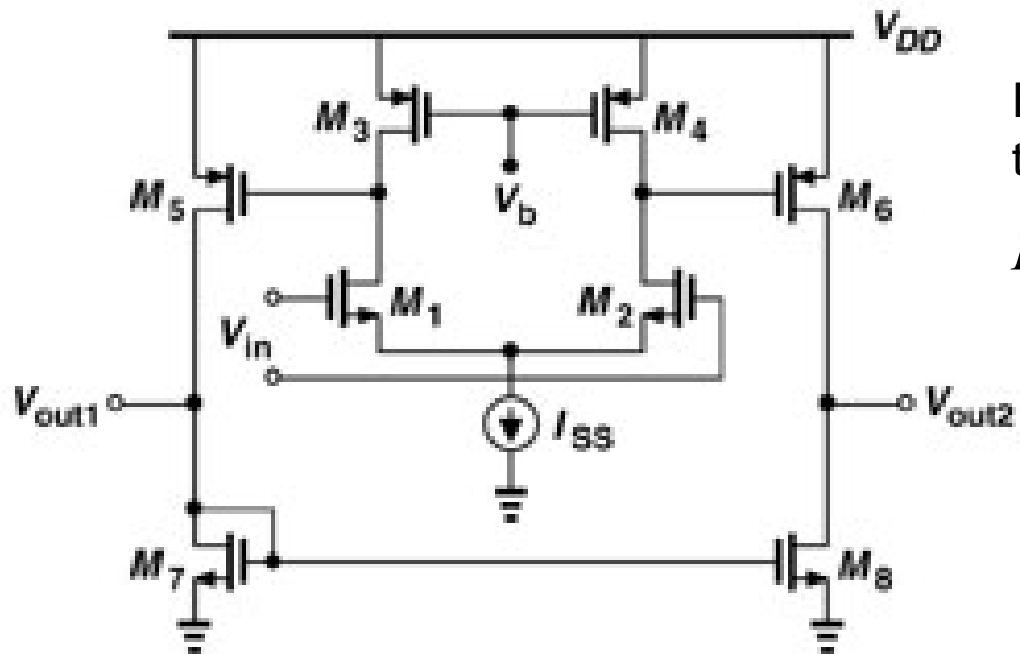
Circuit to measure or simulate the CMRR



Characterizing the opamp

(d) Power Dissipation

The P_D in the opamp is the product of the sum of the currents flowing in the current sources with the power supply voltages



For the two stage opamp, the dissipated power is:

$$P_D = (V_{DD})(I_{D5} + I_{D6} + I_{SS})$$

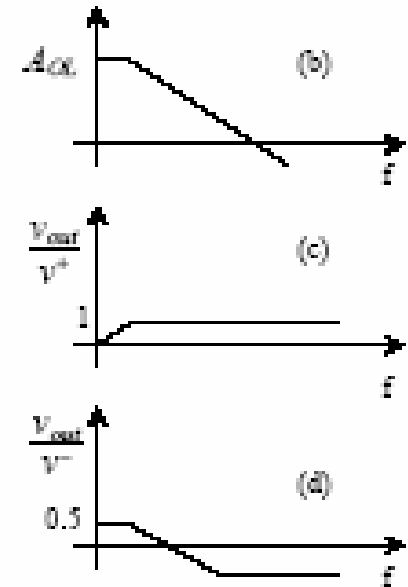
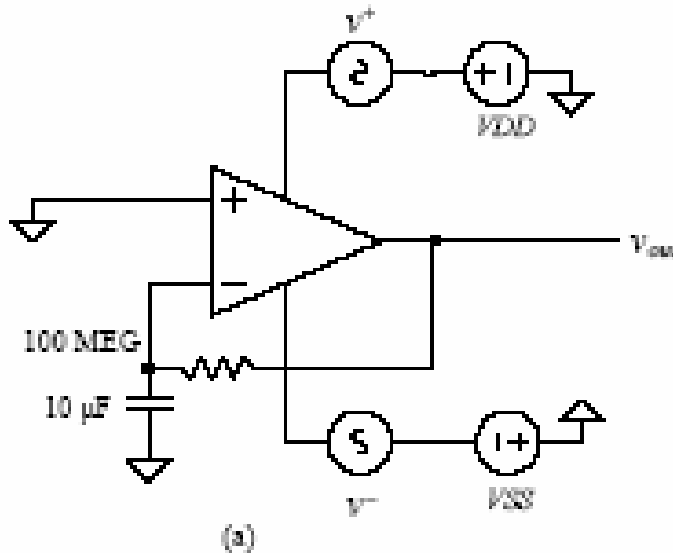
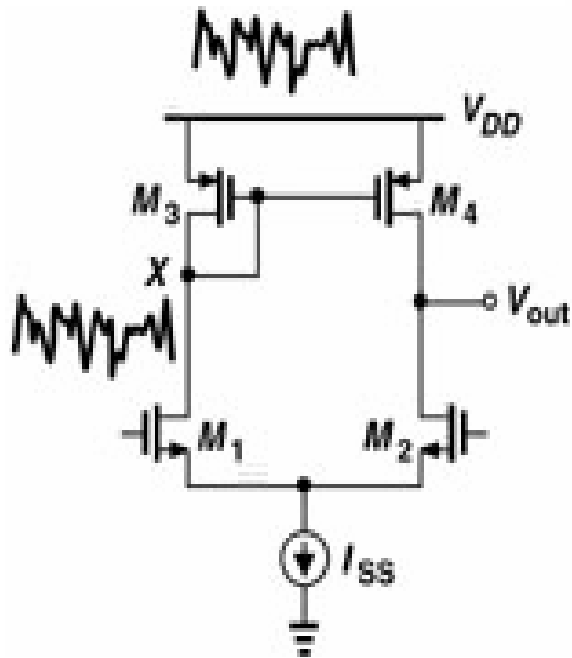
Characterizing the opamp

(e) PSRR:

The power supply rejection ratio is a term used to describe how well the Opamp rejects noise or changes on bias buses.

$$PSSR^+ = \frac{A_{OL}}{v_o / v^+}$$

$$PSSR^- = \frac{A_{OL}}{v_o / v^-}$$



Example of a circuit to simulate the PSRR.

Characterizing the opamp

(e) SR:

A configuration such as the circuit in figure is useful to measure or simulate the slew rate

$$SR = I/C$$

