CHAPTER 6 - CMOS OPERATIONAL AMPLIFIERS

Chapter Outline

Goal

Understand the analysis, design, and measurement of simple CMOS op amps

Design Hierarchy

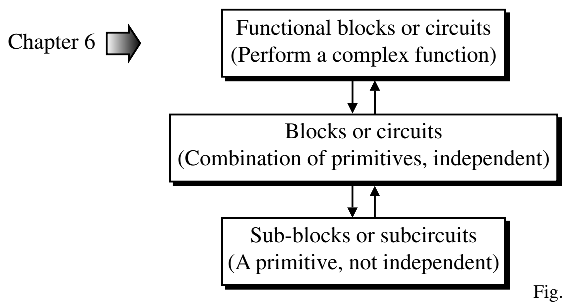


Fig. 6.0-1

The op amps of this chapter are unbuffered and are OTAs but we will use the generic term “op amp”.

SECTION 6.1 - DESIGN OF CMOS OPERATIONAL AMPLIFIERS

High-Level Viewpoint of an Op Amp

Block diagram of a general, two-stage op amp:

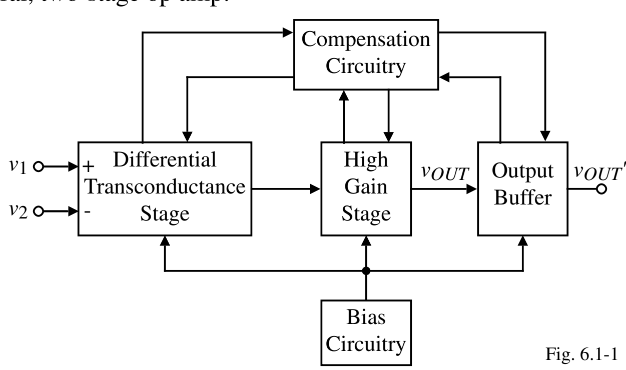


Fig. 6.1-1

- Differential transconductance stage:
  Forms the input and sometimes provides the differential-to-single ended conversion.
- High gain stage:
  Provides the voltage gain required by the op amp together with the input stage.
- Output buffer:
  Used if the op amp must drive a low resistance.
- Compensation:
  Necessary to keep the op amp stable when resistive negative feedback is applied.

Ideal Op Amp

Symbol:

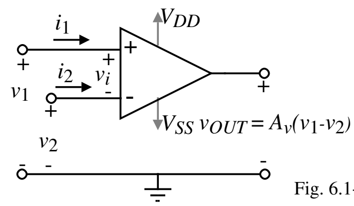


Fig. 6.1-2

Null port:

If the differential gain of the op amp is large enough then input terminal pair becomes a null port.

A null port is a pair of terminals where the voltage is zero and the current is zero.

I.e.,

$$v_1 - v_2 = v_i = 0$$

and

$$i_1 = 0 \text{ and } i_2 = 0$$

Therefore, ideal op amps can be analyzed by assuming the differential input voltage is zero and that no current flows into or out of the differential inputs.

General Configuration of the Op Amp as a Voltage Amplifier

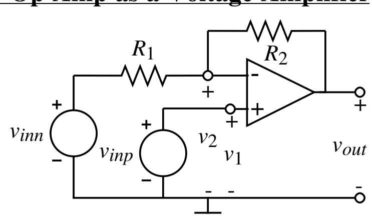


Fig. 6.1-3

Noninverting voltage amplifier:

$$v_{inn} = 0 \quad \Rightarrow \quad v_{out} = \left(\frac{R_1+R_2}{R_1}\right)v_{inp}$$

Inverting voltage amplifier:

$$v_{inp} = 0 \quad \Rightarrow \quad v_{out} = -\left(\frac{R_2}{R_1}\right)v_{inn}$$

Example 6.1-1 - Simplified Analysis of an Op Amp Circuit

The circuit shown below is an inverting voltage amplifier using an op amp. Find the voltage transfer function, v_{out}/v_{in}.

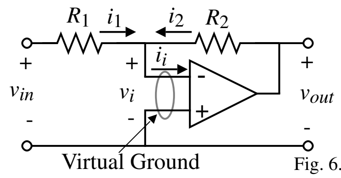


Fig. 6.1-4

Solution

If the differential voltage gain, A_v, is large enough, then the negative feedback path through R_2 will cause the voltage v_i and the current i_i shown on Fig. 6.1-4 to both be zero. Note that the null port becomes the familiar *virtual ground* if one of the op amp input terminals is on ground. If this is the case, then we can write that

$$i_1 = \frac{v_{in}}{R_1}$$

and

$$i_2 = \frac{v_{out}}{R_2}$$

Since, $i_i = 0$, then $i_1 + i_2 = 0$ giving the desired result as

$$\frac{v_{out}}{v_{in}} = -\frac{R_2}{R_1}.$$

Linear and Static Characterization of the Op Amp

A model for a nonideal op amp that includes some of the linear, static nonidealities:

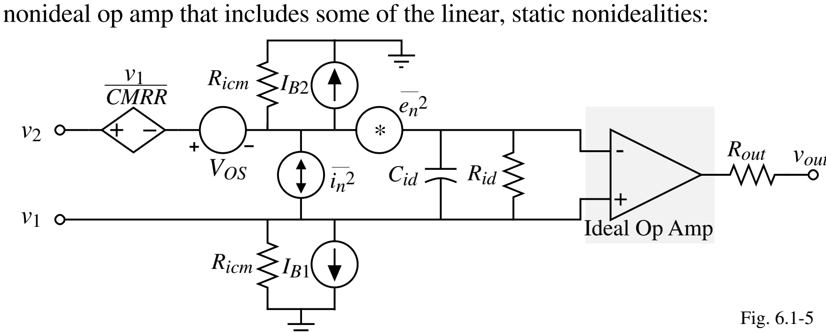


Fig. 6.1-5

where

R_{id} = differential input resistance

C_{id} = differential input capacitance

R_{icm} = common mode input resistance

V_{OS} = input-offset voltage

I_{B1} and I_{B2} = differential input-bias currents

I_{OS} = input-offset current ($I_{OS} = I_{B1}-I_{B2}$)

$CMRR$ = common-mode rejection ratio

$\overline{e_n^2}$ = voltage-noise spectral density (mean-square volts/Hertz)

$\overline{i_n^2}$ = current-noise spectral density (mean-square amps/Hertz)

Linear and Dynamic Characteristics of the Op Amp

Differential and common-mode frequency response:

$$V_{out}(s) = A_v(s)[V_1(s) - V_2(s)] \pm A_c(s)\left(\frac{V_1(s)+V_2(s)}{2}\right)$$

Differential-frequency response:

$$A_v(s) = \frac{A_{v0}}{\left(\frac{s}{p_1} - 1\right)\left(\frac{s}{p_2} - 1\right)\left(\frac{s}{p_3} - 1\right)\cdots}$$

where $p_1, p_2, p_3, \cdots$ are the poles of the differential-frequency response.

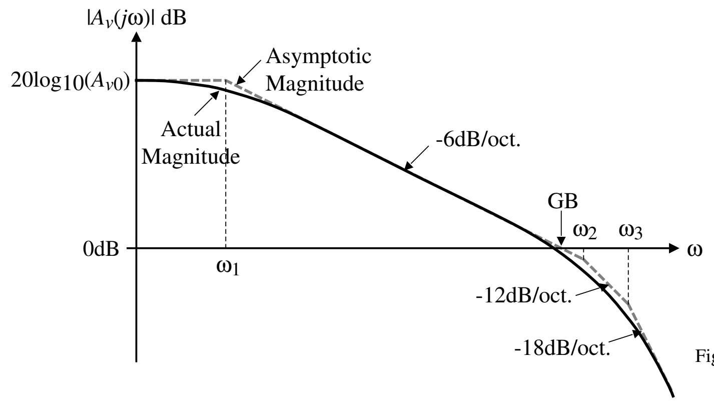


Fig. 6.1-6

Other Characteristics of the Op Amp

Power supply rejection ratio (*PSRR*):

$$PSRR = \frac{\Delta V_{DD}}{\Delta V_{OUT}} A_v(s) = \frac{V_o/V_{in}\ (V_{dd} = 0)}{V_o/V_{dd}\ (V_{in} = 0)}$$

Input common mode range (*ICMR*):

ICMR = the voltage range over which the input common-mode signal can vary without influence the differential performance

Slew rate (*SR*):

SR = output voltage rate limit of the op amp

Settling time (T_s):

T_s = time needed for the output of the op amp to reach a final value to with a predetermined tolerance when excited by a small signal. (SR is large signal excitation)

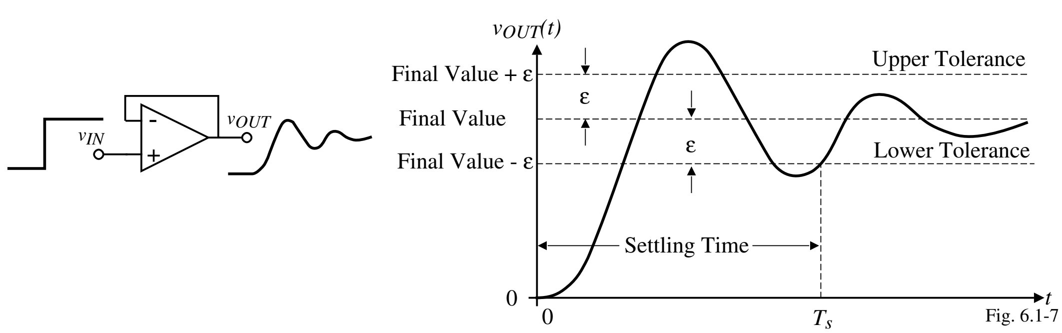


Fig. 6.1-7

Classification of CMOS Op Amps

Categorization of op amps:

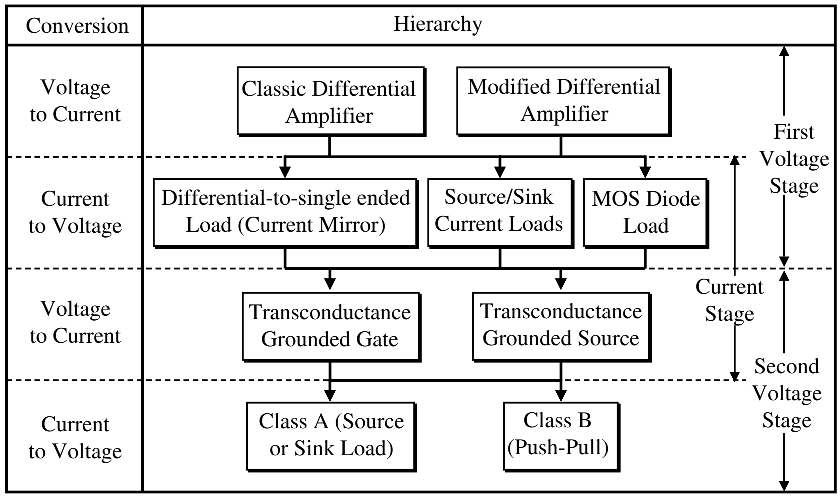


Table 6.1-1

Two-Stage CMOS Op Amp

Classical two-stage CMOS op amp broken into voltage-to-current and current-to-voltage stages:

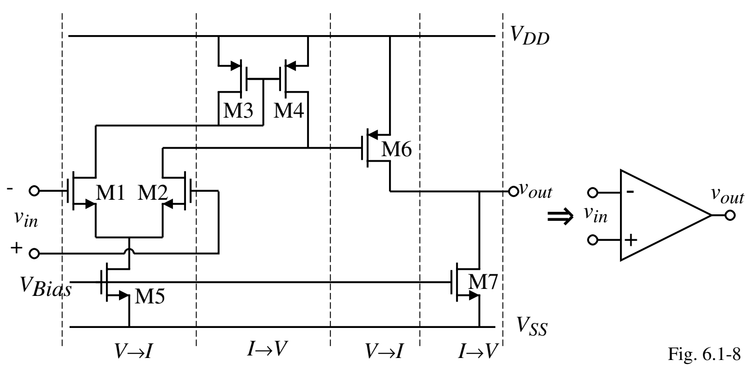


Fig. 6.1-8

Folded Cascode CMOS Op Amp

Folded cascode CMOS op amp broken into stages.

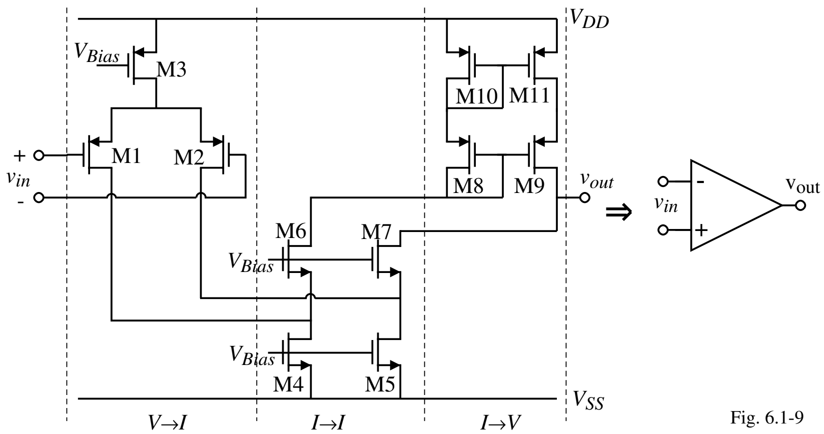


Fig. 6.1-9

Design of CMOS Op Amps

Steps:

1.) Choosing or creating the basic structure of the op amp.

This step generally is defined by a schematic showing the various transistors and their interconnections.

Generally this diagram does not change throughout the remaining portion of the design unless the specifications cannot be met and then a new or modified structure must be developed.

2.) Selection of the dc currents and transistor sizes.

Most of the effort of design is in this category.

Simulators are used to aid the designer in this phase (it is important that the design NOT use the simulator to do design). The general performance of the circuit should be known a priori.

3.) Physical implementation of the design.

Layout of the transistors

Floorplanning the connections, pin-outs, power supply buses and grounds

Extraction of the physical parasitics and resimulation

Verification that the layout is a physical representation of the circuit.

4.) Fabrication

Done by others (take a vacation)

5.) Measurement

Verification of the specifications

Modification of the design as necessary

Boundary Conditions and Requirements for CMOS Op Amps

Boundary conditions:

1. Process specification (V_T, K', C_{ox}, etc.)
2. Supply voltage and range
3. Supply current and range
4. Operating temperature and range

Requirements:

1. Gain
2. Gain bandwidth
3. Settling time
4. Slew rate
5. Common-mode input range, *ICMR*
6. Common-mode rejection ratio, *CMRR*
7. Power-supply rejection ratio, *PSRR*
8. Output-voltage swing
9. Output resistance
10. Offset
11. Noise
12. Layout area

Specifications for a Typical Unbuffered CMOS Op Amp

Boundary Conditions	Requirement
Process Specification	See Tables 3.1-1 and 3.1-2
Supply Voltage	±2.5 V ±10%
Supply Current	100 μA
Temperature Range	0 to 70°C
Specifications	
Gain	≥ 70 dB
Gainbandwidth	≥ 5 MHz
Settling Time	≤ 1 μsec
Slew Rate	≥ 5 V/μsec
Input *CMR*	≥ ±1.5 V
CMRR	≥ 60 dB
PSRR	≥ 60 dB
Output Swing	≥ ±1.5 V
Output Resistance	N/A, capacitive load only
Offset	≤ ±10 mV
Noise	≤ 100nV/$\sqrt{\text{Hz}}$ at 1KHz
Layout Area	≤ 10,000 min. channel length^2

Some Practical Thoughts on Op Amp Design

1.) Decide upon a suitable topology.
- Experience is a great help
- The topology should be the one capable of meeting most of the specifications
- Try to avoid "inventing" a new topology but start with an existing topology

2.) Determine the type of compensation needed to meet the specifications.
- Consider the load and stability requirements
- Use some form of Miller compensation or a self-compensated approach (shown later)

3.) Design device sizes for proper dc, ac, and transient performance.
- This begins with hand calculations based upon approximate design equations.
- Compensation components are also sized in this step of the procedure.
- After each device is sized by hand, a circuit simulator is used to fine tune the design.†

Two basic steps of design:

1.) "First-cut" - this step is to use hand calculations to propose a design that has potential of satisfying the specifications. Design robustness is developed in this step.

2.) Optimization - this step uses the computer to refine and optimize the design.

† A useful rule in analog design is: (Use of a simulator)x(Common sense) = Constant. Do not use a simulator for design but for optimization.

SECTION 6.2 - COMPENSATION OF OP AMPS

Compensation

Objective

Objective of compensation is to achieve stable operation when negative feedback is applied around the op amp.

Types of Compensation

1. Miller - Use of a capacitor feeding back around a high-gain, inverting stage.
   - Miller capacitor only
   - Miller capacitor with an unity-gain buffer to block the forward path through the compensation capacitor. Can eliminate the RHP zero.
   - Miller with a nulling resistor. Similar to Miller but with an added series resistance to gain control over the RHP zero.
2. Self compensating - Load capacitor compensates the op amp (later).
3. Feedforward - Bypassing a positive gain amplifier resulting in phase lead. Gain can be less than unity.

Single-Loop, Negative Feedback Systems

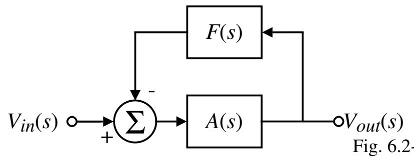


Fig. 6.2-1

$A(s)$ = amplifier gain (normally the differential-mode voltage gain of the op amp)

$F(s)$ = transfer function of the external feedback from the output of the op amp back to the input.

Definitions:

- Open-loop gain = $L(s) = -A(s)F(s)$
- Closed-loop gain = $\dfrac{V_{out}(s)}{V_{in}(s)} = \dfrac{A(s)}{1+A(s)F(s)}$

Stability Requirements:

The requirements for stability for a single-loop, negative feedback system is,

$$|A(j\omega_{0°})F(j\omega_{0°})| = |L(j\omega_{0°})| < 1$$

where $\omega_{0°}$ is defined as

$$\text{Arg}[-A(j\omega_{0°})F(j\omega_{0°})] = \text{Arg}[L(j\omega_{0°})] = 0°$$

Another convenient way to express this requirement is

$$\text{Arg}[-A(j\omega_{0dB})F(j\omega_{0dB})] = \text{Arg}[L(j\omega_{0dB})] > 0°$$

where ω_{0dB} is defined as

$$|A(j\omega_{0dB})F(j\omega_{0dB})| = |L(j\omega_{0dB})| = 1$$

Illustration of the Stability Requirement using Bode Plots

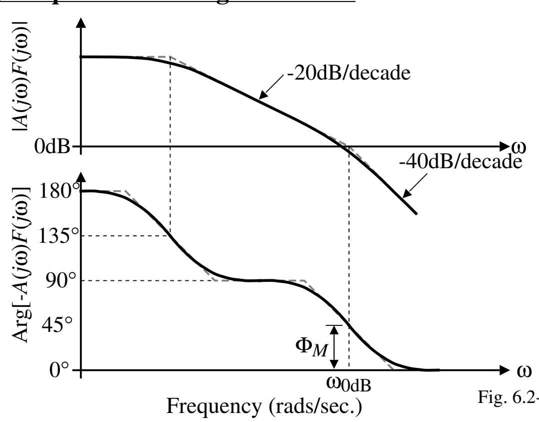


Fig. 6.2-2

A measure of stability is given by the phase when $|A(j\omega)F(j\omega)| = 1$. This phase is called *phase margin*.

$$\text{Phase margin} = \Phi_M = \text{Arg}[-A(j\omega_{0dB})F(j\omega_{0dB})] = \text{Arg}[L(j\omega_{0dB})]$$

Why Do We Want Good Stability?

Consider the step response of second-order system which closely models the closed-loop gain of the op amp.

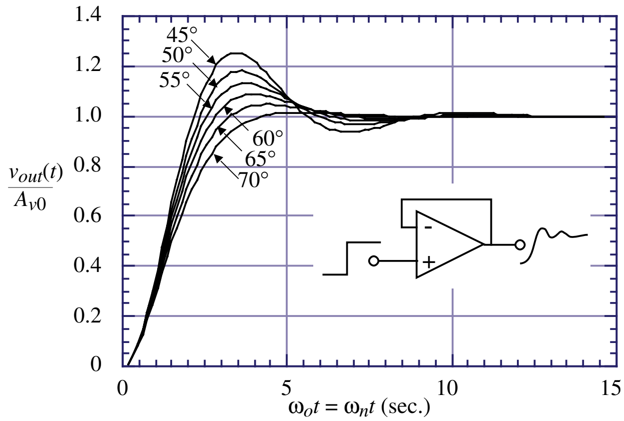


Fig. 6.2-3

A "good" step response is one that quickly reaches its final value.

Therefore, we see that phase margin should be at least 45° and preferably 60° or larger.

(A good rule of thumb for satisfactory stability is that there should be less than three rings.)

Note that good stability is not necessarily the quickest risetime.

The Frequency Response of the Two-Stage Op Amp

Without any compensation, the two-stage op amp can be modeled as shown below.

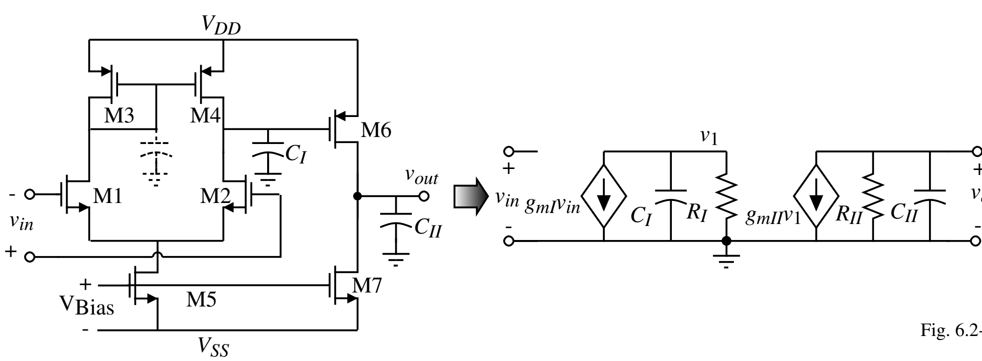


Fig. 6.2-4

The locations for the two poles are given by the following equations

$$p'_1 = \frac{-1}{R_I C_I}$$

and

$$p'_2 = \frac{-1}{R_{II} C_{II}}$$

where R_I (R_{II}) is the resistance to ground seen from the output of the first (second) stage and C_I (C_{II}) is the capacitance to ground seen from the output of the first (second) stage.

Frequency Response of the Op Amp

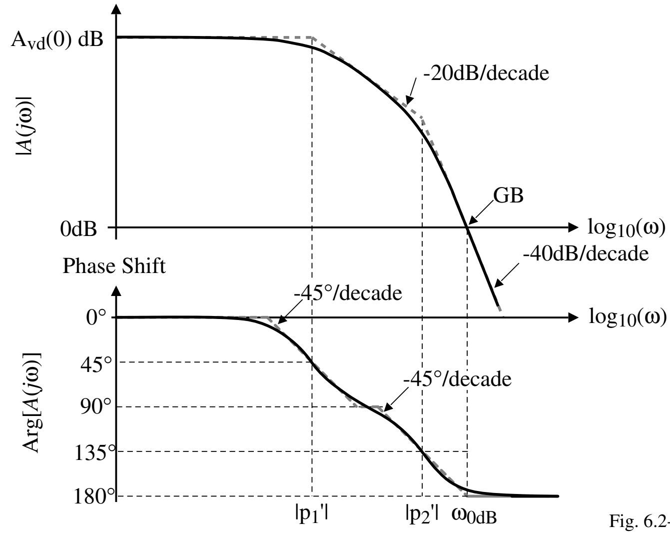


Fig. 6.2-5

Note that the op amp experiences 180° phase shift which will cause poor phase margin in a negative feedback application.

Loop Gain of an Uncompensated Op Amp with Negative Feedback of $F(s) = 1$ [$L(s) = -A(s)$]

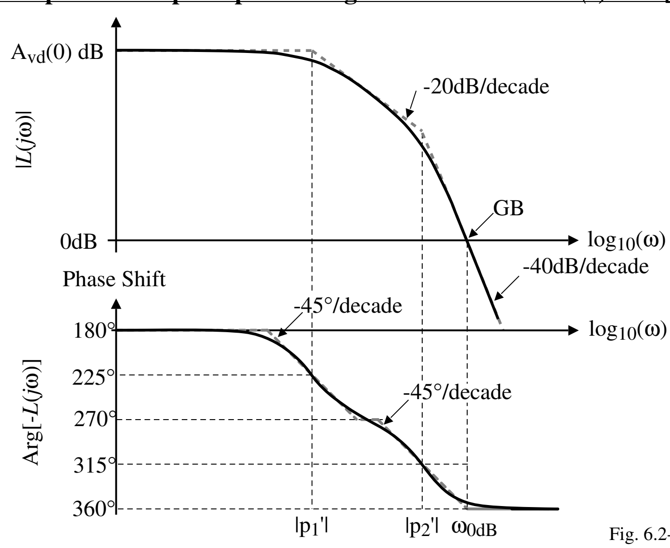


Fig. 6.2-5

Note that the phase margin is much less than 45°.

Therefore, the op amp must be compensated before using it in a closed-loop configuration.

Miller Compensation of the Two-Stage Op Amp

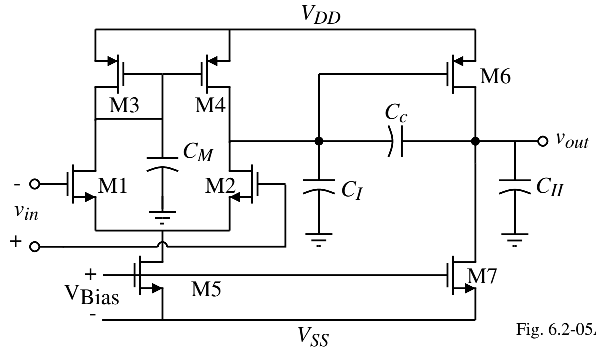


Fig. 6.2-05A

The various capacitors are:

C_c = accomplishes the Miller compensation

C_M = capacitance associated with the first-stage mirror (mirror pole)

C_I = output capacitance to ground of the first-stage

C_{II} = output capacitance to ground of the second-stage

Simplification of the Two-Stage, Small-Signal Frequency Response Model

1.) Assume that $g_{m3} >> g_{ds3} + g_{ds1}$.

2.) Assume that $\frac{g_{m3}}{C_M} >> GB$

Therefore,

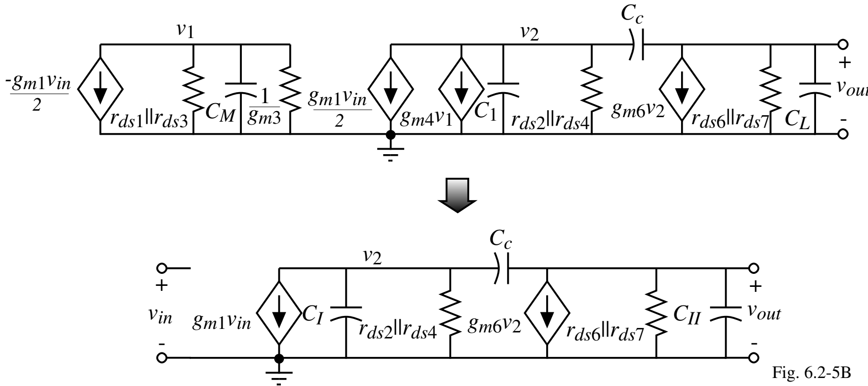


Fig. 6.2-5B

General Two-Stage Frequency Response Analysis

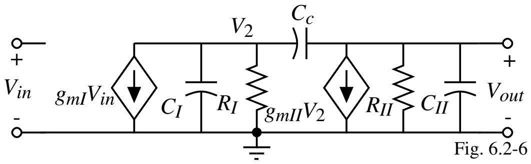


Fig. 6.2-6

where

$$g_{mI} = g_{m1} = g_{m2},\ R_I = r_{ds2}||r_{ds4},\ C_I = C_1$$

and

$$g_{mII} = g_{m6},\ R_{II} = r_{ds6}||r_{ds7},\ C_{II} = C_2 = C_L$$

Nodal Equations:

$$-g_{mI}V_{in} = [G_I + s(C_I + C_c)]V_2 - [sC_c]V_{out} \quad \text{and} \quad 0 = [g_{mII} - sC_c]V_2 + [G_{II} + sC_{II} + sC_c]V_{out}$$

Solving using Cramer's rule gives,

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{g_{mI}(g_{mII} - sC_c)}{G_IG_{II}+s\,[G_{II}(C_I+C_{II})+G_I(C_{II}+C_c)+g_{mII}C_c]+s^2[C_IC_{II}+C_cC_I+C_cC_{II}]}$$

$$= \frac{A_o[1 - s\,(C_c/g_{mII})]}{1+s\,[R_I(C_I+C_{II})+R_{II}(C_2+C_c)+g_{mII}R_IR_{II}C_c]+s^2[R_IR_{II}(C_IC_{II}+C_cC_I+C_cC_{II})]}$$

where, $A_o = g_{mI}g_{mII}R_IR_{II}$

In general, $D(s) = \left(1 - \frac{s}{p_1}\right)\left(1 - \frac{s}{p_2}\right) = 1 - s\left(\frac{1}{p_1} + \frac{1}{p_2}\right) + \frac{s^2}{p_1p_2} \quad \rightarrow \quad D(s) \approx 1 - \frac{s}{p_1} + \frac{s^2}{p_1p_2}$, if $|p_2|>>|p_1|$

$$\therefore \quad \boxed{p_1 = \frac{-1}{R_I(C_I+C_{II})+R_{II}(C_{II}+C_c)+g_{mII}R_IR_{II}C_c} \approx \frac{-1}{g_{mII}R_IR_{II}C_c}}, \quad \boxed{z = \frac{g_{mII}}{C_c}}$$

$$\boxed{p_2 = \frac{-[R_I(C_I+C_{II})+R_{II}(C_{II}+C_c)+g_{mII}R_IR_{II}C_c]}{R_IR_{II}(C_IC_{II}+C_cC_I+C_cC_{II})} \approx \frac{-g_{mII}C_c}{C_IC_{II}+C_cC_I+C_cC_{II}} \approx \frac{-g_{mII}}{C_{II}}}$$

where $C_{II} > C_c > C_I$.

Summary of Results for Miller Compensation of the Two-Stage Op Amp

There are three roots of importance:

1.) Right-half plane zero:

$$z = \frac{g_{mII}}{C_c} = \frac{g_{m6}}{C_c}$$

This root is very undesirable because it boosts the loop magnitude while decreasing the phase.

2.) Dominant left-half plane pole (the Miller pole):

$$p_1 \approx \frac{-1}{g_{mII}R_IR_{II}C_c} = \frac{-(g_{ds2}+g_{ds4})(g_{ds6}+g_{ds7})}{g_{m6}C_c}$$

This root accomplishes the desired compensation.

3.) Left-half plane output pole:

$$p_2 \approx \frac{-g_{mII}}{C_{II}} \approx \frac{-g_{m6}}{C_L}$$

This pole must be beyond the unity-gainbandwidth or the phase margin will not be satisfied.

Root locus plot of the Miller compensation:

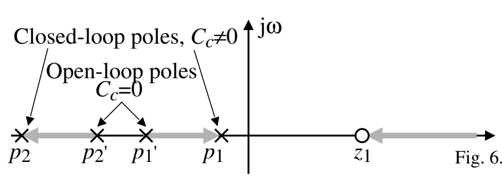


Fig. 6.2-7A

Compensated Open-Loop Frequency Response of the Two-Stage Op Amp

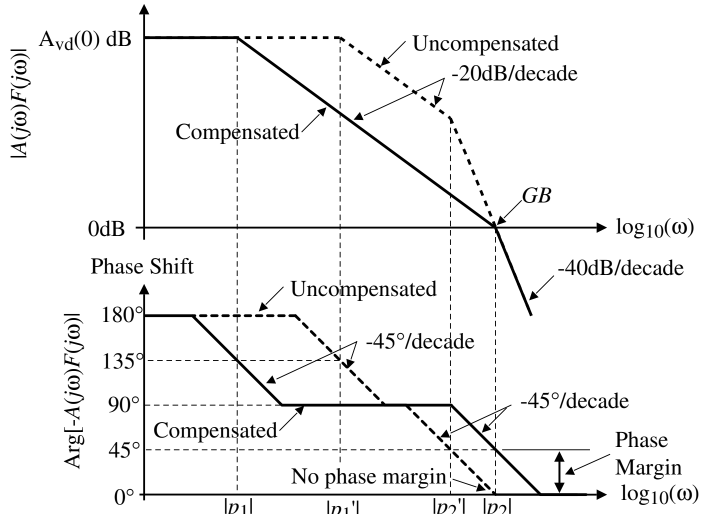


Fig. 6.2-7B

Note that the unity-gainbandwidth, *GB*, is

$$GB = A_{vd}(0)\cdot|p_1| = (g_{mI}g_{mII}R_IR_{II})\frac{1}{g_{mII}R_IR_{II}C_c} = \frac{g_{mI}}{C_c} = \frac{g_{m1}}{C_c} = \frac{g_{m2}}{C_c}$$

Conceptually, where do these roots come from?

1.) The Miller pole:

$$|p_1| \approx \frac{1}{R_I(g_{m6}R_{II}C_c)}$$

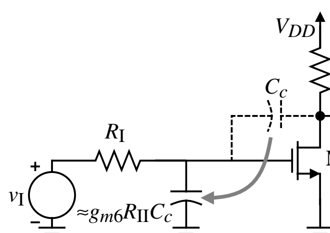


Fig. 6.2-9

2.) The left-half plane output pole:

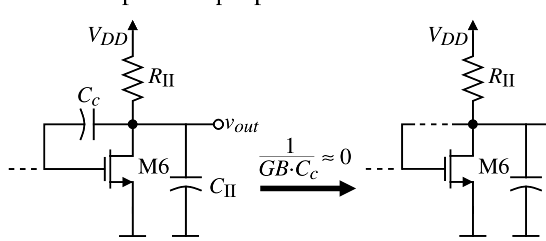


Fig. 6.2-10

$$|p_2| \approx \frac{g_{m6}}{C_{II}}$$

3.) Right-half plane zero (*Zeros always arise from multiple paths from the input to output*):

$$v_{out} = \left(\frac{-g_{m6}R_{II}(1/sC_c)}{R_{II} + 1/sC_c}\right)v' + \left(\frac{R_{II}}{R_{II} + 1/sC_c}\right)v'' = \frac{-R_{II}\left(\frac{g_{m6}}{sC_c} - 1\right)}{D(s)}v$$

where $v = v' = v''$.

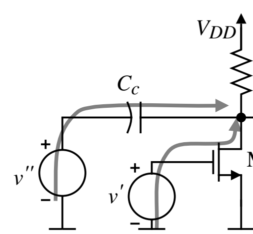


Fig. 6.2-11

Influence of the Mirror Pole

Up to this point, we have neglected the influence of the pole, p_3, associated with the current mirror of the input stage. If $|p_2| \approx |p_3|$, we have problems in compensation. This pole is given approximately as

$$p_3 \approx \frac{-g_{m3}}{C_M}$$

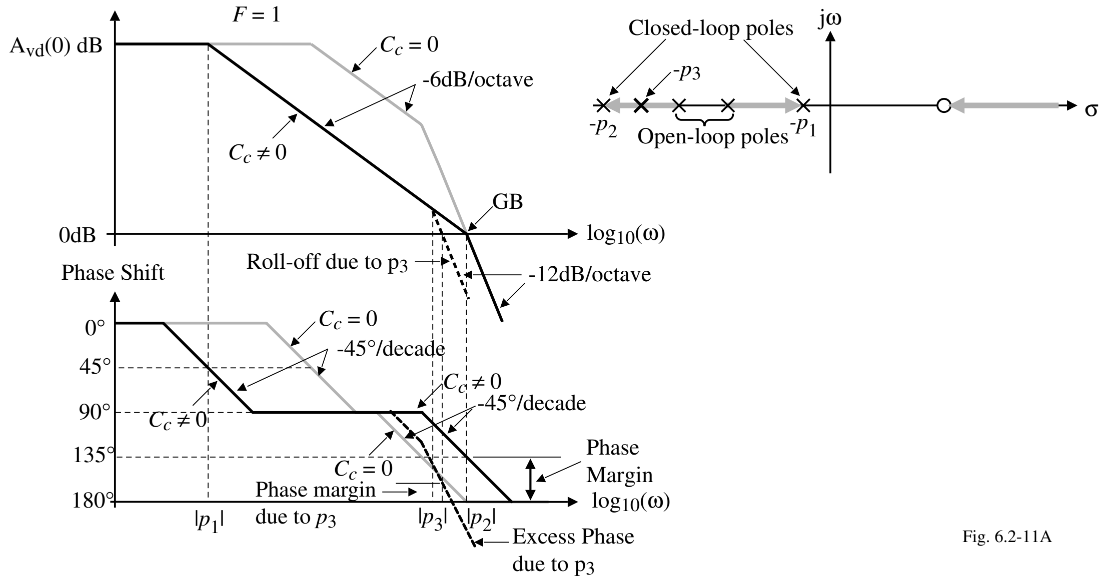


Fig. 6.2-11A

Summary of the Conditions for Stability of the Two-Stage Op Amp

• Unity-gainbandwith is given as:

$$GB = A_v(0)\cdot|p_1| = (g_{mI}g_{mII}R_IR_{II})\cdot\left(\frac{1}{g_{mII}R_IR_{II}C_c}\right) = \frac{g_{mI}}{C_c} = (g_{m1}g_{m2}R_1R_2)\cdot\left(\frac{1}{g_{m2}R_1R_2C_c}\right) = \frac{g_{m1}}{C_c}$$

• The requirement for 45° phase margin is:

$$\pm 180° - \text{Arg}[AF] = \pm 180° - \tan^{-1}\left(\frac{\omega}{|p_1|}\right) - \tan^{-1}\left(\frac{\omega}{|p_2|}\right) - \tan^{-1}\left(\frac{\omega}{z}\right) = 45°$$

Let $\omega = GB$ and assume that $z \geq 10GB$, therefore we get,

$$\pm 180° - \tan^{-1}\left(\frac{GB}{|p_1|}\right) - \tan^{-1}\left(\frac{GB}{|p_2|}\right) - \tan^{-1}\left(\frac{GB}{z}\right) = 45°$$

$$135° \approx \tan^{-1}(A_v(0)) + \tan^{-1}\left(\frac{GB}{|p_2|}\right) + \tan^{-1}(0.1) = 90° + \tan^{-1}\left(\frac{GB}{|p_2|}\right) + 5.7°$$

$$39.3° \approx \tan^{-1}\left(\frac{GB}{|p_2|}\right) \Rightarrow \frac{GB}{|p_2|} = 0.818 \Rightarrow \boxed{|p_2| \geq 1.22GB}$$

• The requirement for 60° phase margin:

$$\boxed{|p_2| \geq 2.2GB \text{ if } z \geq 10GB}$$

• If 60° phase margin is required, then the following relationships apply:

$$\frac{g_{m6}}{C_c} > \frac{10g_{m1}}{C_c} \Rightarrow \boxed{g_{m6} > 10g_{m1}} \qquad \text{and} \qquad \frac{g_{m6}}{C_2} > \frac{2.2g_{m1}}{C_c} \Rightarrow \boxed{C_c > 0.22C_2}$$

Controlling the Right-Half Plane Zero

Why is the RHP zero a problem?

Because it boosts the magnitude but lags the phase - the worst possible combination for stability.

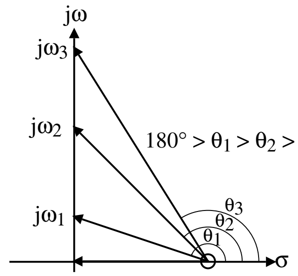


Fig. 6.2-11B

Solution of the problem:

If zeros are caused by two paths to the output, then eliminate one of the paths.

Use of Buffer to Eliminate the Feedforward Path through the Miller Capacitor

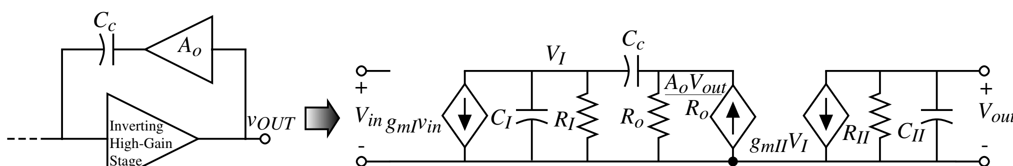


Fig. 6.2-12

If R_o of the buffer is zero, then the transfer function is given by the following equation,

$$\frac{V_o(s)}{V_{\text{in}}(s)} = \frac{(g_{mI})(g_{mII})(R_I)(R_{II})}{1 + s[R_IC_I + R_{II}C_{II} + R_IC_c + g_{mII}R_IR_{II}C_c] + s^2[R_IR_{II}C_{II}(C_I + C_c)]}$$

Using the technique as before to approximate p_1 and p_2 results in the following

$$p_1 \cong \frac{-1}{R_IC_I + R_{II}C_{II} + R_IC_c + g_{mII}R_IR_{II}C_c} \cong \frac{-1}{g_{mII}R_IR_{II}C_c}$$

and

$$p_2 \cong \frac{-g_{mII}C_c}{C_{II}(C_I + C_c)}$$

Comments:

Poles are approximately what they were before with the zero removed.

For 45° phase margin, $|p_2|$ must be greater than GB

For 60° phase margin, $|p_2|$ must be greater than $1.73GB$

Use of Buffer with Finite Output Resistance to Eliminate the RHP Zero

It can be shown that if the output resistance of the buffer amplifier, R_o, is not neglected that a third pole occurs at,

$$p_4 \cong \frac{-1}{R_o[C_I C_c/(C_I + C_c)]}$$

and a LHP zero at

$$z_2 \cong \frac{-1}{R_o C_c}$$

Closer examination shows that if a resistor, called a *nulling resistor*, is placed in series with C_c that the RHP zero can be eliminated or moved to the LHP.

Use of Nulling Resistor to Eliminate the RHP Zero (or turn it into a LHP zero)[†]

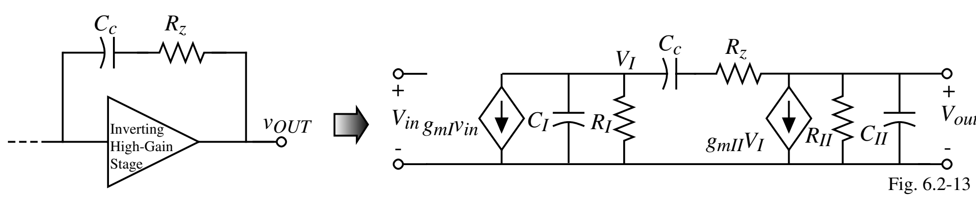


Fig. 6.2-13

Nodal equations:

$$g_{mI}V_{\text{in}} + \frac{V_I}{R_I} + sC_I V_I + \left(\frac{sC_c}{1 + sC_c R_z}\right)(V_I - V_{out}) = 0$$

$$g_{mII}V_I + \frac{V_o}{R_{II}} + sC_{II}V_{out} + \left(\frac{sC_c}{1 + sC_c R_z}\right)(V_{out} - V_I) = 0$$

Solution:

$$\frac{V_{out}(s)}{V_{\text{in}}(s)} = \frac{a\{1 - s[(C_c/g_{mII}) - R_z C_c]\}}{1 + bs + cs^2 + ds^3}$$

where

$$a = g_{mI}g_{mII}R_I R_{II}$$
$$b = (C_{II} + C_c)R_{II} + (C_I + C_c)R_I + g_{mII}R_I R_{II}C_c + R_z C_c$$
$$c = [R_I R_{II}(C_I C_{II} + C_c C_I + C_c C_{II}) + R_z C_c(R_I C_I + R_{II}C_{II})]$$
$$d = R_I R_{II} R_z C_I C_{II} C_c$$

† William J. Parrish, "An Ion Implanted CMOS Amplifier for High Performance Active Filters", Ph.D. Dissertation, 1976, Univ. of Calif., Santa Barbara, CA.

Use of Nulling Resistor to Eliminate the RHP - Continued

If R_z is assumed to be less than R_I or R_{II} and the poles widely spaced, then the roots of the above transfer function can be approximated as

$$p_1 \cong \frac{-1}{(1+g_{mII}R_{II})R_IC_c} \cong \frac{-1}{g_{mII}R_{II}R_IC_c}$$

$$p_2 \cong \frac{-g_{mII}C_c}{C_IC_{II}+C_cC_I+C_cC_{II}} \cong \frac{-g_{mII}}{C_{II}}$$

$$p_4 = \frac{-1}{R_zC_I}$$

and

$$z_1 = \frac{1}{C_c(1/g_{mII} - R_z)}$$

Note that the zero can be placed anywhere on the real axis.

Conceptual Illustration of the Nulling Resistor Approach

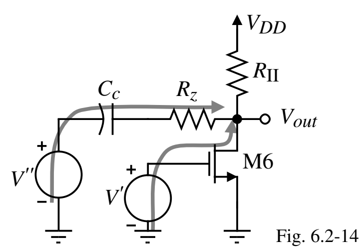


Fig. 6.2-14

The output voltage, V_{out}, can be written as

$$V_{out} = \frac{-g_{m6}R_{II}\left(R_z + \frac{1}{sC_c}\right)}{R_{II}+R_z+\frac{1}{sC_c}}V' + \frac{R_{II}}{R_{II}+R_z+\frac{1}{sC_c}}V'' = \frac{-R_{II}\left[g_{m6}R_z + \frac{g_{m6}}{sC_c} - 1\right]}{D(s)}$$

Setting the numerator equal to zero and assuming $g_{m6} = g_{mII}$ gives,

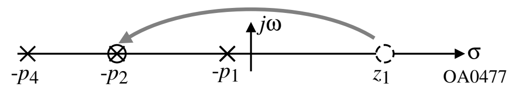
$$z_1 = \frac{1}{C_c(1/g_{mII} - R_z)}$$

A Design Procedure that Allows the RHP Zero to Cancel the Output Pole, p_2

We desire that $z_1 = p_2$ in terms of the previous notation.

Therefore,

$$\frac{1}{C_c(1/g_{mII} - R_z)} = \frac{-g_{mII}}{C_{II}}$$



The value of R_z can be found as

$$R_z = \left(\frac{C_c + C_{II}}{C_c}\right)(1/g_{mII})$$

With p_2 canceled, the remaining roots are p_1 and p_4(the pole due to R_z) . For unity-gain stability, all that is required is that

$$|p_4| > A_v(0)|p_1| = \frac{A_v(0)}{g_{mII}R_{II}R_I C_c} = \frac{g_{mI}}{C_c}$$

and

$$(1/R_z C_I) > (g_{mI}/C_c) = GB$$

Substituting R_z into the above inequality and assuming $C_{II} >> C_c$ results in

$$C_c > \sqrt{\frac{g_{mI}}{g_{mII}} C_I C_{II}}$$

This procedure gives excellent stability for a fixed value of C_{II} ($\approx C_L$).

Unfortunately, as C_L changes, p_2 changes and the zero must be readjusted to cancel p_2.

Increasing the Magnitude of the Output Pole†

The magnitude of the output pole , p_2, can be increased by introducing gain in the Miller capacitor feedback path. For example,

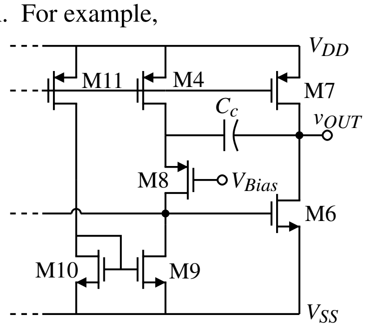
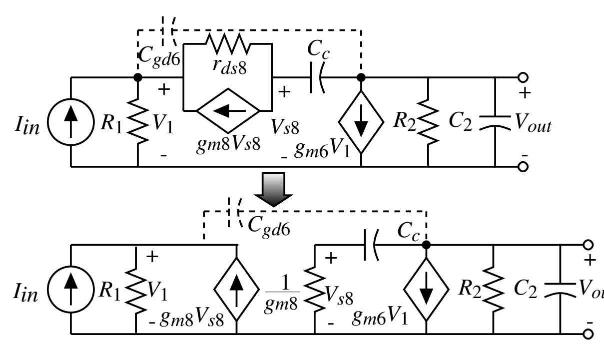


Fig. 6.2-15B



The resistors R_1 and R_2 are defined as

$$R_1 = \frac{1}{g_{ds2} + g_{ds4} + g_{ds9}} \quad \text{and} \quad R_2 = \frac{1}{g_{ds6} + g_{ds7}}$$

where transistors M2 and M4 are the output transistors of the first stage.

Nodal equations:

$$I_{in} = G_1V_1 - g_{m8}V_{s8} = G_1V_1 - \left(\frac{g_{m8}sC_c}{g_{m8} + sC_c}\right)V_{out} \quad \text{and} \quad 0 = g_{m6}V_1 + \left[G_2 + sC_2 + \frac{g_{m8}sC_c}{g_{m8} + sC_c}\right]V_{out}$$

† B.K. Ahuja, "An Improved Frequency Compensation Technique for CMOS Operational Amplifiers," *IEEE J. of Solid-State Circuits*, Vol. SC-18, No. 6 (Dec. 1983) pp. 629-633.

Increasing the Magnitude of the Output Pole - Continued

Solving for the transfer function V_{out}/I_{in} gives,

$$\frac{V_{out}}{I_{in}} = \left(\frac{-g_{m6}}{G_1G_2}\right)\left[\frac{\left(1+\frac{sC_c}{g_{m8}}\right)}{1+s\left[\frac{C_c}{g_{m8}}+\frac{C_2}{G_2}+\frac{C_c}{G_2}+\frac{g_{m6}C_c}{G_1G_2}\right]+s^2\left(\frac{C_cC_2}{g_{m8}G_2}\right)}\right]$$

Using the approximate method of solving for the roots of the denominator illustrated earlier gives

$$p_1 = \frac{-1}{\frac{C_c}{g_{m8}}+\frac{C_c}{G_2}+\frac{C_2}{G_2}+\frac{g_{m6}C_c}{G_1G_2}} \approx \frac{-6}{g_{m6}r_{ds}{}^2C_c}$$

and

$$p_2 \approx \frac{-\frac{g_{m6}r_{ds}{}^2C_c}{6}}{\frac{C_cC_2}{g_{m8}G_2}} = \frac{g_{m8}r_{ds}{}^2G_2}{6}\left(\frac{g_{m6}}{C_2}\right) = \left(\frac{g_{m8}r_{ds}}{3}\right)|p_2'|$$

where all the various channel resistance have been assumed to equal r_{ds} and p_2' is the output pole for normal Miller compensation.

Result:

Dominant pole is approximately the same and the output pole is increased by roughly g_mr_{ds}.

Increasing the Magnitude of the Output Pole - Continued

In addition there is a LHP zero at $-g_{m8}/sC_c$ and a RHP zero due to C_{gd6} (shown dashed in the model on Page 6.2-23) at g_{m6}/C_{gd6}.

Roots are:

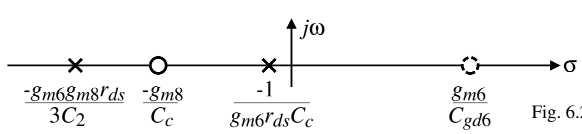


Fig. 6.2-16A

Concept Behind the Increasing of the Magnitude of the Output Pole

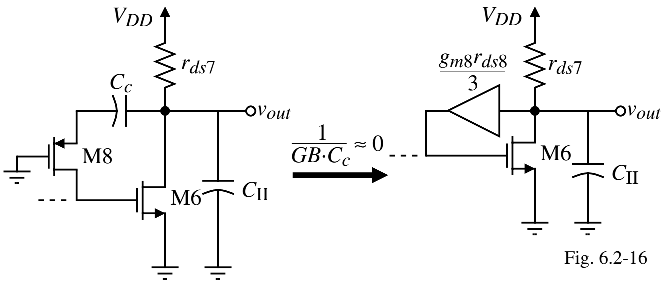


Fig. 6.2-16

$$R_{out} = r_{ds7} || \left(\frac{3}{g_{m6}g_{m8}r_{ds8}}\right) \approx \frac{3}{g_{m6}g_{m8}r_{ds8}}$$

Therefore, the output pole is approximately,

$$|p_2| \approx \frac{g_{m6}g_{m8}r_{ds8}}{3C_{II}}$$

Feedforward Compensation

Use two parallel paths to achieve a LHP zero for lead compensation purposes.

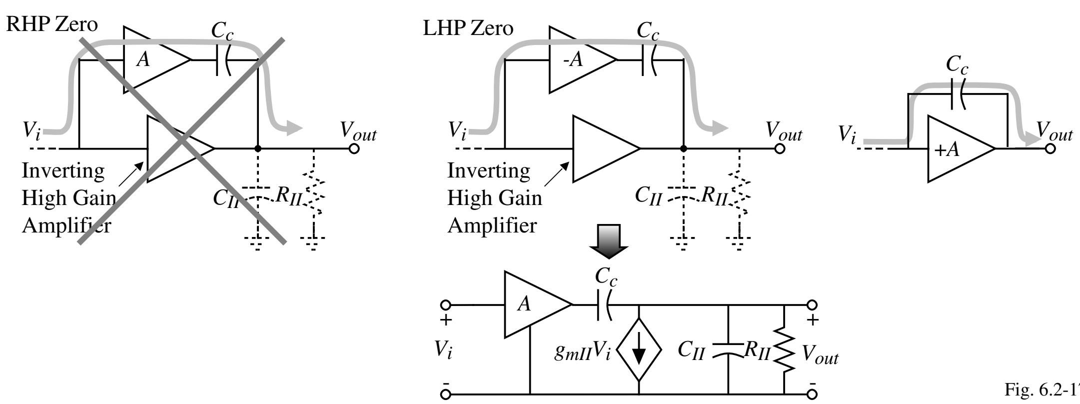


Fig. 6.2-17

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{AC_c}{C_c + C_{II}}\left(\frac{s + g_{mII}/AC_c}{s + 1/[R_{II}(C_c + C_{II})]}\right)$$

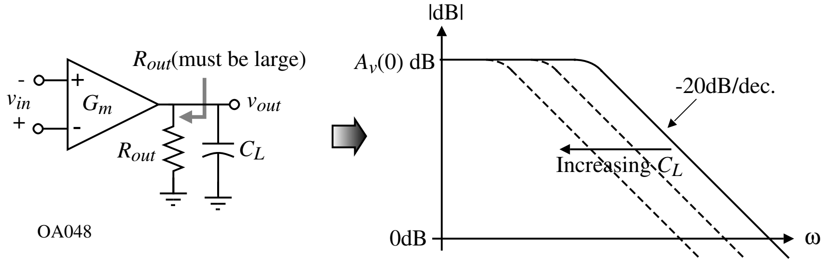
To use the LHP zero for compensation, a compromise must be observed.

- Placing the zero below *GB* will lead to boosting of the loop gain which could deteriorate the phase margin.
- Placing the zero above *GB* will have less influence on the leading phase caused by the zero.

Note that a source follower is a good candidate for the use of feedforward.

Self-Compensated Op Amps

Self compensation occurs when the load capacitor is the compensation capacitor (can never be unstable for resistive feedback)



Voltage gain:

$$\frac{v_{out}}{v_{in}} = A_v(0) = G_m R_{out}$$

Dominant pole:

$$p_1 = \frac{-1}{R_{out}C_L}$$

Unity-gainbandwidth:

$$GB = A_v(0)\cdot|p_1| = \frac{G_m}{C_L}$$

Stability:

Large load capacitors simply reduce the GB and the phase is 90° at the unity gain frequency

Slew Rate of a Two-Stage Op Amp

Remember that slew rate occurs when currents flowing in a capacitor become limited and is given as

$$I_{lim} = C\frac{dv_C}{dt}$$ where v_C is the voltage across the capacitor C.

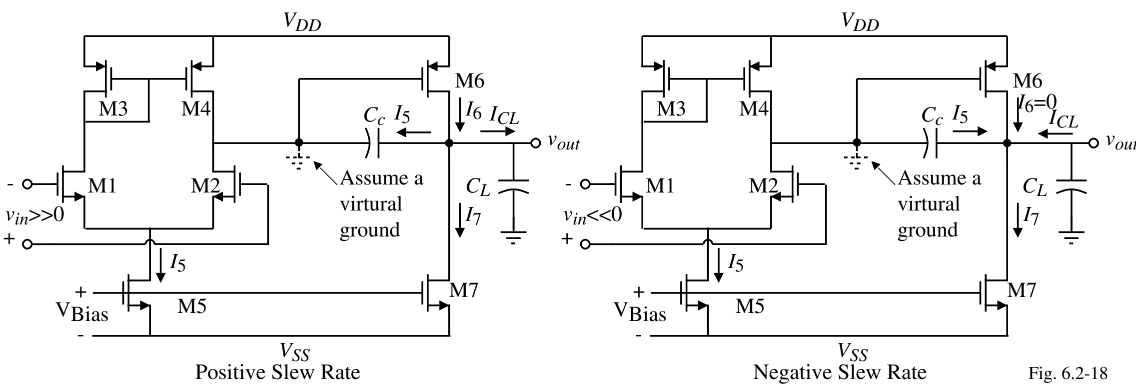


Fig. 6.2-18

$$SR^+ = \min\left[\frac{I_5}{C_c}, \frac{I_6-I_5-I_7}{C_L}\right] = \frac{I_5}{C_c} \text{ because } I_6>>I_5 \qquad SR^- = \min\left[\frac{I_5}{C_c}, \frac{I_7-I_5}{C_L}\right] = \frac{I_5}{C_c} \text{ if } I_7>>I_5.$$

Therefore, if C_L is not too large and if I_7 is significantly greater than I_5, then the slew rate of the two-stage op amp should be,

$$SR = \frac{I_5}{C_c}$$

SECTION 6.3 - TWO-STAGE OP AMP DESIGN

Unbuffered, Two-Stage CMOS Op Amp

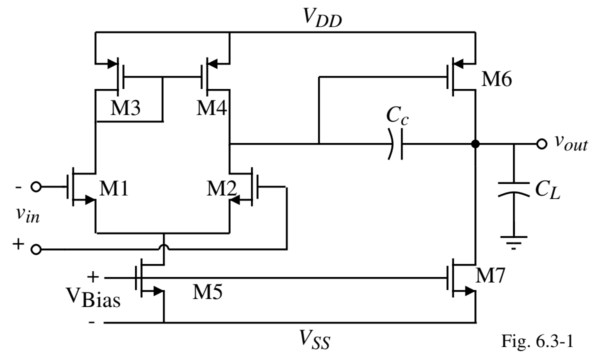


Fig. 6.3-1

Notation:

$$S_i = \frac{W_i}{L_i} = W/L \text{ of the ith transistor}$$

DC Balance Conditions for the Two-Stage Op Amp

For best performance, keep all transistors in saturation.

M4 is the only transistor that cannot be forced into saturation by internal connections or external voltages.

Therefore, we develop conditions to force M4 to be in saturation.

1.) First *assume* that $V_{SG4} = V_{SG6}$. This will cause "proper mirroring" in the M3-M4 mirror. Also, the gate and drain of M4 are at the same potential so that M4 is "guaranteed" to be in saturation.

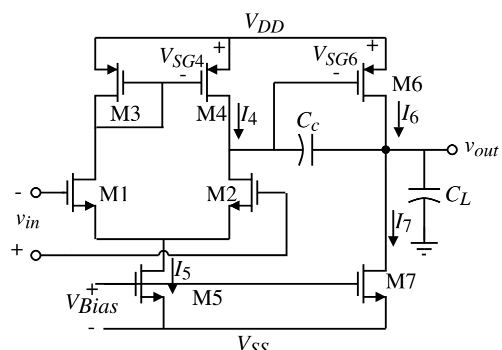


Fig. 6.3-1A

2.) *If* $V_{SG4} = V_{SG6}$, then $I_6 = \left(\frac{S_6}{S_4}\right)I_4$

3.) However, $I_7 = \left(\frac{S_7}{S_5}\right)I_5 = \left(\frac{S_7}{S_5}\right)(2I_4)$

4.) For balance, I_6 must equal I_7 $\Rightarrow$ $\boxed{\frac{S_6}{S_4} = \frac{2S_7}{S_5}}$ which is called the "balance conditions"

5.) So if the balance conditions are satisfied, then $V_{DG4} = 0$ and M4 is saturated.

Design Relationships for the Two-Stage Op Amp

Slew rate $SR = \frac{I_5}{C_c}$ (Assuming $I_7 >> I_5$ and $C_L > C_c$)

First-stage gain $A_{v1} = \frac{g_{m1}}{g_{ds2} + g_{ds4}} = \frac{2g_{m1}}{I_5(\lambda_2 + \lambda_4)}$

Second-stage gain $A_{v2} = \frac{g_{m6}}{g_{ds6} + g_{ds7}} = \frac{g_{m6}}{I_6(\lambda_6 + \lambda_7)}$

Gain-bandwidth $GB = \frac{g_{m1}}{C_c}$

Output pole $p_2 = \frac{-g_{m6}}{C_L}$

RHP zero $z_1 = \frac{g_{m6}}{C_c}$

60° phase margin requires that $g_{m6} = 2.2g_{m2}(C_L/C_c)$ if all other roots are $\geq 10GB$.

Positive ICMR $V_{in(max)} = V_{DD} - \sqrt{\frac{I_5}{\beta_3}} - |V_{T03}|_{(max)} + V_{T1(min)})$

Negative ICMR $V_{in(min)} = V_{SS} + \sqrt{\frac{I_5}{\beta_1}} + V_{T1(max)} + V_{DS5}(sat)$

Saturation voltage $V_{DS}(sat) = \sqrt{\frac{2I_{DS}}{\beta}}$

It is assumed that all transistors are in saturation for the above relationships.

Op Amp Specifications

The following design procedure assumes that specifications for the following parameters are given.

1. Gain at dc, $A_v(0)$
2. Gain-bandwidth, GB
3. Phase margin (or settling time)
4. Input common-mode range, ICMR
5. Load Capacitance, C_L
6. Slew-rate, SR
7. Output voltage swing
8. Power dissipation, P_{diss}

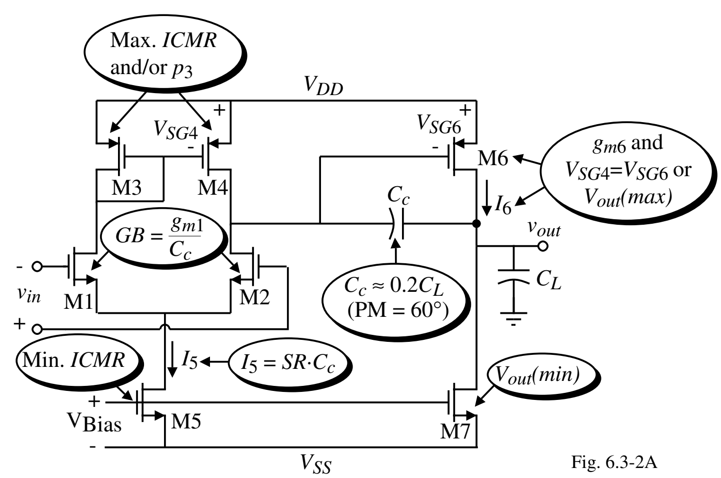


Fig. 6.3-2A

Unbuffered Op Amp Design Procedure

This design procedure assumes that the gain at dc (A_v), unity gain bandwidth (GB), input common mode range (V_{in}(min) and V_{in}(max)), load capacitance (C_L), slew rate (SR), settling time (T_s), output voltage swing (V_{out}(max) and V_{out}(min)), and power dissipation (P_{diss}) are given. Choose the smallest device length which will keep the channel modulation parameter constant and give good matching for current mirrors.

1. From the desired phase margin, choose the minimum value for C_c, i.e. for a 60° phase margin we use the following relationship. This assumes that $z \geq 10GB$.

$$C_c > 0.22C_L$$

2. Determine the minimum value for the "tail current" (I_5) from the largest of the two values.

$$I_5 = SR \cdot C_c \qquad \text{or} \qquad I_5 \cong 10\left(\frac{V_{DD} + |V_{SS}|}{2 \cdot T_s}\right)$$

3. Design for S_3 from the maximum input voltage specification.

$$S_3 = \frac{2I_3}{K'_3[V_{DD} - V_{in}(\text{max}) - |V_{T03}|(\text{max}) + V_{T1}(\text{min})]^2} \geq 1$$

4. Verify that the pole of M3 due to C_{gs3} and C_{gs4} (=0.67$W_3L_3C_{ox}$) will not be dominant by assuming it to be greater than 10 GB

$$\frac{g_{m3}}{2C_{gs3}} > 10GB.$$

5. Design for S_1 (S_2) to achieve the desired GB.

$$g_{m1} = GB \cdot C_c \Rightarrow S_1 = S_2 = \frac{g_{m1}}{K'_1 I_5}$$

Unbuffered Op Amp Design Procedure - Continued

6. Design for S_5 from the minimum input voltage. First calculate V_{DS5}(sat) then find S_5.

$$V_{DS5}(\text{sat}) = V_{in}(\text{min}) - V_{SS} - \sqrt{\frac{I_5}{\beta_1}} - V_{T1}(\text{max}) \geq 100\text{ mV} \;\rightarrow\; S_5 = \frac{2I_5}{K'_5[V_{DS5}(\text{sat})]^2}$$

7. Find S_6 by letting the second pole (p_2) be equal to 2.2 times GB and assuming that $V_{SG4} = V_{SG6}$.

$$g_{m6} = 2.2g_{m2}(C_L/C_c) \quad \rightarrow \quad S_6 = S_4\frac{g_{m6}}{g_{m4}}$$

8. Calculate I_6 from

$$I_6 = \frac{g_{m6}^2}{2K'_6 S_6}$$

Check to make sure that S_6 satisfies the V_{out}(max) requirement and adjust as necessary.

9. Design S_7 to achieve the desired current ratios between I_5 and I_6.

$$S_7 = (I_6/I_5)S_5$$ (Check the minimum output voltage requirements)

10. Check gain and power dissipation specifications.

$$A_v = \frac{2g_{m2}g_{m6}}{I_5(\lambda_2 + \lambda_3)I_6(\lambda_6 + \lambda_7)} \qquad P_{diss} = (I_5 + I_6)(V_{DD} + |V_{SS}|)$$

11. If the gain specification is not met, then the currents, I_5 and I_6, can be decreased or the W/L ratios of M2 and/or M6 increased. The previous calculations must be rechecked to insure that they are satisfied. If the power dissipation is too high, then one can only reduce the currents I_5 and I_6. Reduction of currents will probably necessitate increase of some of the W/L ratios in order to satisfy input and output swings.

12. Simulate the circuit to check to see that all specifications are met.

Example 6.3-1 - Design of a Two-Stage Op Amp

Using the material and device parameters given in Tables 3.1-2 and 3.2-1, design an amplifier similar to that shown in Fig. 6.3-1 that meets the following specifications. Assume the channel length is to be 1µm.

$A_v > 5000$V/V	$V_{DD} = 2.5$V	$V_{SS} = -2.5$V 60° phase margin
$GB = 5$MHz	$C_L = 10$pF	$SR > 10$V/µs
V_{out} range = ±2V	$ICMR = -1$ to 2V	$P_{diss} \le 2$mW

Solution

1.) The first step is to calculate the minimum value of the compensation capacitor C_c, which is

$$C_c > (2.2/10)(10\text{ pF}) = 2.2\text{ pF}$$

2.) Choose C_c as 3pF. Using the slew-rate specification and C_c calculate I_5.

$$I_5 = (3\text{x}10^{-12})(10 \text{ x } 10^6) = 30\ \mu\text{A}$$

3.) Next calculate $(W/L)_3$ using ICMR requirements.

$$(W/L)_3 = \frac{30 \text{ x } 10^{-6}}{(50\text{x}10^{-6})[2.5 - 2 - 0.85 + 0.55]^2} = 15 \quad \rightarrow \quad \boxed{(W/L)_3 = (W/L)_4 = 15}$$

4.) Now we can check the value of the mirror pole, p_3, to make sure that it is in fact greater than 10*GB*. Assume the $C_{ox} = 0.4\text{fF}/\mu\text{m}^2$. The mirror pole can be found as

$$p_3 \approx \frac{-g_{m3}}{2C_{gs3}} = \frac{-\sqrt{2K'_pS_3I_3}}{2(0.667)W_3L_3C_{ox}} = 2.81\text{x}10^9\text{(rads/sec)}$$

or 448 MHz. Thus, p_3, is not of concern in this design because $p_3 >> 10GB$.

Example 6.3-1 - Continued

5.) The next step in the design is to calculate g_{m1} to get

$$g_{m1} = (5\text{x}10^6)(2\pi)(3\text{x}10^{-12}) = 94.25\mu\text{S}$$

Therefore, $(W/L)_1$ is

$$(W/L)_1 = (W/L)_2 = \frac{g_{m1}{}^2}{2K'_NI_1} = \frac{(94.25)^2}{2\cdot 110\cdot 15} = 2.79 \approx 3.0 \Rightarrow \quad \boxed{(W/L)_1 = (W/L)_2 = 3}$$

6.) Next calculate V_{DS5},

$$V_{DS5} = (-1) - (-2.5) - \sqrt{\frac{30\text{x}10^{-6}}{110\text{x}10^{-6}\cdot 3}} - .85 = 0.35\text{V}$$

Using V_{DS5} calculate $(W/L)_5$ from the saturation relationship.

$$(W/L)_5 = \frac{2(30 \text{ x } 10^{-6})}{(110 \text{ x } 10^{-6})(0.35)^2} = 4.49 \approx 4.5 \quad \rightarrow \quad \boxed{(W/L)_5 = 4.5}$$

7.) For 60° phase margin, we know that

$$g_{m6} \ge 10g_{m1} \ge 942.5\mu\text{S}$$

Assuming that $g_{m6} = 942.5\mu$S and knowing that $g_{m4} = 150\mu$S, we calculate $(W/L)_6$ as

$$(W/L)_6 = 15\,\frac{942.5 \text{ x } 10^{-6}}{(150 \text{ x } 10^{-6})} = 94.25 \approx 94$$

Example 6.3-1 - Continued

8.) Calculate I_6 using the small-signal g_m expression: $I_6 = \dfrac{(942.5 \text{ x } 10^{-6})^2}{(2)(50 \text{ x } 10^{-6})(94)} = 94.5\mu\text{A} \approx 95\mu\text{A}$

If we calculate $(W/L)_6$ based on V_{out}(max), the value is approximately 15. Since 94 exceeds the specification and maintains better phase margin, we will stay with $(W/L)_6 = 94$ and $I_6 = 95\mu$A.

With $I_6 = 95\mu$A the power dissipation is

$$P_{diss} = 5\text{V}\cdot(30\mu\text{A}+95\mu\text{A}) = 0.625\text{mW}.$$

9.) Finally, calculate $(W/L)_7$

$$(W/L)_7 = 4.5\left(\frac{95 \text{ x } 10^{-6}}{30 \text{ x } 10^{-6}}\right) = 14.25 \approx 14 \quad \rightarrow \quad \boxed{(W/L)_7 = 14}$$

Let us check the V_{out}(min) specification although the W/L of M7 is so large that this is probably not necessary. The value of V_{out}(min) is

$$V_{out}(\text{min}) = V_{DS7}(\text{sat}) = \sqrt{\frac{2\cdot 95}{110\cdot 14}} = 0.351\text{V}$$

which is less than required. At this point, the first-cut design is complete.

10.) Now check to see that the gain specification has been met

$$A_v = \frac{(94.25 \text{ x } 10^{-6})(942.5 \text{ x } 10^{-6})}{15 \text{ x } 10^{-6}(.04 + .05)95 \text{ x } 10^{-6}(.04 + .05)} = 7{,}696\text{V/V}$$

which meets specifications. An easy way to increase the gain would be to increase the W and L values by a factor of two which because of the decreased value of λ would multiply the above gain by a factor of 20.

Example 6.3-1 - Continued

The final step in the hand design is to establish true electrical widths and lengths based upon ΔL and ΔW variations. In this example ΔL will be due to lateral diffusion only. Unless otherwise noted, ΔW will not be taken into account. All dimensions will be rounded to integer values. Assume that ΔL = 0.2µm. Therefore, we have

$W_1 = W_2 = 3(1 - 0.4) = 1.8$ µm ≈ 2µm
$W_3 = W_4 = 15(1 - 0.4) = 9$µm
$W_5 = 4.5(1 - 0.4) = 2.7$µm ≈ 3µm
$W_6 = 94(1 - 0.4) = 56.4$µm ≈ 56µm
$W_7 = 14(1 - 0.4) = 8.4 \approx 8$µm

The figure below shows the results of the first-cut design. The W/L ratios shown do not account for the lateral diffusion discussed above. The next phase requires simulation.

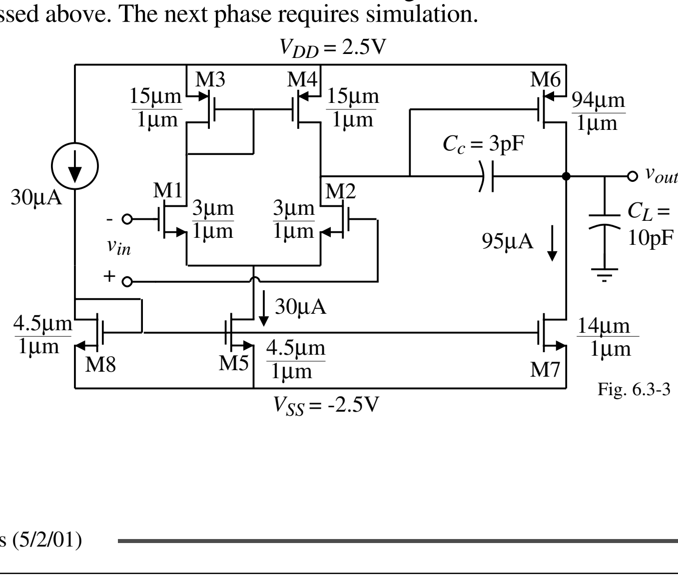


Fig. 6.3-3

Incorporating the Nulling Resistor into the Miller Compensated Two-Stage Op Amp

Circuit:

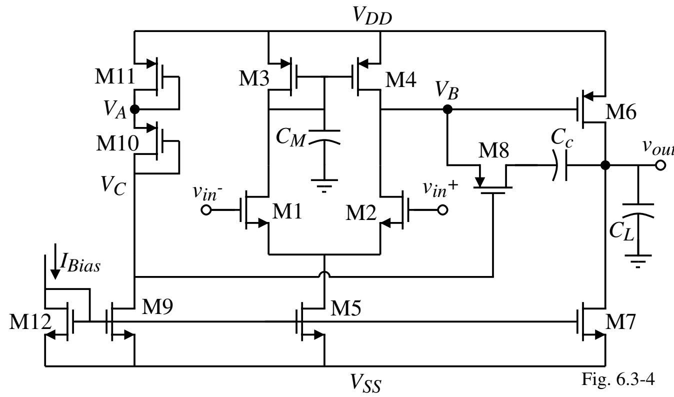


Fig. 6.3-4

We saw earlier that the roots were:

$$p_1 = -\frac{g_{m2}}{A_v C_c} = -\frac{g_{m1}}{A_v C_c} \qquad p_2 = -\frac{g_{m6}}{C_L}$$

$$p_4 = -\frac{1}{R_z C_I} \qquad z_1 = \frac{-1}{R_z C_c - C_c/g_{m6}}$$

where $A_v = g_{m1} g_{m6} R_I R_{II}$. (Note that p_4 is the pole resulting from the nulling resistor compensation technique.)

Design of the Nulling Resistor (M8)

In order to place the zero on top of the second pole (p_2), the following relationship must hold

$$R_z = \frac{1}{g_{m6}}\left(\frac{C_L + C_c}{C_c}\right) = \left(\frac{C_c + C_L}{C_c}\right)\frac{1}{\sqrt{2K'_P S_6 I_6}}$$

The resistor, R_z, is realized by the transistor M8 which is operating in the active region because the dc current through it is zero. Therefore, R_z, can be written as

$$R_z = \frac{dv_{DS8}}{di_{D8}}\bigg|_{V_{DS8}=0} = \frac{1}{K'_P S_8 (V_{SG8} - |V_{TP}|)}$$

The bias circuit is designed so that voltage V_A is equal to V_B.

$$\therefore \quad |V_{GS10}| - |V_T| = |V_{GS8}| - |V_T| \quad \Rightarrow \quad V_{SG11} = V_{SG6} \quad \Rightarrow \quad \left(\frac{W_{11}}{L_{11}}\right) = \left(\frac{I_{10}}{I_6}\right)\left(\frac{W_6}{L_6}\right)$$

In the saturation region

$$|V_{GS10}| - |V_T| = \sqrt{\frac{2(I_{10})}{K'_P(W_{10}/L_{10})}} = |V_{GS8}| - |V_T|$$

$$\therefore \quad R_z = \frac{1}{K'_P S_8}\sqrt{\frac{K'_P S_{10}}{2I_{10}}} = \frac{1}{S_8}\sqrt{\frac{S_{10}}{2K'_P I_{10}}}$$

Equating the two expressions for R_z gives

$$\left(\frac{W_8}{L_8}\right) = \left(\frac{C_c}{C_L + C_c}\right)\sqrt{\frac{S_{10} S_6 I_6}{I_{10}}}$$

Example 6.3-2 - RHP Zero Compensation

Use results of Ex. 6.3-1 and design compensation circuitry so that the RHP zero is moved from the RHP to the LHP and placed on top of the output pole p_2. Use device data given in Ex. 6.3-1.

Solution

The task at hand is the design of transistors M8, M9, M10, M11, and bias current I_{10}. The first step in this design is to establish the bias components. In order to set V_A equal to V_B, then V_{SG11} must equal V_{SG6}. Therefore,

$$S_{11} = (I_{11}/I_6)S_6$$

Choose $I_{11} = I_{10} = I_9 = 15\mu A$ which gives $S_{11} = (15\mu A/95\mu A)94 = 14.8 \approx 15$.

The aspect ratio of M10 is essentially a free parameter, and will be set equal to 1. There must be sufficient supply voltage to support the sum of V_{SG11}, V_{SG10}, and V_{DS9}. The ratio of I_{10}/I_5 determines the (W/L) of M9. This ratio is

$$(W/L)_9 = (I_{10}/I_5)(W/L)_5 = (15/30)(4.5) = 2.25 \approx 2$$

Now $(W/L)_8$ is determined to be

$$(W/L)_8 = \left(\frac{3\text{pF}}{3\text{pF}+10\text{pF}}\right)\sqrt{\frac{1\cdot 94\cdot 95\mu A}{15\mu A}} = 5.63 \approx 6$$

Example 6.3-2 - Continued

It is worthwhile to check that the RHP zero has been moved on top of p_2. To do this, first calculate the value of R_z. V_{SG8} must first be determined. It is equal to V_{SG10}, which is

$$V_{SG10} = \sqrt{\frac{2I_{10}}{K'_P S_{10}}} + |V_{TP}| = \sqrt{\frac{2\cdot 15}{50\cdot 1}} + 0.7 = 1.474\text{V}$$

Next determine R_z.

$$R_z = \frac{1}{K'_P S_8(V_{SG10}-|V_{TP}|)} = \frac{10^6}{50\cdot 5.63(1.474-.7)} = 4.590\text{k}\Omega$$

The location of z_1 is calculated as

$$z_1 = \frac{-1}{(4.590 \text{ x } 10^3)(3\text{x}10^{-12}) - \frac{3\text{x}10^{-12}}{942.5\text{x}10^{-6}}} = -94.46\text{x}10^6 \text{ rads/sec}$$

The output pole, p_2, is

$$p_2 = \frac{942.5\text{x}10^{-6}}{10\text{x}10^{-12}} = -94.25\text{x}10^6 \text{ rads/sec}$$

Thus, we see that for all practical purposes, the output pole is canceled by the zero that has been moved from the RHP to the LHP.

The results of this design are summarized below.

$W_8 = 6$ µm $W_9 = 2$ µm $W_{10} = 1$ µm $W_{11} = 15$ µm

An Alternate Form of Nulling Resistor

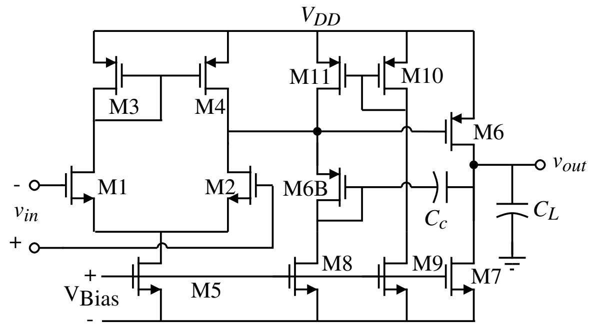


Fig. 6.3-4A

To cancel p_2,

$$z_1 = p_2 \rightarrow \quad R_z = \frac{C_c+C_L}{g_{m6A}C_C} = \frac{1}{g_{m6B}}$$

Which gives

$$g_{m6B} = g_{m6A}\left(\frac{C_c}{C_c+C_L}\right)$$

In the previous example,

g_{m6A} = 942.5μS, C_c = 3pF and C_L = 10pF.

Choose I_{6B} = 10μA to get

$$g_{m6B} = \frac{g_{m6A}C_c}{C_c + C_L} \rightarrow \sqrt{\frac{2K_PW_{6B}I_{6B}}{L_{6B}}} = \left(\frac{C_c}{C_c+C_L}\right)\sqrt{\frac{2K_PW_{6A}I_{D6}}{L_{6A}}}$$

or

$$\frac{W_{6B}}{L_{6B}} = \left(\frac{3}{13}\right)^2 \frac{I_{6A}}{I_{6B}}\frac{W_{6A}}{L_{6A}} = \left(\frac{3}{13}\right)^2\left(\frac{95}{10}\right)(94) = 47.6 \rightarrow W_{6B} = 48\mu m$$

Programmability of the Two-Stage Op Amp

The following relationships depend on the bias current, I_{bias}, in the following manner and allow for programmability after fabrication.

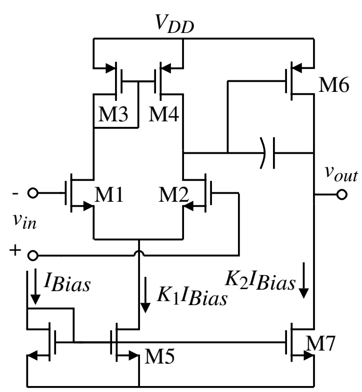


Fig. 6.3-04D

$$A_v(0) = g_{mI}g_{mII}R_IR_{II} \propto \frac{1}{I_{Bias}}$$

$$GB = \frac{g_{mI}}{C_c} \propto \sqrt{I_{Bias}}$$

$$P_{diss} = (V_{DD}+|V_{SS}|)(1+K_1+K_2)I_{Bias} \quad \propto I_{bias}$$

$$SR = \frac{K_1I_{Bias}}{C_c} \propto I_{Bias}$$

$$R_{out} = \frac{1}{2\lambda K_2I_{Bias}} \propto \frac{1}{I_{Bias}}$$

$$|p_1| = \frac{1}{g_{mII}R_IR_{II}C_c} \propto \frac{I_{Bias}^2}{\sqrt{I_{Bias}}} \propto I_{Bias}^{1.5}$$

$$|z| = \frac{g_{mII}}{C_c} \propto \sqrt{I_{Bias}}$$

Illustration of the I_{bias} dependence →

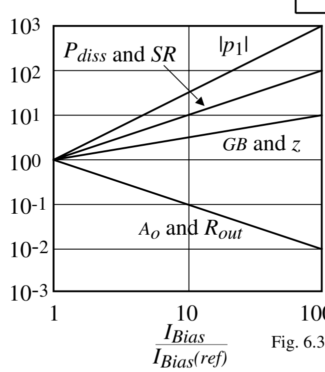


Fig. 6.3-4E

Simulation of the Electrical Design

Area of source or drain = AS = AD = W[L1 + L2 + L3]

where

L1 = Minimum allowable distance between the contact in the S/D and the polysilicon (5µm)

L2 = Width of a minimum size contact (5µm)

L3 = Minimum allowable distance from the contact in S/D to the edge of the S/D (5µm)

∴ AS = AD = Wx15µm

Perimeter of the source or drain = PD = PS = 2W + 2(L1+L2+L3)

∴ PD = PS = 2W + 30µm

Illustration:

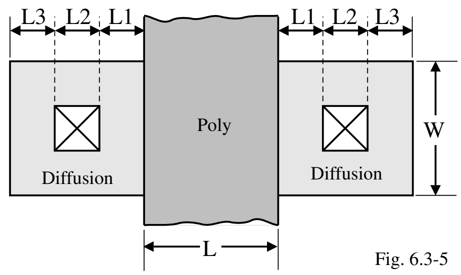


Fig. 6.3-5

5-to-1 Current Mirror with Different Physical Performances

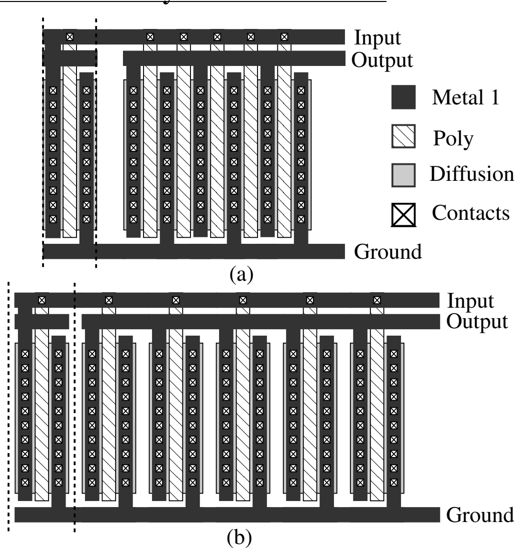


Figure 6.3-6 The layout of a 5-to-1 current mirror. (a) Layout which minimizes area at the sacrifice of matching. (b) Layout which optimizes matching.

1-to-1.5 Transistor Matching

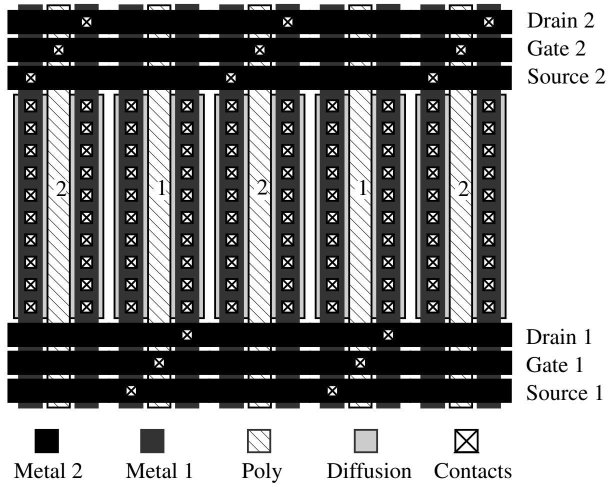


Figure 6.3-7 The layout of two transistors with a 1.5 to 1 matching using centroid geometry to improve matching.

Reduction of Parasitics

The major objective of good layout is to minimize the parasitics that influence the design.

Typical parasitics include:

Capacitors to ac ground

Series resistance

Capacitive parasitics is minimized by minimizing area and maximizing the distance between the conductor and ac ground.

Resistance parasitics are minimized by using wide busses and keeping the bus length short.

For example:

At 2mΩ/square, a metal run of 1000μm and 2μm wide will have 1Ω of resistance.

At 1 mA this amounts to a 1 mV drop which could easily be greater than the least significant bit of an analog-digital converter. (For example, a 10 bit ADC with V_{REF} = 1V has an LSB of 1mV)

Technique for Reducing the Overlap Capacitance

Square Donut Transistor:

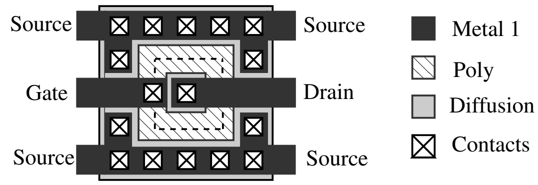


Figure 6.3-8 Reduction of C_{gd} by a donut shaped transistor.

Note: Can get more W/L in less area with the above geometry.

Chip Voltage Bias Distribution Scheme

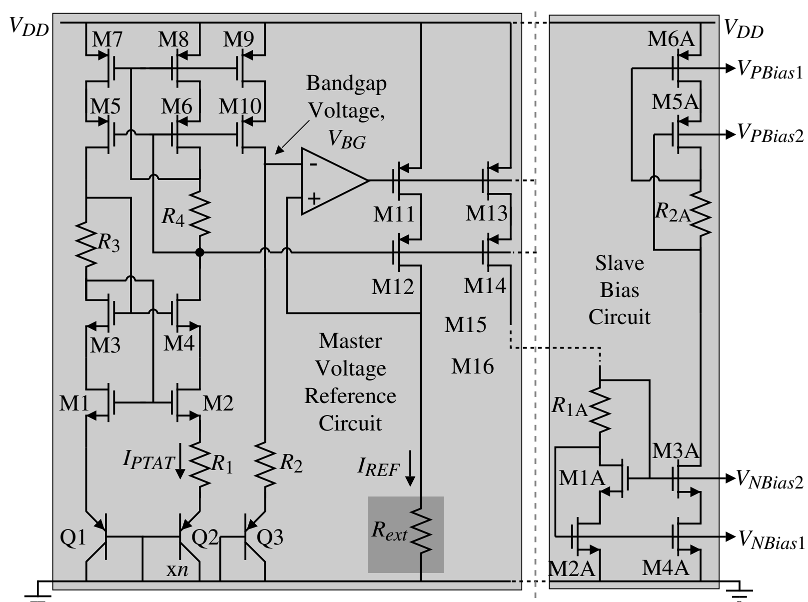


Figure 6.3-9 Generation of a reference voltage which is distributed on the chip as a current to slave bias circuits.

SECTION 6.4 - *PSRR* OF THE TWO-STAGE OP AMP

What is *PSRR*?

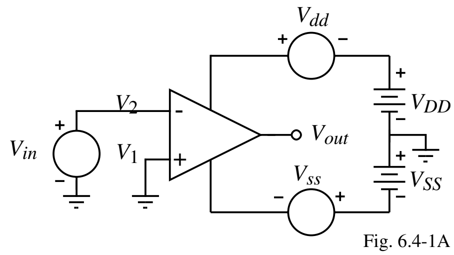


Fig. 6.4-1A

$$PSRR = \frac{A_v(V_{dd}=0)}{A_{dd}(V_{in}=0)}$$

How do you calculate *PSRR*?

You could calculate A_v and A_{dd} and divide.

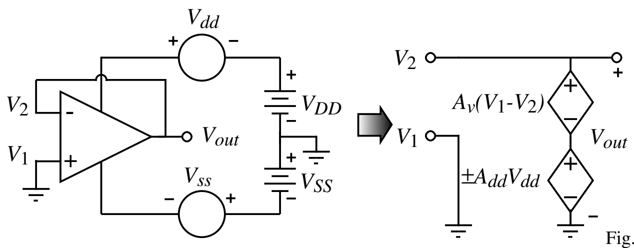


Fig. 6.4-1

$$V_{out} = A_{dd}V_{dd} + A_v(V_1\text{-}V_2) = A_{dd}V_{dd} - A_vV_{out} \quad \rightarrow \quad V_{out}(1+A_v) = A_{dd}V_{dd}$$

$$\therefore\ \frac{V_{out}}{V_{dd}} = \frac{A_{dd}}{1+A_v} \approx \frac{A_{dd}}{A_v} = \frac{1}{PSRR^+}$$ (Good for frequencies up to *GB*)

Positive *PSRR* of the Two-Stage Op Amp

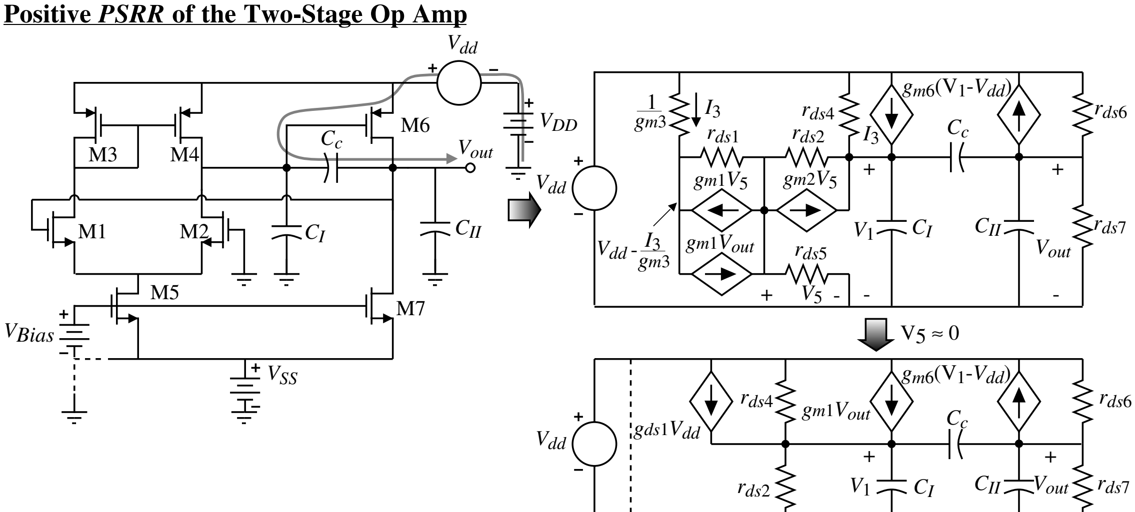


Fig. 6.4-2

The nodal equations are:

$$(g_{ds1} + g_{ds4})V_{dd} = (g_{ds2} + g_{ds4} + sC_c + sC_I)V_1 - (g_{m1} + sC_c)V_{out}$$

$$(g_{m6} + g_{ds6})V_{dd} = (g_{m6} - sC_c)V_1 + (g_{ds6} + g_{ds7} + sC_c + sC_{II})V_{out}$$

Using the generic notation the nodal equations are:

$$G_IV_{dd} = (G_I + sC_c + sC_I)V_1 - (g_{mI} + sC_c)V_{out}$$

$$(g_{mII} + g_{ds6})V_{dd} = (g_{mII} - sC_c)V_1 + (G_{II} + sC_c + sC_{II})V_{out}$$

where $G_I = g_{ds1} + g_{ds4} = g_{ds2} + g_{ds4}$, $G_{II} = g_{ds6} + g_{ds7}$, $g_{mI} = g_{m1} = g_{m2}$ and $g_{mII} = g_{m6}$

Positive *PSRR* of the Two-Stage Op Amp - Continued

Using Cramers rule to solve for the transfer function, V_{out}/V_{dd}, and inverting the transfer function gives the following result.

$$\frac{V_{dd}}{V_{out}} = \frac{s^2[C_cC_I + C_IC_{II} + C_{II}C_c] + s[G_I(C_c+C_{II}) + G_{II}(C_c+C_I) + C_c(g_{mII} - g_{mI})] + G_IG_{II} + g_{mI}g_{mII}}{s[C_c(g_{mII}+G_I+g_{ds6}) + C_I(g_{mII}+g_{ds6})] + G_Ig_{ds6}}$$

We may solve for the approximate roots of numerator as

$$PSRR^+ = \frac{V_{dd}}{V_{out}} \cong \left(\frac{g_{mI}g_{mII}}{G_Ig_{ds6}}\right)\left[\frac{\left(\frac{sC_c}{g_{mI}}+1\right)\left(\frac{s(C_cC_I+C_IC_{II}+C_cC_{II})}{g_{mII}\,C_c}+1\right)}{\left(\frac{sg_{mII}C_c}{G_Ig_{ds6}}+1\right)}\right]$$

where $g_{mII} > g_{mI}$ and that all transconductances are larger than the channel conductances.

$$\therefore \quad PSRR^+ = \frac{V_{dd}}{V_{out}} = \left(\frac{g_{mI}g_{mII}}{G_Ig_{ds6}}\right)\left[\frac{\left(\frac{sC_c}{g_{mI}}+1\right)\left(\frac{sC_{II}}{g_{mII}}+1\right)}{\frac{sg_{mII}C_c}{G_Ig_{ds6}}+1}\right] = \left(\frac{G_{II}A_{vo}}{g_{ds6}}\right)\frac{\left(\frac{s}{GB}+1\right)\left(\frac{s}{|p_2|}+1\right)}{\left(\frac{sG_{II}A_{vo}}{g_{ds6}GB}+1\right)}$$

Positive *PSRR* of the Two-Stage Op Amp - Continued

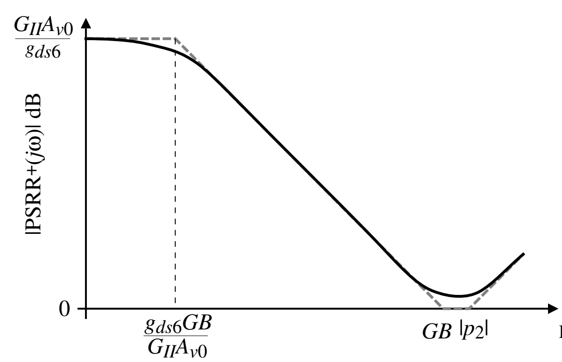


Fig. 6.4-3

At approximately the dominant pole, the *PSRR* falls off with a -20dB/decade slope and degrades the higher frequency $PSRR^+$ of the two-stage op amp.

Using the values of Example 6.3-1 we get:

$PSRR^+(0) = 68.8\text{dB}$, $z_1 = -5\text{MHz}$, $z_2 = -15\text{MHz}$ and $p_1 = -906\text{Hz}$

Concept of the $PSRR^+$ for the Two-Stage Op Amp

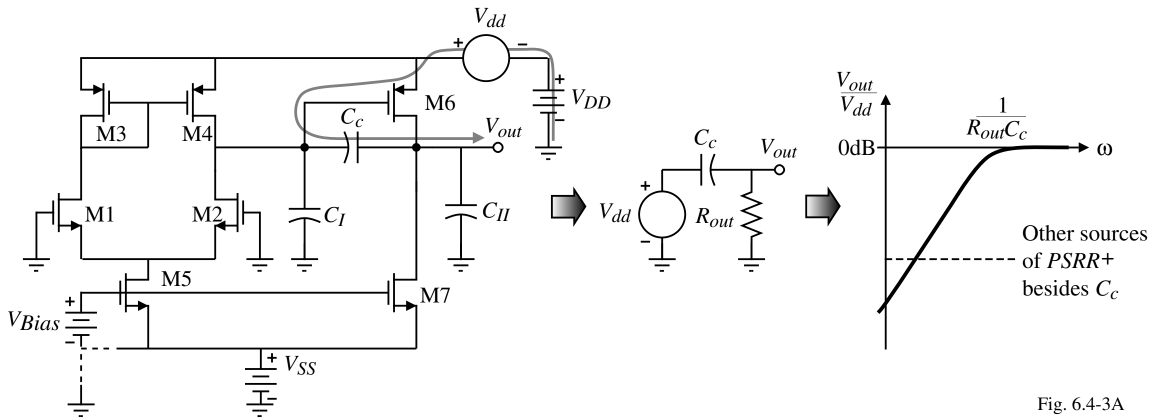


Fig. 6.4-3A

1.) The M7 current sink causes V_{SG6} to act like a battery.

2.) Therefore, V_{dd} couples from the source to gate of M6.

3.) The path to the output is through any capacitance from gate to drain of M6.

Conclusion:

The Miller capacitor C_c couples the positive power supply ripple directly to the output.

Must reduce or eliminate C_c.

Negative *PSRR* of the Two-Stage Op Amp with V_{Bias} Grounded

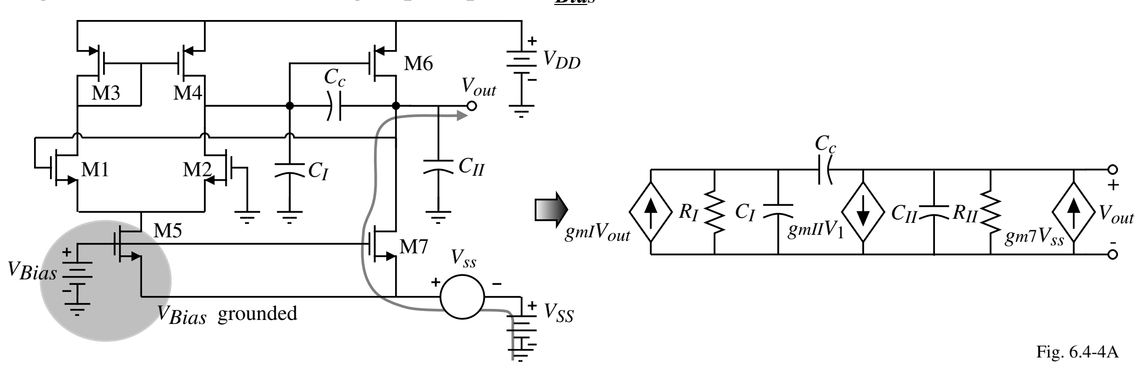


Fig. 6.4-4A

Nodal equations for V_{Bias} grounded:

$$0 = (G_I + sC_c + sC_I)V_1 - (g_{mI} + sC_c)V_o$$

$$g_{m7}V_{ss} = (g_{MII} - sC_c)V_1 + (G_{II} + sC_c + sC_{II})V_o$$

Solving for V_{out}/V_{ss} and inverting gives

$$\frac{V_{ss}}{V_{out}} = \frac{s^2[C_cC_I + C_IC_{II} + C_{II}C_c] + s[G_I(C_c+C_{II}) + G_{II}(C_c+C_I) + C_c(g_{mII} - g_{mI})] + G_IG_{II} + g_{mI}g_{mII}}{[s(C_c+C_I)+G_I]g_{m7}}$$

Negative *PSRR* of the Two-Stage Op Amp with V_{Bias} Grounded - Continued

Again using the technique described previously, we may solve for the approximate roots as

$$PSRR^- = \frac{V_{ss}}{V_{out}} \cong \left(\frac{g_{mI}g_{mII}}{G_I g_{m7}}\right)\left[\frac{\left(\frac{sC_c}{g_{mI}}+1\right)\left(\frac{s(C_cC_I+C_IC_{II}+C_cC_{II})}{g_{mII}\,C_c}+1\right)}{\left(\frac{s(C_c+C_I)}{G_I}+1\right)}\right]$$

This equation can be rewritten approximately as

$$PSRR^- = \frac{V_{ss}}{V_{out}} \cong \left(\frac{g_{mI}g_{mII}}{G_I g_{m7}}\right)\left[\frac{\left(\frac{sC_c}{g_{mI}}+1\right)\left(\frac{sC_{II}}{g_{mII}}+1\right)}{\left(\frac{sC_c}{G_I}+1\right)}\right] = \left(\frac{G_{II}A_{v0}}{g_{m7}}\right)\left[\frac{\left(\frac{s}{GB}+1\right)\left(\frac{s}{|p_2|}+1\right)}{\left(\frac{s}{GB}\frac{g_{mI}}{G_I}+1\right)}\right]$$

Comments:

$PSRR^-$ zeros = $PSRR^+$ zeros

DC gain ≈ Second-stage gain,

$PSRR^-$ pole ≈ (Second-stage gain) x ($PSRR^+$ pole)

Assuming the values of Ex. 6.3-1 gives a gain of 23.7 dB and a pole -147 kHz. The dc value of $PSRR^-$ is very poor for this case, however, this case can be avoided by correctly implementing V_{Bias} which we consider next.

Negative *PSRR* of the Two-Stage Op Amp with V_{Bias} Connected to V_{SS}

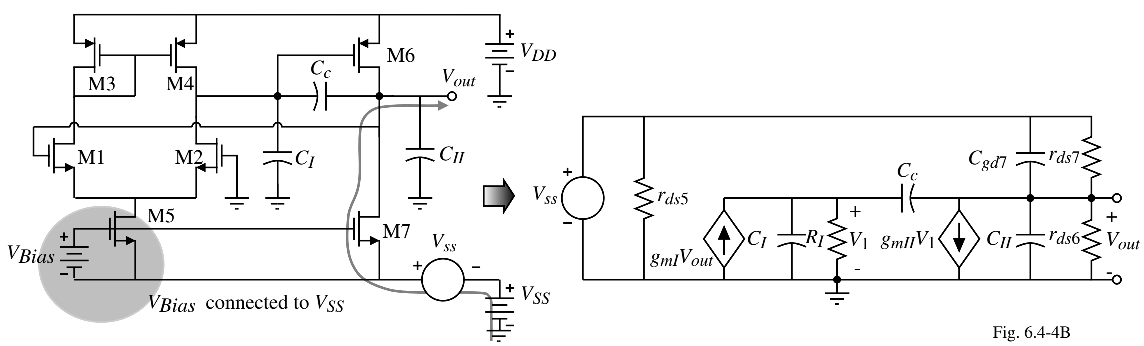


Fig. 6.4-4B

If the value of V_{Bias} is independent of V_{ss}, then the model shown results. The nodal equations for this model are

$$0 = (G_I + sC_c + sC_I)V_1 - (g_{mI} + sC_c)V_{out}$$

and

$$(g_{ds7} + sC_{gd7})V_{ss} = (g_{mII} - sC_c)V_1 + (G_{II} + sC_c + sC_{II} + sC_{gd7})V_{out}$$

Again, solving for V_{out}/V_{ss} and inverting gives

$$\frac{V_{ss}}{V_{out}} = \frac{s^2[C_cC_I+C_IC_{II}+C_{II}C_c+C_IC_{gd7}+C_cC_{gd7}]+s[G_I(C_c+C_{II}+C_{gd7})+G_{II}(C_c+C_I)+C_c(g_{mII}-g_{mI})]+G_IG_{II}+g_{mI}g_{mII}}{(sC_{gd7}+g_{ds7})(s(C_I+C_c)+G_I)}$$

Negative *PSRR* of the Two-Stage Op Amp with V_{Bias} Connected to V_{SS} - Continued

Assuming that $g_{mII} > g_{mI}$ and solving for the approximate roots of both the numerator and denominator gives

$$PSRR^- = \frac{V_{ss}}{V_{out}} \cong \left(\frac{g_{mI}g_{mII}}{G_I g_{ds7}}\right)\left[\frac{\left(\frac{sC_c}{g_{mI}}+1\right)\left(\frac{s(C_cC_I+C_IC_{II}+C_cC_{II})}{g_{mII}\,C_c}+1\right)}{\left(\frac{sC_{gd7}}{g_{ds7}}+1\right)\left(\frac{s(C_I+C_c)}{G_I}+1\right)}\right]$$

This equation can be rewritten as

$$PSRR^- = \frac{V_{ss}}{V_{out}} \approx \left(\frac{G_{II}A_{v0}}{g_{ds7}}\right)\left[\frac{\left(\frac{s}{GB}+1\right)\left(\frac{s}{|p_2|}+1\right)}{\left(\frac{sC_{gd7}}{g_{ds7}}+1\right)\left(\frac{sC_c}{G_I}+1\right)}\right]$$

Comments:

- DC gain has been increased by the ratio of G_{II} to g_{ds7}
- Two poles instead of one, however the pole at $-g_{ds7}/C_{gd7}$ is very large and can be ignored.

Using the values of Ex. 6.3-1 and assume that C_{ds7} = 10fF, gives,

$PSRR^-(0)$ = 76.7dB

Poles at -71.2kHz and -149MHz

Frequency Response of the Negative *PSRR* of the Two-Stage Op Amp with V_{Bias} Connected to V_{SS}

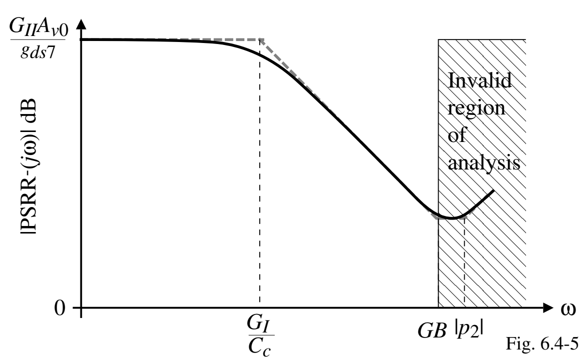


Fig. 6.4-5

Approximate Model for Negative *PSRR* with V_{Bias} Connected to Ground

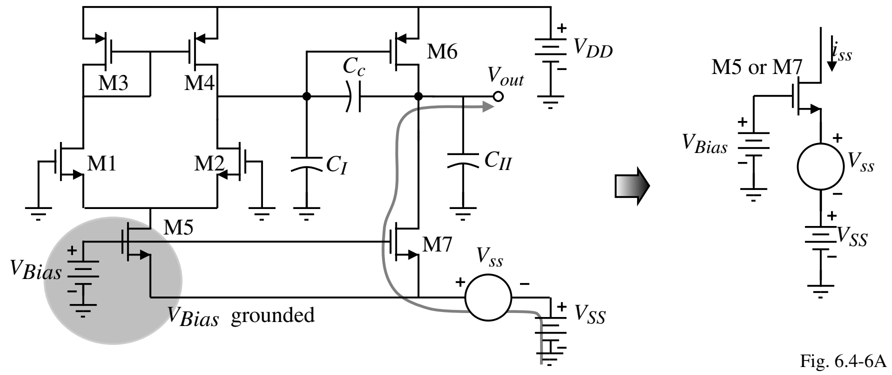


Fig. 6.4-6A

Path through the input stage is not important as long as the *CMRR* is high.

Path through the output stage:

$$v_{out} \approx i_{ss}Z_{out} = g_{m7}Z_{out}V_{ss}$$

$$\therefore \quad \frac{V_{out}}{V_{ss}} = g_{m7}Z_{out} = g_{m7}R_{out}\left(\frac{1}{sR_{out}C_{out}+1}\right)$$

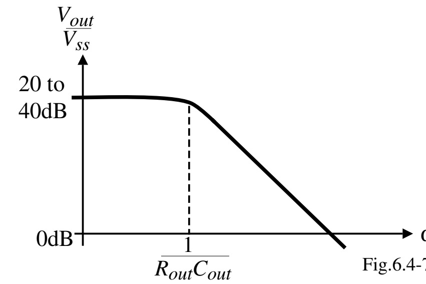


Fig.6.4-7A

Approximate Model for Negative *PSRR* with V_{Bias} Connected to V_{SS}

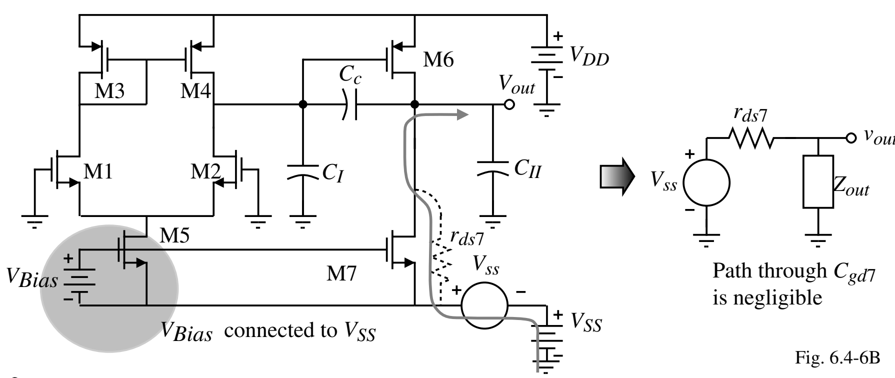


Fig. 6.4-6B

What is Z_{out}?

$$Z_{out} = \frac{V_t}{I_t} \Rightarrow I_t = g_{mII}V_1 = g_{mII}\left(\frac{g_{mI}V_t}{G_I+sC_I+sC_c}\right)$$

Thus, $Z_{out} = \dfrac{G_I+s(C_I+C_c)}{g_{mI}g_{MII}}$

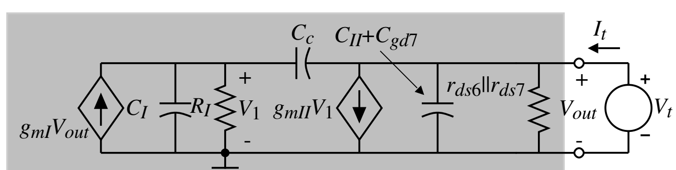


Fig.6.4-7B

$\therefore$

$$\frac{V_{ss}}{V_{out}} = \frac{1+\frac{r_{ds7}}{Z_{out}}}{1} = \frac{s(C_c+C_I) + G_I+g_{mI}g_{mII}r_{ds7}}{s(C_c+C_I) + G_I} \quad \Rightarrow \quad \text{Pole at } \frac{-G_I}{C_c+C_I}$$

The two-stage op amp will never have good *PSRR* because of the Miller compensation.

SECTION 6.5 - CASCODE OP AMPS

Why Cascode Op Amps?

- Control of the frequency behavior
- Can get more gain by increasing the output resistance of a stage
- In the past section, *PSRR* of the two-stage op amp was insufficient for many applications
- A two-stage op amp can become unstable for large load capacitors (if nulling resistor is not used)
- We will see in future sections that the cascode op amp leads to wider *ICMR* and/or smaller power supply requirements

Where Should the Cascode Technique be Used?

- First stage -

    Good noise performance

    Requires level translation to second stage

    Degrades the Miller compensation

- Second stage -

    Self compensating

    Increases the efficiency of the Miller compensation

    Increases *PSRR*

Use of Cascoding in the First Stage of the Two-Stage Op Amp

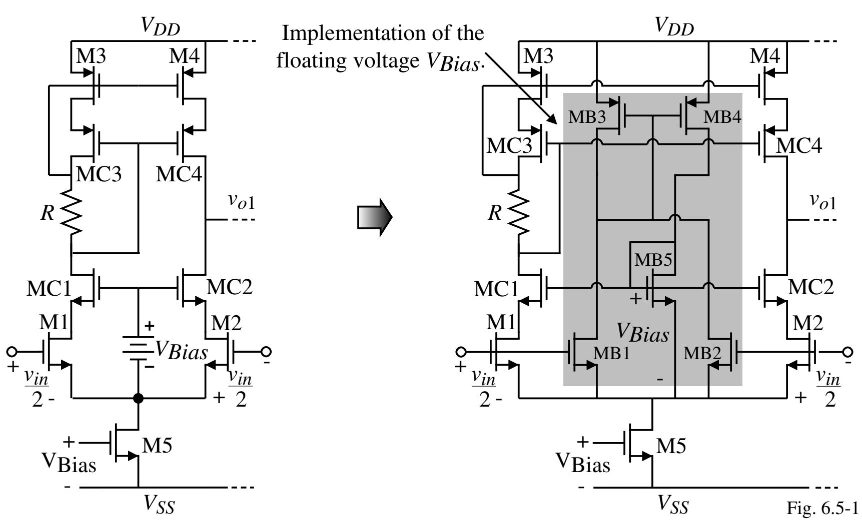


Fig. 6.5-1

R_{out} of the first stage is $R_I \approx (g_{mC2}r_{dsC2}r_{ds2})||(g_{mC4}r_{dsC4}r_{ds4})$

Voltage gain $= \frac{v_{o1}}{v_{in}} = g_{m1}R_I$ [The gain is increased by approximately $0.5(g_{MC}r_{dsC})$]

As a single stage op amp, the compensation capacitor becomes the load capacitor.

Example 6.5-1 Single-Stage, Cascode Op Amp Performance

Assume that all W/L ratios are 10 μm/1 μm, and that $I_{DS1} = I_{DS2} =$ 50 μA of single stage op amp. Find the voltage gain of this op amp and the value of C_I if GB = 10 MHz. Use the model parameters of Table 3.1-2.

Solution

The device transconductances are

$$g_{m1} = g_{m2} = g_{mI} = 331.7\ \mu\text{S}$$

$$g_{mC2} = 331.7\mu\text{S}$$

$$g_{mC4} = 223.6\ \mu\text{S}.$$

The output resistance of the NMOS and PMOS devices is 0.5 MΩ and 0.4 MΩ, respectively.

$\therefore$ R_I = 25 MΩ

$A_v(0)$ = 8290 V/V.

For a unity-gain bandwidth of 10 MHz, the value of C_I is 5.28 pF.

What happens if a 100pF capacitor is attached to this op amp?

GB goes from 10MHz to 0.53MHz.

Two-Stage Op Amp with a Cascoded First-Stage

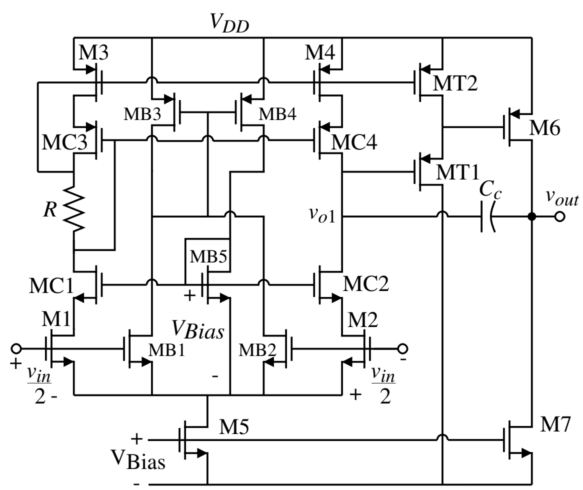


Fig. 6.5-2

- MT1 and MT2 are required for level shifting from the first-stage to the second.
- The $PSRR^+$ is improved by the presence of MT1
- Internal loop pole at the gate of M6 may cause the Miller compensation to fail.
- The voltage gain of this op amp could easily be 100,000V/V

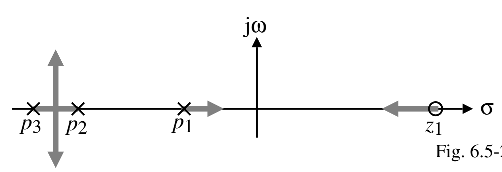


Fig. 6.5-2A

Two-Stage Op Amp with a Cascode Second-Stage

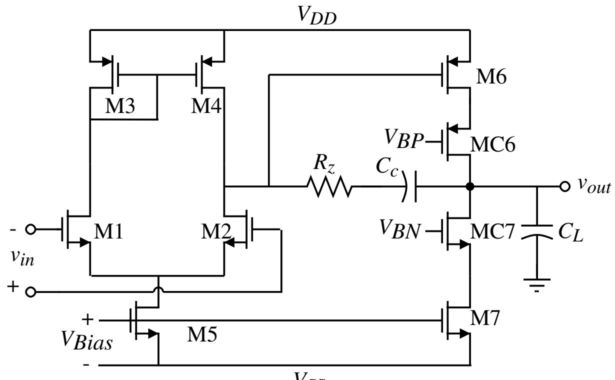


Fig. 6.5-3

$A_v = g_{mI}g_{mII}R_IR_{II}$ where $g_{mI} = g_{m1} = g_{m2}$, $g_{mII} = g_{m6}$,

$$R_I = \frac{1}{g_{ds2} + g_{ds4}} = \frac{2}{(\lambda_2 + \lambda_4)I_{D5}} \text{ and } R_{II} = (g_{mC6}r_{dsC6}r_{ds6})||(g_{mC7}r_{dsC7}r_{ds7})$$

Comments:

- The second-stage gain has greatly increased improving the Miller compensation
- The overall gain is approximately $(g_mr_{ds})^3$ or very large
- Output pole, p_2, is approximately the same if C_c is constant
- The RHP is the same if C_c is constant

A Balanced, Two-Stage Op Amp using a Cascode Output Stage

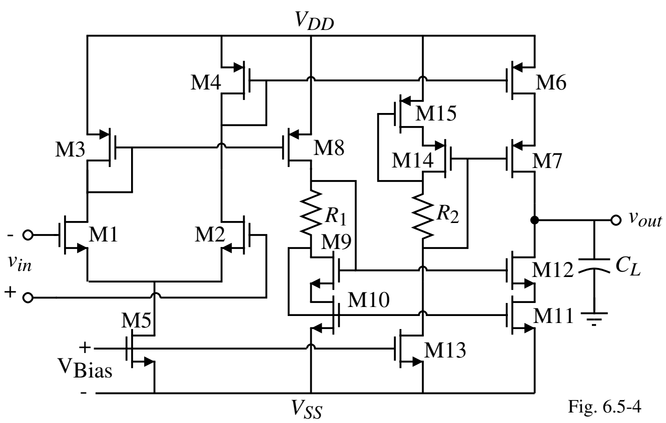


Fig. 6.5-4

$$v_{out} = \left(\frac{g_{m1}g_{m8}}{g_{m3}}\frac{v_{in}}{2} + \frac{g_{m2}g_{m6}}{g_{m4}}\frac{v_{in}}{2}\right)R_{II}$$

$$= \left(\frac{g_{m1}}{2} + \frac{g_{m2}}{2}\right)kv_{in}\, R_{II} = g_{m1}\cdot k\cdot R_{II}\, v_{in}$$

where

$$R_{II} = (g_{m7}r_{ds7}r_{ds6})||(g_{m12}r_{ds12}r_{ds11})$$

and

$$k = \frac{g_{m8}}{g_{m3}} = \frac{g_{m6}}{g_{m4}}$$

Note that this op amp is balanced because the drain-to-ground loads for M1 and M2 are identical.

TABLE 6.5-1 Pertinent Design Relationships for Balanced, Cascode Output Stage Op Amp.

Slew rate $= \dfrac{I_{out}}{C_L}$	$GB = \dfrac{g_{m1}g_{m8}}{g_{m3}C_L}$	$A_v = \dfrac{1}{2}\left(\dfrac{g_{m1}g_{m8}}{g_{m3}} + \dfrac{g_{m2}g_{m6}}{g_{m4}}\right)R_{II}$
$V_{in}(\max) = V_{DD} - \left[\dfrac{I_5}{\beta_3}\right]^{1/2} - \lvert V_{TO3}\rvert(\max) + V_{T1}(\min)$		$V_{in}(\min) = V_{SS} + V_{DS5} + \left[\dfrac{I_5}{\beta_1}\right]^{1/2} + V_{T1}(\min)$

Example 6.5-2 Design of Balanced, Cascoded Output Stage Op Amp

The balanced, cascoded output stage op amp is a useful alternative to the two-stage op amp. Its design will be illustrated by this example. The pertinent design equations for the op amp were given above. The specifications of the design are as follows:

$V_{DD} = -V_{SS} = 2.5$ V

Slew rate = 5 V/μs with a 50 pF load

GB = 10 MHz with a 10 pF load

$A_v \geq 5000$

Input CMR = −1V to +1.5 V

Output swing = ±1.5 V

Use the parameters of Table 3.1-2 and let all device lengths be 1 μm.

Solution

While numerous approaches can be taken, we shall follow one based on the above specifications. The steps will be numbered to help illustrate the procedure.

1.) The first step will be to find the maximum source/sink current. This is found from the slew rate.

$$I_{\text{source}}/I_{\text{sink}} = C_L \times \text{slew rate} = 50\text{ pF}(5\text{ V}/\mu\text{s}) = 250\ \mu\text{A}$$

2.) Next some W/L constraints based on the maximum output source/sink current are developed. Under dynamic conditions, all of I_5 will flow in M4; thus we can write

$$\text{Max. } I_{\text{out}}(\text{source}) = (S_6/S_4)I_5 \quad \text{and} \quad \text{Max. } I_{out}(\text{sink}) = (S_8/S_3)I_5$$

The maximum output sinking current is equal to the maximum output sourcing current if

$$S_3 = S_4,\quad S_6 = S_8,\ \text{ and } S_{10} = S_{11}$$

Example 6.5-2 - Continued

3.) Choose I_5 as 100 μA. Remember that this value can always be changed later on if desirable. This current gives

$$S_6 = 2.5S_4 \ \text{ and } \ S_8 = 2.5S_3$$

Note that S_8 could equal S_3 if $S_{11} = 2.5S_{10}$. This would minimize the power dissipation.

4.) Next design for ±1.5 V output capability. We shall assume that the output must source or sink the 250μA at the peak values of output. First consider the negative output peak. Since there is 1 V difference between V_{SS} and the minimum output, let $V_{DS11}(\text{sat}) = V_{DS12}(\text{sat}) = 0.5$ V (we continue to ignore the bulk effects which should be considered for a more precise design). Under the maximum negative peak assume that $I_{11} = I_{12} = 250\ \mu$A. Therefore

$$0.5 = \sqrt{\frac{2I_{11}}{K'_N S_{11}}} = \sqrt{\frac{2I_{12}}{K'_N S_{12}}} = \sqrt{\frac{500\ \mu\text{A}}{(110\ \mu\text{A/V}^2)S_{11}}}$$

which gives $S_{11} = S_{12} = 18.2$ and $S_9 = S_{10} = 18.2$. Using the same approach for the positive peak gives

$$0.5 = \sqrt{\frac{2I_6}{K'_P S_6}} = \sqrt{\frac{2I_7}{K'_P S_7}} = \sqrt{\frac{500\ \mu\text{A}}{(50\ \mu\text{A/V}^2)S_6}}$$

which gives $S_6 = S_7 = S_8 = 40$ and $S_3 = S_4 = (40/2.5) = 16$.

5.) Next the values of R_1 and R_2 are designed. For the resistor of the self-biased cascode we can write

$$R_1 = \frac{V_{DS12}(\text{sat})}{250\mu\text{A}} = 2\text{k}\Omega \quad \text{and} \quad R_2 = \frac{V_{SD7}(\text{sat})}{250\mu\text{A}} = 2\text{k}\Omega$$

Example 6.5-2 - Continued

Using this value of R_1 (R_2) will cause M11 to slightly be in the active region under quiescent conditions. One could redesign R_1 to avoid this but the minimum output voltage under maximum sinking current would not be realized. The choice is up to the designer and what is important in the circuit performance.

6.) Now we must consider the possibility of conflict among the specifications.

First consider the input CMR. S_3 has already been designed as 16. Using ICMR relationship, we find that S_3 should be at least 4.1. A larger value of S_3 will give a higher value of V_{in}(max) so that we continue to use S_3 = 16 which gives V_{in}(max) = 1.95V.

Next, check to see if the larger W/L causes a pole below the gainbandwidth. Assuming a C_{ox} of 0.4fF/μm^2 gives the first-stage pole of

$$p_3 = \frac{-g_{m3}}{C_{gs3}+C_{gs8}} = \frac{-\sqrt{2K'_P S_3 I_3}}{2(0.667)(W_3L_3+W_8L_8)C_{ox}} = 33.15\text{x}10^9 \text{ rads/sec or } 5.275\text{GHz}$$

which is much greater than 10GB.

7.) Next we find g_{m1} (g_{m2}). There are two ways of calculating g_{m1}.

(a.) The first is from the A_v specification. The gain is

$$A_v = (g_{m1}/2g_{m4})(g_{m6} + g_{m11})\, R_{II}$$

Note that a current gain of k could be introduced by making S_6/S_4 ($S_8/S_3 = S_{11}/S_3$) equal to k.

$$\frac{g_{m6}}{g_{m4}} = \frac{g_{m11}}{g_{m3}} = \sqrt{\frac{2K_P'\cdot S_6\cdot I_6}{2K_P'\cdot S_4\cdot I_4}} = k$$

Example 6.5-2 - Continued

Calculating the various transconductances we get g_{m4} = 282.4 μS, $g_{m6} = g_{m7}$ = 707 μS, $g_{m11} = g_{m12}$ = 707 μS, $r_{ds6} = r_{d7}$ = 0.16 MΩ, and $r_{ds11} = r_{ds12}$ = 0.2 MΩ. Assuming that the gain A_v must be greater than 5000 and k = 2.5 gives g_{m1} > 72.43 μS.

(b.) The second method of finding g_{m1} is from the GB specifications. Multiplying the gain by the dominant pole ($1/C_{II}R_{II}$) gives

$$GB = \frac{g_{m1}(g_{m6} + g_{m11})}{2g_{m4}C_L}$$

Assuming that C_L= 10 pF and using the specified GB gives g_{m1} = 251 μS.

Since this is greater than 72.43μS, we choose $g_{m1} = g_{m2}$ = 251μS. Knowing I_5 gives $S_1 = S_2$ = 11.45 ≈ 12.

8.) The next step is to check that S_1 and S_2 are large enough to meet the −1V input CMR specification. Use the saturation formula we find that V_{DS5} is 0.5248 V. This gives S_5 = 6.6 ≈ 7. The gain becomes A_v = 6,925V/V and GB = 10 MHz for a 10 pF load. We shall assume that exceeding the specifications in this area is not detrimental to the performance of the op amp.

9.) With S_5 = 7 then we can design S_{13} from the relationship

$$S_{13} = \frac{I_{13}}{I_5} S_5 = \frac{125\mu\text{A}}{100\mu\text{A}} 7 = 8.75$$

Example 6.5-2 - Continued

10.) Finally we need to design the value of V_{Bias}, which can be done with the values of S_5 and I_5 known. However, M5 is usually biased from a current source flowing into a MOS diode in parallel with the gate-source of M5. The value of the current source compared with I_5 would define the W/L ratio of the MOS diode.

Table 6.5-2 summarizes the values of *W*/*L* that resulted from this design procedure. The power dissipation for this design is seen to be 2 mW. The next step would be begin simulation.

Table 6.5-2 Summary of W/L Ratios for Example 6.5-2

$S_1 = S_2 = 12$
$S_3 = S_4 = 16$
$S_5 = 7$
$S_6 = S_7 = S_8 = S_{14} = S_{15} = 40$
$S_9 = S_{10} = S_{11} = S_{12} = 18.2$
$S_{13} = 8.75$

Technological Implications of the Cascode Configuration

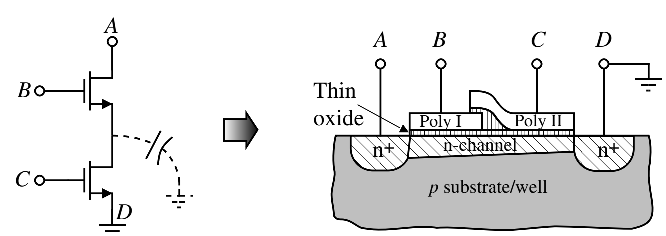


Fig. 6.5-5

If a double poly CMOS process is available, internode parasitics can be minimized.

As an alternative, one should keep the drain/source between the transistors to a minimum area.

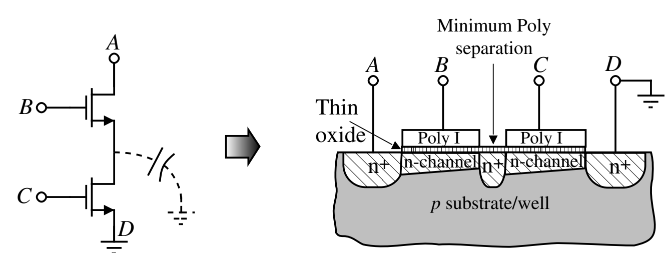
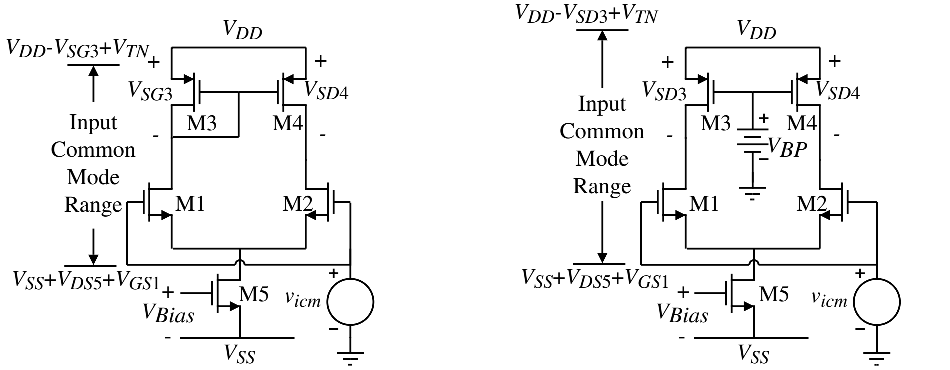


Fig. 6.5-5A

Input Common Mode Range for Two Types of Differential Amplifier Loads



Differential amplifier with a current mirror load.

Differential amplifier with current source loads.

Fig. 6.5-6

In order to improve the ICMR, it is desirable to use current source (sink) loads without losing half the gain. The resulting solution is the *folded* cascode op amp.

The Folded Cascode Op Amp

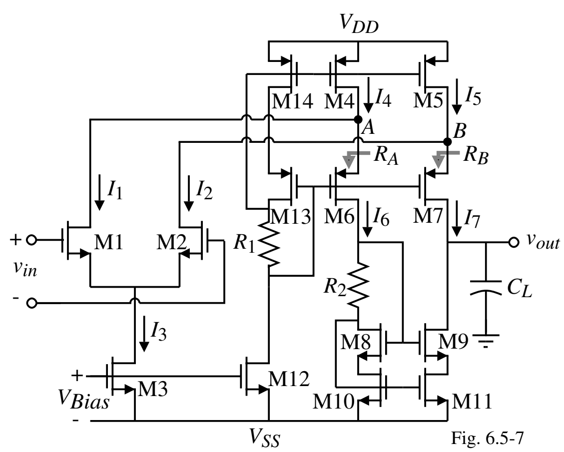


Fig. 6.5-7

Comments:

- The bias currents, I_4 and I_5, should be designed so that I_6 and I_7 never become zero (i.e. I_4=I_5=1.5I_3)
- This amplifier is nearly balanced (would be exactly if R_A was equal to R_B)
- Self compensating
- Poor noise performance, the gain occurs at the output so all intermediate transistors contribute to the noise along with the input transistors. (Some first stage gain can be achieved if R_A and R_B are greater than g_{m1} or g_{m2}.

Small-Signal Analysis of the Folded Cascode Op Amp

Model:

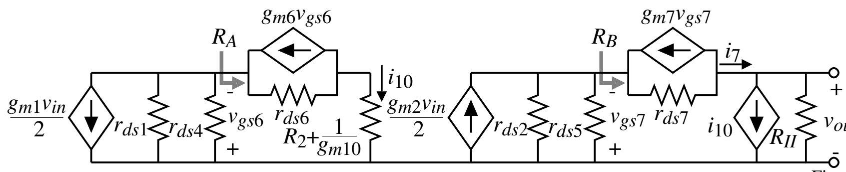


Fig. 6.5-8

Recalling what we learned about the resistance looking into the source of the cascode transistor,

$$R_A = \frac{r_{ds6}+R_2+(1/g_{m10})}{1+g_{m6}r_{ds6}} \approx \frac{1}{g_{m6}} \quad \text{and} \quad R_B = \frac{r_{ds7}+R_{II}}{1+g_{m7}r_{ds7}} \approx \frac{R_{II}}{g_{m7}r_{ds7}} \quad \text{where} \quad R_{II} \approx g_{m9}r_{ds9}r_{ds11}$$

The small-signal voltage transfer function can be found as follows. The current i_{10} is written as

$$i_{10} = \frac{-g_{m1}(r_{ds1}||r_{ds4})v_{in}}{2[R_A+(r_{ds1}||r_{ds4})]} \approx \frac{-g_{m1}v_{in}}{2}$$

and the current i_7 can be expressed as

$$i_7 = \frac{g_{m2}(r_{ds2}||r_{ds5})v_{in}}{2\left[\frac{R_{II}}{g_{m7}r_{ds7}}+(r_{ds2}||r_{ds5})\right]} = \frac{g_{m2}v_{in}}{2\left(1+\frac{R_{II}(g_{ds2}+g_{ds5})}{g_{m7}r_{ds7}}\right)} = \frac{g_{m2}v_{in}}{2(1+k)} \qquad \text{where} \qquad k = \frac{R_{II}(g_{ds2}+g_{ds4})}{g_{m7}r_{ds7}}$$

The output voltage, v_{out}, is equal to the sum of i_7 and i_{10} flowing through R_{out}. Thus,

$$\frac{v_{out}}{v_{in}} = \left(\frac{g_{m1}}{2}+\frac{g_{m2}}{2(1+k)}\right)R_{out} = \left(\frac{2+k}{2+2k}\right)g_{mI}R_{out} \qquad \text{where} \quad R_{out} \approx g_{m9}r_{ds9}r_{ds11}||[g_{m7}r_{ds7}(r_{ds2}||r_{ds5})]$$

Frequency Response of the Folded Cascode Op Amp

The frequency response of the folded cascode op amp is determined primarily by the output pole which is given as

$$p_{out} = \frac{-1}{R_{out}C_{out}}$$

where C_{out} is all the capacitance connected from the output of the op amp to ground.

All other poles must be greater than $GB = g_{m1}/C_{out}$. The approximate expressions for each pole is

1.) Pole at node A: $p_A \approx \frac{-1}{R_A C_A}$

2.) Pole at node B: $p_B \approx \frac{-1}{R_B C_B}$

3.) Pole at drain of M6: $p_6 \approx \frac{-1}{(R_2+1/g_{m10})C_6}$

4.) Pole at source of M8: $p_8 \approx \frac{-g_{m8}}{C_8}$ (Note that for the wide-swing cascode mirror, $p_8 \approx \frac{-g_{m8}r_{ds8}g_{m10}}{C_8}$)

5.) Pole at source of M9: $p_9 \approx \frac{-g_{m9}}{C_9}$

6.) Pole at gate of M10: $p_{10} \approx \frac{-g_{m10}}{C_{10}}$

where the approximate expressions are found by the reciprocal product of the resistance and parasitic capacitance seen to ground from a given node. One might feel that because R_B is approximately r_{ds} that this pole might be too small. However, at frequencies where this pole has influence, C_{out}, causes R_{II} to be much smaller making p_B also non-dominant.

PSRR **of the Folded Cascode Op Amp**

Consider the following circuit used to model the *PSRR*$^-$:

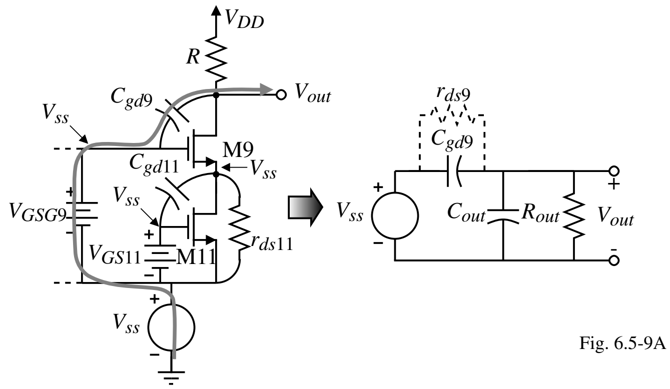


Fig. 6.5-9A

This model assumes that gate, source and drain of M11 and the gate and source of M9 all vary with V_{SS}.

We shall examine V_{out}/V_{ss} rather than *PSRR*$^-$. (Small V_{out}/V_{ss} will lead to large *PSRR*$^-$.)

The transfer function of V_{out}/V_{ss} can be found as

$$\frac{V_{out}}{V_{ss}} \approx \frac{sC_{gd9}R_{out}}{sC_{out}R_{out}+1} \qquad \text{for } C_{gd9} < C_{out}$$

The approximate PSRR$^-$ is sketched on the next page.

Frequency Response of the PSRR$^-$ of the Folded Cascode Op Amp

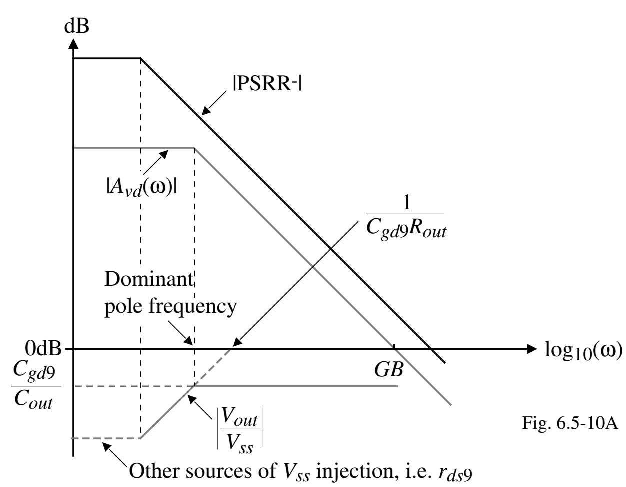


Fig. 6.5-10A

We see that the PSRR of the cascode op amp is much better than the two-stage op amp.

Design Approach for the Folded-Cascode Op Amp

Step	Relationship/Requirement	Design Equation/Constraint	Comments
1	Slew Rate	$I_3 = SR \cdot C_L$	
2	Bias currents in output cascodes	$I_4 = I_5 = 1.2I_3$ to $1.5I_3$	Avoid zero current in cascodes
3	Maximum output voltage, v_{out}(max)	$S_5=\frac{8I_5}{K_P' V_{SD5}^2}$, $S_7=\frac{8I_7}{K_P' V_{SD7}^2}$ Let $S_4=S_{14}=S_5$ & $S_{13}=S_6=S_7$	V_{SD5}(sat) = V_{SD7}(sat) = $0.5[V_{DD}-V_{out}$(min)]
4	Minimum output voltage, v_{out}(min)	$S_{11}=\frac{8I_{11}}{K_N' V_{DS11}^2}$, $S_9=\frac{8I_9}{K_N' V_{DS9}^2}$ Let $S_{10}=S_{11}$ & $S_8=S_9$	V_{DS9}(sat) = V_{DS11}(sat) = $0.5(V_{out}$(min)-$\|V_{SS}\|$)
5	Self-bias cascode	$R_1 = V_{SD14}(\text{sat})/I_{14}$ and $R_2 = V_{DS8}(\text{sat})/I_6$	
6	$GB = \frac{g_{m1}}{C_L}$	$S_1=S_2=\frac{g_{m1}^2}{K_N' I_3}=\frac{GB^2 C_L^2}{K_N' I_3}$	
7	Minimum input CM	$S_3 = \frac{2I_3}{K_N'\left(V_{in}(\min)-V_{SS}-\sqrt{\frac{I_3}{K_N' S_1}}-V_{T1}\right)^2}$	
8	Maximum input CM	$S_4 = S_5 = \frac{2I_4}{K_P'(V_{DD}-V_{in}(\max)+V_{T1})}$	S_4 and S_5 must meet or exceed the requirements of step 3
9	Differential Voltage Gain	$\frac{v_{out}}{v_{in}} = \left(\frac{g_{m1}}{2}+\frac{g_{m2}}{2(1+k)}\right)R_{out} = \left(\frac{2+k}{2+2k}\right)g_{mI}R_{out}$	
10	Power dissipation	$P_{diss} = (V_{DD}-V_{SS})(I_3+I_{12}+I_{10}+I_{11})$	

Example 6.5-3 Design of a Folded-Cascode Op Amp

Follow the above procedure to design the folded-cascode op amp when the slew rate is 10V/µs, the load capacitor is 10pF, the maximum and minimum output voltages are ±2V for ±2.5V power supplies, the *GB* is 10MHz, the minimum input common mode voltage is -1.5V and the maximum input common mode voltage is 2.5V. The differential voltage gain should be greater than 5,000V/V and the power dissipation should be less than 5mW. Use channel lengths of 1µm.

Solution

Following the approach outlined above we obtain the following results.

$$I_3 = SR \cdot C_L = 10\text{x}10^6 \cdot 10^{-11} = 100\mu A$$

Select $I_4 = I_5 = 125\mu A$.

Next, we see that the value of $0.5(V_{DD}-V_{out}(\max))$ is 0.5V/2 or 0.25V. Thus,

$$S_4 = S_5 = S_{14} = \frac{2 \cdot 125\mu A}{50\mu A/V^2 \cdot (0.25V)^2} = \frac{2 \cdot 125 \cdot 16}{50} = 80$$

and assuming worst case currents in M6 and M7 gives,

$$S_6 = S_7 = S_{13} = \frac{2 \cdot 125\mu A}{50\mu A/V^2 (0.25V)^2} = \frac{2 \cdot 125 \cdot 16}{50} = 80$$

The value of $0.5(V_{out}(\min)-|V_{SS}|)$ is also 0.25V which gives the value of S_8, S_9, S_{10} and S_{11} as

$$S_8 = S_9 = S_{10} = S_{11} = \frac{2 \cdot I_8}{K_N' V_{DS8}^2} = \frac{2 \cdot 125}{110 \cdot (0.25)^2} = 36.36$$

The value of R_1 and R_2 is equal to 0.25V/125µA or 2kΩ. In step 6, the value of *GB* gives S_1 and S_2 as

$$S_1 = S_2 = \frac{GB^2 \cdot C_L^2}{K_N' I_3} = \frac{(20\pi\text{x}10^6)^2(10^{-11})^2}{110\text{x}10^{-6} \cdot 100\text{x}10^{-6}} = 35.9$$

Example 6.5-3 - Continued

The minimum input common mode voltage defines S_3 as

$$S_3 = \frac{2I_3}{K_N'\left(V_{in}(\text{min})-V_{SS}-\sqrt{\frac{I_3}{K_N'S_1}}-V_{T1}\right)^2} = \frac{200\text{x}10^{-6}}{110\text{x}10^{-6}\left(-1.5+2.5-\sqrt{\frac{100}{110\cdot 35.9}}-0.75\right)^2} = 20$$

We need to check that the values of S_4 and S_5 are large enough to satisfy the maximum input common mode voltage. The maximum input common mode voltage of 2.5 requires

$$S_4 = S_5 \geq \frac{2I_4}{K_P'[V_{DD}-V_{in}(\text{max})+V_{T1}]} = \frac{2\cdot 125\mu\text{A}}{50\text{x}10^{-6}\mu\text{A/V}^2[0.7\text{V}]^2} = 10.2$$

which is much less than 80. In fact, with $S_4 = S_5 = 80$, the maximum input common mode voltage is 3V. Finally, S_{12}, is given as

$$S_{12} = \frac{125}{100}S_3 = 25$$

The power dissipation is found to be

$$P_{diss} = 5\text{V}(125\mu\text{A}+125\mu\text{A}+125\mu\text{A}) = 1.875\text{mW}$$

The small-signal voltage gain requires the following values to evaluate:

S_4, S_5, S_{13}, S_{14}: $g_m = \sqrt{2\cdot 125\cdot 50\cdot 80} = 1000\mu\text{S}$ and $g_{ds} = 125\text{x}10^{-6}\cdot 0.05 = 6.25\mu\text{S}$

S_6, S_7: $g_m = \sqrt{2\cdot 75\cdot 50\cdot 80} = 774.6\mu\text{S}$ and $g_{ds} = 75\text{x}10^{-6}\cdot 0.05 = 3.75\mu\text{S}$

S_8, S_9, S_{10}, S_{11}: $g_m = \sqrt{2\cdot 75\cdot 110\cdot 36.36} = 774.6\mu\text{S}$ and $g_{ds} = 75\text{x}10^{-6}\cdot 0.04 = 3\mu\text{S}$

S_1, S_2: $g_{mI} = \sqrt{2\cdot 50\cdot 110\cdot 35.9} = 628\mu\text{S}$ and $g_{ds} = 50\text{x}10^{-6}(0.04) = 2\mu\text{S}$

Example 6.5-3 - Continued

Thus,

$$R_{II} \approx g_{m9}r_{ds9}r_{ds11} = (774.6\mu\text{S})\left(\frac{1}{3\mu\text{S}}\right)\left(\frac{1}{3\mu\text{S}}\right) = 86.07\text{M}\Omega$$

$$R_{out} \approx 86.07\text{M}\Omega \,||\, (774.6\mu\text{S})\left(\frac{1}{3.75\mu\text{S}}\right)\left(\frac{1}{2\mu\text{S}+6.25\mu\text{S}}\right) = 19.40\text{M}\Omega$$

$$k = \frac{R_{II}(g_{ds2}+g_{ds4})}{g_{m7}r_{ds7}} = \frac{86.07\text{M}\Omega(2\mu\text{S}+6.25\mu\text{S})(3.75\mu\text{S})}{774.6\mu\text{S}} = 3.4375$$

The small-signal, differential-input, voltage gain is

$$A_{vd} = \left(\frac{2+k}{2+2k}\right)g_{mI}R_{out} = \left(\frac{2+3.4375}{2+6.875}\right)0.628\text{x}10^{-3}\cdot 19.40\text{x}10^{6} = 7{,}464 \text{ V/V}$$

The gain is larger than required by the specifications which should be okay.

Comments on Folded Cascode Op Amps

- Good PSRR
- Good ICMR
- Self compensated
- Can cascade an output stage to get extremely high gain with lower output resistance (use Miller compensation in this case)
- Need first stage gain for good noise performance
- Widely used in telecommunication circuits where large dynamic range is required

SECTION 6.6 - SIMULATION AND MEASUREMENT OF OP AMPS

Simulation and Measurement Considerations

Objectives:

- The objective of simulation is to verify and optimize the design.
- The objective of measurement is to experimentally confirm the specifications.

Similarity Between Simulation and Measurement:

- Same goals
- Same approach or technique

Differences Between Simulation and Measurement:

- Simulation can idealize a circuit
- Measurement must consider all nonidealities

Simulating or Measuring the Open-Loop Transfer Function of the Op Amp

Circuit (Darkened op amp identifies the op amp under test):

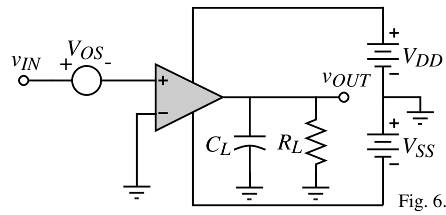


Fig. 6.6-1

Simulation:

This circuit will give the voltage transfer function curve. This curve should identify:

1.) The linear range of operation
2.) The gain in the linear range
3.) The output limits
4.) The systematic input offset voltage
5.) DC operating conditions, power dissipation
6.) When biased in the linear range, the small-signal frequency response can be obtained
7.) From the open-loop frequency response, the phase margin can be obtained (F = 1)

Measurement:

This circuit probably will not work unless the op amp gain is very low.

A More Robust Method of Measuring the Open-Loop Frequency Response

Circuit:

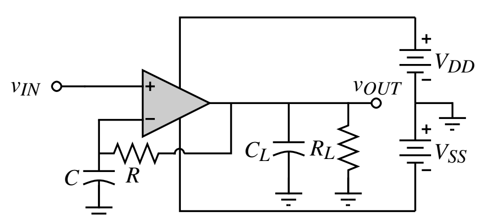


Fig. 6.6-2A

Resulting Closed-Loop Frequency Response:

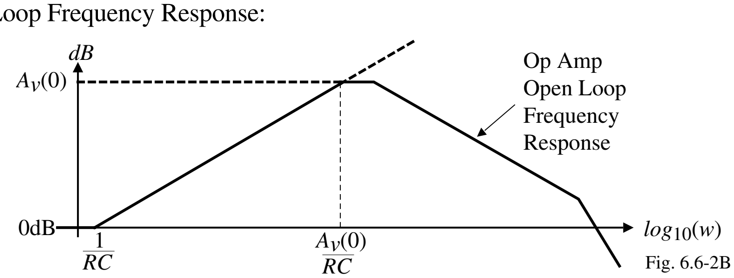


Fig. 6.6-2B

Make the RC product as large as possible.

Example 6.6-1 – Measurement of the Op Amp Open-Loop Gain

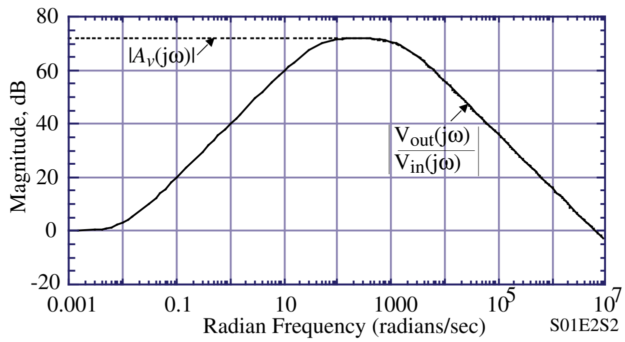
Develop the closed-loop frequency response for op amp circuit shown which is used to measure the open-loop frequency reasponse. Sketch the closed-loop frequency response of the magnitude of V_{out}/V_{in} if the low frequency gain is 4000 V/V, the GB = 1MHz, R = 10MΩ, and C = 10μF. (Ignore R_L and C_L)

Solution

The open-loop transfer function of the op amp is,

$$A_v(s) = \frac{GB}{s + (GB/A_v(0))} = \frac{2\pi \text{x} 10^6}{s + 500\pi}$$

The closed-loop transfer function of the op amp can be expressed as,



$$v_{OUT} = A_v(s)\left[\left(\frac{-1/sC}{R+(1/sC)}\right)v_{OUT} + v_{IN}\right]$$

$$= A_v(s)\left[\left(\frac{-1/RC}{s+(1/RC)}\right)v_{OUT} + v_{IN}\right]$$

$$\therefore \quad \frac{v_{OUT}}{v_{IN}} = \frac{-[s + (1/RC)]A_v(s)}{s + (1/RC) + A_v(s)/RC}$$

$$= \frac{-[s + (1/RC)]}{\frac{s + (1/RC)}{A_v(s)} + 1/RC} = \frac{-(s + 0.01)}{\frac{s + 0.01}{A_v(s)} + 0.01}$$

Substituting, $A_v(s)$ gives,

$$\frac{v_{OUT}}{v_{IN}} = \frac{-2\pi \text{x} 10^6 s - 2\pi \text{x} 10^4}{(s+0.01)(s+500\pi) + 2\pi \text{x} 10^4} = \frac{-2\pi \text{x} 10^6 s - 2\pi \text{x} 10^4}{s^2 + 500\pi s + 2\pi \text{x} 10^4} = \frac{-2\pi \text{x} 10^6 (s + 0.01)}{(s+41.07)(s+1529.72)}$$

The magnitude of the closed-loop frequency response is plotted above.

Simulation and Measurement of Open-Loop Frequency Response with Moderate Gain Op Amps

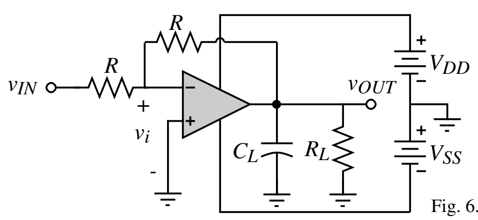


Fig. 6.6-3

Make R as large and measure v_{out} and v_i to get the open loop gain.

Simulation or Measurement of the Input Offset Voltage of an Op Amp

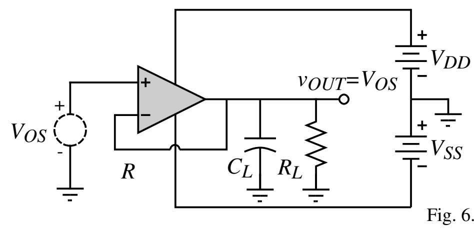


Fig. 6.6-4

Types of offset voltages:

1.) Systematic offset - due to mismatches in current mirrors, exists even with ideally matched transistors.

2.) Mismatch offset - due to mismatches in transistors (normally not available in simulation except through Monte Carlo methods).

Simulation of the Common-Mode Voltage Gain

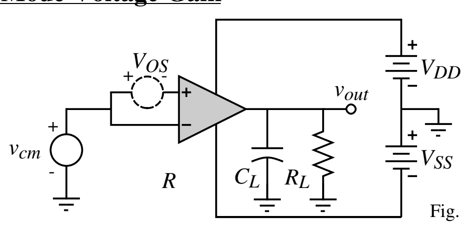


Fig. 6.6-5

Make sure that the output voltage of the op amp is in the linear region.

Measurement of *CMRR* and *PSRR*

Configuration:

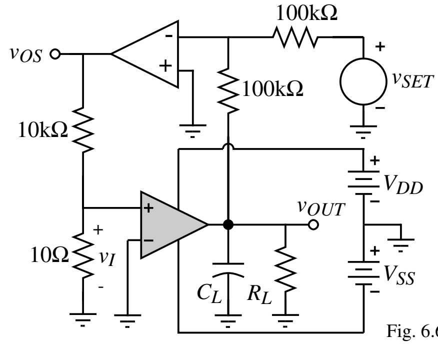


Fig. 6.6-6

Note that $v_I \approx \frac{v_{OS}}{1000}$ or $v_{OS} \approx 1000 v_I$

<u>How Does this Circuit Work?</u>

CMRR:

1.) Set
$V_{DD}' = V_{DD} + 1V$
$V_{SS}' = V_{SS} + 1V$
$v_{OUT}' = v_{OUT} + 1V$

2.) Measure v_{OS} called v_{OS1}

3.) Set
$V_{DD}' = V_{DD} - 1V$
$V_{SS}' = V_{SS} - 1V$
$v_{OUT}' = v_{OUT} - 1V$

4.) Measure v_{OS} called v_{OS2}

5.) $\text{CMRR} = \frac{2000}{|v_{OS2} - v_{OS1}|}$

PSRR:

1.) Set
$V_{DD}' = V_{DD} + 1V$
$V_{SS}' = V_{SS}$
$v_{OUT}' = 0V$

2.) Measure v_{OS} called v_{OS3}

3.) Set
$V_{DD}' = V_{DD} - 1V$
$V_{SS}' = V_{SS}$
$v_{OUT}' = 0V$

4.) Measure v_{OS} called v_{OS4}

5.) $\text{PSRR}^+ = \frac{2000}{|v_{OS4} - v_{OS3}|}$

Note:

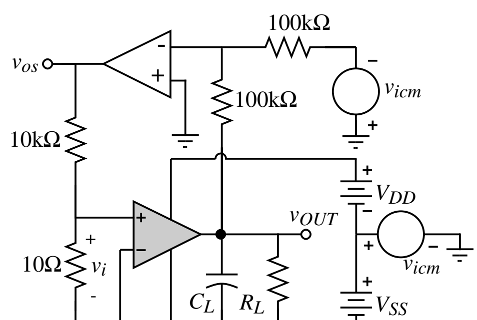
1.) PSRR^- can be measured similar to PSRR^+ by changing only V_{SS}.

2.) The ±1V perturbation can be replaced by a sinusoid to measure CMRR or PSRR as follows:

$$\text{PSRR}^+ = \frac{1000 \cdot v_{dd}}{v_{os}},\ \text{PSRR}^- = \frac{1000 \cdot v_{ss}}{v_{os}},\ \text{and CMRR} = \frac{1000 \cdot v_{cm}}{v_{os}}$$

How Does the Previous Idea Work?

A circuit is shown which is used to measure the *CMRR* and *PSRR* of an op amp. Prove that the *CMRR* can be given as



S99FEP7

$$CMRR = \frac{1000\ v_{icm}}{v_{os}}$$

<u>Solution</u>

The definition of the common-mode rejection ratio is

$$CMRR = \left|\frac{A_{vd}}{A_{cm}}\right| = \frac{\frac{v_{out}}{v_{id}}}{\frac{v_{out}}{v_{icm}}}$$

However, in the above circuit the value of v_{out} is the same so that we get

$$CMRR = \frac{v_{icm}}{v_{id}}$$

But $v_{id} = v_i$ and $v_{os} \approx 1000 v_i = 1000 v_{id}$ $\Rightarrow$ $v_{id} = \frac{v_{os}}{1000}$

Substituting in the previous expression gives,

$$CMRR = \frac{v_{icm}}{\frac{v_{os}}{1000}} = \frac{1000\ v_{icm}}{v_{os}}$$

Simulation of CMRR of an Op Amp

None of the above methods are really suitable for simulation of *CMRR*.

Consider the following:

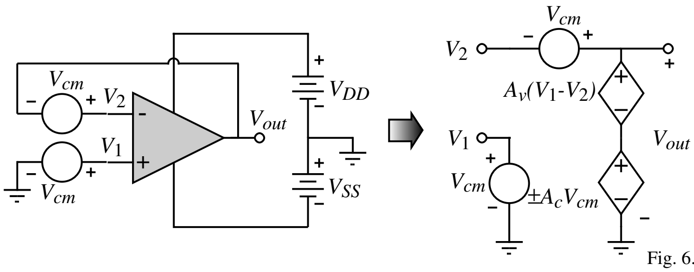


Fig. 6.6-7

$$V_{out} = A_v(V_1-V_2) \pm A_{cm}\left(\frac{V_1+V_2}{2}\right) = -A_v V_{out} \pm A_{cm}V_{cm}$$

$$V_{out} = \frac{\pm A_{cm}}{1+A_v}V_{cm} \approx \frac{\pm A_{cm}}{A_v}V_{cm}$$

$$\therefore \quad \boxed{|CMRR| = \frac{A_v}{A_{cm}} = \frac{V_{cm}}{V_{out}}}$$

***CMRR* of Ex. 6.3-1 using the Above Method of Simulation**

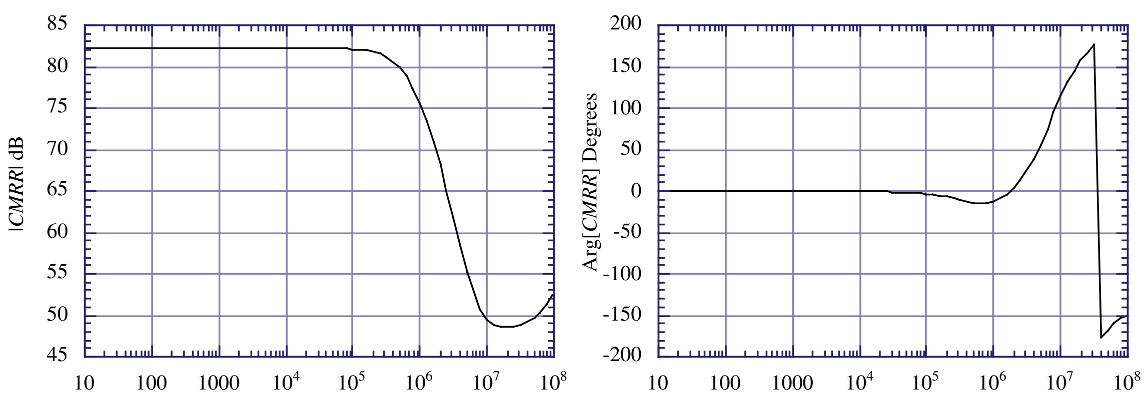


Fig. 6.6-8

Direct Simulation of *PSRR*

Circuit:

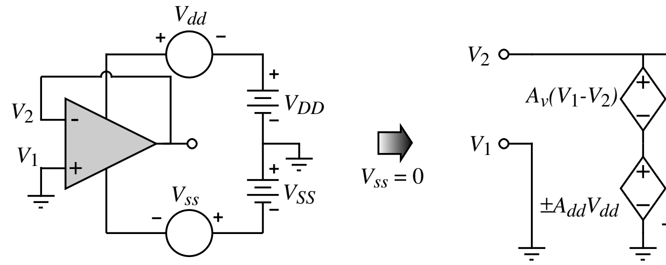


Fig. 6.6-9

$$V_{out} = A_v(V_1-V_2) \pm A_{dd}V_{dd} = -A_vV_{out} \pm A_{dd}V_{dd}$$

$$V_{out} = \frac{\pm A_{dd}}{1+A_v}V_{dd} \approx \frac{\pm A_{dd}}{A_v}V_{dd}$$

$$\therefore \quad \boxed{PSRR^+ = \frac{A_v}{A_{dd}} = \frac{V_{dd}}{V_{out}}} \quad \text{and} \quad \boxed{PSRR^- = \frac{A_v}{A_{ss}} = \frac{V_{ss}}{V_{out}}}$$

Works well as long as *CMRR* is much greater than 1.

Simulation or Measurement of *ICMR*

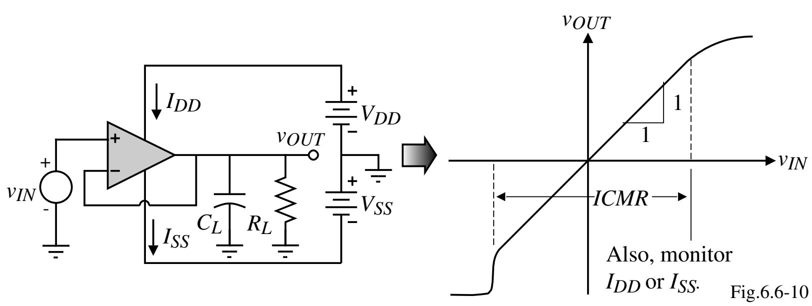


Fig.6.6-10

Initial jump in sweep is due to the turn-on of M5.

Should also plot the current in the input stage (or the power supply current).

Measurement or Simulation of the Open-Loop Output Resistance

Method 1:

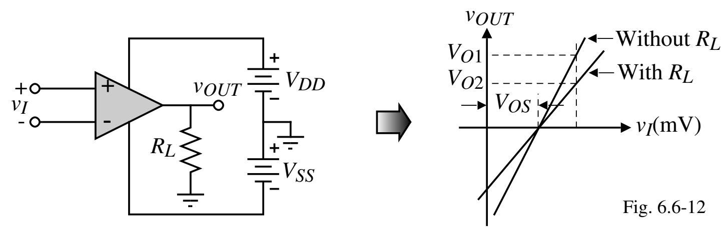


Fig. 6.6-12

$$R_{\text{out}} = R_L\left(\frac{V_{01}}{V_{02}} - 1\right)$$ or vary R_L until $V_{O2} = 0.5V_{O1} \Rightarrow R_{out} = R_L$

Method 2:

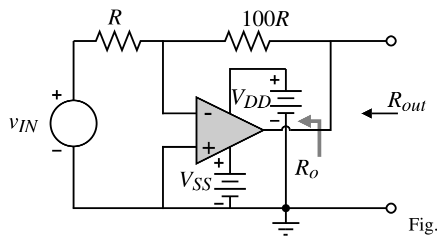


Fig. 6.6-13

$$R_{\text{out}} = \left(\frac{1}{R_o} + \frac{1}{100R} + \frac{A_v}{100R_o}\right)^{-1} \cong \frac{100R_o}{A_v}$$

Measurement or Simulation of Slew Rate and Settling Time

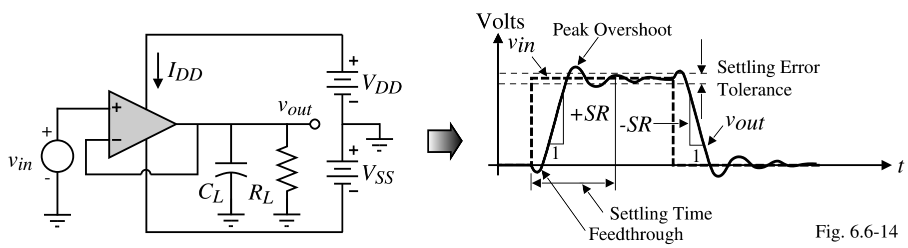


Fig. 6.6-14

If the slew rate influences the small signal response, then make the input step size small enough to avoid slew rate (i.e. less than 0.5V for MOS).

Measurement of Phase Margin from Overshoot

It can be shown (Appendix C) that:

$$\text{Phase Margin (Degrees)} = 57.2958\cos^{-1}\left[\sqrt{4\zeta^4+1} - 2\zeta^2\right]$$

$$\text{Overshoot (\%)} = 100\, exp\left(\frac{-\pi\zeta}{\sqrt{1-\zeta^2}}\right)$$

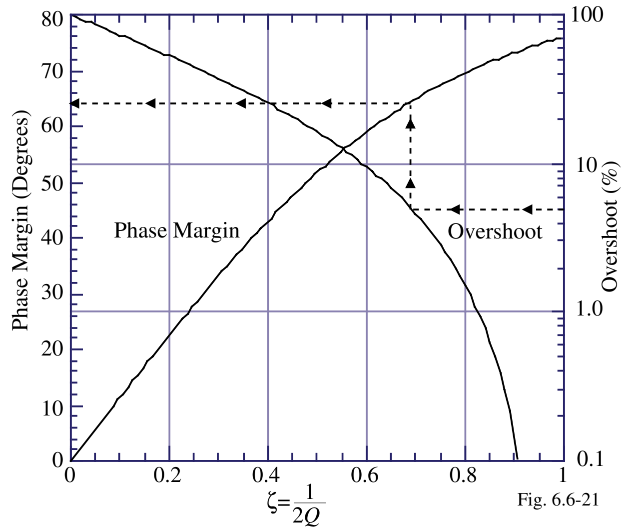


Fig. 6.6-21

For example, a 5% overshoot corresponds to a phase margin of approximately 64°.

Example 6.6-2 Simulation of the CMOS Op Amp of Ex. 6.3-1.

The op amp designed in Example 6.3-1 and shown in Fig. 6.3-3 is to be analyzed by SPICE to determine if the specifications are met. The device parameters to be used are those of Tables 3.1-2 and 3.2-1. In addition to verifying the specifications of Example 6.3-1, we will simulate $PSRR^+$ and $PSRR^-$.

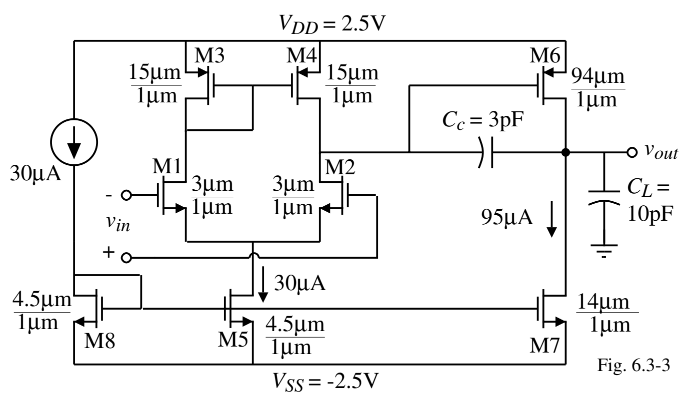


Fig. 6.3-3

Solution/Simulation

The op amp will be treated as a subcircuit in order to simplify the repeated analyses. Table 6.6-1 gives the SPICE subcircuit description of Fig. 6.3-3. While the values of *AD, AS, PD,* and *PS* could be calculated if the physical layout was complete, we will make an educated estimate of these values by using the following approximations.

$$AS = AD \cong W[L1 + L2 + L3]$$

$$PS = PD \cong 2W + 2[L1 + L2 + L3]$$

where $L1$ is the minimum allowable distance between the polysilicon and a contact in the moat (Rule 5C of Table 2.6-1), $L2$ is the length of a minimum-size square contact to moat (Rule 5A of Table 2.6-1), and $L3$ is the minimum allowable distance between a contact to moat and the edge of the moat (Rule 5D of Table 2.6-1).

Example 6.6-2 - Continued

Op Amp Subcircuit:

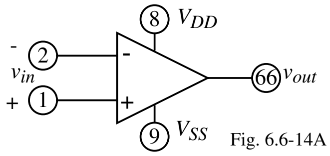


Fig. 6.6-14A

```
.SUBCKT OPAMP 1 2 6 8 9
M1 4 2 3 3 NMOS1 W=3U L=1U AD=18P AS=18P PD=18U PS=18U
M2 5 1 3 3 NMOS1 W=3U L=1U AD=18P AS=18P PD=18U PS=18U
M3 4 4 8 8 PMOS1 W=15U L=1U AD=90P AS=90P PD=42U PS=42U
M4 5 4 8 8 PMOS1 W=15U L=1U AD=90P AS=90P PD=42U PS=42U
M5 3 7 9 9 NMOS1 W=4.5U L=1U AD=27P AS=27P PD=21U PS=21U
M6 6 5 8 8 PMOS1 W=94U L=1U AD=564P AS=564P PD=200U PS=200U
M7 6 7 9 9 NMOS1 W=14U L=1U AD=84P AS=84P PD=40U PS=40U
M8 7 7 9 9 NMOS1 W=4.5U L=1U AD=27P AS=27P PD=21U PS=21U
CC 5 6 3.0P
.MODEL NMOS1 NMOS VTO=0.70 KP=110U GAMMA=0.4 LAMBDA=0.04 PHI=0.7
+MJ=0.5 MJSW=0.38 CGBO=700P CGSO=220P CGDO=220P CJ=770U CJSW=380P
+LD=0.016U TOX=14N
.MODEL PMOS1 PMOS VTO=-0.7 KP=50U GAMMA=0..57 LAMBDA=0.05 PHI=0.8
+MJ=0.5 MJSW=.35 CGBO=700P CGSO=220P CGDO=220P CJ=560U CJSW=350P +LD=0.014U TOX=14N
IBIAS 8 7 30U
.ENDS
```


Example 6.6-2 - Continued

PSPICE Input File for the Open-Loop Configuration:

```
EXAMPLE 6.6-2 OPEN LOOP CONFIGURATION
.OPTION LIMPTS=1000
VIN+ 1 0 DC 0 AC 1.0
VDD 4 0 DC 2.5
VSS 0 5 DC 2.5
VIN - 2 0 DC 0
CL 3 0 10P
X1 1 2 3 4 5 OPAMP
         :
(Subcircuit of previous slide)
         :
.OP
.TF V(3) VIN+
.DC VIN+ -0.005 0.005 100U
.PRINT DC V(3)
.AC DEC 10 1 10MEG
.PRINT AC VDB(3) VP(3)
.PROBE      (This entry is unique to PSPICE)
.END
```

Example 6.6-2 - Continued

Open-loop transfer characteristic of Example 6.6-2:

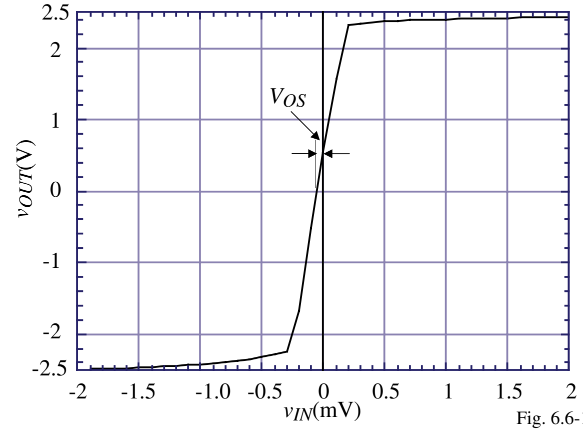


Fig. 6.6-15B

Example 6.6-2 - Continued

Open-loop transfer frequency response of Example 6.3-1:

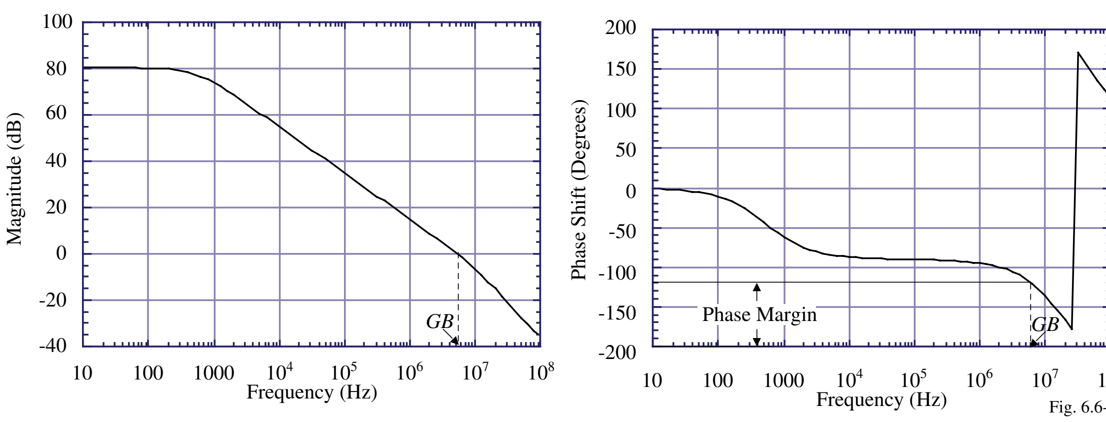


Fig. 6.6-16B

Example 6.6-2 - Continued

Input common mode range of Example 6.3-1:

```
EXAMPLE 6.6-2 UNITY GAIN CONFIGURATION.
.OPTION LIMPTS=501
VIN+ 1 0 PWL(0 -2 10N -2 20N 2 2U 2 2.01U -2 4U  -2 4.01U
+ -.1 6U -.1 6.0 1U .1 8U .1 8.01U -.1  10U -.1)
VDD 4 0 DC 2.5 AC 1.0
VSS 0 5 DC 2.5
CL 3 0 20P
X1 1 3 3 4 5 OPAMP
         :
(Subcircuit of Table 6.6-1)
         :
.DC VIN+ -2.5 2.5  0.1
.PRINT DC V(3)
.TRAN 0.05U 10U 0 10N
.PRINT TRAN V(3) V(1)
.AC DEC 10 1 10MEG
.PRINT AC VDB(3) VP(3)
.PROBE   (This entry is unique to PSPICE)
.END
```

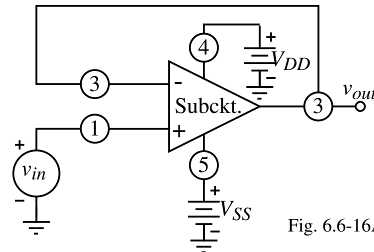


Fig. 6.6-16A

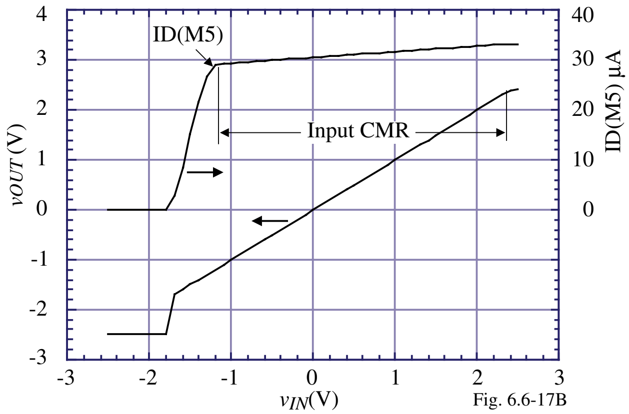


Fig. 6.6-17B

Example 6.6-2 - Continued

Positive *PSRR* of Example 6.3-1:

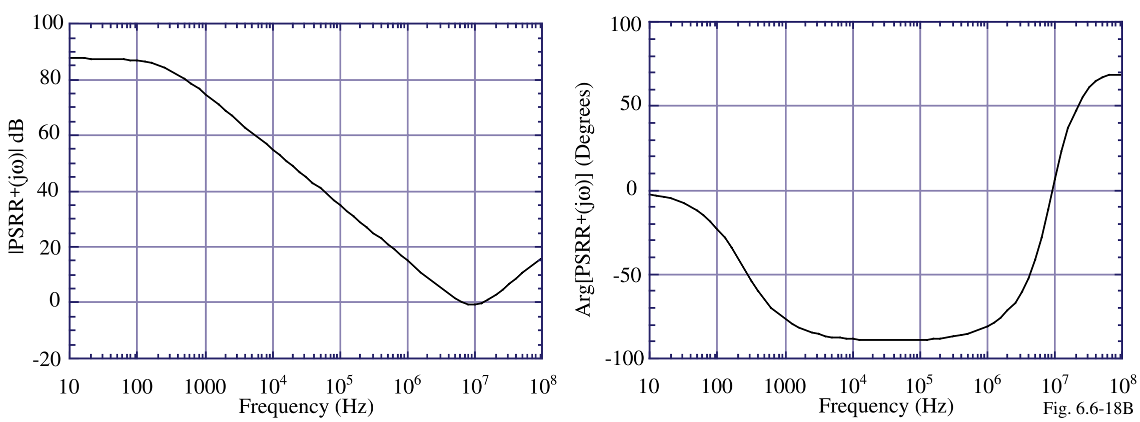


Fig. 6.6-18B

Example 6.6-2 - Continued

Negative *PSRR* of Example 6.3-1:

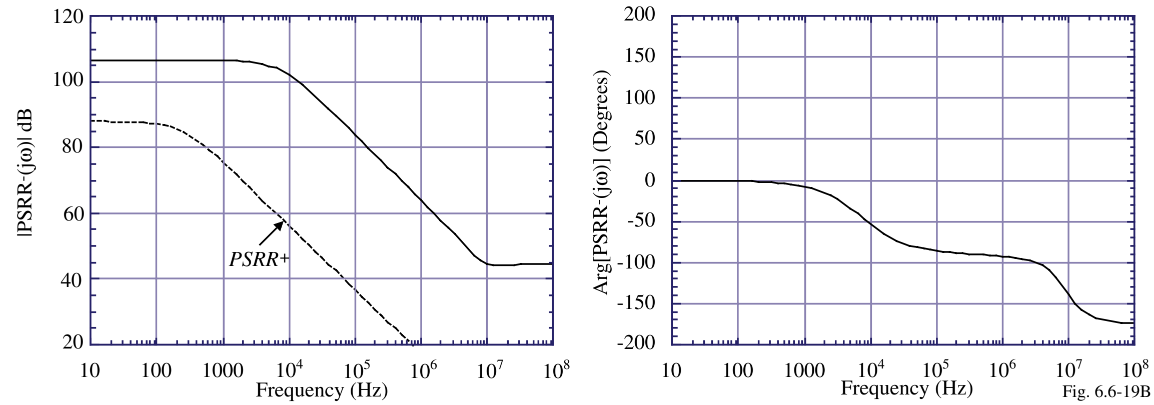


Fig. 6.6-19B

Example 6.6-2 - Continued

Large-signal and small-signal transient response of Example 6.3-1:

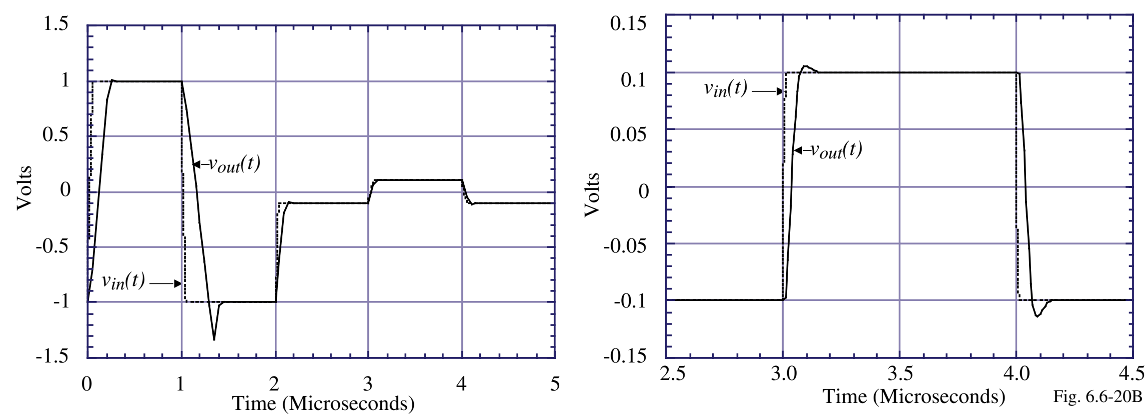


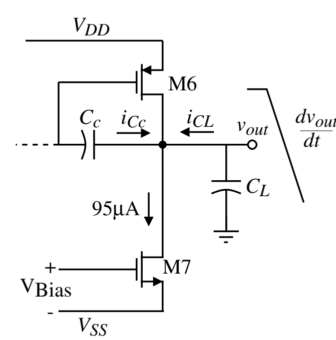
Fig. 6.6-20B

Why the negative overshoot on the slew rate?

If the current sink, M7, cannot sink sufficient current then the output stage is slewing and it can only respond to changes at the output via the external feedback path to the input of the amplifier which involves a delay.

Note that $-dv_{out}/dt \approx -2\text{V}/0.3\mu\text{s} = -6.67\text{V}/\mu\text{s}$. For a 10pF capacitor this requires 66.7μA and only 95μA-66.7μA = 28μA is available for C_c.

For the positive slew rate, M6 can provide whatever current is required by the capacitors and can immediately respond to changes at the output.



Example 6.6-2 - Continued

Comparison of the Simulation Results with the Specifications of Example 6.3-1:

Specification (Power supply = ±2.5V)	Design (Ex. 6.3-1)	Simulation (Ex. 6.6-2)
Open Loop Gain	>5000	10,000
GB (MHz)	5 MHz	5 MHz
Input CMR (Volts)	-1V to 2V	-1.2 V to 2.4 V,
Slew Rate (V/μsec)	>10 (V/μsec)	+10, -7(V/μsec)
P_{diss} (mW)	< 2mW	0.625mW
V_{out} range (V)	±2V	+2.3V, -2.2V
$PSRR^+$ (0) (dB)	-	87
$PSRR^-$ (0) (dB)	-	106
Phase margin (degrees)	60°	65°
Output Resistance (kΩ)	-	122.5kΩ

Example 6.6-3

Why is the negative-going overshoot larger than the positive-going overshoot on the small-signal transient response of Example 6.6-2 (right-hand figure of page 6.6-24)?

Solution

Consider the following circuit and waveform:

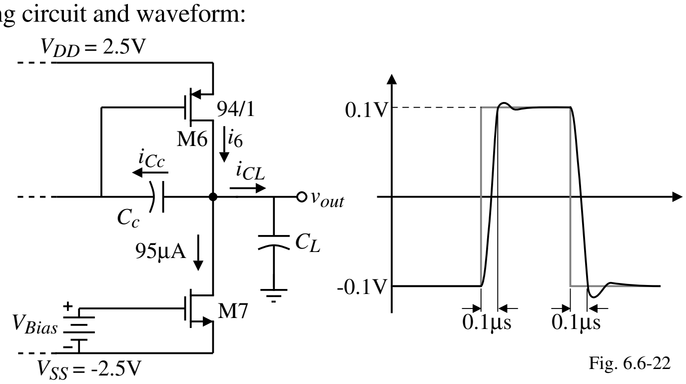


Fig. 6.6-22

During the rise time, $i_{CL} = C_L(dv_{out}/dt)$= 10pF(0.2V/0.1µs) = 20µA and i_{Cc} = 3pf(2V/µs) = 6µA

$\therefore$ i_6 = 95µA + 20µA + 6µA = 121µA $\Rightarrow$ g_{m6} = 1066µS (nominal was 942.5µS)

During the fall time, $i_{CL} = C_L(-dv_{out}/dt)$= 10pF(-0.2V/0.1µs) = -20µA and i_{Cc} = -3pf(2V/µs) = -6µA

$\therefore$ i_6 = 95µA - 20µA - 6µA = 69µA $\Rightarrow$ g_{m6} = 805µS

The dominant pole is $p_1 \approx (R_I g_{m6} R_{II} C_c)^{-1}$ where R_I = 0.694MΩ, R_{II} = 122.5kΩ and C_c = 3pF.

$\therefore$ p_1(95µA) = 4,160 rads/sec, p_1(121µA) = 3,678 rads/sec, and p_1(69µA) = 4,870 rads/sec.

Thus, the phase margin is less during the fall time than the rise time.

SECTION 6.7 - MACROMODELS FOR OP AMPS

Macromodel

A *macromodel* is a model that captures some or all of the performance of a circuit using different components (generally simpler).

A *macromodel* uses resistors, capacitors, inductors, controlled sources, and some active devices (mostly diodes) to capture the essence of the performance of a complex circuit like an op amp without modeling every internal component of the op amp.

Op Amp Characterization

- Small signal, frequency independent
- Small signal, frequency dependent
- Large signal

    Time independent

    Time dependent

Small Signal, Frequency Independent, Op Amp Models

Simple Model

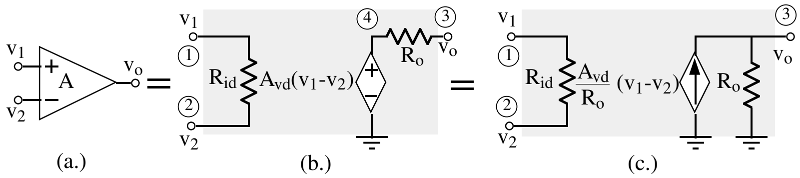


Figure 6.7-1 - (a.) Op amp symbol. (b.) Thevenin form of simple model. (c.) Norton form of simple model.

SPICE Description of Fig. 6.7-1c

```
RID 1 2 {Rid}
RO 3 0 {Ro}
GAVD 0 3 1 2 {Avd/Ro}
```

Subcircuit SPICE Description for Fig. 6.7-1c

```
.SUBCKT SIMPLEOPAMP 1 2 3
RID 1 2 {Rid}
RO 3 0 {Ro}
GAVD 0 3 1 2 {Avd/Ro}
.ENDS SIMPLEOPAMP
```


Example 6.7-1 - Use of the Simple Op Amp Model

Use SPICE to find the voltage gain, v_{out}/v_{in}, the input resistance, R_{in}, and the output resistance, R_{out} of Fig. 6.7-2. The op amp parameters are A_{vd} = 100,000, R_{id} = 1MΩ, and R_o = 100Ω. We want to find the input resistance, R_{in}, the output resistance, R_{out}, and the voltage gain, A_v, of the noninverting voltage amplifier configuration when R_1 = 1kΩ and R_2 = 100kΩ.

Solution

The circuit with the SPICE node numbers is shown in Fig. 6.7-2.

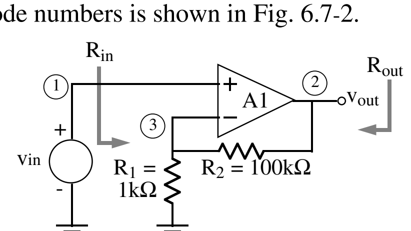


Figure 6.7-2 - Noninverting voltage amplifier for Ex. 6.7-1.

The input file for this example is given as follows.

```
Example 6.7-1
VIN 1 0 DC 0 AC 1
XOPAMP1 1 3 2 SIMPLEOPAMP
R1 3 0 1KOHM
R2 2 3 100KOHM
.SUBCKT SIMPLEOPAMP 1 2 3
RID 1 2 1MEGOHM
RO 3 0 100OHM
GAVD/RO 0 3 1 2 1000
.ENDS SIMPLEOPAMP
.TF V(2) VIN
.END
```

The command .TF finds the small signal input resistance, output resistance, and voltage or current gain of an amplifier. The results extracted from the output file are:

```
****    SMALL-SIGNAL CHARACTERISTICS
        V(2)/VIN =  1.009E+02
        INPUT RESISTANCE AT VIN =  9.901E+08
      OUTPUT RESISTANCE AT V(2) =  1.010E-01.
```

Common Mode Model

Electrical Model:

$$v_o = A_{vd}(v_1 - v_2) + \frac{A_{cm}}{R_o}\left(\frac{v_1+v_2}{2}\right)$$

Macromodel:

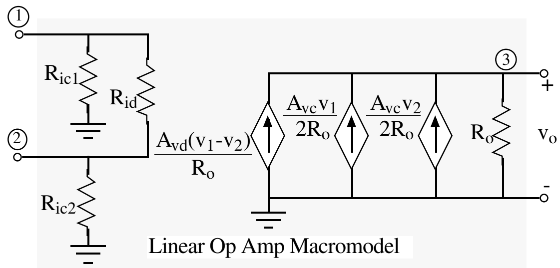


Figure 6.7-3 - Simple op amp model including differential and common mode behavior.

SPICE File:

```
.SUBCKT LINOPAMP 1 2 3
RIC1 1 0 {Ric}
RID 1 2 {Rid}
RIC2 2 0 {Ric}
GAVD/RO 0 3 1 2 {Avd/Ro}
GAVC1/RO 0 3 1 0 {Avc/2Ro}
GAVC2/RO 0 3 2 0 {Avc/2Ro}
RO 3 0 {Ro}
.ENDS LINOPAMP
```

PARAM OPTION

```
.SUBCKT LINOPAMP 1 2 3 PARAM:
RICRES=100MEG, RIDRES=1MEG,
+ AVD/RO=10K, AVC/RO=1, RORES=100
RIC1 1 0 RICRES
RID 1 2 RIDRES
RIC2 2 0 RICRES
GAVD/RO 0 3 1 2 AVD/RO
GAVC1/RO 0 3 1 0 AVC/RO
GAVC2/RO 0 3 2 0 AVC/RO
RO 3 0 RORES
.ENDS LINOPAMP
```


Small Signal, Frequency Dependent Op Amp Models

Dominant Pole Model

$$A_{vd}(s) = \frac{A_{vd}(0)}{(s/\omega_1)} + 1) \quad \text{where } \omega_1 = \frac{1}{R_1C_1} \text{ (dominant pole)}$$

Model Using Passive Components

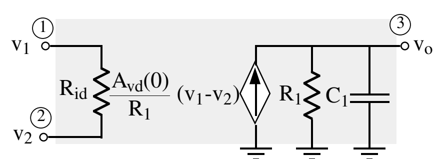


Figure 6.7-4 - Macromodel for the op amp including the frequency response of A_{vd}.

Model Using Passive Components with Constant Output Resistance

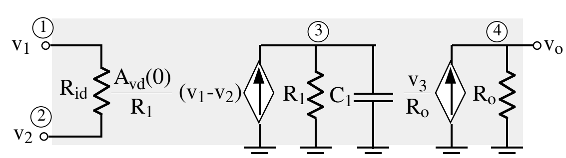


Figure 6.7-5 - Frequency dependent model with constant output resistance.

Example 6.7-2 - Frequency Response of the Noninverting Voltage Amplifier

Use the model of Fig. 4 to find the frequency response of Fig. 6.7-2 if the gain is +1, +10, and +100 V/V assuming that $A_{vd}(0) = 10^5$ and $\omega_1 = 100$ rads/sec.

Solution

The parameters of the model are $R_2/R_1 = 0$, 9, and 99. Let us additionally select $R_{id} = 1M\Omega$ and $R_o = 100\Omega$. We will use the circuit of Fig. 2 and insert the model as a subcircuit. The input file for this example is shown below.

```
Example 6.7-2
VIN 1 0 DC 0 AC 1
*Unity Gain Configuration
XOPAMP1 1 31 21 LINFREQOPAMP
R11 31 0 15GOHM
R21 21 31 1OHM
*Gain of 10 Configuration
XOPAMP2 1 32 22 LINFREQOPAMP
R12 32 0 1KOHM
R22 22 32 9KOHM
*Gain of 100 Configuration
XOPAMP3 1 33 23 LINFREQOPAMP
R13 33 0 1KOHM
R23 23 33 99KOHM
.SUBCKT LINFREQOPAMP 1 2 3
RID 1 2 1MEGOHM
GAVD/RO 0 3 1 2 1000
R1 3 0 100
C1 3 0 100UF
.ENDS
.AC DEC 10 100 10MEG
.PRINT AC V(21) V(22) V(23)
.PROBE
.END
```


Example 6.7-2 - Continued

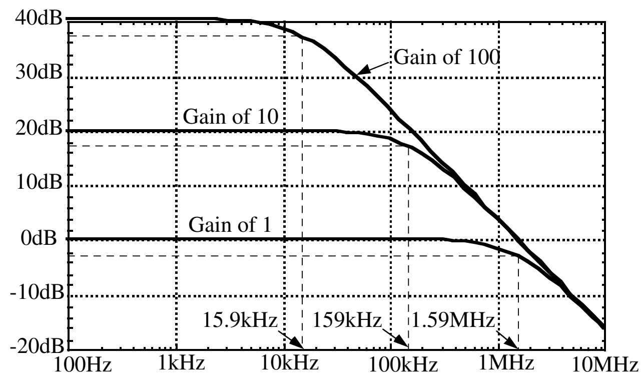


Figure 6.7-6 - Frequency response of the 3 noninverting voltage amplifiers of Ex. 6.7-2.

Behavioral Frequency Model

Use of Laplace behavioral modeling capability in PSPICE.

GAVD/RO 0 3 LAPLACE {V(1,2)} = {1000/(0.01s+1)}.

Implements,

$$G_{Avd/Ro} = \frac{A_{vd}(s)}{R_o} = \frac{\frac{A_{vd}(0)}{R_o}}{\frac{s}{\omega_1} + 1}$$

where $A_{vd}(0)$ = 100,000, R_o = 100Ω, and ω_1 = 100 rps

Differential and Common Mode Frequency Dependent Models

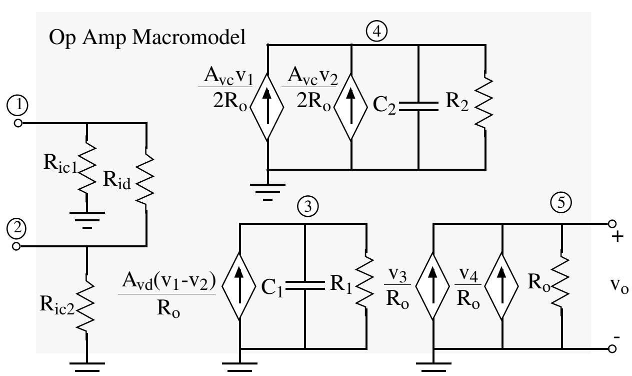
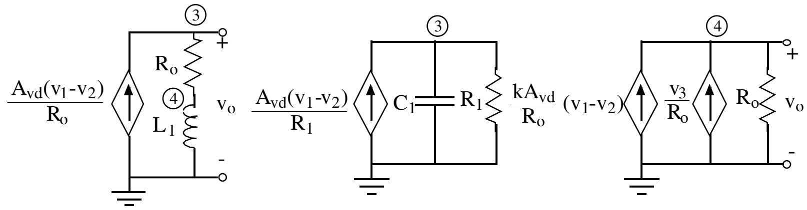


Figure 6.7-7 - Op amp macromodel for separate differential and common voltage gain frequency responses.

Zeros in the Transfer Function

Models:



(a.) (b.)

Figure 6.7-8 - (a.) Independent zero model. (b.) Method of modeling zeros without introducing new nodes.

Inductor:

$$V_o(s) = \left(\frac{A_{vd}(0)}{R_o}\right)(sL_1 + R_o)\ [V_1(s)\text{-}V_2(s)] = A_{vd}(0)\left(\frac{s}{R_o/L_1} + 1\right)[V_1(s)\text{-}V_2(s)]\ .$$

Feedforward:

$$V_o(s) = \left(\frac{A_{vd}(0)}{(s/\omega_1)+1}\right)\left[1+k(s/\omega_1)+k\right]\ [V_1(s)\text{-}V_2(s)]\ .$$

The zero can be expressed as

$$z_1 = -\omega_1\left(1 + \frac{1}{k}\right)$$

where k can be + or - by reversing the direction of the current source.

Example 6.7-3 - Modeling Zeros in the Op Amp Frequency Response

Use the technique of Fig. 8b to model an op amp with a differential voltage gain of 100,000, a pole at 100rps, an output resistance of 100Ω, and a zero in the right-half, complex frequency plane at 10^7 rps.

Solution

The transfer function we want to model is given as

$$V_o(s) = \frac{10^5(s/10^7 - 1)}{(s/100 + 1)}\ .$$

Let us arbitrarily select R_1 as 100kΩ which will make the GAVD/R1 gain unity. To get the pole at 100rps, $C_1 = 1/(100R_1) = 0.1\mu F$. Next, we want z_1 to be 10^7 rps. Since $\omega_1 = 100$rps, then Eq. (6) gives k as -10^{-5}. The following input file verifies this model.

```
Example 6.7-3
VIN 1 0 DC 0 AC 1
XOPAMP1 1 0 2 LINFREQOPAMP
.SUBCKT LINFREQOPAMP 1 2 4
RID 1 2 1MEGOHM
GAVD/R1 0 3 1 2 1
R1 3 0 100KOHM
C1 3 0 0.1UF
GV3/RO 0 4 3 0 0.01
GAVD/RO 4 0 1 2 0.01
RO 4 0 100
.ENDS
.AC DEC 10 1 100MEG
.PRINT AC V(2) VDB(2) VP(2)
.PROBE
.END
```

Example 6.7-3 - Continued

The asymptotic magnitude frequency response of this simulation is shown in Fig. 6.7-9. We note that although the frequency response is plotted in Hertz, there is a pole at 100rps (15.9Hz) and a zero at 1.59MHz (10Mrps). Unless we examined the phase shift, it is not possible to determine whether the zero is in the RHP or LHP of the complex frequency axis.

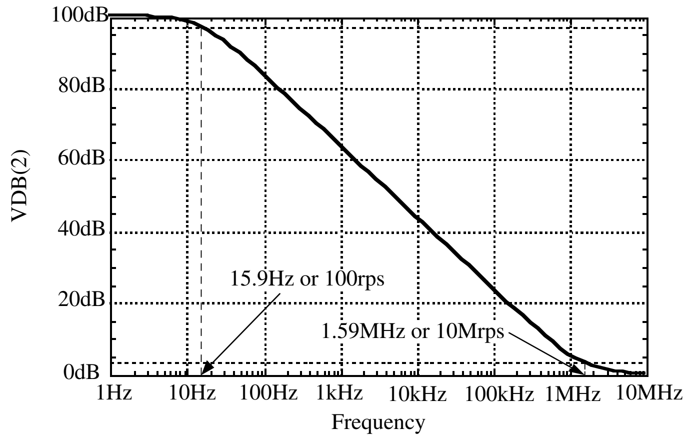


Figure 6.7-9 - Asymptotic magnitude frequency response of the op amp model of Ex. 6.7-3.

Large Signal Macromodels for the Op Amp

Output and Input Voltage Limitations

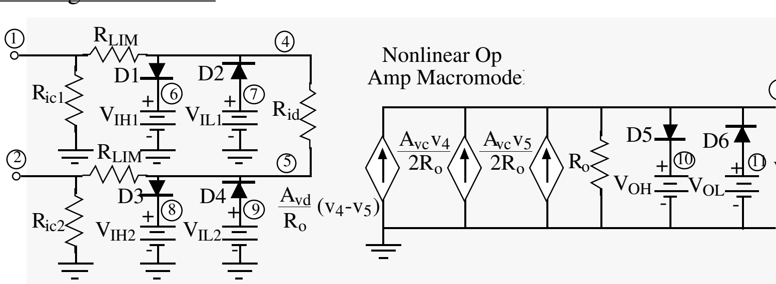


Figure 6.7-10 - Op amp macromodel that limits the input and output voltages.

Subcircuit Description

```
.SUBCKT NONLINOPAMP 1 2 3
RIC1 1 0 {Ricm}
RLIM1 1 4 0.1
D1 4 6 IDEALMOD
VIH1 6 0 {VIH1}
D2 7 4 IDEALMOD
VIL1 7 0 {VIL1}
RID 4 5 {Rid}
RIC2 2 0 {Ricm}
RLIM2 2 5 0.1
D3 5 8 IDEALMOD
VIH2 8 0 {VIH1}
D4 9 5 IDEALMOD
VIL2 9 0 {VIL2}
GAVD/RO 0 3 4 5 {Avd/Ro}
GAVC1/RO 0 3 4 0 {Avc/Ro}
GAVC2/RO 0 3 5 0 {Avc/Ro}
RO 3 0 {Ro}
D5 3 10 IDEALMOD
VOH 10 0 {VOH}
D6 11 3 IDEALMOD
VOL 11 0 {VOL}
.MODEL IDEALMOD D N=0.001
.ENDS
```

Example 6.7-4 - Illustration of the Voltage Limits of the Op Amp

Use the macromodel of Fig. 6.7-10 to plot v_{OUT} as a function of v_{IN} for the noninverting, unity gain, voltage amplifier when v_{IN} is varied from -15V to +15V. The op amp parameters are $A_{vd}(0)$ = 100,000, R_{id} = 1MΩ, R_{icm} = 100MΩ, $A_{vc}(0)$ = 10, R_o = 100Ω, V_{OH} = -V_{OL} = 10V, V_{IH1} =V_{IH2} = -V_{IL1} = -V_{IL2} = 5V.

Solution

The input file for this example is given below.

```
Example 6.7-4
VIN 1 0 DC 0
XOPAMP 1 2 2 NONLINOPAMP
.SUBCKT NONLINOPAMP 1 2 3
RIC1 1 0 100MEG
RLIM1 1 4 0.1
D1 4 6 IDEALMOD
VIH1 6 0 5V
D2 7 4 IDEALMOD
VIL1 7 0 -5V
RID 4 5 1MEG
RIC2 2 0 100MEG
RLIM2 2 5 0.1
D3 5 8 IDEALMOD
VIH2 8 0 5V
D4 9 5 IDEALMOD
VIL2 9 0 -5v
GAVD/RO 0 3 4 5 1000
GAVC1/2RO 0 3 4 0 0.05
GAVC2/2RO 0 3 5 0 0.05
RO 3 0 100
D5 3 10 IDEALMOD
VOH 10 0 10V
D6 11  3 IDEALMOD
VOL 11 0 -10V
.MODEL IDEALMOD D N=0.0001
.ENDS
.DC VIN -15 15 0.1
.PRINT V(2)
.PROBE
.END
```


Example 6.7-4 - Illustration of the Voltage Limits of the Op Amp - Continued

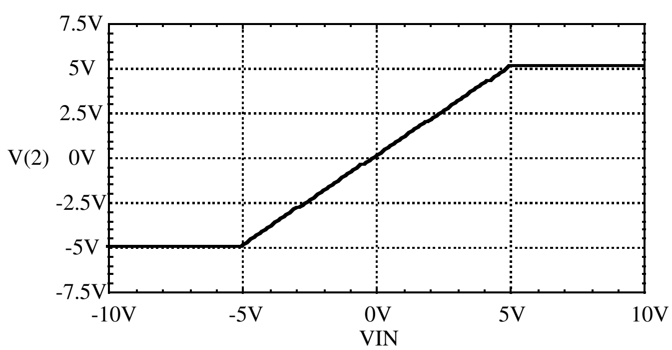
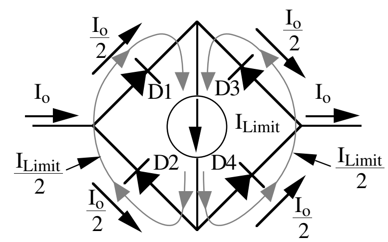


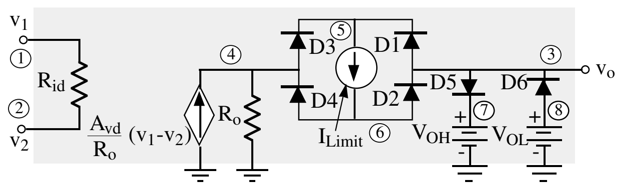
Figure 6.7-11 - Simulation results for Ex. 6.7-4.

Output Current Limiting

Technique:



Macromodel for Output Voltage and Current Limiting:



Example 6.7-5 - Influence of Current Limiting on the Amplifier Voltage Transfer Curve

Use the model above to illustrate the influence of current limiting on the voltage transfer curve of an inverting gain of one amplifier. Assume the V_{OH} = -V_{OL} = 10V, V_{IH} = -V_{IL} = 10V, the maximum output current is ±20mA, and R_1 = R_2 = R_L = 500Ω where R_L is a resistor connected from the output to ground. Otherwise, the op amp is ideal.

Solution

For the ideal op amp we will choose A_{vd} = 100,000, R_{id} = 1MΩ, and R_o = 100Ω and assume one cannot tell the difference between these parameters and the ideal parameters. The remaining model parameters are V_{OH} = -V_{OL} = 10V and I_{Limit} = ±20mA.

The input file for this simulation is given below.

Example 6.7-5 - Influence of Current Limiting on the Amplifier Voltage Transfer Curve

```
VIN 1 0 DC 0
R1 1 2 500
R2 2 3 500
RL 3 0 500
XOPAMP 0 2 3 NONLINOPAMP
.SUBCKT NONLINOPAMP 1 2 3
RID 1 2 1MEGOHM
GAVD 0 4 1 2 1000
RO 4 0 100
D1 3 5 IDEALMOD
D2 6 3 IDEALMOD
D3 4 5 IDEALMOD
D4 6 4 IDEALMOD
ILIMIT 5 6 20MA
D5 3 7 IDEALMOD
VOH 7 0 10V
D6 8 3 IDEALMOD
VOL 8 0 -10V
.MODEL IDEALMOD D N=0.00001
.ENDS
.DC VIN -15 15 0.1
.PRINT DC V(3)
.PROBE
.END
```

Example 6.7-5 - Continued

The resulting plot of the output voltage, v_3, as a function of the input voltage, v_{IN} is shown in Fig. 6.7-14.

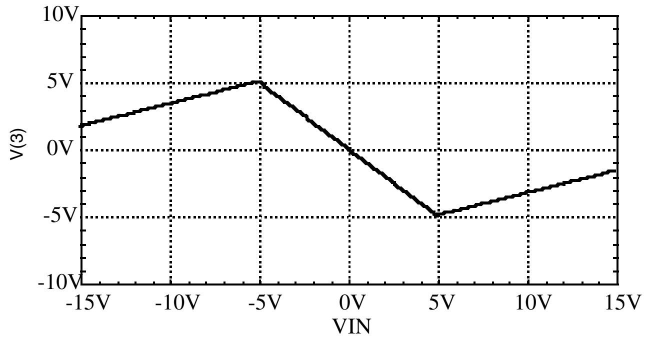


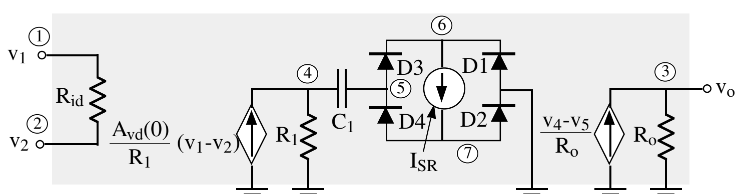
Figure 6.7-14 - Results of Example 6.7-5.

Slew Rate Limiting (Time Dependency)

Slew Rate:

$$\frac{dv_o}{dt} = \frac{\pm I_{SR}}{C_1} = \text{Slew Rate}$$

Macromodel:



Example 6.7-6 - Simulation of the Slew Rate of A Noninverting Voltage Amplifier

Let the gain of a noninverting voltage amplifier be 1. If the input signal is given as

$$v_{in}(t) = 10 \sin(4\text{x}10^5\pi t)$$

use the computer to find the output voltage if the slew rate of the op amp is 10V/μs.

Solution

We can calculate that the op amp should slew when the frequency is 159kHz. Let us assume the op amp parameters of A_{vd} = 100,000, ω_1 = 100rps, R_{id} = 1MΩ, and R_o = 100Ω. The simulation input file based on the macromodel of Fig. 6.7-15 is given below.

Example 6.7-6 - Simulation of slew rate limitation

```
VIN 1 0 SIN(0 10 200K)
XOPAMP 1 2 2 NONLINOPAMP
.SUBCKT NONLINOPAMP 1 2 3
RID 1 2 1MEGOHM
GAVD/R1 0 4 1 2 1
R1 4 0 100KOHM
C1 4 5 0.1UF
D1 0 6 IDEALMOD
D2 7 0 IDEALMOD
D3 5 6 IDEALMOD
D4 7 5 IDEALMOD
ISR 6 7 1A
GVO/R0 0 3 4 5 0.01
RO 3 0 100
.MODEL IDEALMOD D N=0.0001
.ENDS
```


Example 6.7-6 - Continued

The simulation results are shown in Fig. 6.7-16. The input waveform is shown along with the output waveform. The influence of the slew rate causes the output waveform not to be equal to the input waveform.

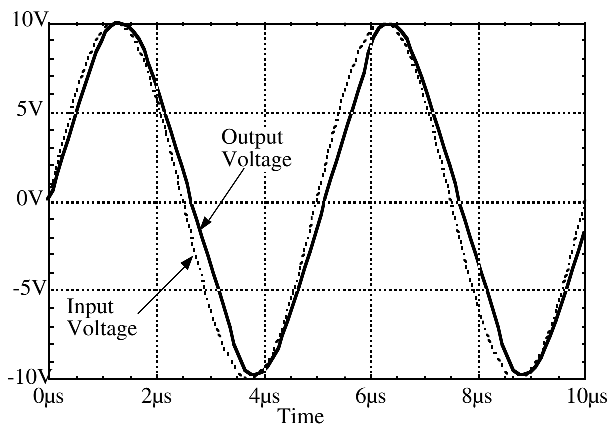


Figure 6.7-16 - Results of Ex. 6.7-6 on modeling the slew rate of an op amp.

SPICE Op Amp Library Models

Macromodels developed from the data sheet for various components.

Key Aspects of Op Amp Macromodels

- Use the simplest op amp macromodel for a given simulation.
- All things being equal, use the macromodel with the min. no. of nodes.
- Use the SUBCKT feature for repeated use of the macromodel.
- Be sure to verify the correctness of the macromodels before using.
- Macromodels are a good means of trading simulation completeness for decreased simulation time.

SECTION 6.8 - SUMMARY

- Topics
  - Design of CMOS op amps
  - Compensation of op amps
    - - Miller
    - - Self-compensating
    - - Feedforward
  - Two-stage op amp design
  - Power supply rejection ratio of the two-stage op amp
  - Cascode op amps
  - Simulation and measurement of op amps
  - Macromodels of op amps
- Purpose of this chapter is to introduce the simple two-stage op amp to illustrate the concepts of op amp design and to form the starting point for the improvement of performance of the next chapter.
- The design procedures given in this chapter are for the purposes of understanding and applying the design relationships and should not be followed rigorously as the designer gains experience.

