

# **EE 610**

# **ANALOG VLSI CIRCUITS**



## **Project Report**

## **Novel CMOS Current Schmitt Trigger**

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# CMOS Current Schmitt Trigger

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*Two CMOS current Schmitt Triggers based on current mirrors are simulated.*

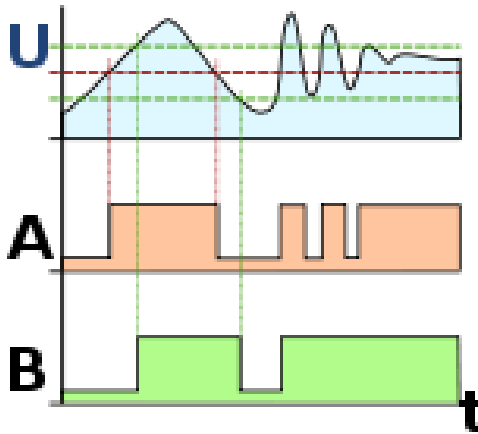
- The significant feature of one circuit is that one threshold current is controlled by a bias current and the other by an MOS transistor dimension, depending on the circuit implementation.*
  - The significant feature of the other circuit is that the hysteresis is independent of process parameters, transistor dimensions and power supplies. The hysteresis is determined by two currents and is adjustable over the range of the input current.*
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## Introduction

A **Schmitt trigger** is a **comparator** circuit that incorporates **positive feedback**.

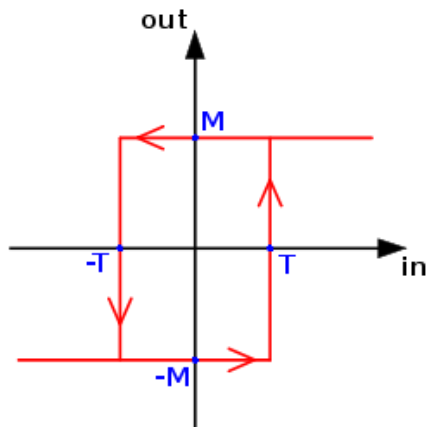
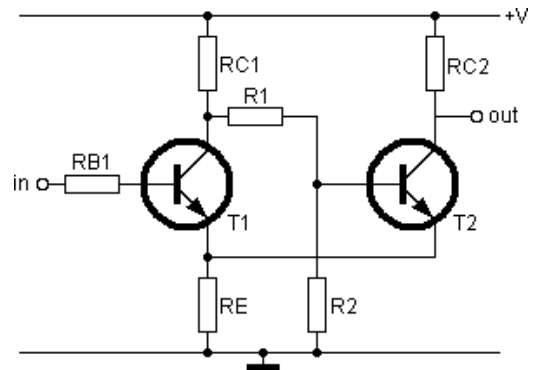
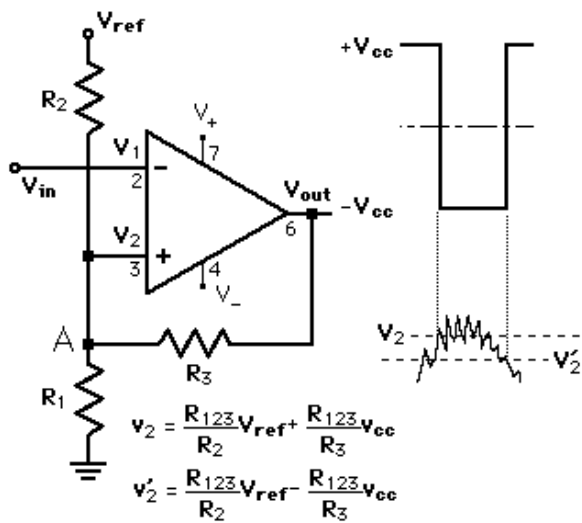
When the input is higher than a certain chosen threshold, the output is high; when the input is below another (lower) chosen threshold, the output is low; when the input is between the two, the output retains its value. The trigger is so named because the output retains its value until the input changes sufficiently to trigger a change. This dual threshold action is called hysteresis, and implies that the Schmitt trigger has some memory. In fact, the Schmitt trigger is a bistable multivibrator.

For a **Current Schmitt trigger** the input is a current instead of a voltage, which makes the output voltage snap alternately to a logical signal with two stable states ('low' and 'high'), depending on the difference between the input and **two threshold currents**. Current Schmitt triggers are particularly useful in photo-detectors, optical remote control, and medical instruments. They are of special interest in CMOS technology as interfaces between analogue and digital circuits integrated on a chip.



The effect of using a Schmitt trigger (B) instead of a comparator (A).

## Schmitt trigger configurations



Typical hysteresis curve

# Circuit Description and operation of the Schmitt triggers

## (I) Hysteresis width dependent on MOS parameters

In the case of CMOS integrated (voltage) Schmitt triggers, there are only a few MOS transistors used and the regenerative feedback is established by MOS transistors as well, to avoid the need for resistors. The threshold voltages are determined by the transistor geometries and the process parameters, and normally also by supply voltages.' Thus, the hysteresis of Schmitt triggers after their integration will remain fixed, unless power supplies, temperature and other physical parameters change.

The CMOS current Schmitt trigger simulated is shown in Fig. 1. It consists of a current comparator (M1, M2 and M3, M4), an inverter (M6 and M7) and an additional transistor M5, which may either be of a PMOS or NMOS type. M5 ensures the positive feedback and makes the current comparator to become a current Schmitt trigger as described below.

First, consider the circuit of Fig. 1, where M5 is assumed to be removed. The input current  $I_{in}$  is applied to the drain of M3, while a reference current  $I_o$  is applied to the drain of M1. M1, M2 and M3, M4 are matched pairs forming current mirrors with a ratio of 1: 1, i.e.  $I_{in}$  and  $I_o$  are reproduced by M4 and M2, respectively, if they are operating in saturation mode. Therefore, the threshold current of this comparator is equal to  $I_o$ , i.e. when  $I_{in}$  is less than  $I_o$ ,  $V_A$  becomes 'low', hence  $V_o$  will be high. Conversely,  $V_o$  will be 'low' when  $I_{in}$  exceeds  $I_o$ .

Now let us reinsert M5 into Fig. 1 to realize a CMOS current Schmitt trigger. M5 provides a regenerative feedback by feeding current dependent on  $V_A$  to one of the current mirrors. If  $I_{in}$  is much lower than  $I_o$ ,  $V_A$  is 'low', i.e. M4 is working in the saturation mode while M5 and M2 are not saturated. The reason for transistor M5 and M2 operating in the triode region is as follows:

M5 is operated with a gate voltage  $V_{gs5}$  much higher than its drain voltage (which is identical to the  $V_{gs3}$ ) thus driving it into its ohmic region. The drain current  $I_{d2}$  is equal to  $I_{d4}$  which is  $I_{d4} = I_{in} - I_{d5}$ . Thus

$$I_{d2} = I_{in} - I_{d5} < I_o \quad (1)$$

i.e. the reference current  $I_o$ , cannot be mirrored into M2, thus forcing M2 into the triode mode.

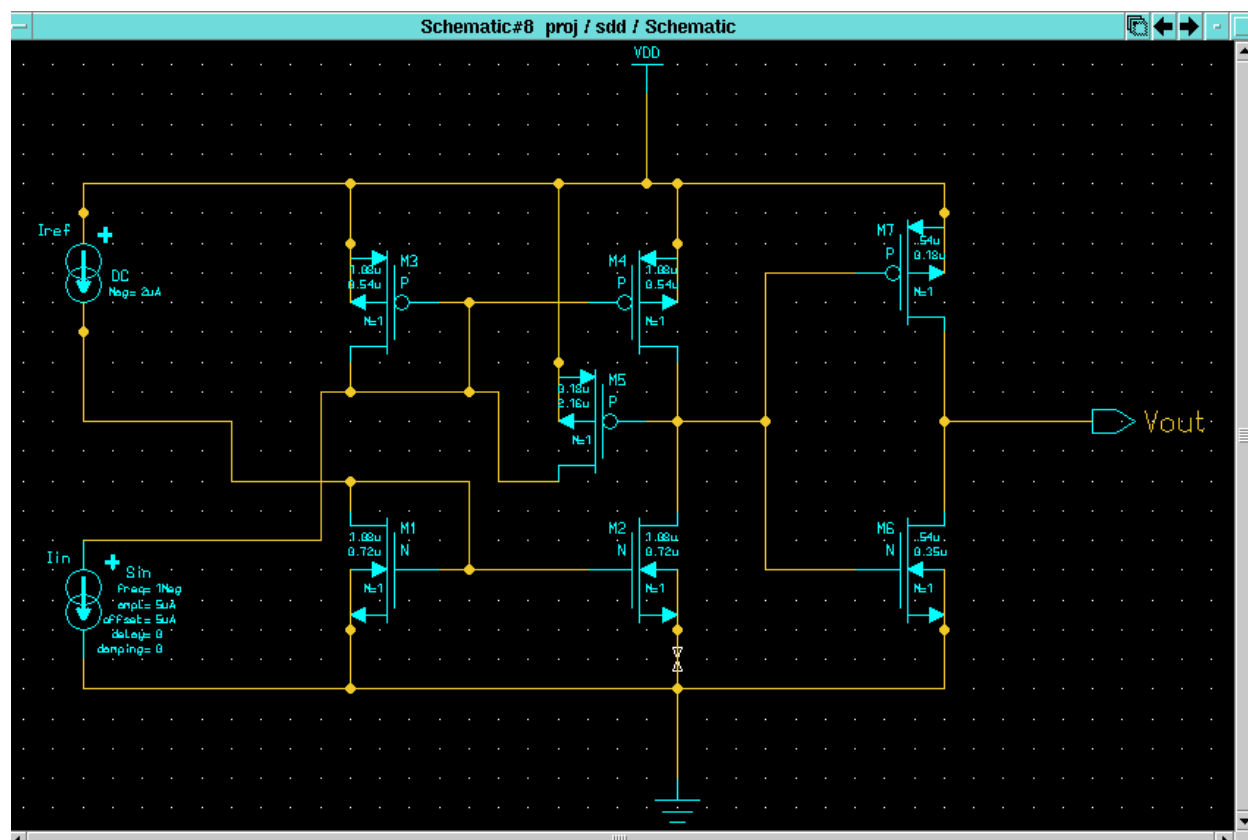
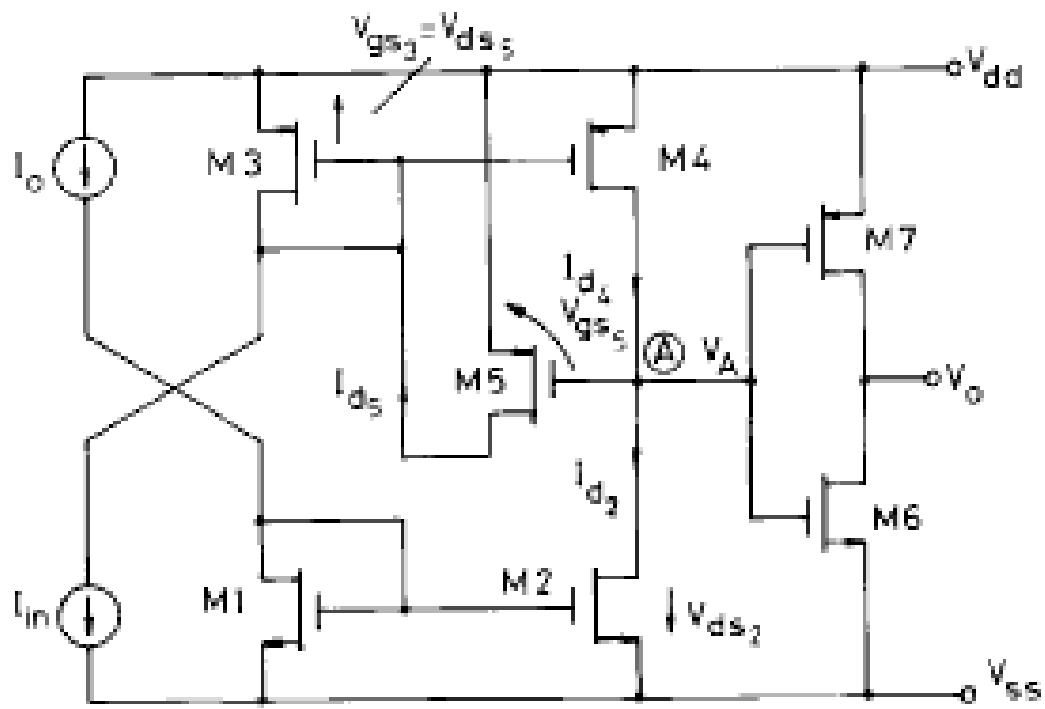


Fig 1 showing the Circuit and Schematic

When increasing  $I_{in}$ , the upper threshold current  $I_{th}$ , is reached when  $I_{d2} = I_o$ . At this point M2 has reached its maximum drain current value it is able to feed into node A, and it now acts as a current mirror with respect to M1 and therefore enters into the saturation mode. According to eqn. 1 this occurs at the current

$$I_{th} = I_o + I_{d5} \quad (2)$$

Augmenting  $I_{in}$ , beyond this point raises  $V_{ds2}$ , at a high rate, thus decreasing  $I_{d3}$  and switching  $V_A$ , to 'high' through regenerative action. Choosing appropriate geometrical dimensions of M4 and M5, the feedback transistor M5 is held in a non conducting condition ( $I_{d5} = 0$ ) while  $V_A$ , is 'high'. This condition is fulfilled when  $\sqrt{(2I_o/K_4)} \leq |V_{Tp}|$ , is the absolute value of the PMOS threshold voltage and  $K_2 = \mu C_{ox} (W/L)^2$ . Here  $\mu_o$  is mobility of carrier,  $C_{ox}$  is oxide capacitance per unit area,  $W$  is width of channel and  $L$  is length of channel. A subsequent decrease of  $I_{in}$ , switches  $V_A$ , back to 'low' at the threshold level  $I_{th}$  like a simple current comparator, thus

$$I_{th} \approx I_o \quad (3)$$

The upper threshold current  $I_{th}$  is calculated as follows. As stated above  $V_A$ , switches from 'low' to 'high' while increasing  $I_{in}$ , when  $I_{d4}$ , equals  $I_o$ , and M2 enters the saturation mode. Using the quadratic model of MOS transistors in the strong inversion mode the respective  $V_{ds2}$  reads:

$$\begin{aligned} V_{ds2} &= \sqrt{(2I_o/K_2)} \\ -V_{gs5} &= V_{dd} - V_{ss} - V_{ds2} \end{aligned} \quad (4)$$

And its drain voltage is

$$-V_{ds5} = -V_{gs5} = \sqrt{\left(\frac{2I_o}{K_3}\right)} - V_{Tp} = \sqrt{\left(\frac{2I_o}{K_3}\right)} + |V_{Tp}| \quad (5)$$

The drain current  $I_{d5}$ , can be calculated from the well known current equation in the triode region

$$I_{d5} = K_5 [(V_{gs5} - V_{T,r})V_{ds5} - \frac{1}{2}V_{ds5}^2] \quad (6)$$

Using eqns. 2, 4-6 yields

$$\begin{aligned} I_{th} = I_0 + K_5 & \\ & \times \left[ \left( V_{dd} - V_{ss} - \sqrt{\left( \frac{2I_0}{K_2} \right) - |V_{T,r}|} \right) \right. \\ & \left. \times \left( \sqrt{\left( \frac{2I_0}{K_3} \right) + |V_{T,r}|} \right) - \frac{1}{2} \left( \sqrt{\left( \frac{2I_0}{K_3} \right) + |V_{T,r}|} \right)^2 \right] \end{aligned} \quad (7)$$

The hysteresis width obtained from  $\mathbf{yI} = I_{th} - I_{tl} = I_{d5}$  according to eqn. 7 it is determined by transistor dimensions of M5,  $I_0$ , and process parameters. Thus, the hysteresis width ( $\mathbf{yI}$ ) can be chosen by the geometry of M5.

# Simulation Results

Fig 1 has been simulated using Mentor graphics tools. The respective transistor dimensions and circuit parameters are given below:

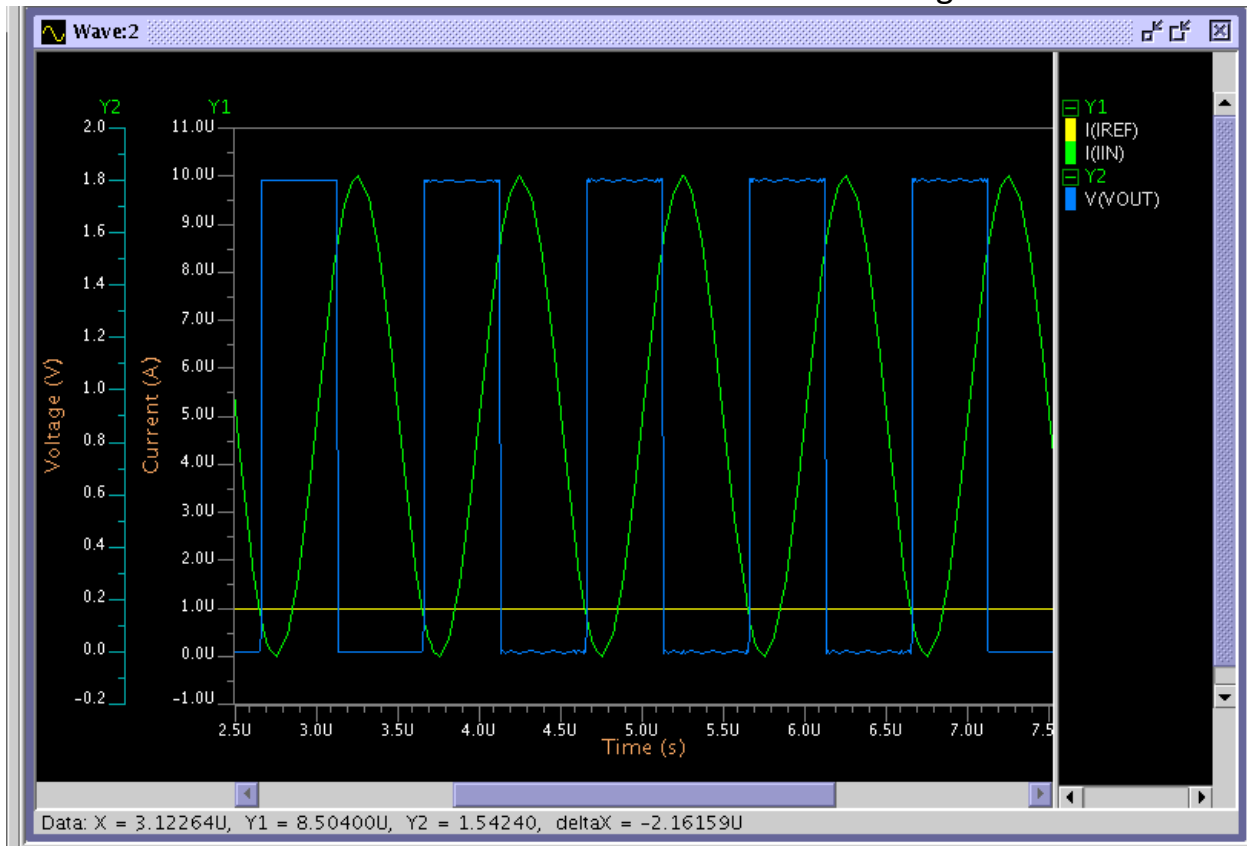
Transistors	W $\mu\text{m}$	L $\mu\text{m}$
M1, M2	1.08	0.72
M3, M4	1.08	0.54
M5	0.18	1.08
M6	0.54	0.36
M7	0.54	0.36

$$V_{dd} = 1.8 \text{ V}$$

$$V_{ss} = 0 \text{ V}$$

$$I_o = 1 \mu\text{A}$$

DC transfer and AC transfer characteristics of  $I_{in}$  against  $V_o$

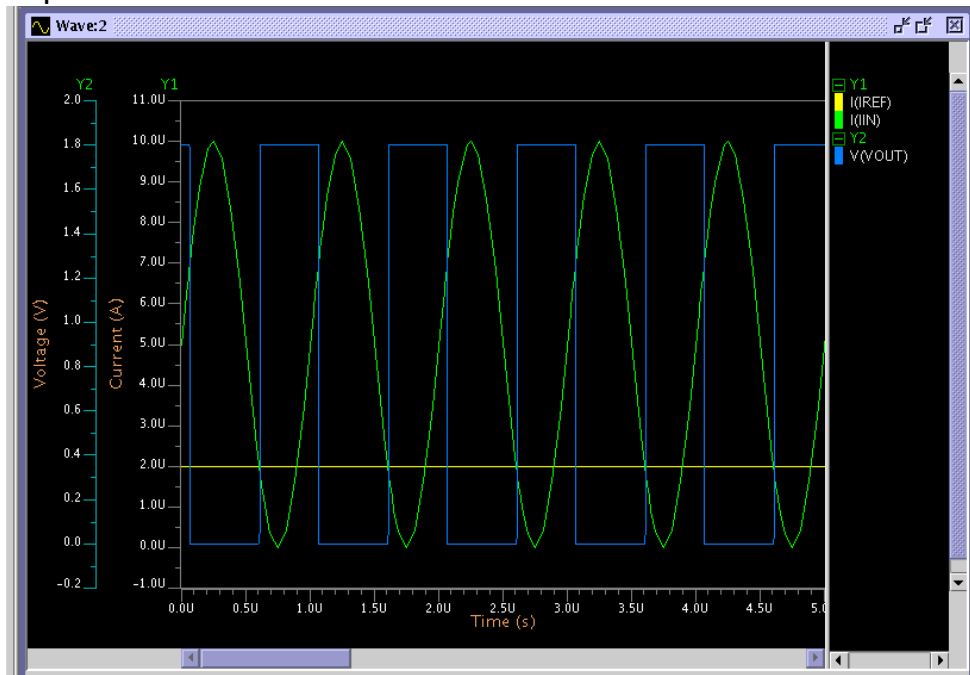


The hysteresis current is  $7.54 \mu\text{A}$

### Changing the width and length of the transistor M5

➤  $W = 0.18 \mu\text{m}$

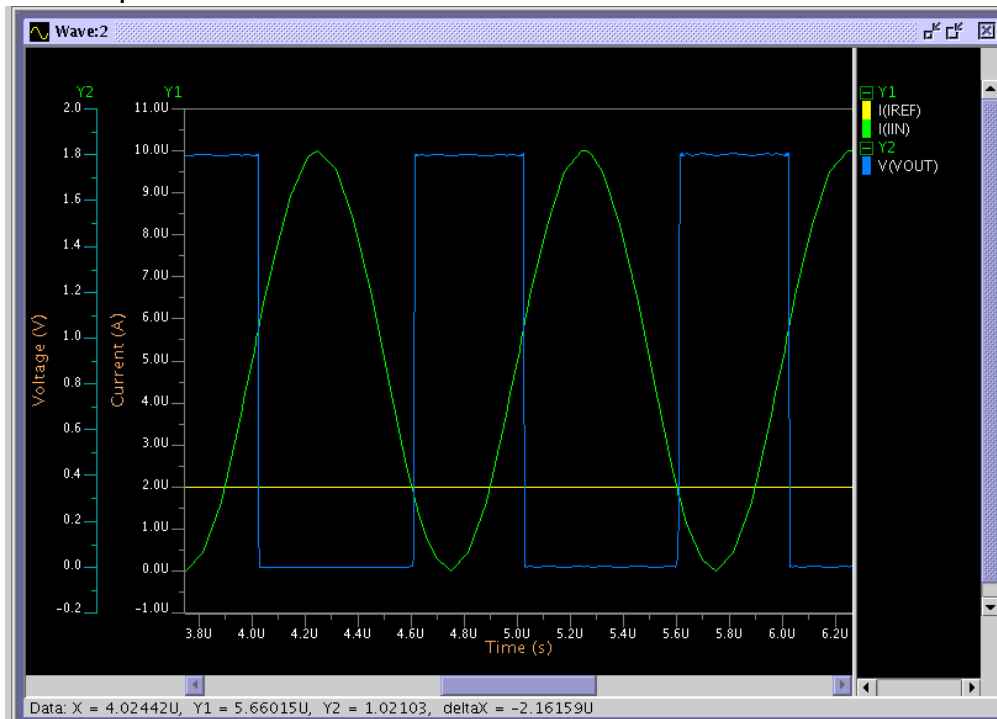
$L = 1.62 \mu\text{m}$



Hysteresis current is  $5.12 \mu\text{A}$

➤  $W = 0.18 \mu\text{m}$

$L = 2.16 \mu\text{m}$



Hysteresis current is  $3.72 \mu\text{A}$

## (II) Hysteresis width independent of MOS parameters

The previous CMOS current Schmitt trigger based on current mirrors possessed advantages that it is a simple structure with easy design. In this circuit, one of the thresholds is defined by a current and the other depends on process parameters, transistor dimensions and the supply voltages. Hence, the circuit layout is application-specific, and a spread of the parameters has to be tolerated from chip to chip as well as from batch to batch. This means an accurate hysteresis, required in some applications, is rather difficult to achieve.

Secondly, the hysteresis is dependent on supply voltages. Thirdly, it is often desirable in practice that the hysteresis can be adjusted by currents or voltages to meet various needs.

### Description

In the Fig given below M3, M4 and M5 and M6, are matched pairs which compare the currents  $I_{d1} + I_I$  and  $I_{in}$ . The output of this comparator controls the differential switching stage (M1 and M2), via an inverter (M7 and M8). Therefore, a regenerative feedback exists in the loop. We start with an input, denoted as  $I_{in}$ , which is very small in comparison with the current  $I_I$ ;  $V_A$  at node A is then 'high'. The output voltage  $V_o$  will be 'low', which turns M1 on and M2 off. As a result,  $I_o$  flows through M1. The current through M3 is

$$I_{th} = I_o + I_I \quad (1)$$

which represents the high threshold current of the Schmitt trigger.

If  $I_{in}$  increases and exceeds  $I_{th}$ ,  $V_A$  will snap to 'low' and  $V_o$  to 'high'. Owing to the action of positive feedback M1 is now cut off and M2 is on. The threshold current of the comparator is switched to  $I_I$  thus

$$I_{tl} = I_I \quad (2)$$

and the output of the circuit flips back to 'low' when  $I_{in}$  is decreased below  $I_{tl}$ . From eqns. 1 and 2 the hysteresis current is

$$\Delta I = I_{th} - I_{tl} = I_o$$

We can now summarize the operation of this current Schmitt trigger as follows. The threshold current of the comparator is determined exclusively by the current through M3. This current is controlled by  $V_o$  via switching M1 on and off alternately.

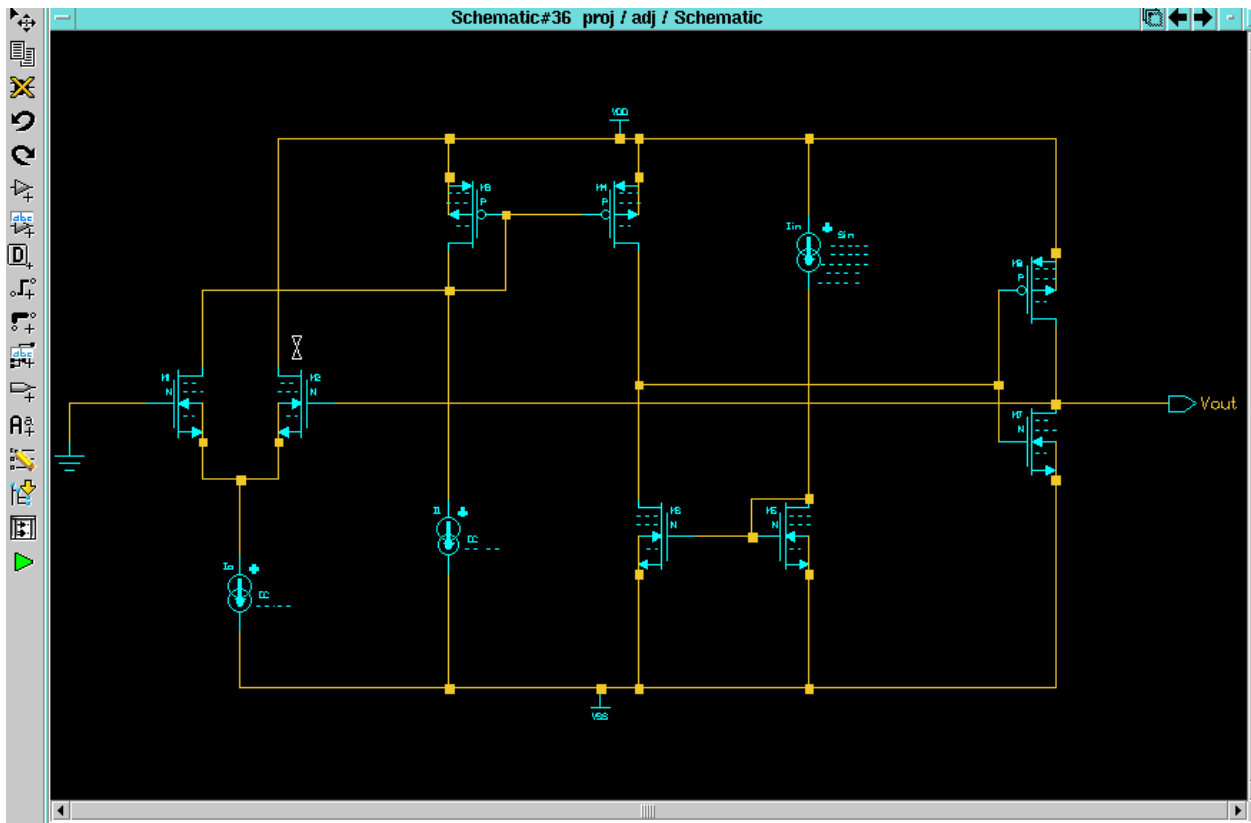
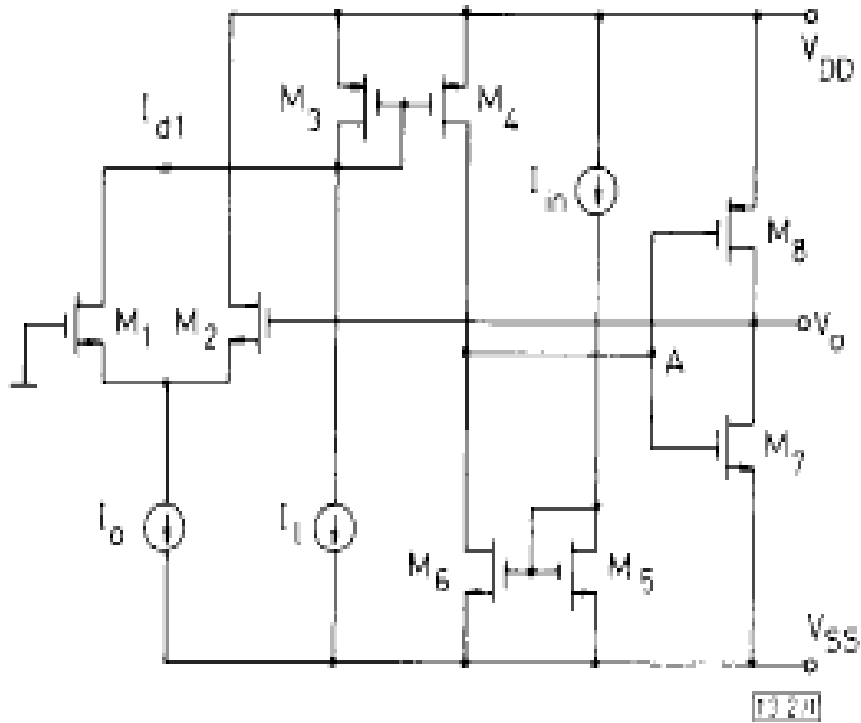


Fig 2 showing the Circuit and Schematic

## Simulation Results

Fig 2 has been simulated using Mentor graphics tools. The respective transistor dimensions and circuit parameters are given below:

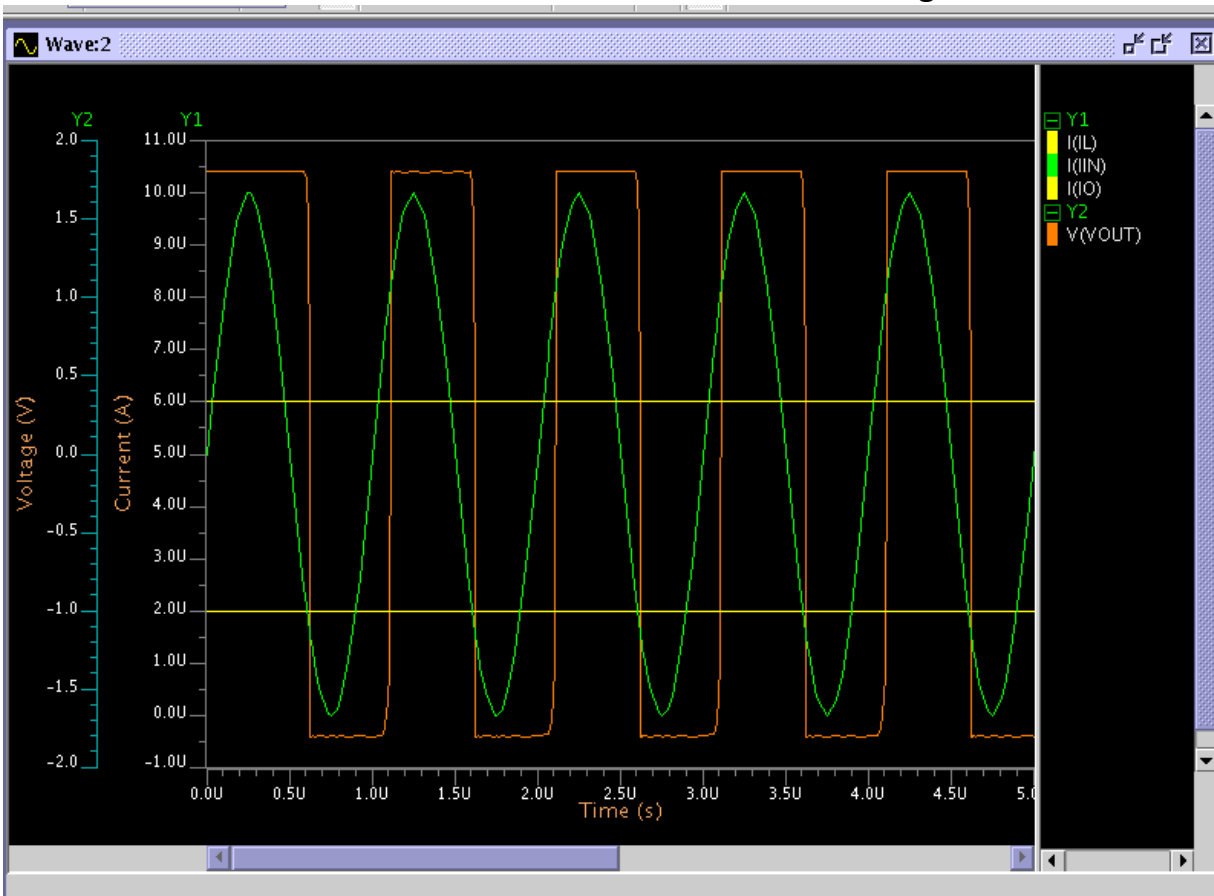
Transistors	W $\mu\text{m}$	L $\mu\text{m}$
M1, M2	0.54	0.18
M3, M4	0.18	0.54
M5, M6	0.18	0.72
M7	0.54	0.36
M8	0.54	0.24

$$V_{dd} = 1.8 \text{ V}$$

$$V_{ss} = -1.8 \text{ V}$$

$$I_o = 4 \mu\text{A} \quad I_l = 2 \mu\text{A}$$

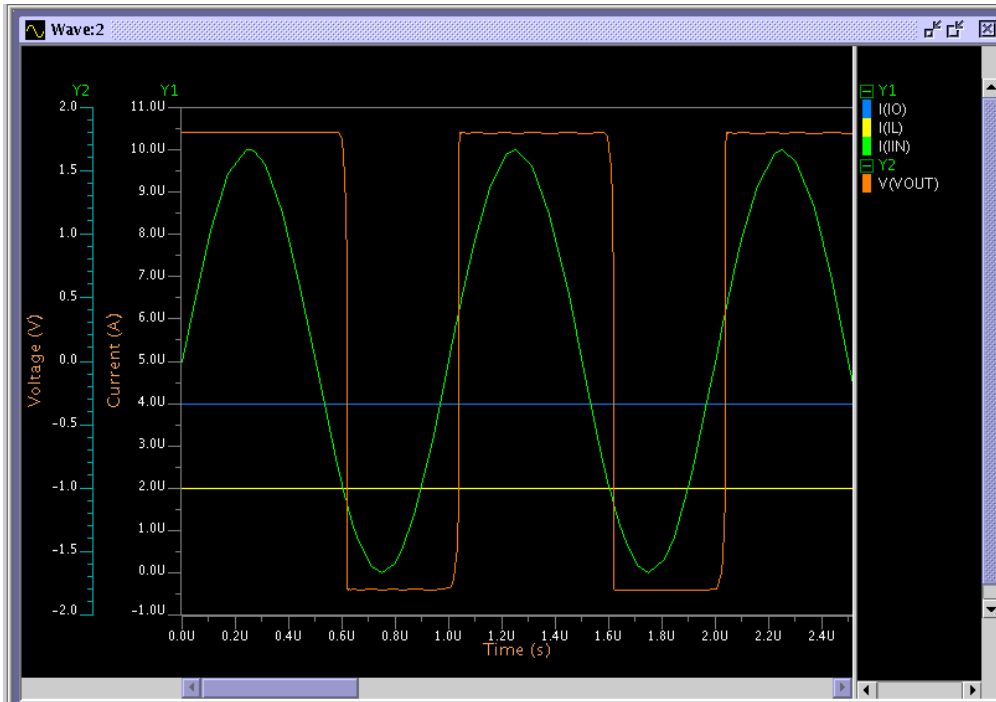
DC transfer and AC transfer characteristics of  $I_{in}$  against  $V_o$



Hysteresis current is  $4 \mu\text{A} = I_o$

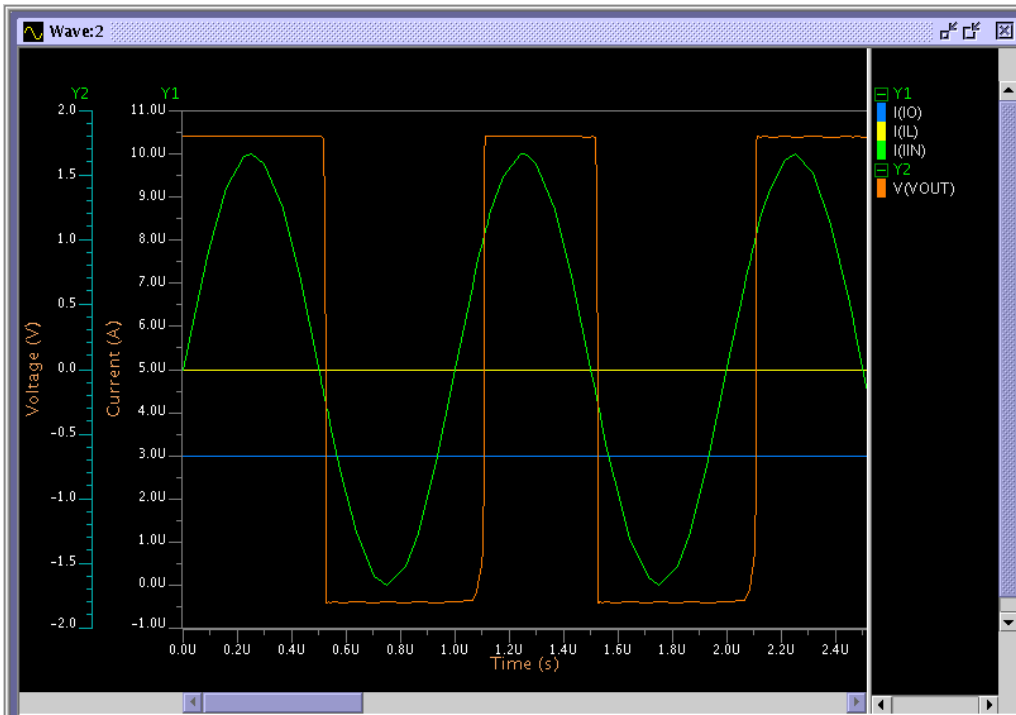
## Changing $I_o$ and $I_l$

- $I_o = 2 \mu\text{A}$   $I_l = 2 \mu\text{A}$



Hysteresis current is  $2 \mu\text{A} = I_o$

- $I_o = 2 \mu\text{A}$   $I_l = 3 \mu\text{A}$



Hysteresis current is  $2 \mu\text{A} = I_o$

## Comments

- The first CMOS current Schmitt trigger based on current mirrors possessed advantages that it is a simple structure with easy design. In this circuit, one of the thresholds is defined by a current and the other depends on process parameters, transistor dimensions and the supply voltages
- The second design has advantage that now we have full control over both the thresholds, hence the output can be achieved as desired.

## References

- Z. WANG, W. GUGGENBUHL.: 'NOVEL CMOS CURRENT SCHMITT TRIGGER' , *ELECTRONICS LETTERS* 24th November 1988 Vol. 24 No. 24
- Z. WANG, W. GUGGENBUHL.: 'CMOS CURRENT SCHMITT TRIGGER WITH FULLY ADJUSTABLE HYSTERESIS' , *ELECTRONICS LETTERS* 16th March 1989 Vol. 25 No. 6
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