“Techniques for Simulation and Measurement of Op Amps”

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Abstract: - This paper presents the background for simulating and testing a CMOS op amp. When we design a CMOS op amp, we start with building blocks whose performance can be analyzed to a first order approximation by hand/calculator methods of analysis. This provides us the insight as the design of the circuit develops. However, at some point we must turn to a better means of simulation. For the CMOS op amp this is generally a computer analysis program such as SPICE. After fabrication, for testing and evaluating CMOS op amp we must verify each specification over a large number of op amps to ensure a working op amp in case of process variation.

Key-words:- Operational amplifier, complementary metal-oxide semiconductor, common-mode range.

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1 Introduction

Advances in the signal processing, analog/digital conversion and continuingly scale down of CMOS nanotechnology have ushered in the era of analog IC design with multistandard challenge. This paper is intended for working professionals who have no experience on simulation and measurement of op amp, but are interested in building hands-on experience on optimized op amp simulation.

The op amp is one of the basic and important circuit which has a wide applications in several analog circuits. By simulation and measurement we have to meet most of the specifications like- open-loop gain, open-loop frequency response (including phase margin), input-offset voltage, common-mode gain, power-supply rejection ratio, common-mode input and output voltage ranges, open-loop output resistance and the transient response including slew rate. The techniques for each of these measurements will be presented in this paper. Because the simulation and measurement of the CMOS op amp are almost identical, they are presented simultaneously. The concepts presented here are applicable to all types of computer-simulation programs.

The paper is organized as follows: in section-2 we present all the configurations for simulating and measuring the above specified and many other characteristics. The section-3 gives conclusion of this paper.

2 Configurations for Simulation and Measurement

2.1 Open-Loop Configuration

One of the most difficult steps to perform successfully is the Simulation or measurement of the op amp in an open-loop configuration. The high differential gain of the op amp is the reason for that.

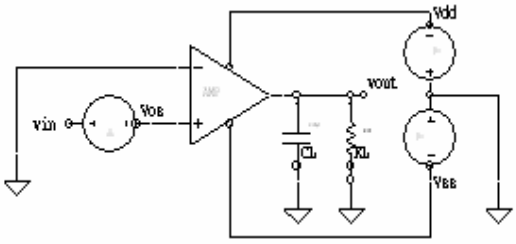

Fig. 1.Open-Loop mode with offset compensation

Fig.1 shows how this step might be performed. Vos is an external voltage whose value is adjusted to keep the dc value of vout between the power-supply limits. Without Vos the op amp will driven to the positive or negative power supply for either the measurement or simulation cases. It is necessary to be able to find Vos to the accuracy of the magnitude of the power supply divided by the low-frequency differential gain (typically in the range of mV). Although this method works well for simulation, the practical characteristics of the op amp make the method almost impossible to use for measurement.

A more suitable method for measuring the open-loop gain is shown in the circuit of fig.2.In this

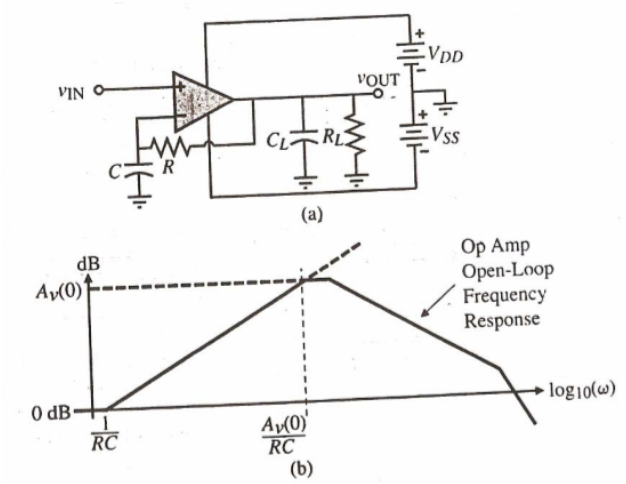

Fig. 2 (a) A method of measuring the open-loop characteristics with dc bias stability
Fig. 2(b) Asymptotic magnitude plot of voltage transfer function

circuit it is necessary to select the reciprocal RC time constant a factor of Av(0) times less than the anticipated dominant pole of op amp. Under these conditions, the op amp has total dc feedback, which stabilizes the bias. The dc value of vout will exactly the dc value of vin. The true open loop frequency characteristics will not be observed until the frequency is approximately A(0) times 1\RC. Above this frequency, the ratio of vout to vin is essentially the open-loop gain of the op amp. This method works well for both simulation and measurement.

Simulation or measurement of the open-loop gain of the op amp will characterize the open loop transfer curve, the open loop output-swing limits, the phase margin, the dominant pole, the unity-gain bandwidth, and other open-loop characteristics. The designer should connect the anticipated loading at the output in order to get meaningful results.

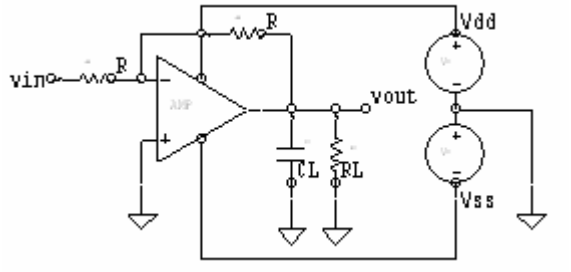

Fig. 3 Configuration for simulating or measuring the open-loop frequency response for moderate gain of an op-amp

In some cases, where the open-loop gain is not too large, the open-loop gain can be measured by applying vin in the circuit fig.3 and measuring vout and vin. In this configuration, one must be careful that R is large enough not to cause a dc current load on the output of the op amp.

2.2 Measuring the Input-Offset Voltage
The dc input-offset voltage can be measured using the circuit of fig.4. If the dc input offset voltage is too small, it can be amplified by using a resister

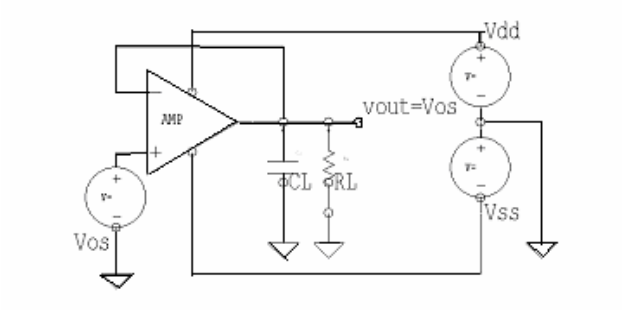

Fig. 4 Configuration for measuring the input offset voltage and the simulation of the systematic offset voltage of an op-amp

Divider in the negative feedback path. One must remember that Vos will vary with time and temperature and is very difficult to precisely measure experimentally. Interestingly enough, Vos cannot be simulated.

2.3 Simulating Common-Mode Gain
The common mode gain is most easily simulated or measured using fig 5. It is seen that if Vos fails to keep the op amp in the linear region, this configuration will fail. More often than not, the designer wishes to measure or simulate the CMRR. The common-mode gain could be derived from the CMRR and the open loop gain if necessary.

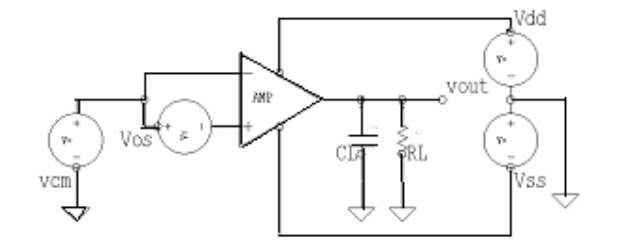

Fig. 5 Configuration for simulating the common mode gain

2.4 Measuring Common-Mode Rejection Ratio (CMRR)

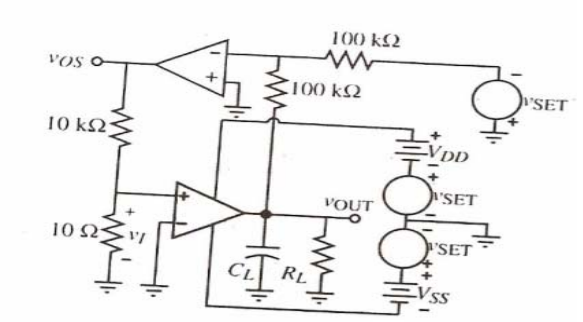

Fig. 6 Circuit used to measure CMRR and PSRR

A method of measuring the CMRR of an op amp, which is more robust, is given in fig.6 [2]. While the method can be used for dynamic characterization, we will explain the operation from a static viewpoint. Assume that first all vSET voltage sources are increased by some amount, say, 1V. This causes the output and the power supplies to the op amp under test to be increased by 1V. As a result of this a voltage vI, will appear at the input of the op amp under test. The vI will be equal to the common mode output voltage of 1V divided by the differential voltage gain of the op amp under test. This change in vI can be measured at vos as approximately 1000 vI. Let this value of vos be designated as Vos1. Next, all vSET voltage sources are decreased by the same amount (in order to cancel any +ve or –ve signal differences). This measure of the vos is designated as Vos2. The CMRR can be found as

$$\text{CMRR}=2000 / |\text{Vos1-Vos2}| \qquad (1)$$

If the vSET sources are replaced by a small signal voltage called vicm, then it can be shown that the CMRR can be given as

$$\text{CMRR}=1000\ \text{vicm} / \text{vos} \qquad (2)$$

Using this approach, one could apply vicm and sweep the frequency to measure vos and the CMRR as a function of frequency.

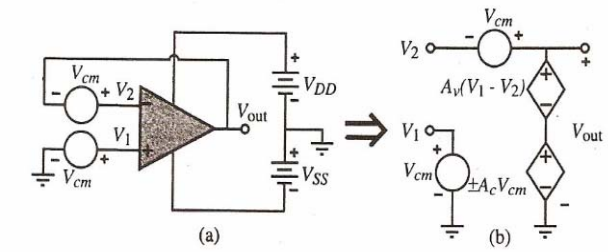

Fig. 7(a) Configuration for direct simulation of CMRR
Fig 7(b) Model for (a)

While the above method could be used for simulation of the CMRR, there are easier methods if simulation of CMRR is the goal. The objective of simulation is to get an output that is equal to CMRR or can be related to CMRR. Fig.7a shows a method that can accomplish this objective. Two identical voltage source designated as Vcm are placed in series with both op amp inputs where the op amp is connected in the unity gain configuration. A model of this circuit is shown in fig.7b. It can be shown that

$$\text{Vout/Vcm} = \pm \text{Ac}/1+\text{Av}\ (\pm\text{Ac}/2)$$
$$\simeq |\text{Ac}|/\text{Av} = 1/\text{CMRR} \qquad (3)$$

Computer simulation can be used to calculate above equation directly. If the simulator has a post processing capability, then it is usually possible to plot the reciprocal of the transfer function so that CMRR can be plotted directly.

2.5 Measuring Power-Supply Rejection Ratio (PSRR)

The configuration of fig.6 can also be used to measure the power supply rejection ratio, PSRR. The procedure sets all vSET voltage sources to zero except for the one in series with Vdd. Set this source to +1V. In this case, v1 is the input-offset voltage for Vdd+1 V.

Measure Vos under these conditions and designate it as Vos3. Next, set Vdd to Vdd-1 V using the vSET source in series with Vdd; measure Vos and designate it as Vos4. The PSRR of the Vdd supply is given as

$$\text{PSRR of Vdd} = 2000 / |\text{Vos3-Vos4}| \qquad (4)$$

Similarly for the Vss rejection ratio, change Vss and keep Vdd constant while Vout is at 0V. The above formula can be applied in the same manner to find the –ve power supply rejection ratio. This approach is also suitable for the measuring PSRR as a function of frequency of the appropriate vSET voltage sources are replaced with a sinusoid.

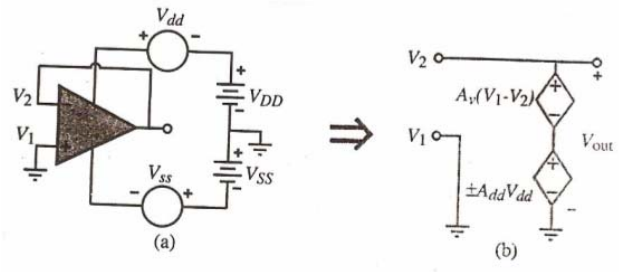

Fig. 8(a) Configuration for direct simulation or measurement of PSRR
Fig 8(b) Model of (a) with Vss = 0

Fig.8 shows a configuration similar to fig.4 that is suitable for measuring the PSRR as a function of frequency. A small sinusoidal voltage is inserted in series with Vdd(Vss) to measure PSRR+ (PSRR-). From equation 4 it was shown that

$$\text{Vout/Vdd} \simeq 1/\text{PSRR} \quad \text{or}$$

$$\text{Vout/Vss} \simeq 1/\text{PSRR-} \qquad (5)$$

This procedure was the method by which PSRR was calculated for the two stage op amp. This method works well as long as the CMRR is much greater than 1.

2.6 Measurement of Common-Mode Voltage Range

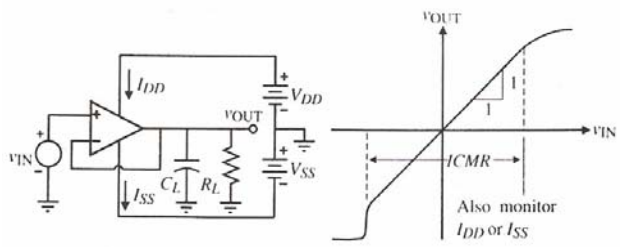

Fig. 9 Measurement of input common-mode voltage range of an op-amp

The input and output common mode voltage range can be defined for both the open loop and closed loop modes of the op amp. For the open loop case, only the output CMR makes sense. One of the configuration of fig.1 or 3 can be used to measure the output CMR. Typically, the open loop, output CMR is about half the power supply range. Because the op amp is normally used in a closed loop mode, it makes more sense to measure or simulate the input and output CMR for this case. The unity gain configuration is useful for measuring or simulating the input CMR. Fig 9 shows the configuration and the anticipated results. The linear part of the transfer curve where the slope is unity corresponds to the input common mode voltage range. The initial jump in the voltage sweep from the –ve values of vIN to +ve values is due to the tern-on of M5.

2.7 Measurement of Output Voltage Swing

In the unity gain configuration, the linearity of the transfer curve is limited by the ICMR. Using a configuration of higher gain, the linear part of the transfer curve corresponds to the output voltage swing of the amplifier. This is illustrated in fig.10 for an inverting gain of 10 configuration. RL should be selected to represent the actual circumstance.

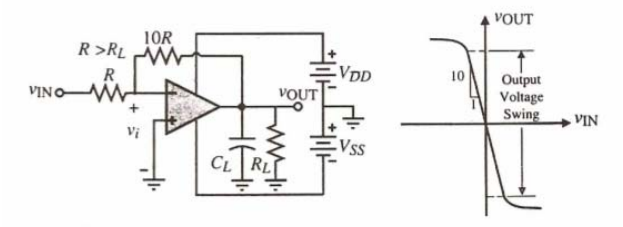

Fig. 10 Measurement of output voltage gain

2.8 Measurement of Open-Loop Output Resistance

The output resistance can be measured by connecting a load resistance RL to the op amp output in the open loop configuration. The measuring configuration is shown in fig.11

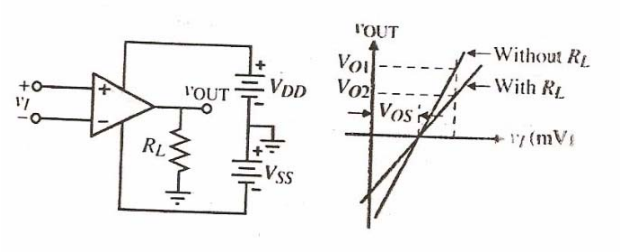

Fig. 11 Measurement of open-loop output resistance

The voltage drop caused by RL at a constant value of vIN can be used to calculate the output resistance as

Rout =RL (V01/V02-1) (6)

It is assumed that Av is in the range of 1000 and that R is greater than R0. Measuring Rout and knowing Av allows one to calculate the output resistance of the op amp R0 from above equation. Other schemes for measuring the output impedance of op amps can be found in the literature.

2.9 Measurement of Slew Rate

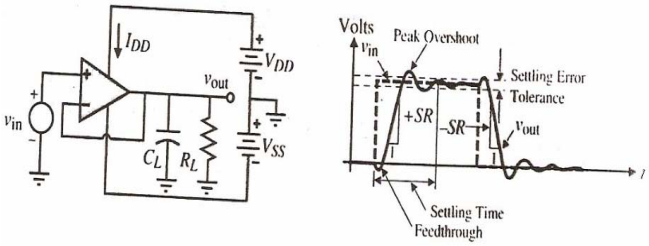

Fig. 12 Measurement of slew rate and settling time

The configuration of fig.12 is useful for measuring the slew rate and the settling time. This gives the details of the measurement for best accuracy, the slew rate and settling time should be measured separately. If the input step is sufficiently small (<0.5V), the output should not slew and the transient response will be a linear response. The settling time can easily be measured. If the input step magnitude is sufficiently large, the op amp will slew by virtue of not having enough current to charge or discharge the compensating and/or load capacitances. The slew rate is determined from the slope of the output waveform during the rise or fall of the output. The output

loading of the op amp should be present during the settling time and slew rate measurements.

3 Conclusion

This paper presents the background for simulating and testing a CMOS op amp. After fabrication, for testing and evaluating CMOS op amp we must verify each specification over a large number of op amps to ensure a working op amp in case of process variation. Other simulations (such as noise tolerance, process parameter variations, and temperature) can also be performed.

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