Lecture 11: Cascode and Buffered Operational Amplifiers

November 27, 2007

Cascode Op Amps

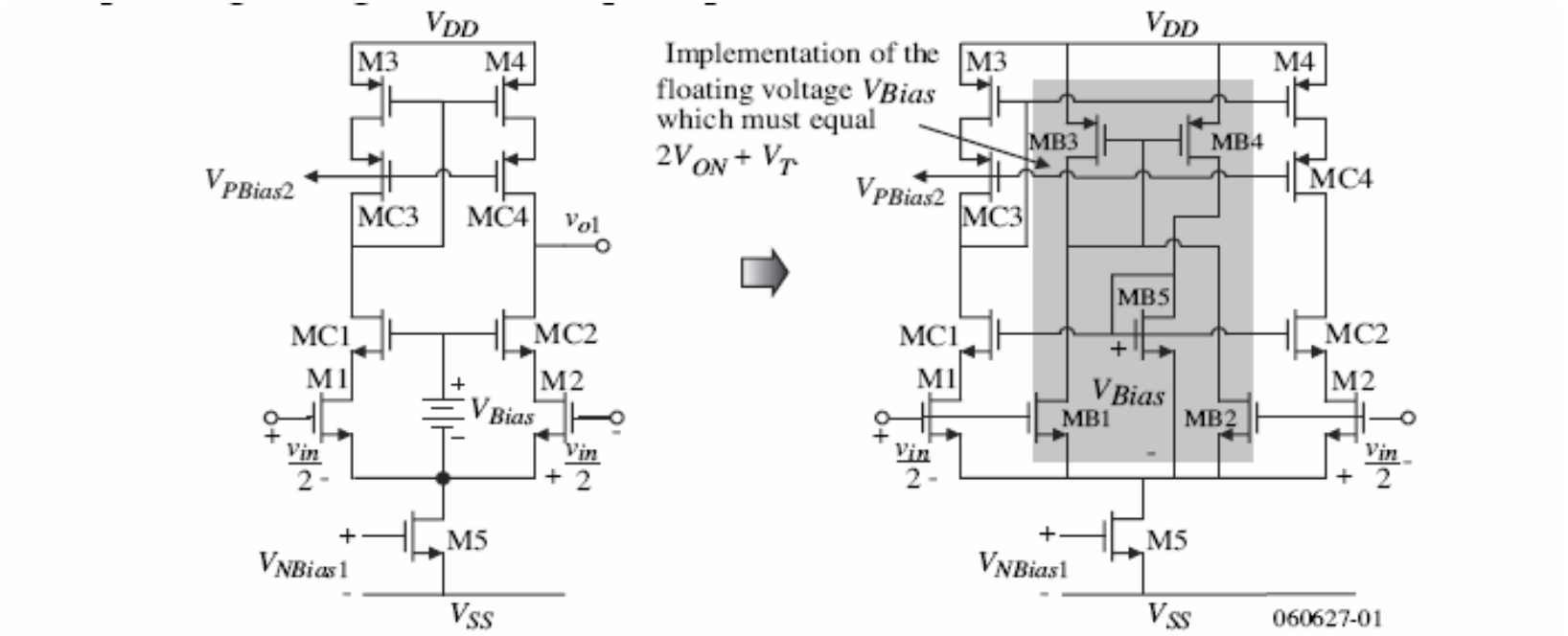
Why Cascode Op Amps?

- Control of the frequency behavior
- Can get more gain by increasing the output resistance of a stage
- In the past section, *PSRR* of the two-stage op amp was insufficient for many applications
- A two-stage op amp can become unstable for large load capacitors (if nulling resistor is not used)
- The cascode op amp leads to wider *ICMR* and/or smaller power supply requirements

Where Should the Cascode Technique be Used?

- First stage -
  - Good noise performance
  - Requires level translation to second stage
  - Degrades the Miller compensation
- Second stage -
  - Self compensating
  - Increases the efficiency of the Miller compensation
  - Increases *PSRR*

Simple Single Stage Cascode Op Amp



R_{out} of the first stage is $R_I \approx (g_{mC2}r_{dsC2}r_{ds2})||(g_{mC4}r_{dsC4}r_{ds4})$

Voltage gain $= \frac{v_{o1}}{v_{in}} = g_{m1}R_I$ [The gain is increased by approximately $0.5(g_{MC}r_{dsC})$]

As a single stage op amp, the compensation capacitor becomes the load capacitor.

Example: Single-Stage, Cascode Op Amp Performance

Assume that all W/L ratios are 10 μm/1 μm, and that $I_{DS1} = I_{DS2} =$ 50 μA of single stage op amp. Find the voltage gain of this op amp and the value of C_I if GB = 10 MHz. Use the model parameters of Table 3.1-2.

Solution

The device transconductances are

$g_{m1} = g_{m2} = g_{mI} = 331.7\ \mu$S

$g_{mC2} = 331.7\,\mu$S

$g_{mC4} = 223.6\ \mu$S.

The output resistance of the NMOS and PMOS devices is 0.5 MΩ and 0.4 MΩ, respectively.

$\therefore \quad R_I = 25$ MΩ

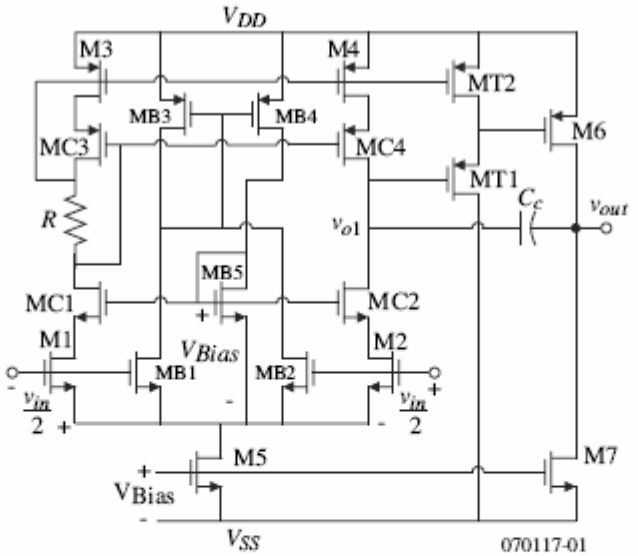
$A_V(0) = 8290$ V/V.

For a unity-gain bandwidth of 10 MHz, the value of C_I is 5.28 pF.

What happens if a 100pF capacitor is attached to this op amp?

GB goes from 10MHz to 0.53MHz.

Two-Stage Op Amp with a Cascoded First-Stage



- MT1 and MT2 are required for level shifting from the first-stage to the second.
- The $PSRR^+$ is improved by the presence of MT1
- Internal loop pole at the gate of M6 may cause the Miller compensation to fail.
- The voltage gain of this op amp could easily be 100,000V/V

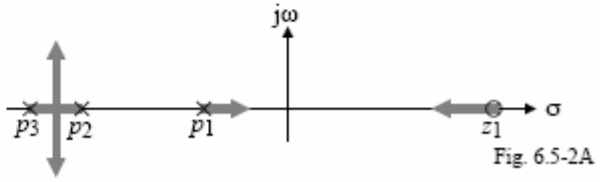


Fig. 6.5-2A

Two-Stage Op Amp with a Cascode Second-Stage

$$A_v = g_{mI} g_{mII} R_I R_{II}$$

where $g_{mI} = g_{m1} = g_{m2}$, $g_{mII} = g_{m6}$,

$$R_I = \frac{1}{g_{ds2} + g_{ds4}} = \frac{2}{(\lambda_2 + \lambda_4) I_{D5}}$$

and

$$R_{II} = (g_{mC6} r_{dsC6} r_{ds6}) \| (g_{mC7} r_{dsC7} r_{ds7})$$

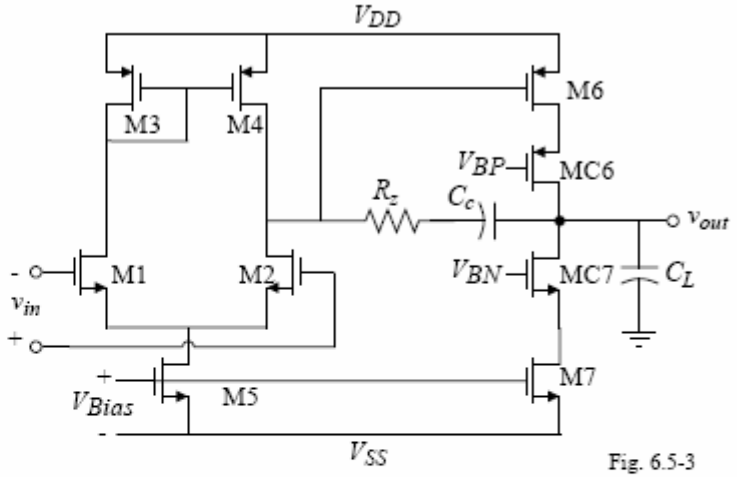
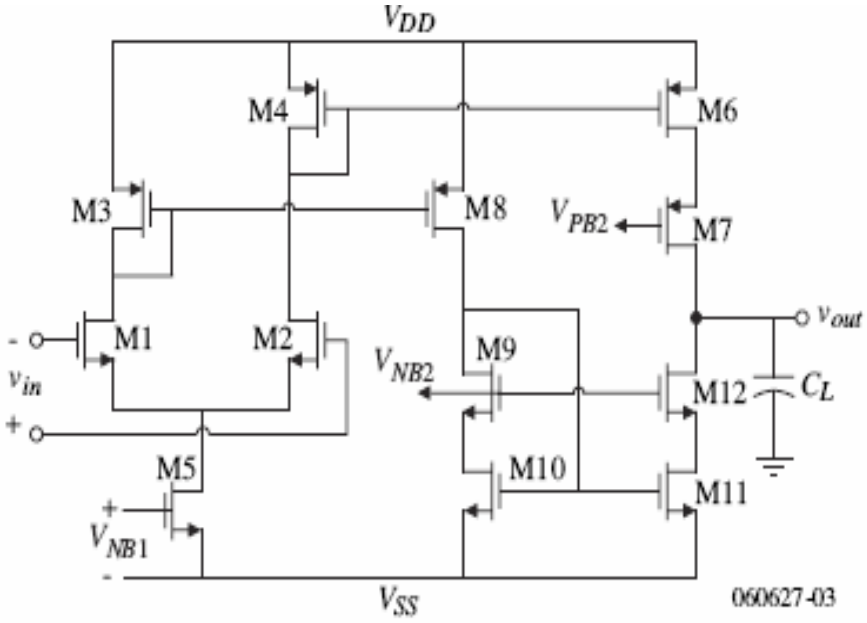


Fig. 6.5-3

Comments:

- The second-stage gain has greatly increased improving the Miller compensation
- The overall gain is approximately $(g_m r_{ds})^3$ or very large
- Output pole, p_2, is approximately the same if C_c is constant
- The zero RHP is the same if C_c is constant
- PSRR is poor unless the Miller compensation is removed (then the op amp becomes self compensated)

A Balanced, Two-Stage Op Amp using a Cascode Output Stage



$$v_{out} = \left(\frac{g_{m1}g_{m8}}{g_{m3}}\frac{v_{in}}{2} + \frac{g_{m2}g_{m6}}{g_{m4}}\frac{v_{in}}{2}\right) R_{II}$$

$$= \left(\frac{g_{m1}}{2} + \frac{g_{m2}}{2}\right) k v_{in} R_{II} = g_{m1} \cdot k \cdot R_{II} v_{in}$$

where

$$R_{II} = (g_{m7} r_{ds7} r_{ds6}) \| (g_{m12} r_{ds12} r_{ds11})$$

and

$$k = \frac{g_{m8}}{g_{m3}} = \frac{g_{m6}}{g_{m4}}$$

This op amp is balanced because the drain-to-ground loads for M1 and M2 are identical.

Design Relationships for Balanced, Cascode Output Stage Op Amp.

$$\text{Slew rate} = \frac{I_{out}}{C_L} \qquad GB = \frac{g_{m1}g_{m8}}{g_{m3}C_L} \qquad A_v = \frac{1}{2}\left(\frac{g_{m1}g_{m8}}{g_{m3}} + \frac{g_{m2}g_{m6}}{g_{m4}}\right) R_{II}$$

$$V_{in}(\max) = V_{DD} - \left[\frac{I_5}{\beta_3}\right]^{1/2} - |V_{TO3}|(\max) + V_{T1}(\min) \qquad V_{in}(\min) = V_{SS} + V_{DS5} + \left[\frac{I_5}{\beta_1}\right]^{1/2} + V_{T1}(\min)$$

Design of Balanced, Cascoded Output Stage Op Amp

The balanced, cascoded output stage op amp is a useful alternative to the two-stage op amp. Its design will be illustrated by this example. The pertinent design equations for the op amp were given above. The specifications of the design are as follows:

$V_{DD} = -V_{SS} = 2.5$ V — Slew rate = 5 V/μs with a 50 pF load

$GB = 10$ MHz with a 25 pF load — $A_v \geq 5000$

Input CMR = −1V to +1.5 V — Output swing = ±1.5 V

Use the parameters of Table 3.1-2 and let all device lengths be 1 μm.

Solution

While numerous approaches can be taken, we shall follow one based on the above specifications. The steps will be numbered to help illustrate the procedure.

1.) The first step will be to find the maximum source/sink current. This is found from the slew rate.

$$I_{\text{source}}/I_{\text{sink}} = C_L \times \text{slew rate} = 50 \text{ pF}(5 \text{ V}/\mu\text{s}) = 250 \ \mu\text{A}$$

2.) Next some W/L constraints based on the maximum output source/sink current are developed. Under dynamic conditions, all of I_5 will flow in M4; thus we can write

$$\text{Max. } I_{\text{out}}(\text{source}) = (S_6/S_4)I_5 \quad \text{and} \quad \text{Max. } I_{out}(\text{sink}) = (S_8/S_3)I_5$$

The maximum output sinking current is equal to the maximum output sourcing current if

$$S_3 = S_4, \quad S_6 = S_8, \text{ and } S_{10} = S_{11}$$

Design of Balanced, Cascoded Output Stage Op Amp (cont)

3.) Choose I_5 as 100 μA. This current (which can be changed later) gives

$$S_6 = 2.5S_4 \quad \text{and} \quad S_8 = 2.5S_3$$

Note that S_8 could equal S_3 if $S_{11} = 2.5S_{10}$. This would minimize the power dissipation.

4.) Next design for ±1.5 V output capability. We shall assume that the output must source or sink the 250μA at the peak values of output. First consider the negative output peak. Since there is 1 V difference between V_{SS} and the minimum output, let $V_{DS11}(\text{sat}) = V_{DS12}(\text{sat}) = 0.5$ V (we continue to ignore the bulk effects). Under the maximum negative peak assume that $I_{11} = I_{12} = 250$ μA. Therefore

$$0.5 = \sqrt{\frac{2I_{11}}{K'_N S_{11}}} = \sqrt{\frac{2I_{12}}{K'_N S_{12}}} = \sqrt{\frac{500\ \mu\text{A}}{(110\ \mu\text{A/V}^2)S_{11}}}$$

which gives $S_{11} = S_{12} = 18.2$ and $S_9 = S_{10} = 18.2$. For the positive peak, we get

$$0.5 = \sqrt{\frac{2I_6}{K'_P S_6}} = \sqrt{\frac{2I_7}{K'_P S_7}} = \sqrt{\frac{500\ \mu\text{A}}{(50\ \mu\text{A/V}^2)S_6}}$$

which gives $S_6 = S_7 = S_8 = 40$ and $S_3 = S_4 = (40/2.5) = 16$.

Design of Balanced, Cascoded Output Stage Op Amp (cont)

5.) Now we must consider the possibility of conflict among the specifications.

First consider the input CMR. S_3 has already been designed as 16. Using ICMR relationship, we find that S_3 should be at least 4.1. A larger value of S_3 will give a higher value of $V_{in}(\max)$ so that we continue to use $S_3 = 16$ which gives $V_{in}(\max) = 1.95$V.

Next, check to see if the larger W/L causes a pole below the gainbandwidth. Assuming a C_{ox} of 0.4fF/μm^2 gives the first-stage pole of

$$p_3 = \frac{-g_{m3}}{C_{gs3}+C_{gs8}} = \frac{-\sqrt{2K'_P S_3 I_3}}{(0.667)(W_3L_3+W_8L_8)C_{ox}} = 33.15\text{x}10^9 \text{ rads/sec or } 5.275\text{GHz}$$

which is much greater than $10GB$.

6.) Next we find g_{m1} (g_{m2}). There are two ways of calculating g_{m1}.

(a.) The first is from the A_v specification. The gain is

$$A_v = (g_{m1}/2g_{m4})(g_{m6} + g_{m8})\, R_{II}$$

Note, a current gain of k could be introduced by making S_6/S_4 ($S_8/S_3 = S_{11}/S_3$) equal to k.

$$\frac{g_{m6}}{g_{m4}} = \frac{g_{m11}}{g_{m3}} = \sqrt{\frac{2K_P'\cdot S_6\cdot I_6}{2K_P'\cdot S_4\cdot I_4}} = k$$

Calculating the various transconductances we get $g_{m4} = 282.4$ μS, $g_{m6} = g_{m7} = g_{m8} =$ 707 μS, $g_{m11} = g_{m12} = 707$ μS, $r_{ds6} = r_{d7} = 0.16$ MΩ, and $r_{ds11} = r_{ds12} = 0.2$ MΩ. Assuming that the gain A_v must be greater than 5000 and $k = 2.5$ gives $g_{m1} > 72.43$ μS.

Design of Balanced, Cascoded Output Stage Op Amp (cont)

(b.) The second method of finding g_{m1} is from the *GB* specifications. Multiplying the gain by the dominant pole ($1/C_{II}R_{II}$) gives

$$GB = \frac{g_{m1}(g_{m6} + g_{m8})}{2g_{m4}C_L}$$

Assuming that C_L= 25 pF and using the specified *GB* gives g_{m1} = 251 μS.
Since this is greater than 72.43μS, we choose $g_{m1} = g_{m2} = 251\mu$S. Knowing I_5 gives $S_1 = S_2 = 5.7 \approx 6$.

8.) The next step is to check that S_1 and S_2 are large enough to meet the –1V input CMR specification. Use the saturation formula we find that V_{DS5} is 0.261 V. This gives S_5 = 26.7 ≈ 27. The gain becomes A_v = 6,925V/V and *GB* = 10 MHz for a 25 pF load. We shall assume that exceeding the specifications in this area is not detrimental to the performance of the op amp.

9.) Knowing the currents and *W/L* values, the bias voltages V_{NB1}, V_{NB2} and V_{PB2} can be designed.

The *W/L* values resulting from this design procedure are shown below. The power dissipation for this design is seen to be 2 mW. The next step would be simulation.

$S_1 = S_2 = 6$ $S_3 = S_4 = 16$ $S_5 = 27$
$S_6 = S_7 = S_8 = 40$ $S_9 = S_{10} = S_{11} = S_{12} = 18.2$

Technological Implications of the Cascode Configuration

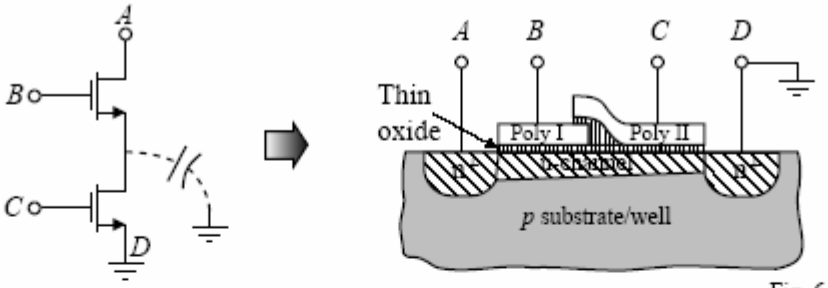


Fig. 6.5-5

If a double poly CMOS process is available, internode parasitics can be minimized.
As an alternative, one should keep the drain/source between the transistors to a minimum area.

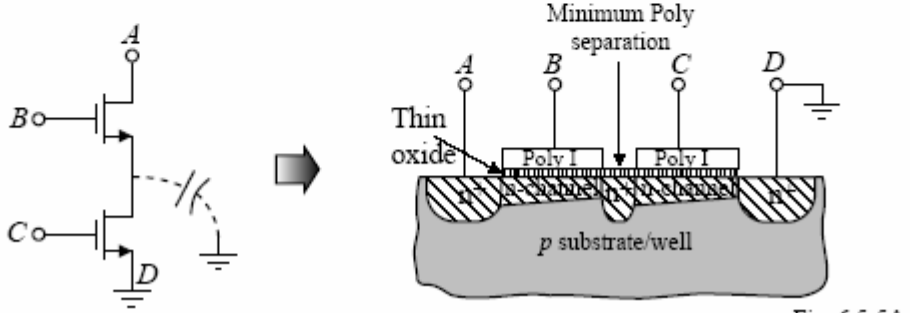
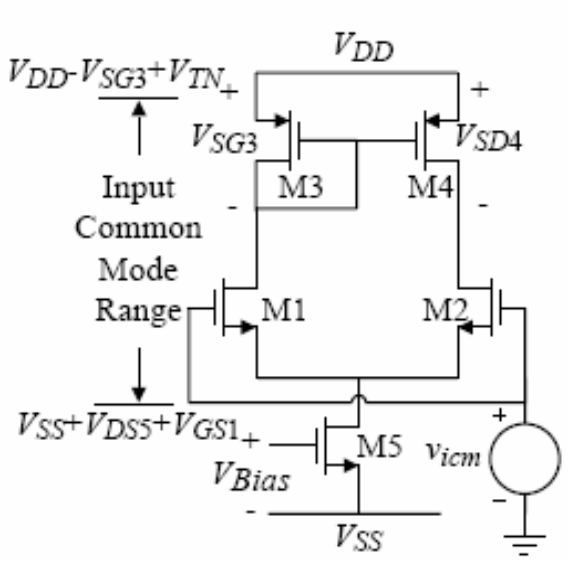
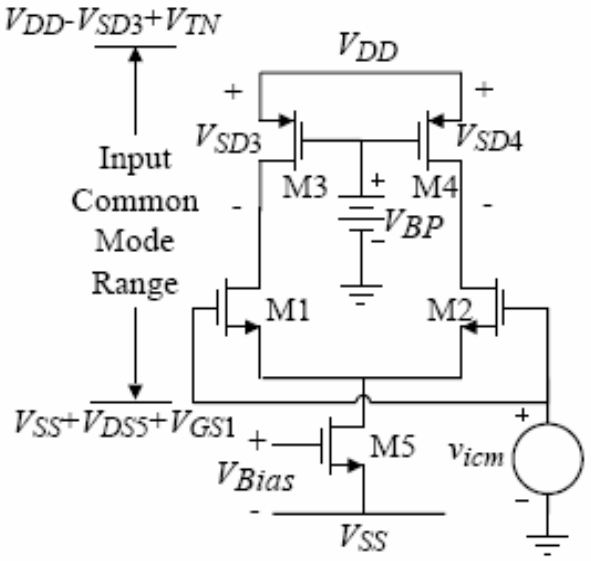


Fig. 6.5-5A

Input Common Mode Range for Two Types of Differential Amplifier Loads



Differential amplifier with a current mirror load.

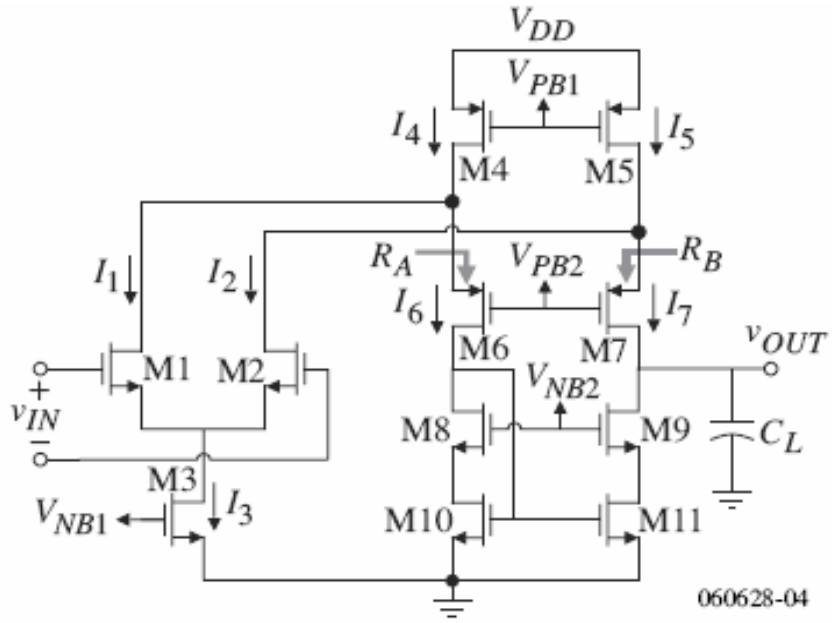


Differential amplifier with current source loads. Fig. 6.5-6

In order to improve the ICMR, it is desirable to use current source (sink) loads without losing half the gain.

The resulting solution is the *folded* cascode op amp.

The Folded Cascode Op Amp



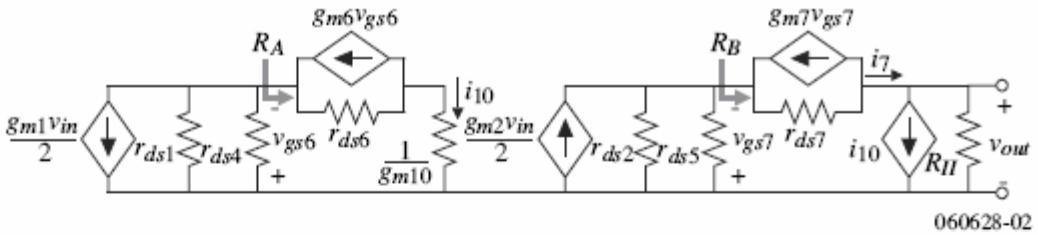
Comments:

- I_4 and I_5, should be designed so that I_6 and I_7 never become zero (i.e. I_4=I_5=1.5I_3)
- This amplifier is nearly balanced (would be exactly if R_A was equal to R_B)
- Self compensating
- Poor noise performance, the gain occurs at the output so all intermediate transistors contribute to the noise along with the input transistors. (Some first stage gain can be achieved if R_A and R_B are greater than g_{m1} or g_{m2}.

Small-Signal Analysis of the Folded Cascode Op Amp

Model:

Recalling what we learned about the resistance looking into the source of the cascode transistor;



$$R_A = \frac{r_{ds6}+(1/g_{m10})}{1+g_{m6}r_{ds6}} \approx \frac{1}{g_{m6}} \quad \text{and} \quad R_B = \frac{r_{ds7}+R_{II}}{1+g_{m7}r_{ds7}} \approx \frac{R_{II}}{g_{m7}r_{ds7}} \quad \text{where} \quad R_{II} \approx g_{m9}r_{ds9}r_{ds11}$$

The small-signal voltage transfer function can be found as follows. The current i_{10} is written as

$$i_{10} = \frac{-g_{m1}(r_{ds1}\|r_{ds4})v_{in}}{2[R_A+(r_{ds1}\|r_{ds4})]} \approx \frac{-g_{m1}v_{in}}{2}$$

and the current i_7 can be expressed as

$$i_7 = \frac{g_{m2}(r_{ds2}\|r_{ds5})v_{in}}{2\left[\frac{R_{II}}{g_{m7}r_{ds7}}+(r_{ds2}\|r_{ds5})\right]} = \frac{g_{m2}v_{in}}{2\left(1+\frac{R_{II}(g_{ds2}+g_{ds5})}{g_{m7}r_{ds7}}\right)} = \frac{g_{m2}v_{in}}{2(1+k)} \quad \text{where} \quad k = \frac{R_{II}(g_{ds2}+g_{ds5})}{g_{m7}r_{ds7}}$$

The output voltage, v_{out}, is equal to the sum of i_7 and i_{10} flowing through R_{out}. Thus,

$$\frac{v_{out}}{v_{in}} = \left(\frac{g_{m1}}{2}+\frac{g_{m2}}{2(1+k)}\right)R_{out} = \left(\frac{2+k}{2+2k}\right)g_{mI}R_{out}$$

Frequency Response of the Folded Cascode Op Amp

The frequency response of the folded cascode op amp is determined primarily by the output pole which is given as

$$p_{out} = \frac{-1}{R_{out}C_{out}}$$

where C_{out} is all the capacitance connected from the output of the op amp to ground. All other poles must be greater than $GB = g_{m1}/C_{out}$. The approximate expressions for each pole is

1.) Pole at node A: $p_A \approx - g_{m6}/C_A$
2.) Pole at node B: $p_B \approx - g_{m7}/C_B$
3.) Pole at drain of M6: $p_6 \approx -g_{m10}/C_6$
4.) Pole at source of M8: $p_8 \approx -(g_{m8}r_{ds8}g_{m10})/C_8$
5.) Pole at source of M9: $p_9 \approx -g_{m9}/C_9$

where the approximate expressions are found by the reciprocal product of the resistance and parasitic capacitance seen to ground from a given node. One might feel that because R_B is approximately r_{ds} that this pole might be too small. However, at frequencies where this pole has influence, C_{out}, causes R_{out} to be much smaller making p_B also non-dominant.

Example: Folded Cascode, CMOS Op Amp

Assume that all $g_{mN} = g_{mP} = 100\mu\text{S}$, $r_{dsN} = 2\text{M}\Omega$, $r_{dsP} = 1\text{M}\Omega$, and $C_L = 10\text{pF}$. Find all of the small-signal performance values for the folded-cascode op amp.

$R_{II} = 0.4\text{G}\Omega$, $R_A = 10\text{k}\Omega$, and $R_B = 4\text{M}\Omega$ $\therefore$ $k = \dfrac{0.4\text{x}10^{9}(0.3\text{x}10^{-6})}{100} = 1.2$

$$\frac{v_{out}}{v_{in}} = \left(\frac{2+1.2}{2+2.4}\right)(100)(57.143) = 4{,}156\text{V/V}$$

$$R_{out} = R_{II} \,\|[g_{m7} r_{ds7}(r_{ds5}\|r_{ds2})] = 400\text{M}\Omega\|[(100)(0.667\text{M}\Omega)] = 57.143\text{M}\Omega$$

$$|p_{out}| = \frac{1}{R_{out}C_{out}} = \frac{1}{57.143\text{M}\Omega \cdot 10\text{pF}} = 1{,}750 \text{ rads/sec.} \Rightarrow 278\text{Hz} \Rightarrow GB = 1.21\text{MHz}$$

PSRR of the Folded Cascode Op Amp

Consider the following circuit used to model the $PSRR^-$:

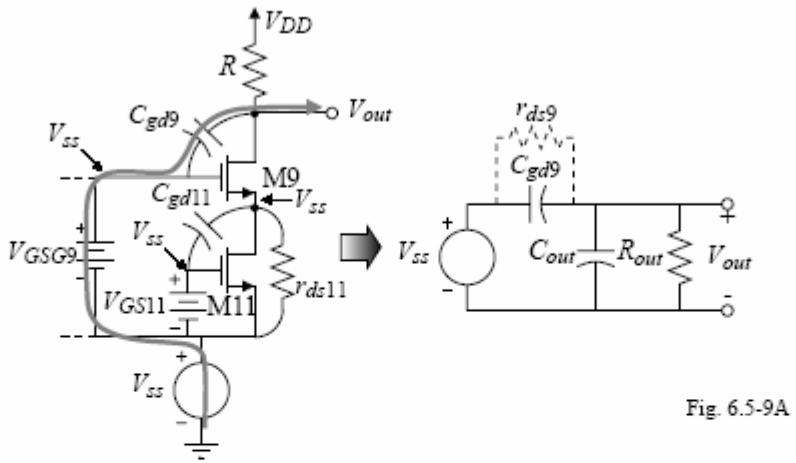


Fig. 6.5-9A

This model assumes that gate, source and drain of M11 and the gate and source of M9 all vary with V_{SS}.

We shall examine V_{out}/V_{ss} rather than $PSRR^-$. (Small V_{out}/V_{ss} will lead to large $PSRR^-$.)

The transfer function of V_{out}/V_{ss} can be found as

$$\frac{V_{out}}{V_{ss}} \approx \frac{sC_{gd9}R_{out}}{sC_{out}R_{out}+1} \quad \text{for } C_{gd9} < C_{out}$$

The approximate $PSRR^-$ is sketched on the next page.

Frequency Response of the PSRR- of the Folded Cascode Op Amp

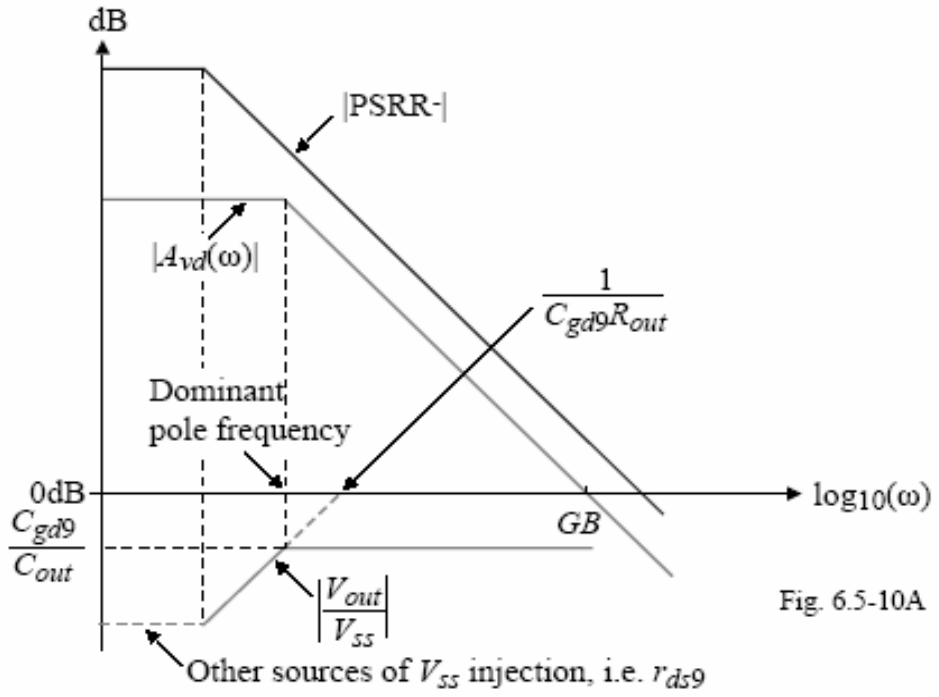


Fig. 6.5-10A

We see that the PSRR of the cascode op amp is much better than the two-stage op amp.

Design Approach for the Folded-Cascode Op Amp

Step	Relationship	Design Equation/Constraint	Comments
1	Slew Rate	$I_3 = SR \cdot C_L$	
2	Bias currents in output cascodes	$I_4 = I_5 = 1.2I_3$ to $1.5I_3$	Avoid zero current in cascodes
3	Maximum output voltage, v_{out}(max)	$S_5 = \frac{2I_5}{K_P' V_{SD5}^2}$, $S_7 = \frac{2I_7}{K_P' V_{SD7}^2}$, ($S_4$=$S_5$ and S_6= S_7)	V_{SD5}(sat)=V_{SD7}(sat) = 0.5[V_{DD}-V_{out}(max)]
4	Minimum output voltage, v_{out}(min)	$S_{11} = \frac{2I_{11}}{K_N' V_{DS11}^2}$, $S_9 = \frac{2I_9}{K_N' V_{DS9}^2}$, ($S_{10}$=$S_{11}$and S_8=S_9)	V_{DS9}(sat)=V_{DS11}(sat) = 0.5[V_{out}(min)-V_{SS}]
5	$GB = \frac{g_{m1}}{C_L}$	$S_1 = S_2 = \frac{g_{m1}^2}{K_N' I_3} = \frac{GB^2 C_L^2}{K_N' I_3}$	
6	Minimum input CM	$S_3 = \frac{2I_3}{K_N' \left(V_{in}(\min) - V_{SS} - \sqrt{(I_3/K_N' S_1)} - V_{T1}\right)^2}$	
7	Maximum input CM	$S_4 = S_5 = \frac{2I_4}{K_P' \left(V_{DD} - V_{in}(\max) + V_{T1}\right)^2}$	S_4 and S_5 must meet or exceed value in step 3
8	Differential Voltage Gain	$\frac{v_{out}}{v_{in}} = \left(\frac{g_{m1}}{2} + \frac{g_{m2}}{2(1+k)}\right) R_{out} = \left(\frac{2+k}{2+2k}\right) g_{mI} R_{out}$	$k = \frac{R_{II}(g_{ds2}+g_{ds4})}{g_{m7} r_{ds7}}$
9	Power dissipation	$P_{diss} = (V_{DD}-V_{SS})(I_3+I_{10}+I_{11})$	

Example: Design of a Folded-Cascode Op Amp

Follow the procedure given to design the folded-cascode op amp when the slew rate is 10V/μs, the load capacitor is 10pF, the maximum and minimum output voltages are ±2V for ±2.5V power supplies, the *GB* is 10MHz, the minimum input common mode voltage is -1.5V and the maximum input common mode voltage is 2.5V. The differential voltage gain should be greater than 5,000V/V and the power dissipation should be less than 5mW. Use channel lengths of 1μm.

Solution

Following the approach outlined above we obtain the following results.

$$I_3 = SR \cdot C_L = 10\text{x}10^{6} \cdot 10^{-11} = 100\mu\text{A}$$

Select $I_4 = I_5 = 125\mu$A.

Next, we see that the value of $0.5(V_{DD}\text{-}V_{out}(\text{max}))$ is 0.5V/2 or 0.25V. Thus,

$$S_4 = S_5 = \frac{2 \cdot 125\mu\text{A}}{50\mu\text{A/V}^2 \cdot (0.25\text{V})^2} = \frac{2 \cdot 125 \cdot 16}{50} = 80$$

and assuming worst case currents in M6 and M7 gives,

$$S_6 = S_7 = \frac{2 \cdot 125\mu\text{A}}{50\mu\text{A/V}^2 (0.25\text{V})^2} = \frac{2 \cdot 125 \cdot 16}{50} = 80$$

The value of $0.5(V_{out}(\text{min})\text{-}|V_{SS}|)$ is also 0.25V which gives the value of S_8, S_9, S_{10} and S_{11} as

$$S_8 = S_9 = S_{10} = S_{11} = \frac{2 \cdot I_8}{K_N' V_{DS8}^2} = \frac{2 \cdot 125}{110 \cdot (0.25)^2} = 36.36$$

Example: Design of a Folded-Cascode Op Amp (cont)

In step 5, the value of GB gives S_1 and S_2 as

$$S_1 = S_2 = \frac{GB^2 \cdot C_L^2}{K_N' I_3} = \frac{(20\pi \text{x} 10^6)^2 (10^{-11})^2}{110\text{x}10^{-6} \cdot 100\text{x}10^{-6}} = 35.9$$

The minimum input common mode voltage defines S_3 as

$$S_3 = \frac{2I_3}{K_N' \left(V_{in}(\min) - V_{SS} - \sqrt{\frac{I_3}{K_N' S_1}} - V_{T1} \right)^2} = \frac{200\text{x}10^{-6}}{110\text{x}10^{-6} \left(-1.5 + 2.5 - \sqrt{\frac{100}{110 \cdot 35.9}} - 0.7 \right)^2} = 91.6$$

We need to check that the values of S_4 and S_5 are large enough to satisfy the maximum input common mode voltage. The maximum input common mode voltage of 2.5 requires

$$S_4 = S_5 \geq \frac{2I_4}{K_P' [V_{DD} - V_{in}(\max) + V_{T1}]^2} = \frac{2 \cdot 125\mu\text{A}}{50\text{x}10^{-6} \mu\text{A/V}^2 [0.7\text{V}]^2} = 10.2$$

which is much less than 80. In fact, with $S_4 = S_5 = 80$, the maximum input common mode voltage is 3V.

The power dissipation is found to be

$$P_{diss} = 5\text{V}(125\mu\text{A} + 125\mu\text{A}) = 1.25\text{mW}$$

Example: Design of a Folded-Cascode Op Amp (cont)

The small-signal voltage gain requires the following values to evaluate:

S_4, S_5: $g_m = \sqrt{2 \cdot 125 \cdot 50 \cdot 80} = 1000\mu S$ and $g_{ds} = 125\text{x}10^{-6} \cdot 0.05 = 6.25\mu S$

S_6, S_7: $g_m = \sqrt{2 \cdot 75 \cdot 50 \cdot 80} = 774.6\mu S$ and $g_{ds} = 75\text{x}10^{-6} \cdot 0.05 = 3.75\mu S$

S_8, S_9, S_{10}, S_{11}: $g_m = \sqrt{2 \cdot 75 \cdot 110 \cdot 36.36} = 774.6\mu S$ and $g_{ds} = 75\text{x}10^{-6} \cdot 0.04 = 3\mu S$

S_1, S_2: $g_{mI} = \sqrt{2 \cdot 50 \cdot 110 \cdot 35.9} = 628\mu S$ and $g_{ds} = 50\text{x}10^{-6}(0.04) = 2\mu S$

Thus,

$$R_{II} \approx g_{m9} r_{ds9} r_{ds11} = (774.6\mu S)\left(\frac{1}{3\mu S}\right)\left\|\left(\frac{1}{3\mu S}\right)\right. = 86.07\text{M}\Omega$$

$$R_{out} \approx 86.07\text{M}\Omega \| (774.6\mu S)\left(\frac{1}{3.75\mu S}\right)\left\|\left(\frac{1}{2\mu S + 6.25\mu S}\right)\right. = 19.40\text{M}\Omega$$

$$k = \frac{R_{II}(g_{ds2}+g_{ds4})}{g_{m7} r_{ds7}} = \frac{86.07\text{M}\Omega(2\mu S + 6.25\mu S)(3.75\mu S)}{774.6\mu S} = 3.4375$$

The small-signal, differential-input, voltage gain is

$$A_{vd} = \left(\frac{2+k}{2+2k}\right) g_{mI} R_{out} = \left(\frac{2+3.4375}{2+6.875}\right) 0.628\text{x}10^{-3} \cdot 19.40\text{x}10^{6} = 7{,}464 \text{ V/V}$$

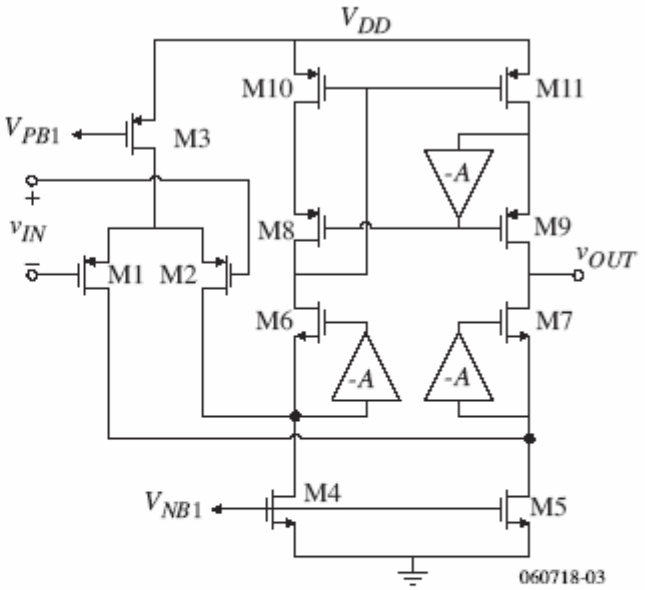
The gain is larger than required by the specifications which should be okay.

Comments on Folded Cascode Op Amps

- Good PSRR
- Good ICMR
- Self compensated
- Can cascade an output stage to get extremely high gain with lower output resistance (use Miller compensation in this case)
- Need first stage gain for good noise performance
- Widely used in telecommunication circuits where large dynamic range is required

Enhanced-Gain, Folded Cascode Op Amps

If more gain is needed, the folded cascode op amp can be enhanced to boost the output impedance even higher as follows.



Voltage gain = $g_{m1}R_{out}$,

where

$$R_{out} \approx [Ar_{ds7}g_{m7}(r_{ds1} \| r_{ds5})] \| (Ar_{ds9}g_{m9}r_{ds11})$$

Since $A \approx g_m r_{ds}$ the voltage gain would be in the range of 100,000 to 500,000.

Note that to achieve maximum output swing, it will be necessary to make sure that M5 and M11 are biased with $V_{DS} = V_{DS}(\text{sat})$.

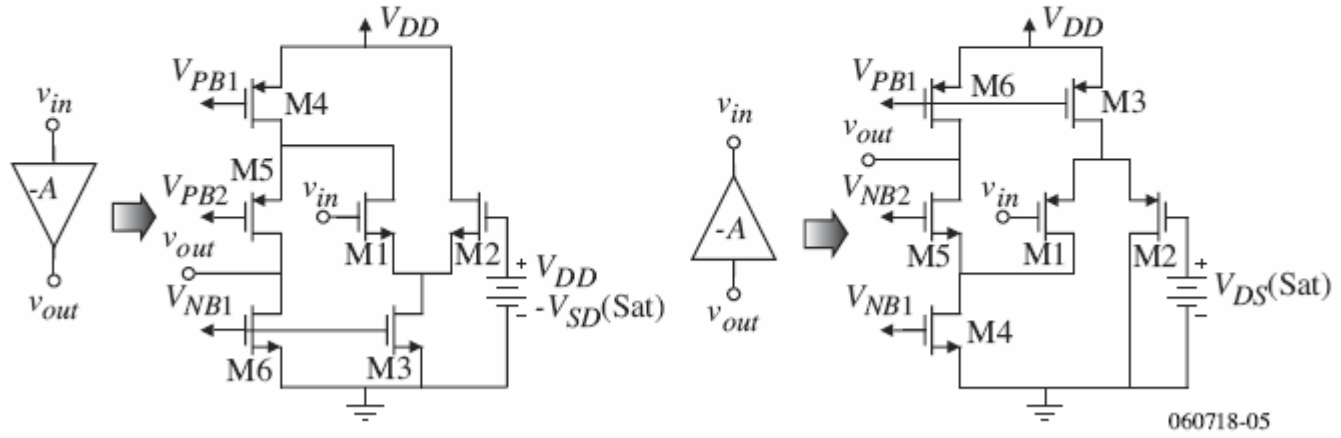
What are the Enhancement Amplifiers?

Requirements:

1.) Need a gain of $g_m r_{ds}$.

2.) Must be able to set the dc voltage at its input to get wide-output voltage swing.

Possible Enhancement Amplifiers:

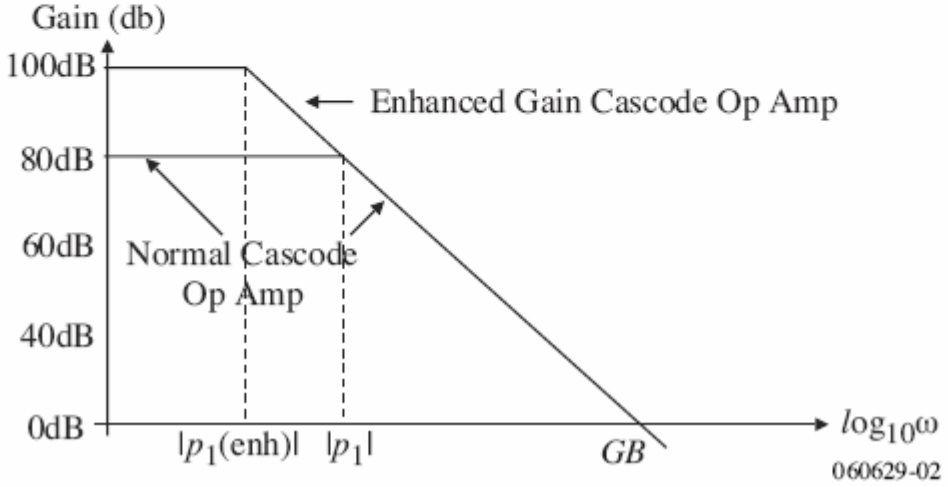


Frequency Response of the Enhanced Gain Cascode Op Amps

Normally, the frequency response of the cascode op amps would have one dominant pole at the output. The frequency response would be,

$$A_V(s) = g_{m1}\left(\frac{R_{out}(1/sC_{out})}{R_{out}+1/sC_{out}}\right) = \frac{g_{m1}R_{out}}{sR_{out}C_{out}+1} = \frac{g_{m1}R_{out}}{1-\frac{s}{p_1}}$$

If the amplifier used to boost the output resistance had no frequency dependence then the frequency response would be as follows.



Frequency Response of the Enhanced Gain Cascode Op Amps (cont)

- Does the pole in the feedback amplifier A have an influence?

  Although the output resistance can be modeled as,

$$R_{out}' \approx R_{out} A_o \left(\frac{1 - \frac{s}{p_2 A_o}}{1 - \frac{s}{p_2}} \right)$$

  it has no influence on the frequency response because C_{out} has shorted out any influence a change in R_{out} might have.

- Higher order poles come from a diversion of the current flow in the op amp to ground rather than the intended destination of the current to the output. These poles that divert the current are:
  - Pole at the source of M6 (Ag_{m6}/C_6)
  - Pole at the source of M7 (Ag_{m7}/C_7)
  - Pole at the drain of M8 (Ag_{m10}/C_8)
  - Pole at the source of M9 (Ag_{m9}/C_6)
  - Pole at the drain of M10 ($g_{m8} r_{ds8} g_{m10}/C_{10}$)

Note that the enhancement amplifiers cause all higher-order poles to be moved out by $|A|$. Therefore, the GB of the enhanced gain cascode op amp should be able to be increased by $|A|$.

Buffered Op Amps

Buffered Op Amps

- Illustrate the method of lowering the output resistance of simple op amps
  - Open-loop MOSFET buffered op amps
  - Closed-loop MOSFET buffered op amps (shunt negative feedback)
  - BJT output op amps
- Show examples

What is a Buffered Op Amp?

- A buffered op amp is an op amp with a low value of output resistance, R_o.

$$10\Omega \leq R_o \leq 1000\Omega$$

- The result is a voltage-controlled, voltage-source amplifier.
  - Requirements are generally the same as for the output amplifier:
    - Low output resistance
    - Large output signal swing
    - Low distortion
    - High efficiency

The Source Follower as a Buffer

Class-A Follower:

- Simple, gain < 1
- Lower efficiency
- $R_{out} = \dfrac{1}{g_m + g_{mbs}} \approx 500$ to 1000Ω
- Level shift from input to output

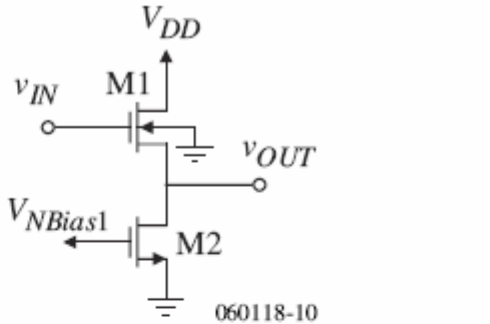
Push-Pull Follower:

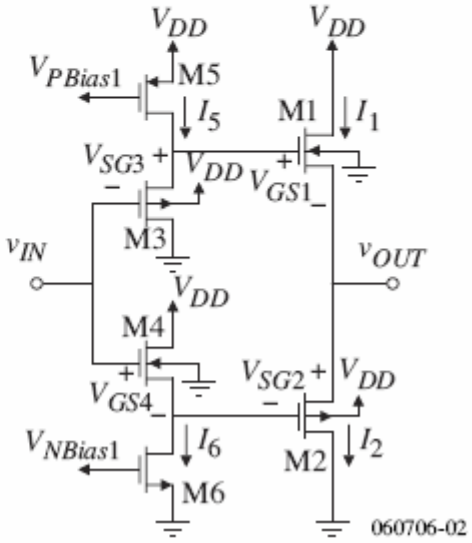
- Voltage loss from 2 cascaded followers
- Higher efficiency
- Current in M1 and M2 determined by:

$$V_{GS4} + V_{SG3} = V_{GS1} + V_{SG2}$$

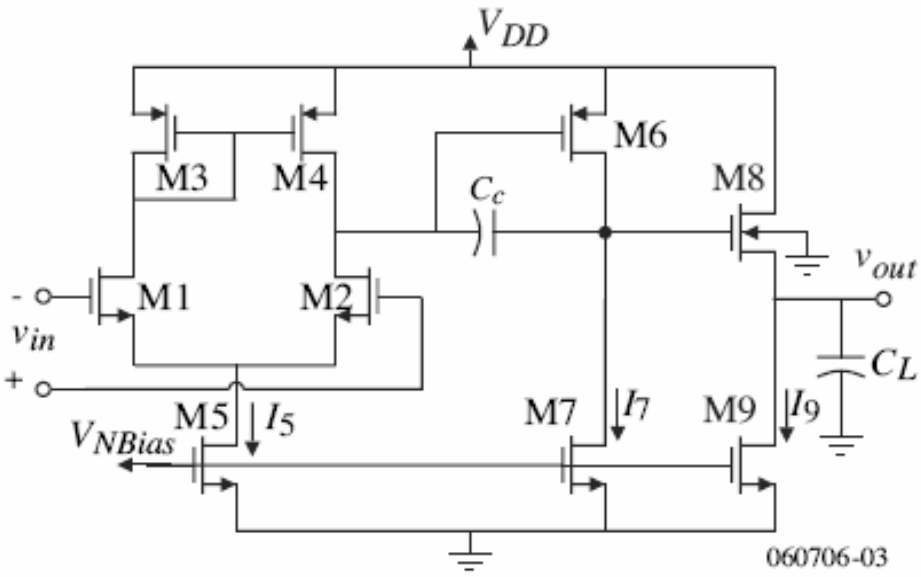
$$\sqrt{\frac{2I_6}{K_n'(W_4/L_4)}} + \sqrt{\frac{2I_5}{K_p'(W_3/L_3)}} = \sqrt{\frac{2I_1}{K_n'(W_1/L_1)}} + \sqrt{\frac{2I_2}{K_p'(W_2/L_2)}}$$

Use the W/L ratios to define I_1 and I_2 from I_5 and I_6





Two-Stage Op Amp with Follower



Power dissipation now becomes $(I_5 + I_7 + I_9)V_{DD}$

Gain becomes,

$$A_v = \left(\frac{g_{m1}}{g_{ds2}+g_{ds4}}\right)\left(\frac{g_{m6}}{g_{ds6}+g_{ds7}}\right)\left(\frac{g_{m8}}{g_{m8}+ g_{mbs8}+g_{ds8}+g_{ds9}}\right)$$

Source-Follower, Push-Pull Output Op Amp

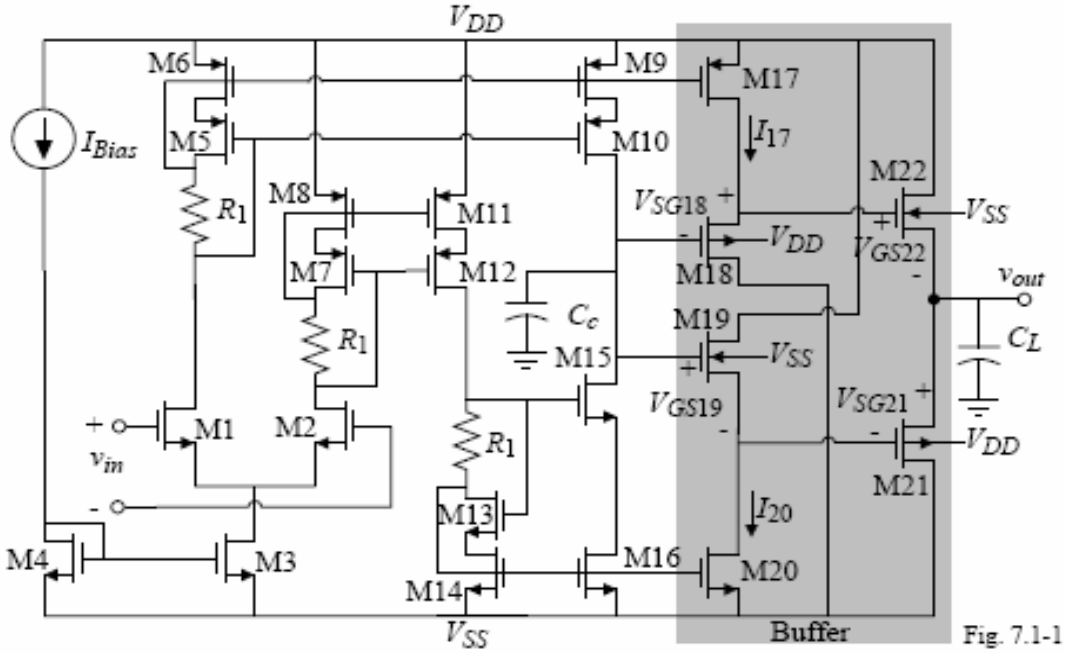


Fig. 7.1-1

$R_{out} \approx \frac{1}{g_{m21}+g_{m22}} \leq 1000\Omega$, $A_v(0)$=65dB (I_{Bias}=50μA), and GB = 60MHz for C_L = 1pF

Compensation of Op Amps with Output Amplifiers

Compensation of a three-stage amplifier:

This op amp introduces a third pole, p'_3 (what about zeros?)

With no compensation,

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{-A_{vo}}{\left(\frac{s}{p'_1} - 1\right)\left(\frac{s}{p'_2} - 1\right)\left(\frac{s}{p'_3} - 1\right)}$$

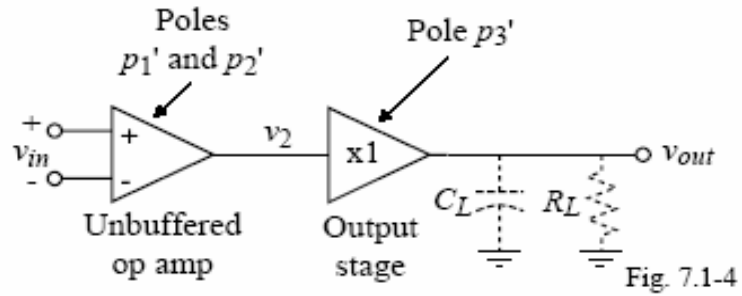
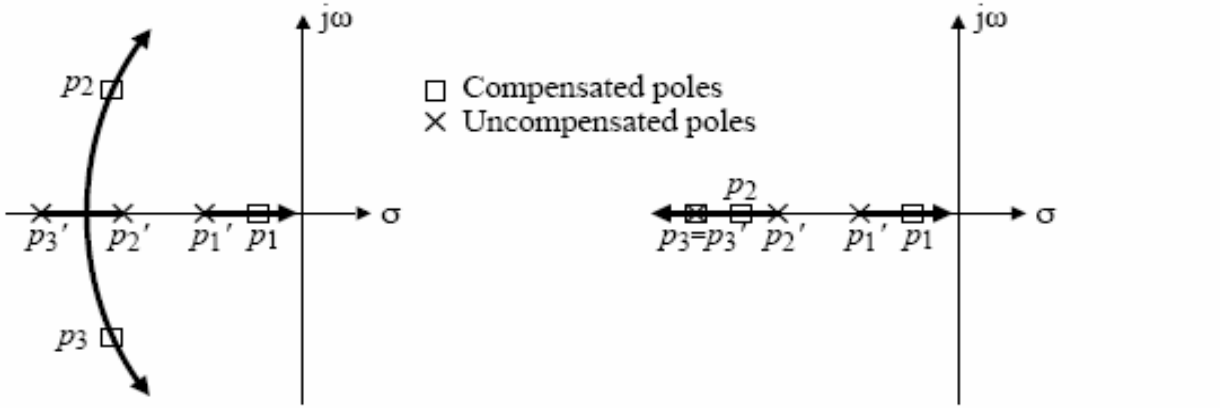


Fig. 7.1-4

Illustration of compensation choices:



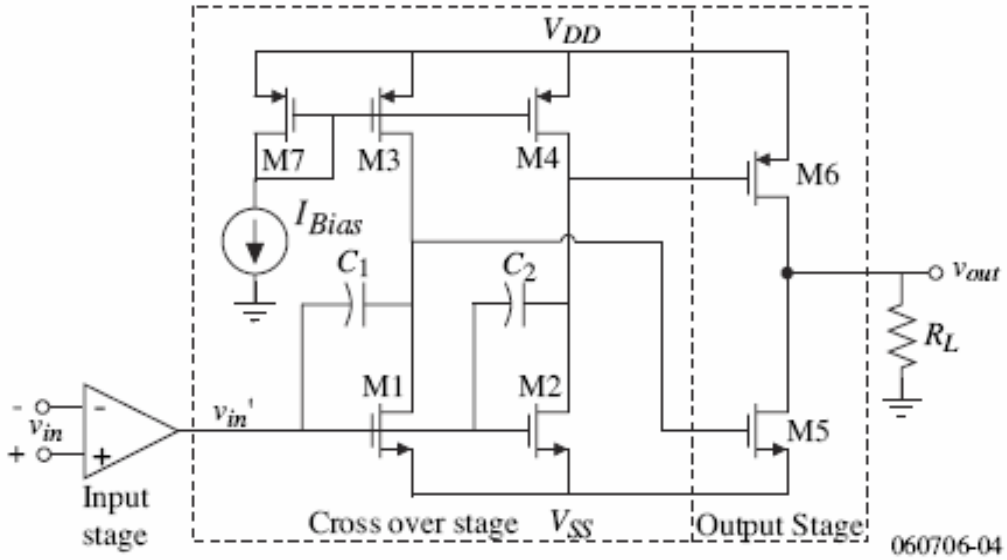
Miller compensation applied around both the second and the third stage.

Miller compensation applied around the second stage only.

Fig. 7.1-5

Crossover-Inverter, Buffer Stage Op Amp

Principle: If the buffer has high output resistance and voltage gain (common source), this is okay if when loaded by a small R_L the gain of this stage is approximately unity.



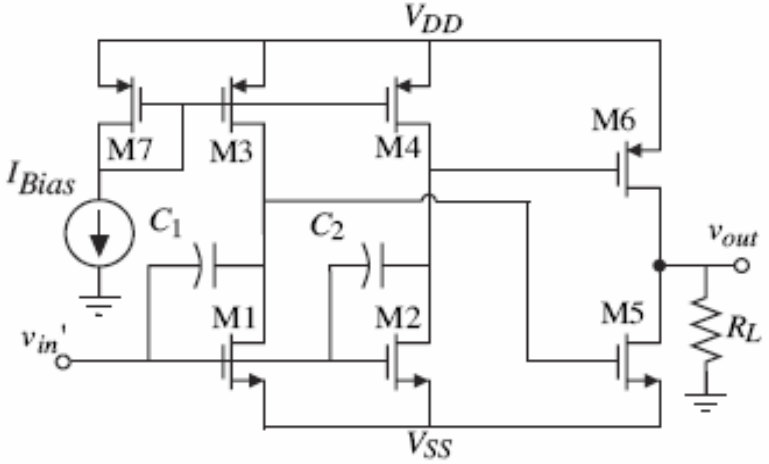
This op amp is capable of delivering 160mW to a 100Ω load while only dissipating 7mW of quiescent power!

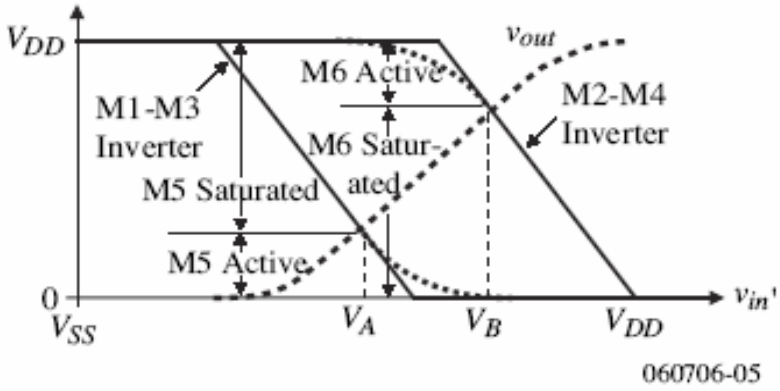
Crossover-Inverter, Buffer Stage Op Amp - Continued

How does the output buffer work?

The two inverters, M1-M3 and M2-M4 are designed to work over different regions of the buffer input voltage, v_{in}'.

Consider the idealized voltage transfer characteristic of the crossover inverters:





Crossover voltage $\equiv V_C = V_B - V_A \geq 0$

V_C is designed to be small and positive for worst case variations in processing.

Low Output Resistance Op Amp

To get low output resistance using MOSFETs, negative feedback must be used.

Ideal implementation:

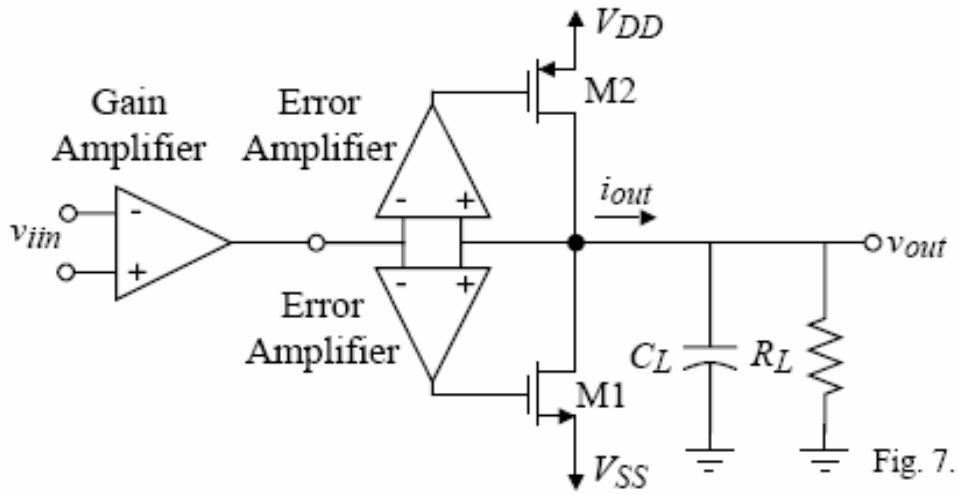


Fig. 7.1-5A

Comments:

- The output resistance will be equal to $r_{ds1} || r_{ds2}$ divided by the loop gain
- If the error amplifiers are not perfectly matched, the bias current in M1 and M2 is not defined

Low Output Resistance Op Amp - Continued

Offset correction circuitry:

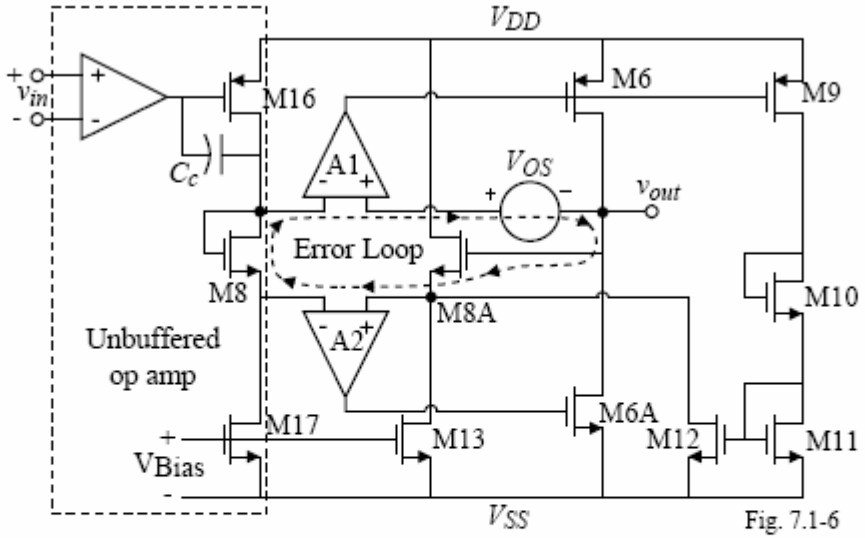


Fig. 7.1-6

The feedback circuitry of the two error amplifiers tries to insure that the voltages in the loop sum to zero. Without the M9-M12 feedback circuit, there is no way to adjust the output for any error in the loop. The circuit works as follows:

When V_{OS} is positive, M6 tries to turn off and so does M6A. I_{M9} reduces thus reducing I_{M12}. A reduction in I_{M12} reduces I_{M8A} thus decreasing V_{GS8A}. V_{GS8A} ideally decreases by an amount equal to V_{OS}. A similar result holds for negative offsets and offsets in $EA2$.

Low Output Resistance Op Amp - Continued

Error amplifiers:

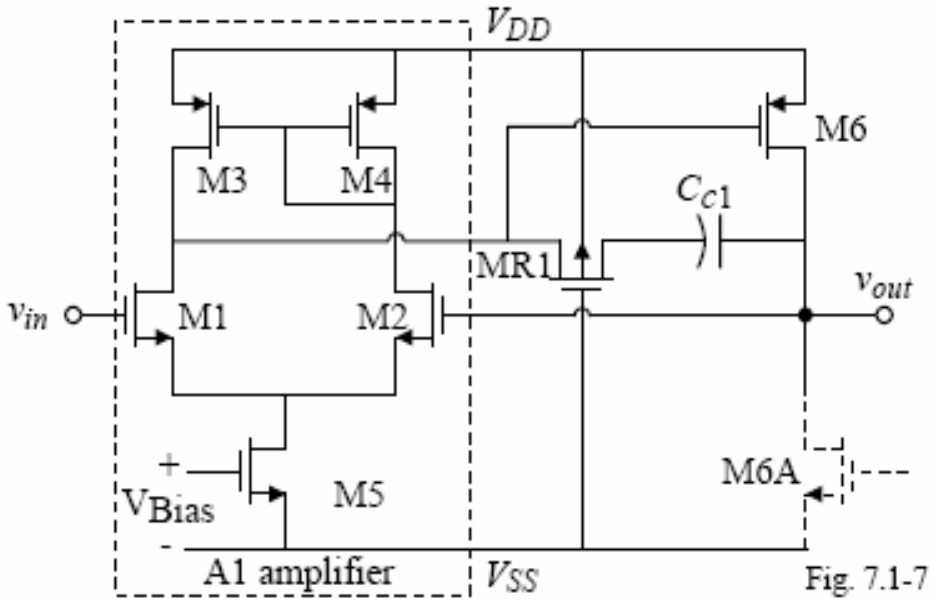
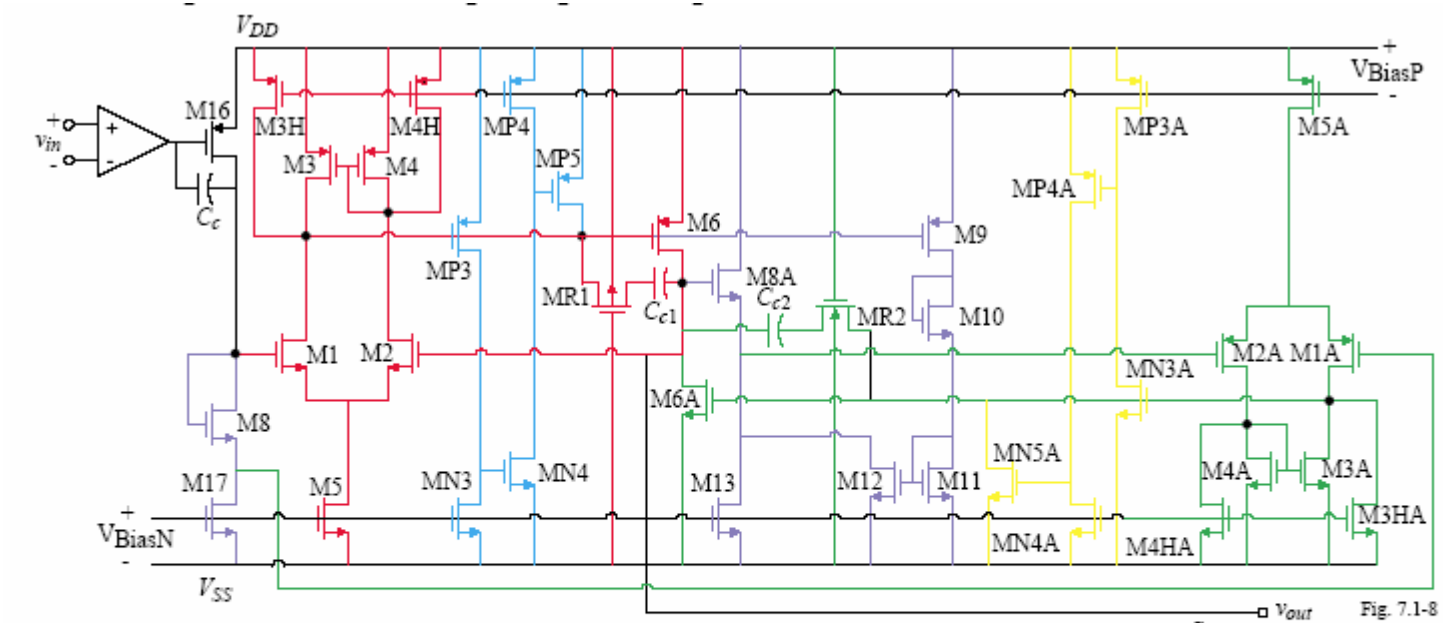


Fig. 7.1-7

Low Output Resistance Op Amp – Complete Schematic

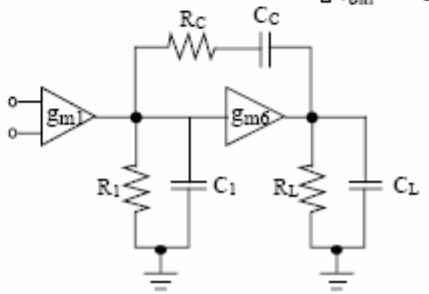


Short circuit protection(max. output ±60mA):

MP3-MN3-MN4-MP4-MP5

MN3A-MP3A-MP4A-MN4A-MN5A

$$R_{out} \approx \frac{r_{ds6} \| r_{ds6A}}{\text{Loop Gain}} \approx \frac{50\text{k}\Omega}{5000} = 10\Omega$$



Simpler Implementation of Negative Feedback to Achieve Low Output Resistance

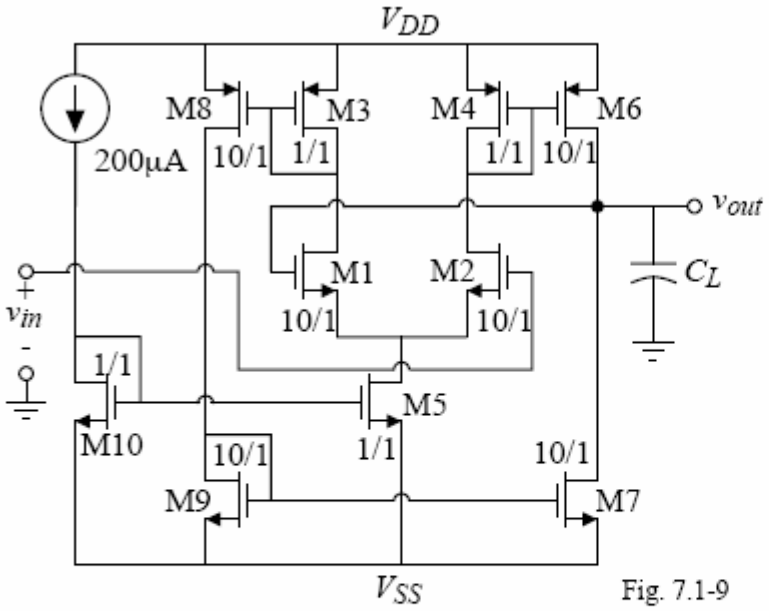


Fig. 7.1-9

Output Resistance:

$$R_{out} = \frac{R_o}{1+LG}$$

where

$$R_o = \frac{1}{g_{ds6}+g_{ds7}}$$

and

$$|LG| = \frac{g_{m2}}{2g_{m4}}(g_{m6}+g_{m7})R_o$$

Therefore, the output resistance is:

$$R_{out} = \frac{1}{(g_{ds6}+g_{ds7})\left[1+\left(\frac{g_{m2}}{2g_{m4}}\right)(g_{m6}+g_{m7})R_o\right]}$$

Example - Low Output Resistance Using Shunt Negative Feedback Buffer

Find the output resistance of above op amp using the model parameters of Table 3.1-2.

Solution

The current flowing in the output transistors, M6 and M7, is 1mA which gives R_o of

$$R_o = \frac{1}{(\lambda_N+\lambda_P)1\text{mA}} = \frac{1000}{0.09} = 11.11\text{k}\Omega$$

To calculate the loop gain, we find that

$$g_{m2} = \sqrt{2K_N' \cdot 10 \cdot 100\mu\text{A}} = 469\mu\text{S}$$

$$g_{m4} = \sqrt{2K_P' \cdot 1 \cdot 100\mu\text{A}} = 100\mu\text{S}$$

and

$$g_{m6} = \sqrt{2K_P' \cdot 10 \cdot 1000\mu\text{A}} = 1\text{mS}$$

Therefore, the loop gain is

$$|LG| = \frac{469}{100}\ 12 \cdot 11.11 = 104.2$$

Solving for the output resistance, R_{out}, gives

$$R_{out} = \frac{11.11\text{k}\Omega}{1 + 104.2} = 106\Omega \text{(Assumes that } R_L \text{ is large)}$$

BJTs Available in CMOS Technology

Illustration of an NPN substrate BJT available in a p-well CMOS technology:

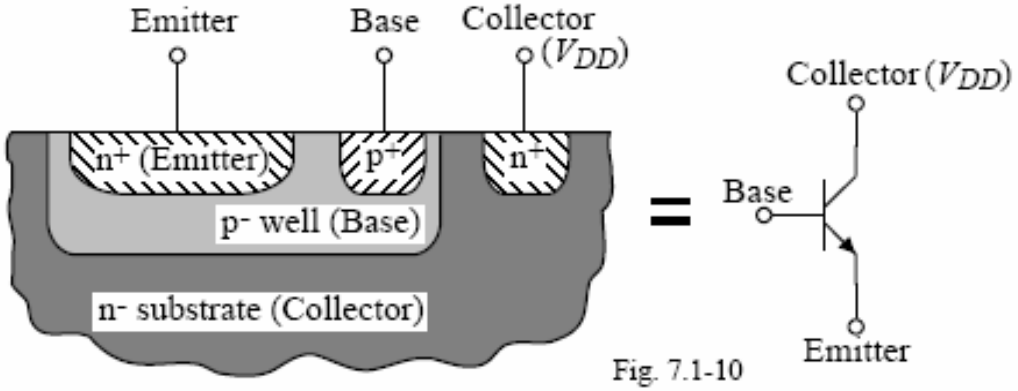


Fig. 7.1-10

Comments:

- g_m of the BJT is larger than the FET so that the output resistance w/o feedback is lower
- Can use the lateral or substrate BJT but since the collector is on ac ground, the substrate BJT is preferred
- Current is required to drive the BJT

Two-Stage Op Amp with a Class-A BJT Output Buffer Stage

Purpose of the M8-M9 source follower:

1.) Reduce the output resistance (includes whatever is seen from the base to ground divided by $1+\beta_F$)

2.) Reduces the output load at the drains of M6 and M7

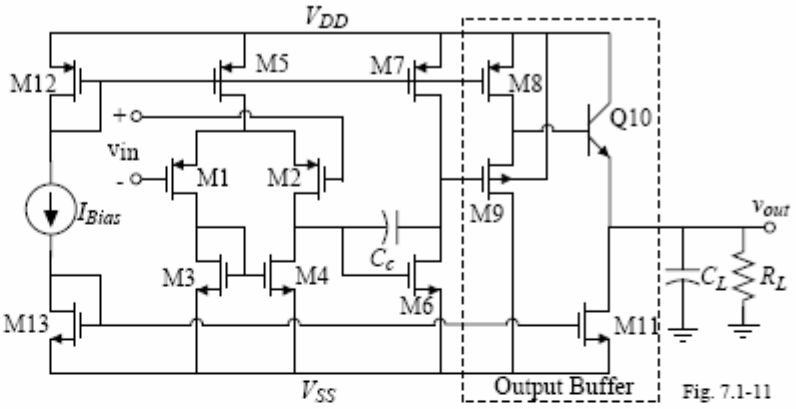


Fig. 7.1-11

Small-signal output resistance :

$$R_{out} \approx \frac{r_{\pi 10} + (1/g_{m9})}{1+\beta_F} = \frac{1}{g_{m10}} + \frac{1}{g_{m9}(1+\beta_F)}$$

$= 51.6\Omega + 6.7\Omega = 58.3\Omega$ where $I_{10}=500\mu A$, $I_8=100\mu A$, $W_9/L_9=100$ and β_F is 100

$$v_{OUT}(\max) = V_{DD} - V_{SD8}(\text{sat}) - v_{BE10} = V_{DD} - \sqrt{\frac{2K_P'}{I_8(W_8/L_8)}} - V_t \ln\left(\frac{I_{c10}}{I_{s10}}\right)$$

Voltage gain:

$$\frac{v_{out}}{v_{in}} \approx \left(\frac{g_{m1}}{g_{ds2}+g_{ds4}}\right) \left\| \left(\frac{g_{m6}}{g_{ds6}+g_{ds7}}\right) \right\| \left(\frac{g_{m9}}{g_{m9}+g_{mbs9}+g_{ds8}+g_{\pi 10}}\right) \left\| \left(\frac{g_{m10}R_L}{1+g_{m10}R_L}\right)\right.$$

Compensation will be more complex because of the additional stages.

Example - Designing the Class-A, Buffered Op Amp

Use the parameters of Table 3.1-2 along with the BJT parameters of $I_s = 10^{-14}$A and $\beta_F = 100$ to design the class-A, buffered op amp to give the following specifications. Assume the channel length is to be 1μm.

$V_{DD} = 2.5$V $V_{SS} = -2.5$V GB = 5MHz $A_{vd}(0) \geq 5000$V/V Slew rate ≥ 10V/μs

$R_L = 500\Omega$ $R_{out} \leq 100\Omega$ $C_L = 100$pF $ICMR = -1$V to 2V

Solution

Because the specifications above are similar to the two-stage design of Ex. 6.3-1, we can use these results for the first two stages of our design. However, we must convert the results of Ex. 6.3-1 to a PMOS input stage. The results of doing this give $W_1 = W_2 = 6\mu$m, $W_3 = W_4 = 7\mu$m, $W_5 = 11\mu$m, $W_6 = 43\mu$m, and $W_7 = 34\mu$m.

BJT follower:

$SR = 10$V/μs and 100pF capacitor give $I_{11} = 1$mA.

$\therefore$ If $W_{13} = 44\mu$m, then $W_{11} = 44\mu\text{m}(1000\mu\text{A}/30\mu\text{A}) = 1467\mu$m.

$I_{11} = 1\text{mA} \Rightarrow 1/g_{m10} = 0.0258\text{V}/1\text{mA} = 25.8\Omega$

MOS follower:

To source 1mA, the BJT requires 20μA ($\beta = 100$) from the MOS follower.

Therefore, select a bias current of 100μA for M8.

If $W_{12} = 44\mu$m, then $W_8 = 44\mu\text{m}(100\mu\text{A}/30\mu\text{A}) = 146\mu$m.

Example - Designing the Class-A, Buffered Op Amp

If $1/g_{m10}$ is 25.8Ω, then design g_{m9} as

$$\frac{1}{g_{m10}} = \frac{1}{g_{m9}(1+\beta_F)} = 25.8\Omega \quad \rightarrow \quad g_{m9} = \frac{1}{(25.8\Omega)(1+\beta_F)} = \frac{1}{25.8 \cdot 101} = 384\mu S$$

$\therefore \quad g_{m9}$ and $I_9 \Rightarrow W/L = 6.7$

To calculate the voltage gain of the MOS follower we need to find g_{mbs9}.

$$\therefore \qquad g_{mbs9} = \frac{g_{m9}\gamma_N}{2\sqrt{2\phi_F + V_{BS9}}} = \frac{384 \cdot 0.4}{2\sqrt{0.7+2}} = 46.7\mu S$$

where we have assumed that the value of V_{SB9} is approximately 2V.

$$\therefore \qquad A_{MOS} = \frac{384\mu S}{384\mu S + 46.7\mu S + 4\mu S + 5\mu S} = 0.873$$

The voltage gain of the BJT follower is

$$A_{BJT} = \frac{500}{25.8+500} = 0.951 \text{ V/V}$$

Thus, the gain of the op amp is

$$A_{vd}(0) = (7777)(0.873)(0.951) = 6459 \text{ V/V}$$

The power dissipation of this amplifier is,

$$P_{diss.} = 5\text{V}(1255\mu\text{A}) = 6.27\text{mW}$$

Summary

- A buffered op amp requires an output resistance between $10\Omega \leq R_o \leq 1000\Omega$
- Output resistance using MOSFETs only can be reduced by,
  - Source follower output $(1/g_m)$
  - Negative shunt feedback (frequency is a problem in this approach)
- Use of substrate (or lateral) BJT's can reduce the output resistance because g_m is larger than the g_m of a MOSFET
- Adding a buffer stage to lower the output resistance will most likely complicate the compensation of the op amp

High Frequency Op Amps

HIGH SPEED/FREQUENCY OP AMPS

- Increase the GB of operational amplifiers
  - Extending the GB of conventional op amps
- Cascading of Amplifiers
  - Voltage amplifiers
  - Voltage amplifiers using current feedback

INCREASING THE GB OF OP AMPS

What is the Influence of *GB* on the Frequency Response?

The unity-gainbandwidth represents a limit in the trade-off between closed loop voltage gain and the closed-loop -3dB frequency.

Example of a gain of -10 voltage amplifier:

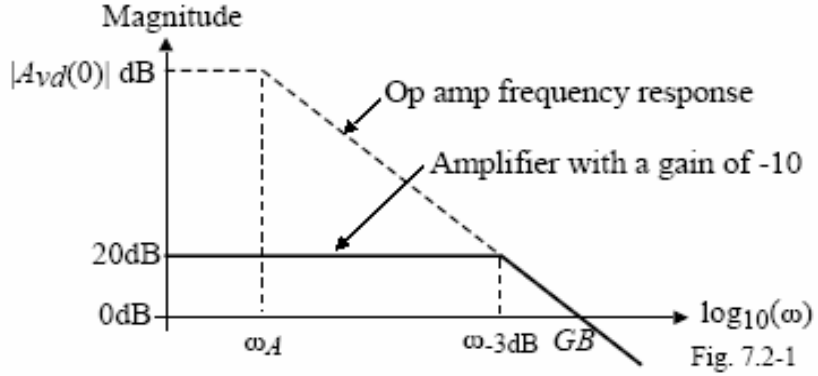


Fig. 7.2-1

What causes the *GB*?

We know that

$$GB = \frac{g_m}{C}$$

where g_m is the transconductance that converts the input voltage to current and C is the capacitor that causes the dominant pole.

This relationship assumes that all higher-order poles are greater than *GB*.

What is the Limit of Gain-Bandwidth?

The following illustrates what happens when the next higher pole is not greater than *GB*:

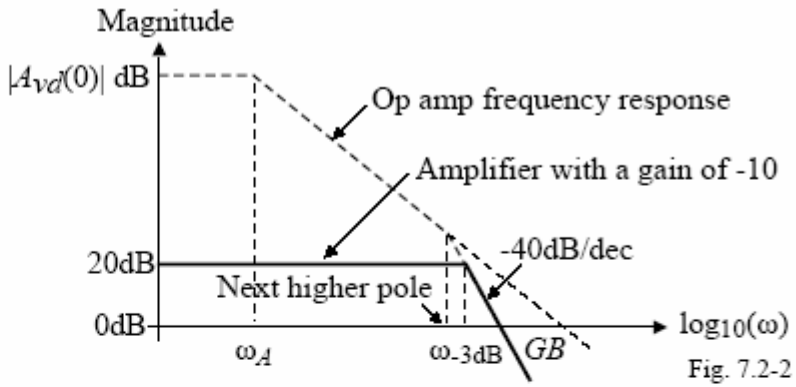


Fig. 7.2-2

For a two-stage op amp, the poles and zeros are:

1.) Dominant pole $p_1 = \dfrac{-g_{m1}}{A_V(0)C_c}$

2.) Output pole $p_2 = \dfrac{-g_{m6}}{C_L}$

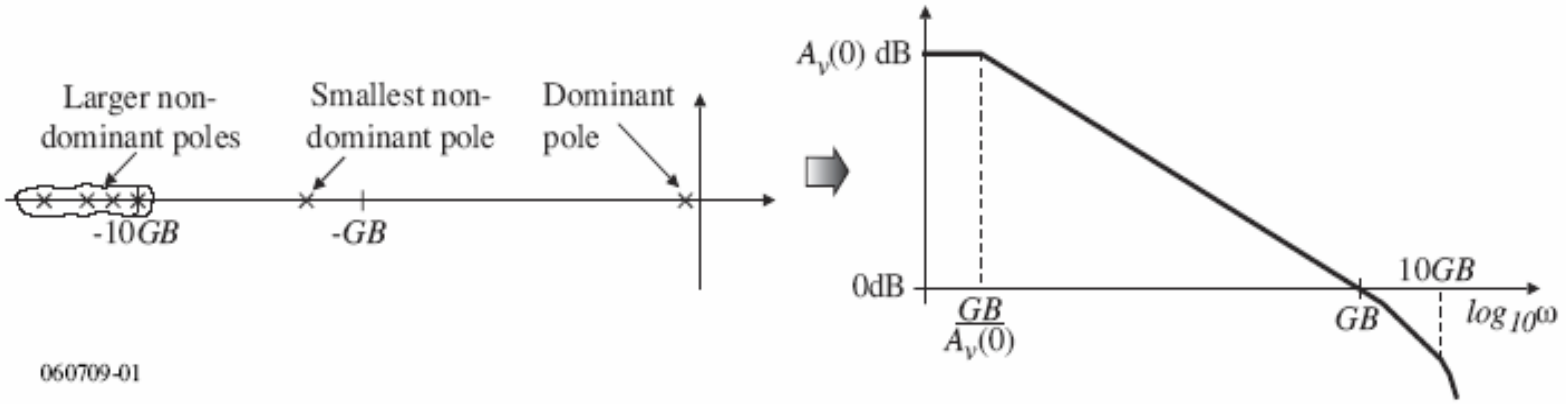
3.) Mirror pole $p_3 = \dfrac{-g_{m3}}{C_{gs3}+C_{gs4}}$ and $z_3 = 2p_3$

4.) Nulling pole $p_4 = \dfrac{-1}{R_z C_I}$

5.) Nulling zero $z_1 = \dfrac{-1}{R_z C_c - (C_c/g_{m6})}$

Higher Poles

For reasonable phase margin, the smallest higher-order pole should be 2-3 times larger than GB if all other higher-order poles are larger than $10GB$.



If the higher-order poles are not greater than $10GB$, then the distance from GB to the smallest non-dominant pole should be increased for reasonable phase margin.

Increasing the *GB* of a Two-Stage Op Amp

1.) Use the nulling zero to cancel the closest pole beyond the dominant pole.

2.) The maximum *GB* would be equal to the magnitude of the second closest pole beyond the dominant pole.

3.) Adjust the dominant pole so that $2.2GB \approx$ (second closest pole beyond the dominant pole)

Illustration which assumes that p_2 is the next closest pole beyond the dominant pole:

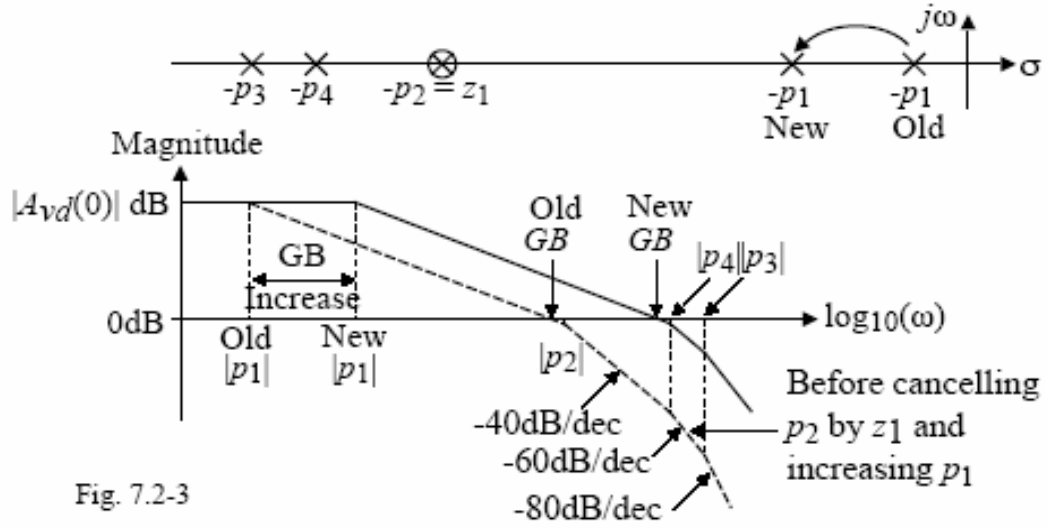


Fig. 7.2-3

Example - Increasing the *GB* of the Two-Stage Op Amp Design

Use the two-stage op amp designed in Example 6.3-1 and apply the above approach to increase the gainbandwidth as much as possible.

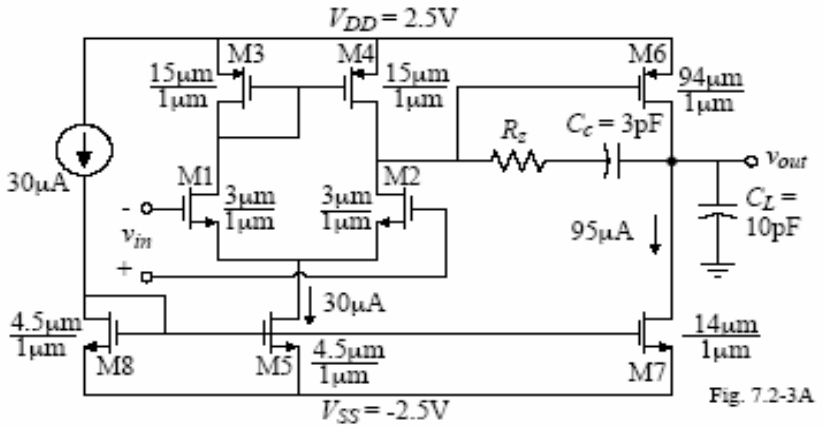


Fig. 7.2-3A

Solution

1.) First find the values of p_2, p_3, and p_4.

(a.) From Ex. 6.3-2, we see that

$p_2 = -94.25\text{x}10^6$ rads/sec.

(b.) p_3 was found in Ex. 6.3-1 as

$p_3 = -2.81\text{x}10^9$ rads/sec. (also there is a zero at $-5.62\text{x}10^9$ rads/sec.)

(c.) To find p_4, we must find C_I which is the output capacitance of the first stage of the op amp. C_I consists of the following capacitors,

$$C_I = C_{bd2} + C_{bd4} + C_{gs6} + C_{gd2} + C_{gd4}$$

For C_{bd2} the width is 3μm $\Rightarrow$ L1+L2+L3=3μm $\Rightarrow$ AS/AD=$9\mu\text{m}^2$ and PS/PD=12μm.

For C_{bd4} the width is 15μm $\Rightarrow$ L1+L2+L3=3μm $\Rightarrow$ AS/AD=$45\mu\text{m}^2$ and PS/PD=36μm.

From Table 3.2-1:

$C_{bd2} = (9\mu\text{m}^2)(770\text{x}10^{-6}\text{F/m}^2) + (12\mu\text{m})(380\text{x}10^{-12}\text{F/m}) = 6.93\text{fF}+4.56\text{fF} = 11.5\text{fF}$

$C_{bd4} = (45\mu\text{m}^2)(560\text{x}10^{-6}\text{F/m}^2) + (36\mu\text{m})(350\text{x}10^{-12}\text{F/m}) = 25.2\text{fF}+12.6\text{F} \approx 37.8\text{fF}$

Example - Increasing the *GB* of the Two-Stage Op Amp Design

C_{gs6} is given by Eq. (10b) of Sec. 3.2 and is

$$C_{gs6}=CGDO\cdot W_6+0.67(C_{ox}W_6L_6)=(220\text{x}10^{-12})(94\text{x}10^{-6})+(0.67)(24.7\text{x}10^{-4})(94\text{x}10^{-12})$$
$$= 20.7\text{fF} + 154.8\text{fF} = 175.5\text{fF}$$

$C_{gd2} = 220\text{x}10^{-12}\text{x}3\mu\text{m} = 0.66\text{fF}$ and $C_{gd4} = 220\text{x}10^{-12}\text{x}15\mu\text{m} = 3.3\text{fF}$

Therefore, $C_I = 11.5\text{fF} + 37.8\text{fF} + 175.5\text{fF} + 0.66\text{fF} + 3.3\text{fF} = 228.8\text{fF}$. Although C_{bd2} and C_{bd4} will be reduced with a reverse bias, let us use these values to provide a margin. In fact, we probably ought to double the whole capacitance to make sure that other layout parasitics are included. Thus let C_I be 300fF.

In Ex. 6.3-2, R_z was 4.591kΩ which gives $p_4 = -0.726\text{x}10^9$ rads/sec.

2.) Using the nulling zero, z_1, to cancel p_2, gives p_4 as the next smallest pole.

For 60° phase margin $GB = |p_4|/2.2$ if the next smallest pole is more than $10GB$.

$\therefore \quad GB = 0.726\text{x}10^9/2.2 = 0.330\text{x}10^9$ rads/sec. or 52.5MHz.

This value of GB is designed from the relationship that $GB = g_{m1}/C_c$. Assuming g_{m1} is constant, then $C_c = g_{m1}/GB = (94.25\text{x}10^{-6})/(0.330\text{x}10^9) = 286\text{fF}$. It might be useful to increase g_{m1} in order to keep C_c above the surrounding parasitic capacitors (C_{gd6} = 20.7fF). The success of this method assumes that there are no other roots with a magnitude smaller than $10GB$.

Example - Increasing the *GB* of the Folded Cascode Op Amp

Use the folded-cascode op amp designed in Example 6.5-3 and apply the above approach to increase the gainbandwidth as much as possible. Assume that the drain/source areas are equal to 2μm times the width of the transistor and that all voltage dependent capacitors are at zero voltage.

Solution

The poles of the folded cascode op amp are:

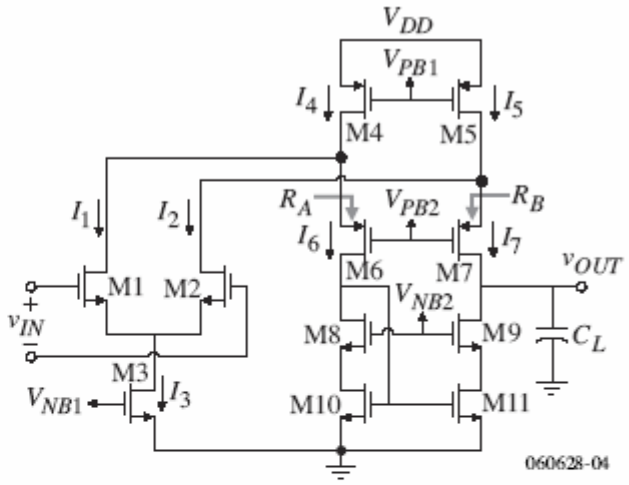
$$p_A \approx \frac{-1}{R_A C_A}$$ (the pole at the source of M6)

$$p_B \approx \frac{-1}{R_B C_B}$$ (the pole at the source of M7)

$$p_6 \approx \frac{-g_{m10}}{C_6}$$ (the pole at the drain of M6)

$$p_8 \approx \frac{-g_{m8} r_{ds8} g_{m10}}{C_8}$$ (the pole at the source of M8)

$$p_9 \approx \frac{-g_{m9}}{C_9}$$ (the pole at the source of M9)



Example - Increasing the *GB* of the Folded Cascode Op Amp (cont)

Let us evaluate each of these poles.

1.) For p_A, the resistance R_A is approximately equal to g_{m6} and C_A is given as

$$C_A = C_{gs6} + C_{bd1} + C_{gd1} + C_{bd4} + C_{bs6} + C_{gd4}$$

From Ex. 6.5-3, $g_{m6} = 744.6\mu S$ and capacitors giving C_A are found using the parameters of Table 3.2-1 as,

$$C_{gs6} = (220\text{x}10^{-12}\cdot 80\text{x}10^{-6}) + (0.67)(80\text{x}10^{-6}\cdot 10^{-6}\cdot 24.7\text{x}10^{-4}) = 149\text{fF}$$

$$C_{bd1} = (770\text{x}10^{-6})(35.9\text{x}10^{-6}\cdot 2\text{x}10^{-6}) + (380\text{x}10^{-12})(2\cdot 37.9\text{x}10^{-6}) = 84\text{fF}$$

$$C_{gd1} = (220\text{x}10^{-12}\cdot 35.9\text{x}10^{-6}) = 8\text{fF}$$

$$C_{bd4} = C_{bs6} = (560\text{x}10^{-6})(80\text{x}10^{-6}\cdot 2\text{x}10^{-6}) + (350\text{x}10^{-12})(2\cdot 82\text{x}10^{-6}) = 147\text{fF}$$

and

$$C_{gd4} = (220\text{x}10^{-12})(80\text{x}10^{-6}) = 17.6\text{fF}$$

Therefore,

$$C_A = 149\text{fF} + 84\text{fF} + 8\text{fF} + 147\text{fF} + 17.6\text{fF} + 147\text{fF} = 0.553\text{pF}$$

Thus,

$$p_A = \frac{-744.6\text{x}10^{-6}}{0.553\text{x}10^{-12}} = -1.346\text{x}10^{9} \text{ rads/sec.}$$

2.) For the pole, p_B, the capacitance connected to this node is

$$C_B = C_{gd2} + C_{bd2} + C_{gs7} + C_{gd5} + C_{bd5} + C_{bs7}$$

Example - Increasing the *GB* of the Folded Cascode Op Amp (cont)

The various capacitors above are found as

$C_{gd2} = (220\text{x}10^{-12} \cdot 35.9\text{x}10^{-6}) = 8\text{fF}$

$C_{bd2} = (770\text{x}10^{-6})(35.9\text{x}10^{-6} \cdot 2\text{x}10^{-6}) + (380\text{x}10^{-12})(2 \cdot 37.9\text{x}10^{-6}) = 84\text{fF}$

$C_{gs7} = (220\text{x}10^{-12} \cdot 80\text{x}10^{-6}) + (0.67)(80\text{x}10^{-6} \cdot 10^{-6} \cdot 24.7\text{x}10^{-4}) = 149\text{fF}$

$C_{gd5} = (220\text{x}10^{-12})(80\text{x}10^{-6}) = 17.6\text{fF}$

and

$C_{bd5} = C_{bs7} = (560\text{x}10^{-6})(80\text{x}10^{-6} \cdot 2\text{x}10^{-6}) + (350\text{x}10^{-12})(2 \cdot 82\text{x}10^{-6}) = 147\text{fF}$

The value of C_B is the same as C_A and g_{m6} is assumed to be the same as g_{m7} giving $p_B = p_A = -1.346\text{x}10^9$ rads/sec.

3.) For the pole, p_6, the capacitance connected to this node is

$C_6 = C_{bd6} + C_{gd6} + C_{gs8} + C_{gs9}$

The various capacitors above are found as

$C_{bd6} = (560\text{x}10^{-6})(80\text{x}10^{-6} \cdot 2\text{x}10^{-6}) + (350\text{x}10^{-12})(2 \cdot 82\text{x}10^{-6}) = 147\text{fF}$

$C_{gs8} = (220\text{x}10^{-12} \cdot 36.4\text{x}10^{-6}) + (0.67)(36.4\text{x}10^{-6} \cdot 10^{-6} \cdot 24.7\text{x}10^{-4}) = 67.9\text{fF}$

and

$C_{gs9} = C_{gs8} = 67.9\text{fF} \qquad C_{gd6} = C_{gd5} = 17.6\text{fF}$

Therefore,

$C_6 = 147\text{fF} + 17.6\text{fF} + 67.9\text{fF} + 67.9\text{fF} = 0.300\text{pF}$

Example - Increasing the *GB* of the Folded Cascode Op Amp (cont)

From Ex. 6.5-3, $g_{m6} = 744.6\text{x}10^{-6}$. Therefore, p_6, can be expressed as

$$-p_6 = \frac{744.6\text{x}10^{-6}}{0.300\text{x}10^{-12}} = 2.482\text{x}10^{9} \text{ rads/sec.}$$

4.) Next, we consider the pole, p_8. The capacitance connected to this node is

$$C_8 = C_{bd10} + C_{gd10} + C_{gs8} + C_{bs8}$$

These capacitors are given as,

$$C_{bs8} = C_{bd10} = (770\text{x}10^{-6})(36.4\text{x}10^{-6}\cdot 2\text{x}10^{-6}) + (380\text{x}10^{-12})(2\cdot 38.4\text{x}10^{-6}) = 85.2\text{fF}$$

$$C_{gs8} = (220\text{x}10^{-12}\cdot 36.4\text{x}10^{-6}) + (0.67)(36.4\text{x}10^{-6}\cdot 10^{-6}\cdot 24.7\text{x}10^{-4}) = 67.9\text{fF}$$

and

$$C_{gd10} = (220\text{x}10^{-12})(36.4\text{x}10^{-6}) = 8\text{fF}$$

The capacitance C_8 is equal to

$$C_8 = 67.9\text{fF} + 8\text{fF} + 85.2\text{fF} + 85.2\text{fF} = 0.246\text{pF}$$

Using the values of Ex. 6.5-3 of 774.6μS, the pole p_8 is found as,

$$-p_8 = g_{m8} r_{ds8}\, g_{m10}/C_8 = -774.6\mu\text{S}\cdot 774.6\mu\text{S}\cdot/3\mu\text{S}\cdot 0.246\text{pF} = -812.4\text{x}10^{9} \text{ rads/sec.}$$

5.) The capacitance for the pole at p_9 is identical with C_8. Therefore, since g_{m9} is 774.6μS, the pole p_9 is found to be $-p_9 = 3.149\text{x}10^{9}$ rads/sec.

Example - Increasing the *GB* of the Folded Cascode Op Amp (cont)

The poles are summarized below:

p_A = -1.346x10^9 rads/sec p_B = -1.346x10^9 rads/sec p_6 = -2.482x10^9 rads/sec

p_8 = -812.4x10^9 rads/sec p_9 = -3.149x10^9 rads/sec

The smallest of these poles is p_A or p_B. Since p_6 and p_9 are not much larger than p_A or p_B, we will find the new *GB* by dividing p_A or p_B by 6 (rather than 2.2) to get 224x10^6 rads/sec $\approx$ 200x10^6. Thus the new *GB* will be 200/2π or 32MHz. The magnitude of the dominant pole is given as

$$p_{dominant} = \frac{GB}{A_{vd}(0)} = \frac{200\text{x}10^6}{7{,}464} = 26{,}795 \text{ rads/sec.}$$

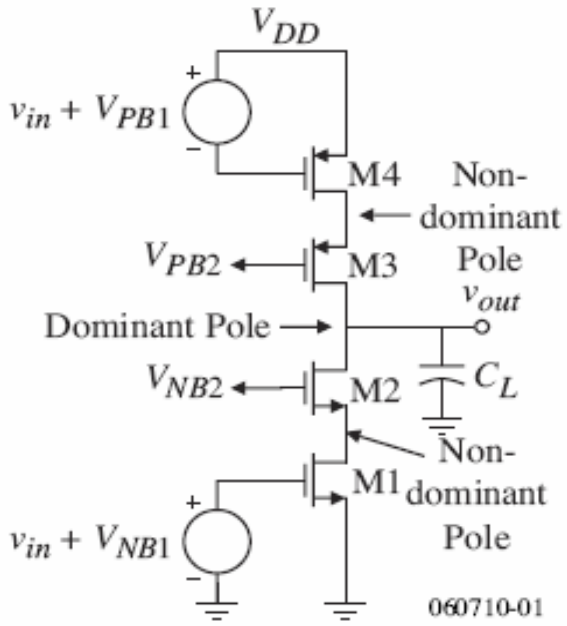
The value of load capacitor that will give this pole is

$$C_L = \frac{1}{p_{dominant} \cdot R_{out}} = \frac{1}{26.795\text{x}10^3 \cdot 19.4\text{M}\Omega} \approx 1.9\text{pF}$$

Therefore, the new *GB* = 32MHz compared with the old *GB* = 10MHz.

Elimination of Higher-Order Poles

The minimum circuitry for a cascode op amp is shown below:



If the source-drain area between M1 and M2 and M3 and M4 can be minimized, the non-dominant poles will be quite large.

CASCADED AMPLIFIERS USING CURRENT FEEDBACK AMPLIFIERS

Advantages of Using Current Feedback

Why current feedback:

- Higher *GB*
- Less voltage swing ⇒ more dynamic range

What is a current amplifier?

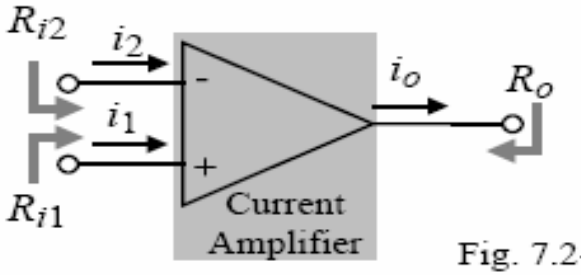


Fig. 7.2-8A

Requirements:

$i_o = A_i(i_1\text{-}i_2)$

$R_{i1} = R_{i2} = 0\Omega$

$R_o = \infty$

Ideal source and load requirements:

$R_{source} = \infty$

$R_{Load} = 0\Omega$

Bandwidth Advantage of a Current Feedback Amplifier

Consider the inverting voltage amplifier shown using a current amplifier with negative current feedback:

The output current, i_o, of the current amplifier can be written as

$$i_o = A_i(s)(i_1 - i_2) = -A_i(s)(i_{in} + i_o)$$

The closed-loop current gain, i_o/i_{in}, can be found as

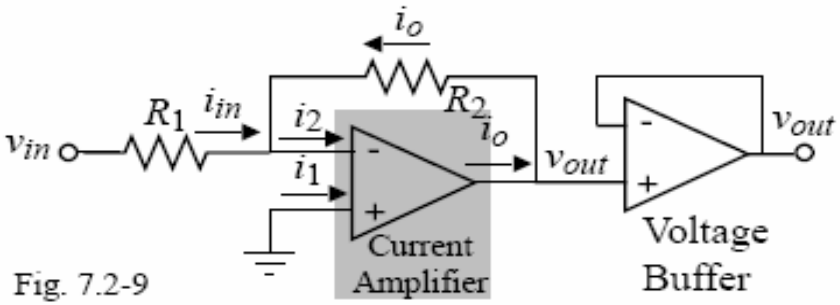


Fig. 7.2-9

$$\frac{i_o}{i_{in}} = \frac{-A_i(s)}{1+A_i(s)}$$

However, $v_{out} = i_o R_2$ and $v_{in} = i_{in} R_1$. Solving for the voltage gain, v_{out}/v_{in} gives

$$\frac{v_{out}}{v_{in}} = \frac{i_o R_2}{i_{in} R_1} = \left(\frac{-R_2}{R_1}\right)\left(\frac{A_i(s)}{1+A_i(s)}\right)$$

If $A_i(s) = \dfrac{A_o}{\dfrac{s}{\omega_A} + 1}$, then

$$\frac{v_{out}}{v_{in}} = \left(\frac{-R_2}{R_1}\right)\left(\frac{A_o}{1+A_o}\right)\left(\frac{\omega_A(1+A_o)}{s + \omega_A(1+A_o)}\right) \quad \Rightarrow \quad A_v(0) = \frac{-R_2 A_o}{R_1(1+A_o)} \quad \text{and} \quad \boxed{\omega_{-3dB} = \omega_A(1+A_o)}$$

Bandwidth Advantage of a Current Feedback Amplifier (continued)

The unity-gainbandwidth is,

$$GB = |A_v(0)|\ \omega_{-3dB} = \frac{R_2 A_o}{R_1(1+A_o)} \cdot \omega_A(1+A_o) = \frac{R_2}{R_1} A_o \cdot \omega_A = \frac{R_2}{R_1} GB_i$$

where GB_i is the unity-gainbandwidth of the current amplifier.

Note that if GB_i is constant, then increasing R_2/R_1 (the voltage gain) increases GB.

Illustration:

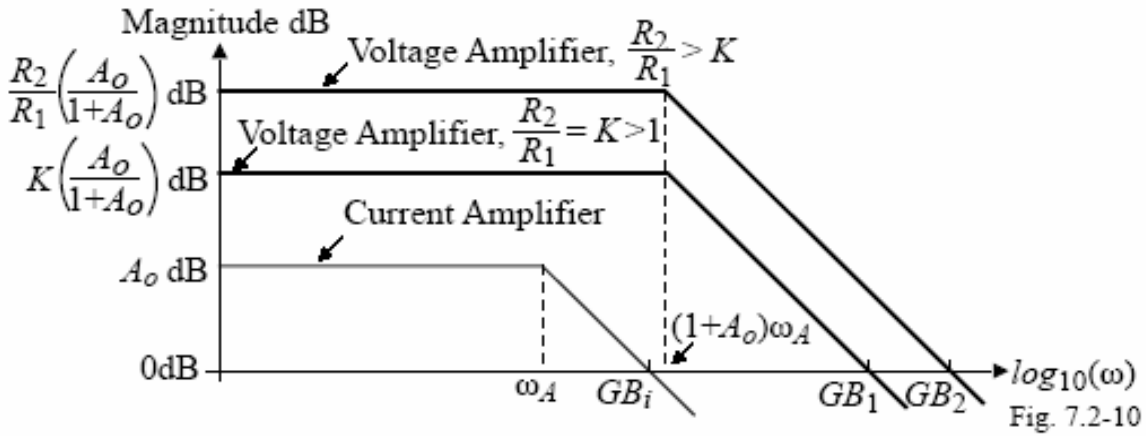


Fig. 7.2-10

Note that $GB_2 > GB_1 > GB_i$

The above illustration assumes that the *GB* of the voltage amplifier realizing the voltage buffer is greater than the *GB* achieved from the above method.

A Wide-Swing, Cascode Current Mirror as a High Frequency Amplifier

The current mirror shown below increases the value of R_2 by increasing the output resistance of the current mirror.

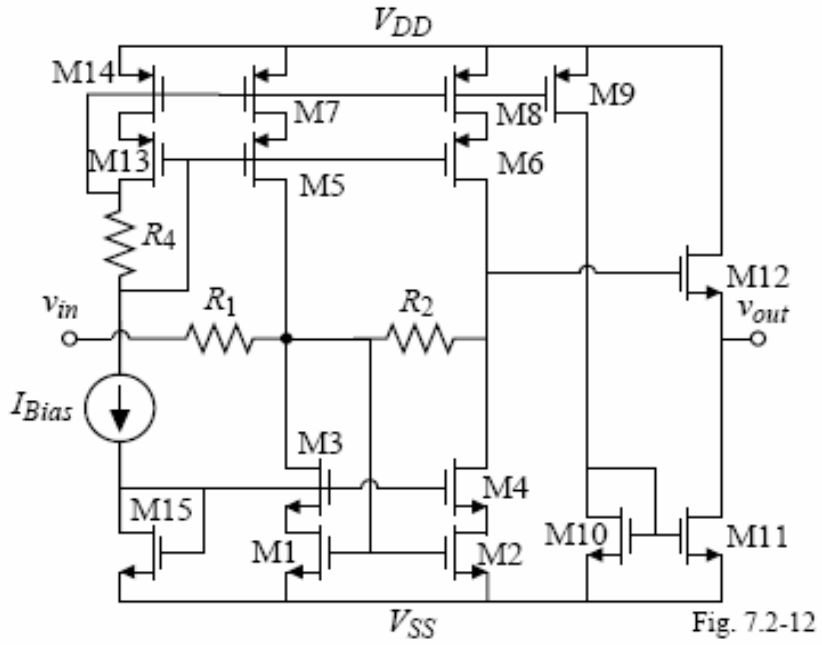


Fig. 7.2-12

Limitations:

$$R_1 > \frac{1}{g_{m1}} \text{ and } R_2 < g_{m4} r_{ds4} r_{ds2} \| g_{m6} r_{ds6} r_{ds8} \Rightarrow \frac{R_2}{R_1} << g_{m1}(g_{m4} r_{ds4} r_{ds2} \| g_{m6} r_{ds6} r_{ds8})$$

Example - Design of a High *GB* Voltage Amplifier using Current Feedback

Design the wide-swing, cascode voltage amplifier to achieve a gain of -10V/V and a *GB* of 500MHz which corresponds to a -3dB frequency of 50MHz.

Solution

Since we know what the gain is to be, let us begin by assuming that C_o will be 100fF. Thus to get a *GB* of 500MHz, R_1 must be 3.2kΩ and R_2 = 32kΩ. Therefore, $1/g_{m1}$ must be less than 3200Ω (say 300Ω). Therefore we can write

$$g_{m1} = \sqrt{2KI'(W/L)} = \frac{1}{300\Omega} \rightarrow \quad 5.56\text{x}10^{-6} = K' \cdot I \cdot \frac{W}{L} \rightarrow \quad 0.0505 = I \cdot \frac{W}{L}$$

At this point we have a problem because if W/L is small to minimize C_o, the current will be too high. If we select W/L = 200μm/1μm we will get a current of 0.25mA. However, using this W/L for M4 and M6 will give a value of C_o that is greater than 100fF. Therefore, select W/L = 200 for M1, M3, M5 and M7 and W/L = 20μm/1μm for M2, M4, M6, and M8 which gives a current in these transistors of 25μA.

Since R_2/R_1 is multiplied by 1/11 let R_2 be 110 times R_1 or 352kΩ.

Now select a W/L for M12 of 20μm/1μm which will now permit us to calculate C_o. We will assume zero-bias on all voltage dependent capacitors. Furthermore, we will assume the diffusion area as 2μm times the W. C_o can be written as

$$C_o = C_{gd4} + C_{bd4} + C_{gd6} + C_{bd6} + C_{gs12}$$

Example - Design of a High *GB* Voltage Amplifier using Current Feedback

The information required to calculate these capacitors is found from Table 3.2-1. The various capacitors are,

$C_{gd4} = C_{gd6} = CGDO \times 10\mu\text{m} = (220\text{x}10^{-12})(20\text{x}10^{-6}) = 4.4\text{fF}$

$C_{bd4} = CJ\text{x}AD_4 + CJSW\text{x}PD_4 = (770\text{x}10^{-6})(20\text{x}10^{-12}) + (380\text{x}10^{-12})(44\text{x}10^{-6})$

$= 15.4\text{fF} + 16.7\text{fF} = 32.1\text{fF}$

$C_{bd6} = (560\text{x}10^{-6})(20\text{x}10^{-12}) + (350\text{x}10^{-12})(44\text{x}10^{-6}) = 26.6\text{fF}$

$C_{gs12} = (220\text{x}10^{-12})(20\text{x}10^{-6}) + (0.67)(20\text{x}10^{-6} \cdot 10^{-6} \cdot 24.7\text{x}10^{-4}) = 37.3\text{fF}$

Therefore,

$C_o = 4.4\text{fF} + 32.1\text{fF} + 4.4\text{fF} + 26.6\text{fF} + 37.3\text{fF} = 105\text{fF}$

Note that if we had not reduced the W/L of M2, M4, M6, and M8 that C_o would have easily exceeded 100fF. Since 105fF is close to our original guess of 100fF, let us keep the values of R_1 and R_2. If this value was significantly different, then we would adjust the values of R_1 and R_2 so that the GB is 500MHz. One must also check to make sure that the input pole is greater than 500MHz.

The design is completed by assuming that $I_{Bias} = 100\mu\text{A}$ and that the current in M9 through M12 be $100\mu\text{A}$. Thus $W_{13}/L_{13} = W_{14}/L_{14} = 20\mu\text{m},/1\mu\text{m}$ and W_9/L_9 through W_{12}/L_{12} are $20\mu\text{m}/1\mu\text{m}$.

Example - Design of a High *GB* Voltage Amplifier using Current Feedback

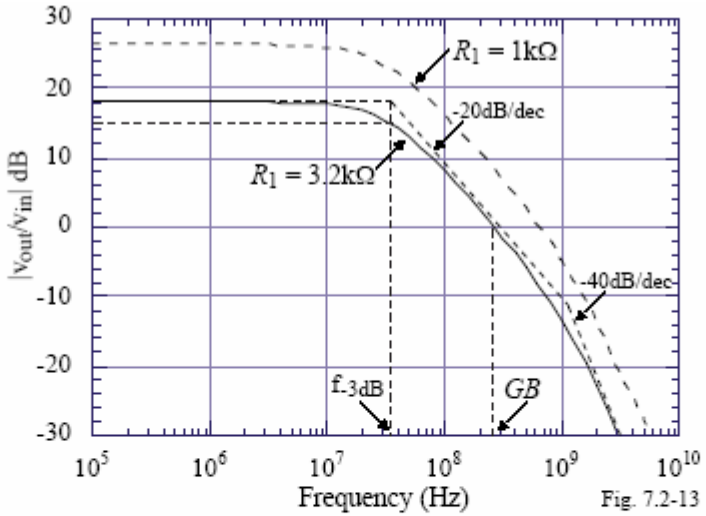


Fig. 7.2-13

Simulation Results:

$f_{-3dB} \approx 38$MHz *GB* ≈ 300MHz Closed-loop gain = 18dB

(Loss of -2dB is attributed to source follower and R_1)

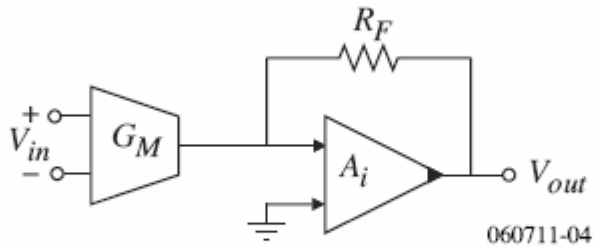
Note second pole at about 1GHz. To get these results, it was necessary to bias the input at -1.7VDC using ±3V power supplies.

If R_1 is decreased to 1kΩ results in:

Gain of 26.4dB, f_{-3dB} = 32MHz, and *GB* = 630MHz

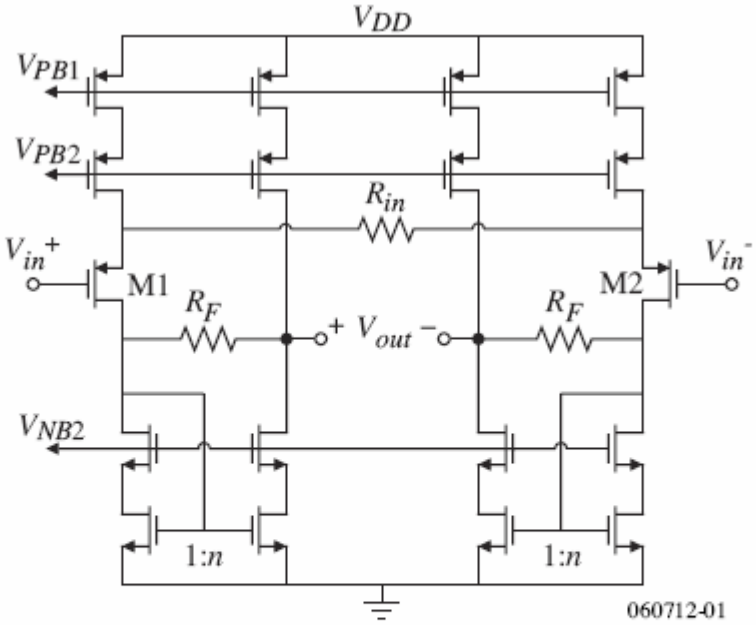
Current Feedback Amplifier

The difficulties of making the input resistance of the current amplifier small compared to R_1 can be solved with the following block diagram:



$$\frac{V_{out}}{V_{in}} = \frac{-G_M R_F A_i}{1 + A_i}$$

Differential Implementation of the Current Feedback Amplifier



$$I_{in} = \frac{g_{m1}}{1 + 0.5 g_{m1} R_{in}} \left(\frac{V_{in}^+ - V_{in}^-}{2} \right) \quad \text{and} \quad V_{out} = \frac{n\,(2R_F)}{1+n} I_{in}$$

$$\frac{V_{out}}{V_{in}} \approx \frac{2nR_F}{R_{in}}$$