Designing Operational Transconductance Amplifiers For Low Voltage Operation

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Abstract

To design Operational Transconductance Amplifiers (OTA) for high-performance applications it is necessary to use cascoded current mirrors. However, in low-voltage applications one cannot use the standard cascoded current mirror because it reduces the already limited voltage range at the the output of the OTA beyond that which is acceptable. The solution to this problem is to use the generalized high-swing cascoded current mirror, previously developed by the authors, in place of the standard cascoded current mirror. With these newer OTA designs it is possible to have cascoding in the design without significantly reducing the linear output voltage range. High-swing OTAs already do exist; however, they were limited to only single cascoded designs. With our generalized scheme one can build multiple cascoded OTAs that have significantly larger bandwidth for the same low-frequency gain than single cascoded OTAs, and do not sacrifice any of the linear output voltage range.

1. Introduction

An Operational Transconductance Amplifier (OTA) designed using the standard cascoded MOSFET current mirror [1] is of little value for low-voltage applications because of the loss of linear output voltage range that results from the cascoding of transistors. In fact, on low-voltage processes this loss of linear output voltage range is so large that it many cases one cannot use any cascoding in the OTA design at all. This severely limits the gain-bandwidth product of the OTA, and as a result some applications that were implemented on a 5 volt process cannot be implemented on a lower voltage process. The goal of this paper is to show that this problem can be largely circumvented by redesigning the OTAs using the generalized high-swing cascoded current mirror, previously described by the authors [2]. Moreover, we already know that the high-swing approach is feasible since OTA designs have been created using the single-cascoded version of the high-swing current mirror [3],[4]. Thus the originality of our work is generalizing high-swing OTAs so that multiple cascoded transistors can be used. This is no small improvement because as we will show in this paper the extra cascoding can improve the gain of the OTA without losing any of the bandwidth or linear output voltage range of the OTA. This improved gain can be use to compensate for the lost signal resolution that comes with the reduced supply voltages, by allowing circuits to have larger loop gains and thus greater accuracy. As an example, a comparison between the single and double cascoded current mirror OTA shows that the double cascoded design has a gain-bandwidth product of more than an order of magnitude greater than the single cascode design and does not sacrifice any of the linear output voltage range.

Figure 1 shows the general form of the current mirror and current steering OTA that are based on the standard cascoded current mirror. Both designs are composed of a biased NMOS differential pairs, transistors T_1 and T_2, whose differential output current is fed into either a pair of PMOS current mirrors as is the case in (a) or into a pair of PMOS folded cascode circuits as is the case in (b). The current mirror OTA then recombine the currents using an NMOS mirror, thus resulting in a single output. On the other hand, the current steering OTA simply takes the outputs after the folded cascode circuit, leaving us with a fully-differential design. In both figures we have used dashed lines to indicate that the number of cascoded transistor is arbitrary.

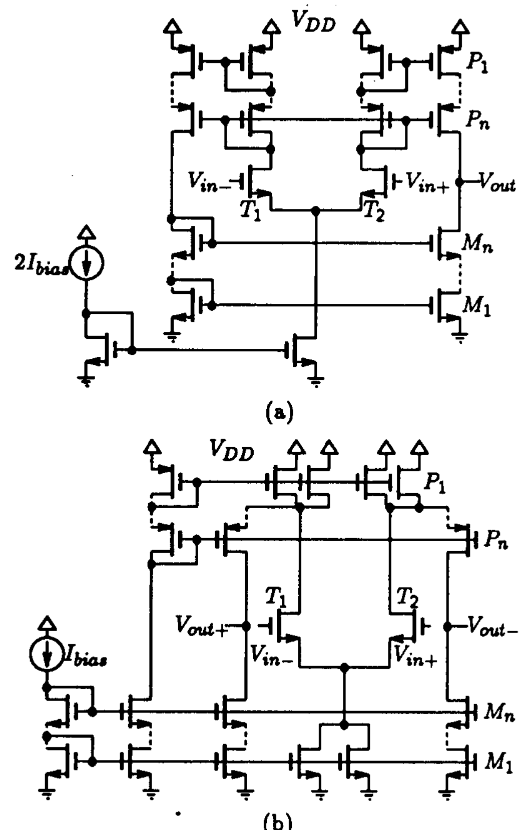

Figure 1 Cascoded OTA designs: (a) Current mirror OTA (b) Fully differential current steering OTA. Dashed lines indicate multiple cascoding

The linear output voltage range will be limited to the range of output voltages for which all of the cascoded transistors at the output are in saturation. In both the current mirror and current steering OTAs these transistors are P_1 through P_n and M_1 through M_n. The conditions that keep these transistors in saturation are set up by the standard cascoded current mirror,

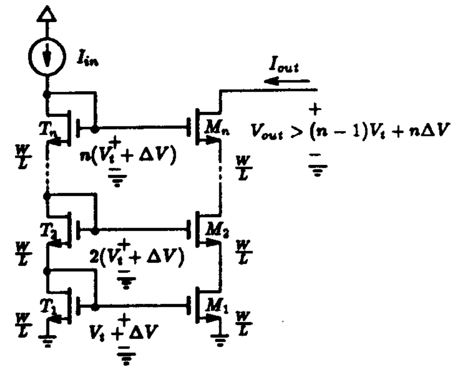

Figure 2 Cascode current mirror circuit.

which is shown in Figure 2. In this current mirror we have a chain of diode-connected transistors, labelled T_1 through T_n, with T_n being on the top. The gates of these transistors are connected to the gates of a second chain of transistors, labelled M_1 through M_n. For a general design, the transistors can have different widths and lengths. However, we will assume here that all the transistors in the current mirror, and therefore in the OTA, have the same dimensions. This simplifies the analysis of the circuit; also, described later, there are other reasons for insisting the transistors have the same dimensions. The current applied to the chain of diode-connected transistors T_1 through T_n creates a set of gate voltages which bias the second chain of transistors M_1 through M_n such that the output current I_{out} is equal to the input current I_{in}. In [2] it was shown that the linear output voltage range of this current mirror can be expressed as follows:

$$V_{out} > n\Delta V + (n-1)V_t. \tag{2}$$

Where n is the number of cascoded transistors, V_t is the threshold voltage of the MOSFET, and ΔV is given by

$$\Delta V = \sqrt{\frac{I_{in}}{K\frac{W}{L}}}. \tag{3}$$

Here K is the process dependent parameter $\mu C_{OX}/2$. ¿From Eqn. (3) we can see that each cascoded transistor reduces the linear output voltage range by $V_t + \Delta V$. While we can reduce the ΔV term by increasing the width of the transistor we cannot reduce V_t. Obviously, the limitation on a PMOS current mirror would be the same except that the process dependent parameters K and V_t would change. From this analysis we can conclude that the linear output voltage range of the OTA designs in Figure 1 would be

$$V_{linear} = V_{DD} - (n-1)V_{tN} - (n-1)V_{tP} - n\Delta V_N - n\Delta V_P. \tag{4}$$

Where the subscripts N and P indicate that the parameter is related to the NMOS and PMOS transistors, respectively. We can see how limited this range will be by taking the example of a single cascoded OTA on a 3 volt supply with V_t's of approximately 1 volt. The resulting linear range of 1 volt would be insufficient for many applications.

This paper will continue in the next section by providing a brief review of the generalized high-swing cascode current mirror. The next section will then show how to use the generalized high-swing cascode current mirror to design high-swing versions of the current steering and current mirroring OTAs. While we conclude that this result was already known for single-cascoded designs, in Section 4, it is argued that multiple cascoding leads to larger bandwidth designs for the exact same low frequency gain. As an example, we compare the designs of the single and double cascoded current mirror OTA and show how we can increase the gain-bandwidth product by more than an order of magnitude without losing any linear output voltage range. Conclusions are provided in Section 5.

2. Review Of The High-Swing Cascode Current Mirror

In this section we will briefly review the generalized high-swing cascode current mirror covered in our previous work [2].

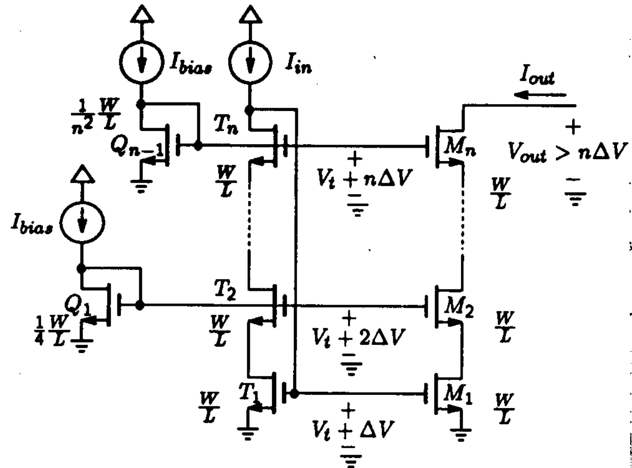

Figure 3 A generalized high-swing cascode current mirror circuit.

The structure of the high-swing multiple-cascode current mirror circuit is shown in Figure 3. It is similar to the standard cascode current mirror in that it is composed of two chains of stacked transistors. It differs in the way in which the gate voltage of each transistor pair T_i-M_i is formed. The gate voltages of the transistor pair T_i-M_i in the circuit of Figure 3 (excluding T_1-M_1) are biased independent of each other, unlike those in the standard cascoded current mirror circuit. Each transistor pair is biased using a diode-connected transistor Q_i fed by a current source I_{bias}. The input current I_{in} to the current mirror circuit of Figure 3 forces the gate-to-source voltage of each transistor T_i to be equal to $\Delta V + V_t$, where ΔV is defined in Eqn. (3), assuming of course that the transistor is in saturation. With independent control over the gate voltage of each transistor, one can ensure that each transistor is biased in the saturation region by forcing the drain-to-source voltage of each transistor to be greater than or equal to ΔV, i.e. $V_{ds} > V_{gs}$-V_t.

For example, transistor T_1 has a V_{gs} of $\Delta V + V_t$; therefore to stay in saturation its drain voltage must be greater than ΔV. This forces the value of the gate voltage on T_2 to be greater than $2\Delta V + V_t$ because its V_{gs} is equal to $V_t + \Delta V$. To place this bias voltage on the gate of transistor T_2 the width-to-length ratio of transistor Q_1 is set equal to $\frac{1}{4}$(W/L), with I_{bias} set equal to I_{in}. This process can be repeated up the chain until the gate voltage on transistor T_n is determined. A more complete description of the design procedure can be found in [2]. The conclusion of that work was that the output resistance of the current mirror was the same as in the standard cascode design, namely

$$R_{out} = g_m^{(n-1)} r_o^n, \tag{5}$$

but with a linear output voltage range that is larger than that of the cascode current mirror circuit of Figure 1 by a voltage of $(n-1)V_t$, namely

$$V_{out} > n\Delta V. \tag{6}$$

Note that previously this result was known only for $n = 2$ ([4], [5]).

When originally proposed the dimensions of the transistor in the generalized high-swing cascoded current mirror were allowed to be of arbitrary width and length. However, design experience has shown that one should make the dimensions of all the transistors the same. The reason for this is that the bias scheme described above was developed using simple first-order device equations, but in reality one cannot expect these expressions to accurately predict the node voltages in the circuit, and as a result one could find some of the transistors operating outside of their saturation region. Even if more complex models were used, it is unlikely that they will accurately predict the correct behavior of transistors with different dimensions. Thus, by restricting ourselves to one size of device we can make a more robust current mirror. However, the bias circuits use transistors that require aspect ratios that have different lengths than those used in the mirror circuit. Thus a new bias scheme is required.

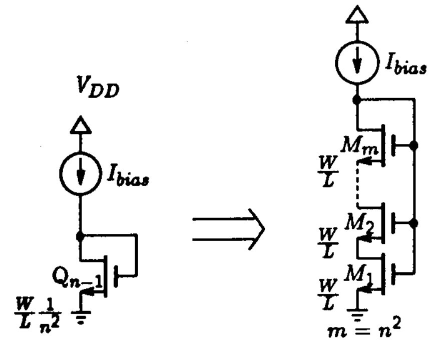

Figure 4 Improved biasing scheme.

The new bias scheme is shown in Figure 4. In place of the single bias transistor Q_{n-1} we stack m transistors on top of one another with their gates all connected together. By placing the transistors in this fashion we have created a voltage on their gates that would be the same as if we reduced that aspect ratio of a single transistor by the factor m. If we make $m = n^2$ then the bias voltage generated by the cascoded transistors will be equal to or slightly greater than the require bias voltage. It is worth noting that this scheme would bias the transistors right at the edge of saturation thus introducing some risk that some of the transistors in the current mirror will leave the saturation region, either due to the body effect or to process variation. Therefore we have found that it is best to bias the transistors further into saturation by making the number of bias transistors m larger than n^2. We suggest that $m = n^2 + n - 1$ will add a sufficient safety margin.

3. Low Voltage OTA Designs

The design of the new low-voltage OTAs requires only a straightforward substitution of the high-swing cascoded current mirrors for each of the standard cascoded current mirror in the OTAs shown in Figure 1. The resulting current mirroring and current steering OTAs are shown in Figures 5 and 6, respectively. We have assigned dimensions to the various transistors in each of the designs. The transistors in the differential pairs, T_1 and T_2, have a width of W_{dif} and a length of L_{dif}. The transistors in the NMOS current mirrors have a width of W_N and a length of L_N. The bias circuits for those NMOS current mirrors also use transistors of the same dimensions,

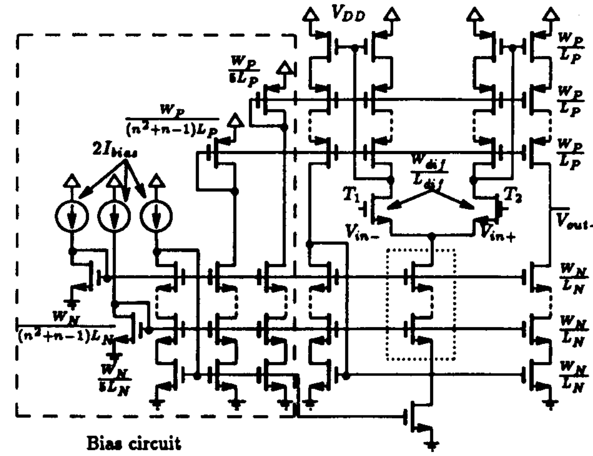

Figure 5 Generalized high-swing current mirror OTA design.

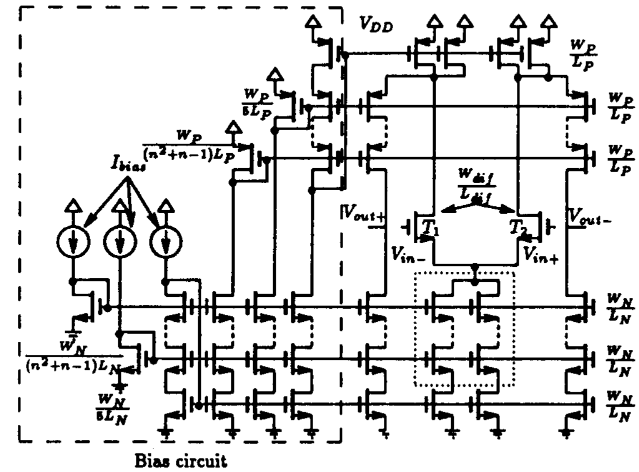

Figure 6 Generalized high-swing current steering OTA design.

but use the method described in the last section to change the effective aspect ratio. Similarly, the transistors PMOS current mirrors are of uniform dimensions with the width being W_P and the length being L_P. The number of cascoded transistors is arbitrary as is indicated by short dashed lines in the figures. However, cascoding the transistors associated with the current source used to bias the differential pair is optional, as is indicated by dotted lines. Whether or not cascoding is used here depends on the common-mode requirements. The bias circuit is highlighted with long-dashed lines, and while it is larger than that in the standard OTA, only one such circuit is needed if there are multiple OTAs. Both of the designs of Figure 5 and 6 have the same linear output voltage range, namely

$$V_{linear} = V_{DD} - (\sqrt{n^2+n-1})\Delta V_N - (\sqrt{n^2+n-1})\Delta V_P. \tag{10}$$

Comparing this with the linear range of the standard design, given in Eqn. 4, we find that the linear range has increased by approximately $(n-1)V_{tN} + (n-1)V_{tP}$ which is a vast improvement. Also because we have eliminated the dependence of the threshold voltages of the transistors, we can make the output swing arbitrarily close to the full voltage range of V_{DD}. Note that this result was already known for the case of $n = 2$.

While Eqn. (10) expresses the full linear output voltage range available, the output voltage swing will only be symmetrical if ΔV_N equals ΔV_P. Assuming that

$$K = K_P = \frac{K_N}{3}, \tag{11}$$

we can guarantee that $\Delta V_N = \Delta V_P$ if we make the aspect ratio of the PMOS transistors three times larger than that of the NMOS transistors. Also for simplicity we design the OTAs such that the length of the NMOS and PMOS transistor are the same, thus

$$L = L_P = L_N \text{ and } W = W_P = 3W_N. \tag{12}$$

4. Increased Gain-Bandwidth Product Through Cascoding

As we showed in the last section with the high-swing OTA one can increase the number of cascoded transistors without significantly reducing its output swing. One might ask whether it is necessary or even useful to use more than one level of cascoding in the OTA. It might seem that more cascoding would simply reduce the maximum bandwidth of the OTA and not provide much benefit other than increase the low frequency gain. However, we can trade-off the extra gain for greater bandwidth by shorting the length of the cascoded transistors in the OTA, and as a result have a greater bandwidth than that which is possible with a single cascoded stage. In this section we will examine this tradeoff and show how additional cascoding can be used to increase the gain-bandwidth product of the current mirror OTA.

There are two methods that increase the low-frequency gain of current mirror OTA, either increase the length of the transistors or cascode more transistors. The conventional problem with cascoding was that it resulted in a large loss in linear output swing for the OTA, and thus was of only limited use. However, since this problem has been eliminated it is worth while to re-investigate which of the two choices are better. The decision as to which is better will depend both on the application that the OTA is used in and on what process it is fabricated. For instance, in the past when line widths on CMOS processes were 3 μm or greater the gains of single cascoded OTAs would be large enough for most application so that any additional cascoding was unnecessary. On the other hand, the same is not true for a submicron process. Recognizing that longer length devices would essentially limit us forever to present-day OTA bandwidths, it is apparent that the only way to increase the bandwidth of an OTA is to decrease the length of the appropriate devices. Of course, it might turn out that in order to get sufficient gain, the additional cascoding that is required might reduce the overall bandwidth of the OTA below that which is achievable by increasing the lengths of the appropriate transistors. Fortunately, we have found evidence that this is not the case as will be illustrated with the following example.

In this example we have compared the low-frequency gain versus maximum bandwidth for the current mirror OTA of Figure 5 using single and double cascoded current mirrors. The results of these simulations are shown in Figure 7. To ensure that the comparison were fair we have imposed the restrictions that both OTAs use the same bias current of 60 μA, and have the same linear output voltage range of 2 volts on a 3.3-V power supply. Also the dimensions of the differential pair W_{dif} and L_{dif} were chosen to be 180 μm and 3 μm, respectively. Starting with minimum length transistors we simulated the open loop response of both designs using a SPICE AC analysis, using models obtained from Northern Telecom's 1.2 μm CMOS process, and extracted the low-frequency gain and maximum bandwidth. The maximum bandwidth, or f_t, was selected as the frequency at which the phase contribution of the parasitic poles was 45 degrees, thus ensuring that the OTA is stable in closed loop operation. Next we increased the length of the transistor in the OTA, along with a corresponding increase in the widths so that the linear output voltage range of 2 volts was maintained, and simulated again. This, of course, increases the low-frequency gain of the OTAs at the expense of bandwidth, as is clearly indicated in Figure 7 by the downward slope of the two lines. What is evident in the figure is that for the same low-frequency gain the bandwidth of the double cascoded OTA is much larger. In fact, when we compare the single and double cascoded OTA that have a gain of 100 dB we see that the double cascoded design has a maximum bandwidth, or gain-bandwidth, that is more than an order of magnitude greater than the single cascoded OTA. This result clearly indicates that using cascoding to increase the low-frequency gain provide larger bandwidth than if we increase the length of the transistor in the design.

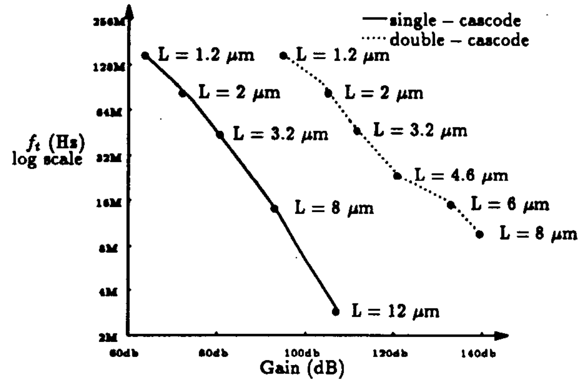

Figure 7 Comparison of gain-bandwidth for the single and double cascoded current mirror OTA design. For both designs the supply voltage was 3.3 volts and the linear output range of the OTA was 2 volts.

5. Conclusions

This paper generalizes the scheme used to create a high-swing single cascoded OTAs so that it may be applied to the case of a multiple cascoded OTAs. Using this new technique it is possible to design multiple cascoded OTAs that have linear output voltage ranges that can be arbitrary close to the supply voltages and thus are very suitable for low-voltage applications. It was shown how multiple cascoding can be used to design OTA that have a large gain-bandwidth product than single cascoded OTA, but do not sacrifice any of the linear output voltage range.

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