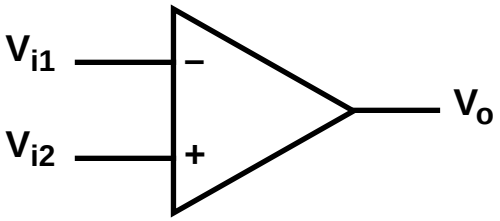
Chapter 3 MOS Operational Amplifiers

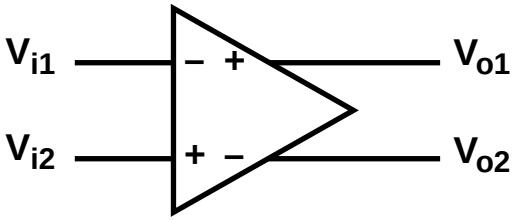
APPLICATIONS

- **Filters**
- **Precision amplification**
- **Analog arithmetic operations**
- **Impedance transformation**

NOTATION:

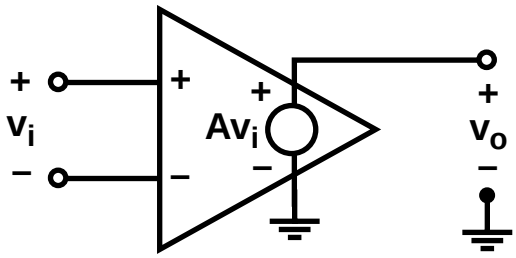


SINGLE ENDED



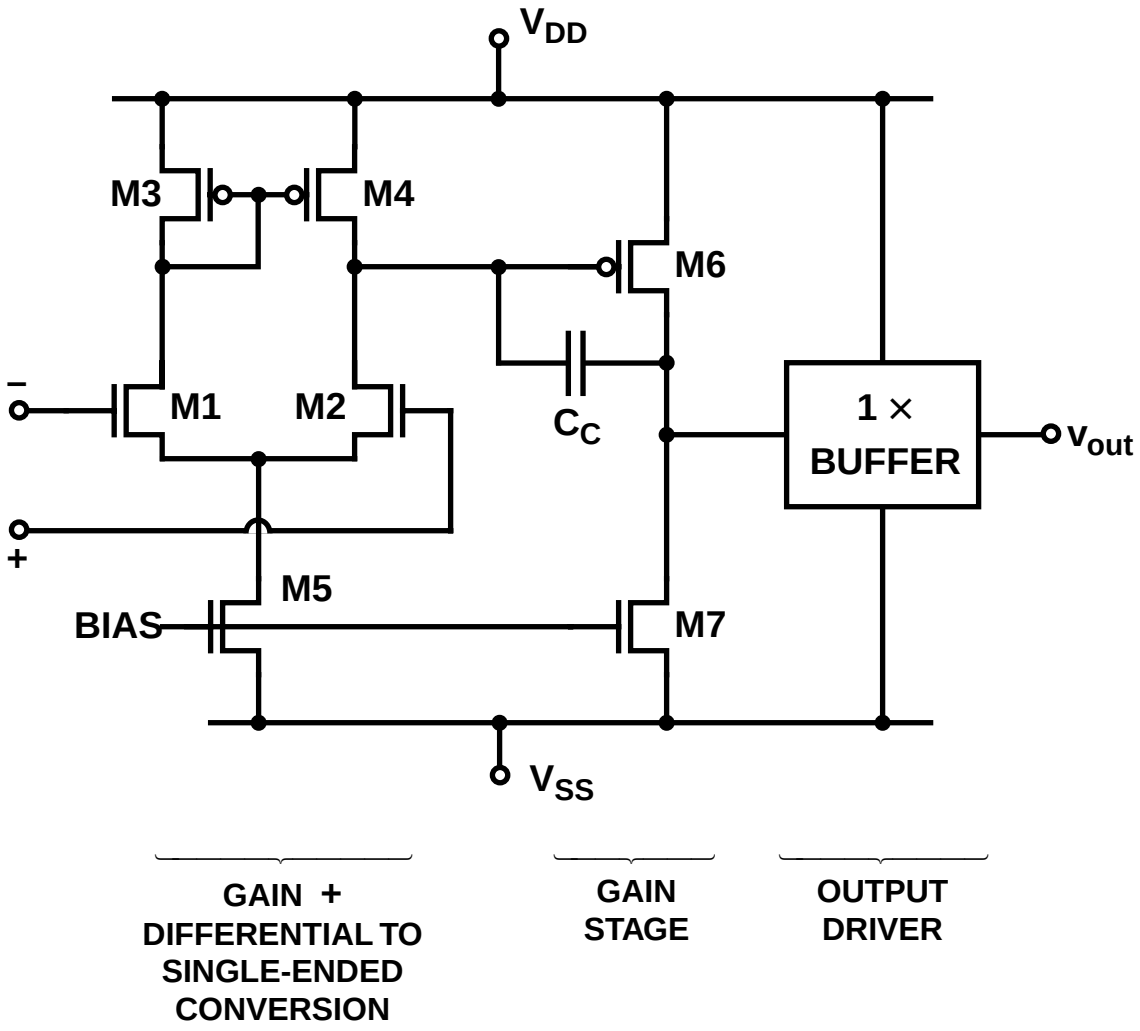
FULLY DIFFERENTIAL

IDEAL OP AMP:

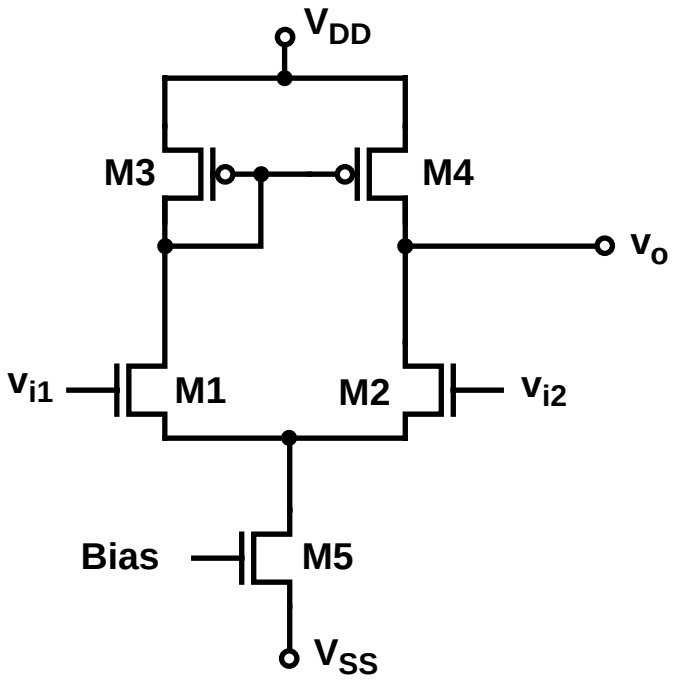


$v_o = Av_i$ **(Ideally** $A \rightarrow \infty$**)**

Basic 2-Stage Op Amp



Op Amp Input Stage



Source-coupled pair + current-mirror load

- **Source coupled pair provides $\Delta V \rightarrow \Delta I$**
- **Current mirror provides $\Delta I \rightarrow \Delta V$, as well as differential to single-ended conversion with good common-mode rejection**

Differential & Common-Mode Gain

$$A_{dm} \equiv \left.\frac{v_o}{v_{id}}\right|_{v_{ic}=0} = \left.\frac{v_o}{v_{i1}-v_{i2}}\right|_{v_{i1}=-v_{i2}}$$

$$A_{cm} \equiv \left.\frac{v_o}{v_{ic}}\right|_{v_{id}=0} = \left.\frac{2v_o}{v_{i1}+v_{i2}}\right|_{v_{i1}=v_{i2}}$$

$$v_o = A_{dm}v_{id} + A_{cm}v_{ic}$$

For an op amp with a single-ended output

$$\text{CMRR} = A_{dm}/A_{cm} \quad \text{(common-mode rejection ratio)}$$

Small-Signal Input-Stage Model

The frequency response of the current mirror load is typically dominated by "load pole" at its output. It also contains a nondominant pole-zero pair in the neighborhood of ω_t, the cutoff frequency of the mirror transistors.

A small-signal model of the op amp input stage can be formed by combining models for the source-coupled pair and the current-mirror load. The following simplifying assumptions can be used to reduce this model to very simple quasi-differential half circuit.

Simplifying Assumptions:

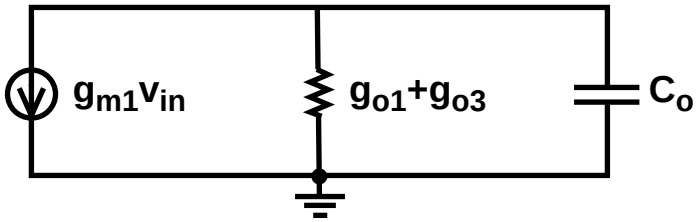
- **Devices in the circuit are matched so that**

  $g_{m1} = g_{m2}$, $g_{o1} = g_{o2}$

  $g_{m3} = g_{m4}$, $g_{o3} = g_{o4}$

- $g_{m1}, g_{m3} >> g_{o1}, g_{o3}$
- **The currents through g_{o1} and g_{o2} into the tail node are negligible in comparison with the g_{m1} and g_{m2} currents into that node**
- **The frequency response of the stage is dominated by the time constant at the output node**
- **The inputs of the stage are driven from low source impedances, so that the influence of input capacitances on the differential frequency response can be neglected**
- **The nondominant pole-zero pair associated with the current mirror are close together and can be neglected**

Under the preceding assumptions, the input stage can be modeled as:



where $v_{in} = v_{i2} - v_{i1}$ is the differential input, defined as positive for the non-inverting input of the two-stage amplifier, and C_o is the equivalent load capacitance seen by the input stage

The differential-mode gain of the input stage is thus

$$A_{dm}(s) \cong \frac{A_{dm}(0)}{1 - \frac{s}{p_1}}$$

where

$$A_{dm}(0) = \frac{g_{m1}}{g_{o1} + g_{o3}}$$

$$p_1 = -\frac{g_{o1} + g_{o3}}{C_L}$$

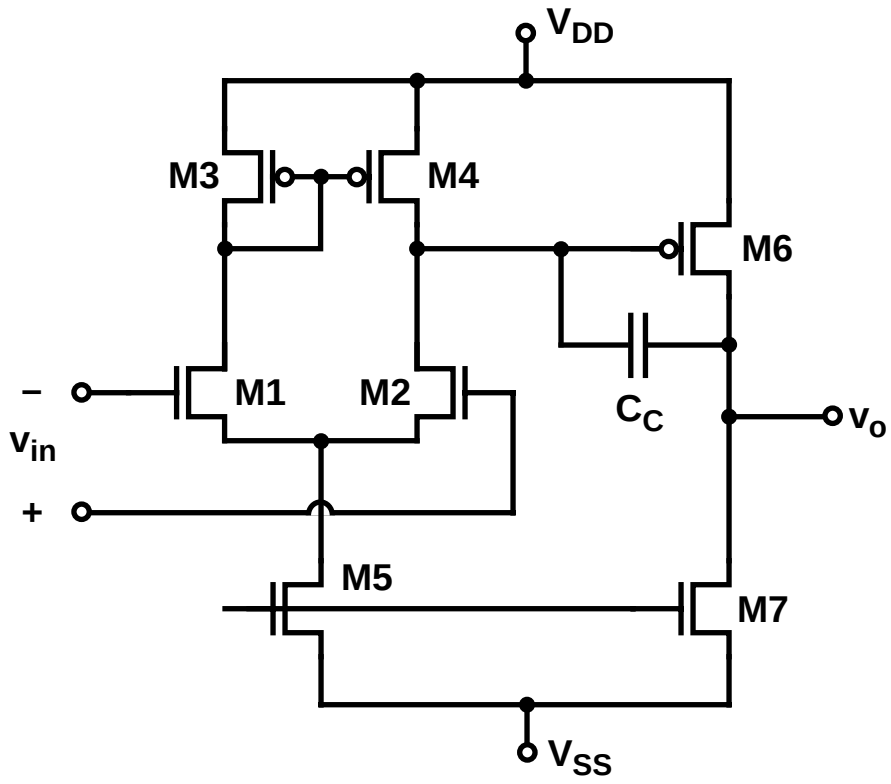
The common-mode response is governed by the same dominant pole as the differential response (the "load" pole)

$$A_{cm}(s) \cong \frac{A_{cm}(0)}{1 - \frac{s}{p_1}}$$

and has the low-frequency gain

$$A_{cm}(0) \cong -\frac{g_{o5}}{2g_{m3}}$$

Two-Stage Op Amp Response



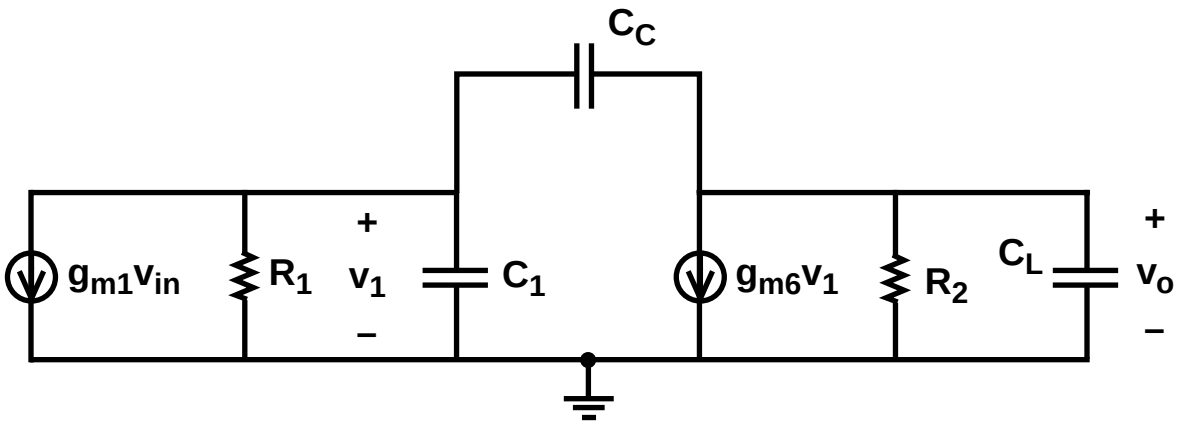
COMMON-MODE RESPONSE

Since the output of the first stage is single-ended, the common-mode response of the 2-stage op amp is governed by this stage; moreover

$$CMRR_{\text{Op Amp}} = CMRR_{\text{ Input Stage}}$$

DIFFERENTIAL-MODE RESPONSE

A small-signal model for the differential response of the two stage op amp can be formed by replacing the equivalent load capacitance in the differential mode model for the input stage with the small-signal model for the common-source second stage:



where

$$G_1 = 1/R_1 = g_{o2} + g_{o4} = g_{o1} + g_{o3}$$

$$G_2 = 1/R_2 = g_{o6} + g_{o7}$$

$$C_1 = C_{db2} + C_{db4} + C_{gs6} + C_{p1}$$

$$C_L = C_{db6} + C_{db7} + C_{p2} + C_{load}$$

$$C_c = C_{gd6} + C_{comp}$$

C_{comp} is the pole-splitting compensation capacitance, while C_{p1} and C_{p2} are parasitic capacitances at the pole-splitting and output nodes of the amplifier.

Solving for $A_V(s) = v_o(s)/v_{in}(s)$

$$A_V(s) \approx A_V(0)\frac{(1 - s/z_1)}{D(s)}$$

where

$$A_V(0) = g_{m1}g_{m6}R_1R_2$$

$$z_1 = \frac{g_{m6}}{C_C}$$

$$D(s) = 1 + \alpha_1 s + \alpha_2 s^2 = \left(1 - \frac{s}{p_1}\right)\left(1 - \frac{s}{p_2}\right)$$

$$\alpha_1 = R_1(C_1 + C_C) + R_2(C_L + C_C) + g_{m6}R_1R_2C_C$$

$$\alpha_2 = R_1R_2(C_1C_L + C_1C_C + C_LC_C)$$

If a "dominant pole" condition exists ($|p_1| << |p_2|$), which is the expected case in a fully-compensated op amp, then

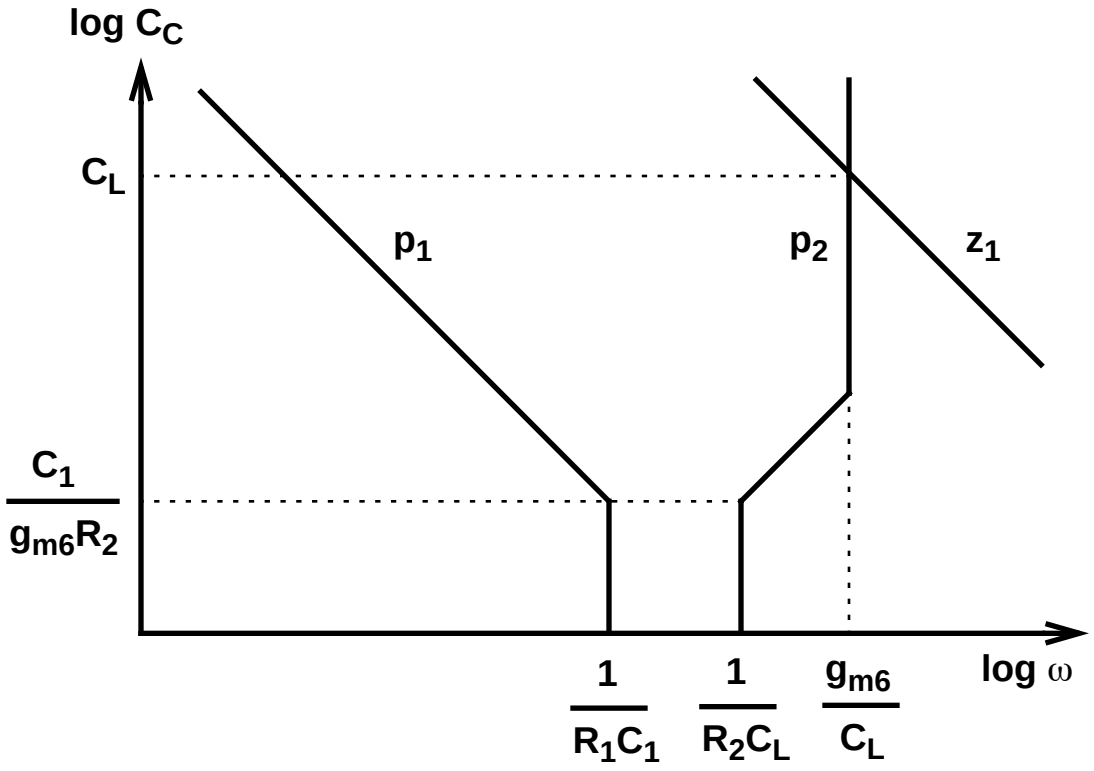
$$p_1 \cong -\frac{1}{\alpha_1} \quad \text{and} \quad p_2 \cong -\frac{\alpha_1}{\alpha_2} = \frac{1}{\alpha_2 p_1}$$

Further, if $g_{m6} >> G_1, G_2$ and $C_1 << C_C, C_L$, then

$$p_1 \cong -\frac{1}{g_{m6}R_1R_2C_C} = -\frac{1}{|A_V(0)|}\left(\frac{g_{m1}}{C_C}\right)$$

$$p_2 \cong -\frac{g_{m6}C_C}{C_1C_L + C_1C_C + C_LC_C} \cong -\frac{g_{m6}}{C_L}$$

Op Amp Frequency Compensation



POLE SPLITTING

The capacitance C_C in the simplified small-signal model of 2-stage op amp acts as a "pole-splitting" capacitor that separates the two poles, p_1 and p_2. p_1 is associated with the internal node between the first and second stage and is the dominant pole, while p_2 is associated with the output node, and thus the op amp's load.

To ensure the stability of the op amp when configured in a unity-gain configuration (voltage follower), the value of C_C must be large enough so that

$$\omega_u << |p_2|$$

where ω_u = op amp unity-gain frequency.

If the op amp is fully compensated, then it has a one-pole response out to ω_u:

$$\left|A_V(\omega_u)\right| \cong \left|A_V(0)\right|\left|\frac{p_1}{\omega_u}\right| = 1$$

and

$$\omega_u = \left|A_V(0)\right|\left|p_1\right| = \frac{g_{m1}}{C_C}$$

Thus,

$$\frac{\left|p_2\right|}{\omega_u} \cong \frac{g_{m6}}{g_{m1}}\left(\frac{C_C}{C_L}\right)$$

and to ensure that $\omega_u < |p_2|$

$$C_C > \frac{g_{m1}}{g_{m6}}C_L$$

Typically, ω_u is kept a factor of 2 or 3 smaller than $|p_2|$.

<u>Feedforward Zero</u>

Because the zero z_1 in the differential response of the 2-stage op amp is in the right half of the s-plane (RHP zero), it will degrade the amplifier's phase margin in the same way as the nondominant pole as the frequency approaches ω_u

Therefore, it is also necessary that

$$\omega_u << |z_1|$$

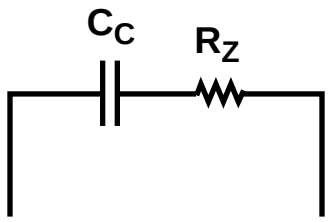
However,

$$\frac{z_1}{\omega_u} = \frac{g_{m6}}{g_{m1}}$$

Since in a MOS op amp it is usually the case that $g_{m1} \cong g_{m6}$ in order to achieve sufficient gain, it is necessary to move or cancel z_1.

NULLING RESISTOR

The most common approach to compensating for the feedforward zero is to use a "nulling resistor" to approximately cancel z_1.



Analysis of the small-signal behavior of the 2-stage op amp with a nulling resistor R_Z in series with the compensation capacitor C_C indicates that the voltage transfer function is modified by a change in location of the zero z_1 and the introduction of a third pole, p_3.

That is,

$A_V(0)$, p_1 and p_2 remain the same as w/o R_Z

$$z_1 = \frac{1}{C_C\left(\frac{1}{g_{m6}} - R_Z\right)}$$

$$p_3 \cong -\frac{1}{R_Z C_1}$$

When $R_Z = 1/g_{m6}$, the feedforward zero is removed (z_1 is moved to infinity).

If R_Z is increased above $1/g_{m6}$, z_1 is moved into the left half plane and brought toward the origin. Thus, it can be used to cancel p_3, or even p_2 (see Black, et al., JSSC, 12/80, pp. 929-938).

If

$$R_Z = \frac{1}{g_{m6}}\left(\frac{C_C}{C_C - C_1}\right)$$

then $|z_1| = |p_3|$ and a simple 2-pole response is obtained for the amplifier without feedforward zero.

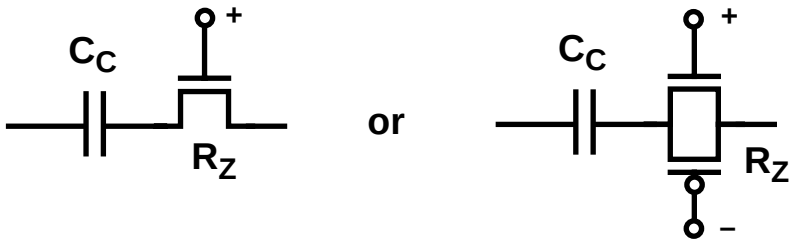
Even more aggressively, z_1 can be used to cancel the lowest nondominant pole, p_2

$$|z_1| = |p_2| \quad \Rightarrow \quad R_Z = \frac{1}{g_{m6}}\left(1 + \frac{C_L}{C_C}\right)$$

The amplifier then has a 2-pole response with p_3, rather than p_2, being the lowest nondominant pole. However, because of additional nondominant poles in an actual amplifier, optimal settling is achieved when $|z_1|$ is slightly less than $|p_3|$. When z_1 is used to cancel p_2,

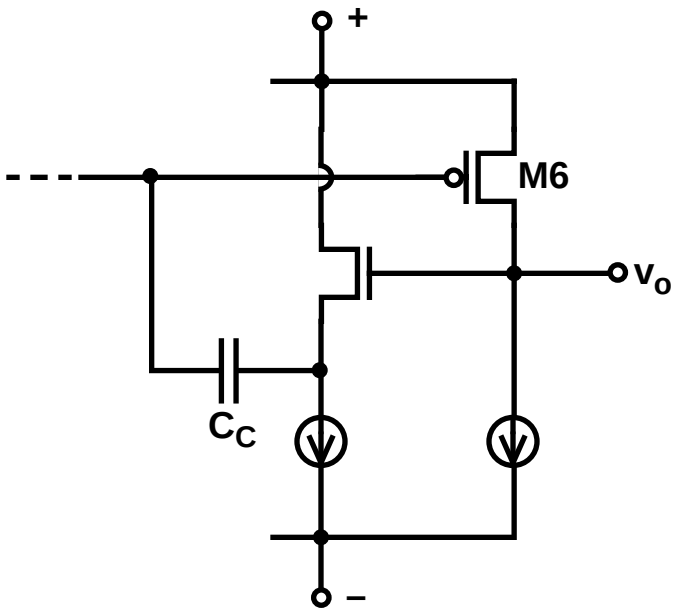
$$C_L(\text{maximum}) \approx \left(\frac{C_C}{C_1}\right) C_C$$

The resistor R_Z can be implemented with a transistor, or pair of complementary transistors, operated in the linear region.

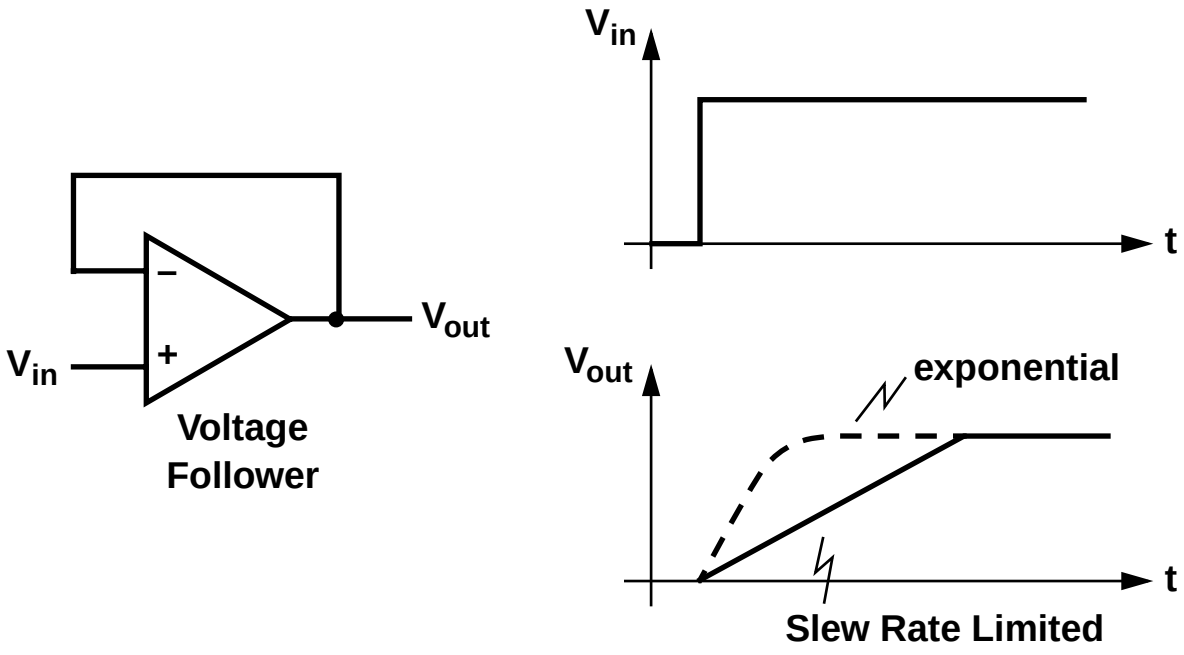


If z_1 is used to cancel p_2 it is important that R_Z be implemented in a way that ensures $|z_1|$ will track $|p_2|$ over large variations in processing, temperature and supply voltage. If the p_2, z_1 doublet separates, a slow settling component is introduced into the op amp's step response. The paper by Black, et al. describes a circuit for biasing R_Z that will provide the proper tracking for $|z_1|$.

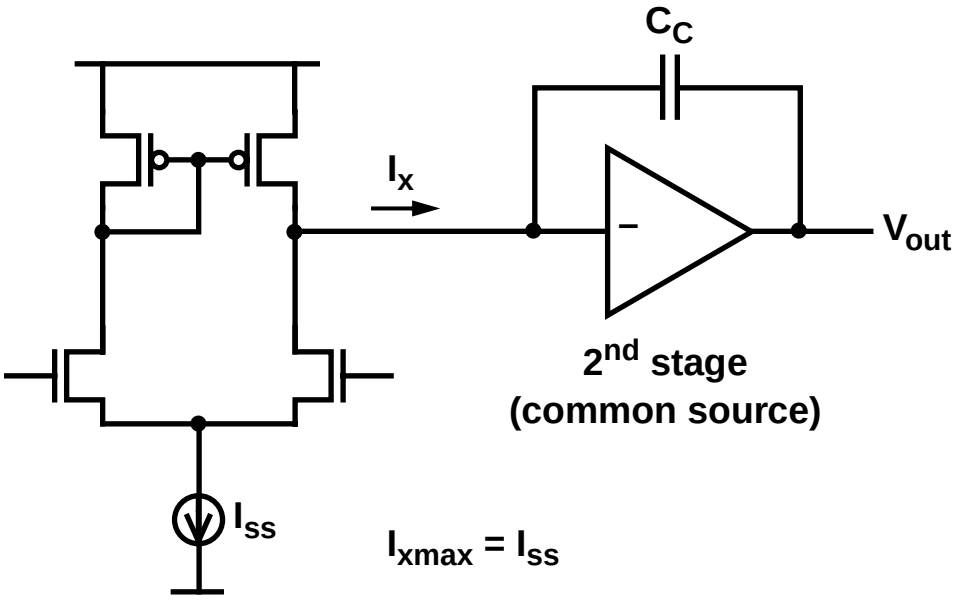
The feedforward zero can also be eliminated with a source follower



Slew Rate



In the basic 2-stage op amp the slew rate is generally limited by the current available from the input stage to charge and discharge C_C.



In this case the maximum slew rate, SR, is

$$SR = \frac{dV_{out}}{dt} = \frac{I_{xmax}}{C_C} = \frac{I_{ss}}{C_C}$$

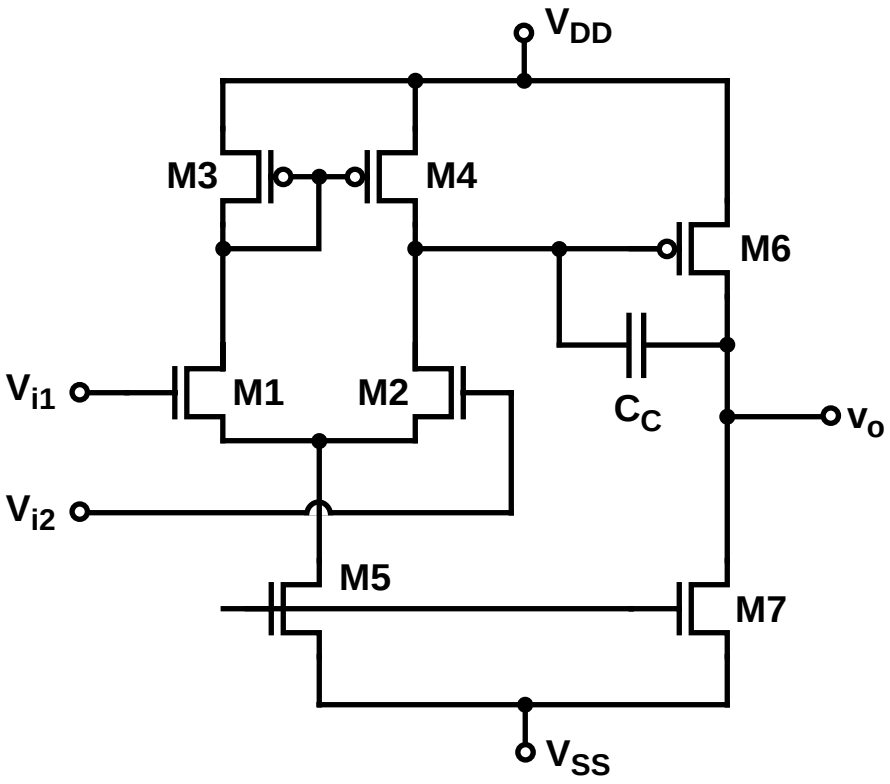
Upon substituting $C_C = g_{m1}/\omega_u$

$$SR = \frac{I_{ss}}{g_{m1}} \cdot \omega_u = (V_{gs1} - V_T) \cdot \omega_u$$

$$\therefore \quad SR = (\Delta V_{iM}/\sqrt{2}) \cdot \omega_u$$

Thus, the slew rate is related to ΔV_{iM}, the magnitude of the differential input voltage needed to fully switch the tail current of the input pair to one side of the pair.

Systematic Offset



Because of the relatively limited amount of gain that can be obtained in the first stage of the 2-stage MOS op amp (in comparison with bipolar op amps), the current mirror and the second stage can significantly influence the input-referred offset of the circuit.

Therefore, M3, M4 and M6 must be carefully sized so that when $V_{i1} = V_{i2}$, $V_o = 0$

If the input stage transistors are balanced, then $V_{i1} = V_{i2}$ when $V_{ds4} = V_{ds3}$. But, since

$$V_{ds4} = V_{gs6}$$

V_{ds4} is governed by the size and drain current of M6

To ensure

$$V_{gs6} = V_{ds3}$$

when $V_{out} = 0$, the first-order constraint is

$$\frac{W_3/L_3}{W_6/L_6} = \frac{W_4/L_4}{W_6/L_6} = \frac{1}{2}\left(\frac{W_5/L_5}{W_7/L_7}\right)$$

Furthermore, to minimize the influence of process variations it is best to choose

$$L_3 = L_4 = L_6$$

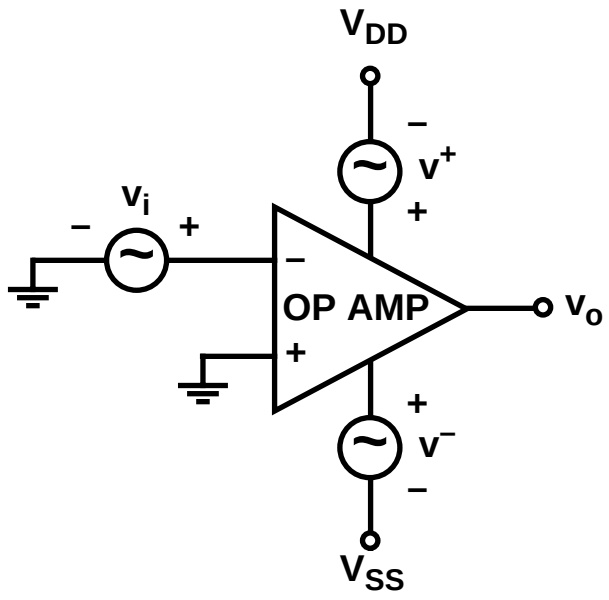
However, this constraint may conflict with gain, frequency response or noise constraints.

Power Supply Rejection

Noise induced on the supply rails can appear at the output of an op amp. In mixed-signal circuits, or in high-speed digital systems, supply noise can be especially severe.

POWER SUPPLY REJECTION RATIO

It is important to minimize the "gain" from the supply rails to the output; that is, to REJECT supply variations.



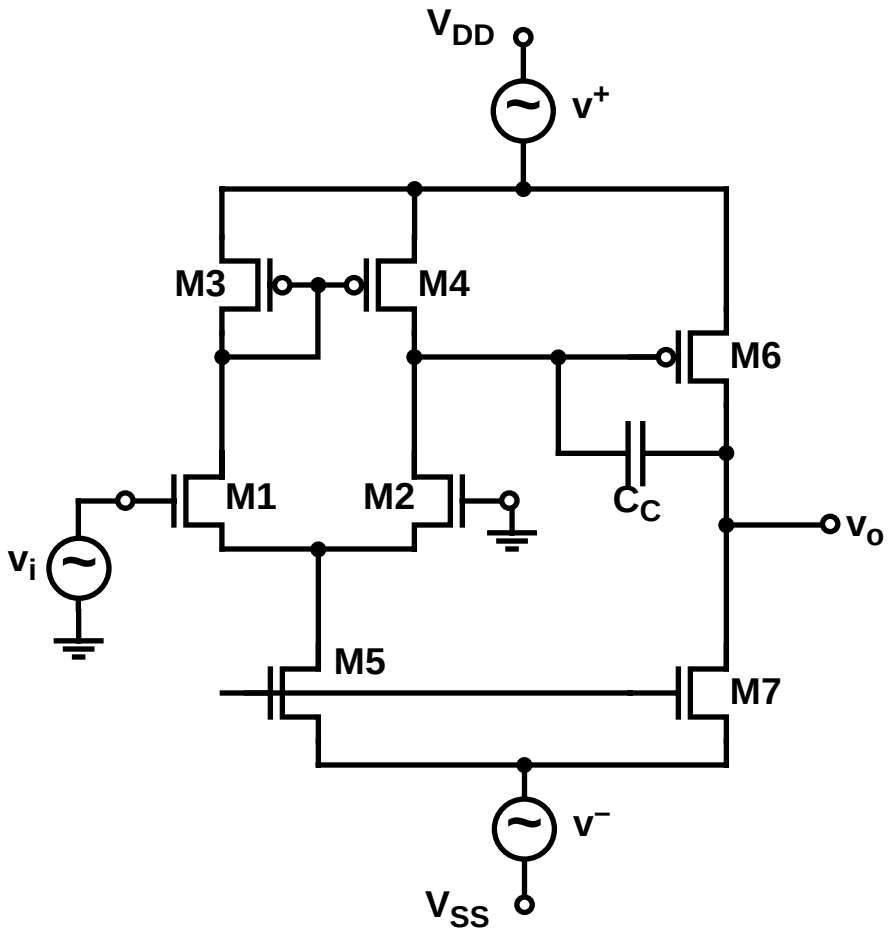
$$v_o = A_{dm}v_i + A^+v^+ + A^-v^- + A_{cm}\left(\frac{v_i}{2}\right)$$

Define

$$PSRR^+ = A_{dm}(\omega)/A^+(\omega)$$

$$PSRR^- = A_{dm}(\omega)/A^-(\omega)$$

In a 2-stage CMOS op amp



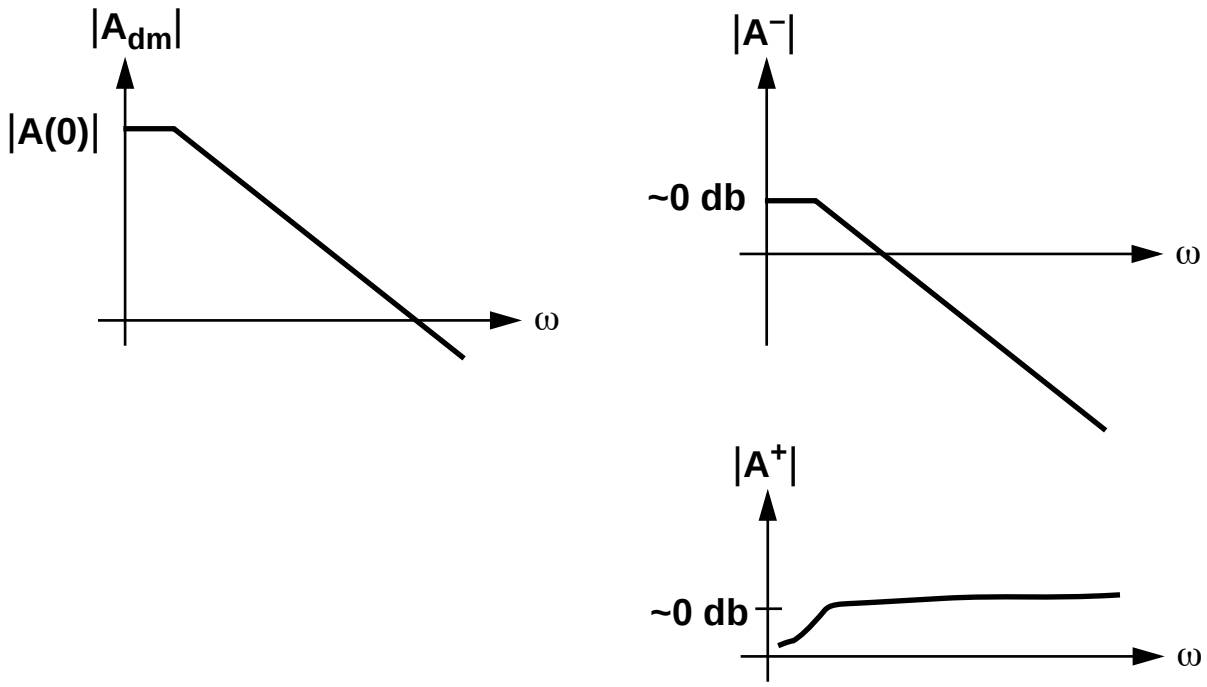
A^- is largely determined by g_{o5} & g_{o7}. It is typically ≤ unity at low frequencies and, more importantly, it rolls off with frequency in the same fashion as the open loop gain.

$\therefore$ $PSRR^-$ remains approximately constant with frequency.

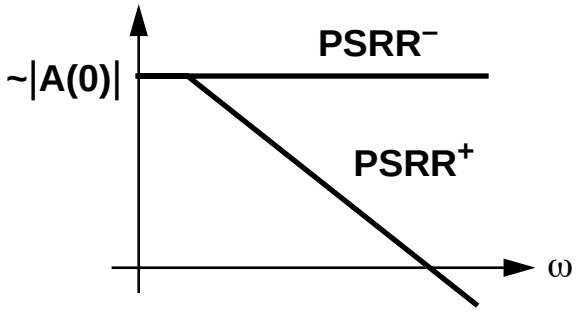
At frequencies above the dominant pole (which is determined by C_C), C_C "shorts" the gate and drain of M6. Since I_{d6} is constant, V_{gs6} remains constant. Thus, v_{g6} and v_o track v^+.

$\therefore$ $|A^+| \approx 1$ except at very low frequencies and $PSRR^+$ falls with frequency along with the open loop gain A_{dm}.

Typically,

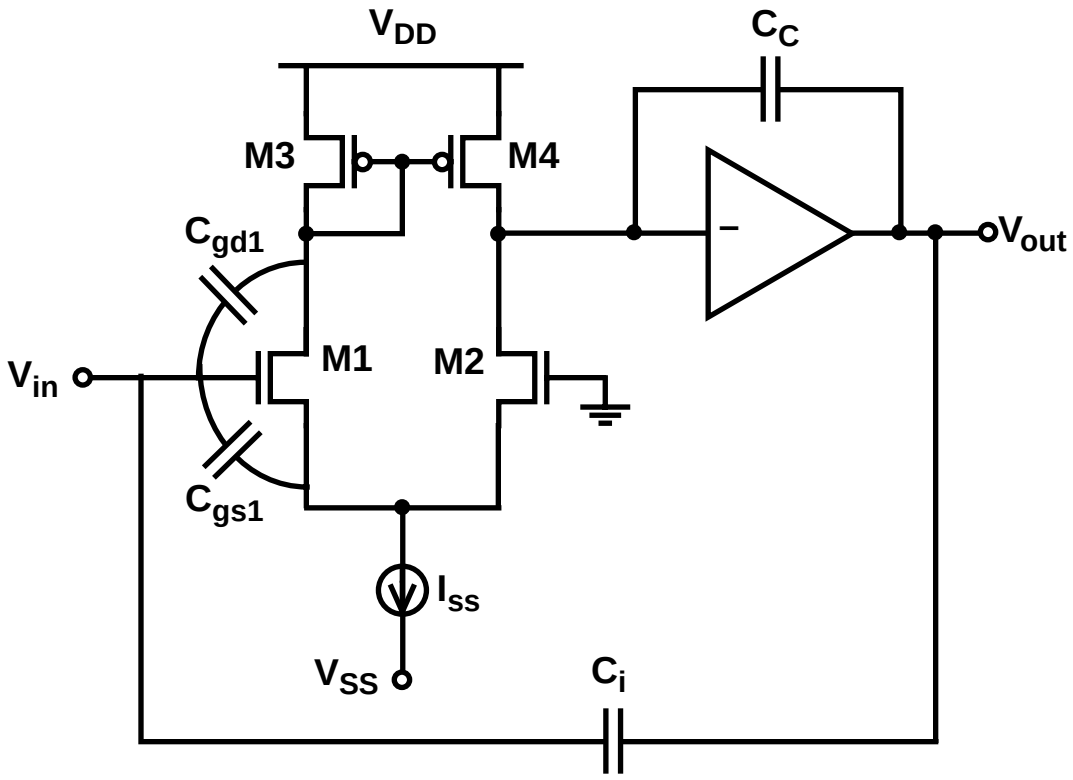


Thus,



"SUPPLY" CAPACITANCE

Another potentially significant source of coupling between the supply rails and the output is commonly referred to as "supply" capacitance. This term refers to the coupling from one, or both, of the supply rails into the input nodes of an op amp. It is primarily in circuits such as single-ended sampled-data integrators



The most important contributors to this type of coupling are displacement currents in the capacitances C_{gs1} and C_{gd1}. These currents flow into the summing node and the resulting charge is accumulated on the integration capacitor, C_i.

It is straightforward to determine that

$$\frac{\partial V_{out}}{\partial V_{SS}} \cong \frac{C_{gs1}}{C_i}\left[\frac{\partial I_{ss}}{\partial V_{SS}} \cdot \frac{1}{g_{m1}} + \frac{\partial V_{T1}}{\partial V_{SS}}\right]$$

$$\frac{\partial V_{out}}{\partial V_{DD}} \cong \frac{C_{gd1}}{C_i}\left[1 - \frac{\partial I_{ss}}{\partial V_{DD}} \cdot \frac{1}{2g_{m3}}\right]$$

From these equations it is apparent that some of the important factors influencing the supply capacitance coupling are:

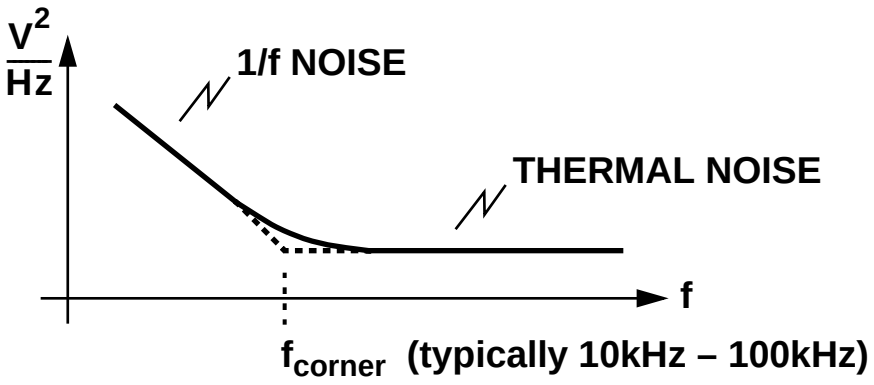
- **Variation in the drain voltage of M1 due to changes in V_{DD}; as a consequence current flows through C_{gd1} into the summing node. Cascode devices can be used to minimize this effect.**
- **Variation in body bias of M1 as a result of supply variations, resulting in a change in V_{T1}. This in turn results in change in V_{gs1}, inducing a displacement current in C_{gs1}. If M1 and M2 are implemented in a well (they would have to be PMOS transistors in an n-well technology), then the well can be tied to the common sources of M1 and M2 to eliminate this effect.**
- **Variation in I_{ss} with supply voltage. It is thus important that I_{ss} be generated in a fashion that is supply independent.**

Interconnect crossovers may also couple supply variations into the summing node.

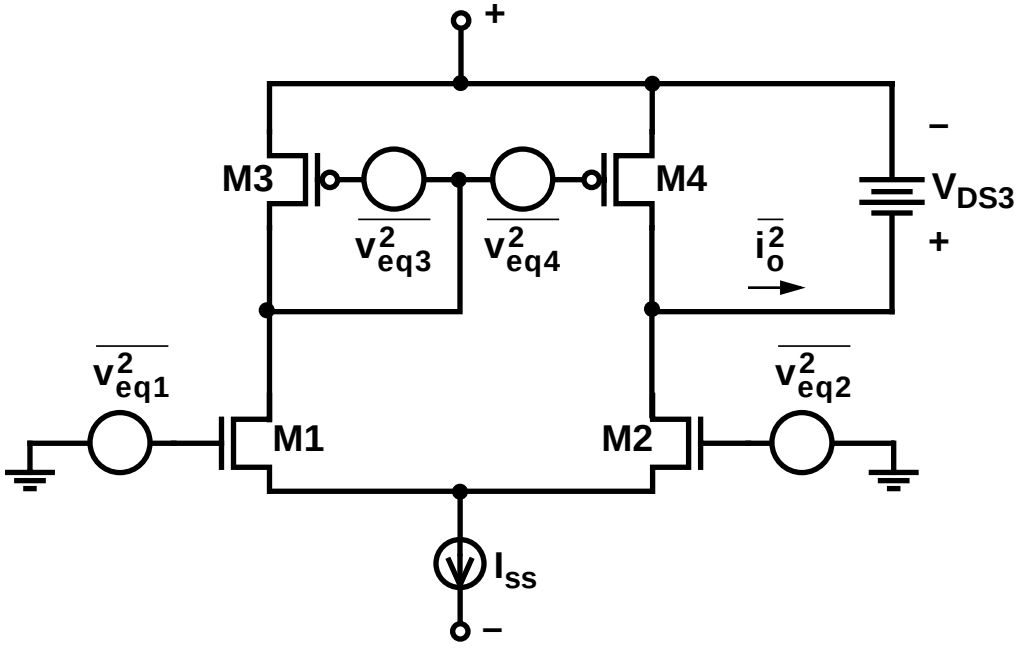
Fully differential circuits are an obvious means of avoiding the most severe supply capacitance problems.

Noise in CMOS Op Amps

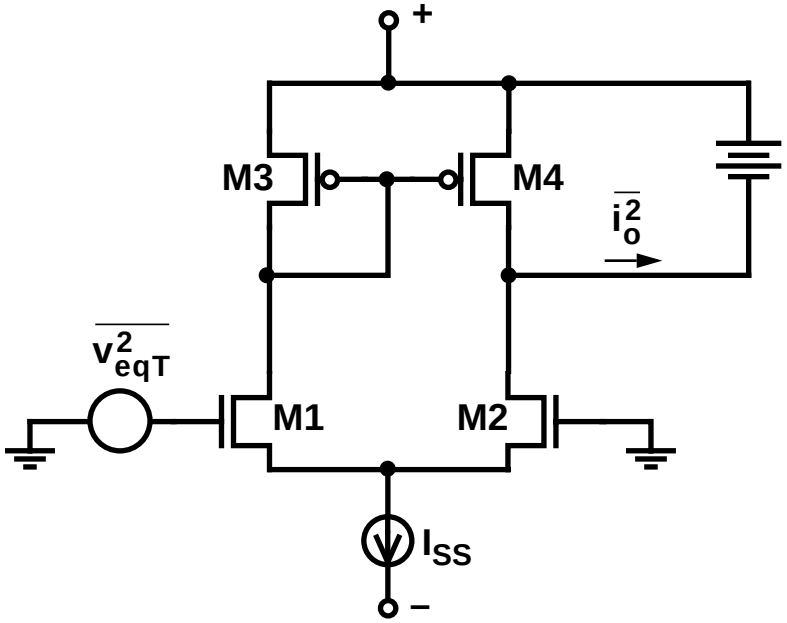
The two main components of noise in MOS transistors are 1/f (flicker) noise and thermal noise. The 1/f component is especially high in MOS devices, resulting in a relatively high "noise corner frequency."



The gain of the input stage in a MOS op amp is usually large enough so that the input-referred noise of the overall amplifier is dominated by the noise contributions from the input-stage transistors.



Referring all of the device equivalent noise voltage sources to an equivalent input noise voltage for the amplifier



Equating the output noise currents, $\overline{i_o^2}$, in the above circuits results in

$$\overline{v_{eqT}^2} = \overline{v_{eq1}^2} + \overline{v_{eq2}^2} + \left(\frac{g_{m3}}{g_{m1}}\right)^2 (\overline{v_{eq3}^2} + \overline{v_{eq4}^2})$$

where it is assumed that $g_{m2} = g_{m1}$ and $g_{m4} = g_{m3}$

1/f NOISE

For an MOS transistor the input-referred 1/f noise can be modeled as

$$\frac{\overline{v_{1/f}^2}}{\Delta f} = \frac{K_f}{fWLC_{ox}}$$

where K_f is the FLICKER NOISE COEFFICIENT

K_f is very process dependent; also, it is generally larger in NMOS transistors than in PMOS devices

A typical value for an NMOS transistor is $K_f = 3\times10^{-24}\ V^2F$

Using this model for each transistor in the input stage, the input-referred 1/f noise for the entire stage is

$$\frac{\overline{v_{1/fT}^2}}{\Delta f} = \frac{2K_{fN}}{fW_1L_1C_{ox}} + \left(\frac{g_{m3}}{g_{m1}}\right)^2\left(\frac{2K_{fP}}{fW_3L_3C_{ox}}\right)$$

assuming that $L_2 = L_1$, $W_2 = W_1$, $L_4 = L_3$ and $W_4 = W_3$

Since $I_{d3} = I_{d1}$

$$\left(\frac{g_{m3}}{g_{m1}}\right)^2 = \frac{\mu_P C_{ox}(W_3/L_3)}{\mu_N C_{ox}(W_1/L_1)}$$

Therefore

$$\frac{\overline{v_{1/fT}^2}}{\Delta f} = \frac{2K_{fN}}{fW_1L_1C_{ox}} + \frac{\mu_P(W_3/L_3)}{\mu_N(W_1/L_1)}\left(\frac{2K_{fP}}{fW_3L_3C_{ox}}\right)$$

$$= \frac{2K_{fN}}{fW_1L_1C_{ox}}\left[1 + \frac{K_{fP}\mu_P L_1^2}{K_{fN}\mu_N L_3^2}\right]$$

THERMAL NOISE

The input-referred thermal noise for an NMOS transistor is

$$\frac{\overline{v_{eq}^2}}{\Delta f} = 4kT\left(\frac{2}{3g_m}\right)$$

Thus, for the input stage of the MOS op amp

$$\frac{\overline{v_{eqT}^2}}{\Delta f} = 4kT\left(\frac{4}{3g_{m1}}\right) + \left(\frac{g_{m3}}{g_{m1}}\right)^2\left[4kT\left(\frac{4}{3g_{m3}}\right)\right]$$

$$= 4kT\left(\frac{4}{3g_{m1}}\right)\left[1 + \frac{g_{m3}}{g_{m1}}\right]$$

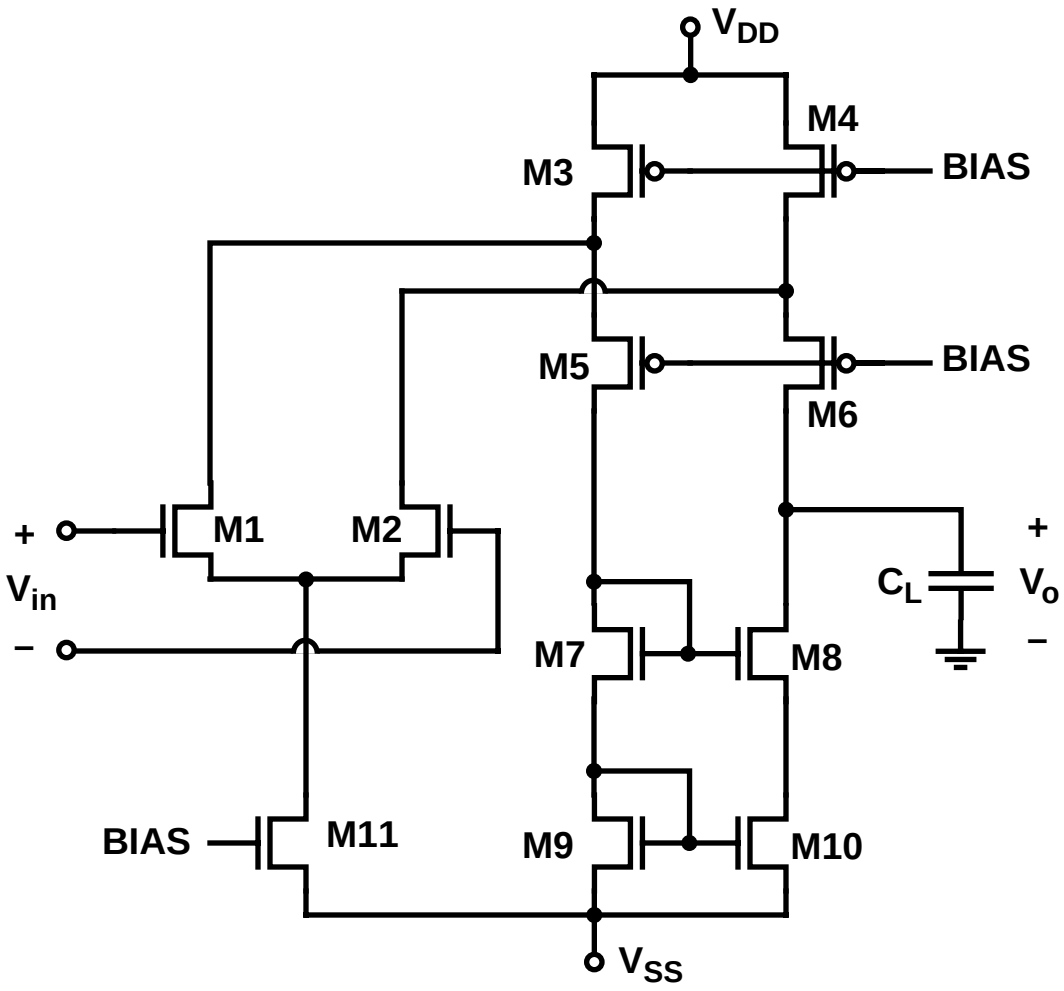
$$= 4kT\left(\frac{4}{3g_{m1}}\right)\left[1 + \sqrt{\frac{\mu_P(W_3/L_3)}{\mu_N(W_1/L_1)}}\right]$$

$$= 4kT\left(\frac{4}{3\sqrt{2\mu_N C_{ox}(W_1/L_1)I_{d1}}}\right)\left[1 + \sqrt{\frac{\mu_P(W_3/L_3)}{\mu_N(W_1/L_1)}}\right]$$

Single-Stage CMOS Op Amps

Through the use of cascoding, gain comparable to that of a 2-stage amplifier can be achieved in a single stage (Choi, et al., JSSC, 12/83, pp. 652-664). To achieve the maximum input and output signal ranges, cascoding can be employed in a "folded" architecture.

Folded Cascode



The output resistance of the cascoded single-stage amplifier is increased by $g_m r_o$ relative to the basic 2-stage op amp with a common-source second stage. The transconductance of the stage is simply the g_m of the input pair. Thus, the voltage gain is comparable to that of the two-stage op amp

$$|A_V(0)| \cong \frac{g_{m1}}{\left(\frac{g_{o2}+g_{o4}}{g_{m6}r_{o6}}\right)+\left(\frac{g_{o10}}{g_{m8}r_{o8}}\right)}$$

- **The dominant pole of the folded cascode amplifier is associated with the output node.**

$\therefore$ **C_L provides the frequency compensation. An increase in C_L lowers the amplifier's unity-gain bandwidth but does not compromise its phase margin.**

- **The nondominant poles in the folded cascode are those associated with the cascode devices M5 and M6, and the current mirror, M7 - M10. All of these poles are located near the transistor ω_t and are therefore normally much greater in magnitude than the lowest nondominant pole in the 2-stage op amp, $|p_2| = g_{m6}/C_L$.**

Advantages

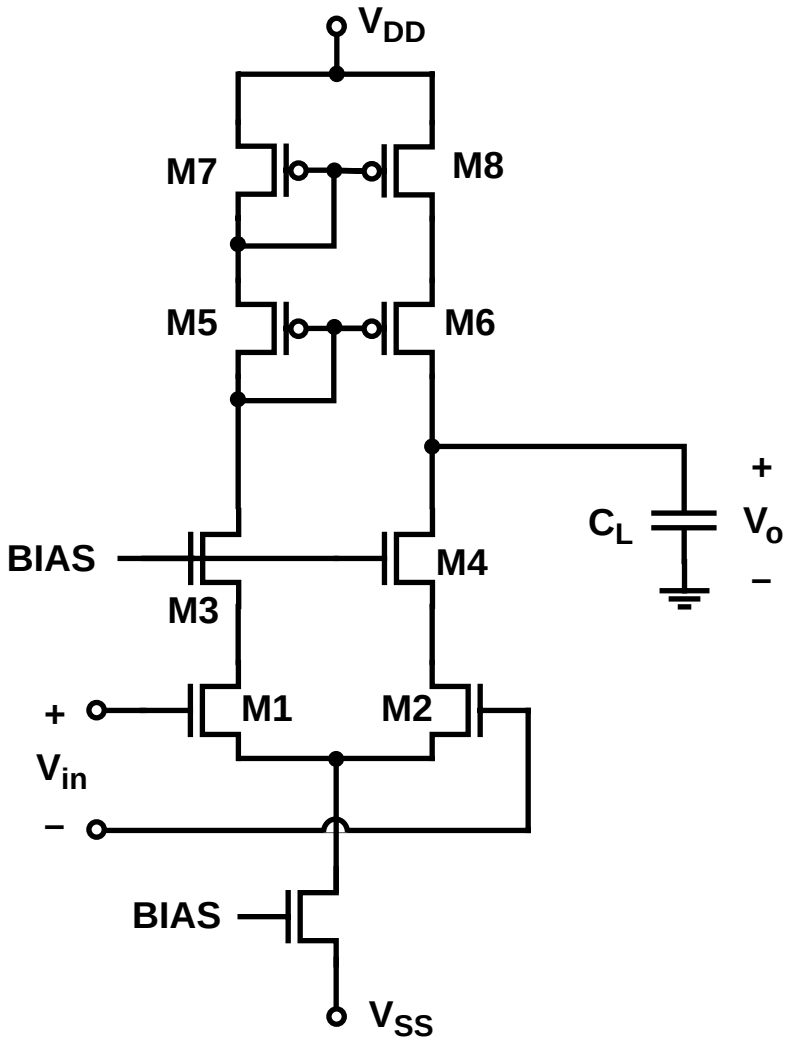
- **Simple compensation, since C_C is C_L**
- **High speed, since the nondominant poles are near $-\omega_t$**
- **Good PSRR since there is no pole splitting**
- **Good C_L drive capability**

Disadvantages

- **Reduced output swing**
- **Higher noise**

Telescopic Op Amp

Gain comparable to a 2-stage op amp can also be obtained in a cascoded single stage without folding



Advantages

- **Single bias current**
- **Input pair and cascode transistors are NMOS**

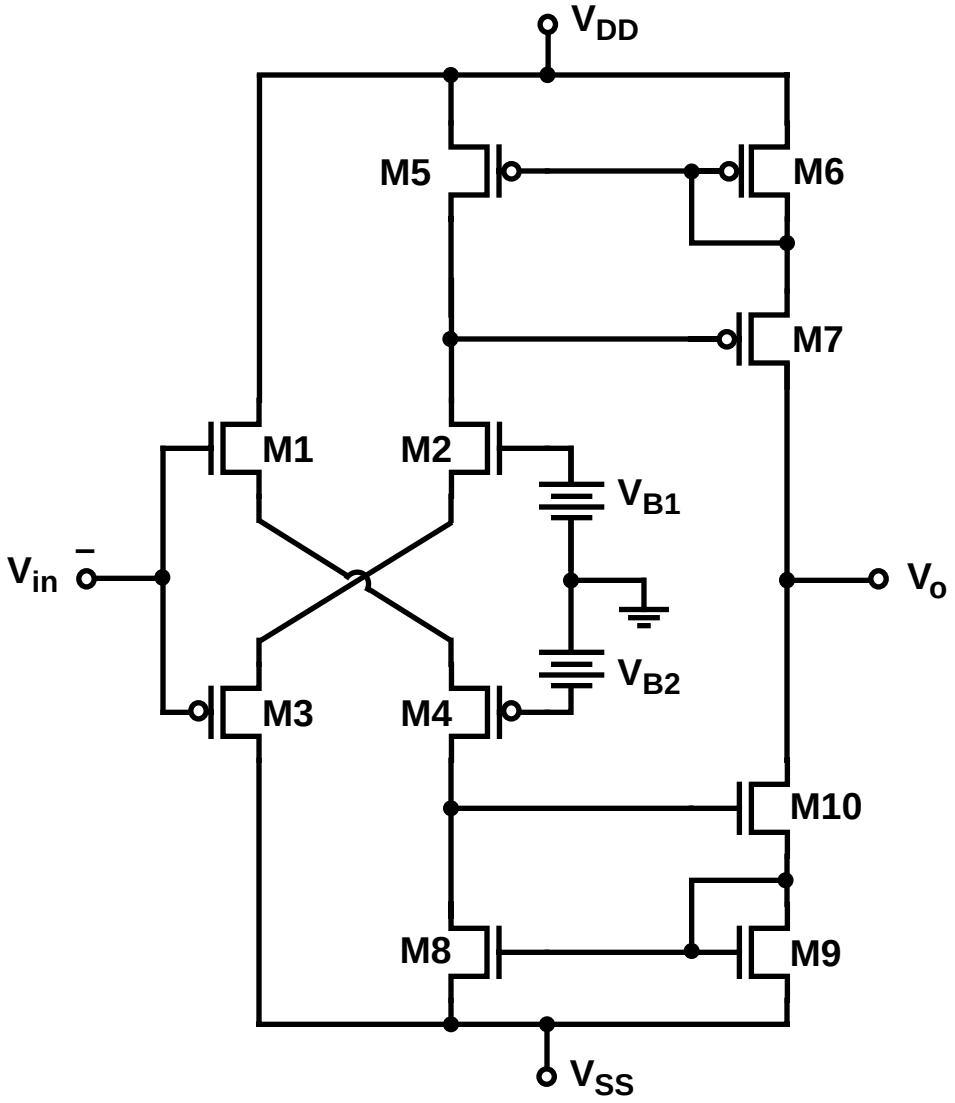
Disadvantage

- **Reduced output swing and common-mode input range**

Class AB Push-Pull Amplifier

Ref: Castello & Gray, JSSC, 12/85

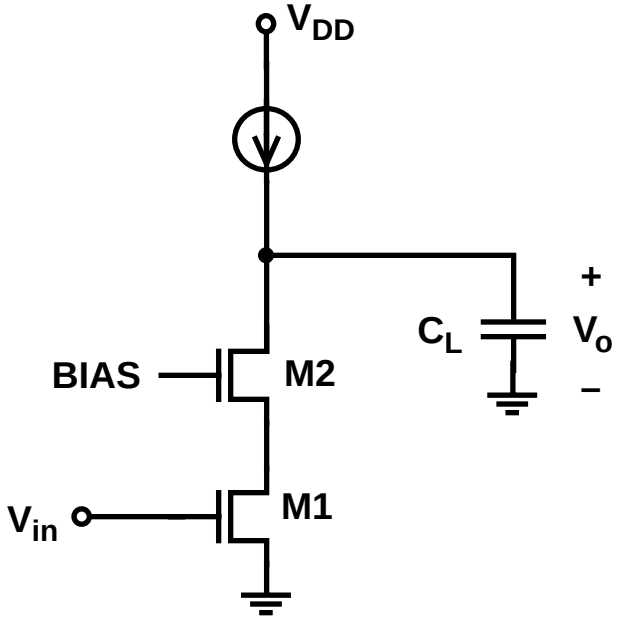
"Class AB" ≡ an amplifier that can sink and source currents much larger than its quiescent bias current



- **Inverting input only**
- **When V_{in} = 0, the quiescent currents are set by V_{B1} & V_{B2}**
- **As V_{in} goes positive, the current in M1 & M4 increases until $V_{in} = V_{DD}$, while M2 & M3 turn off. Therefore, the mirror circuit M5-M7 turns off, while a very strong drive is supplied to the mirror M8-M10.**

Gain-Enhanced Cascodes

SIMPLE CASCODE



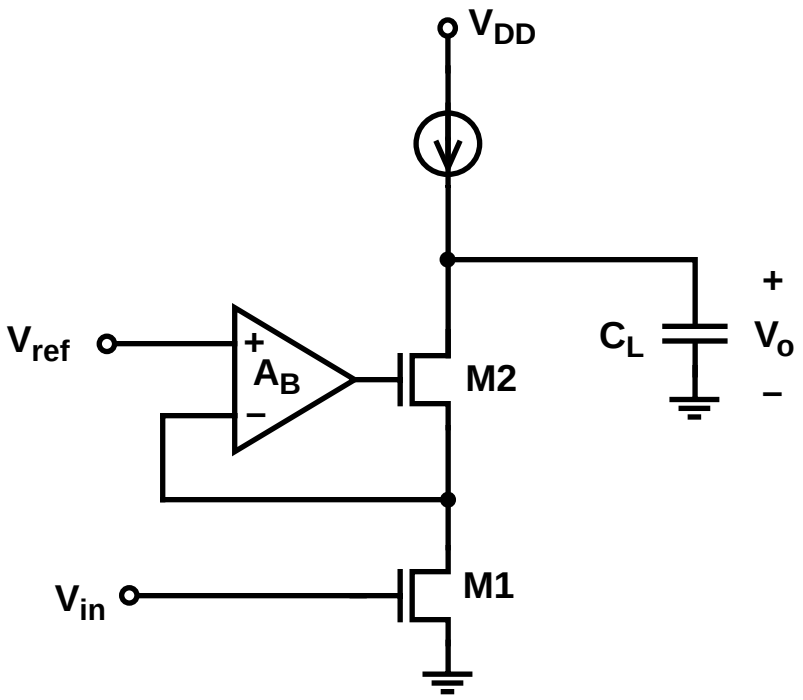
$$A_V(0) = g_{m1} \cdot r_{out}$$

$$r_{out} = (g_{m2}r_{o2} + 1) \cdot r_{o1} + r_{o2}$$

$$\cong g_{m2}r_{o2}r_{o1}$$

$$\therefore A_V(0) \cong g_{m1}g_{m2}r_{o2}r_{o1}$$

"GAIN-BOOSTED" CASCODE (Bult & Geelen, JSSC, 12/90)



$$r_{out} = [g_{m2}r_{o2}(A_B + 1) + 1] \cdot r_{o1} + r_{o2}$$

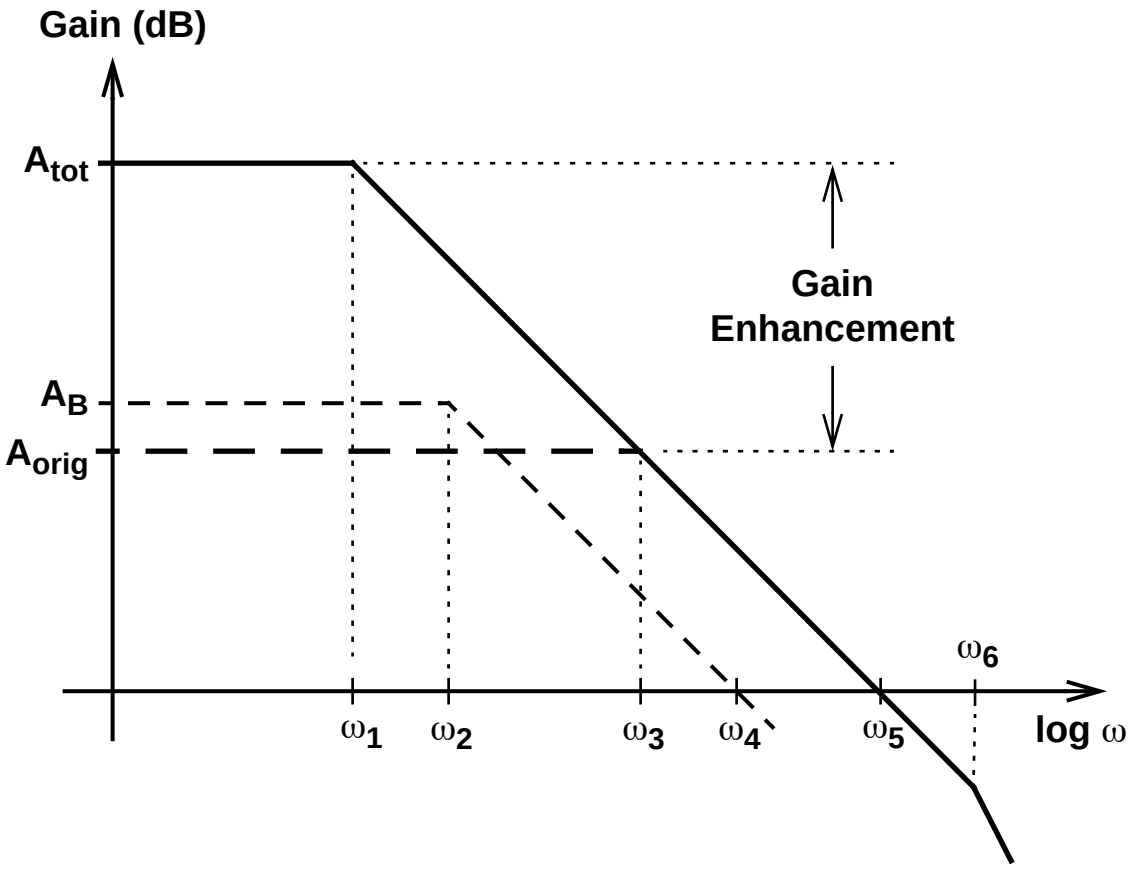
$$\cong g_{m2}r_{o2}A_Br_{o1}$$

$$A_V(0) = g_{m1}r_{out} = g_{m1}g_{m2}r_{o1}r_{o2}A_B$$

The "gain-boosted" cascode boosts the output resistance, and thus the low-frequency gain, by A_B. In comparison with "double cascoding" it provides a larger output swing and improved frequency response (it avoids the introduction of another nondominant pole)

Note: To achieve the increased gain, the output resistance of the "current source" load must be increased to a value comparable to r_{out}.

Frequency Response of Gain-Boosted Cascode



- **Assume a single-pole response for the gain boosting amplifier with the pole at $-\omega_2$ and a unity gain bandwidth of ω_4.**
- **The unity-gain bandwidth, ω_5, of the overall cascode is unchanged and still determined by the load capacitance: $\omega_5 = g_{m1}/C_L$**
- **The total gain, A_{tot}, decreases above ω_1 due to C_L; therefore, $|A_B(j\omega)|$ may decrease above ω_1:**

$$\omega_2 > \omega_1 \Rightarrow \omega_2 \cdot A_B > \omega_1 \cdot A_B \quad \text{(i.e. } \omega_4 > \omega_3\text{)}$$

- **For stability of the local feedback loop, the unity-gain bandwidth of A_B, ω_4, should be less than the magnitude of the nondominant pole associated with M2:**

$$\omega_4 < \omega_6 = g_{m2}/C_{T2}$$

Settling Behavior:

- **The boosted gain is achieved by increasing the output impedance $Z_{out}(j\omega)$ by a factor of approximately $(A_B + 1)$.**
- **Consideration of the total impedance at the output node (including C_L) reveals the presence of a pole-zero doublet near ω_4; such doublets can introduce a slow settling component into the amplifier's response.**
- **The slow settling can be made "fast enough" by ensuring**

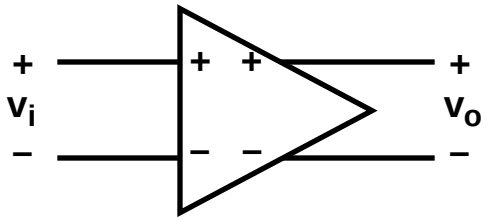
  $$\omega_4 > f\omega_5$$

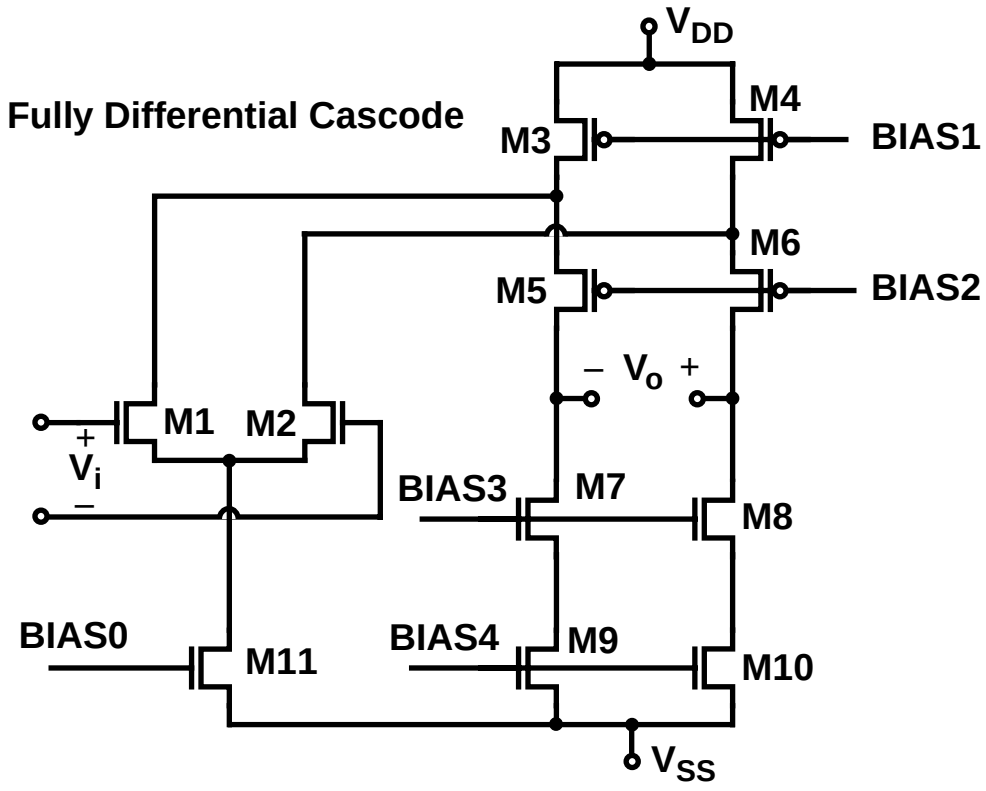
  where ω_5 is the unity-gain bandwidth of the cascode stage and f is the "feedback factor" when the stage is embedded in a closed loop ($f \leq 1$) .
- **For unity gain feedback, f = 1 and**

  $$\omega_5 < \omega_4 < \omega_6$$

Since the gain boosting amplifier need only drive M2, it is not difficult to meet the constraints on its bandwidth. Moreover, it can usually be implemented with smaller devices, and less current, than the main stage. (see the Bult and Geelen reference)

Fully Differential Circuits

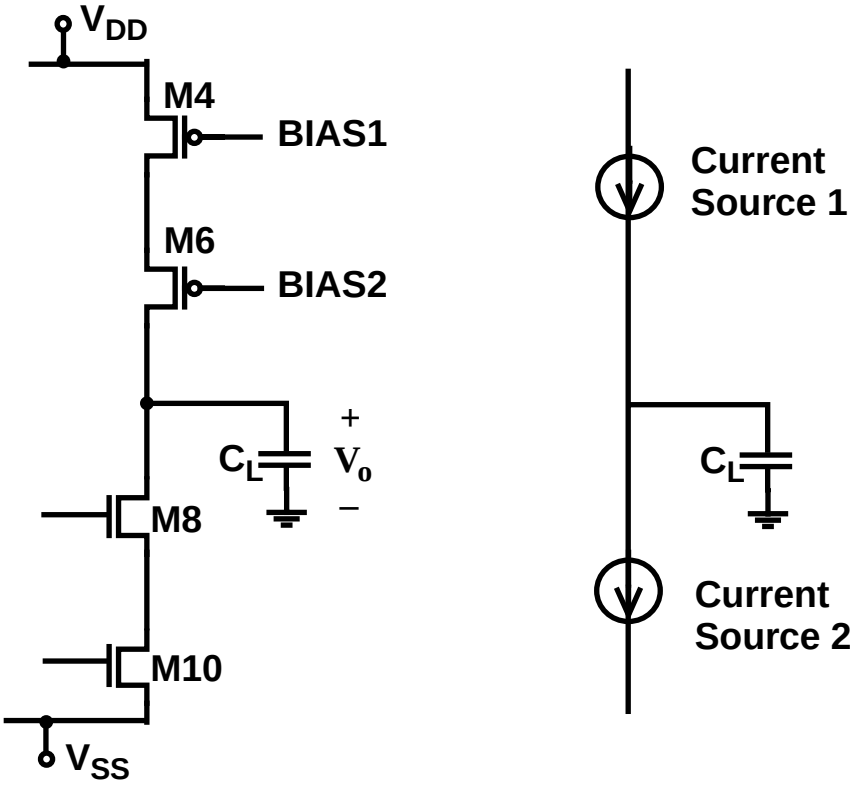




- **High PSRR since supply variations appear as common-mode signals**
- **Effective output swing is doubled, while the input-referred noise is unchanged in comparison with a single-ended output op amp. Therefore, a 6dB increase in maximum dynamic range is achieved**
- **Problem is establishing the dc biasing**

Common-Mode Feedback

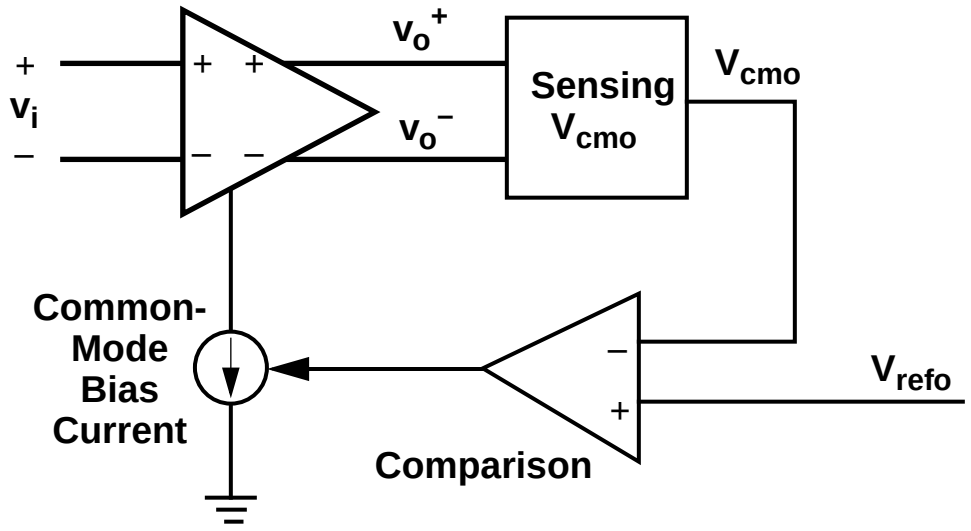
- **In fully differential circuits, the differential feedback does not set the common-mode dc bias points.**
- **Stable dc bias points at the output of a fully differential amplifier requires common-mode feedback.**
- **Without common-mode feedback, the output voltage of a fully differential amplifier is set by the mismatch of two current sources. It typically drifts to either supply rail when one current source moves into triode region.**

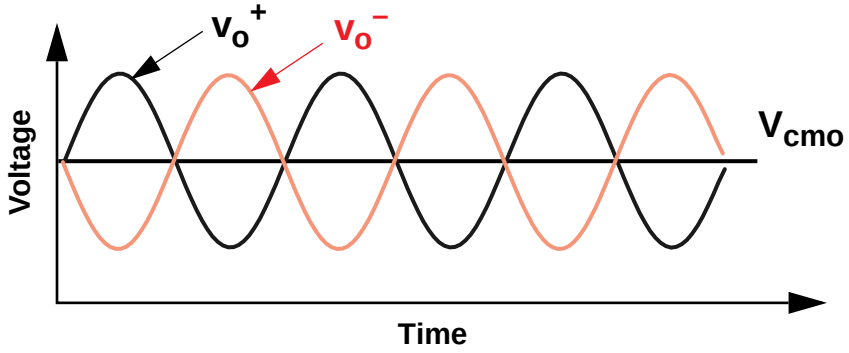


Common-mode feedback has three key components:

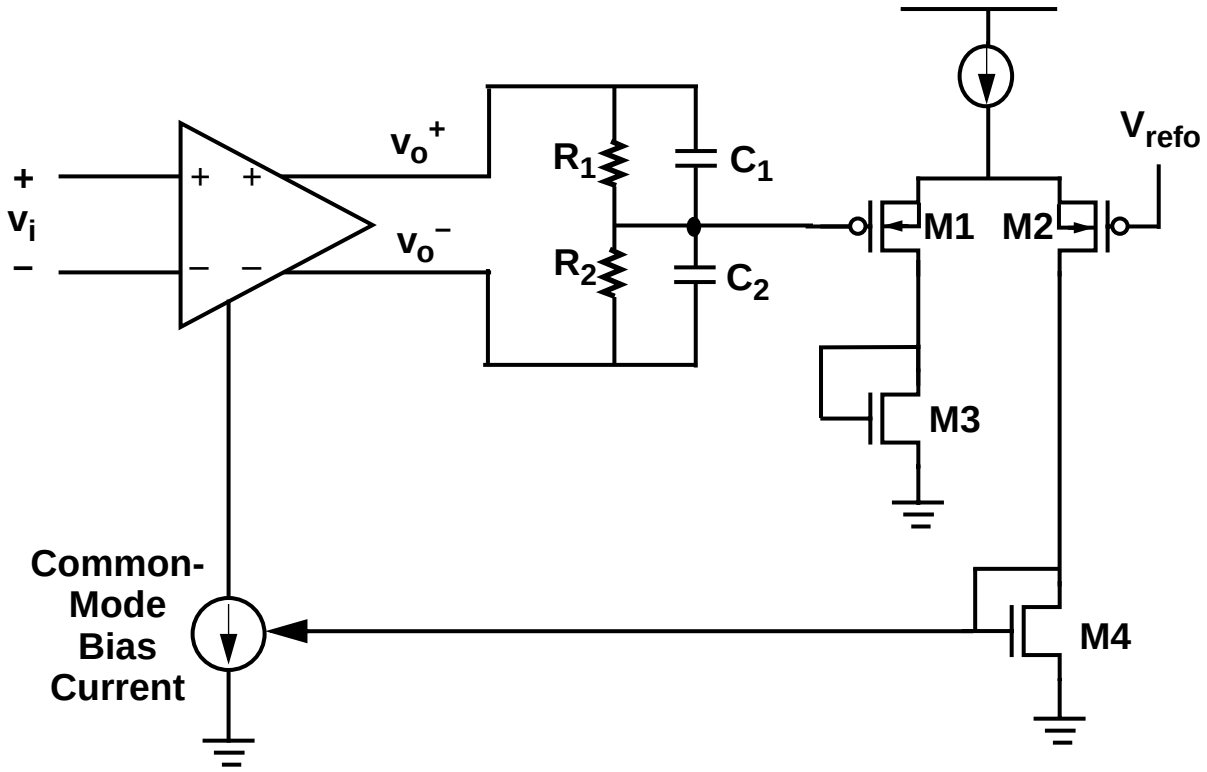
- **sampling of the common-mode output voltage:**
  - **resistor divider**
  - **MOS differential pair**
  - **switched-capacitor circuit**
- **comparison with reference voltage (can be implicit)**
- **feedback of common-mode error signal**
  - **adjust output common-mode voltage via common-mode bias current.**

CONCEPTUAL MODEL



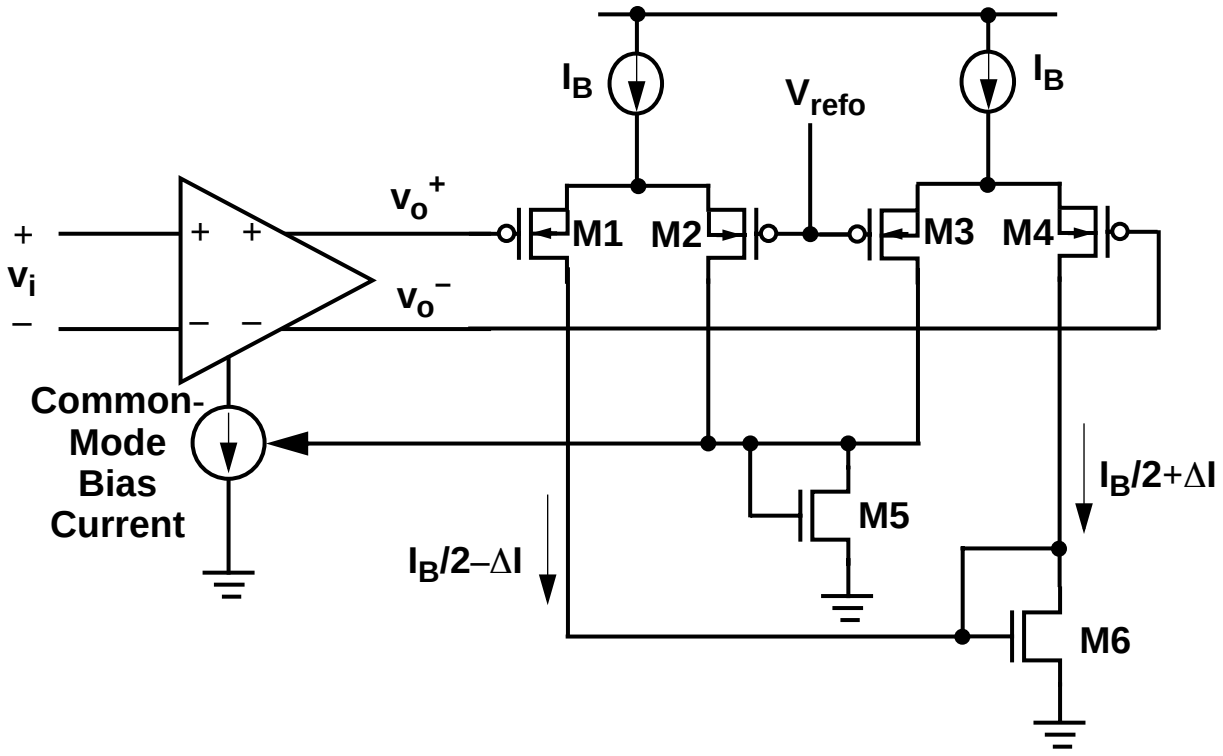


Setting the Common-Mode Output Voltage Using Resistive Dividers (Banu, Khoury, Tsividis, JSSC 12/1988)



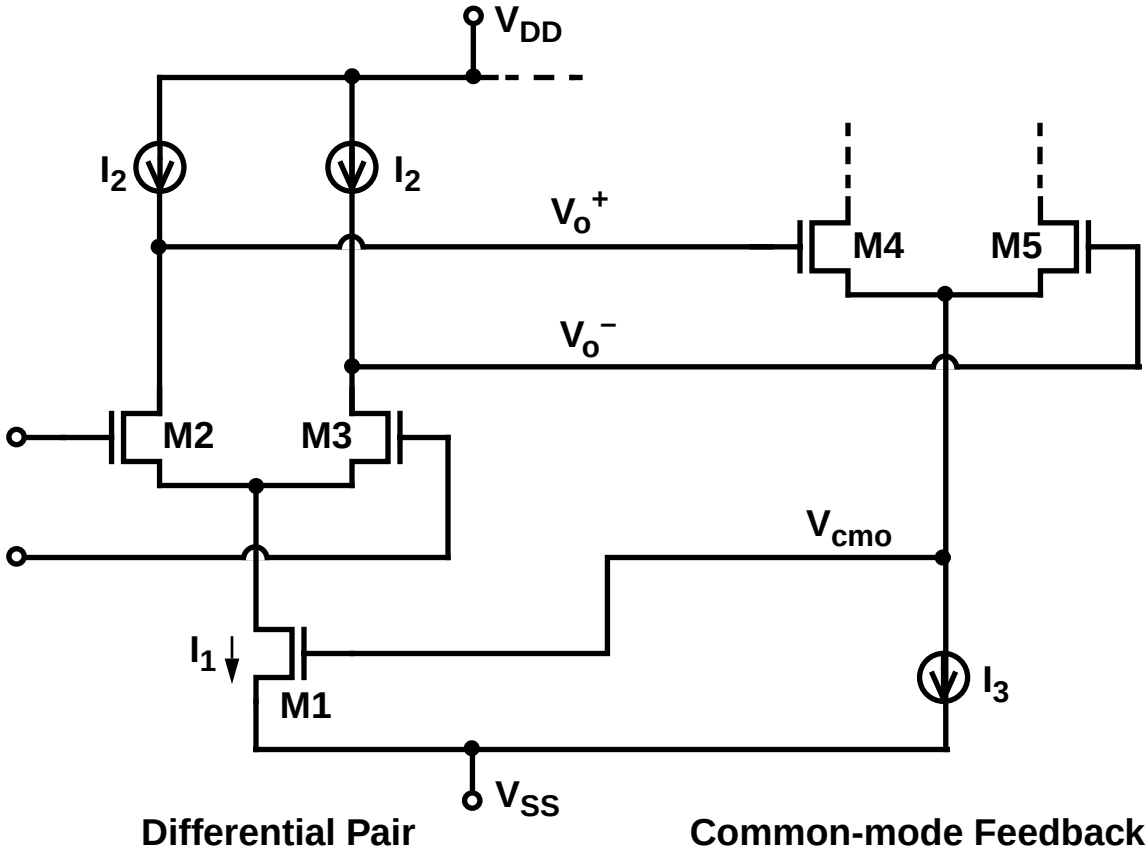
- The common-mode output voltage is sensed using resistive voltage divider. $R_1 = R_2 \sim 40k$. Capacitors C1 and C2 improve the frequency response of the voltage divider.
- The common mode voltage is explicitly compared with a reference voltage V_{refo}.
- The error signal is used to adjust the common-mode bias current via a current mirror (M4).
- The op amp must be able to drive resistive loads. Source followers may be used to buffer the resistive divider if needed. However, these buffers will reduce maximum common-mode output voltage range.
- M1, which must not turn off during operation, will limit common-mode output swing.

Common-Mode Voltage Sensing with Differential Pairs



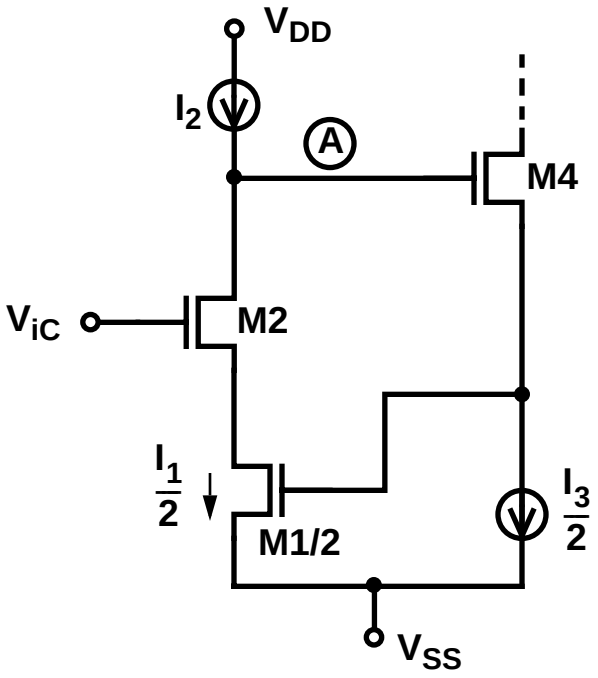
- **Two PMOS differential pairs used for sensing the common-mode output voltage.**
- **The common mode voltage is explicitly compared with a reference voltage V_{refo}.**
- **The error signal is used to adjust the common-mode bias current via a current mirror (M5).**
- **Maximum output common-mode range is limited by M1- M4. M1 through M4 should not turn off during operation. Use of source degeneration resistor can improve output range.**

Common-Mode Voltage Sensing with Source Followers



- **Source follower acts a common-mode sensing circuit.**
- **The common-mode voltage is implicitly compared with desired output voltage by scaling the size of transistor M1.**
- **Current source M1 sets the output common-mode voltage.**

Common-Mode Half Circuit:



Negative feedback forces

$$\frac{I_1}{2} = I_2$$

Then,

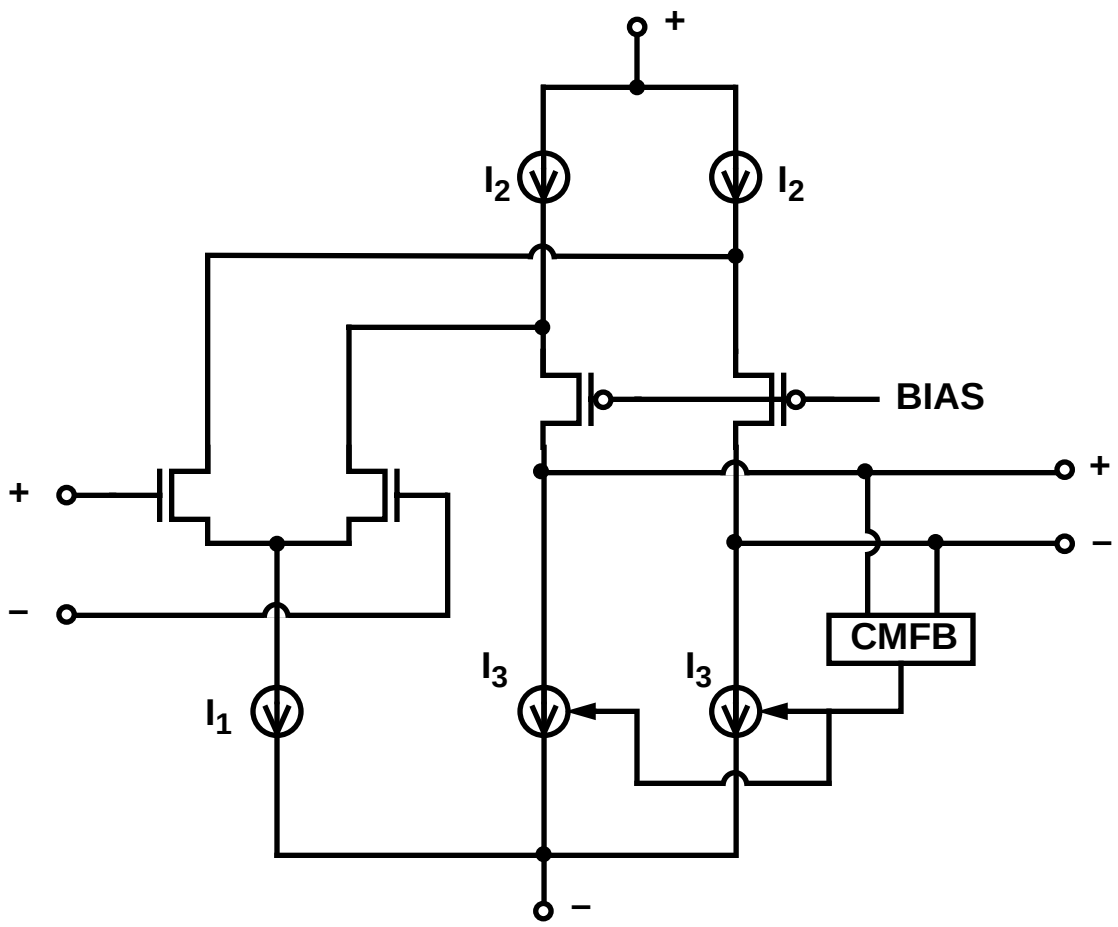
$$V_A = V_{SS} + V_{gs1} + V_{gs4}$$

where

$$V_{gs4} = V_{T4} + \sqrt{\frac{I_3}{k_4}}$$

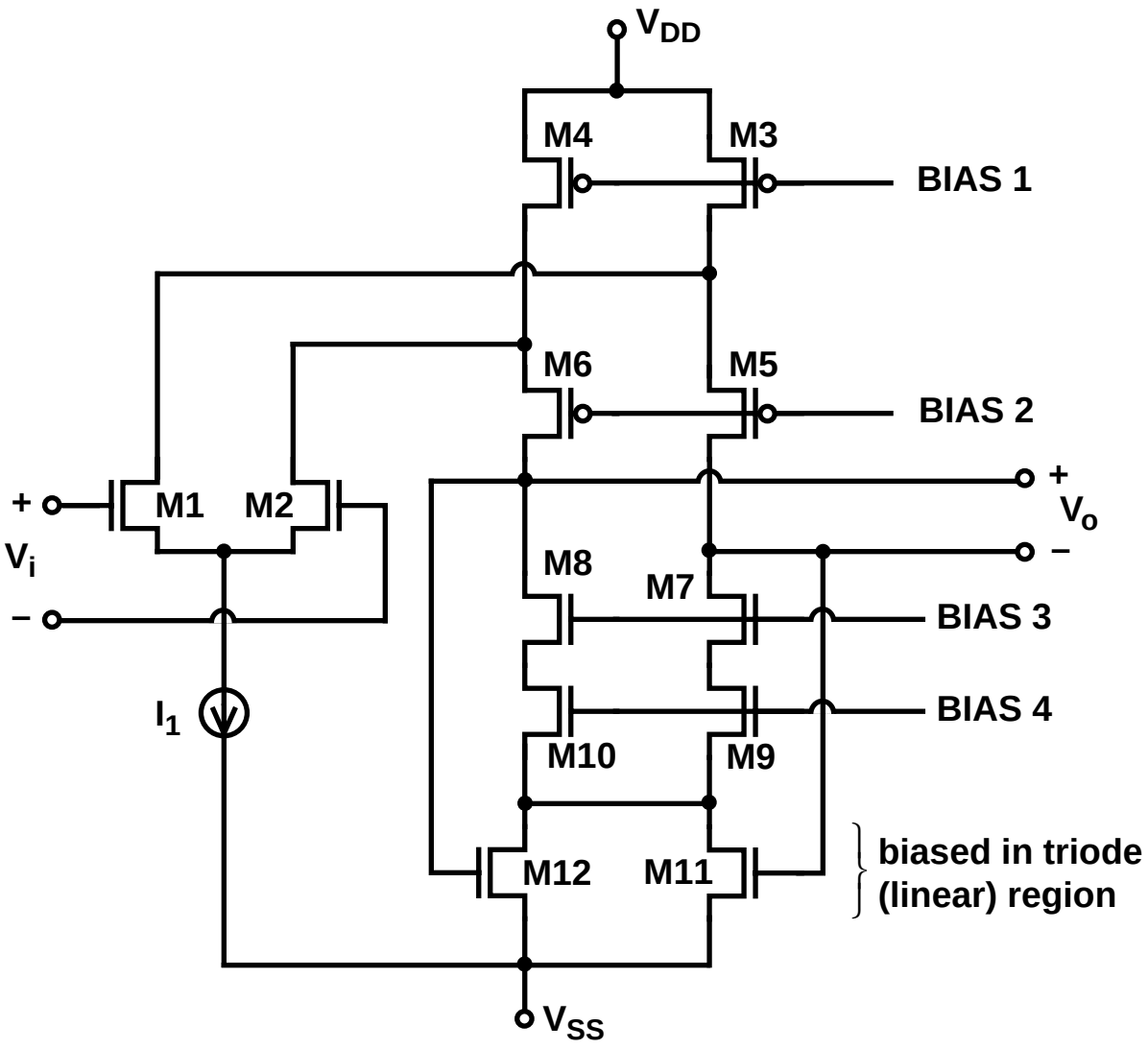
$$V_{gs1} = V_{T1} + \sqrt{\frac{2I_2}{k_1/2}} = V_{T1} + \sqrt{\frac{4I_2}{k_1}}$$

Fully-Differential Folded Cascode



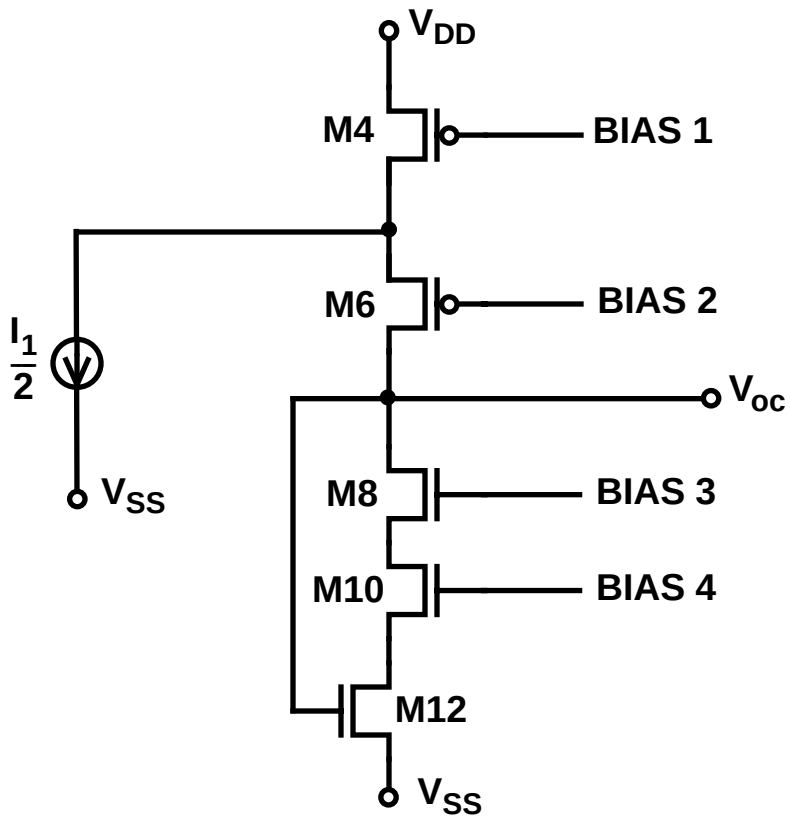
Common-mode feedback modulates I_3 so as to maintain V_{oc}

Common-Mode Voltage Sensing Using Transistors in the Linear Region



M11 and M12, which are biased in the linear region, sense the common-mode output voltage and correspondingly modulate the current in M9 and M10 so as to maintain the desired common-mode output level

Common-Mode Half Circuit:



M12 is biased in the linear region, while M8 & M10 are saturated. Thus, V_{oc} can be determined from the following relationships.

$$V_{oc} = V_{SS} + V_{gs12}$$

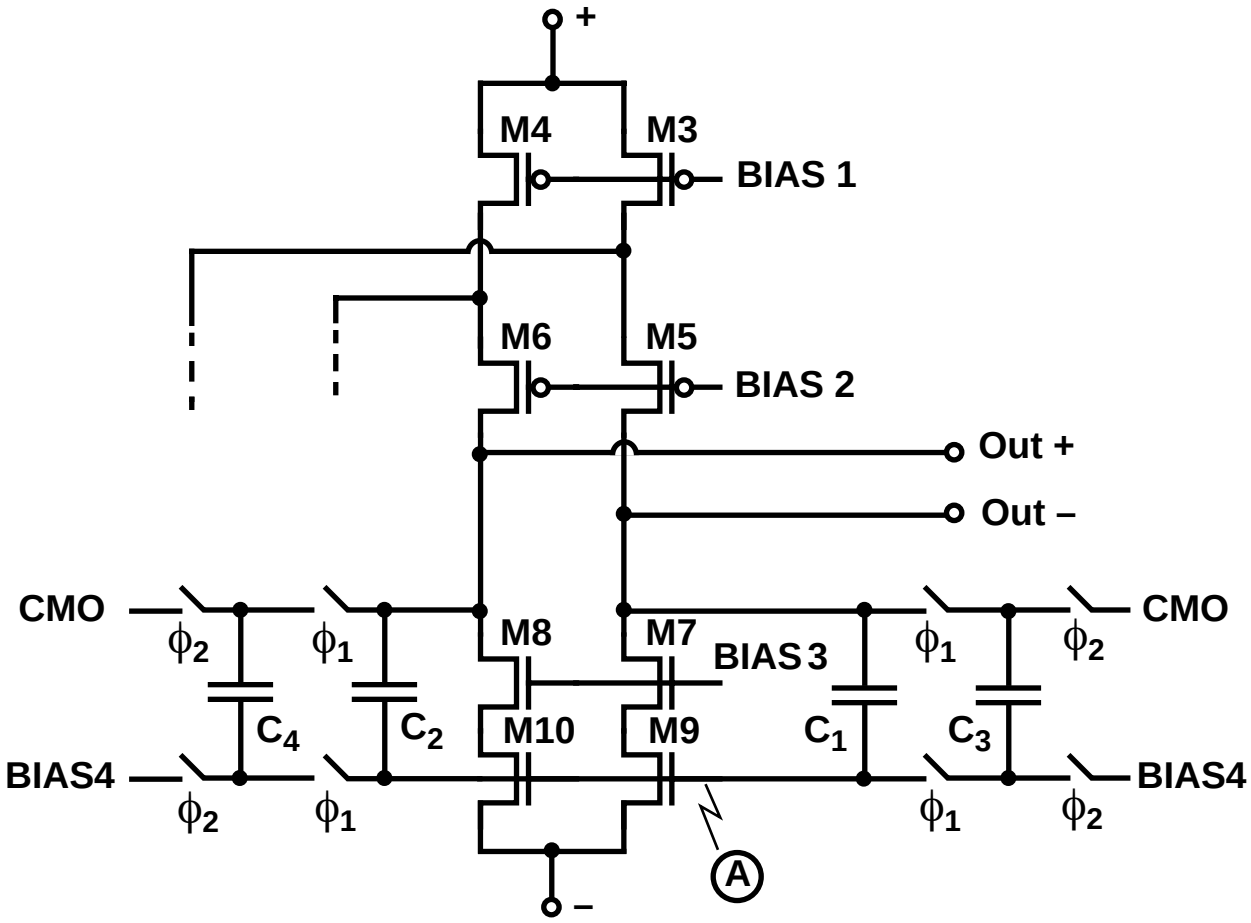
$$I_{d12} = I_{d4} - I_1/2$$

$$I_{d12} = k_{12}\left(V_{gs12} - V_{T12} - \frac{V_{ds12}}{2}\right)V_{ds12}$$

$$V_{ds12} = V_{BIAS4} - V_{gs10} - V_{SS}$$

$$V_{gs10} = V_{T10} + \sqrt{\frac{2I_{d10}}{k_{10}}} = V_{T10} + \sqrt{\frac{2I_{d12}}{k_{10}}}$$

Dynamic Common-Mode Biasing



C_1 and C_2 are nominally equal capacitors that form a voltage divider to sense the common-mode output voltage and level shift that voltage to node A.

Capacitors C_3 and C_4, together with the switches controlled by ϕ_1 and ϕ_2, are used to establish and maintain the desired dc level shift voltage on C_1 and C_2.

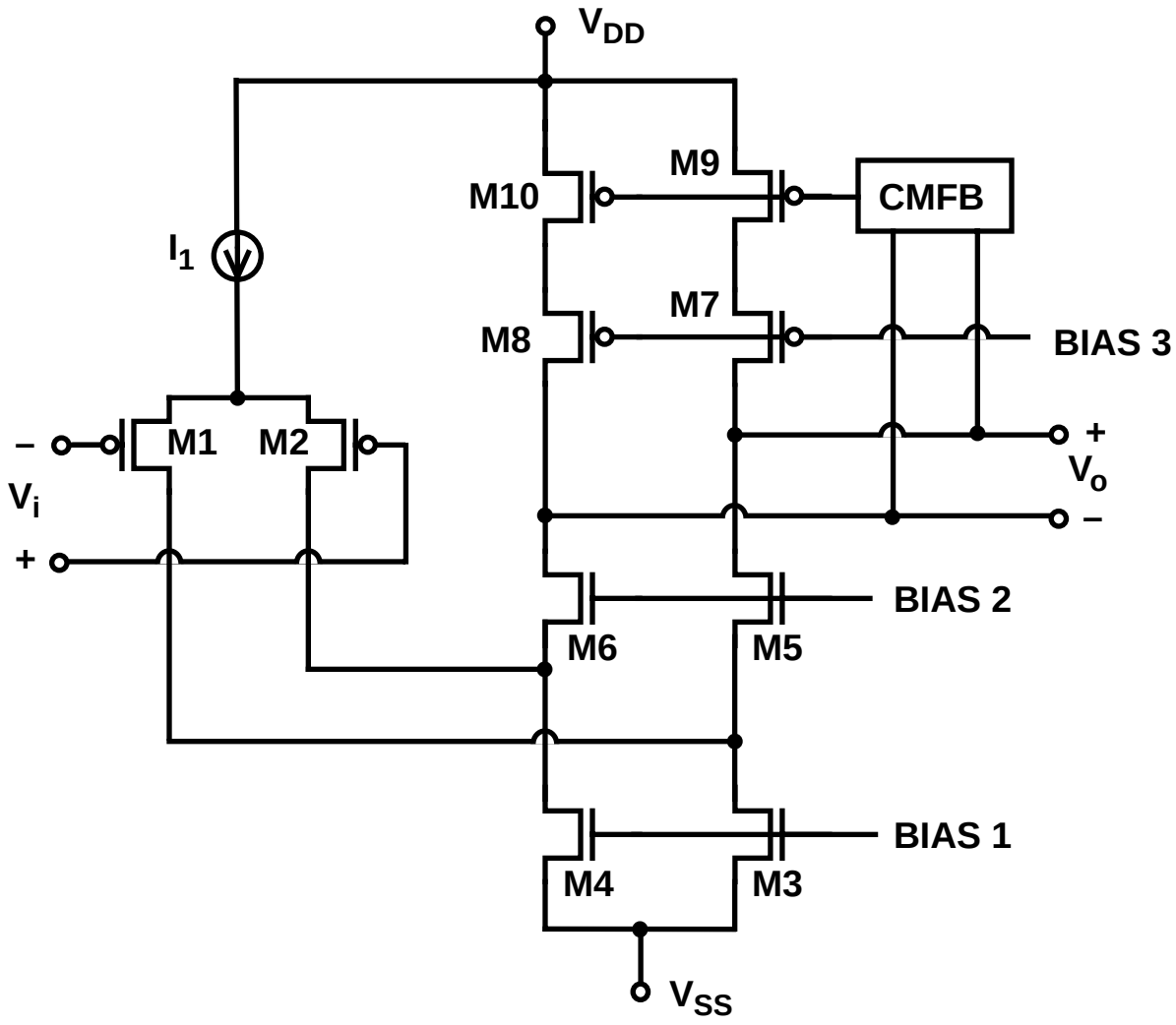
CMO = desired common-mode output voltage

BIAS4 = corresponding bias voltage needed at node A

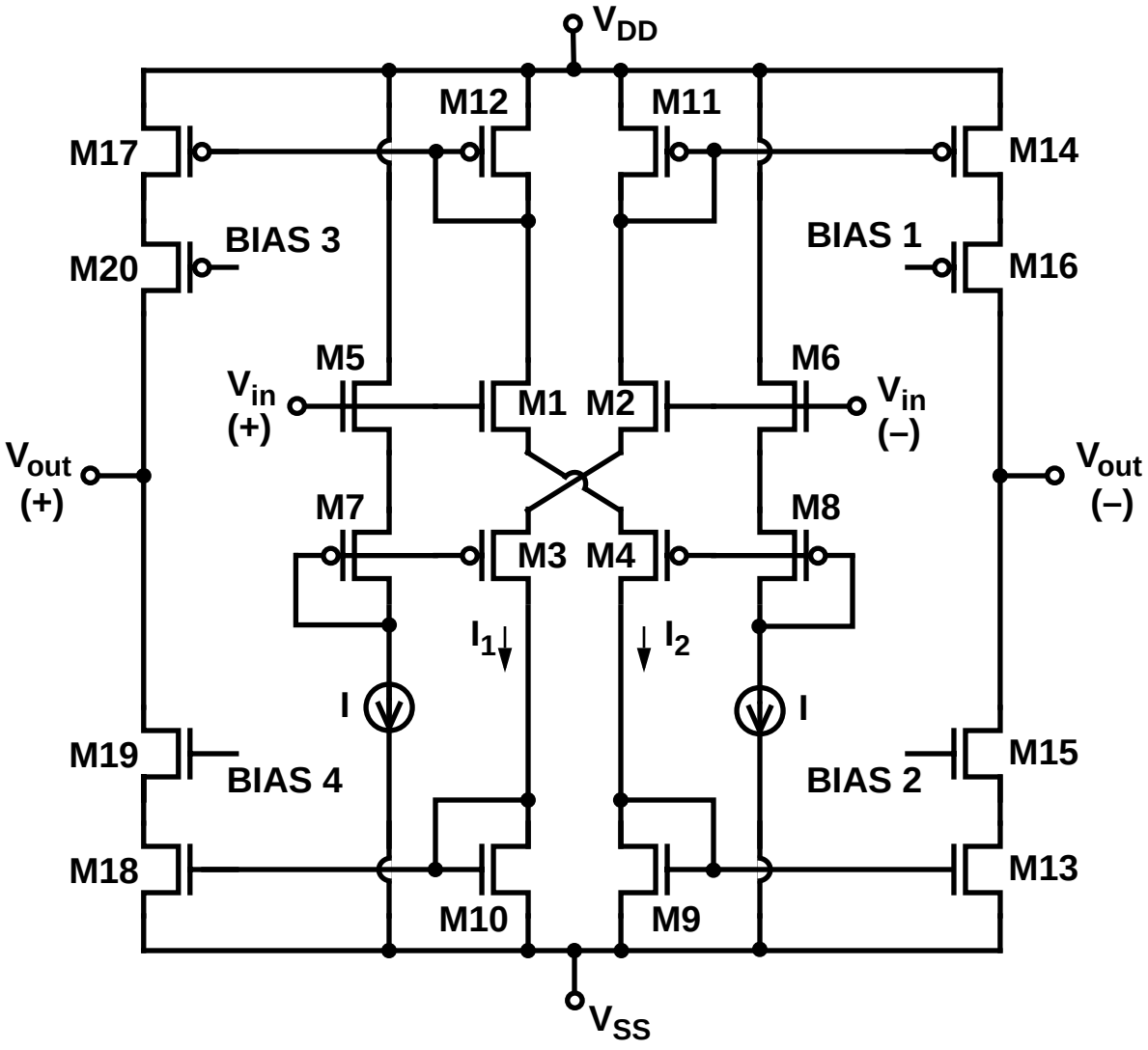
This circuit provides a full rail-to-rail common-mode output range and is widely used in switched-capacitor circuits

In practice, for both folded-cascode and 2-stage op amps a PMOS differential pair is often used for the input stage. PMOS transistors require larger devices to achieve a comparable g_m in the first stage, but:

- **NMOS transistors are then used for either the cascode transistors or the second stage, resulting in a higher unity-gain bandwidth since the lowest nondominant pole is larger.**
- **PMOS devices typically have lower 1/f noise than NMOS transistors**
- **Results in larger input capacitance**



Fully-Differential Class AB Op Amp



If M1, M2, M5 and M6 are identical and M3, M4, M7 and M8 are identical, then when $V_{in}(+) = V_{in}(-)$

$$I_1 = I_2 = I$$

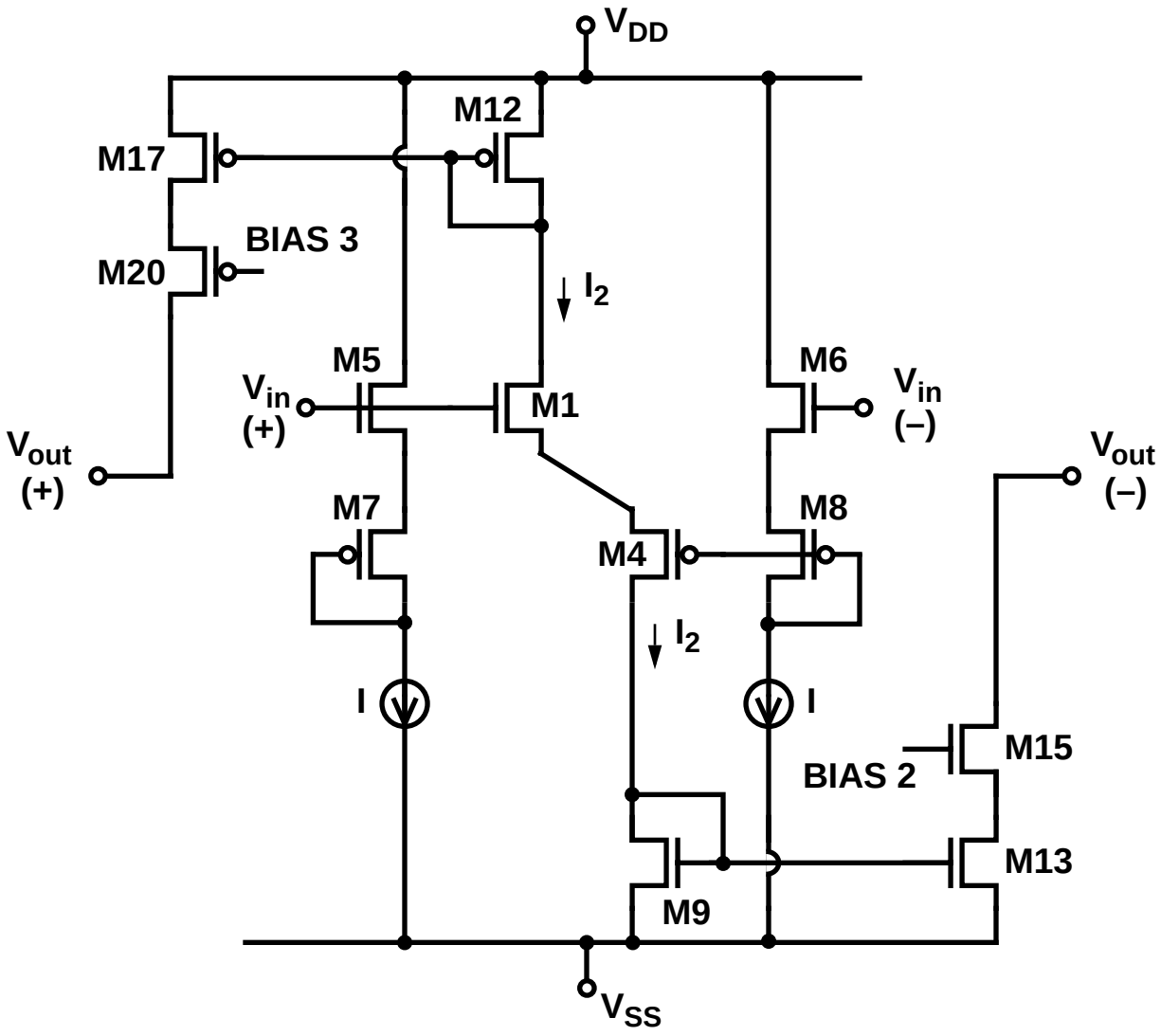
Furthermore, if the current mirrors have a gain of 1, then

$$I_{d20} = I_{d16} = I$$

and

$$I_{DD} = 6I$$

For a large positive differential input, half of the circuit is cut off and the active portion of the circuit becomes:



SELECTED OPERATIONAL AMPLIFIER REFERENCES

1. P. R. Gray and R. G. Meyer. “MOS Operational Amplifier Design - A Tutorial Overview,” *IEEE J. of Solid-State Circuits*, vol. SC-17, pp. 969-982, Dec. 1982.

2. K. Bult and G. J. Geelen, “A Fast-Settling CMOS Op Amp for SC Circuits with 90-dB Gain,” *IEEE J. of Solid-State Circuits*, vol. 25, pp. 1379-1384, Dec. 1990.

3. R. Castello and P. R. Gray, “A High-Performance Micropower Switched-Capacitor Filter,” *IEEE J. of Solid-State Circuits*, vol. SC-20, pp. 1122-1132, Dec. 1985.